Fifth Quarterly Report

for

PHOTON-COUPLED ISOLATION SWITCH

(1 January to 31 March 1967)

Contract No. 951340

Prepared by

E. L. Bonin

of

Texas Instruments Incorporated
Semiconductor-Components Division
Post Office Box 5012
Dallas, Texas 75222

for

Jet Propulsion Laboratory
California Institute of Technol
4800 Oak Grove Drive
Pasadena, California 91103

Fifth Quarterly Report

for

PHOTON-COUPLED ISOLATION SWITCH

(1 January to 31 March 1967)

Contract No. 951340

Prepared by

E. L. Bonin

of

Texas Instruments Incorporated
Semiconductor-Components Division
Post Office Box 5012
Dallas, Texas 75222

for

Jet Propulsion Laboratory
California Institute of Technology
4800 Oak Grove Drive
Pasadena, California 91103

ABSTRACT

A new integrated circuit switch device, called the Photon-Coupled Isolation Switch, is being developed. This device exhibits electrical isolation between the output switch terminals and the driving source by using internal photon generation and detection techniques. The Isolation Switch consists of a monolithic silicon (Si) integrated circuit, a gallium arsenide (GaAs) photon emitting diode, and a Si phototransistor in a single integrated circuit package. The integrated circuit supplies forward bias for the GaAs diode and, with DTL circuitry, has provision for up to 10 inputs. The GaAs diode is optically coupled to the phototransistor which acts as the electrically isolated output switch.

The program is divided into two phases:

Phase I, design and breadboarding of the driver circuit and development of the GaAs emitting diode-Si phototransistor pair (GaAs Switch).

Phase II, integration of the driver circuit and prototype production of the complete Isolation Switch.

Previously, under Phase I, the GaAs Switch was developed and the design and breadboard evaluation of the driver circuit were largely completed. During the last quarter of the program, twenty GaAs Switches were shipped to JPL for evaluation. Also, modifications of the driver circuit design were made to allow use of improved, lower-forward-voltage-drop GaAs emitting diodes and of base-type diffusions for all integrated circuit resistors. This marks completion of Phase I.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION I

INTRODUCTION

The capability to couple signals between circuits operating at different d-c potentials is not available in conventional integrated circuits. This highly desirable transformer function cannot be provided effectively with conventional processing techniques. Electrical isolation is being achieved in the present contract, however, by using photon coupling between solid-state light-emitting and photodetecting devices. Efficient signal coupling is being obtained using a gallium arsenide (GaAs) P-N junction emitting diode and a silicon (Si) P-N junction photodetector, both of which have photo responses which peak near 0.9 μm at 25°C. Previous devices developed which use the GaAs-Si optical pair include an isolated-input transistor, an isolated-gate P-N-P-N type switch, a multiplex switch requiring no driving transistor, and an isolated-input pulse amplifier. [1,2]

The device now under development combines three semiconductor chips: a monolithic Si integrated circuit, a GaAs emitting diode, and a Si phototransistor. The integrated circuit chip consists of a DTL gate which is designed to supply forward bias to the GaAs diode. Inputs (up to 10) are applied to the driver circuit which thereby biases the GaAs diode into the photon-emitting mode. The emitting diode is optically coupled to the phototransistor with a high-refractive-index glass. Light absorption by the phototransistor, primarily near the collector-base P-N junction, biases the transistor as would electrical biasing of the base. However, using optical techniques, the output transistor is electrically isolated from the driving source.

The development program is divided into two phases. Phase I is concerned with the development of the emitting diode-phototransistor pair (GaAs Switch) and the design

and breadboard testing of the driver circuit. In Phase II, the driver circuit is integrated in a monolithic Si wafer and the three device chips are combined in an integrated circuit package (Isolation Switch). Previously, under Phase I, the GaAs Switch was developed. Modifications were required for the initial transistor design to eliminate inversion layer formation on the transistor surface. Although the inversion layers were not formed when the transistor was operated alone, they developed at high temperatures after the GaAs diode was bonded to the transistor with optical coupling glasses. Transistors built with the modified design demonstrated the desired ranges for leakage current, breakdown voltage, and current gain. Also in previous periods, the design of the driver circuit was nearly completed.

In the last quarter of the program, GaAs Switches were tested according to the requirements of the Isolation Switch. Twenty devices were shipped to JPL for evaluation. Changes were also made in the design of the driver circuit to allow use of GaAs diodes with lower forward voltages and to use base-type diffusions for all resistors. The latter allows a greater tolerance for important circuit parameters. A detailed analysis was made of the saturation voltage characteristics of the driver circuit transistors. Also analyzed were the effects of using active transistors in the input of the driver in place of the diode gates.

SECTION II

TECHNICAL DISCUSSION

A. PHASE I GaAs SWITCH

1. Construction

Each GaAs Switch consists of a GaAs light emitting diode optically coupled with a high-refractive-index S-Se-As glass to a high-gain Si phototransistor, as shown in Figure 1. The package used is the JEDEC type TO-89, 1/8- x 1/4-inch integrated circuit flat-pack. Of twenty GaAs Switches delivered under Phase I of the program, ten were internally encapsulated with an epoxy for added structural rigidity, as previously described.[1,2] After lids were welded on each package, hermetic sealing was tested using Radiflo which indicated leakage rates less than 10^{-8} cc/s air and also using a bubble test in 65°C alcohol which indicated no gross leakages.

2. Electrical Testing

Measured data for the twenty GaAs Switches delivered are shown in Table I. The measuring circuits are indicated in Figures 2 and 3. The collector-emitter saturation voltage V_{CES} and collector current I_C were measured using previously derived worst-case minimum values for the light-emitting diode current I_F of 24.5, 24, and 22 mA at −20, 25, and 100°C, respectively. As shown in Table I, V_{CES} increases with increasing temperature. The greatest value for the units is 0.24 V compared to the specification of 0.6 V maximum.

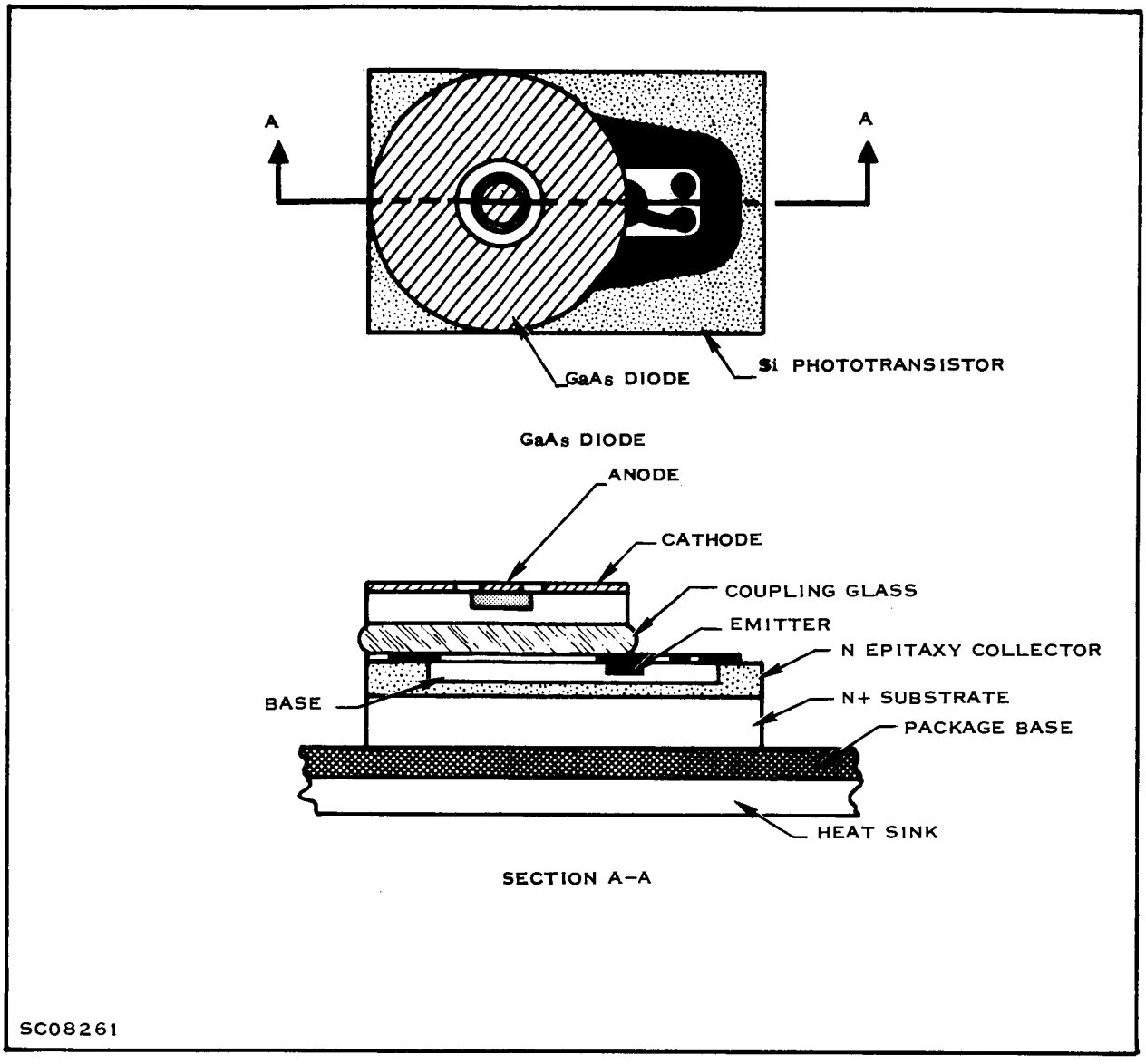

Figure 1. GaAs Switch Construction

Current I_C is minimum at 100°C. The smallest value shown for the devices is 16 mA, with 19 of the devices having an I_C of 22 mA or greater. This compares to an acceptable minimum of 15 mA at the worst-case temperature of 100°C. [2/]

Collector-emitter leakage current I_{CEO} is maximum at 100°C. Two of the devices have values above the 10-μA tentative maximum value. [2/] The 10-μA limit seriously limited yields. For units tested which were otherwise good, only about half had leakages below 10 μA. About three-fourths had leakages below 20 μA.

Table I. Data for Phase I Devices Shipped

Parameter	V_{CES}			I_C			I_{CEO}		BV_{CEO}		C_{iso}	t_1	t_2	V_{n1}	V_{n2}
Units	V			mA			μA		V		pF	μs	μs	V	V
Conditions	I_F = W.C.* I_C = 10 mA			I_F = W.C.* V_{CE} = 0.6 V			V_{CE} = 20 V		I_C = 100 μA		f = 1 kHz	—	—	v_i = 5 V	v_i = −5 V
T_A(°C)	−20°C	25°C	100°C	−20°C	25°C	100°C	25°C	100°C	25°C	100°C	25°C	25°C	25°C	25°C	25°C
Device No.	With No Epoxy														
5	0.09	0.16	0.18	40	35	25	0.0012	4.1	71	66	2.3	3.1	59	1.7	1.6
8	0.11	0.13	0.20	35	32	22	0.00013	1.5	75	72	2.1	3.5	52	1.8	1.5
10	0.08	0.11	0.16	42	37	26	0.0014	5.6	64	61	2.8	3.6	20	1.8	1.5
12	0.10	0.12	0.18	34	32	24	0.0009	3.1	64	60	2.3	3.6	56	1.7	1.6
13	0.08	0.10	0.16	45	39	28	0.0005	2.4	70	66	2.0	2.7	64	1.8	1.6
14	0.10	0.12	0.17	40	36	26	0.0038	8.4	61	55	2.3	3.1	68	1.7	1.6
29	0.09	0.11	0.16	39	37	26	0.0005	2.4	65	62	2.5	2.7	56	1.7	1.6
31	0.09	0.11	0.16	38	37	26	0.0002	2.4	55	53	2.3	2.9	63	1.7	1.6
32	0.10	0.12	0.17	35	35	25	0.0011	4.4	84	68	1.8	2.5	49	1.8	1.7
34	0.10	0.14	0.17	34	25	25	0.0003	2.8	77	69	2.0	3.3	46	1.8	1.7
	With Epoxy														
18	0.11	0.14	0.20	32	31	23	0.0013	3.4	78	67	3.0	2.7	29	1.7	1.6
19	0.09	0.11	0.17	37	35	25	0.0006	4.8	57	54	2.0	3.0	62	1.7	1.6
21	0.09	0.11	0.17	39	36	26	0.0005	6.2	60	57	2.3	2.9	70	1.7	1.5
22	0.09	0.11	0.16	39	36	26	0.0002	1.7	64	61	2.6	2.9	52	1.7	1.6
23	0.09	0.12	0.17	37	34	25	0.0001	0.07	65	63	1.8	2.8	54	1.7	1.6
24	0.09	0.11	0.16	42	37	26	0.0009	3.6	54	52	1.9	2.8	74	1.7	1.6
25	0.09	0.11	0.17	41	37	25	0.0013	4.7	58	55	2.1	2.7	62	1.7	1.5
39	0.10	0.12	0.18	32	32	24	0.0039	10.6	64	59	3.4	5.1	56	1.7	1.5
41	0.11	0.14	0.20	29	29	22	0.0050	10.0	71	62	6.4	4.0	33	1.6	1.4
46	0.14	0.16	0.24	18	20	16	0.0051	12.2	85	66	2.0	6.6	30	1.9	1.7

* Worst Case Values: T_A = −20°C 25°C 100°C
I_F = 24.5 mA 24 mA 22 mA

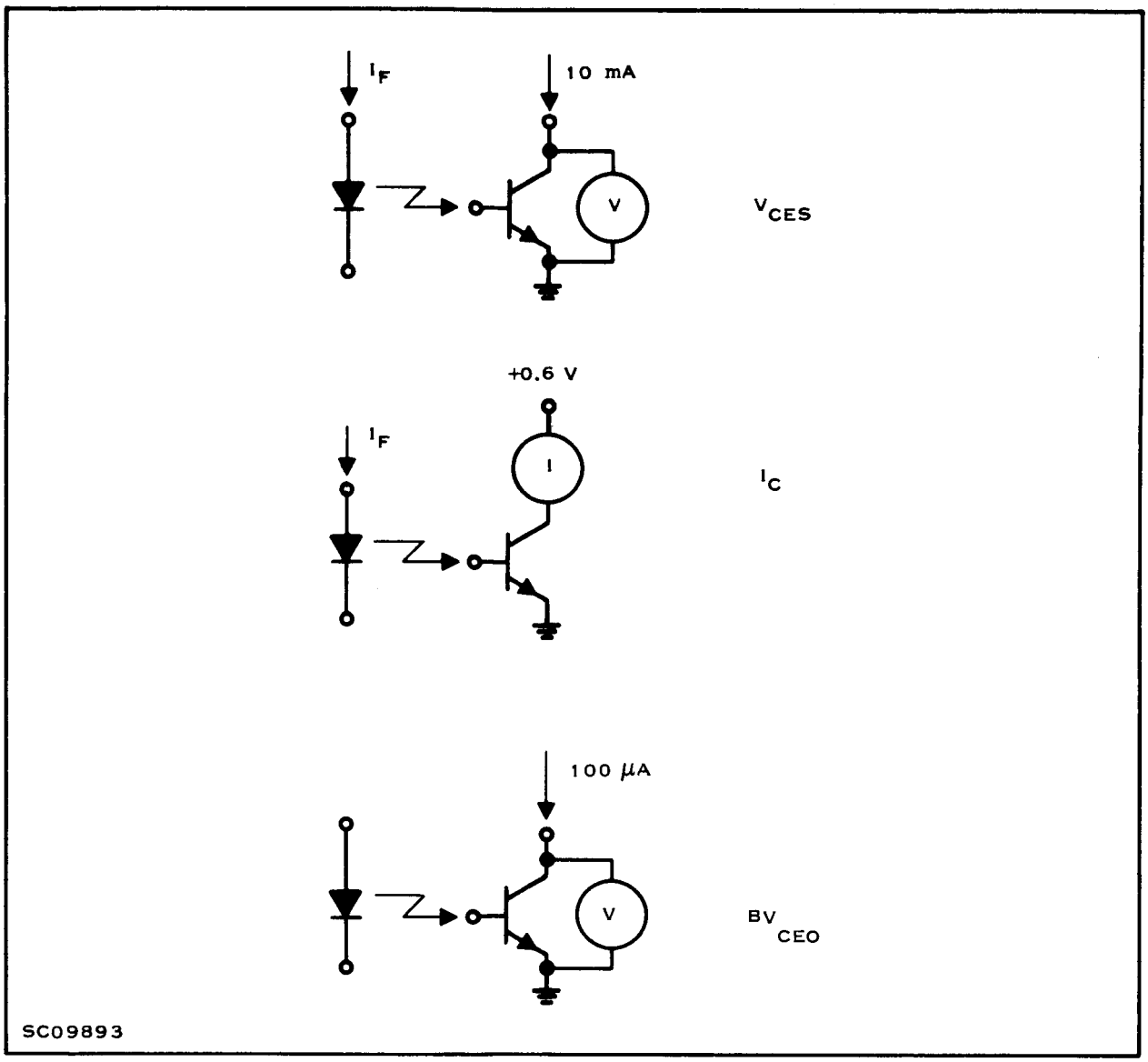

Figure 2. Measuring Circuits for V_{CES}, I_C, and BV_{CEO}

The collector-emitter breakdown voltages BV_{CEO} for the devices were above 52 V at 100°C and greater for the reduced temperatures compared to the specification of 35 V minimum.

The isolation capacitance C_{iso} is a maximum of 6.4 pF, measured between the terminals of the light emitting diode and the collector and emitter terminals of the transistor. Most values are below 3 pF. This compares to the specification of 10 pF maximum for the Isolation Switch.

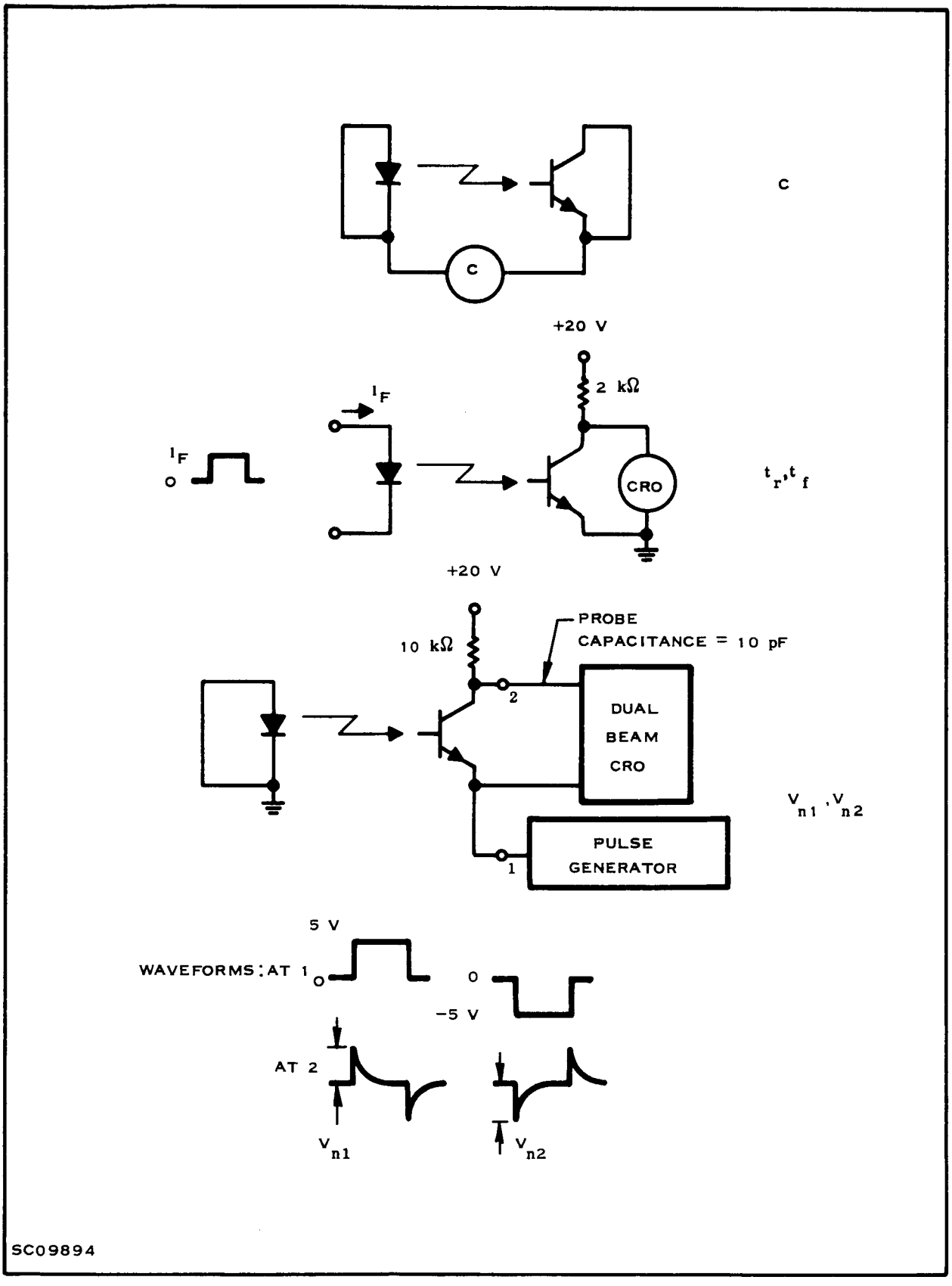

Figure 3. Measuring Circuits for C, t_r, t_f, V_{n1} and V_{n2}

Total rise and fall times, t_1 and t_2, had maximum values of 6.6 and 74 μs, respectively, compared to specifications of 10 and 100 μs maximum. Noise transmissibility was a maximum of 1.9 V compared to the specification of 2.0 V maximum. The measured values are actually conservative, since measuring jig capacitances tend to increase the values somewhat.[2/]

3. Environmental Testing

Nineteen GaAs Switches having epoxy encapsulation and eleven without epoxy were subjected to vibration consisting of thirty five g's of rms vibration swept sinusoidally from 20 to 2000 Hz and then returned to 20 Hz during a 15-minute period. The devices were hard mounted in each of three mutually perpendicular planes. All of the devices passed the test without lead rupture or significant change in the optical coupling. The relative optical coupling was determined by measuring the collector-base current with forward bias applied to the light-emitting diode.

The devices were then subjected to temperature cycling. Each of 10 cycles consisted of 15 minutes at −65°C, 5 minutes at +25°C, 15 minutes at +200°C, and 5 minutes at +25°C in immediate succession. Of the 19 epoxied devices, 7 passed without lead rupture or change in optical coupling. Of the 12 others, one or more leads were ruptured. Of the 11 devices without epoxy, no lead ruptures were exhibited. However, only 1 had no change in optical coupling. The other 10 exhibited an optical coupling reduction of over 90%. For the unepoxied devices, these results are in agreement with previous observations of the softness of the coupling glass at high temperatures.[1/] The glass with the greater operating temperature is being used. Additional testing is being performed to adequately define the usable operating temperature range for the device.

B. DRIVER CIRCUIT

1. Design Analysis

The driver circuit has been re-analyzed to increase the allowable forward voltage range for the GaAs emitting diode. A significant fraction of GaAs diodes now fabricated have forward drops somewhat below the range used for the original design. The new tolerance range generously allows for further improvements. The new driver circuit design also uses base-type diffusions for all resistors. The lower temperature coefficient of resistance compared to those of collector- and emitter-type diffusions allows a greater tolerance for all important parameters in the circuit.

It was also found in the course of the driver circuit analyses that the photo-induced leakage in the phototransistor, as a result of the small current in the GaAs diode in the off-condition, could be significantly reduced either by the addition of a resistor shunting the GaAs diode or the use of an active transistor in place of each input diode. The resistor shunt was selected on the basis of simplicity, reliability and device yields. An analysis for an active input transistor is described in a following section. Also, in the following section, a detailed analysis of the saturation voltage characteristics of the driver-circuit transistors is described.

The basic driver circuit is shown in Figure 4. It is expected that small changes will be made in the nominal resistor values when the integrated circuit layout is made in Phase II of the program. These changes will be the result of adjusting resistor lengths to even-dimensional increments. Final component values will be given in the next interim report.

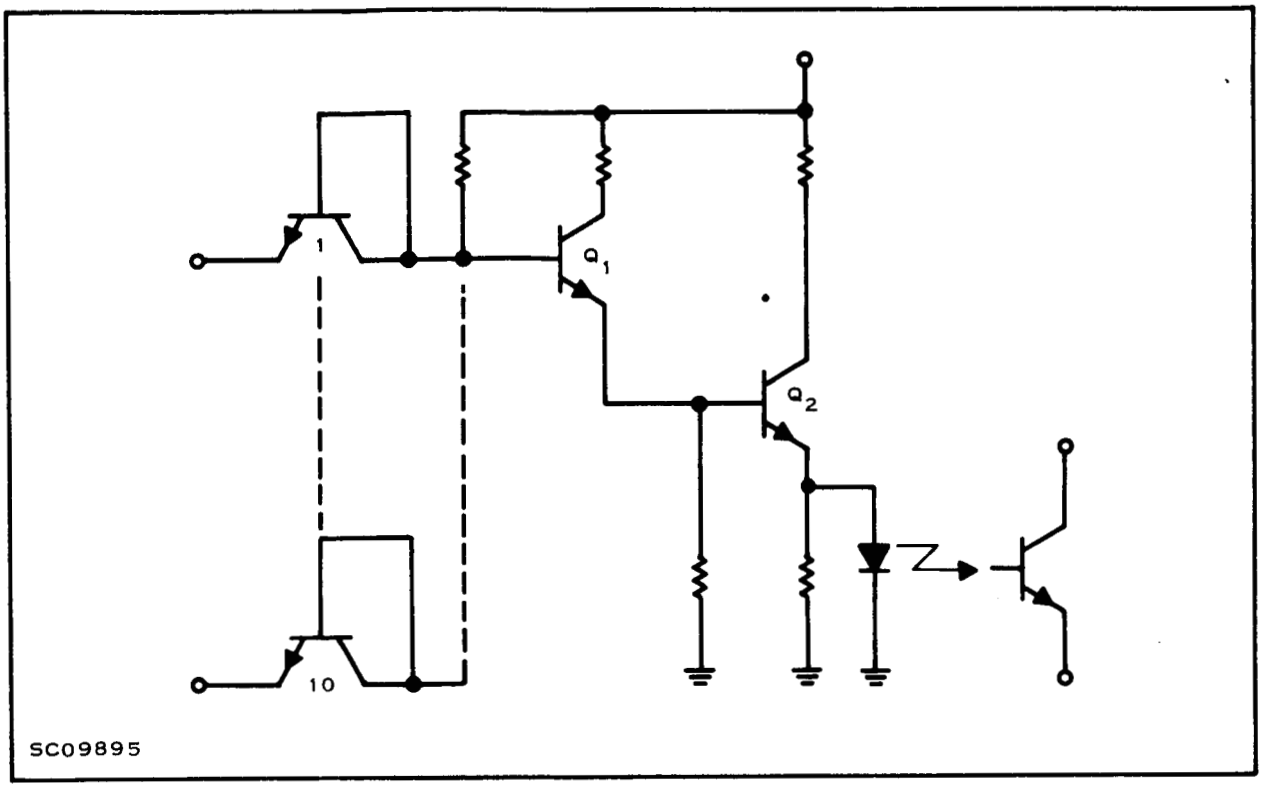

Figure 4. Basic Driver Circuit

2. Transistor Characterization

The test circuit used to characterize the saturation characteristics of driver circuit transistors is shown in Figure 5. In this circuit, common-base connections of PNP transistors are used as constant-current sources for the base and collector currents of the transistor under test. Emitter current is measured with meter A. Meter G is an electronic null meter. Resistors R_B and R_C are precision decade resistance units. Voltages V_{CE} and V_{BE} are measured using a voltmeter with an input impedance of 200 megohms. These voltages are measured as functions of the ratio of collector to base currents I_C/I_B and emitter current I_E. The independent variables I_C/I_B and I_E were chosen because V_{CE} and V_{BE} are slowly changing functions of these variables.

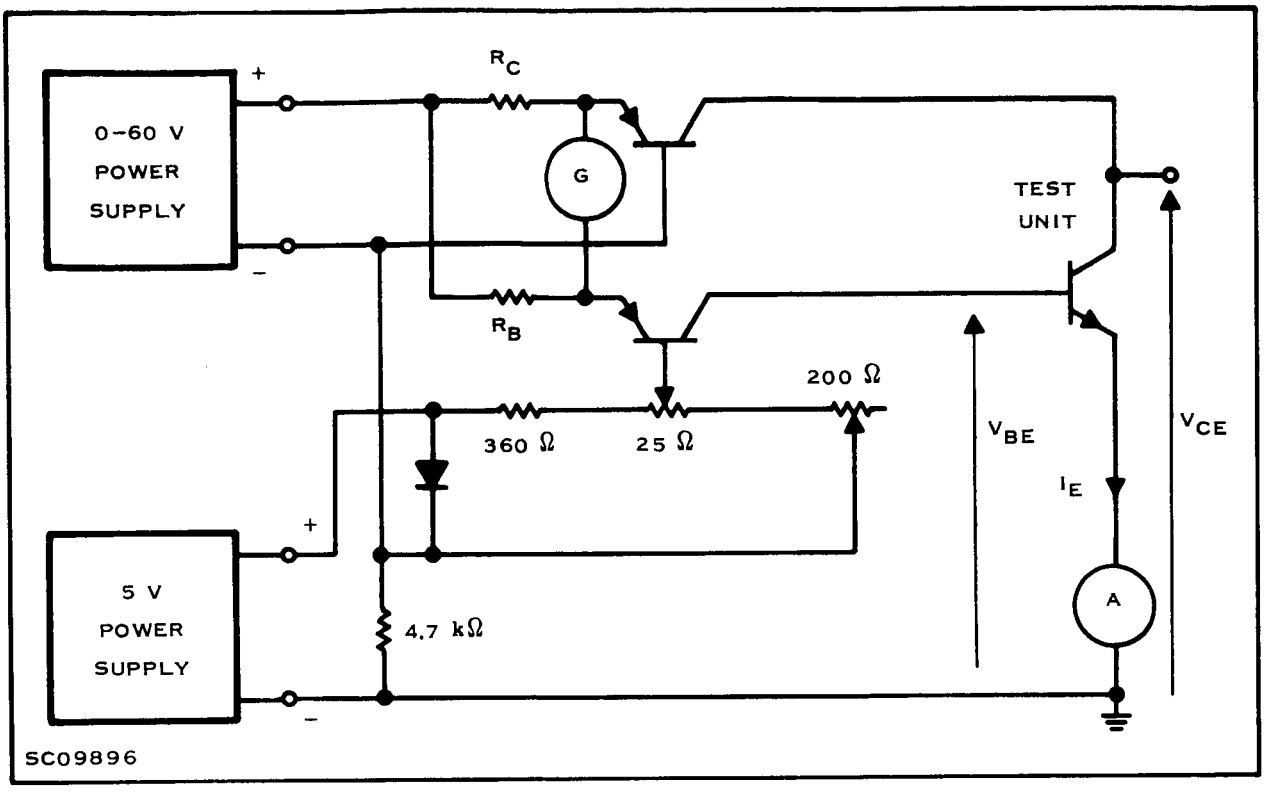

Figure 5. Transistor Saturation Characteristics Test Circuit

The measurement procedure begins with the selection of I_C/I_B. Resistors R_B and R_C are set so that R_B/R_C is equal to I_C/I_B. Then the variable power supply is adjusted to set the desired emitter current I_E. The 200-ohm and 25-ohm variable resistors are adjusted to null meter G. Usually, after the power supply and nulling resistor settings are touched up, a group of similar transistors may be tested with no further adjustments. In practice, the test units are in an environmental test chamber and are switch-selected for connection to the external test circuits. Tables II, III, IV, V, and VI give transistor V_{CES} and V_{BE} results. The units tested are transistors of the same process and geometry to be used for Q_1 in the driver circuit (see Figure 4). Transistor Q_2 will have four times the area of Q_1, so measured current values should be multiplied by four to describe Q_2.

Table II. Base-Emitter Voltages for Characterization of Q_1 and of Q_2 at $I_{E_2} = 4\ I_E$

Parameter		V_{BE}											
Units		V											
Conditions		I_E = 0.5 mA			I_E = 1 mA			I_E = 2 mA			I_E = 5.5 mA		
T_A(°C)		−20°C	25°C	100°C	−20°C	25°C	100°C	−20°C	25°C	100°C	−20°C	25°C	100°C
Device No.	I_C/I_B												
	30	0.790	0.706	0.560	0.810	0.730	0.592	0.832	0.750	0.622	0.880	0.800	0.690
1	35	0.790	0.705	0.560	0.810	0.726	0.590	0.830	0.746	0.620	0.880	0.798	0.685
	40	0.786	0.704	0.560	0.808	0.725	0.588	0.830	0.746	0.620	0.875	0.796	0.682
	30	0.775	0.690	0.542	0.796	0.716	0.574	0.822	0.738	0.610	0.878	0.799	0.685
2	35	0.774	0.690	0.540	0.796	0.715	0.570	0.820	0.736	0.606	0.875	0.796	0.682
	40	0.775	0.688	0.540	0.795	0.714	0.570	0.820	0.736	0.605	0.874	0.794	0.678
	30	0.782	0.700	0.555	0.802	0.722	0.582	0.825	0.740	0.616	0.870	0.794	0.682
3	35	0.782	0.700	0.552	0.800	0.720	0.580	0.824	0.740	0.615	0.870	0.790	0.678
	40	0.782	0.698	0.552	0.800	0.720	0.580	0.822	0.740	0.612	0.866	0.786	0.674
	30	0.761	0.672	0.525	0.785	0.700	0.558	0.815	0.728	0.595	0.860	0.785	0.668
4	35	0.762	0.672	0.523	0.785	0.698	0.555	0.810	0.723	0.592	0.855	0.780	0.662
	40	0.761	0.671	0.521	0.783	0.695	0.554	0.810	0.722	0.590	0.850	0.778	0.658
	30	0.770	0.681	0.535	0.790	0.708	0.565	0.820	0.735	0.600	0.860	0.790	0.673
5	35	0.770	0.681	0.531	0.790	0.705	0.563	0.815	0.731	0.599	0.860	0.787	0.670
	40	0.770	0.680	0.531	0.790	0.703	0.561	0.815	0.730	0.596	0.860	0.783	0.665
	30	0.778	0.689	0.541	0.795	0.711	0.570	0.820	0.739	0.605	0.862	0.791	0.673
6	35	0.775	0.688	0.541	0.795	0.710	0.570	0.815	0.735	0.602	0.861	0.789	0.670
	40	0.775	0.688	0.540	0.793	0.710	0.568	0.815	0.733	0.601	0.860	0.785	0.665
	30	0.770	0.681	0.533	0.792	0.708	0.565	0.820	0.737	0.601	0.871	0.800	0.680
7	35	0.770	0.681	0.531	0.792	0.706	0.562	0.820	0.735	0.600	0.870	0.797	0.675
	40	0.770	0.680	0.531	0.790	0.705	0.561	0.820	0.732	0.599	0.870	0.792	0.671

Table III. Collector-Emitter Voltages for Characterization of Q_1 and of Q_2 at $I_{E_2} = 4\ I_E$

Parameter		V_{CE}											
Units		V											
Conditions		I_E = 0.5 mA			I_E = 1 mA			I_E = 2 mA			I_E = 5.5 mA		
T_A(°C)		−20°C	25°C	100°C	−25°C	25°C	100°C	−25°C	25°C	100°C	−25°C	25°C	100°C
Device No.	I_C/I_B												
1	30	0.082	0.088	0.103	0.088	0.096	0.113	0.104	0.112	0.136	0.160	0.178	0.216
	35	0.092	0.096	0.112	0.097	0.102	0.122	0.112	0.126	0.143	0.168	0.183	0.225
	40	0.102	0.104	0.118	0.108	0.112	0.127	0.120	0.126	0.150	0.178	0.202	0.233
2	30	0.074	0.074	0.081	0.078	0.083	0.096	0.095	0.106	0.128	0.168	0.192	0.238
	35	0.082	0.080	0.087	0.084	0.088	0.103	0.100	0.110	0.133	0.174	0.195	0.247
	40	0.092	0.086	0.097	0.090	0.092	0.107	0.105	0.113	0.137	0.178	0.205	0.251
3	30	0.078	0.086	0.102	0.087	0.097	0.119	0.110	0.120	0.152	0.178	0.202	0.253
	35	0.082	0.092	0.110	0.093	0.102	0.124	0.114	0.126	0.157	0.187	0.208	0.263
	40	0.090	0.097	0.115	0.098	0.108	0.130	0.120	0.132	0.162	0.194	0.220	0.272
4	30	0.045	0.049	0.058	0.053	0.059	0.073	0.069	0.080	0.100	0.122	0.147	0.183
	35	0.049	0.053	0.062	0.056	0.063	0.076	0.072	0.082	0.102	0.125	0.151	0.191
	40	0.053	0.056	0.065	0.059	0.066	0.079	0.074	0.085	0.107	0.131	0.153	0.197
5	30	0.058	0.064	0.076	0.066	0.075	0.092	0.092	0.097	0.121	0.142	0.170	0.215
	35	0.063	0.068	0.081	0.070	0.079	0.096	0.088	0.100	0.126	0.149	0.173	0.221
	40	0.067	0.072	0.085	0.074	0.082	0.100	0.091	0.105	0.130	0.153	0.180	0.229
6	30	0.065	0.073	0.088	0.073	0.084	0.103	0.089	0.108	0.132	0.151	0.180	0.230
	35	0.070	0.078	0.095	0.078	0.089	0.110	0.096	0.111	0.139	0.158	0.188	0.239
	40	0.075	0.083	0.099	0.082	0.093	0.112	0.099	0.115	0.142	0.165	0.192	0.246
7	30	0.059	0.064	0.076	0.069	0.077	0.093	0.090	0.100	0.125	0.161	0.190	0.243
	35	0.063	0.069	0.081	0.073	0.080	0.097	0.094	0.105	0.130	0.167	0.195	0.249
	40	0.068	0.073	0.086	0.077	0.084	0.101	0.098	0.109	0.132	0.173	0.199	0.251

Table IV. Base-Emitter Voltages for Characterization of Q_2 at $I_{E_2} = 4\ I_E$

Parameter		V_{BE}								
Units		V								
Conditions		I_E = 5.5 mA			I_E = 7.75 mA			I_E = 11 mA		
T_A(°C)		−20°C	25°C	100°C	−25°C	25°C	100°C	−20°C	25°C	100°C
Device No.	I_C/I_B									
1	15	0.895	0.818	0.708	0.920	0.840	0.740	0.945	0.875	0.780
	20	0.890	0.810	0.700	0.910	0.838	0.735	0.940	0.870	0.770
	25	0.885	0.804	0.695	0.905	0.830	0.726	0.934	0.860	0.760
2	15	0.890	0.815	0.705	0.920	0.845	0.742	0.950	0.880	0.782
	20	0.886	0.808	0.698	0.915	0.838	0.735	0.944	0.875	0.775
	25	0.882	0.800	0.692	0.910	0.833	0.725	0.940	0.870	0.765
3	15	0.882	0.806	0.700	0.905	0.830	0.734	0.930	0.860	0.766
	20	0.878	0.800	0.694	0.900	0.825	0.724	0.922	0.855	0.758
	25	0.875	0.797	0.686	0.896	0.820	0.718	0.918	0.850	0.750
4	20	0.865	0.792	0.680	0.889	0.820	0.711	0.910	0.848	0.742
	25	0.861	0.790	0.671	0.885	0.811	0.705	0.905	0.840	0.745
5	20	0.870	0.800	0.688	0.895	0.825	0.718	0.920	0.855	0.751
	25	0.865	0.795	0.679	0.890	0.820	0.710	0.915	0.848	0.743
6	20	0.872	0.801	0.688	0.895	0.825	0.719	0.920	0.855	0.752
	25	0.868	0.796	0.680	0.890	0.821	0.710	0.915	0.849	0.743
7	20	0.871	0.810	0.690	0.910	0.840	0.729	0.940	0.872	0.769
	25	0.871	0.805	0.685	0.905	0.833	0.720	0.935	0.866	0.760

Table V. Collector-Emitter Voltages for Characterization of Q_2 at $I_{E_2} = 4\ I_E$

Parameter		V_{CE}								
Units		V								
Conditions		I_E = 5.5 mA			I_E = 7.75 mA			I_E = 11 mA		
T_A(°C)		−20°C	25°C	100°C	−20°C	25°C	100°C	−25°C	25°C	100°C
Device No.	I_C/I_B									
1	15	0.136	0.152	0.183	0.167	0.190	0.225	0.208	0.230	0.282
	20	0.144	0.160	0.197	0.178	0.198	0.242	0.224	0.245	0.301
	25	0.153	0.170	0.207	0.188	0.208	0.254	0.238	0.260	0.320
2	15	0.152	0.167	0.201	0.192	0.213	0.253	0.246	0.268	0.330
	20	0.158	0.180	0.217	0.205	0.227	0.272	0.265	0.290	0.350
	25	0.164	0.186	0.228	0.212	0.240	0.288	0.280	0.310	0.370
3	15	0.153	0.173	0.213	0.192	0.216	0.267	0.242	0.270	0.340
	20	0.163	0.185	0.230	0.203	0.230	0.287	0.262	0.290	0.370
	25	0.172	0.193	0.243	0.215	0.243	0.303	0.277	0.310	0.400
4	20	0.115	0.135	0.172	0.146	0.171	0.219	0.189	0.220	0.279
	25	0.120	0.141	0.179	0.152	0.179	0.226	0.199	0.230	0.290
5	20	0.131	0.154	0.198	0.165	0.192	0.247	0.211	0.248	0.310
	25	0.139	0.161	0.205	0.175	0.201	0.258	0.225	0.260	0.330
6	20	0.140	0.162	0.208	0.172	0.201	0.259	0.221	0.259	0.330
	25	0.148	0.172	0.219	0.182	0.212	0.271	0.238	0.275	0.350
7	20	0.152	0.179	0.229	0.200	0.232	0.299	0.269	0.310	0.390
	25	0.158	0.185	0.235	0.208	0.241	0.301	0.278	0.320	0.410

Table VI. Base-Emitter and Collector-Emitter Voltages for Characterization of Transistor Input Devices

Parameter		V_{BE}						V_{CE}					
Units		V						V					
Conditions		V_{BE} for I_E = 0.1 mA			V_{BE} for I_E = 0.2 mA			V_{CE} for I_E = 0.1 mA			V_{CE} for I_E = 0.2 mA		
T_A(°C)		−20°C	25°C	100°C	−20°C	25°C	100°C	−20°C	25°C	100°C	−25°C	25°C	100°C
Device No.	I_C/I_B												
	30	0.750	0.660	0.502	0.765	0.680	0.528	0.084	0.087	0.098	0.082	0.086	0.098
1	35	0.750	0.660	0.502	0.765	0.680	0.526	0.100	0.097	0.108	0.093	0.095	0.108
	40	0.750	0.660	0.502	0.765	0.680	0.528	0.345	0.110	0.117	0.110	0.104	0.116
	30	0.730	0.642	0.484	0.750	0.660	0.508	0.125	0.084	0.075	0.089	0.076	0.075
2	35	0.734	0.642	0.484	0.750	0.660	0.506	0.157	0.096	0.082	0.107	0.084	0.081
	40	0.734	0.644	0.482	0.750	0.660	0.505	0.233	0.107	0.088	0.130	0.092	0.087
	30	0.744	0.656	0.498	0.760	0.675	0.520	0.076	0.081	0.093	0.074	0.086	0.094
3	35	0.744	0.656	0.498	0.760	0.674	0.520	0.084	0.088	0.100	0.082	0.088	0.101
	40	0.744	0.656	0.496	0.760	0.672	0.520	0.094	0.095	0.108	0.089	0.094	0.108
	30	0.720	0.622	0.468	0.740	0.645	0.492	0.049	0.046	0.048	0.045	0.046	0.050
4	35	0.720	0.622	0.468	0.740	0.645	0.491	0.054	0.051	0.052	0.049	0.050	0.054
	40	0.720	0.622	0.465	0.738	0.642	0.490	0.060	0.055	0.056	0.054	0.054	0.058
	30	0.730	0.632	0.479	0.748	0.655	0.501	0.063	0.060	0.066	0.058	0.059	0.068
5	35	0.728	0.632	0.479	0.747	0.653	0.501	0.070	0.065	0.071	0.063	0.064	0.073
	40	0.728	0.632	0.478	0.745	0.652	0.500	0.078	0.071	0.076	0.069	0.069	0.077
	30	0.738	0.642	0.488	0.752	0.661	0.510	0.064	0.069	0.080	0.063	0.069	0.082
6	35	0.735	0.642	0.487	0.752	0.661	0.510	0.071	0.075	0.087	0.068	0.075	0.088
	40	0.735	0.642	0.485	0.752	0.660	0.509	0.077	0.081	0.093	0.073	0.080	0.093
	30	0.732	0.635	0.478	0.748	0.655	0.500	0.054	0.057	0.066	0.054	0.058	0.068
7	35	0.730	0.632	0.478	0.747	0.655	0.500	0.060	0.062	0.072	0.059	0.063	0.073
	40	0.730	0.632	0.476	0.746	0.652	0.500	0.065	0.067	0.076	0.064	0.068	0.077

3. Analysis of Active Input Transistors

An alternate connection for the ten inputs will be discussed by referring to Figure 6. Figure 6(a) shows a diode-connected transistor input device. This connection was used in Figure 4. By connecting each transistor as shown in Figure 6(b), the voltage at the base terminal of transistor Q_1 can be made smaller than for connection (a) by proper selection of R_A and R_B. The object of this connection is to

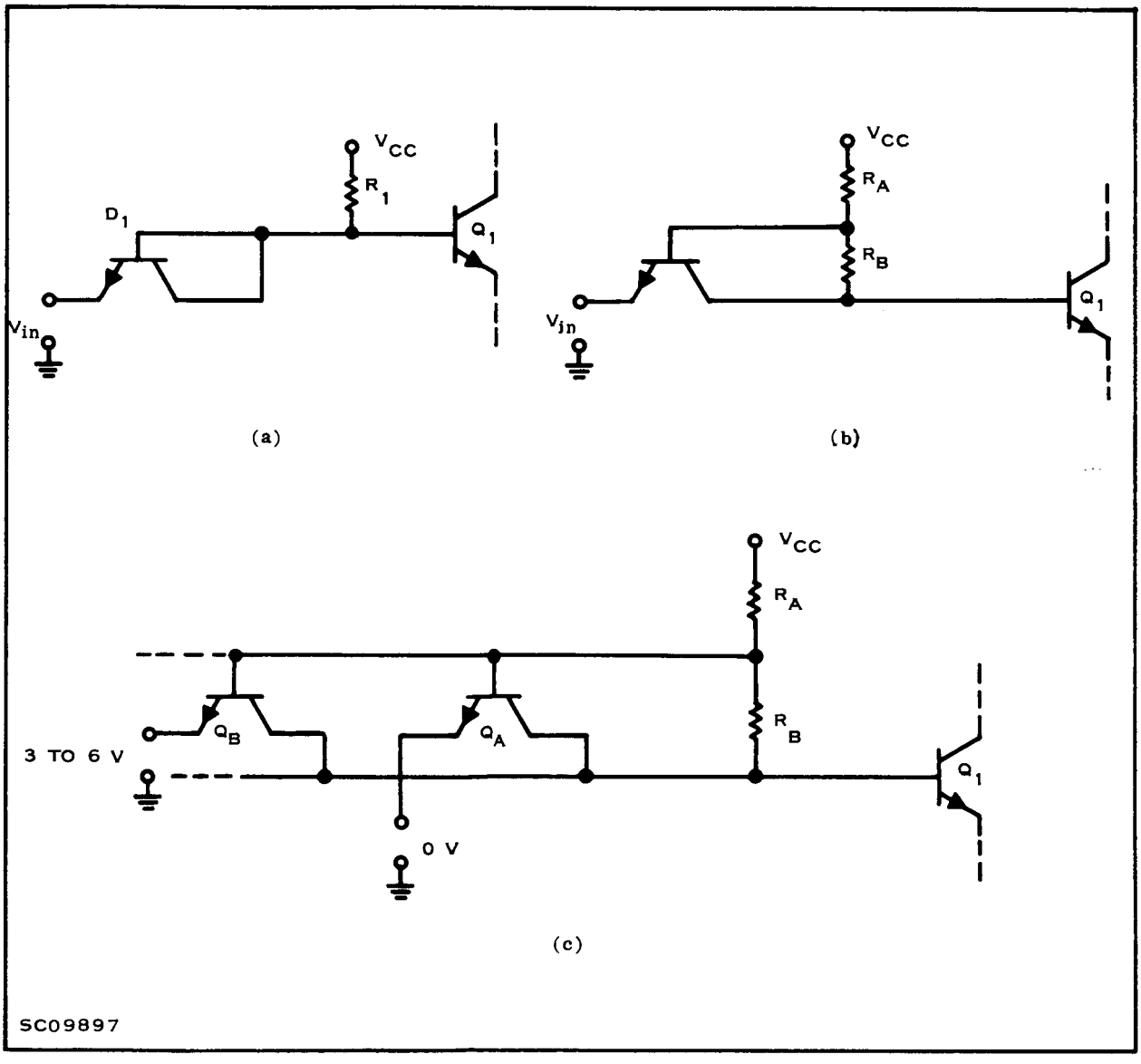

Figure 6. Alternate Input Connections

make certain that the light emitting diode current will be small when $V_{in} = 1$ V. The lower limit for R_A is set by the requirement $(I_{RA})(V_{CC\ max}) \leq 1$ mW when $V_{in} = 0$. This requirement gives $I_{RA} \leq 0.222$ mA for $V_{CC} = 4.0 \pm 0.5$ V. Because the base-emitter voltages for the input devices are nearly the same for connections (a) and (b), R_A and R_1 are equal. For the ON state, the total resistance between supply and the base terminal of Q_1 is R_1 for connection (a), and $R_1 + R_B$ for connection (b). At the lower limits of supply voltage, less base current is available in connection (b), requiring a larger minimum gain for Q_1.

In connection (a) the inputs are isolated from each other by a reverse-biased junction when one input is on and another off. For connection (b) interaction between inputs is possible, as will be discussed by referring to Figure 6(c). With zero input voltage for transistor Q_A and transistor Q_A in saturation, the base-collector junction of transistor Q_B is forward biased while the base-emitter junction is reverse biased. Transistor Q_B is thus biased for inverse operation. In contrast to connection (a), where input currents are limited to junction leakages, input currents for connection (c) can be large if V_{BC} is large. Note that V_{BC} is the difference between V_{BE} and V_{CE} of transistor Q_A. At 100°C and $I_C/I_B \leq 30$, $V_{BC} \geq 0.43$ V. For $V_{BC} = 0.43$ V, I_E for transistor B can be 60 μA. A worst-case analysis for this input connection would require $V_{BC\ max} = 0.68$ V at −20°C. Again, about 60 μA input current could result.

Because of the interaction between inputs and because less base drive is available for Q_1, the transistor input connection is not recommended.

SECTION III

CONCLUSIONS AND RECOMMENDATIONS

Phase I has been completed with the delivery of twenty GaAs Switches and the design of the driver circuit.

Plans, under Phase II, now call for design of the integrated circuit diffusion masks for the driver circuit and of the package for the complete Isolation Switch.

SECTION IV

REFERENCES

1. Texas Instruments Incorporated, "Photon-Coupled Isolation Switch," JPL Contract No. 951340, Third Quarterly Report, 1 July to 30 September, 1966.

2. Texas Instruments Incorporated, "Photon-Coupled Isolation Switch," JPL Contract No. 951340, Fourth Quarterly Report, 1 October to 31 December, 1966.