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DESIGN AND DEVELOPMENT OF A HIGH POWER, LOW SATURATION VOLTAGE SILICON SWITCHING TRANSISTOR

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ABSTRACT

Following the development of a silicon transistor with 0.2V saturation drop at the rate of 75A, the present effort is to attain a design goal of 0.1V under the same conditions. The use of single chip, thin silicon and two methods of generating the symmetrical junction design for low saturation voltage are described. The computer optimized topographical design has been completed and results are presented. Materials acquired for experimental work are reported.

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I. INTRODUCTION

During 1966 and early 1967 Westinghouse developed a transistor with 0.2V saturation drop at 75A under Jet Propulsion Laboratory Contract No. JPL-951303.(1) Theoretical considerations indicate the feasibility of a transistor with a saturation voltage of 0.1V at 75A collector current. This is the object of the present effort with a design goal of .07V.

Generally the determinant factor for low $V_{CE(sat)}$ is to operate the transistor with as low a current density as is practical commensurate with the size of silicon material. While it is possible to increase the total emitter periphery length or to parallel a number of transistors for reducing the current density and thereby the saturation voltage, it appears more valuable to advance the state-of-the-art by fully utilizing the device theory of controlling the lateral distribution of current density in both emitter-base and collector-base junctions.

With the latest development of thin crystals, it appears theoretically justifiable to extend the presently successful simultaneous-diffused (SDT) process. The use of thin crystal will permit steeper concentration gradients in both the emitter and collector regions thereby increasing the injection efficiency. The thin crystal will also minimize any possible internal series resistance in the emitter and collector regions. Whereas processing steps are well defined, improved handling techniques and process refinements are required to minimize breakage. Experience with relatively thin wafers has shown that breakage is the major yield detractor. It is also known that the incidence of breakage is related to the number and/or type of processing steps employed. Obviously, the number of high temperature operations should be minimized. Since the previously developed

(1) T. C. New, P. J. Kannam, F. G. Ernick and P. M. Kisinko, "High Power, Low Saturation Voltage, Switching Transistors," presented at 1966 International Electron Devices Meeting in Washington, D.C. (Credit due to JPL sponsorship.).

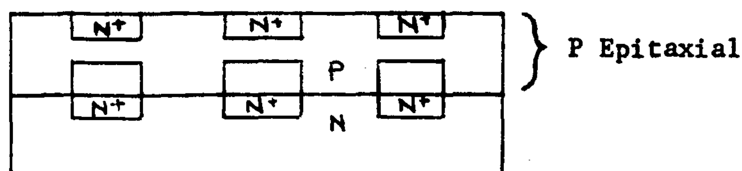
single-diffused process requires deep diffusions to obtain relatively narrow base widths, it is desirable to use a "strong" N-type diffusion source such as ammonium phosphate. Whereas, ammonium phosphate does yield deep, high concentration diffusions, it is incompatible with planar technology since it is not masked effectively by conventional oxides. It is convenient, therefore, to employ mesa etching techniques in conjunction with the ammonium phosphate diffusions. However physical deformation caused by mesa etching will weaken the structure and enhance the possibility of breakage through subsequent processing.

Therefore planar technology with existing phosphorous oxychloride diffusions will be used for the thin wafer approach. The flow for this process is shown in Figure 1, Page 6 .

A second consideration for designing a transistor with low saturation voltage involves the effect of current crowding at the emitter edge. By controlling the collector geometry such that the collector region directly under the emitter is identical to the emitter geometry, the gradient in the base under high injection should assume the best symmetry. Thereby the current distributions and the voltage drops across both the emitter-base and the collector-base junctions would also be similar. Thus, the difference of the two voltages which determines the $V_{CE(sat)}$ would be minimized.

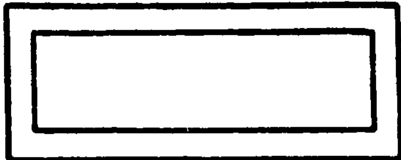
Two different processes are being investigated and implemented in order to achieve the desired collector geometry.

The epitaxial selective collector type will incorporate a selective arsenic diffusion prior to epitaxial growth. The desired corss-sectional structure is shown below.

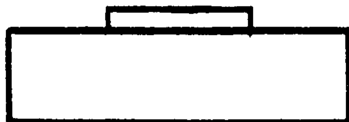


THIN WAFER PROCESS

Starting Material
20 ohm-cm P-type Si
2.0 ± .05 mils thick



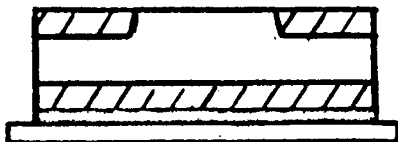
Oxidation
Thickness 7,000Å



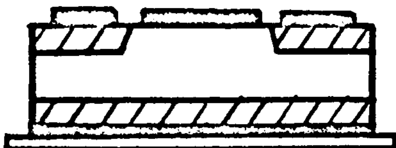
Emitter and Photomasking
Defines emitter region

$POCl_3$ Deposition
$W_B \sim 35\mu$

Final Drive and Slow Cool
$W_B \sim 12\mu$



Molybdenum Mounting
Ag Solder



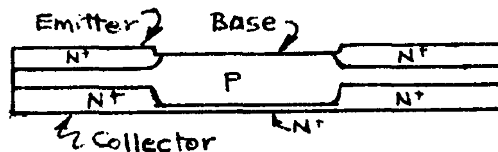
Contact Evaporation
Al ~ 30KA

FIGURE 1

This will provide geometrically symmetrical emitter-collector profiles. It is necessary to employ arsenic (or antimony) rather than phosphorous as the subcollector diffusant in order to minimize autodoping.

It is possible that the concentration step in the collector may not be sharp enough to provide the desired effect. This lack of sharpness would be caused by outdiffusion from the substrate as well as from the arsenic deposit and from the fact that it is difficult to achieve arsenic concentrations much more than a factor of 10 or 20 times greater than the concentration of the N-type substrate. However, should the experimental results so indicate, the problem may be alleviated with a multiple epitaxial growth technique.

A second selective collector method is also being implemented to achieve the diffused structure by double-sided selective diffusion as shown in the following structure.

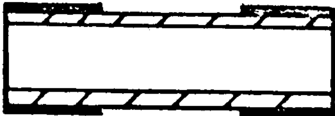


However, it requires a double-sided alignment of masks for photoresist operation. Several methods of achieving the double-sided alignment are available. To insure proper precision, it is necessary to acquire a new alignment machine which provides front-to-back alignment via infrared transmission. This machine should also provide exposure on either side. Another possibility with less precision involves the use of a fixture which has mechanical stops and photographically imprinted indices. The processing sequence for the symmetrically diffused type is shown in Figure 2, Page 8.

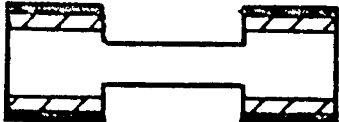
SYMMETRICALLY DIFFUSED TRANSISTOR

Starting Material
20 ohm-cm P-type
5-6 mils thick

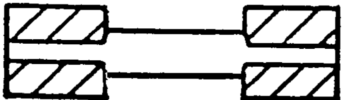
N^+ Deposit
Emitter and collector
x_j = 5.0 - 6.0μ
ρ_s = ~1.0 ohm/□



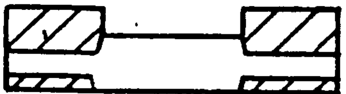
Emitter-Collector Masks
Define emitter and collector geometries



Silicon Etch
Remove N^+ region from base
Depth ~.6 mil

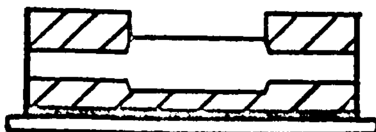


N^+ Drive
x_j ~1.5 mils



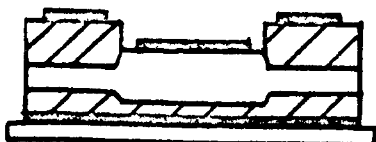
Collector Lapping
Provide planar mounting surface

Collector N^+ Diffusion
Provide N^+ Collector Surface



Molybdenum Mounting

Ag solder



Contact Evaporation
Al ~30KA

FIGURE 2

II. PROGRESS FOR THE CURRENT QUARTER

A. MATERIALS AND PROCESSING

Silicon starting materials have been received for the various approaches described in the previous section. Evaluations of the materials for the thin wafer approach and the symmetrically diffused, selective collector approach are listed in Figure 3, Page 10, and Figure 4, Page 11.

Material for the epitaxial selective collector is N-type, .01 ohm-cm material. The arsenic floating collector diffusion is being done as commonly practiced in the fabrication of integrated circuits. The target parameters for the arsenic diffusion are a diffusion depth of 8 microns and a surface concentration of 1.8×10^{19} atoms per cm^3.

B. GEOMETRY AND MASK DESIGN

The geometry which will be used initially for these studies is the sunburst design utilized earlier in the Contract No. JPL-951303. An improved sunburst geometry has been designed, which has the following features:

1. Increased aluminum width on emitter fingers
2. Larger contact areas for both emitter and base
3. Alignment marks to aid in registration of the contact mask
4. Increased emitter edge length resulting from optimization techniques described below

The optimum dimensions for a sunburst design are not immediately obvious. For a given transistor diameter, the emitter edge length is determined primarily by the radius of the central base dot, since this dimension determines both the number and the length of the fingers. The number of fingers decreases with decreasing base dot radius, but the length of the fingers increases. Therefore there is an optimum radius, which is derived as follows: (Page 12)

SILICON EVALUATION

TO E. R. Stonebraker P. O. No. 31L-21157

Supplier Monsanto (Monothin)

Amount Received 20 slices

Department Transistor Engineering

Crystal No. 699726

Type P

Diameter > 1.125"

Thickness 0.003" (polished one side)

Orientation 1-1-1 ± 1.5°

Resistivity:

Skin -----

Radial 17-19-18 ohm-cm

Gradient 10.3%

Dislocation Density (Westinghouse 5 Point Count System)

0-200-0-400-200/cm^2

Lifetime not measured

Lineage none

L. H. Weitzman

FIGURE 3

SILICON EVALUATION

TO F. G. Ernick P. O. No. 31L-11398

Supplier Texas Instruments

Amount Received 1 crystal

Department Transistor Engineering

Crystal No. 14207

Type P

Diameter 1.25"

Length 9.9"

Orientation 1-1-1 ± 0°

Resistivity:

Skin 15-14.5-14.5-14.5-14.5-18.5-19-24-18 ohm-cm

Radial 14-13-14 ohm-cm

Gradient 7.1%

Dislocation Density (Westinghouse 5 Point Count System)

200-800-200-200-400/cm^2

Lifetime 100μsec

Lineage none

L. H. Weitzman

FIGURE 4

$$N = \frac{2\pi \ R_i}{w + s} \quad (1)$$

where N = the number of fingers

R_i = the radius of the base dot

w = the width of the base fingers

s = the spacing between base fingers at the edge of the base dot

$$E = 2N(R_o - R_i) \quad (2)$$

where E = the emitter edge length

R_o = the radius of the circle defined by the outer ends of the base fingers

(This equation is an approximation because the contributions of the ends of the fingers are neglected.)

Substituting Equation 1 in 2,

$$E = \frac{4\pi \ R_i \ (R_o - R_i)}{w + s} = \frac{4\pi}{w + s} (R_i R_o - R_i^2)$$

differentiating

$$\frac{dE}{dR_i} = \frac{4\pi}{w + s} (R_o - 2R_i)$$

for E_{max}, let $\frac{dE}{dR_i} = 0$

$$0 = \frac{4\pi}{w + s} (R_o - 2R_i)$$

giving the final result

$$R_{i\,(max)} = \frac{R_o}{2}$$

It can be seen that for this idealized case, the optimum base dot radius is one-half the radius defined by the ends of the base fingers and is independent of w and s.

A useful equation for approximating the maximum emitter edge length is:

$$E_{max} = \frac{\pi R_o^2}{w + s}$$

While the relationships derived above are useful in designing sunburst geometries, they have shortcomings, namely:

1. They do not demand an integral number of fingers.
2. The inclusion of rounded tips on the fingers may shift the optimum R_i slightly.

A program has been written using an IBM QUIKTRAN time-sharing computer in order to overcome the shortcomings listed above and to speed up the design process. The program operates roughly as follows:

1. The user enters the width of the base fingers, the spacing between base fingers at the base dot, and the radius defined by the tips of the base fingers. These quantities are generally fixed by the transistor package, photofabrication capabilities, and base finger resistances.
2. The computer calculates optimum emitter edge length (including the contributions by the ends of the fingers). The print-out includes the number of fingers, the base dot radius, emitter edge length, and the angle between fingers.
3. The program offers the user the option of changing the number of fingers and/or the base dot radius, and calculates new dimensions where appropriate.

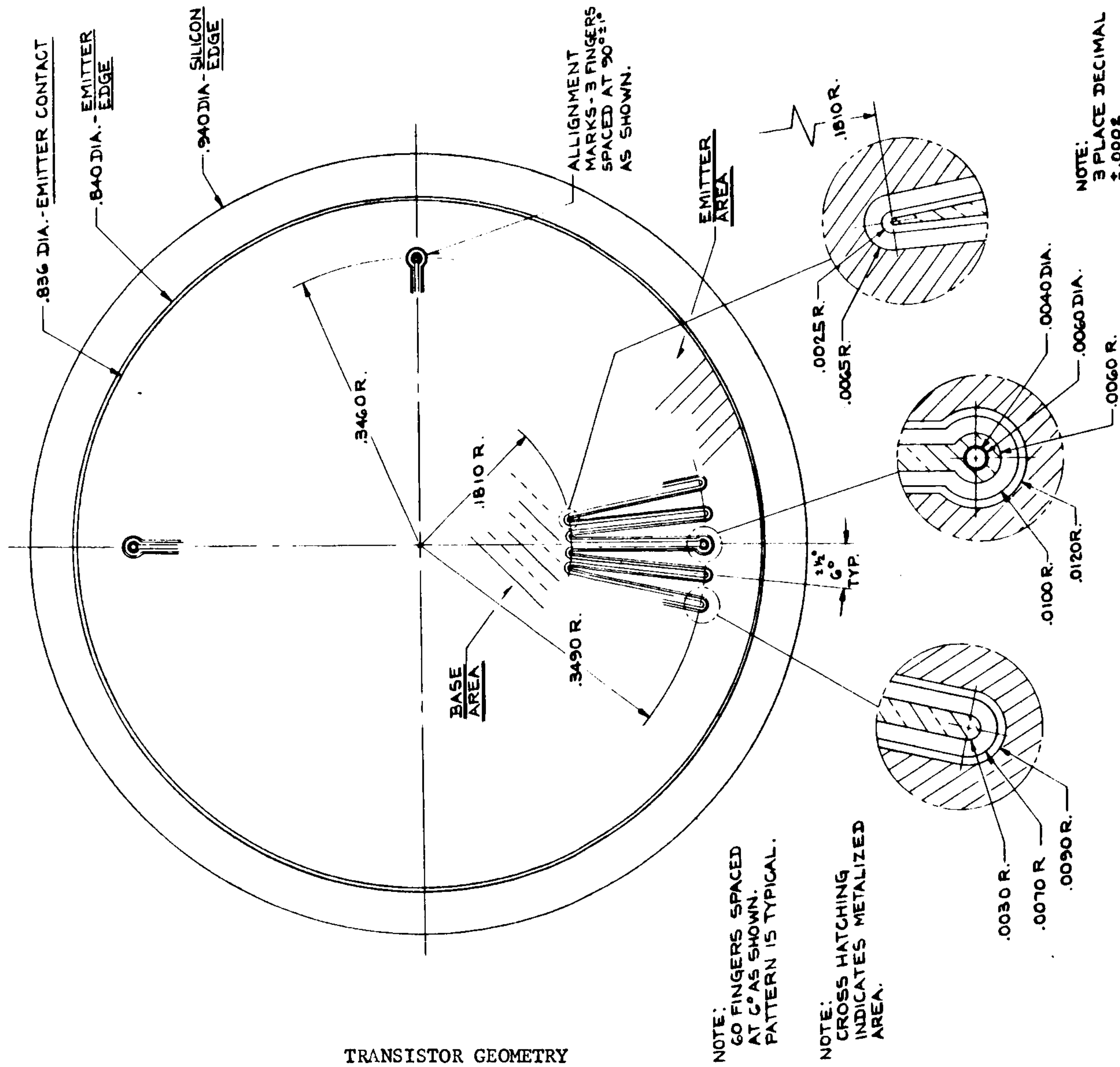
The computer print-out of the calculations for the redesigned geometry is shown in Figure 5, Page 14. A sketch of this geometry appears in Figure 6, Page 15. The significant improvements of this design include:

COMPUTER PRINT-OUT

```
    START(0)
 ENTER WIDTH, SPACING, OUTSIDE RADIUS
.014/.005/.349
 NUMBER   RADIUS   EDGE    ANGLE  SPACING
  60.0 0.181437  21.898 6.000 0.005000
 TO CHANGE N, START 100; R, START 110; N AND R, START 120.


    START(120)
 ENTER NUMBER, INSIDE RADIUS
60./.181
 NOTE...SPACING IS SMALLER THAN ORIGINAL VALUE
 NUMBER   RADIUS   EDGE    ANGLE  SPACING
  60.0 0.181000  21.946 6.000 0.004954
```

FIGURE 5



TRANSISTOR GEOMETRY

FIGURE 6

1. Emitter edge length increased from 17.4 inches to 21.9 inches.
2. Emitter contact region width increased from .040 inches to .060 inches.
3. Base contact region diameter increased from .242 inches to .349 inches.
4. Emitter metallization comes within .002 inches of emitter edge instead of .004 inches, giving slightly lower resistance along an emitter finger. This is accomplished with no decrease in registration tolerance since the actual tolerance is the distance between the base finger and the lateral diffusion from the emitter.
5. The effective resistance of the base fingers has been reduced to less than half the original value since the fingers are shorter (reduced from .236 to .1805 inches) and more numerous (increased from 36 to 60).

III. PROGRAM FOR THE NEXT PERIOD

Transistors will be fabricated by the three approaches described in the introduction. Emphasis in the thin wafer approach will be placed upon handling techniques. Plastic tweezers and Bernoulli pickups will be used to minimize the generation of stress points which may induce breakage.

A mask alignment fixture is being acquired which will permit:

1. Simultaneous double-sided exposure through prealigned masks
2. Back-side alignment by the use of infrared illumination through the slice.

This equipment will be used for the symmetrically diffused, selective collector approach.

Initial work on all three approaches will utilize the geometry employed earlier in the Contract No. JPL-951303 until masks with the redesigned geometry are available.