RESEARCH AND DEVELOPMENT STUDY

ON MULTIMODE SYSTEM APPLICATIONS IN THE AREA OF TIME OF FLIGHT AND COINCIDENCE MEASUREMENTS

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ON MULTIMODE SYSTEM APPLICATIONS IN THE AREA OF TIME OF FLIGHT AND COINCIDENCE MEASUREMENTS

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SUMMARY - Multimode System

Recently the need for a multimode digital storage device has become more and more pronounced. The utilization of such a system offers significant economic benefits to user groups by eliminating duplication of expensive components not compatible with all applications. Such a system has been designed, fabricated and installed at NASA Electronics Research Center, Cambridge, Massachusetts by Nuclear Data, Inc. It incorporates a 4096 channel memory with 20 binary bit storage (1,048,575 counts), a 4 μsec memory cycle time, 16 megahertz analog to digital converters and built in arithmetic capability. Display and data manipulation have been incorporated which provide the latest in visual interpretation techniques. The analog to digital converters contain inputs for uni-polar and bi-polar pulses, coincidence and anti-coincidence inputs, D.C. or slowly varying A.C. signal analysis.

These various input capabilities and data manipulation features were incorporated to facilitate the many input requirements as outlined later in this report.

It is most strongly felt that this portion of the system greatly exceeded the expectations and requirements outlined in the contract.

INTRODUCTION - Multimode Systems

A multimode system was designed and delivered to fulfill the first section of this contract. The design parameters for this device were established through the joint efforts of Nuclear Data, Inc. and the National Aeronautics and Space Administration. The primary objective at the conceptual level was to develop a digital storage device capable of performing both routine and complex experiments, utilizing the same instrument in various experimental endeavors. It was concluded that many areas of research, although unrelated, required the use of similar counting and analysis systems and this served as the foundation on which the design was based.

The research areas for which investigations were planned were listed and catagorized as a function of instrument utilization. The results of this listing were somewhat startling. It was determined that as many as ten areas of research can be served by one single instrument system resulting in a considerable economy in terms of specialized instrumentation. The utilization of this single instrument system covers the following research areas:

1. Digital time of flight measurements in the area of slow neutron energies.

2. Coincidence experiments, both of single and multi-dimensional nature.

3. Compatibility with all nuclear radiation detectors and related detection systems.

4. Measuring mass and velocity of simulated micrometeoroids.

5. Measurements of time dependent de-excitation spectra of nuclear radiation from a standard source.

6. Mossbauer effect analysis.

7. Measurement of time dependent de-excitation spectra of electromagnetic radiation from excited atoms.

8. Measurement of spatial and time dependent distribution of temperature along one axis of a shock tube.

9. Pulse width analysis - measurement of the total time a pulse exists above a pre-determined reference level.

10. Pulse height vs time of flight - measuring both parameters of a time dependent relationship and storing this information in a two dimensional matrix.

Many more applications for such a system exist and are currently in use; however, a discussion of those applications is beyond the scope of this report.

GENERAL INFORMATION - Multimode System

The series 3300 analyzer system manufactured by Nuclear Data has the following advantages:

It is modular (including circuit cards and mechanical assembly) and, therefore, can be tailored to the needs of researchers in the nuclear, medical, and aerospace fields. Identical modules are used for a wide range of special-purpose data acquisition and processing systems. By substituting different modules, such variables as data storage capacity and types of information input/output are easily changed. Modular construction makes possible a system that expands from the two analog to digital converters provided to eight; from 4096 memory channels to 16,384 channels; from single or dual parameter real time totalizing to a delayed time totalizing buffer tape system handling eight dependent coincident parameters, one, two, or three dependent parameters out of any total up to eight, eight independent parameters, four dual independent parameters of different count rates, or any other data source with comparable logic levels operating on the "ready-resume" data transmission concept.

Detailed specifications covering the entire series 3300 systems are included in Appendix V.

Note should be made of the following specifications which typify the engineering advancements made with this system and which contribute to its flexibility and usefulness.

1. Memory Cycle Time: 4 μsec. This very fast memory storage time provides NASA with data acquisition rates unavailable in any other system. Due to reduced dead time, time related experiments can be performed faster and with greater precision.

2. Analysis Capability: Multiple input independent, and multiple input dependent experiments are routine. Up to four independent, non-related inputs or two dependent inputs can be processed simultaneously. These inputs can originate in widely different detectors without varying the system operation.

3. Readout and Visual Presentation: Controls are provided to present memory data in three different display configurations: slice, contour, isometric. Additional display controls affect display angle, digital region selection, analog region selection, area intensification, area blanking and expanded selectable area viewing (scanmaster). Digital memory readout is also under these controls.

4. Patch programming: Any desired experimental configuration can be programed through the use of front panel patch plugs.

5. Readout device selection: Digital readout devices, analog recorders, or magnetic tape systems can be switch selected by front panel controls. All circuitry for controlling digital and analog recorders is included.

Because of this multimode system, the applications anticipated by NASA represent a small number of the total experiments for which the series 3300 is currently being used. Assembling a list of all applications is beyond the scope of this report but a representative list is included in the "INTRODUCTION - Multimode Systems".

SUMMARY - Time of Flight Systems

Digital time of flight measurements have been accomplished for several years to determine the mass and velocity of both nuclear particles and microparticles. In general, these devices suffered from drawbacks which did not allow simple incorporation into a flexible multi mode system. In addition to these "interface" considerations, a basic design approach was desired which would lend itself to digitizing speeds beyond the slow neutron region. This was considered to be essential to future experimental demands to easily facilitate high speed endeavors without fear of obsolescence and troublesome interfaces.

Under this contract, a time of flight unit was designed to more than fill these basic demands. This design can be used in areas where high digitizing rates are required without starting anew. The basic design incorporates a time range (channel width) which is switch selectable in ten (10) steps (Figure 1). The range is variable from 0.25 μsec/channel to 128 μsec/channel. The time uncertainty (jitter) [3] per channel is greatly reduced through the use of a prescaler. The function of the prescaler is to divide the basic oscillator frequency of 32 megahertz to 4 megahertz by a binary factor.

(3) See Footnote Page 12

Time jitter is further reduced through the use of a double derandomizing circuit which is incorporated within the prescaler. In essence the double derandomizer serves to insure starting and stopping the scaling of the digital pulse train in synchronization with the pulse train itself. In other words, this device eliminates the uncertainty concerning the arrival of a start pulse with respect to the pulse train.

Time resolution has been improved by the incorporation of a new technique which eliminates propagation time errors in the delay circuitry. This technique represents an important improvement over conventional devices due to the automatic correction for propagation time in the delay circuit. The primary effect created by propagation time is that the address register will not settle down sufficiently upon completion of delay to allow acceptance of the next pulse. The next pulse is, of course, the first channel of data and must not be subjected to uncertainty.

Another meaningful contributor to the flexibility of this instrument is its A.E.C. modular construction. This insures compatability with other instrument manufacturers both mechanically and electronically.

We feel our goals under this section of the contract were 100% achieved and we also made a significant advance in the state-of-the-art.

INTRODUCTION - Time of Flight

Digital measurements of the flight time for nuclear particles have been performed for many years. The measurement involves the gating of a crystal-controlled oscillator by the departure of a particle from a source (chopper) and the interaction of the particle within a detector. The total travel time along the flight path is determined by counting the number of oscillator pulses occuring during the interval between the departure and interaction of the particle. Various time of flight devices have been commercially available for some time. Some of these devices suffered from drawbacks ranging from minor to severe. A partial list of these limitations is shown:

1. Channel width selection: 7 or 8 selections.
2. Total delay available: Limited to a maximum of 8192 channels; usually less. In some units, the delay was a multiple of the time range selected.
3. Number of channels available: 1024 maximum.
4. Time jitter: Typically large, due to small pre-scaling factor.
5. Pulse width analysis: Not available.
6. Fixed delay: Inherent in all systems as a result of the use of the main scaler for delay scaling. The propagation time of the final pulse through the scaler introduced a fixed delay which must be normalized in data.

7. Interface & Packaging: Limited to use with one memory.

8. Channel Profile: Usually poor.

9. Price: $5,000.00 to $65,000.00. The more expensive units normally require special memories.

A research and development effort was undertaken to eliminate as many of the above problems as possible. Another guideline was to utilize the basic design over a wide range of oscillator frequencies. This goal was established in an effort to fulfill all time of flight application by changing logic speed, thereby, utilizing the same package for all applications.

As preliminary studies progressed, it became apparent that a trade-off of features was required due to interaction within the logic. In selecting the capabilities of the system, we had to limit the choices to those features which did not conflict with the performance of others. For example, by utilizing the main scaler as a delay scaler, the delay range of the instrument increased which increased the fixed delay, thereby, solving one problem while aggravating another. Several similar approaches were tried with similar results.

Various approaches were attempted to solve secondary problems; as

in transfer techniques. One such technique is referred to as a "reading on the fly". In operation, the sequence is as follows: Upon the arrival of a detector pulse, the number in the register is transferred to the memory in a time shorter than the period of the oscillator. The register is not interrupted and continues to scale until the next event occurs. Events will not be transferred if storage of the previous event is still under way. The shadow time[(2)] becomes equal to the memory cycle time of the storage device. Unfortunately, this technique does not prove to be practical from either an economic or engineering viewpoint. The transfer time becomes a function of the oscillator frequency which imposes extremely strict requirements on the transfer process. To date, high speed transfers have proved to be unreliable at speeds beyond 250 nsec. As a result of these findings, this approach was abandoned. Our goal for a prototype to operate at all oscillator frequencies, greatly influenced this decision.

The final design is based on the update scaler technique which eliminates the problems associated with "on the fly" transfers but does introduce a "shadow". This technique is described below:

(2) Shadow: This term refers to the time in which the time of flight module is unable to process data. A shadow occurs after every event and consists of transfer and storage time.

THE TIME OF FLIGHT MODULE

The time of flight module consists of six main sections and a unique system for tying these together. The oscillator, update scaler, and the main register are found in all digital time of flight units. The unique aspects of the design are found in the delay scaler and the double derandomizer, while the final component, the pre-scaler may or may not be found in other units.

THE MAIN OSCILLATOR

The main oscillator is a 32 megahertz crystal controlled oscillator. (see Figure 2). The oscillator is free running and is gated randomly by the start pulse. 32 megahertz was chosen to provide significant pre-scaling thereby, directing pulses to the main scaler which suffered from a minimum of jitter(3). The jitter associated with this device is 1/64 μsec maximum when operating in the 1/4 μsec per channel mode. The frequency of the pulse train as it enters the main scaler is 4 megahertz.

DOUBLE DERANDOMIZER

The double derandomizer (Figure 2) is used to improve the absolute time profile of the channel. Channel profile is required to be as good as possible in any digitizing system to insure the accuracy of the measurement.

(3) Time jitter is normally defined as being the total time uncertainty in any given measurement. Time jitter is composed of start time errors and stop time errors directly and internal delays indirectly. To reduce time jitter, a high speed oscillator should be used which is gated into a prescaler. The prescaler divides this frequency to the desired range. When a start pulse occurs, the most time uncertainty involved, is one high frequency pulse which is some fraction of the prescaler output or considerably less than one channel.

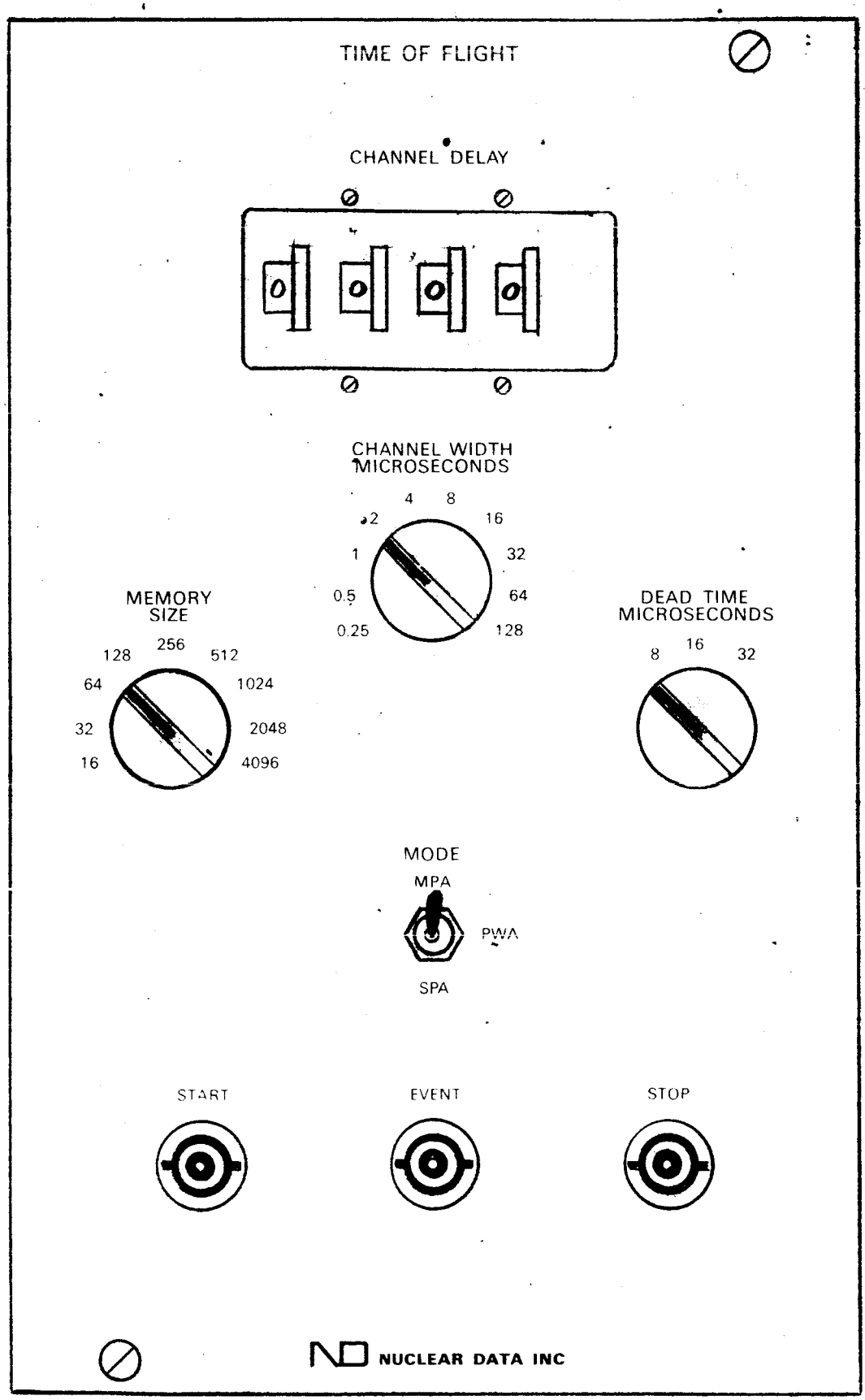

TIME OF FLIGHT
CHANNEL DELAY
CHANNEL WIDTH
MICROSECONDS
4
8
2
16
1
32
0.5
64
0.25
128
MEMORY
SIZE
256
128
512
64
1024
32
2048
16
4096
DEAD TIME
MICROSECONDS
8
16
32
MODE
MPA
PWA
SPA
START
EVENT
STOP
NUCLEAR DATA INC

FIG 1

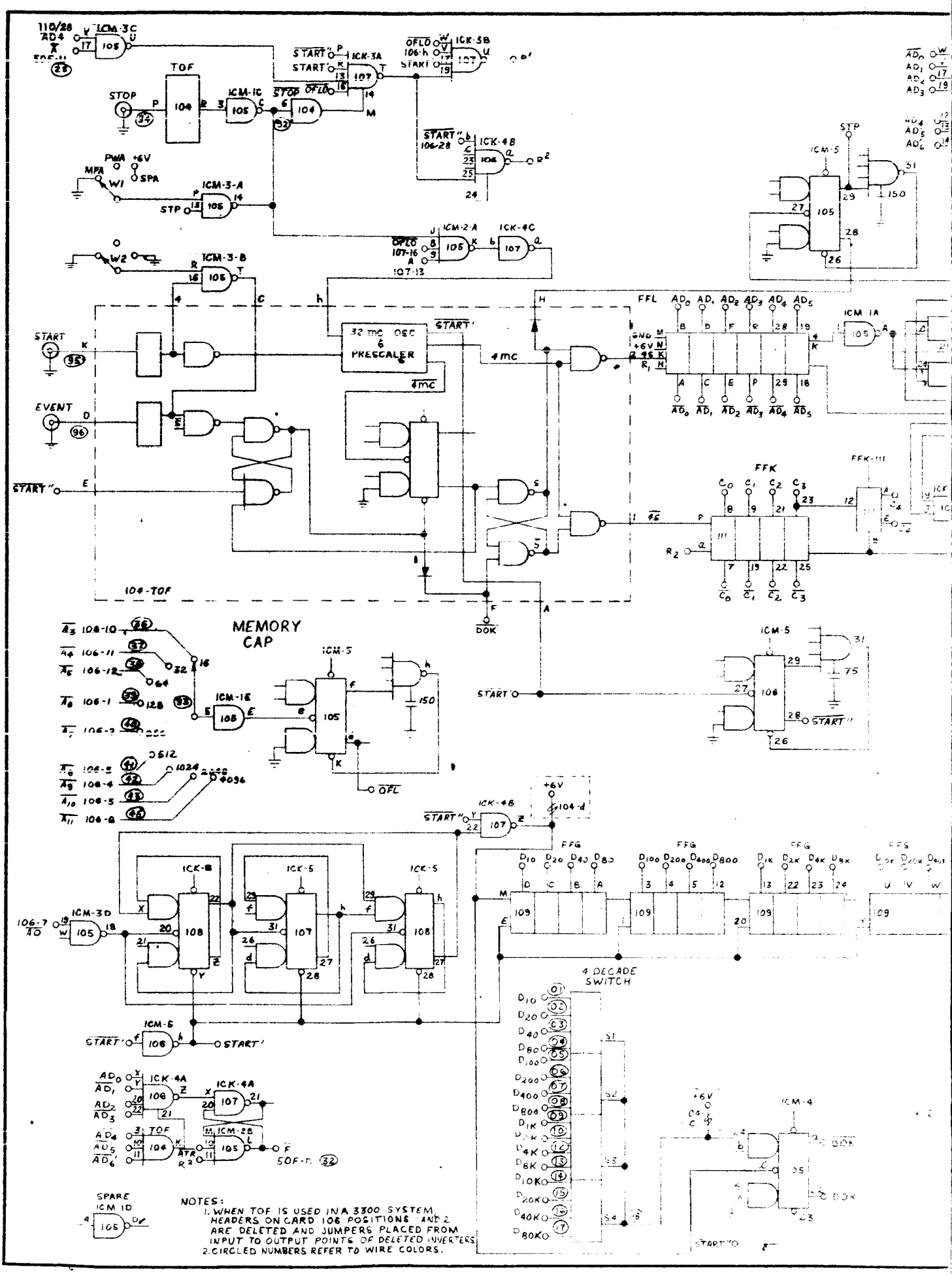

TOF
PRESCALER
32 mc OSC
MEMORY CAP
FFL
FFK
FFG
4 DECADE SWITCH
START
START'
STOP
EVENT
4mc
OFL
DOK
104-TOF
NOTES:
1. WHEN TOF IS USED IN A 3300 SYSTEM, HEADERS ON CARD 106 POSITIONS 1 AND 2 ARE DELETED AND JUMPERS PLACED FROM INPUT TO OUTPUT POINTS OF DELETED INVERTERS
2. CIRCLED NUMBERS REFER TO WIRE COLORS.

Fig 2-1

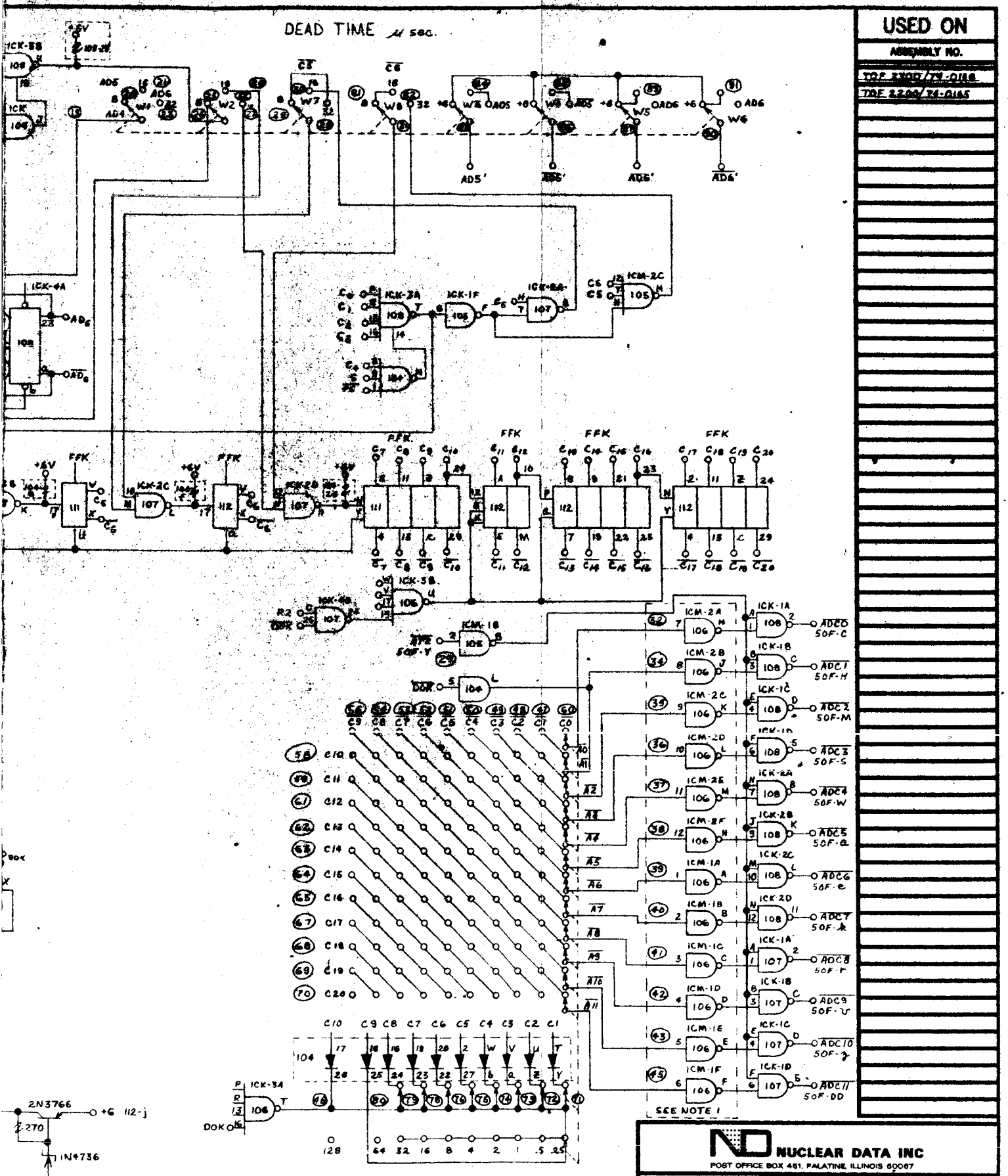

DEAD TIME μ sec.
USED ON
ASSEMBLY NO.
TOF 2300/74-0118
TOF 2200/74-0185
NUCLEAR DATA INC
POST OFFICE BOX 451, PALATINE, ILLINOIS 60067
TIME OF FLIGHT 2200/3300
SYSTEM DIAGRAM
SHEET 2 OF 3
DRAWN BY: R.M.G.
CHECKED BY:
DATE DRAWN: 11-2-67
APPROVED BY:
L-75
CHANNEL WIDTH μ sec
SEE NOTE 1
2N3766
1N4736

FIG 2-2

In essence, channel profile is a determination of the absolute width of any channel within the system. Each channel should be exactly 250 nsec wide (if that scale is chosen) and the center line from channel to channel must also be 250 nsec. Time jitter will influence channel profile. Double derandomization reduces the time jitter associated with the arrival of a start and stop signal with respect to the main oscillator period. Two things contribute to time jitter: (a) the error associated with the determination of a start signal (t_o) with respect to the main oscillator and (b) the error associated with the determination of an event signal (detected event) with respect to the main oscillator. Assuming the main oscillator is stable (in this case, approximate stability is 1 part in 10^6), these two factors are the only influence on time jitter, ignoring secondary effects such as fixed delay, etc. In any case, these two factors can only influence the first event detected when measurements are made without delay time.

The term double derandomization is derived from two primary considerations: (1) The start signal (t_o) and the oscillator pulse train must enable the electronic circuits through an "AND" Gate (2). The arrival of these two pulses trigger a pair of flip-flops which then insure absolute synchronization with the pulse train. In other words, the start signal can only satisfy the

"AND" gate requirement when the oscillator is undergoing a positive excursion. This insures a maximum delay in enabling, of one half cycle or 1/64 of a microsecond. After enabling has occured, the next oscillator pulse is used to direct the pulse train into the pre-scaler. Double derandomization is derived from the use of two consecutive pulses to trigger the gate to the pre-scaler. This insures absolute time synchronization in all measurements due to accurate time reference with respect to t_o. The arrival of an event signal can occur at any time during one complete cycle, hence, a synchronized start is essential to eliminate errors at both ends of the measurement. Care has been taken to gate at the 32 MHz input to the pre-scaler to avoid large uncertaintities in the start time. As the pre-scaler serves to reduce the frequency to 4 MHz, the greatest error which can occur is 1/32 μsec or 1/8 channel.

PRE-SCALER

The function of the pre-scaler is to reduce the frequency from 32 MHz to 4 MHz to increase accuracy in measurements and to reduce time jitter. The pre-scaler is a 3 bit binary scaler, constructed of M.E.C.L.[4]

(4) Motorola emitter coupled logic.

blocks, and is located in the circuit between the double derandomizer, the main oscillator, and the main scaler. With the incorporation of the divide by 8 pre-scaler, this module possesses the least time jitter of all units available.

MAIN SCALER

The main scaler contains 21 binary bits (see Figure 2) which provides the widest selectable time range of all units available. A front panel switch allows selection of channel width ranging from 0.25 μsec to 128 μsec in binary increments. Two other front panel switches affect the operation of this scaler. The first switch, channel width, determines the number of bits to be used for dividing the 4 MHz pulse train by the proper factor to equal the channel width selected. The second switch determines the total number of bits used as a function of total time range and memory size.

Considering the 21 bits as lying in a row from left to right, the bits are arranged in increasing weight from $MS2^0$ to $MS2^{20}$. If a 4096 channel memory is used, the maximum number of bits is 12. The channel width

switch selects which bit is the one to be wired to the least significant bit of the memory, while the range or memory size switch selects which scaler bit represents the most significant bit of the memory. As the channel width is increased, the least significant bit selected moves from left to right while as the memory size is decreased, the most significant bit selected moves from right to left. The total number of bits selected can be extended to 13 or 14 if an 8192 or 16,384 channel memory is used.

THE UPDATE OR DEAD TIME SCALER

The dead time scaler is a 7 bit binary scaler covering a selectable time range which is equal to 8, 16, or 32 channel widths. The purpose of this scaler is to correct the main scaler for the time it is busy in transferring event information to the memory, and therefore, not able to keep track of time. At the exact instant an event signal occurs, the 4 MHz pulse train is gated off to the main scaler and gated on to the update scaler. When the dead time selected has elapsed, the main scaler is updated equal to the content of the update scaler and the 4 MHz pulse train is gated back to the main scaler. The dead time provided insures compatibility with slower memory systems such as computer systems and older equipment.

DELAY SCALER

The purpose of the delay scaler is to provide selectable delays before the pulse train is directed to the main scaler. The delay scaler is located between the pre-scaler and the main scaler. The function of this scaler is to provide a delay in counting in the main scaler until some pre-set time has elapsed. An example might be in an experiment where 1/4 μsec time widths were selected but the range of interest was longer than the total time available with the memory used. A delay of up to 99,990 channels can be selected to compensate for the memory size and until this delay time has elapsed, counting will not occur in the main scaler.

The delay scaler is a separate component, which is unique to time-of-flight units, and is a decimal device. Front panel switches allow selection of delays from 0 to 99,990 channels in increments of 10 channels. A unique operating technique eliminates all propagation delays which normally affect the main scaler. It does so in the following manner: Propagation delays are a result of the time required for a scaler to "carry" an event throughout the entire scaler and produce an output indicating this process has been completed. The delay time is a function of the length of the scaler and the circuitry used. Our circuit utilizes an innovation incorporating a "set-ten"principle. In this manner when a start pulse is

generated, the delay scaler is set to 10. This, of course, means that the delay scaler will stop 10 channels sooner than it should. The propagation time to inform the circuitry that delay -10 has occured may be in the order of 2 or 3 channels. At this point, the signal may be present 7 or 8 channels before the real delay has occured. The output of the delay scaler is gated by the first decade of its scaler, however, resulting in the delay of the signal until the first decade carries a 10. This method completely eliminates propagation times and further improves the accuracy of the measurement.

OPERATION OF THE TIME OF FLIGHT UNIT

The preceding discussion of the major components in this module demonstrates how many of the problems in previous units have been eliminated. The only serious drawback not eliminated is the shadow time. The shadow results from the dead time associated with event storage. It can be referred to as a pulse pair resolution. During the period of dead time, the time-of-flight unit cannot detect the arrival of another event resulting in a blind period or shadow.

When a start pulse arrives, it simultaneously resets the main scaler and up-date scaler, sets 10 in the delay scaler, and sets the double derandomizer gate. The next clock pulse directs the synchronized pulse train to the

main scaler or the delay scaler if a delay has been set. If a delay of zero is set, the delay scaler is switched out and the pulse train is directed to the main scaler. The number of pulses required to equal one channel is determined by the position of the front panel switch. If the scaler reaches the memory size selected before an event occurs, the scaler automatically resets and waits for the next start signal. If an event were to occur before the delay time expired or before the pre-scaling was completed, this event would be ignored.

THE EVENT PULSE

When an event pulse arrives after scaling has begun in the main scaler, the pulse train is interrupted while storage occurs in the memory. The update scaler monitors time for its pre-selected duration after which the main scaler is updated and counting is resumed. This process is continued until the register overflows which causes an automatic reset and awaits the arrival of the next start pulse.

STOP

A stop signal aborts the run, clears all scalers, inhibits transfer and awaits the next signal.

SINGLE PARTICLE ANALYSIS

In this mode, the time-of-flight module stops after an event signal is transferred to the memory and awaits another start signal.

PULSE WIDTH ANALYSIS

This mode of operation is used to determine the length of time a pulse exists above a predetermined value. The signal to be measured is connected to the start input. The leading edge of the pulse, or its rise above baseline, acts as a start signal. The scaler continues to count until the trailing edge or its decay to baseline occurs, and counting is stopped. The leading edge acts as a start pulse while the trailing edge acts as the event pulse. Reset is automatic upon the arrival of the next pulse.

PACKAGING FLEXIBILITY

Construction of this unit is almost exclusively of integrated circuits. The components are mounted on plug-in cards and packaged in NIM-NASA standard modules. Voltage levels were standardized in agreement with the AEC Committee Report TID-20893.

EXPERIMENTAL FLEXIBILITY

This module is designed to plug-in the data acquisition section of the multimode system. It can be used independently or in conjunction with other multimode modules. Experiments of single parameter or N-parameter can be performed without circuit modification. It can be used with other time of flight modules or an analog to digital converter in multi-parameter experiments. Two time of flight units can be used simultaneously with external logic, to eliminate shadow areas or to increase the range. Several units can be used to provide several windows.

CONCLUSION

The results of research and development work on the time of flight unit exceeded our most optimistic goals. The module can satisfy experimentalists in several fields. It can be built for $2500.00.

Future work in the time of flight area would be limited to a design of a unit using faster logic to obtain increased resolution.

A prototype time of flight unit will be provided NASA for extended evaluation.

SUMMARY - COINCIDENCE SYSTEMS

Coincidence experiments are increasing in importance in experimental endeavors ranging from nuclear structure studies to determination of elemental composition of materials. The wide variety of detectors and coincidence time requirements encountered in these experiments meant a sizable investment in equipment to meet the electronic demands of the individual experimenter. Due to the large assortment of devices necessary to perform typical experiments of this nature, the experimenter was forced to pay relatively high prices for each module because the economic benefit derived from high volume production was totally lacking.

Improvements in both commercially available components and circuit design indicated that a consolidation of functions in the components of the system might contribute to higher volumn production and lower overall cost. An attempt was made to reduce the cost of coincidence systems while simultaneously improving the operation and performance characteristics of the individual system components. This contract provided for studies of this nature to be carried out. As a result of this work, a new pre-amplifier, amplifier, time pick off/delay module, fast coincidence gate module

and power supply were designed. The modules were designed to comprise a versatile coincidence system applicable in all areas of coincidence counting experiments.

The primary motivation behind the pre-amplifier design was to produce a pre-amplifier which would be compatible with any detector. This eliminates the necessity for a pre-amplifier performing a single role in an overall counting system. The results of this design were very impressive; not only is the preamplifier compatible with all types of detector, but the low noise characteristics of the device make it very desirable in the most sophisticated high resolution counting system. The amplifier, like the pre-amplifier, proved to be beyond design expectations and in recent studies contributed the least distortion and noise contribution of any amplifier tested. The combination of the pre-amplifier and amplifier where pre-amplifier power is provided by the amplifier, is ideally suited for high resolution studies with or without coincidence operation. These two devices appear to be significantly better than those previously available in the same price region.

The time pick off/delay module design incorporates operational features superior to existing units, allows a reduced selling price, and provides a

variable delay for detector system time matching. In general, the test results obtained with this module, although impressive, indicated more thought should be given to this problem. As a result of this further investigation, another design is presently under way to improve the time reference for each pulse. The present studies indicate that high gain, non-linear amplification at the pre-amplifier input might provide greater accuracy. However, the present time pick off/delay module has proved to be comparable with the specifications of other units of this type.

The final module within the coincidence system is the fast coincidence gate. The module contains continuously variable time resolution, 2 t from 20 nanoseconds to 200 nanoseconds. At the time this report was written, tests were still being conducted on this module. Additional work is required to insure complete satisfaction of the design specifications.

INTRODUCTION-COINCIDENCE SYSTEMS

The value of fast coincidence systems in studying nuclear reactions or in determinations involving the elemental mixtures in materials has been adequately established. In routine counting systems coincidence techniques have not been widely used due to a variety of reasons. One primary restriction on widespread use of such techniques is the relatively high investment required to assemble a system. Of secondary importance are such things as timing limitations, adaptability with existing equipment, and duplication of routine system components.

Our initial goal under this contract was to attempt to solve the timing problems associated with coincidence systems. In particular we were interested in the problems involved when using dissimiliar detectors; i.e., lithium drifted germanium and sodium iodide. The primary reason for interest being the difference in signal rise time. As work progressed, it became apparent that the possibility existed of producing an entire coincidence system. The project was expanded to include: High Voltage Supply, Pre-Amplifier, Amplifier, Single Channel Analyzer, Time Pick Off/Delay Module, and Fast Coincidence Gate module.

The main effort under this contract centered about the Time Pick Off/Delay Module and Coincidence Gate Module. Additional engineers were added to the project to design and construct the remainder of the modules. The entire coincidence system is outlined below:

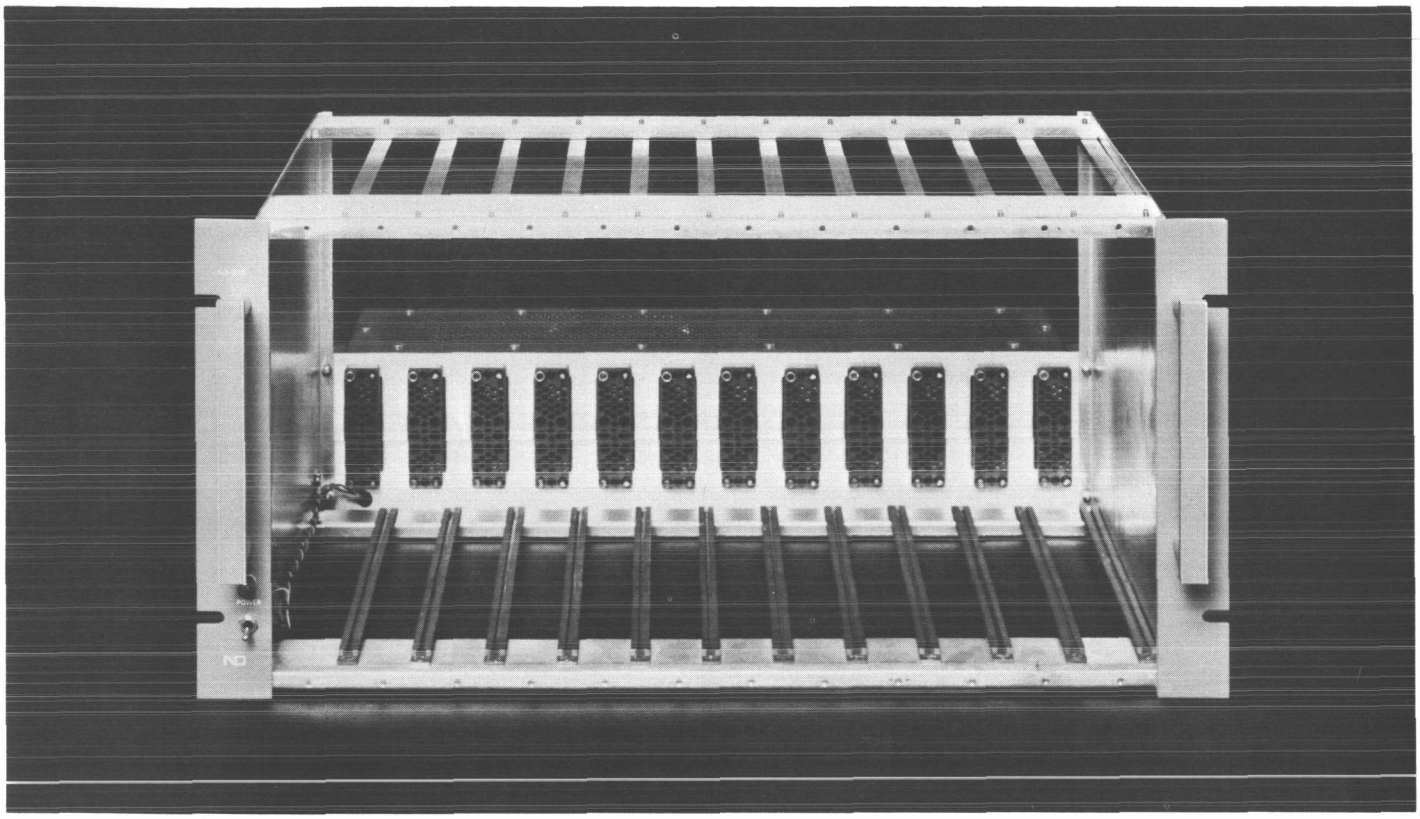
PACKAGING CONSIDERATIONS

Prior to starting design of the coincidence system, it was decided that any instrument developed should conform to the AEC Committee on Nuclear Instrumentation Report TID-20893. NASA has also widely accepted these standards for size, power requirements, connectors and other features. As a result of using these standards, any resulting instrument would be usable in any bin available, regardless of the manufacturer. Figure 3 shows a standard bin and power supply. Further effort would be made to keep module sizes to a minimum in order to conserve space and save on the number of module widths used. Each modular width costs approximately $60.00 in bin space.

TECHNICAL SPECIFICATIONS

NUCLEAR DATA INC.
100 West Golf Road
Palatine, Illinois 60067
Phone A.C. 312 • 529-4600

ND-510 MODULAR INSTRUMENTATION BIN AND ND-527 BIN POWER SUPPLY



The ND-510 Modular Instrumentation Bin and ND-527 Bin Power Supply provide mechanical and electrical facilities to accommodate a wide variety of nuclear instrument modules. Both units conform to the recommendations of the A.E.C. Committee on Nuclear Instrumentation as outlined in AEC Report TID-20893.

ND-510 MODULAR INSTRUMENTATION BIN

Up to twelve single width modules, or combinations of multiple width modules can be mounted in the ND-510 Bin. A welded cadmium-plated steel frame, combined with aluminum module guides and rear panel, provides exceptional strength and lightness. The bin power switch and indicator lamp are located on the front mounting flange for ease of accessibility without sacrifice of module space.

Dimensions: 8-3/4" high x 19" wide x 10-3/4" deep (depth with power supply is 16-1/4").

Weight: Approximately 9 pounds (less power supply).

Module Receptacles: Twelve AMP type 202516-3.

Receptacle Wiring: All receptacles are wired in parallel in accordance with AEC Report TID-20893.

ND-527 BIN POWER SUPPLY

All D.C. operating voltages required for module operation, as outlined in AEC Report TID-20893, are provided by the ND-527 Bin Power Supply. This unit is the Power Designs Model AEC-320-3, a multi-output silicon solid state D.C. power supply.

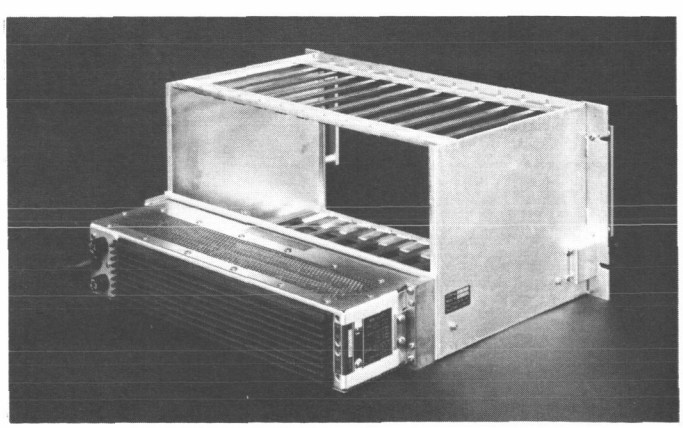


FIG 3

MECHANICAL

Dimensions: 3.5" high x 16.9" wide x 5.5" deep.

Weight: Approximately 18 pounds.

ELECTRICAL

Power Requirements: 103-129 or 206-258 vac, 50-65 Hz, single phase, 200 watts maximum.

Operating Temperature Range: 0-50° centigrade (0-60° centigrade with 3% derating).

Output Voltage and Current Rating:

A Supply = +12 vdc at 2 amperes.
B Supply = −12 vdc at 2 amperes.
C Supply = +24 vdc at 1 ampere.
D Supply = −24 vdc at 1 ampere.

Note: Total combined output must not exceed 72 watts.

Regulation: ±0.1% for 100% change in load or line variations within operating range.

Ripple and Noise: 3MV peak-to-peak, max.

Temperature Coefficient: 0.02%/°C between 0°C and 60°C.

Stability: ±0.3% maximum voltage variation over 24-hour period after 60-minute warm-up including variations due to load or line changes within the operating range.

Long-Term Stability: Maximum drift less than ±0.5% over 6-month period at constant load, line or ambient temperature conditions after 24-hour warm-up.

Voltage Adjustment Range: ±1%, nominal.

Voltage Resettability: ±0.05%, max.

Current Limiting Threshold:

2.2 amperes, min., for 12-volt supplies.
1.2 amperes, min., for 24-volt supplies.

Printed in U.S.A. 5/67

HIGH VOLTAGE POWER SUPPLY

One expensive requirement of coincidence systems or of any detector system, is the power supply. Normally, several different types of power supplies are needed to satisfy experimental requirements NaI systems consume a large amount of current. Ge(Li) systems require exceptional stability and protection against sudden power failure (actually, the FETs in the preamp of Ge(Li) systems require this protection). Proportional counters require higher voltages than other detectors. A typical power supply is shown in Figure 4. Note that it is specifically designed for solid state detectors.

With these various and divergent requirements in mind, an attempt was made to design an all purpose power supply to aid in the reduction of costs of total coincidence systems. It was recognized that different power supplies were needed for detectors in use in any coincidence experiment. These extra components contributed greatly to the overall system cost. Another routine variable in all systems was the pre-amplifier which again contributed to the system cost. The high voltage supply and pre-amplifier were considered to represent one phase of this project. Work was begun on the simultaneous development of both modules.

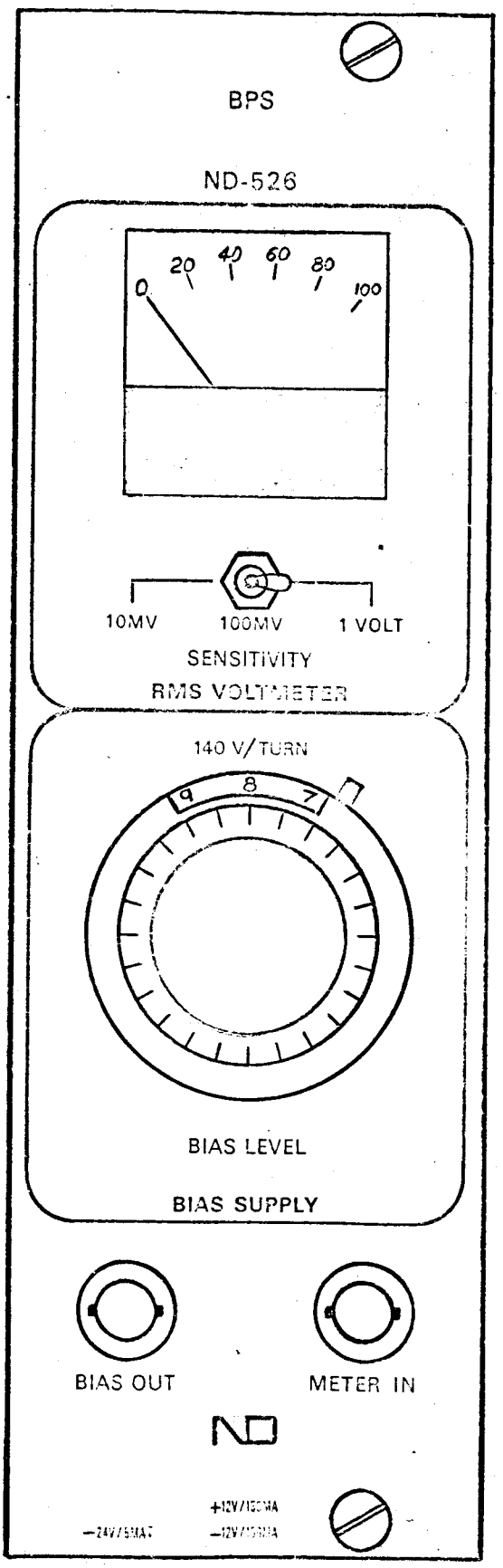

BPS
ND-526
0
20
40
60
80
100
10MV
100MV
1 VOLT
SENSITIVITY
RMS VOLTMETER
140 V/TURN
9
8
7
BIAS LEVEL
BIAS SUPPLY
BIAS OUT
METER IN
ND

FIG 4

The result of this effort was a very stable high voltage power supply designed for biasing all types of detectors (Figure 4). Detector bias voltages up to 2500 volts D.C. were obtained by conversion of a relatively low D.C. voltage to a 25 kilohertz, A.C. voltage by means of an electronic "chopper". This A.C. voltage is rectified, doubled, filtered and applied across a series combination of miniature gaseous reference elements which provide a highly stable source voltage for constant current loads. (See Figure 5.)

Two front panel controls provide adjustment of the output voltage over a range of 0 to 2500 volts. An eleven position switch provides coarse adjustment with a range of 0 to 2250 volts in 250 volt steps, and a single turn potentiometer provides fine adjustment with a continuous control range of 250 volts for each increment of the coarse adjust switch.

Two separate controls were required because a potentiometer with a range of 0 to 2500 volts is not commercially available. The maximum rate of change of the output voltage is limited by a 0.2 second time constant. This protects both the detector and preamplifier inputs from damage which may result from sudden adjustment-induced voltage changes.

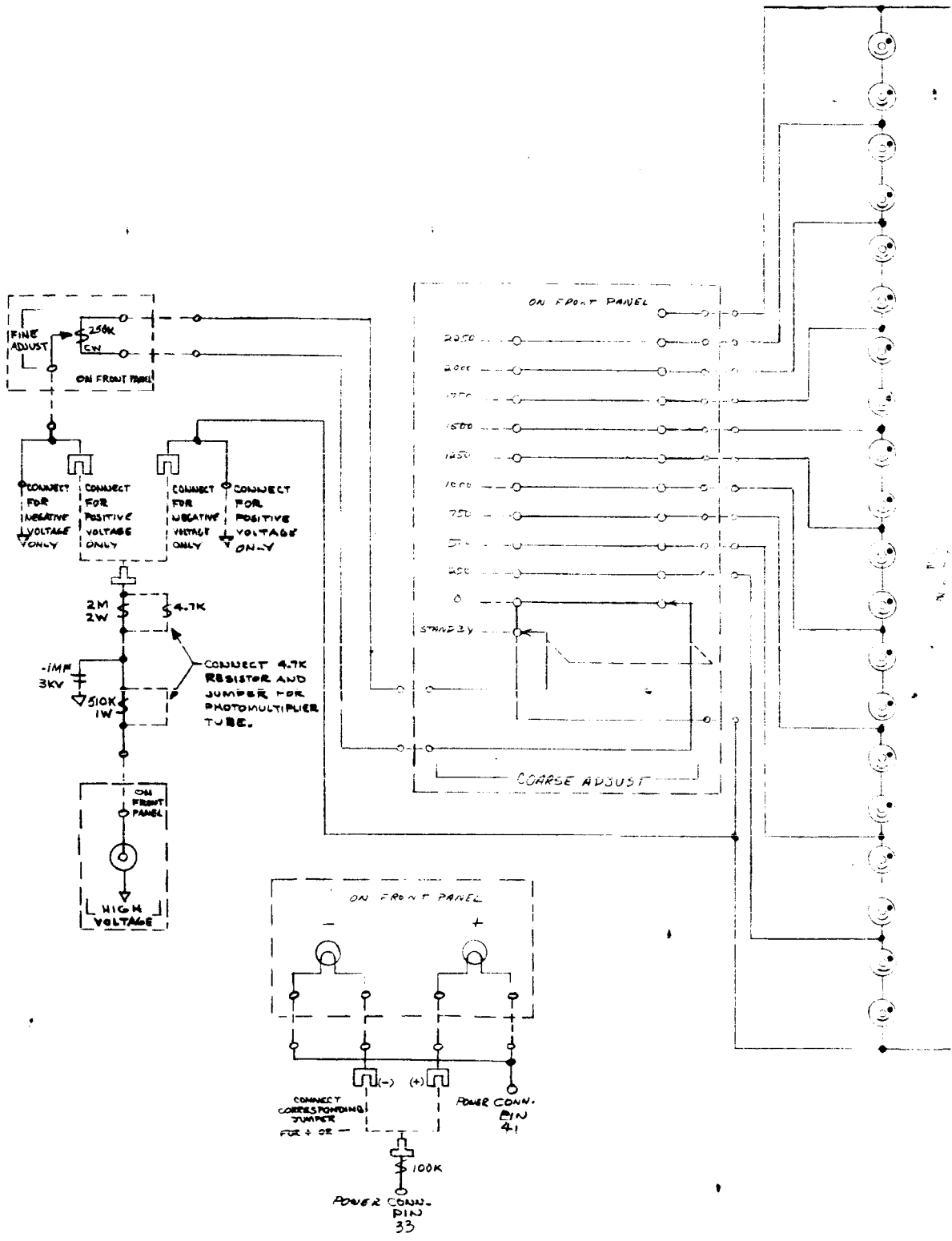
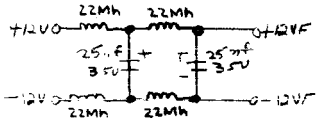
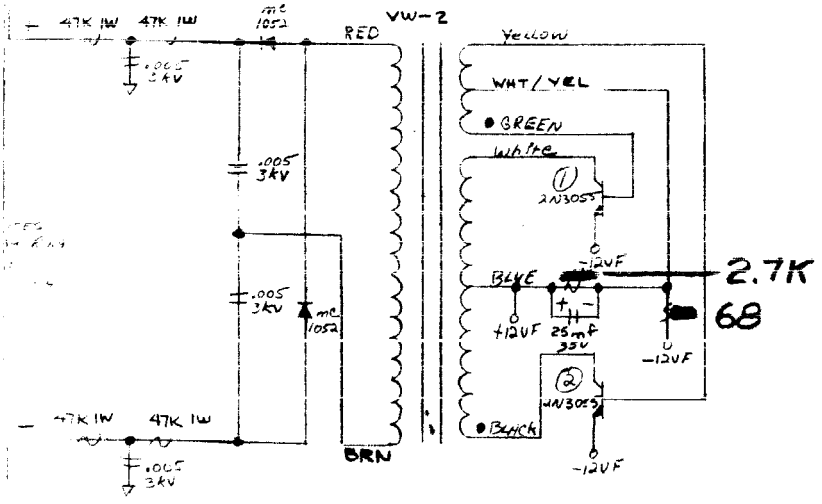

FINE ADJUST
250K
CW
ON FRONT PANEL
CONNECT FOR NEGATIVE VOLTAGE ONLY
CONNECT FOR POSITIVE VOLTAGE ONLY
CONNECT FOR NEGATIVE VOLTAGE ONLY
CONNECT FOR POSITIVE VOLTAGE ONLY
2M 2W
4.7K
.1MF 3KV
510K 1W
CONNECT 4.7K RESISTOR AND JUMPER FOR PHOTOMULTIPLIER TUBE.
ON FRONT PANEL
HIGH VOLTAGE
ON FRONT PANEL
2250
2000
1750
1500
1250
1000
750
500
250
0
STANDBY
COARSE ADJUST
ON FRONT PANEL
−
+
(−)
(+)
CONNECT CORRESPONDING JUMPER FOR + OR −
POWER CONN. PIN 41
100K
POWER CONN. PIN 33

Fig 5-1





Power Connector

SIGNAL

+12V	16
-12V	17
Sig GND	4A
P.R.G.	3V
115VAC	33
	41

ON REAR PANEL

NOTES:
1 – ALL DIODES ARE GD 548 OR EQUIVALENT, EXCEPT AS NOTED.
2 – ALL RESISTORS ARE 1/4W, 5%, EXCEPT AS NOTED.
3 – ALL CAPACITORS ARE pf, EXCEPT AS NOTED.
4 – SYMBOLS:
- SELENIUM
- SILICON
- GERMANIUM
- ZENER
- TUNNEL
- SIG GND

USED ON

ASSEMBLY NO.

ND-537/[redacted]
74-0104

NUCLEAR DATA INC
POST OFFICE BOX 451, PALATINE, ILLINOIS 60067

DIAGRAM, Schematic
(HVS) Board

DRAWN BY: JDC	CHECKED BY: [illegible]	570-0165-[redacted]
DATE DRAWN: 3/30/67	APPROVED BY:	

FORM NDS-103

01

FIG 5

Versatility is a prime factor in the design of the high voltage supply module in that, by simply relocating internal jumpers, the module is adapted for biasing photomultiplier type detectors or detectors requiring negative bias voltages.

The high voltage supply is housed in a standard AEC double width module and operates with standard bin power supply voltages.

Specifications of the high voltage supply are as follows:

Output Voltage: 0 to 2500 volts D.C.

Output Current: 1 milliampere, maximum.

Output Polarity: Positive (negative output obtained by relocating two jumper wires).

Output Impedance: 510 kilohms (4.7 kilohms output impedance obtained by adding a resistor and a jumper wire for use with photomultiplier type detectors)

Output Ripple: 0.001% (25 millivolts peak to peak at full load; 2500 volts D.C. at 1 milliampere).

Bias Stability: Temperature -- 0.013% per degree centigrade, A.C. line voltage -- 0.0005% per 10% change in line voltage.

Regulation: 0.8% full load to no load.

Bias Control: Coarse -- 0 to 2250 volts in 250 volt steps.

Fine ----250 volt continuous range for each coarse step.

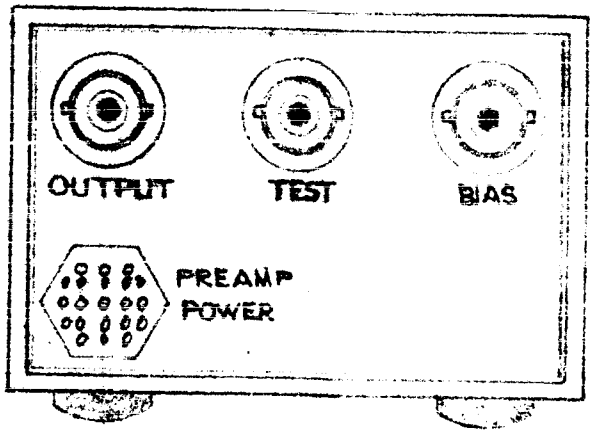
Output Time Constant: A 0.2 second time constant limits the maximum rate of change of the output voltage.

The final design, therefore, has the voltage range required by proportional counters, the stability required by Ge(Li) detectors, the current output for NaI detectors, and the protection required by Field Effect Transistor preamplifiers. All design goals on the high voltage supply were accomplished.

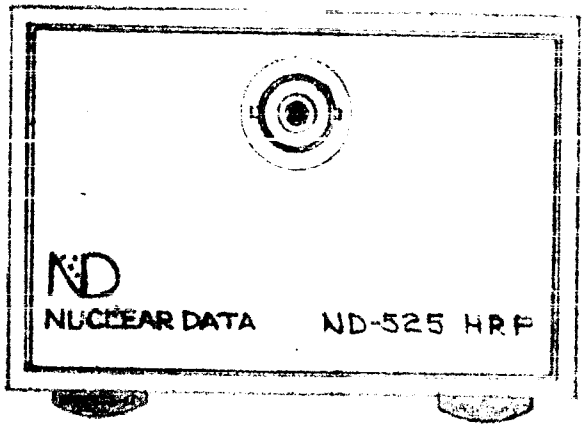
PRE-AMPLIFIER

The goal in pre-amplifier design was to simplify the circuitry and at the same time develop an all purpose pre-amplifier. Previous pre-amplifiers were designed for specific applications.

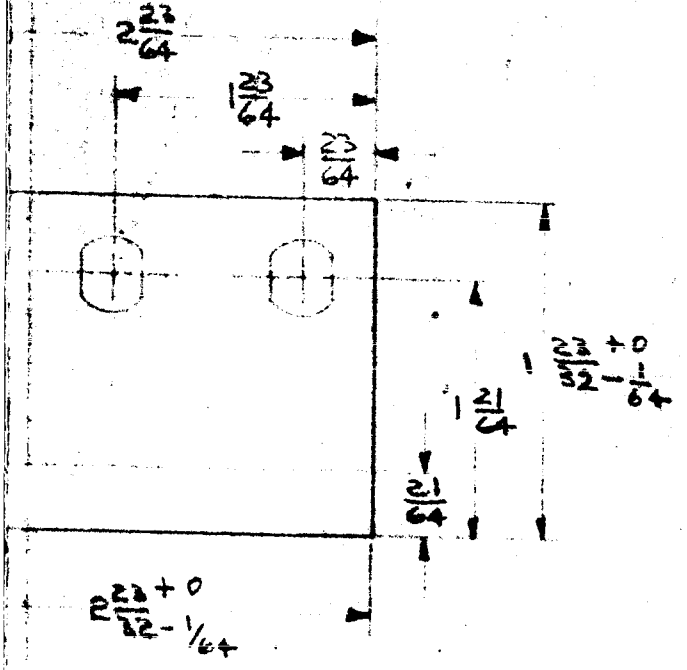
The result of this development is a charge-sensitive pre-amplifier which provides good resolution for use with semi-conductor detectors operating at room temperatures and has the necessary sensitivity for use with low-energy scintillation detectors and proportional counters (Figure 6).



REAR



FRONT



FRONT AND REAR PANEL
ND-525 HRP LAYOUT.
G.M.W. 8/3/66

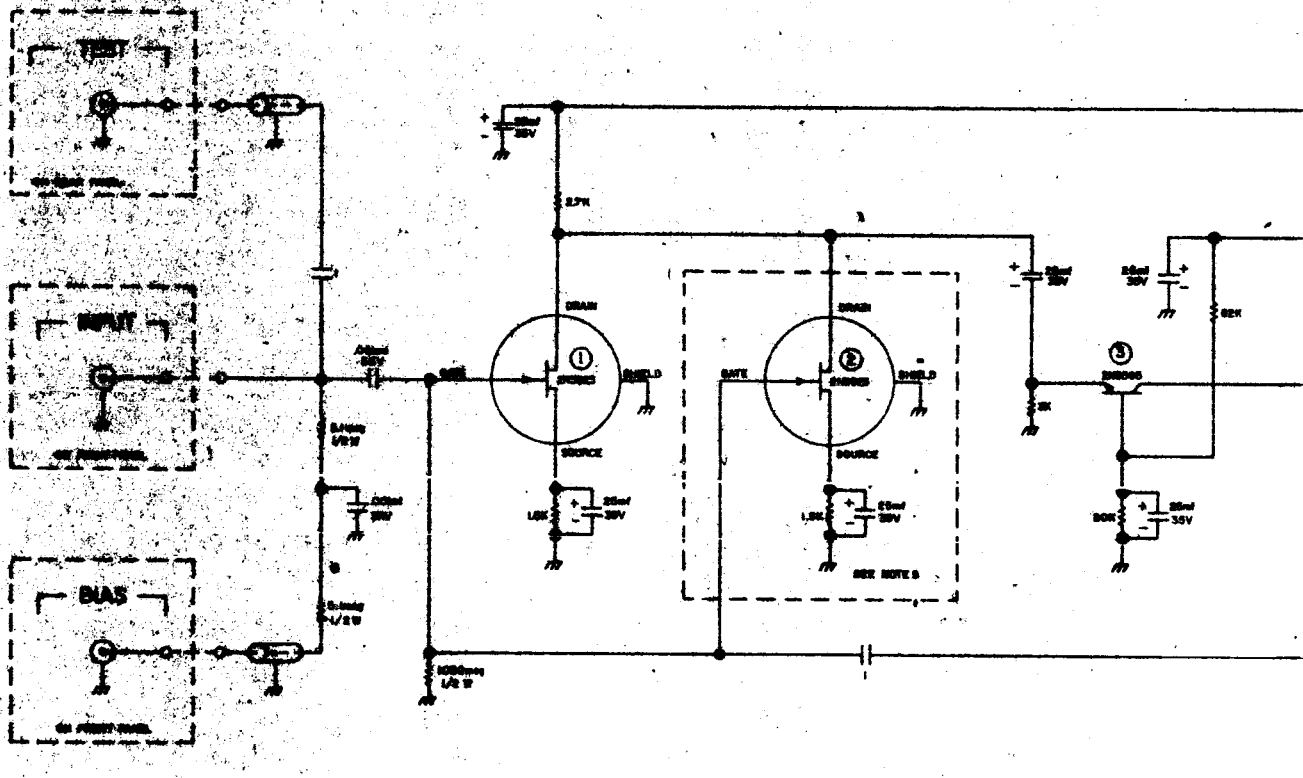
FIG 6

The pre-amplifier is comprised of a double field effect transistor (FET) input and a line driver (Figure 7). The preamplifier normally accepts negative charge inputs, however, by relocating three jumper wires, it will accommodate positive charge inputs.

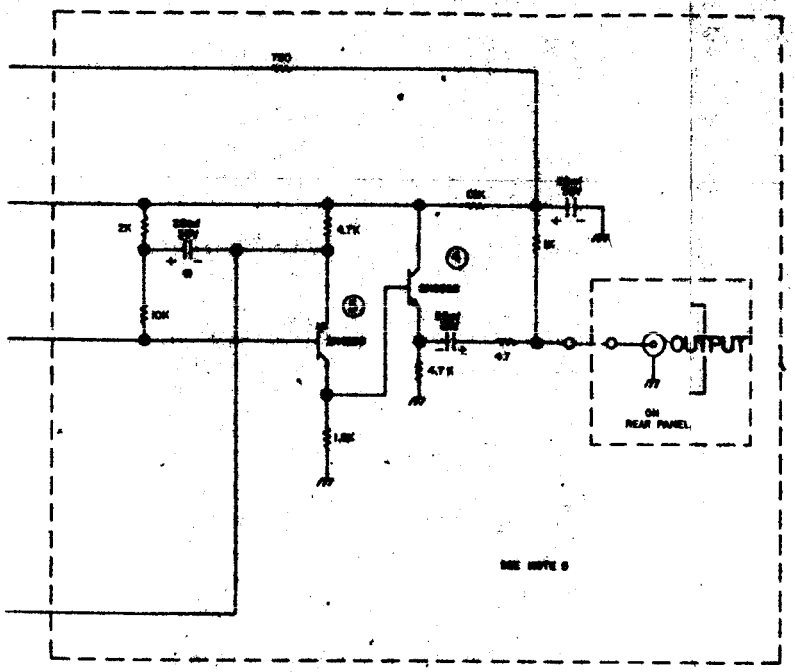
The change-over from solid state detectors to scintillation detectors or proportional counters requires the change of two components, the input capacitor and resistor in the bias circuit. The required values are as follows:

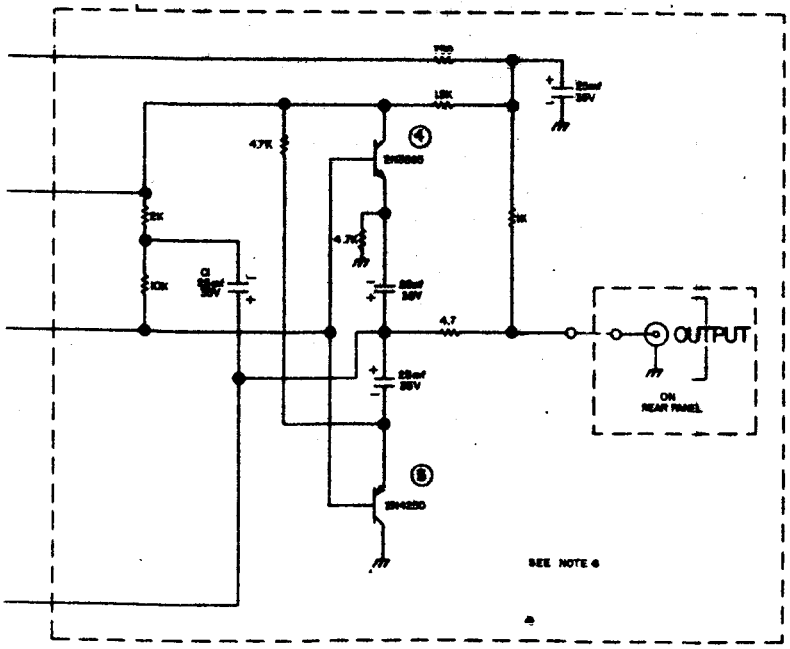
Type Detector	Input Capacitor	Bias Resistor
Ge(Li)	.001mf	5.1 meg
Proportional Counter	.010 mf	1.0 meg
Scintillators	.100 mf	100K

An additional saving was made possible by bringing operating power, +24 V d.c. through the same cable that carries the output signals. By tying this preamplifier to the amplifier designed for the coincidence system, additional savings were made possible. In addition to the pre-amplifier input and output connectors, two connectors, designated TEST and BIAS, were provided. The TEST connectors provide an input for application of a proper polarity voltage pulse to check system performance. The BIAS connector provides an input for application of high



NOTES:
1 – ALL
2 – ALL
3 – ALL
4 – 9V





USED ON

ASSEMBLY NO.

DIODES ARE GD 548 OR EQUIVALENT, EXCEPT AS NOTED.
RESISTORS ARE 1/4W, 5%, EXCEPT AS NOTED.
CAPACITORS ARE pf, EXCEPT AS NOTED.
SYMBOLS:
— SELENIUM
— SILICON
— GERMANIUM
— ZENER
— TUNNEL
SHIELD GND

5 — USE THIS FOR POSITIVE INPUT.
6 — USE THIS FOR NEGATIVE INPUT.
7 — POLARITY OF CAPACITOR C1 MUST CHANGE ON THE EC. BOARD ACCORDING TO SCHEMATIC.
8 — ⊕ FOR POSITIVE CHARGE INPUT.
⊖ FOR NEGATIVE CHARGE INPUT.
9 — USE THIS CIRCUIT WHEN A SHARPER SLOPE IS DESIRED.

NUCLEAR DATA INC
POST OFFICE BOX 481, PALATINE, ILLINOIS 60067

DIAGRAM, SCHEMATIC
(PRE AMPLIFIER) BOARD

DRAWN BY: R.M.S.	CHECKED BY: F.C.W.	S7. -0162-00C
DATE DRAWN: 8-8-67	APPROVED BY: M.K.	

FIG 7

voltage (up to 2500 volts) to bias an external detector.

SPECIFICATIONS:

Input Polarity: Normally negative charge inputs; by relocating three jumper wires, positive charge inputs are accommodated.

Noise (Ge): 2 keV at 10 pF, external capacitance.

Noise Slope: .04 keV/pF, external capacitance.

Rise Time: 75 nanoseconds at 0 pF, external capacitance.

200 nanoseconds at 100 pF, external capacitance.

Output Polarity: Always positive.

Saturation Levels: +6 volts and -3 volts.

Integral Linearity: 0 to 1 volt, 0.1% or better.

Temperature Stability: 0.1% per degree centigrade.

Power Requirements: +24 V d.c. at 5 milliamperes.

The preamplifier design achieved the majority of the design requirements originally outlined. It can be used with all types of detectors by merely changing plug-in components; it can carry the high voltage requirements of proportional counters, it can be built for significantly less

than the price of competitive instruments which can be used with only one type of detector.

Further improvement is possible. The FETs used in this preamp have Gm of 4,000 to 5,000 and Cgs (capacitance gate to source) of 0.6pF. It appears that FETs with Gm of 15,000 and Cgs of 0.3pF could result in an improvement in preamplifier specifications from 2 keV noise to 1.5 keV and from 0.04 keV/pF noise slope for external capacitance to 0.2 keV/pF.

Another improvement which seems possible is the introduction of positive feedback. This could eliminate the noise slope increase with increased capacitance. Noise would be limited to 2 keV regardless of input capacitance.

AMPLIFIER

Generally speaking, amplifiers are the most complex module in a detection system. Since two or more are required in a coincidence experiment, amplifiers usually require large space and a sizeable portion of the investment in a coincidence system. A great deal of effort was, therefore, expended in designing the amplifiers for the coincidence system. A typical multipurpose amplifier is shown in (Figure 8).

The result of the amplifier development can be seen in Figure 9.

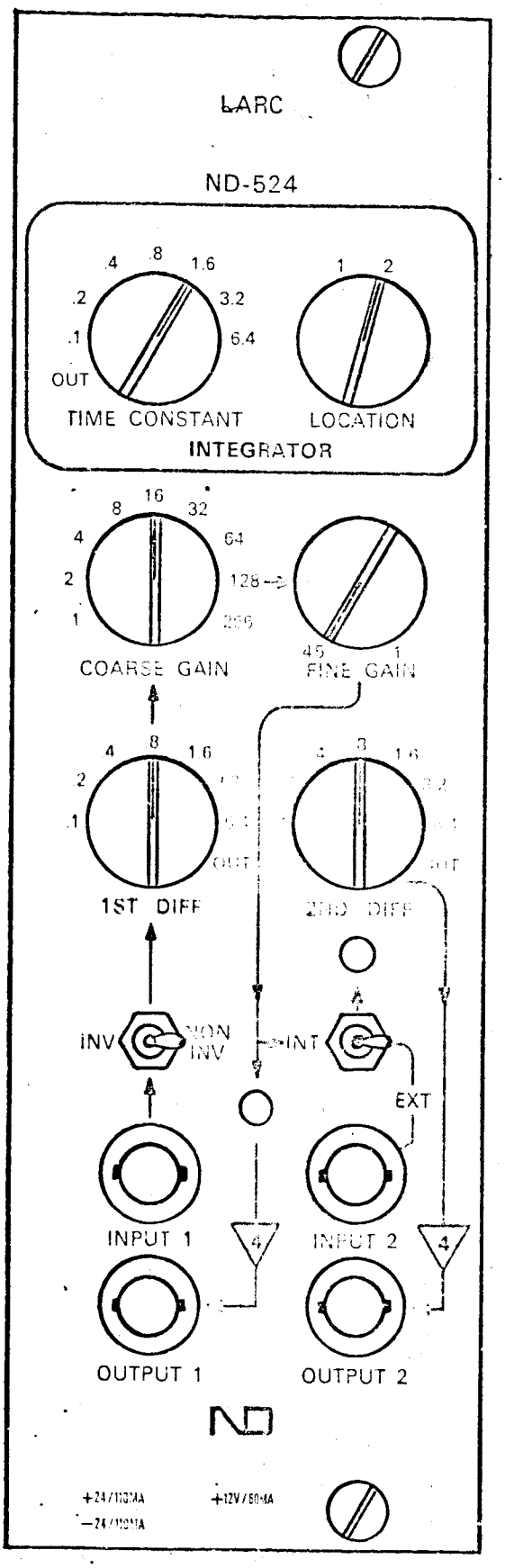

LARC
ND-524
.4
.8
1.6
.2
3.2
.1
6.4
OUT
TIME CONSTANT
1
2
LOCATION
INTEGRATOR
8
16
32
4
64
2
128
1
256
COARSE GAIN
45
1
FINE GAIN
4
8
1.6
2
.1
OUT
1ST DIFF
2ND DIFF
INV
NON INV
INT
EXT
INPUT 1
INPUT 2
4
4
OUTPUT 1
OUTPUT 2
+24/110MA
+12V/60MA
—24/110MA

FIG 8

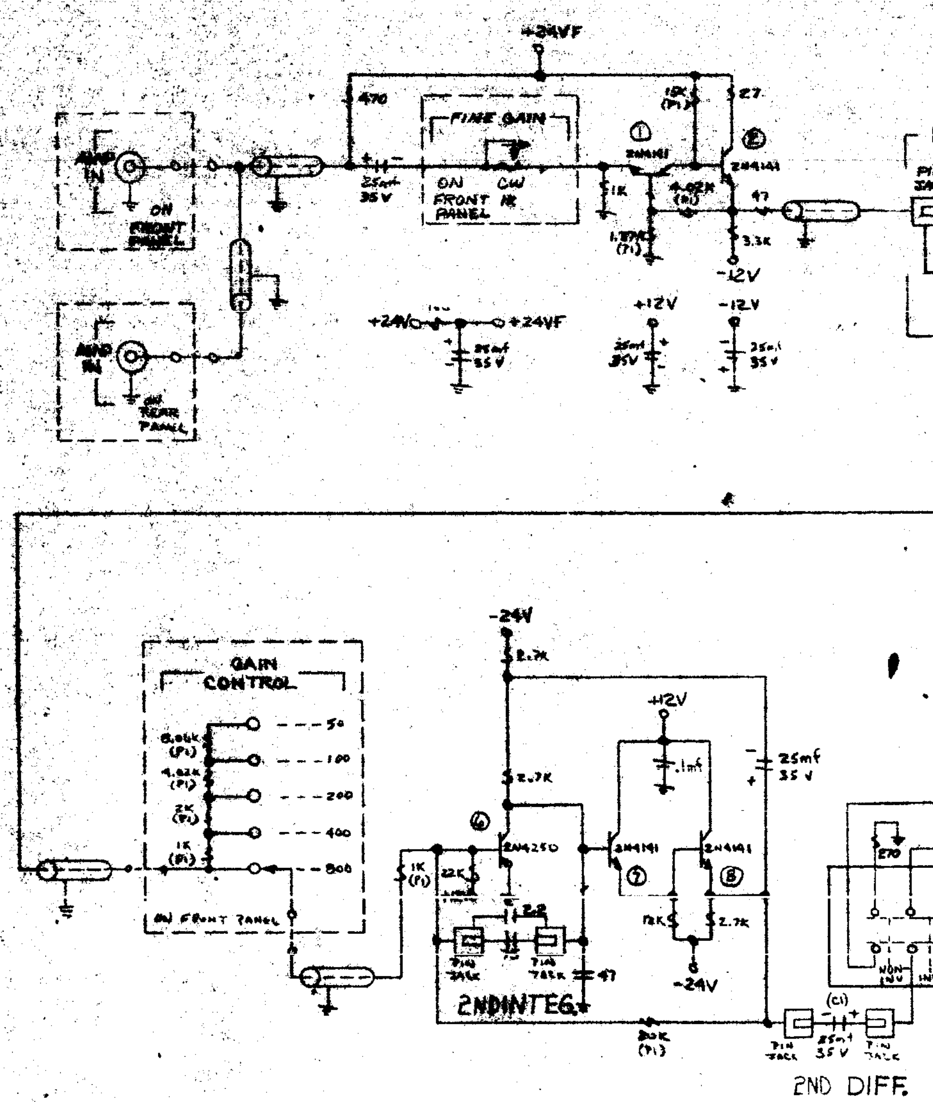
A number of features were incorporated to provide an excellent amplifier at a minimum cost. First, +24 volts was made available to drive the pre-amplifier through the amplifier input cable. This arrangement provided economies in both the pre-amplifier and amplifier.

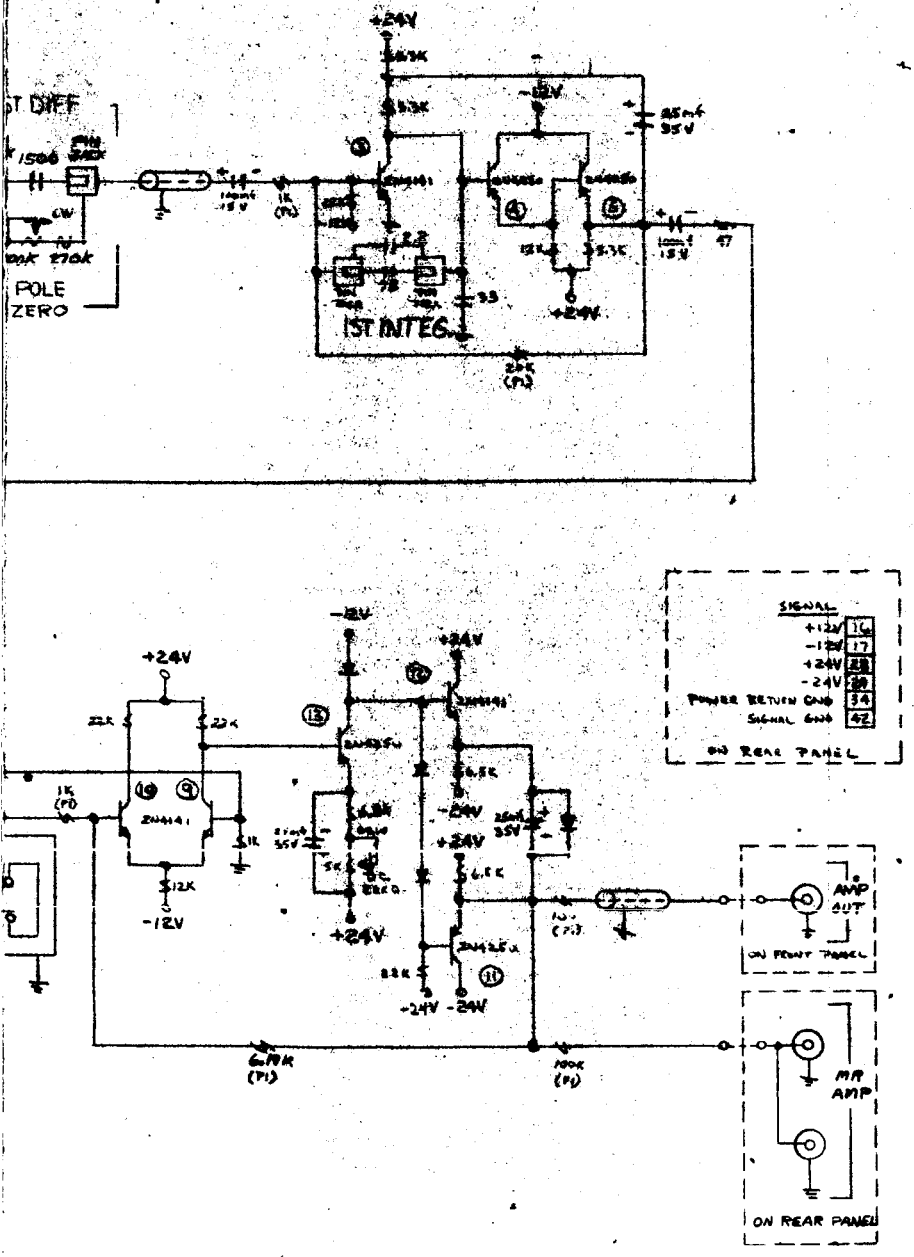
The next design feature of the system was to build in variable pole zero clipping.[4] By making this clipping adjustable, it was found that the pre-amplifier did not require pole zero clipping, and that the clipping need not be compensated for changes in time constants within the amplifier.

Another feature of the design was the removal of differentiator and integrator controls from the front panel. (See Figure 9). These controls have been replaced with plug-in capacitors on pin jacks for selection of time constants. There are four capacitors, two each for differentiators and integrators. This design has been incorporated because many users select optimum settings on their amplifiers and lock the amplifier in that position. The user still has the choice of single or double differentiation.

It should be pointed out that this amplifier was designed around two stages of differentiation and two stages of integration only. In theory, the larger the number of integration stages, the smaller the noise. By

(4) See "Elimination of Undesirable Undershoot in the Operation and Testing of Nuclear Pulse Amplifiers" - Nowlin and Blankenship - Review of Scientific Instruments, Volume 36 - number 12 - December 1965.


+24VF
470
FINE GAIN
ON FRONT PANEL
CW
25mf 35V
2N4141
27
1K
3.3K
-12V
+12V
+24V
AMP IN
ON FRONT PANEL
GAIN CONTROL
50
100
200
400
800
-24V
2.7K
+12V
25mf 35V
2N4250
2N4141
12K
-24V
47
2ND INTEG.
2ND DIFF.



NOTES:
1 - ALL DIODES ARE 6064 OR EQUIVALENT, EXCEPT AS NOTED.
2 - ALL RESISTORS ARE 1/4W, 5%, EXCEPT AS NOTED.
3 - ALL CAPACITORS ARE μf, EXCEPT AS NOTED.
4 - SYMBOLS:
- SELENIUM
- SILICON, 1N914B
- GERMANIUM
- ZENER
- TUNNEL
- POWER RETURN GND, SIGNAL GND (SEE NOTE 6)

5 - (P) ALL PRECISION RESISTORS ARE 1/8 W ±1% METAL FILM.
6 - THESE TWO GNDS JUMPER TOGETHER TO A COMMON GND
7 - (C) CHANGE TO 150pf FOR SECOND CUP

USED ON
ASSEMBLY NO.
NO. REQ. 7E2-0153

NUCLEAR DATA INC
POST OFFICE BOX 451, PALATINE, ILLINOIS 60067

DIAGRAM, SCHEMATIC
"ARC" BOARD

DRAWN BY: KWW	CHECKED BY:	S70-0163-00D
DATE DRAWN: 6-14-67	APPROVED BY:	

FIG 9

carefully designing the two stages of integration, a noise figure of 4.0 microvolts referred to the input was achieved with single differentiation and 5.0 microvolts with double differentiation. These figures are a factor of 2 or 3 better than existing amplifiers. Other specifications of the amplifier are also as good as or better than existing designs. We are quite happy with the results of the design effort on this amplifier.

Specifications of the amplifier are as follows:

Amplifier Input: Two BNCs (one front, one rear) accept positive, low level signals from a pre-amplifier. Input impedance is approximately 1000ohms.

Gain Stability: 0.03% per degree centigrade.

Gain Controls: Coarse: 50 to 800 in binary steps.

Fine: 0.5 to 1 continuous range between coarse steps.

Pulse Shaping: Two passive differentiators and two active integrators. First differentiator is pole-zero compensated to cancel undershoot effects. The RC shaping time constants can be changed by replacing four capacitors. These capacitors are equipped with pin jacks for easy insertion or removal.

Noise: 4.0 microvolts, referred to the input at maximum gain and with single differentiation and double integration or 5.0 microvolts with double differentiation and integration.

Overload: With single differentiation and double integration--Recovers from 500 x overload in 3 non-overloaded pulse widths.

Characteristic Rise Time: With single differentiation--300 nanoseconds.

Amplifier Output: Signal Characteristics--Front panel BNC provides positive or negative monopolar or bipolar voltage pulses (internal switch selectable).

Impedence -- 100 ohms

Saturation Levels -- +12 volts and

-12 volts.

Integral Linearity -- 0.1% from 0 to 10 volts.

M/R Amplifier Output: Signal Characteristics - Rear Panel BNC provides positive, monopolar current pulses.

Impedance -- 100K ohms.

Saturation Levels -- +0.12

milliampere and -0.12 milliampere.

Integral Linearity -- 0.1%

Single Channel Analyzer

Development of a single channel analyzer has not, as yet, started as part of this program. The design would be based on the single channel analyzer shown in Figure 10 and Figure 11.

As part of the program, however, it was found that integral discriminators could be useful in simple coincidence systems. A simple discriminator was, therefore, designed. Its mechanical configuration was such that it could fit into the amplifier module or be separately packaged in pairs (Figure 12).

Specifications on the discriminator are as follows:

Input: Impedance -- approximately 7.5 kilohms.

Sensitivity -- 30 millivolts to 10 volts, selected by a front panel control

Linearity: 0.5%, 30 millivolts to 10 volts.

Stability: 0.1% per degree centigrade.

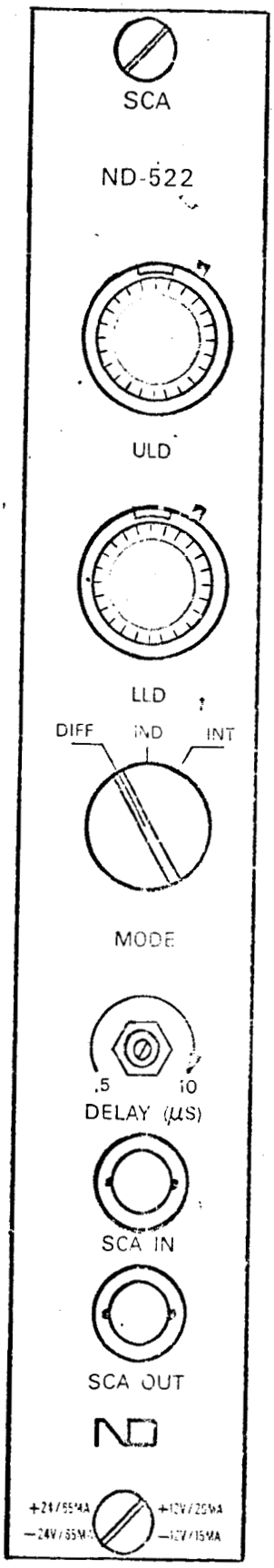
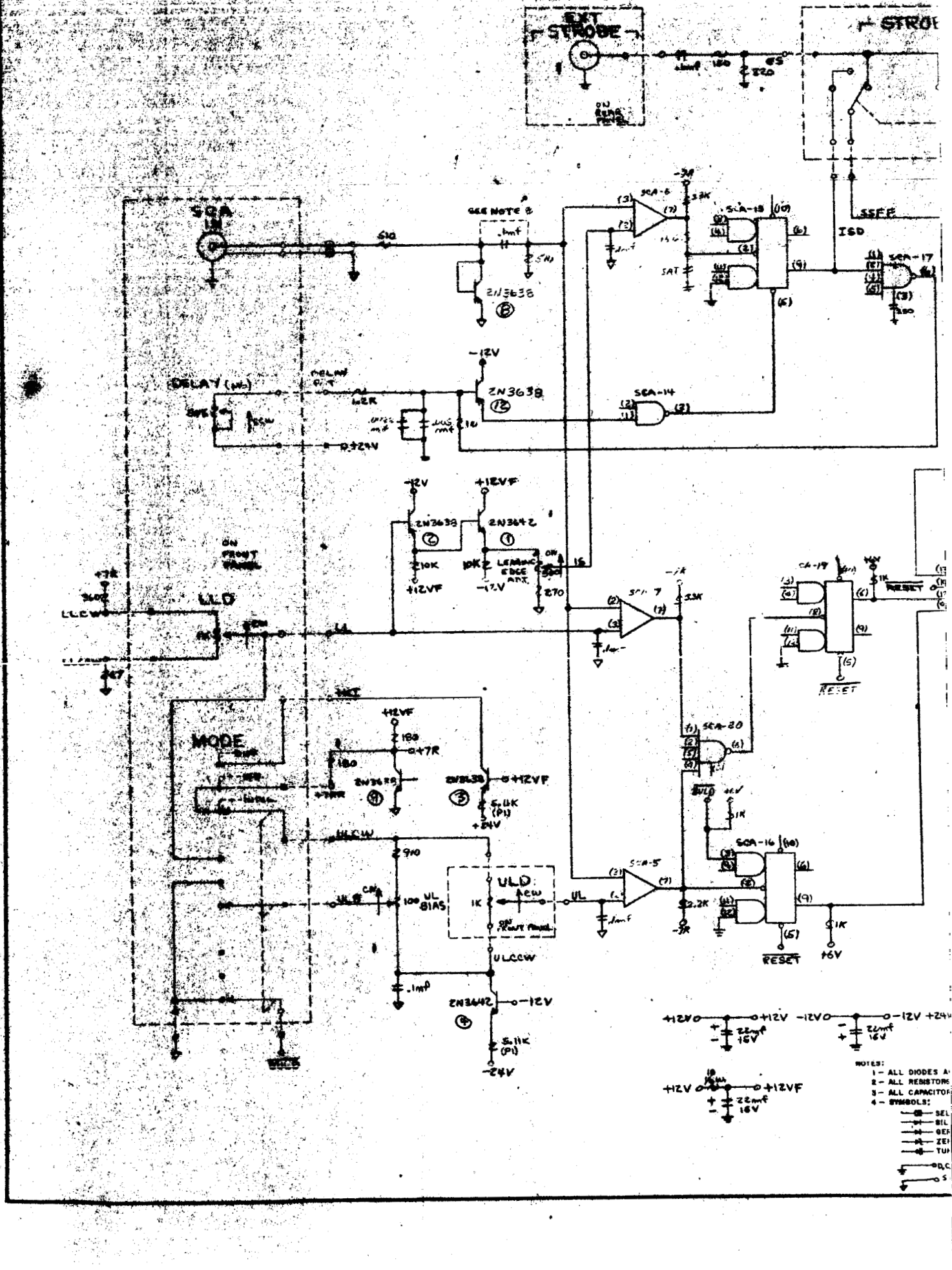
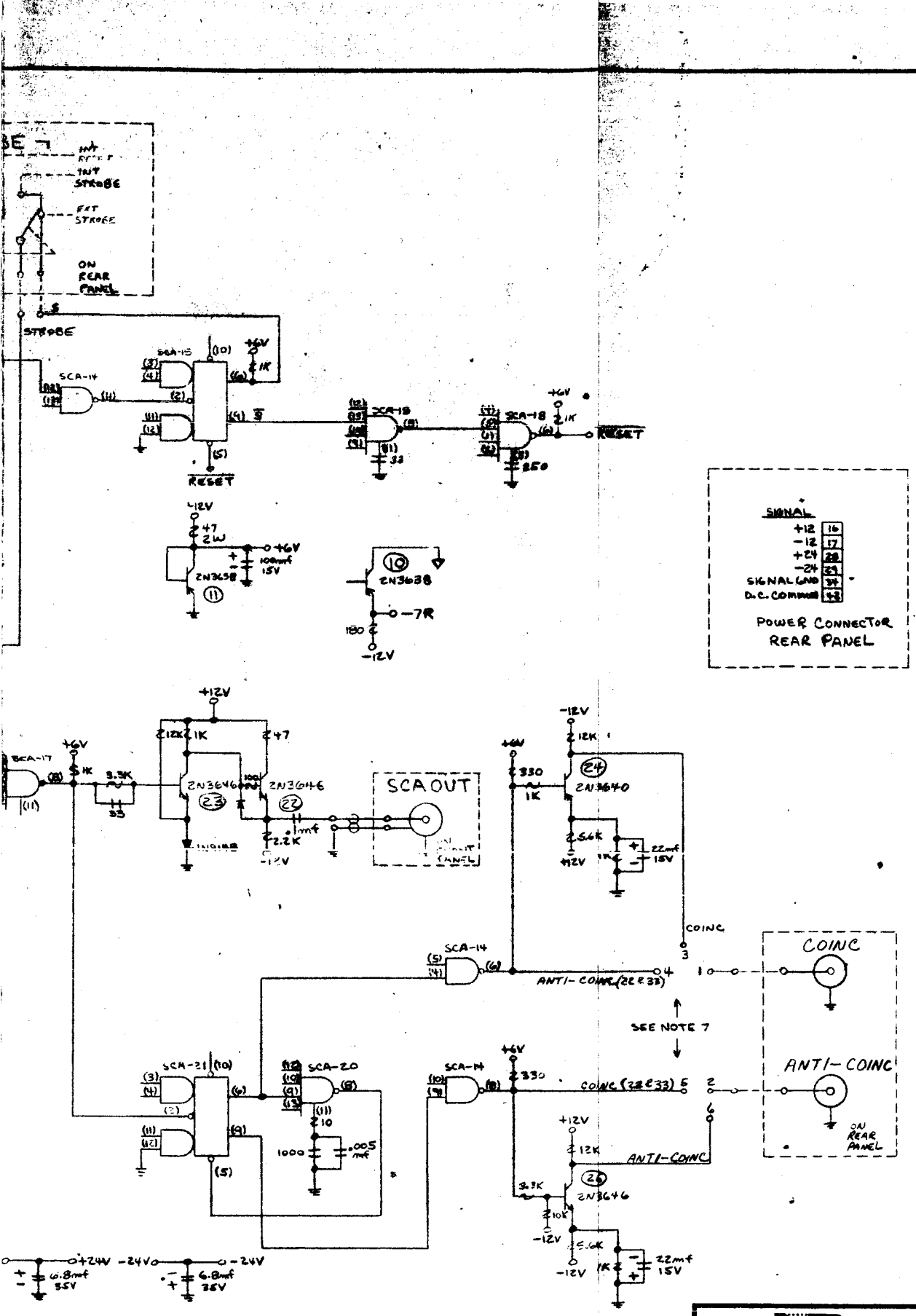

SCA
ND-522
ULD
LLD
DIFF
IND
INT
MODE
.5
10
DELAY (μS)
SCA IN
SCA OUT
ND
+24V/65MA
+12V/20MA
-24V/65MA
-12V/15MA

FIG 10


EXT STROBE
SCA IN
DELAY (μs)
MODE
ULD
ULCCW
SCA-6
SCA-13
SCA-17
SCA-14
SCA-7
SCA-19
SCA-20
SCA-16
SCA-5
2N3638
2N3642
RESET
NOTES:
1 – ALL DIODES A
2 – ALL RESISTORS
3 – ALL CAPACITOR
4 – SYMBOLS:



E 6964 OR EQUIVALENT, EXCEPT AS NOTED.
ARE 1/4W, 5%, EXCEPT AS NOTED.
ARE M, EXCEPT AS NOTED.

NIUM
ON
IANIUS
ER
IEL
OMMON
NAL GND

5. -(P1) ALL PRECISION RESISTORS ARE ¼ W. ± 1% METAL FILM.
6. INTEGRATED CIRCUIT HEADER VALUES:
   5,4,7 - μA710C 13,15,16,17,21 - 948 14-946 17-944 18,20-930
   24, 27, 28 - OPTIONAL HEADERS
   INTEGRATED CIRCUIT VOLTAGES:
   HDRS. 5&7, - PIN 1 - SIGNAL GND PIN 4 - -7R PIN 8 - +12VF
   BALANCE OF HDRS. - PIN 7 - D.C. COMMON PIN 14 - +6V
7. ND ANALYZERS 2200 & 3300, WIRE 1 TO 5 & 2 TO 4
   ALL OTHER ANALYZERS WIRE 1 TO 3 & 2 TO 6
8. INSERT THIS JUMPER FOR D.C. COUPLING.
4 S.C.T. SELECT AT TAT

USED ON

ASSEMBLY NO.

ND-582/89-0100

NUCLEAR DATA INC
POST OFFICE BOX 481, PALATINE, ILLINOIS 60067

DIAGRAM, SCHEMATIC "SCA" BOARD

DRAWN BY: R.J.C.	CHECKED BY: G.M.W.	S70-0381-05
DATE DRAWN: 9/6/67	APPROVED BY:	

FIG 11

Fig. 12

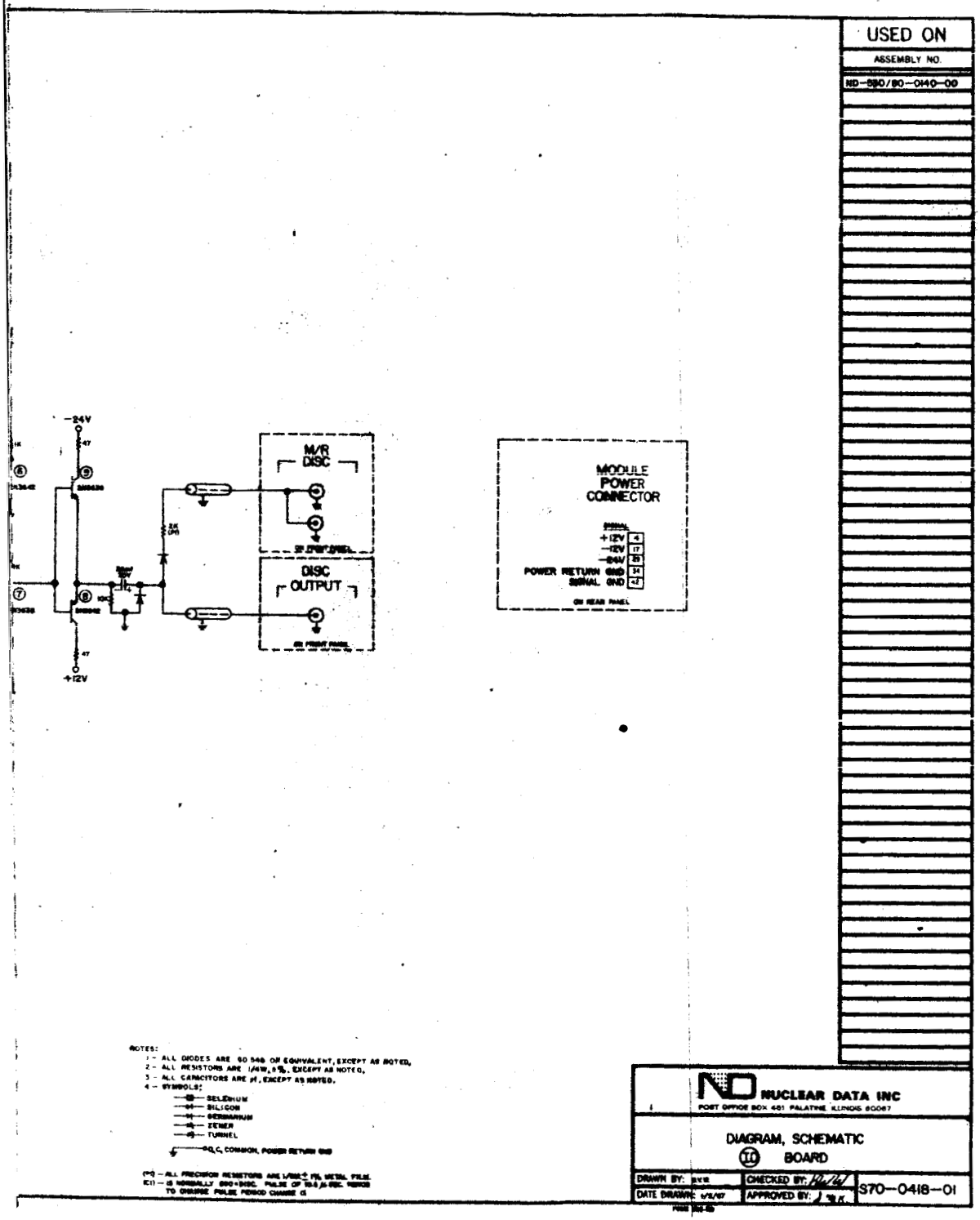

USED ON
ASSEMBLY NO.
ND-880/80-0140-00
-24V
+12V
M/R DISC
DISC OUTPUT
MODULE POWER CONNECTOR
+12V
-12V
-24V
POWER RETURN GND
SIGNAL GND
ON REAR PANEL
NOTES:
1 - ALL DIODES ARE 1N 548 OR EQUIVALENT, EXCEPT AS NOTED.
2 - ALL RESISTORS ARE 1/4W, 5%, EXCEPT AS NOTED.
3 - ALL CAPACITORS ARE pf, EXCEPT AS NOTED.
4 - SYMBOLS:
SELENIUM
SILICON
GERMANIUM
ZENER
TUNNEL
COMMON, POWER RETURN GND
NUCLEAR DATA INC
POST OFFICE BOX 451 PALATINE, ILLINOIS 60067
DIAGRAM, SCHEMATIC
BOARD
DRAWN BY:
CHECKED BY:
DATE DRAWN:
APPROVED BY:
S70-0418-01

FIG 12

Discriminator Output: Signal Characteristics -- Front panel BNC provides a positive 10 volt rectangular pulse.

Impedance -- 50 ohms.

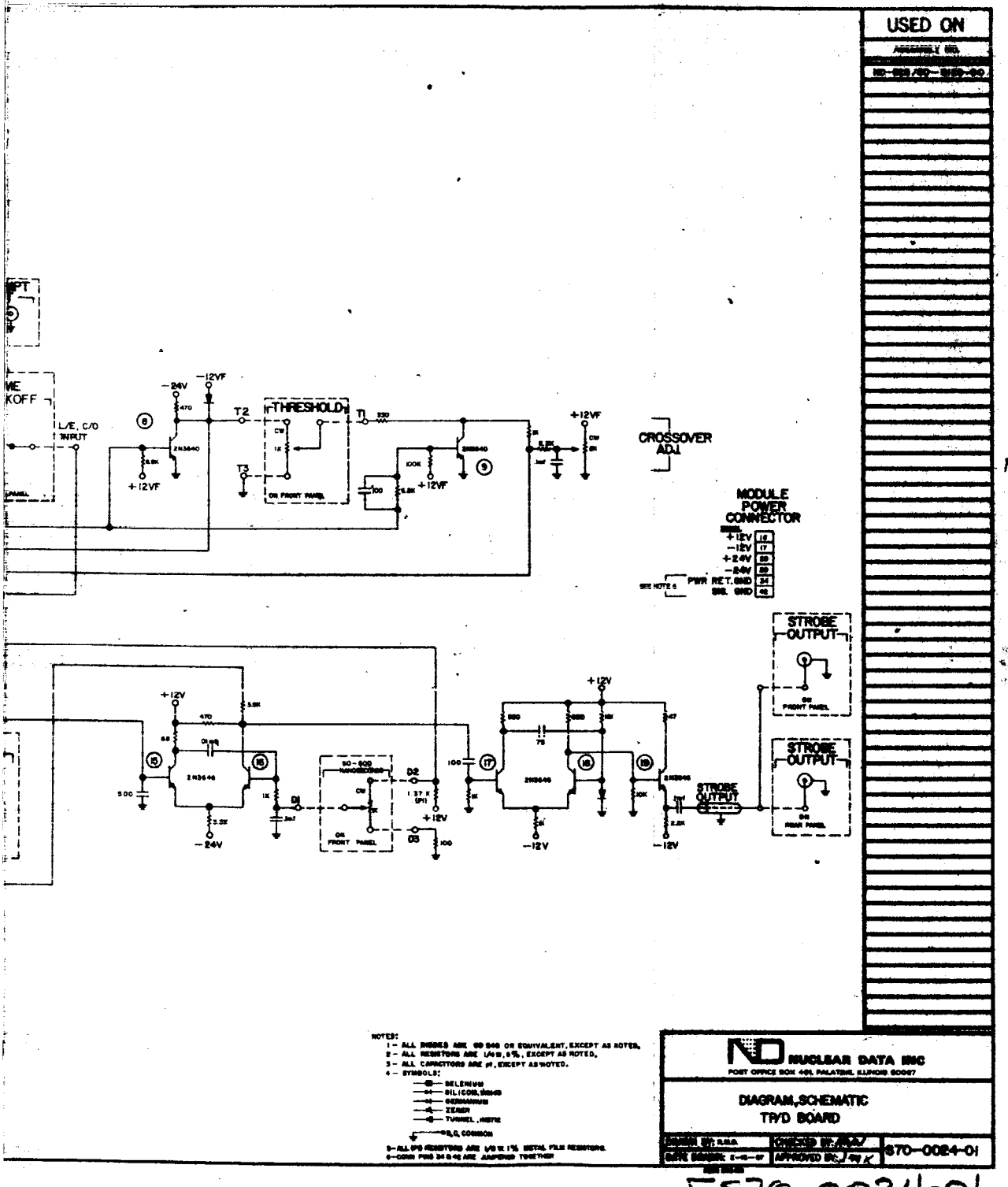
Pulse Shape -- Nominally 10 microseconds FWHM, 0.15 microsecond rise and fall times. Pulse width may be decreased to 0.5 microsecond minimum by a single component value change.

Time Pick-Off/Delay Module

The time pick-off module, Figure 13, is the portion of the coincidence system that provides an output pulse timed to a point on the input pulse. This point may be the leading edge of a unipolar or bipolar pulse or the cross-over point of a bipolar pulse. The outputs, or lack of one, from two or more time pick-off units are then fed to a coincidence gate, where a decision is made as to whether a coincidence or anti-coincidence occurred within some preset time.

A typical coincidence system may appear as indicated in Figure 14. Since there are two distinct sets of detectors and electronics up until the coincidence gate, the first problem we wished to eliminate was that of different timing lags on the two legs. In any coincident event, two particles interacting within the detectors simultaneously may not appear to be

FIG 1



E570-0024-01

FIG 13

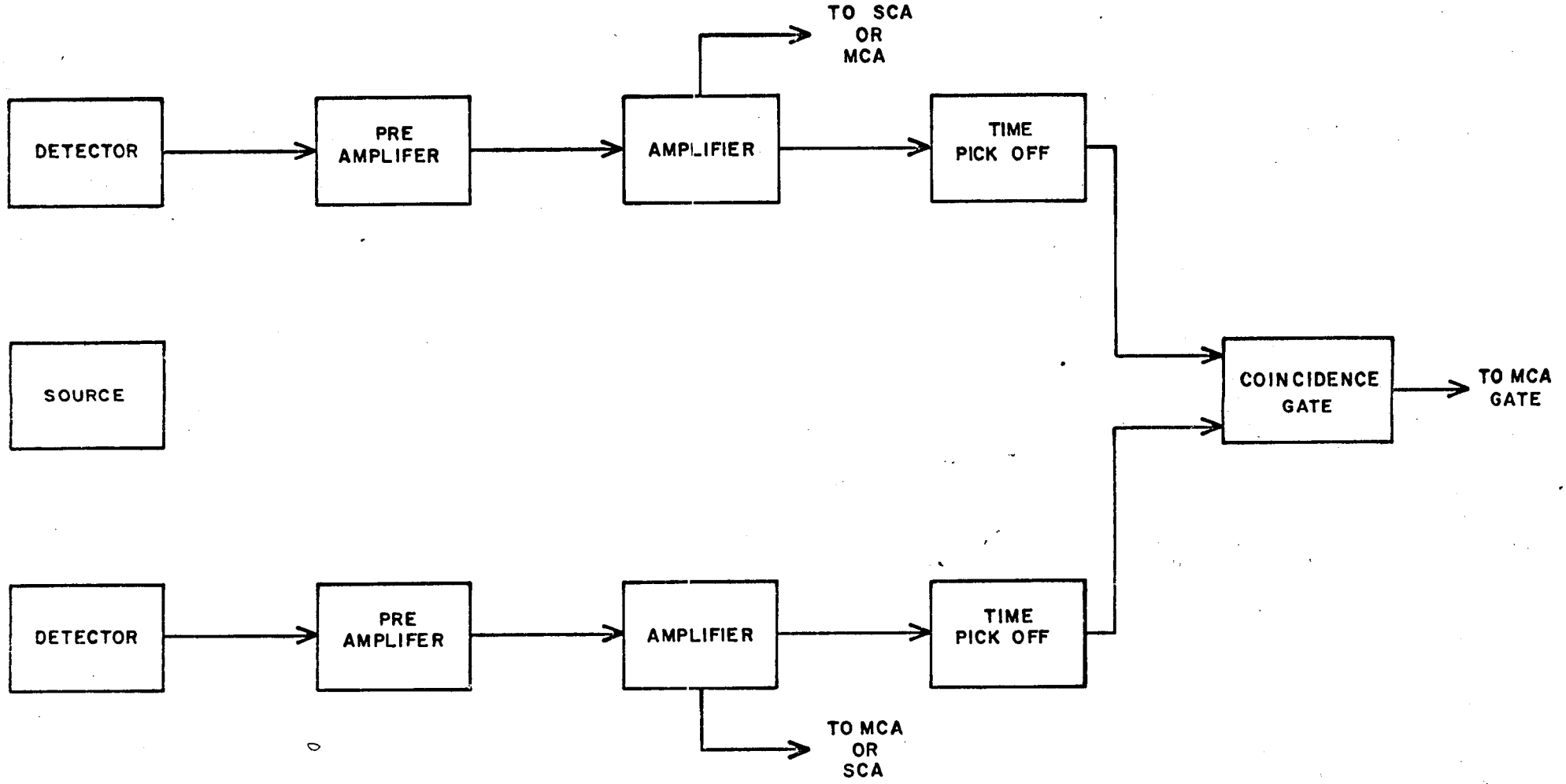


FIG. 14 TYPICAL COINCIDENCE SYSTEM

coincident. Differences in response of the detectors, differences in the pre-amplifiers and amplifiers may make the two pulses at the time pick-off module appear to arrive at different times. In order to eliminate this problem and to give the time pick-off module greater flexibility, a variable delay was built into the module.

This circuit allows 50 nanoseconds to 1.5 useconds delay prior to issuing a strobe pulse. By using the inspect point on the coincident gate module, the delays can now be established to compensate for detection system differences. This feature considerably simplifies properly setting up the coincidence system.

This module was designed with both leading edge and cross-over timing modes. Some controversy exists as to when to use which mode and exactly where in the circuit to place the time pick-off module. A number of variables may interact and the experimenter has to make a decision as to which parameter is most important to him.

Count rate is one factor. In general, the higher the count rate, the more advantageous is cross-over timing, hence, placing the time pick-off unit after the amplifiers.

The energy of interest is another factor.

If a wide band of energies is desired in the NaI systems, or very high resolution is desired in Ge(Li) systems, placing the time pick-off unit after the amplifier is again advantageous.

However, if energies of interest are restricted in NaI experiments or if timing accuracy is more important than resolution in Ge(Li) experiments, it appears that leading edge timing after the pre-amplifier and amplifier is, however, somewhat detrimental to energy resolution.

We have favored energy resolution in the design of the time pick-off module rather than time resolution. The time pick-off module has been designed to be used after an amplifier and to provide high resolution at the cost of time resolution.

Specifications on this unit are as follows:

Input: 0 - 10 volt initially positive, bipolar, linear signal, double RC differentiated or double delay line. Input impedance is approximately 1 kilohm.

Timing: Delay Range: Adjustable in the X1 position from 50 to 500 nanoseconds; in the X3 position, from 0.15 to 1.5 microseconds.

Threshold: Sensitivity Range: Variable from 0.5 to 9.6 volts.

Time walk: Less than 4 nanoseconds over full range.

Temperature Stability: Time walk as a function of temperature, including both time pick-off and delay circuits, is 0.7% of delay, or 0.1 nanoseconds per ^{o}C, whichever is greater.

Time Walk: For an input amplitude change of 10 volts to 1 volt, time walk is less than 4 nanoseconds. For an input amplitude change of 10 volts to 0.5 volt, time walk is less than 10 nanoseconds.

Strobe Output: For a resistive load of 100 ohms -- +6.5 volts rise time of 15 nanoseconds, fall time of 20 nanoseconds, duration of 300 nanoseconds at FWHM.

For a capacitive load of 100 Picofarads -- +8 volts, rise time of 12 nanoseconds, fall time of 200 nanoseconds, duration of 320 nanoseconds at FWHM.

Prompt Output (rear panel): +3.8 volts, rise time of 20 nanoseconds, fall time of 20 nanoseconds, pulse duration determined by the time between the leading edge and cross-over points of

the input pulse, occurs 40 nanoseconds before strobe output (with delay controls set at minimum). Output impedance, 50 ohms.

Work will continue in this area in order to 1) reduce the walk of the unit and 2) investigate further the adaptability of this unit to leading edge timing of signals from pre-amplifiers.

COINCIDENCE GATE

Of the many modules under development, this proved to be the most difficult to perfect. Work is continuing in this area but the results are somewhat disappointing. The primary cause for concern lies in the area of generating a single gate pulse for every coincident event. A simplified discussion of the problem encountered is as follows: When an input arrives at the fast coincidence gate from either Time Pickoff unit, an internal pulse of 2 t width is generated. If an input from the other Time Pickoff unit should arrive during this time, an output gate signal is generated. If the time requirements are not fulfilled, an output pulse cannot be originated. To date, accidental coincidence rates were determined to have been much too high and the cause of this has been traced to the following: Whenever an internal pulse has occurred, it is accompanied by a series of smaller amplitude pulses caused by ringing of the primary pulse. These ringing pulses double, triple or even quadruple the acceptable coincident time

period. This effect is further complicated by the provision for variable coincidence resolving times which does not provide a convenient means for establishing a fixed time window.

As work on this project has progressed, little attention was given to absolute values regarding laboratory type coincidence experiments. Many tests were performed using pulse generators which did not exhibit this phenomena due to the lack of random inputs. Before this report was prepared in final draft, more extensive random input tests were performed with rather critical analysis given to experimental results. At that time, the abnormally high accidental rates were detected and time has not permitted rectification of the problem.

The design of this module contains a number of features useful in setting up coincident experiments. Any input may be selected for coincidence, anti-coincidence, or disabled. In addition, singles, doubles, or triples in any combination may be selected.

Specifications on this system are as follows:

Inputs: Three front panel BNC connectors accept positive 3-10 volt pulses with a maximum rise time of 25 nanoseconds and a minimum input pulse width of 30 nanoseconds, Input impedance is

approximately 1 kilohm.

Logic Function Selection: Three toggle switches, one per input, select the logic function to be performed.

Coincidence Threshold: The acceptance level of the output logic can be selected as follows: In singles, any one input, or one or more in coincidence, provides an output; in doubles, any two coincident inputs; in triples, three coincident inputs.

Resolving time: The pulse width of the signals generated by each input, as applied to the output logic circuits, can be varied from 10 - 110 nanoseconds with a resultant 2t range of 20 - 220 nanoseconds.

When any one input is switched to anti-coincidence, its pulse width is extended from t to 2t, insuring optimum anti-coincidence operation.

Timing Inspect: The timing inspect point presents the sum of all three inputs for observation, allowing normalization of system delays by direct observation.

Gate Outputs: D.C. coupled outputs with the following levels:

+ Gate: "0" - 12 volts
"1" + 1 volt

- Gate: "0" + 1 volt
"1" - 12 volts

This unit requires further work and Nuclear Data is continuing efforts in this area.

CONCLUSION

The total work performed under this contract has been shown to be both extensive and economical. The Multimode System itself is more than adequate for the experimental program anticipated. It contains useful features from input to output which greatly enhance its flexibility. Its speed and resolution in analysis, minimum storage time, and versatility in display and readout contribute to the continued high performance the system has thus far demonstrated. This portion of the contract has proven to fulfill each detail of the requirements with the majority of the specifications exceeded.

The time of flight development work has, like the Multimode system, exceeded the early expectations of the designers. The high frequency oscillator, prescaler, double derandomizer, expanded delay, and channel width range have added significantly to the current state of the art. As the report clearly indicates work on this project was a complete success.

The results of the total coincidence system are somewhat disappointing in the light of the success achieved in the Multimode system and the time of flight. These results should be reviewed from a

more positive viewpoint, however, when serious consideration is given to the development of a preamplifier, amplifier, bias supply, and the upward trend in the time pick-off unit and the coincidence gate program. We have successfully completed work on the former Modules while work is continuing on the latter two.

To summarize some of the advances made over the period covered by the contract, an impressive list of user orientated advantages has been assembled:

(1) Duplication of power supplies has been eliminated.

(2) Duplication of preamplifiers has been eliminated.

(3) Special power supplies have been eliminated.

(4) A great reduction in size has been achieved.

(5) Bothersome delay lines have been eliminated.

(6) High quality-high performance amplifiers are now available at a great reduction in cost.

(7) Physical packaging in agreement with AEC/NASA standards.

(8) Integrated circuitry used extensively.

(9) Preamplifier power supplies have been eliminated.

(10) Interchangeability of components is assured through standard NIM modules.

This total project has contributed several significant advantages over systems previously available. Because of the additional effort made by Nuclear Data, Inc. to expand the special coincidence modules into a total spectroscopy system we feel we have contributed significantly in bringing that phase of the contract to a successful completion.

The authors wish to acknowledge the diligent efforts by Mr. William Jacobs in amplifier design, Mr. Mitchell Leifer and Mr. Frank Spokas in Time of Flight design.

Total time extended on this system was as follows:

High voltage supply	160 hours
Pre-amplifier	200 hours
Amplifier	320 hours
Single channel analyzer (Integral discriminator)	40 hours
Time pick-off/Delay Module	320 hours
Coincidence gate	360 hours
Time of Flight	480 hours

APPENDIX I

TIME OF FLIGHT MODULE

INSTRUCTION MANUAL

Interim Edition
September, 1967

NUCLEAR DATA, INC.
Post Office Box 451
Palatine, Illinois 60067

CONTENTS

INTRODUCTION

GENERAL

This NIM compatible Digital Time of Flight Module is a highly accurate and versatile unit that can be used with the Series 3300 or 2200 System Analyzer (as specified when ordered) to measure one-quarter microsecond minimum channel widths when performing operations such as encountered in neutron time of flight measurements. Pulse width analysis and single pulse analysis experiments may also be performed as selected by a front panel switch. A 32 MHz, crystal controlled oscillator minimizes channel time jitter and insures long term stability. A switch selectable, delay time control is included that incorporates no fixed internal delay and can be used to delay the start of analysis for up to 99,990 channels. A variable dead time, and memory capacity switch completes the complement of controls.

SPECIFICATIONS

Start Input

Pulse Requirements

Amplitude:	2 to 20 volts.
Polarity:	Positive.
Rise Time:	Noncritical; should be uniform.

Input Impedance — Approximately 2000 ohms.

Event Input

Pulse Requirements

Amplitude:	2 to 20 volts.
Polarity:	Positive.
Rise Time:	Noncritical; should be uniform.

Input Impedance — Approximately 2000 ohms.

Stop Input

Pulse Requirements

Amplitude:	2 to 20 volts.
Polarity:	Positive.
Rise Time:	Noncritical; should be uniform.

Input Impedance — Approximately 2000 ohms.

Input Signal Attenuation

None required as long as signal returns to less than one volt prior to completion of operation.

Clock Oscillator

32 MHz, crystal-controlled.

Channel Width (Time Duration)

0.25 to 128 microseconds switch selectable in binary increments.

Channel Time Jitter

$\pm$ 1/64 microsecond.

Delay Time

0 to 99,990 channels thumbwheel switch selectable in 10 channel increments.

Fixed Delay

No fixed delay is incorporated in this unit. Delay times are as selected.

Dead Time

8, 16 or 32 microseconds, switch selectable.

Memory Size

16 to 4,096. Channels switch selectable in binary increments. 8192 or 16,384 sizes optional.

Power Requirements

+12 volts D.C. at 1 ampere.

-12 volts D.C. at 250 milliamperes.

Size

8.71" high x 5.36" wide x 9.7" deep (equivalent to four standard AEC single width modules).

PREPARATION FOR USE

INTERCONNECTIONS

SERIES 3300 SYSTEM

1. Insert the Time of Flight Module into any standard AEC bin with a power supply.

2. On the Series 3300 System remove the cable between the DATA ACQUISITION receptacle on the Data Handling Section and the PROGRAM INPUT receptacle on the Data Acquisition Section and connect it from the DATA ACQUISITION receptacle to the TIME OF FLIGHT - 50 receptacle on this module.

SERIES 2200 SYSTEM

1. Insert the Time of Flight Module into any standard AEC bin with a power supply.

2. Remove the ADC pigtail connector (on the Master Control Module) from the Series 2200 ADC and connect it to the TIME OF FLIGHT - 50 receptacle on this module.

CONTROL FUNCTIONS

CHANNEL WIDTH (MICROSECONDS)

This control establishes the time duration, during which a given event will be accepted for storage in a given channel.

CHANNEL DELAY

This thumbwheel switch selects the number of channels for which the unit will not accept any events and the program counter will remain at the reset state. This control enables the user to gain better resolution of data that normally appears at the end of the time of flight measurement.

DEAD TIME (MICROSECONDS)

This three position switch selects the time for which the unit, after accepting an event for processing, will not accept another. The time selected should be that minimum time which is greater than the memory cycle time. The DEAD TIME Control corrects for the time required to complete a memory cycle so that multiple events may be processed during a single sweep cycle.

MEMORY SIZE

This switch selects the memory size that is required or available.

MODE

This three position switch selects the operating mode of the Time of Flight Module.

MPA (Multiple Pulse Analysis)

This position permits multiple pulse analysis during a single cycle.

PWA (Pulse Width Analysis)

This position permits pulse width analysis, i.e., channel number is proportional to the incoming pulse width.

SPA (Single Pulse Analysis)

This position permits single pulse analysis per cycle. After event storage, the Time of Flight Module is reset and awaits another start signal.

OPERATION

The following instructions describe the normal method of set-up of this Time of Flight Module. In all cases, specific control settings depend upon experiment requirements. These instructions assume that all ancillary equipment is interconnected and operating properly and all power is on. All modes of operation are set up in the same manner. The procedure is as follows:

1. On the MEMORY SIZE Switch, select the number corresponding to the number of channels being used.

2. Select the desired channel width using the CHANNEL WIDTH Switch.

3. Using the CHANNEL DELAY Thumbwheel, select the amount of channel delay desired.

4. Select the dead time required using the DEAD TIME Switch. When this unit is used with a Series 2200 System in Live/Static display or a Series 3300 System with the display off, the memory cycle time is 6 microseconds. The DEAD TIME Switch is then normally set at position 8.

5. Select the mode of operation desired, using the MODE Switch.

6. Supply the proper signals to the START and EVENT BNC connectors on the front panel. The signals required are described in the SPECIFICATION Section of this manual. The STOP input is used only to externally stop and reset the unit. It is normally not used.

NOTE

When in the PWA mode, the pulse to be measured should be connected to the START BNC. The STOP and EVENT BNC's are not used in this mode.

APPENDIX II

ND-532ARC AMPLIFIER RC

INSTRUCTION MANUAL

First Edition
September, 1967

NUCLEAR DATA, INC.
Post Office Box 451
Palatine, Illinois 60067

CONTENTS

INTRODUCTION

GENERAL DESCRIPTION

The ND-532ARC Module is a linear amplifier with RC pulse shaping designed for nuclear pulse spectroscopy. When used with its companion, ND-533 Preamplifier Module, the ND-532ARC provides the necessary resolution and gain for use with Mössbauer systems, proportional detectors or low energy scintillation detectors.

> Note: When the ND-532ARC Module is used with a preamplifier other than its companion, ND-533 Preamplifier, the 470 ohm resister at the input must be disconnected. This resistor supplies +24 volts D.C. operating power to the ND-533 Preamplifier through the AMP IN BNC.

RC pulse shaping is provided by two passive differentiators and two active integrators. The first differentiator is pole-zero compensated to cancel under shoot effects. The RC shaping time constants can be changed by replacing four capacitors. These capacitors are equipped with pin jacks for easy insertion or removal. A switch, mounted on the printed circuit board, provides for selection of either a positive or negative output pulse. Maximum gain with double differentiation and integration is 800 and with single differentiation and double integration, 1600. Gain is adjusted by two front panel controls: a five position switch for coarse gain adjustment with a 16:1 range in 2:1 steps and a single turn potentiometer for fine gain adjustment with a 2:1 continuous range between coarse steps. Noise, referred to the input at maximum gain and with double differentiation and integration, is 5.0 microvolts and with single differentiation and double integration, 4.0 microvolts.

In addition to the normal amplifier output, the ND-532ARC provides a simultaneous standardized current pulse output at the rear panel M/R AMP BNC. This output is appropriate for use in a multiple input mixer/router system for multichannel analyzers, or can be applied in a variety of other spectrometer and signal gating configurations.

SPECIFICATIONS

AMPLIFIER INPUT

Two BNC's (one front, one rear) accept positive, low level signals from a preamplifier. Input impedance is approximately 1000 ohms.

GAIN STABILITY

0.03% per degree centigrade.

GAIN CONTROLS

Coarse -- 50 to 800 in binary steps.

Fine -- 0.5 to 1 continuous range between coarse steps.

PULSE SHAPING

Two passive differentiators and two active integrators. First differentiator is pole-zero compensated to cancel undershoot effects. The RC shaping time constants can be changed by replacing four capacitors. These capacitors are equipped with pin jacks for easy insertion or removal.

NOISE

4.0 microvolts, referred to the input at maximum gain and with single differentiation and double integration or 5.0 microvolts with double differentiation and integration.

OVERLOAD

With single differentiation and double integration -- Recovers from 500 x overload in 3 non-overloaded pulse widths.

CHARACTERISTIC RISE TIME

With single differentiation -- 300 nanoseconds.

AMPLIFIER OUTPUT

Signal Characteristics -- Front panel BNC provides positive or negative,monopolar or bipolar voltage pulses (internal switch selectable).

Impedance -- 100 ohms.

Saturation Levels -- +12 volts and -12 volts.

Integral Linearity -- 0.1% from 0 to $\pm$10 volts.

M/R AMPLIFIER OUTPUT

Signal Characteristics -- Rear Panel BNC provides positive or negative,monopolar or bipolar current pulses (internal switch selectable).

Impedance -- 100K ohms.

Saturation Levels -- +0.12 milliampere and -0.12 milliampere.

Integral Linearity -- 0.1% from 0 to $\pm$0. 10 milliampere.

POWER REQUIREMENTS

+24 volts D.C. at 25 milliamperes.

-24 volts D.C. at 10 milliamperes.

+12 volts D.C. at 15 milliamperes.

-12 volts D.C. at 25 milliamperes.

SIZE

8.71" high x 1.34" wide x 9.7" deep (standard AEC single width module).

WEIGHT

Approximately 1.5 pounds.

CONTROLS AND CONNECTORS

FRONT PANEL

COARSE GAIN CONTROL

Provides adjustment of the overall amplifier gain from 50 to 800 in binary steps. The overall amplifier gain with double differentiation and integration corresponds to the setting of the COARSE GAIN control.

FINE GAIN CONTROL

Provides an overlapping adjustment of the overall amplifier gain with a .5 to 1 continuous range for each setting of the COARSE GAIN control.

AMP IN (Amplifier Input) BNC

Accepts positive, low-level signals from an external preamplifier. Also provides +24 volts D.C. operating power to the ND-533 Preamplifier.

> Note: When a preamplifier other than the ND-533 is used, the 470 ohm resistor at the input must be disconnected as this resistor supplies the +24 volts D.C. operating power to the ND-533 Preamplifier.

AMP OUT (Amplifier Output) BNC

Provides positive or negative, monopolar or bipolar voltage pulses for use with an external analog to digital converter, single channel analyzer or crossover timing unit.

> Note: Positive or negative output is selected by the internal INV/NON INV switch.

REAR PANEL

AMP IN (Amplifier Input) BNC

Accepts positive low-level signals from an external preamplifier. This BNC is connected directly to the front panel AMP IN BNC.

M/R AMP (Mixer/Rejector Amplifier Output) BNC

Provides positive or negative, monopolar or bipolar current pulses for use with an external multiple input mixer/router system or a variety of other spectrometer and signal gating configurations.

Note: Positive or negative output is selected by the internal INV/NON INV switch. This switch must be in the NON INV position when output is used with a multiple input mixer/router system as this system will only accept positive current pulse inputs.

BLOCK DIAGRAM DESCRIPTION

Positive low-level signals at the AMP IN BNC are coupled through the FINE GAIN control to an operational amplifier having a variable gain of two to four. The gain of the operational amplifier is determined by the ratio established by the setting of the FINE GAIN control and the feedback resistor (FB1). The output of the operational amplifier is applied to the first differentiator circuit which is pole-zero compensated to cancel the undershoot effect of pulse differentiation. Signals from the first differentiator circuit enter the first operational integrator which has a fixed gain of eight. The output of the first operational integrator is coupled through the COARSE GAIN switch to the second operational integrator which has a variable gain of 0.5 to 8. The gain of the second operational integrator is determined by the ratio established by the setting of the COARSE GAIN switch and the feedback resistor (FB3). The output of the second operational integrator is coupled through the second differentiator circuit and the INV/NON INV switch to another operational amplifier having a fixed gain of six. The output of this operational amplifier is applied to two output BNC's: AMP OUT which provides positive voltage pulses when the INV/NON INV switch is in the NON INV position or negative voltage pulses when the INV/NON INV switch is in the INV position and M/R AMP which provides positive or negative current pulses again depending upon the positioning of the INV/NON INV switch.

Note: If the M/R AMP output is applied to the input of the ND-521 M/R Mixer/Rejector Module, the INV/NON INV switch must be in the NON INV position as the ND-530 M/R will only accept positive current pulses.

The second differentiator circuit can be removed by replacing its capacitor with the largest valued capacitor supplied. However, without the second differentiation, the maximum amplifier gain is increased by a factor of two from 800 to 1600. The RC shaping time constants can be varied by changing the values of the four capacitors in the two differentiator and integrator circuits. These capacitors are equipped with pin jacks for easy insertion or removal.

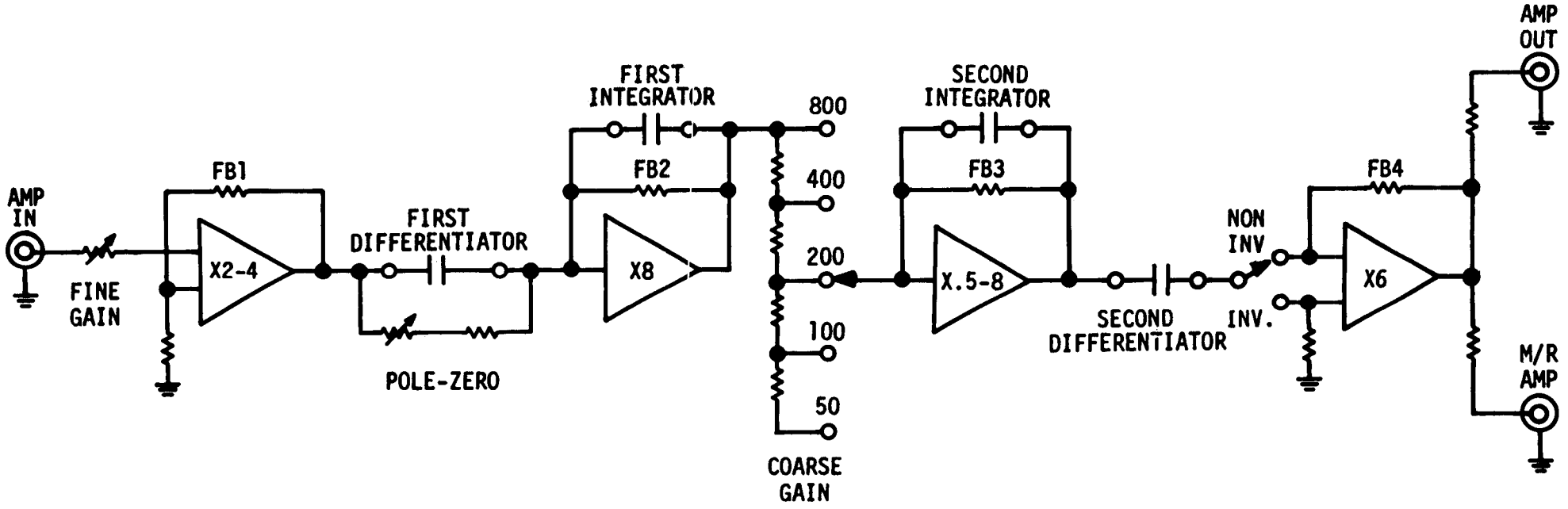
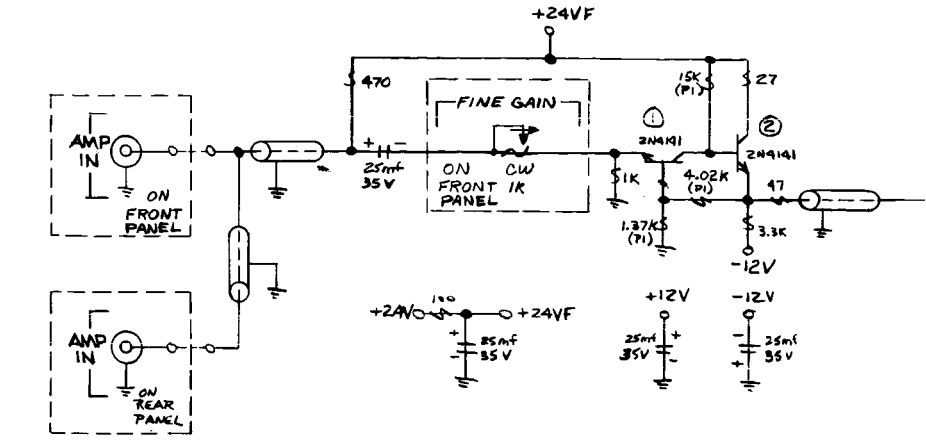
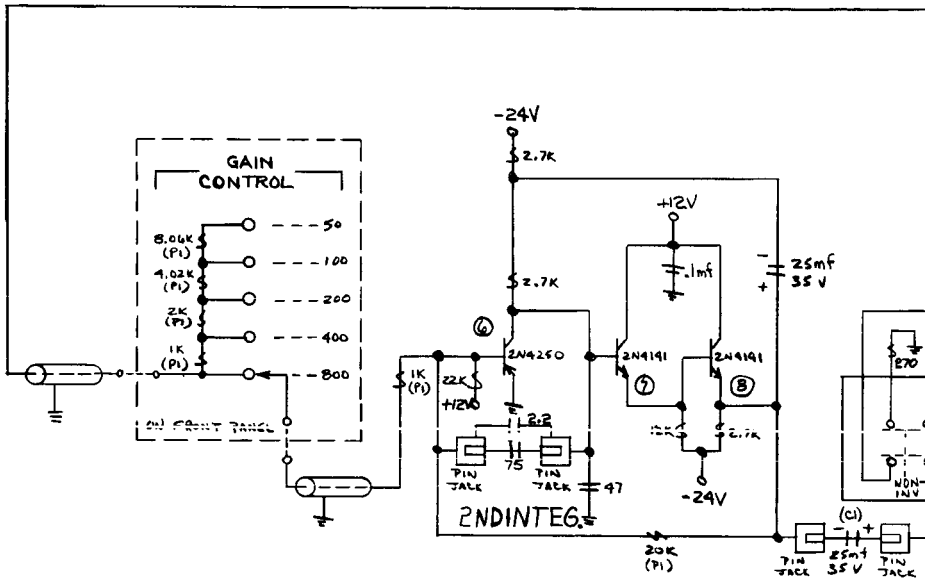
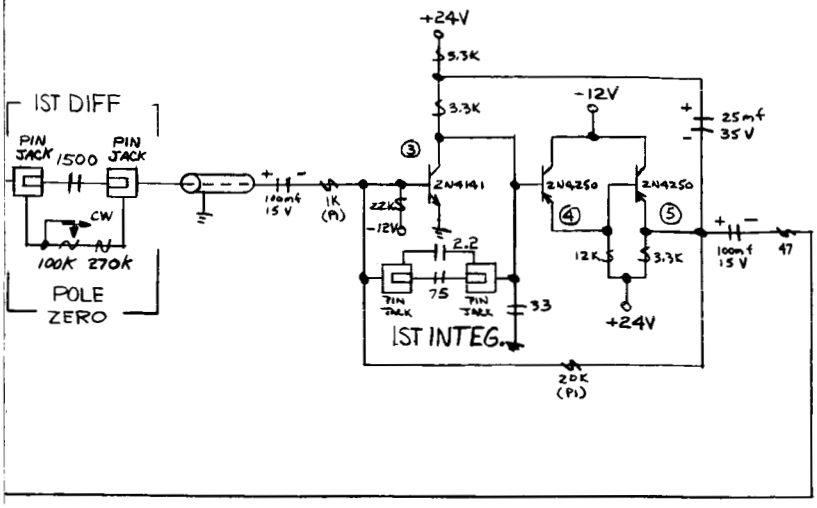


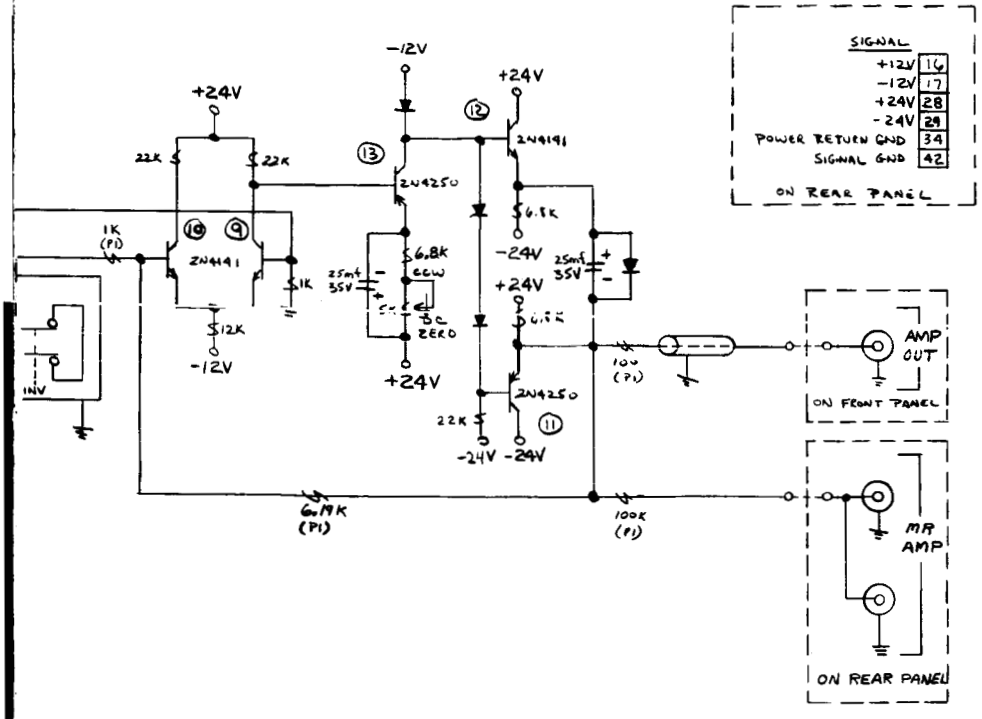
FIGURE 2

BLOCK DIAGRAM OF ND-532 ARC AMPLIFIER RC


+24VF
470
FINE GAIN
ON FRONT PANEL
CW 1K
25mf 35V
15K (P1)
27
2N4141
2N4141
1K
4.02K (P1)
47
1.37K (P1)
3.3K
-12V
AMP IN
ON FRONT PANEL
AMP IN
ON REAR PANEL
+24V
100
+24VF
85mf 35V
+12V
25mf 35V
-12V
25mf 35V


GAIN CONTROL
8.06K (P1)
4.02K (P1)
2K (P1)
1K (P1)
50
100
200
400
800
ON FRONT PANEL
-24V
2.7K
2.7K
+12V
.1mf
25mf 35V
2N4250
2N4141
2N4141
1K (P1)
22K
+12V
2.2
PIN JACK
75
PIN JACK
47
2NDINTEG.
2.7K
-24V
20K (P1)
(C1)
PIN JACK
25mf 35V
PIN JACK
270
NON-INV
2ND DIFF.





SIGNAL	
+12V	16
-12V	17
+24V	28
-24V	29
POWER RETURN GND	34
SIGNAL GND	42

ON REAR PANEL

NOTES:
1 – ALL DIODES ARE G064 OR EQUIVALENT, EXCEPT AS NOTED.
2 – ALL RESISTORS ARE 1/4W, 5%, EXCEPT AS NOTED.
3 – ALL CAPACITORS ARE pf, EXCEPT AS NOTED.
4 – SYMBOLS:
- SELENIUM
- SILICON, IN914B
- GERMANIUM
- ZENER
- TUNNEL
- POWER RETURN GND, SIGNAL GND (SEE NOTE 6)

5- (P1) ALL PRECISION RESISTORS ARE 1/8 W ±1% METAL FILM.
6- THESE TWO GNDS JUMPER TOGETHER TO A COMMON GND
7- (C1) CHANGE TO 150pf FOR SECOND CLIP.

USED ON

ASSEMBLY NO.

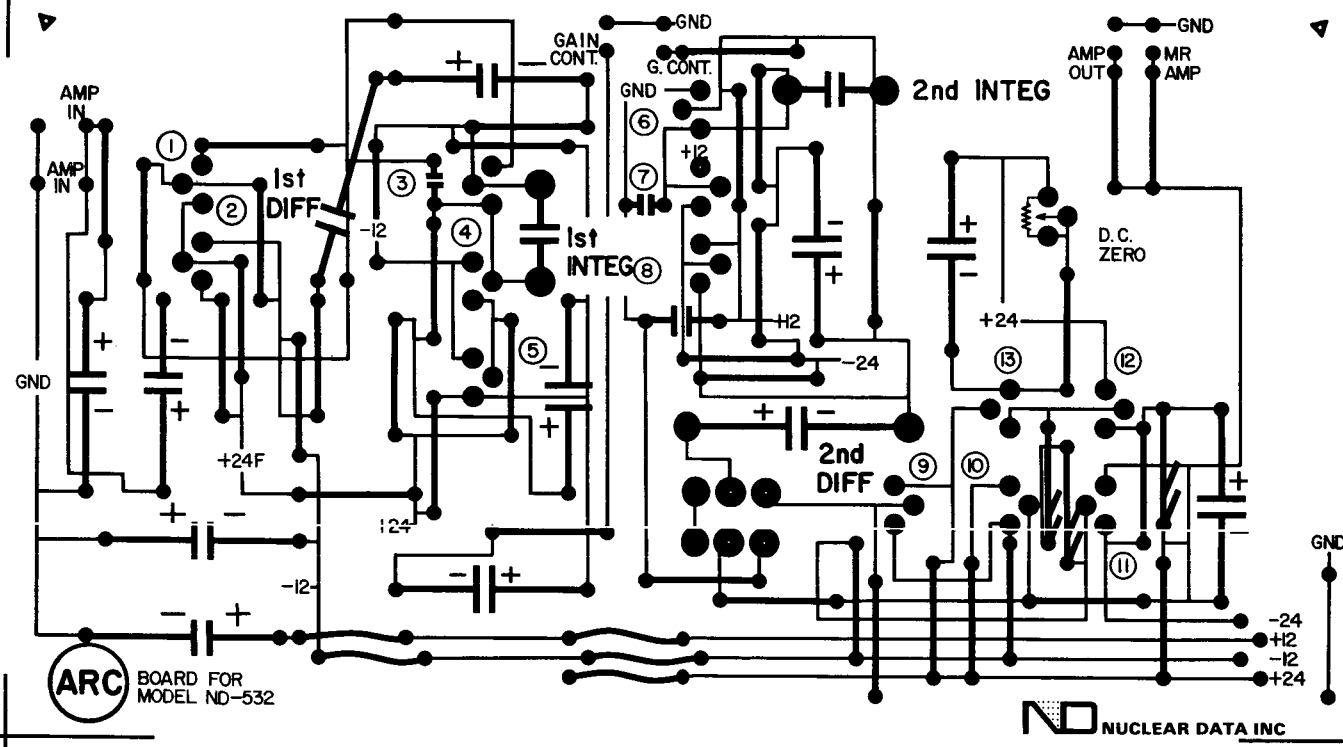
ND-532 / 80-0155

NUCLEAR DATA INC
POST OFFICE BOX 451, PALATINE, ILLINOIS 60067

DIAGRAM, SCHEMATIC
"ARC" BOARD

DRAWN BY: KWW	CHECKED BY:	S70-0163-00D
DATE DRAWN: 6-14-67	APPROVED BY:	

FORM NDS-103


AMP IN
AMP IN
GND
1st DIFF
+24F
-12
GAIN CONT.
1st INTEG
-24
GND
G. CONT.
GND
+12
2nd INTEG
+12
-24
2nd DIFF
GND
AMP OUT
MR AMP
D.C. ZERO
+24
GND
-24
+12
-12
+24
ARC
BOARD FOR MODEL ND-532
ND NUCLEAR DATA INC

APPENDIX III

APPENDIX III

REFERENCES

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APPENDIX IV

TECHNICAL SPECIFICATIONS

NUCLEAR DATA INC.
100 West Golf Road
Palatine, Illinois 60067
Phone A.C. 312 • 529-4600

ND-526 BIAS POWER SUPPLY

The ND-526 BPS is an ultra-stable bias power supply designed specifically for operation of solid state detectors. It is housed in a standard AEC double width module and operates with standard bin power supply voltages. Detector operating potentials of up to 1400 volts D.C. are obtained by conversion of relatively low D.C. voltage from the bin power supply to 20KHz A.C. voltage by means of an electronic "chopper", the output of which is coupled to a voltage multiplier. The output of the voltage multiplier is shunted by series-connected miniature gaseous reference elements to provide an extremely stable source voltage for constant current loads.

A ten-turn calibrated front panel control provides adjustment of output voltage over a range of 0 to 1400 volts. The maximum rate of change for output voltage adjustment is limited by a 0.5 second time constant. This protects both the detector and the preamplifier input from damage which may result from sudden adjustment-induced voltage changes.

An A.C. RMS voltmeter is also included as a noise indicator for determining optimum detector voltage settings. It can also be used to determine which integrating and differentiating time constants of a linear pulse amplifier, such as the ND-524 LARC, provide optimum signal-to-noise ratio.

BIAS SUPPLY

Output Voltage:
0-1400 volts D.C.

Output Polarity:
Positive (negative output obtained by relocating three internal jumpers).

Output Impedance:
100 K ohms.

Output Noise:
0.4 millivolts rms, from 2Hz to 4MHz.

Bias Stability:
Temperature - 0.007%/°C.
A.C. Line Voltage - 0.0005%/10% change in line voltage.

Bias Control:
Ten turn potentiometer calibrated at 140 volts per turn.

Output Time Constant:
A 0.5 second time constant limits the maximum rate of change of output voltage.

RMS NOISE INDICATOR

Input Impedance:
1,000 ohms (D.C. voltage not to exceed ±15 volts).

Indication:
Front panel meter.

Accuracy:
10%

Sensitivity:
10 mv rms full scale, 100 mv rms full scale, and 1 volt rms full scale, by means of a three position switch.

Band Width:
20 Hz to 2MHz.

GENERAL

Connectors:
Bias Output - UG 931/U (MHV).
RMS Input - UG 290/U (BNC).

Power Requirements:
+12 volts at 150 ma.
−12 volts at 150 ma.
−24 volts at 5 ma.

Size:
8.71" high x 2.68" wide x 9.7" deep (Standard AEC Double Width).

Weight:
4 pounds.

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TECHNICAL SPECIFICATIONS

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100 West Golf Road
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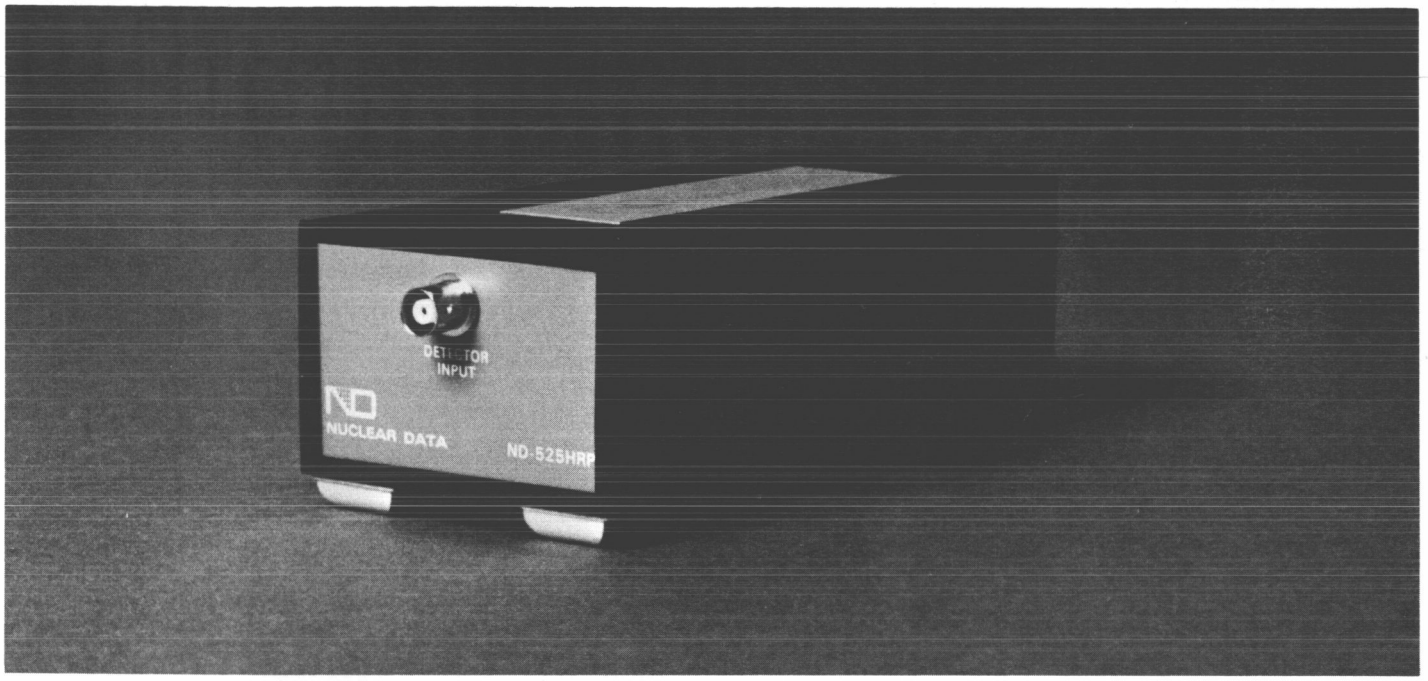


ND-525HRP HIGH RESOLUTION PREAMPLIFIER

Extremely high resolution capabilities inherent in cooled Ge(Li) detectors are realized only to the extent of limits imposed by associated electronics, especially the necessary charge-sensitive preamplifier. The ND-525HRP is a high resolution charge sensitive preamplifier which provides the high degree of performance consistent with state-of-the-art technique.

Two selected field effect transistors (FET's), connected in parallel, are used in the input circuitry to provide excellent low noise performance. The ND-525 can also be supplied, at additional cost, with four parallel-connected FET's to provide greater low noise performance with detector capacitance exceeding 250 picofarads. A decay time constant of 55 microseconds, which is pole-zero compensated to minimize pulse undershoot effects, is provided by the charge-sensitive circuit group. The voltage output from the charge-sensitive group is amplified by a factor of four voltage sensitive group. A single component in this group can be changed to yield any amplification factor from 2 to 16, if desired.

Operating voltages can be obtained from the companion ND-524LARC linear pulse amplifier preamplifier power output, or from a standard AEC bin power supply.

CHARGE SENSITIVE GROUP

Conversion Gain:

54 mv/Mev (Ge).

Input Polarity:

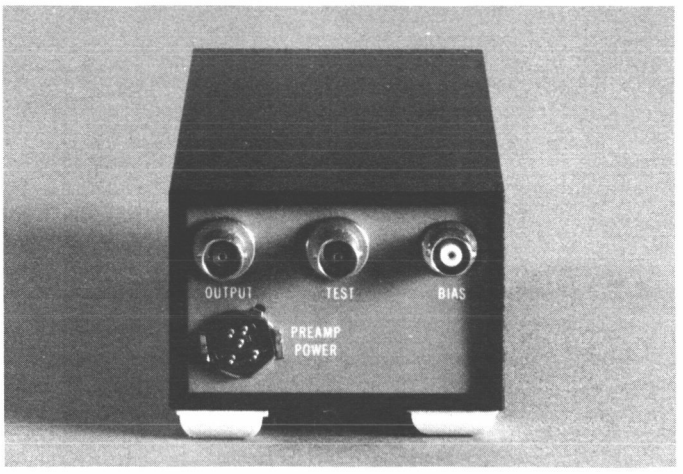
Either.

Noise (Ge):

Less than 2 Kev at 10 pf, external capacitance.

Noise Slope:

Less than .04 Kev/pf, external capacitance.



ND-525HRP High Resolution Preamplifier rear panel showing Output, Test, Bias, and Preamp Power connectors.

Input Capacitance:
Hot — 20,000 pf (minimum).
Cold — 20 pf.

Rise Time:
50×10^{-9} sec at 0 pf, external capacitance.
80×10^{-9} sec at 100 pf, external capacitance.
150×10^{-9} sec at 1000 pf, external capacitance.

Sensitivity Loss as a Function of Detector Capacitance:
2% at 500 pf.
5% at 1000 pf.

Decay Time Constant:
55 microseconds ±2%.

VOLTAGE SENSITIVE GROUP

Voltage Gain:
x4; standard (single) component change gives any value from 2 to 16.

Output Impedance:
100 ohms ±1% D.C. coupled.

Output Voltage:
±10 volts linear; ±12 volts saturated into open circuit.
±5 volts linear; ±6 volts saturated into 100 ohms.

GENERAL

Output Polarity:
Inversion of input.

Integral Linearity:
Less than 0.1% for 0-10 volt output (unterminated).

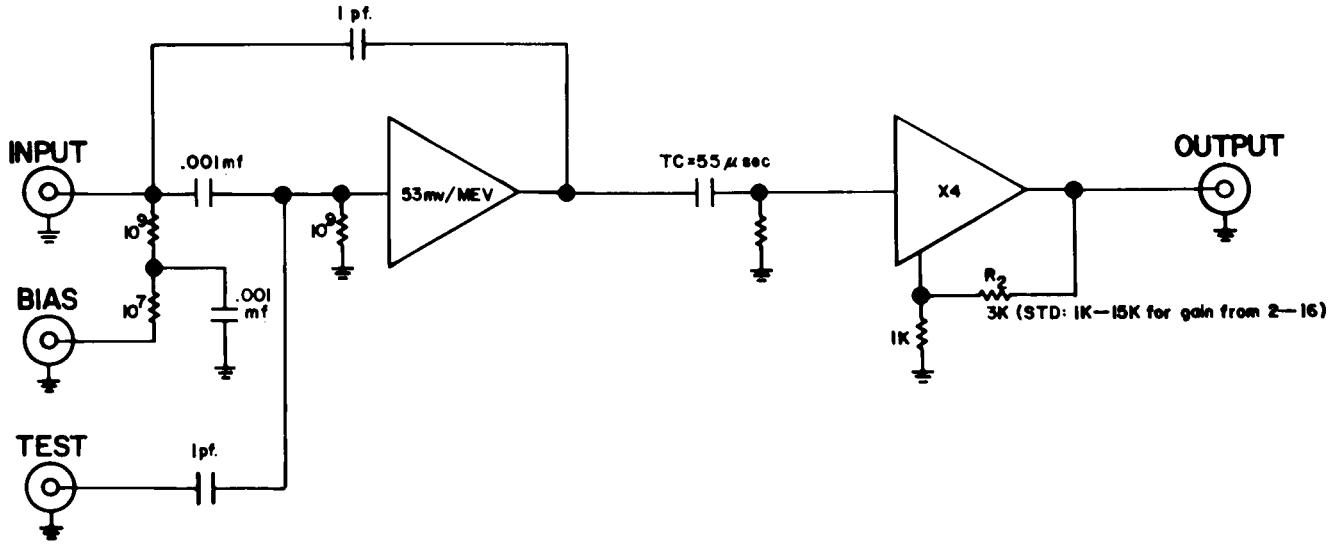
Temperature Stability:
0.005%/°C.

Connectors:
Input - UG 931/U (MHV).
Detector Bias - UG 931/U (MHV); Up to 2000 volts bias may be applied.
Test - UG 290/U (BNC); An internal 1.0 pf ±.25 pf test capacitor is provided.
Output - UG 290/U (BNC).
Power - Amphenol 126-218.

Power Requirements:
+24 volts at 20 ma.
−24 volts at 20 ma.
+12 volts at 30 ma.

Size:
7-1/8" long x 3" wide x 2" high, exclusive of connectors and mounting feet.

Weight:
1.25 pounds.



BLOCK DIAGRAM OF ND—525 HRP

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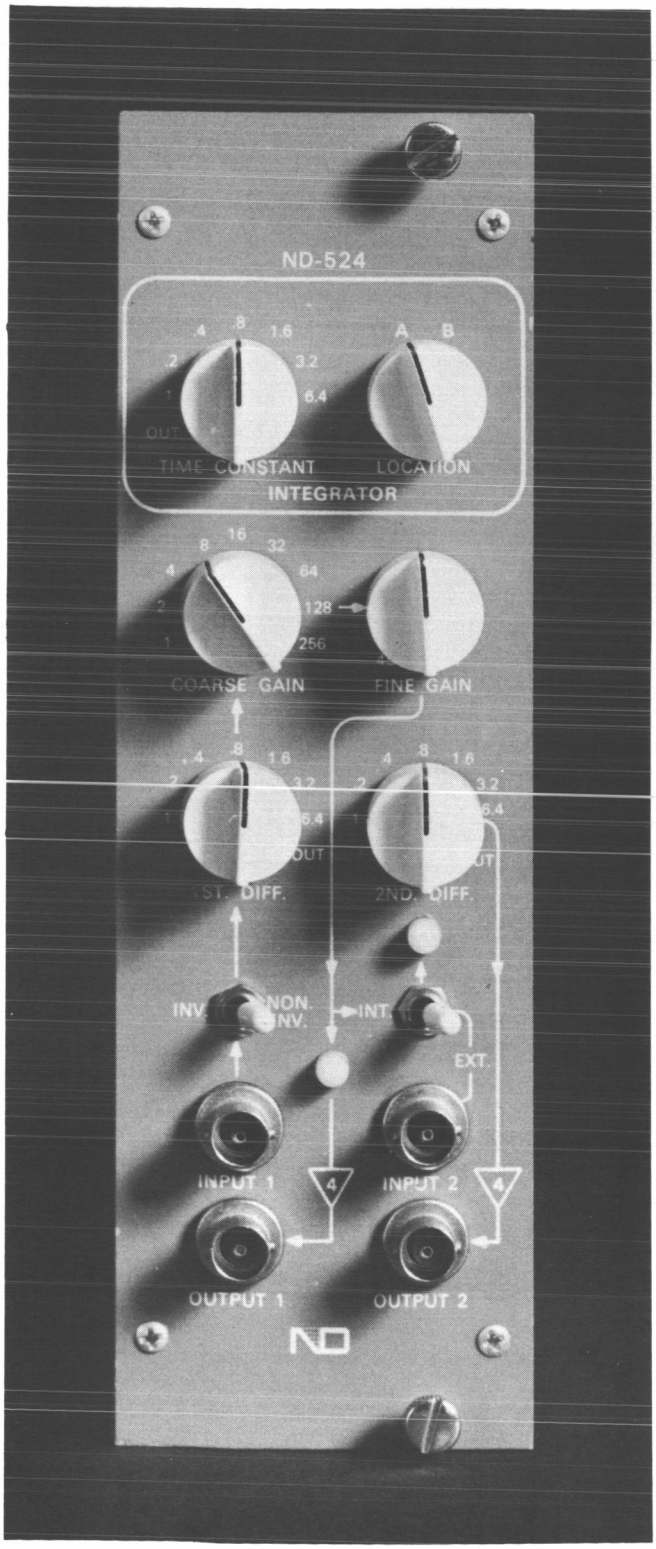


ND-524 LARC LINEAR AMPLIFIER

The ND-524 LARC is a high performance linear pulse amplifier specifically designed for high resolution nuclear pulse spectroscopy. It is especially well suited for application with solid state detectors where low noise, optimum pulse shaping, and excellent overload recovery are required. When used with an appropriate low noise preamplifier, the ND-524 provides the linear amplification and pulse shaping necessary for high resolution multichannel analysis with analog-to-digital converters such as used in the Nuclear Data Series 2200 and 3300 systems. R.C. pulse shaping is provided by two independently adjustable differentiators, and an independently adjustable double integrator. The first differentiator is pole-zero compensated to minimize undershoot effects, and the integrator, which utilizes both passive and active elements, provides a more nearly gaussian response to improve signal-to-noise ratio.

Sectionalized construction facilitates insertion of discriminators, linear gates, timing pick-offs or other similar instrumentation. The input section, which has a maximum gain of 256, contains the first differentiator and the amplifier gain controls. Two independent output sections each have a fixed gain of four. The second differentiator is located within one of the two output sections, and the integrator location can be switch selected to precede either output section. If desired, the two output sections can be cascaded to provide a maximum amplifier gain of 4096. The ND-524 LARC is packaged in a standard AEC double width module, so that up to six units may be housed in a single AEC bin. All inputs and outputs appear on both the front and rear panels to simplify interconnection. A D. C. power output for operation of the companion ND-525 HRP high resolution preamplifier is also provided.

SPECIFICATIONS

Input 1:

Two BNC connectors (one front, one rear). Input accepts positive or negative low level signals (D. C. level not to exceed 15 volts). Input impedance; 1000 ohms ±1% for positive or negative signal.

Input 2:

Two BNC connectors (one front, one rear). Input accepts positive or negative 0-10 volt signals (D. C. level not to exceed 15 volts). This input is coupled to a final amplification section which has a fixed gain of X4. Input impedance; 1000 ohms ±1% for positive or negative signals.

Polarity:

For signals applied to INPUT 1; output is the same polarity as input (non-inverted), or output is opposite polarity as input (inverted).

Gain Capability:

Gain of 1024 for output pulses with one integration and two differentiations of equal time constant. Gain is continuously adjustable over a range of 4-1024. The two output sections can be cascaded to provide a gain of 4096.

Gain Stability:

Less than 0.005% per degree C and 0.01% per 10% change in line voltage.

Pulse Shaping:

Double integration and two differentiations, with time constants independently variable in 2:1 steps over a range from 0.1 to 6.4 microseconds. In addition, it is possible to disable each differentiation and the double integration individually, so that with all three disabled, the amplifier has an output rise time of 80 nanoseconds and fall time of 10 milliseconds, for a step function input.

Noise:

Less than 8 microvolts, referred to input, for a singly differentiated — double* integrated pulse with 1.6 microsecond time constant at all gains from 64-1024.

Integral linearity:

Less than 0.1% over the output range of 0.1 to 10 volts open circuited, or 0.05 to 5 volts into 100 ohms, either polarity.

Differential Linearity:

Less than 0.4% over the output range of 0.1 to 10 volts open circuited, or 0.05 to 5 volts into 100 ohms, either polarity.

Crossover Walk:

Not more than ±2 manoseconds for doubly differentiated pulses over full linear output range and not more than ±1 manosecond over full gain control range.

Overload Performance:

Double differentiated — double* integrated: Recovery to 1% of rated output in 2 non-overloaded pulse widths for an overload of 500 times for all time constants.

Single differentiated — double* integrated: An overload of 100 times produces an undershoot not greater than 5% of full scale for time constants up to 1.6 microseconds.

*Double Integrator: consists of two ganged low pass filters with identical response, followed by a non-inverting amplifier with a gain which compensates for filter attenuation.

Maximum Count Rate:

No limitation on count rate.

Pole Zero Compensated:

The first differentiator is compensated for undershoot effects at all selected time constants. Optimum input decay time for pole zero compensation is 55 microseconds ±5%.

Output 1:

Two BNC connectors (one front, one rear) provide a 10 volt, open circuit, output signal. Impedance is 100 ohms ±1%, short circuit protected. The two outputs have a common source impedance of 0.2 ohms.

Output 2:

Two BNC connectors (one front, one rear) provide a 10 volt, open circuit, output signal. Impedance is 100 ohms ±1%, short circuit protected. The two outputs have a common source impedance of 0.2 ohms.

Connectors:

All signal connectors BNC, duplicated on front and rear panels. Preamplifier D. C. power connector Amphenol, type 126-218, located on rear panel.

Power Requirements:

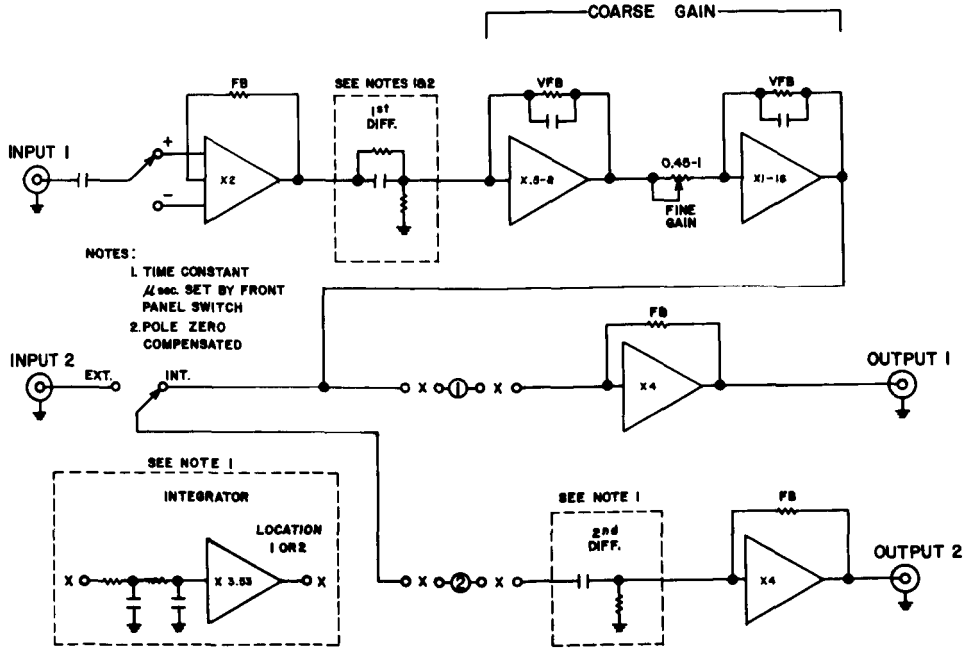
+24 volts at 110 ma.
−24 volts at 110 ma.
+12 volts at 60 ma.

Size:

8.71" high x 2.68" wide x 9.7" deep (Standard AEC Double Width).

Weight:

Approximately 2 pounds and 8 ounces.



BLOCK DIAGRAM OF ND-524 LARC

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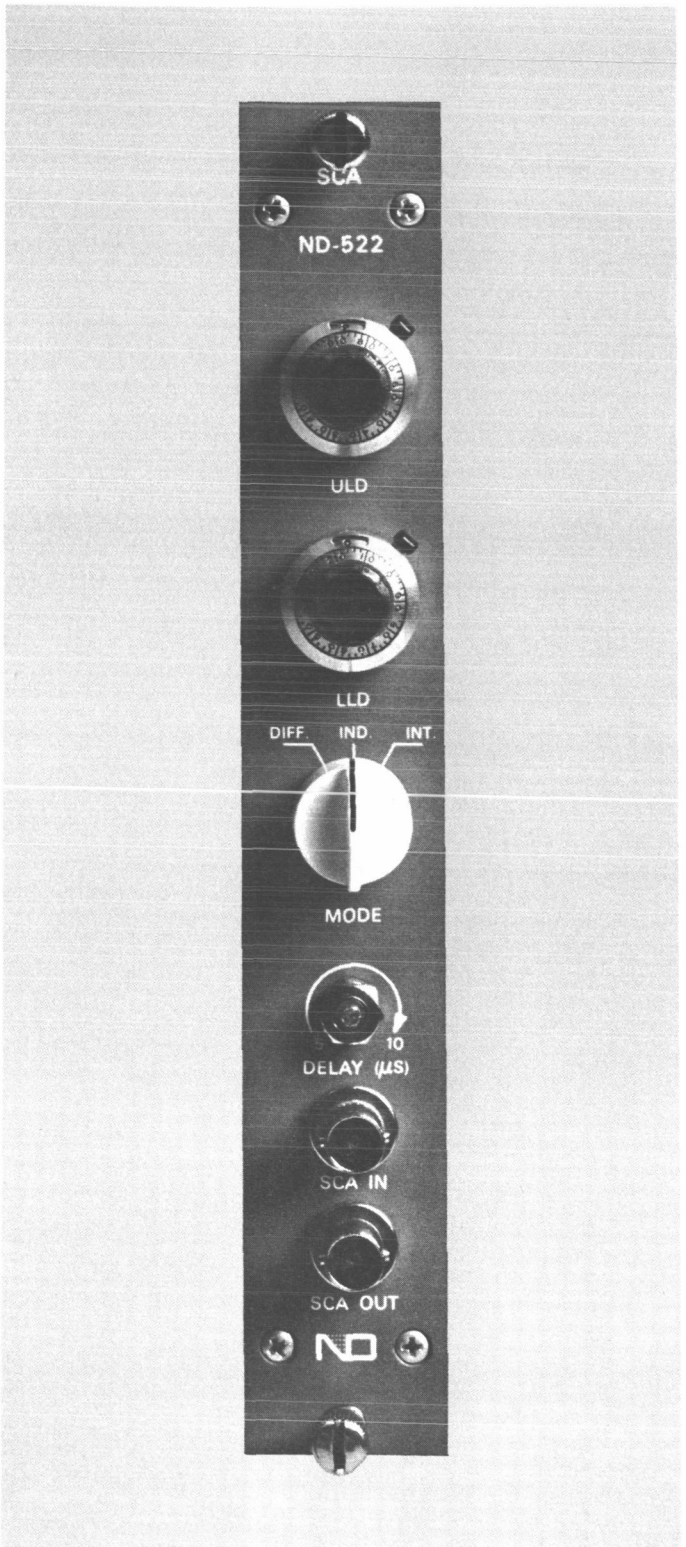

ND-522 SCA SINGLE CHANNEL ANALYZER

The ND-522 Single Channel Analyzer module generates an output whenever a linear input signal satisfies the pulse height requirements imposed by the LOWER LEVEL and UPPER LEVEL discriminators. These discriminators may be operated in one of three modes, as determined by the front panel Mode switch, and their discrimination level is adjusted by two ten-turn front panel controls. Provisions for timing the occurence of an output signal by either internally generated strobe pulses, externally applied strobe pulses, or an internally generated reset with externally applied strobe pulses for coincidence timing, are provided by means of a Strobe mode switch. The strobing capabilities provided by this analyzer enable it to be used in a wide variety of coincidence or anti-coincidence gating systems.

A unique feature of the ND-522 SCA is the variable output delay timing obtained with internal strobe operation. The front panel Delay control allows the operator to delay the internal strobe pulse from 0.5 to 10 microseconds with respect to the onset of leading edge of discriminator triggering. In coincidence gating systems, where linear signals (up to 10 microseconds rise and fall time constants) must be handled, no additional linear signal delay circuits are required since input pulse width imposes no restrictions on discriminator triggering.

Single Channel Analyzer Input

Signal Requirements Front panel BNC accepts positive monopolar or initially positive bi-polar amplifier outputs to ±15 volts. Input rise times .05 to 10 microseconds with less than 0.1% sensitivity change.

Input Impedance 1,000 ohms, A.C. coupled, long time constant. D.C. coupling is recommended for bipolar pulse and pulses greater than +12 volts.

Mode Switch

Integral Upper Level Discriminator (delta E) is disabled. The only criteria for pulse acceptance being an amplitude exceeding the Lower Level Discriminator threshold (E) setting.

Independent Both E and delta E discriminators operate separately. Pulse acceptance occurs when the pulse amplitude lies between E and delta E settings.

Differential Delta E operates with respect to E. Pulse acceptance occurs when the pulse amplitude lies between E and delta E.

Lower Level Discriminator

Range From 100 millivolts to 10 volts in all three operating modes.

Integral Linearity 0.3% over the range from 100 millivolts to 10 volts.

Upper Level Discriminator

Range From 100 millivolts to 10 volts in the Independent Mode and from E to E +2 volts (i.e., 0% to 20% window) in the Differential Mode.

Integral Linearity 0.3% for both Independent and Differential Modes.

Differential Linearity Does not exceed 1% of window width.

Internal Strobe Discriminator

Generates a strobe pulse when input signal exceeds its threshold. Internal Strobe Discriminator Threshold is referenced to the Lower Level Discriminator Threshold; an internal trimpot provides continuous control of this bias from 0.35 E to E. A front panel delay control enables the actual strobe operation to occur at any time from 0.5 to 10 usec after Internal Strobe Discriminator triggering.

Strobe Switch

Internal Internal strobe discriminator determines timing of SCA output signal in relationship to the setting on the front panel Delay control.

External When in External strobe an SCA output signal is generated after a suitable strobe pulse is applied. The strobe pulse may be applied at any time after the E discriminator triggers.

Internal Reset Internal strobe discriminator resets the E and delta E discriminators as in normal Internal strobe operation, but the single channel analyzer anticoincidence gate must be strobed with an external pulse within the time period set on the front panel Delay control, if an SCA output signal is to be generated. Delays up to 30 microseconds may be obtained with additional capacitance.

External Strobe Input

Signal Requirements Rear panel BNC accepts a 3 volt to 10 volt positive pulse.

Impedance Approximately 400 ohms, A.C. coupled.

Pulse Shape Minimum width 20 nanoseconds. Leading edge used for timing and should be fast, i.e. 10-20 nanoseconds rise time, for minimum single channel output time jitter.

Single Channel Analyzer Output

Signal Characteristics Front panel BNC delivers a 10 volt positive rectangular pulse.

Impedance 50 ohms, A. C. coupled.

Pulse Shape 300 nanoseconds FWHM; 15 nanoseconds rise time, 15 nanoseconds fall time.

Pulse Pair Resolution

Approximately 0.6 microseconds in internal strobe.

Coincidence Output

Signal Characteristics Rear panel BNC provides a 6 volt positive rectangular pulse when D.C. coupled to the COINC/ANTI-COINC input of either a Series 2200 or 3300 Nuclear Data analyzer. A 2 volt positive rectangular pulse may be obtained by changing the position of two wires.

Pulse Shape Nominally 6 microseconds FWHM, a single component change allows output pulse widths from 1 to 10 microseconds.

Anti-Coincidence Output

Signal Characteristics Rear panel BNC provides a 6 volt negative rectangular pulse when D.C. coupled to the COINC/ANTI-COINC input of either a Series 2200 or 3300 Nuclear Data analyzer. A 2 volt negative rectangular pulse may be obtained by changing the position of two wires.

Pulse Shape Nominally 6 microseconds FWHM, a single component change allows output pulse widths from 1 to 10 microseconds.

General

Power Requirements +24 vdc at 25 ma
+12 vdc at 200 ma
−12 vdc at 50 ma
−24 vdc at 3 ma

Size 8.71" high x 1.34" wide x 9.7" deep (standard AEC single width).

Weight Approximately 2 pounds.

Part Number

74-0110

APPENDIX V

TECHNICAL SPECIFICATIONS

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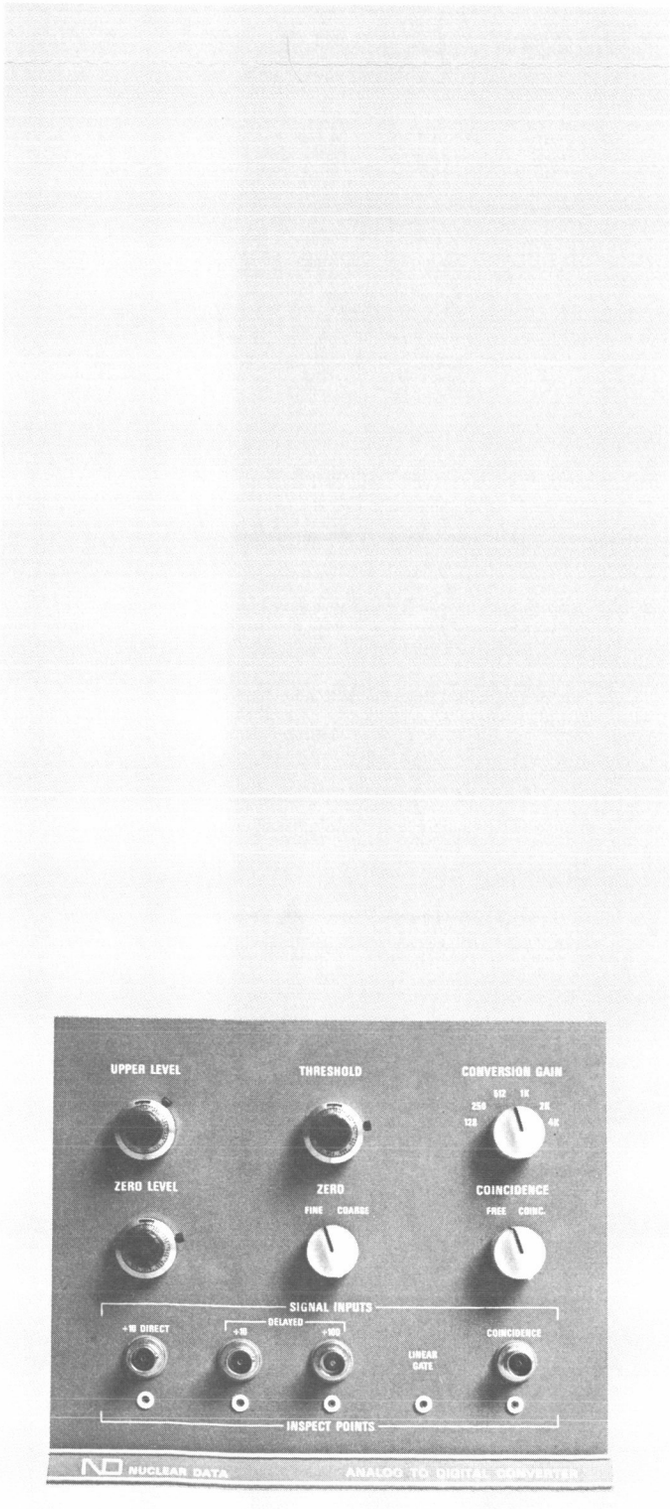

SERIES 3300 ANALOG TO DIGITAL CONVERTER

The Analog to Digital Converter Module (ADC) is designed primarily for processing of amplitude-modulated signal pulses, such as encountered in nuclear pulse height analysis. It contains an analog-to-digital converter and a twelve-bit address scaler that provide resolution of up to 4096 channels in-line.

Data acquisition efficiency is enhanced by a 16 megacycle digitizing rate which significantly reduces ADC dead time effects. The digitizing oscillator is crystal-controlled to ensure high long term stability. If desired, the ADC can be operated to accept input signals only when externally generated coincidence gating pulses are supplied.

Analog Conversion Gains

128, 256, 512, 1024, 2048, and 4096 addresses full scale.

Direct Access Signal Input

Pulse Requirements

- Amplitude: 0 to 10 volts nominal at minimum zero level.
- Polarity: Positive.
- Rise Time: 0.1 microsecond minimum, 5 microseconds maximum.
- Duration: 0.5 to 3 microseconds.

Slow A.C. and D.C. Signal Requirements

- Amplitude: 0 to 10 volts nominal at minimum zero level.
- Polarity: Positive (a D.C. offset can be introduced for analysis of bipolar signals of up to 10 volts peak-to-peak amplitude).

Input Impedance — Approximately 2 kilohms.

10 Volt Signal Input (Delayed)

Pulse Requirements

- Amplitude: 0 to 10 volts nominal at minimum zero level.
- Polarity: Positive or bipolar.
- Rise Time: 0.1 microsecond minimum, 5 microseconds maximum, exponential.
- Duration: 0.5 to 3 microseconds.

Internal Delay — 1.25 microseconds.
Input Impedance — Approximately 2.2 kilohms.

100 Volt Signal Input (Delayed)

Pulse Requirements

- Amplitude: 0 to 100 volts nominal at minimum zero level.
- Polarity: Positive or bipolar.
- Rise Time: 0.1 microsecond minimum, 5 microseconds maximum, exponential.

Duration: 0.5 to 3 microseconds.
Internal Delay — 1.25 microseconds.
Input Impedance — Approximately 22 kilohms.

Coincidence Input

Signal Requirements
Amplitude: +2 to +8 volts.
Polarity: Positive.
Duration: 0.1 microsecond minimum.
Input Impedance — Approximately 1 milliampere SINK (DTL Logic).

Conversion Time (PHA)

.0625N microsecond, where N is equal to the number of address advances produced for a given amplitude or duration, plus X ÷ 512 microseconds, where X is equal to the selected analog conversion gain.

Linearity

Integral
Better than 0.1% over the top 99% of full scale.

Differential
Less than 1% deviation from mean channel width over top 99% of full scale.

Zero Level

Adjustable from 0 to 100% of full scale.

Threshold

Adjustable from 0 to 25% of full scale, as selected by a front panel control.

Upper Level

Adjustable from 75% to 100% of full scale, as selected by a front panel control.

Stability

Time
Less than one channel drift per day at stable ambient temperature.
Temperature
Less than 0.1% zero drift and 0.2% gain drift per 5°C increase from 15°C to 40°C.

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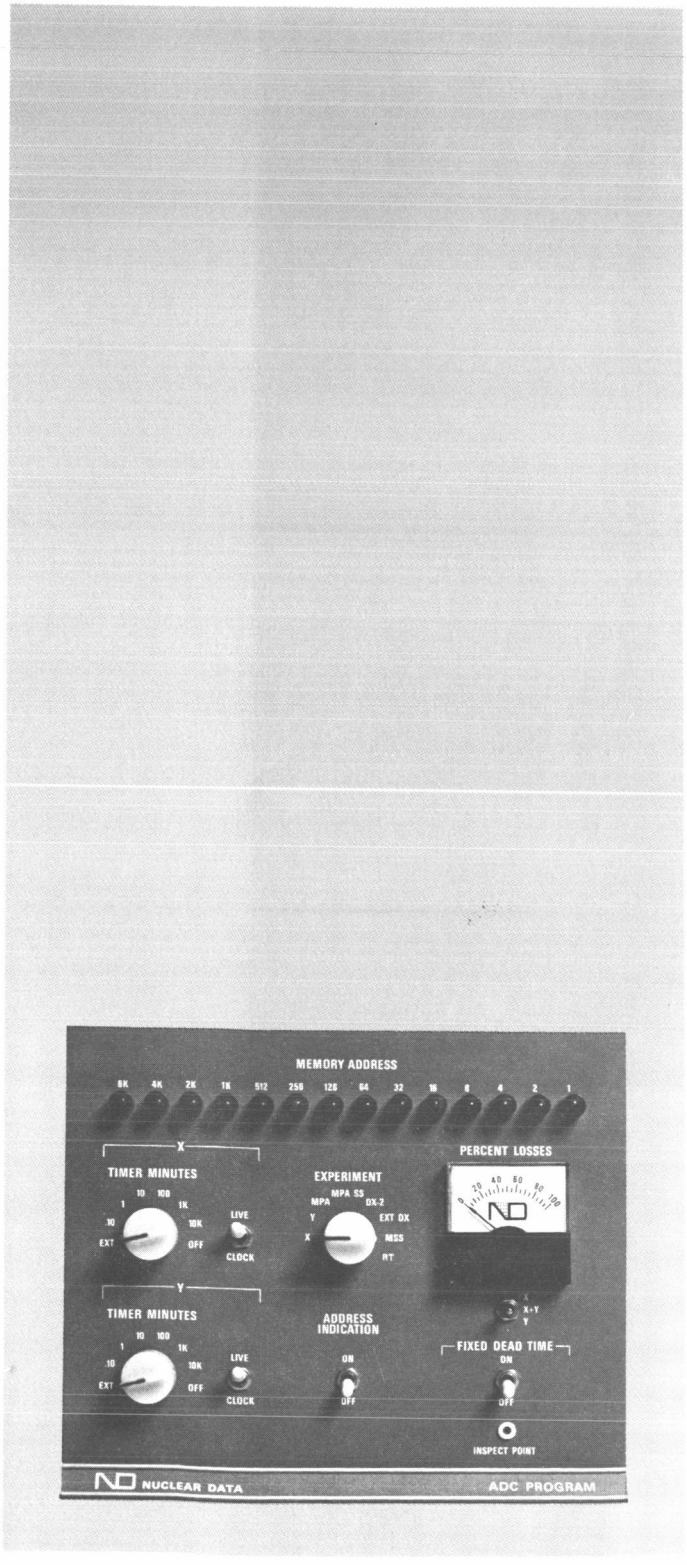

SERIES 3300 ADC PROGRAM

The ADC Program Module establishes the logical conditions for a variety of operations with either one or two Analog-to-Digital Converter Modules (ADC's). Operations which can be selected include single parameter analysis with either the X ADC or Y ADC, two parameter analysis with both the X and Y ADC's, two parameter operation with periodic singles spectra sampling, time-shared single parameter analysis (digiplex) with both ADC's, externally controlled digiplex, spectrum multiscaling and routing.

Two time reference oscillators, one for the X ADC and the other for the Y ADC, are provided for experiment timing. Either clock or live timing, with a wide range of reference units, can be selected. A fixed dead time for each ADC conversion gain factor can also be selected, if desired.

Memory address lamps are included to provide a binary indication of storage location. In addition, dead time indication is provided by a percent losses meter. A front panel control enables selection of dead time indication for either the X ADC, the Y ADC, or a combination of both.

ADC Operation

X: Single parameter analysis with X ADC.

Y: Single parameter analysis with Y ADC.

MPA: Two parameter analysis with both X and Y ADC's.

Singles Sampling: Two parameter analysis with periodic sampling of singles from X ADC and Y ADC, with singles stored in X=0 plane and Y=0 plane, respectively.

Digiplex 2: Single parameter analysis, with time-shared memory storage for data from the X ADC and the Y ADC.

External Digiplex: Time-shared single parameter analysis with external control.

Spectrum Multiscaling: Time-sequenced single parameter analysis, with separate storage for the spectrum acquired during each dwell period.

Routing: Single parameter analysis with time-shared ADC and separate storage for data from the X ADC for up to four inputs.

X & Y Time Units

0.1, 1, 10, 100 1K, or 10K minutes. An external time base can also be introduced, or the internal reference oscillator can be turned off, if desired.

Time Reference Stability

24 hours; Less than 0.01% deviation at constant ambient temperature.

Temperature: Less than 0.1% deviation per 10°C increase from 5°C to 45°C.

Live Time Accuracy

Better than 0.5% at input count rates of 5,000 pulses per second, with experiment times for adequate probability statistics.

Memory Address Indication

14 bits, scale of 16,384-1.

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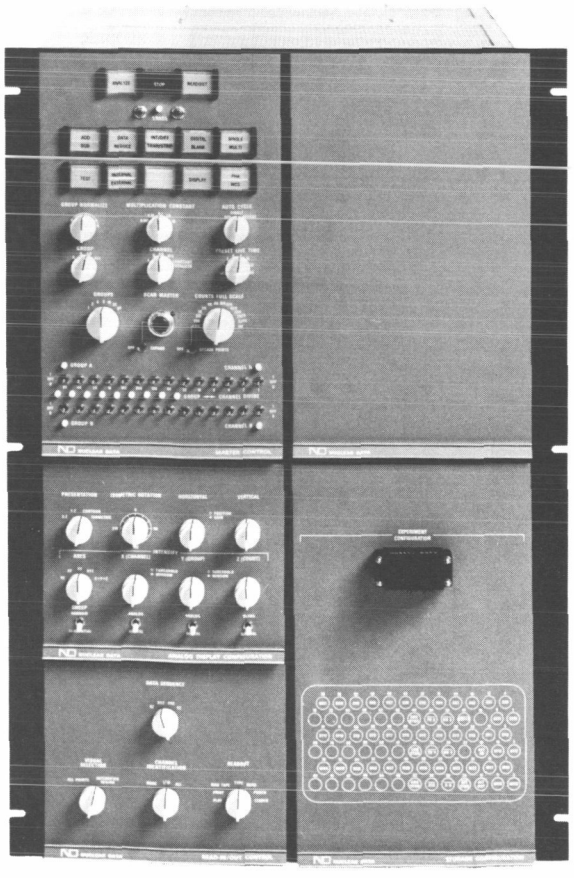


SERIES 3300 DATA HANDLING MAIN FRAME AND STORAGE CONFIGURATION

The nucleus of the basic Series 3300 Analyzer System is a modular data handling unit. It consists of a main signal distribution frame and modules associated with data handling functions. The signal distribution frame, which provides the mechanical and electrical facilities for acceptance of the modules, also incorporates digital circuitry required for data processing and related operations. Construction of the signal distribution frame is such that it can be housed in a standard relay rack or other similar enclosure.

Modules included in the basic Series 3300 Data Handling Unit are Master Control, Read-In/Out Control, Analog Display Configuration, and Storage Configuration. The Storage Configuration Module, which determines the storage format of data supplied by the System Data Acquisition Unit, can be replaced by other input data conditioning modules such as "Digital Band Selector" and "Region of Interest". A vacant module housing is also included with the basic Series 3300 Data Handling Unit. Its position can be occupied by a module such as a computer interface or an automatic program sequencer, if expansion of system capabilities is desired.

DATA HANDLING MAIN FRAME

Logic Levels

Standard logic levels of plus six (+6) volts for a logical "one" or true condition, and zero (0) volts for a logical "zero" or false condition are used throughout to facilitate system testing and to simplify interfacing, if required.

Address Register

The Address Register can retain sixteen bits of binary information. It can accept up to fourteen binary bits of information by means of parallel transfer, and provides parallel access to each bit for transfer out purposes. Up to fourteen of the least significant bits are used to locate storage locations in the System Memory. The two most significant bits are used exclusively for operations associated with the system display function.

In addition, the Address Register will scale at rates of up to one megacycle per second (1 MHz) and will operate as a shift register for system display functions.

Memory Register

The Memory Register can retain up to twenty bits of binary information. It will operate as an add or subtract scaler at rates of at least one megacycle per second (1 MHz). It provides binary information for storage in the System Memory during memory "write" operation, and accepts information of the

same bit content during memory "read" operation. Information can also be entered into the Memory Register by means of parallel transfer, and parallel access is provided for transfer out purposes.

Data Processing Register

The Data Processing Register accommodates up to twenty-four bits of binary or binary-coded decimal information. It will operate as either an add or subtract scaler, and forward or backward shift register. It is used in the modification of stored data during operations such as integration, stripping, and algebraic addition with data read from external sources.

In addition, the Data Processing Register is used in the formatting and binary to binary-coded decimal conversion of data for appropriate readout devices. It is also used in the reverse operation of conversion and formatting of data read in from external sources for memory storage or algebraic addition with previously stored data.

Serial Binary Adder

A Serial Binary Adder circuit is included for use in operations such as integration, stripping, and algebraic addition of read-in data with stored data.

Main Control Circuits

All flip-flops associated with the main operating modes of the system, i.e., Accumulate, Display, Readout, Stop, etc., are included.

Register Buffers

All buffers required for operations with the Address Register, Memory Register, and Data Processing Register are included.

Readout Timing Control

a. Digital Readout and Read-in
A timing control scaler for generation of program pulses during digital readout and read-in operations is included.

b. Magnetic Tape Readout and Read-in
A timing control scaler for generation of program pulses during magnetic tape readout and read-in operations is included.

Digital Readout and Read-in Solenoid Drivers

The solenoid drivers required for operation of appropriate digital readout and read-in devices is included.

Input/Output Connectors

Connectors are provided on a rear apron for cabling to and from the Data Acquisition Section, to and from the System Memory, to and from a Magnetic Tape Control Main Frame, to and from an external programmer, and to and from the System Power Supply. Also provided are connectors for operation of a high-speed parallel printer, paper tape punch, paper tape reader, typewriter, display oscilloscope, and X-Y recorder. Facilities for operation of a high-speed point plotter are also included.

Synchronization Points

A rear apron switch enables selection of oscilloscope synchronization points for system test and checking.

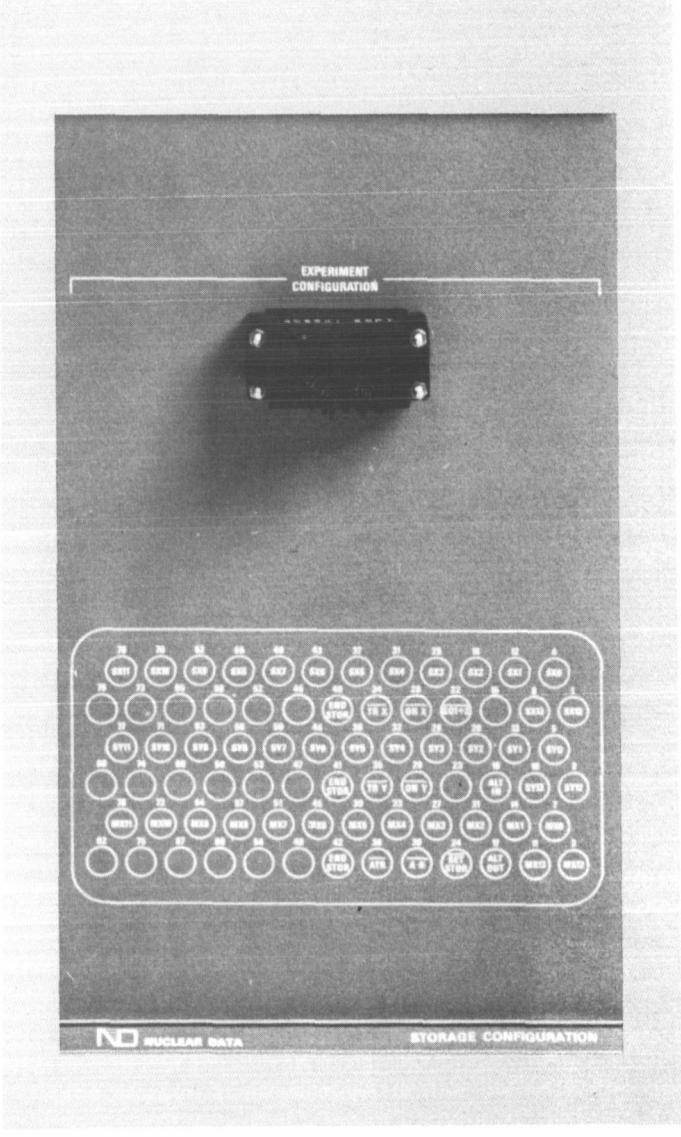
Sign Identification

For digital readout, disabling of non-significant zero suppression for negative number obtained by over-subtracting can be selected by a rear apron switch.

STORAGE CONFIGURATION MODULE

Program Receptacle

A front panel program board receptacle accepts a variety of pre-wired program plugs which establish the storage configuration of the memory. Storage configurations are $2^n \times 2^n$ where 2^n can be any binary multiple, providing the product of the two multiples does not exceed the number of channels in the system memory.



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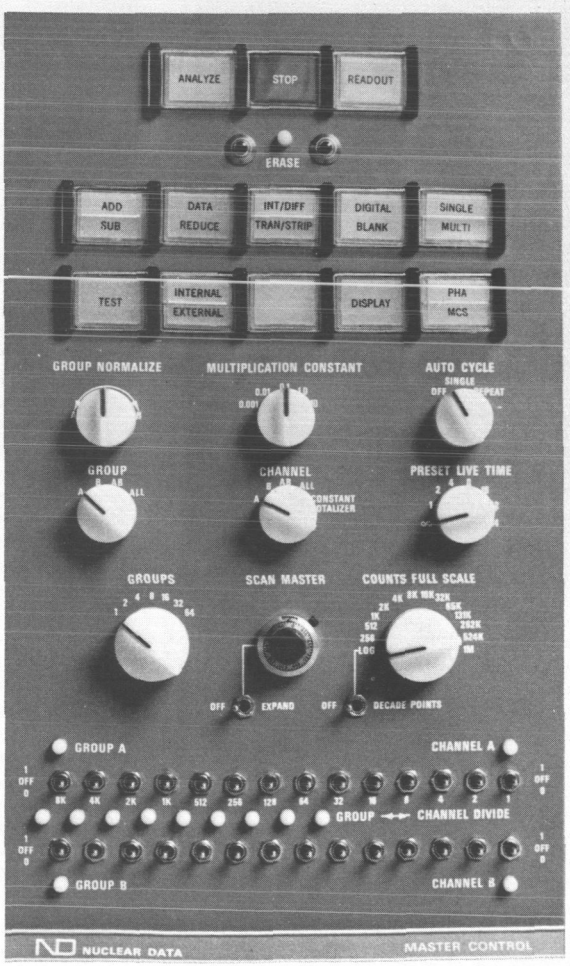

SERIES 3300 MASTER CONTROL

The Master Control Module contains facilities for establishing the primary operating modes of the Series 3300 System. In conjunction with the Data Handling Main Frame, it provides the facilities for all data processing functions. After data has been acquired, it can be subjected to operations such as spectrum stripping, integration, differentiation, multiplication, and transfer from one selected memory group to another.

Front panel controls enable digital selection of memory groups and channels for data storage, display, processing, and readout. Display intensification and digital blanking aid in determining area of interest location. The digital channel selection range is continuous down to one channel. Digital group size can be selected in binary steps down to 64 channels.

Logical programming for both pulse height analysis and multichannel scaling operation is another standard capability. In addition, a unique "Scan Master" feature enables stored data to be paraded through an expanded display window for closer examination. Only those data channels within the expanded window are addressed, providing a high scan rate regardless of window location.

Main Mode Selection

Illuminated pushbuttons establish the main operating modes of the system, i.e., Analyze, Stop, and Readout.

Sub-Mode Selection

Illuminated pushbuttons establish operational submodes subordinate to each main operating mode. These include:

DISPLAY — before, during, and after accumulation. During accumulation of data, display is provided prior to and after analysis of each event.
ADD/SUBTRACT — establishes whether data will be added to or subtracted from that previously stored in the System Memory.

TEST — provides a programmed add-one input to each channel of the memory interrogated during display operation. Add-one or subtract-one can be selected by means of the ADD/SUBTRACT Control.

PHA/MCS — PHA establishes the logical programming for pulse height analysis, MCS; the logical programming for multichannel scaling.

SINGLE/MULTI — SINGLE determines that, during display operations only one or two selected memory groups from the X-Axis channels will be interrogated; during readout, only one selected memory group will be interrogated; MULTI determines that all channels will be interrogated.

INTERNAL/EXTERNAL — INTERNAL enables manual selection of certain control functions, i.e., Analyze, Stop, Readout, Add/Subtract, and Data Reduce. EXTERNAL enables these functions to be externally programmed.

DIGITAL BLANK — increases the rate of display to provide optimum viewing of data digitally selected for area of interest intensification.

DATA REDUCE — initiates operation, as determined by the INTEGRATE/DIFFERENTIATE // TRANSFER/STRIP Control.

INTEGRATE/DIFFERENTIATE//TRANSFER/STRIP Control — INTEGRATE/DIFFERENTIATE enables selection of contiguous channels for either integration or differentiation of data stored within those channels. TRANSFER/STRIP enables data from a selected memory group to be multiplied by a constant, and then added to or subtracted from data in another memory group.

A multiplication constant indicator is provided by the first channel of each transfer group. The multiplication constants provided are 10, 1, 0.1, 0.01, and 0.001. Transfer also enables data read in from external sources to be added to, or subtracted from a selected memory group.

Memory Group Selection

Group size can be selected in binary steps (2^n) from 64 to the maximum number of channels provided by the System Memory.

Channel Selection

One channel or a selected band of channels in each memory group can be selected for digital intensification during display operation.

Arithmetic Decoding Resolution

In linear display, nine-bit decoding of digital arithmetic data provides resolution of up to 1 part in 512. Display ranges are provided in binary steps (2^n) from 256 to the maximum capacity of the System Memory.

Display Overlap

Stored data in two selected memory groups can be overlapped and normalized.

Automatic Programming

A control is provided for selection of three different program sequences:

1. Accumulate data for a preset time and then stop.
2. Accumulate data for a preset time and then automatically read out stored data nondestructively.
3. Accumulate data for a preset time, read out stored data destructively, and then repeat the same sequence until stopped by the operator.

Preset Live Times

For data accumulation in pulse height analysis, preset live time units are provided in binary steps (2^n) from 1 to 16 for an 18-bit memory word length or from 1 to 64 for a 20-bit memory word length. Live time units can be from .1 to 10K minutes, or some other externally determined increment, as established by the Data Acquisition Section of the system. A setting of infinity on the Preset Live Time Control enables data acquisition to continue indefinitely until stopped by the operator.

Logarithmic Display

Logarithmic display, either with or without a decade calibration pattern, can be selected. Decade calibration levels up to the most significant digit of maximum memory capacity are generated internally to facilitate display calibration.

"Scan Master" Display Expansion

A selected portion of the display can be expanded horizontally by a factor of ten to twenty as determined by a factory set level. Only the selected portion of the display is scanned to provide optimum viewing.

Memory Erasure Interlock

The memory, or selected portions thereof, can be cleared to zero only when two electrically interlocked pushbuttons are pressed simultaneously. This prevents inadvertent loss of data when one pushbutton is contacted accidentally. An indicator which physically separates the pushbuttons is illuminated when both are pressed.

Display Oscillators

Two display oscillators are included: (1) an address advance oscillator and (2) a shifting oscillator for logarithmic and linear display of arithmetic data.

Decade Pattern Generator

A decade pattern generator is included for calibration purposes in logarithmic display.

Digital to Analog Converters

Circuitry for decoding digital address and arithmetic data to an analog equivalent for display and readout operation is included. Decoded analog voltages are supplied via driver amplifiers.

"Scan Master" Generator

The circuitry associated with the generation of "Scan Master" horizontal display expansion is included.

Memory Group & Channel Select Gates

Logical gating circuitry for memory groups and channel region of interest selection is included.

Display Selection Control Gates

Logical gating circuitry for selection of various display operations is included.

Display Overlap Generator

The circuitry associated with the generation of display overlap for two selected memory groups is included.

Punched Tape Short/Long Leader

The circuitry associated with the generation of either a long or short leader for punched paper tape readout is included.

Lamp Drivers

Lamp driver circuitry for the illuminated indicators is included.

Address Identification Generator

Circuitry associated with the identification of memory group and channel region of interest for digital readout is included.

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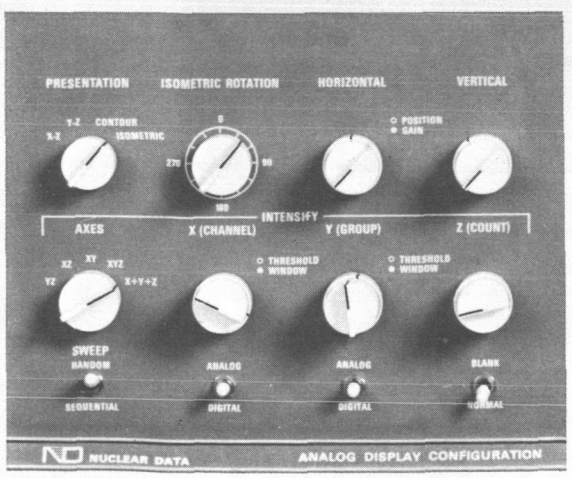

SERIES 3300 ANALOG DISPLAY CONFIGURATION

The Analog Display Configuration Module provides an exceptional degree of data-viewing versatility. It also provides a totally new display generation technique which resolves the problem of presenting large numbers of storage channels (words) at one time with a minimum of flicker effect. This is accomplished by means of unique quasi-random address selection circuitry.

Three basic methods of display can be selected: slice, with counts proportional to degree of vertical point displacement as a function of either of two input parameters; isometric, with counts proportional to degree of vertical point displacement as a function of two input parameters; and contour, with displacement a function of two input parameters. Either logarithmic or linear point displacement and point intensification can be selected for all display methods except the Z axis in logarithmic. In addition, decade calibration points can be superimposed on the logarithmic slice and isometric displays to aid in count level determination.

A feature which is especially useful in isometric display is a facility for rotating the analog presentation through 360° about its axis of symmetry. This makes it possible to observe energy relationships which may not be visible at some viewing angles.

During static display, data can be presented by high speed sequential scanning or by the quasi-random selection technique, as determined by a front panel control. During accumulation, even at extremely low counting rates, the viewing of data is greatly enhanced by the quasi-random technique.

Types of Display

The following types of display can be selected:

XZ — When SINGLE or MULTI submode operation has been chosen, display points are displaced vertically in linear or logarithmic relationship to the arithmetic data stored in each channel.

YZ — When MULTI submode operation has been chosen, each display point is displaced vertically in linear or logarithmic relationship to the arithmetic data stored in all channels of successive Y-axis slices.

CONTOUR — When MULTI submode operation has been chosen, display points represent the coordinate intersection of the X parameter (relative channel within a group) and the Y parameter (memory groups). Controllable count level discrimination provides selective blanking of displayed data points.

ISOMETRIC — Graduated displacement of horizontal display axes (relative channels within a group) and vertical display axes (memory groups) with data points displaced vertically in linear or logarithmic relationship to the arithmetic data stored in each absolute channel.

Isometric Display Rotation

The Isometric Display can be rotated 360° about its axis of symmetry in graduated steps of 15° to facilitate interpretation of two parameter data.

Display Position & Gain Control

Vertical and horizontal gain and position control is provided.

Region of Interest Intensification

A region of interest can be intensified by analog or digital selection for either closer examination or readout purposes.

X-Y-Z Analog Intensification Generators

Circuitry is included for analog selection and generation of area intensification.

Display & Analog Readout Amplifiers

Operational amplifiers for generation of analog deflection signals are included.

Post Voltage Regulators

Additional voltage regulation for analog display and readout circuitry is included to provide high stability and clarity in analog presentation.

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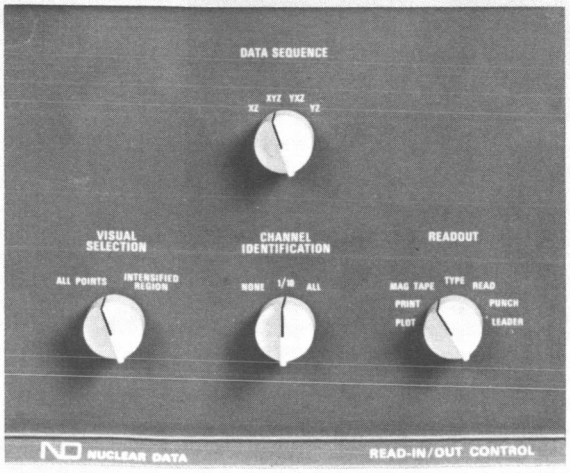

SERIES 3300 READ-IN/OUT CONTROL

The Read-In/Out Control Module provides control facilities for readout of stored data from the System Memory via a wide variety of analog and digital output devices. Included are facilities for high speed analog recorders, the IBM Model B Output Typewriter, the ND-316 Autofinger/IBM 721 Selectric Typewriter combination, Tally Paper Tape Perforator, and, upon request, high speed parallel printers. High speed magnetic tape readout of arithmetic data (counts) via an external Magnetic Tape Control Unit and tape transport can also be selected.

Control facilities for read-in of data via either a Tally Paper Tape Reader or an external Magnetic Tape Control Unit and tape transport are also included. In addition, front panel controls are provided for selection of address identification and arithmetic data sequence during digital readout.

Punched paper tape readout format conforms to the American Standard Code for Information Interchange, unless otherwise specified at time of purchase. Arithmetic data is punched in 1-2-4-8 binary-coded decimal form. An internal switch enables selection of either ASCII Code or IBM Code for punched paper tape read-in.

In conjunction with the Master Control Module and the Analog Display Configuration Module, a front panel control enables data to be visually selected for readout. The visual selection is accomplished by either digital discrimination with the Master Control Module, or by analog discrimination with the Analog Display Configuration Module.

Analog Readout Speed

Determined by maximum rate of plotter (typically 20 points per second for Houston 6550).

Digital Readout Speed

IBM Model B Typewriter: 10 characters per second; non-significant zeros are suppressed.

ND-316 Autofinger/IBM 721 Selectric: 12 characters per second; non-significant zeros are suppressed.

Tally Paper Tape Punch: 60 characters per second (120 characters per second upon request).

Parallel Printer: Determined by maximum rate of printer (30 lines per second for Franklin Model 1230).

Digital Read-in Speed

Tally Paper Tape Reader: 60 characters per second (120 characters per second upon request).

Address Identification

Address Identification during readout can be selected for either every tenth channel or every channel. It can also be disabled, if desired.

Data Sequence Selection

When address identification of data to be read out has been selected, the format can be chosen as follows:

XZ — Arithmetic data read out from each address location is preceded by either an absolute channel number, or the relative channel number within a selected memory group size, depending on whether single or multi submode operation has been selected at the Master Control Module.

XYZ — Arithmetic data is preceded by (1) the relative channel number within a selected memory group size (X), and (2) the consecutive number of the group (Y) being read out.

YXZ — Arithmetic data is preceded by (1) the consecutive number of the group being read out (Y) and (2) the relative channel number within a selected memory group size (X).

YZ — Arithmetic data is preceded by the consecutive number of the group being read out.

Visual Readout Selection

A facility is provided to enable readout of only that data chosen by region of interest display intensification.

Punched Tape Readout Code

Data is read out with ASCII Code, unless otherwise specified at time of purchase. Either an IBM compatible or ASCII Code can be selected for read-in of data with punched paper tape.

Type/Punch/Read Timing Generator

A timing generator is included which programs the sequence of operations for readout with either a typewriter or paper tape perforator, or read-in with a paper tape reader.

Zero Suppression Generator

Circuitry is included for suppression of non-significant zeros during typewriter readout.

B.C.D. to Decimal Decoder

Four-line B.C.D. to ten-line decimal decoder circuitry for typewriter readout is included.

Punched Paper Tape Coder

Coding circuitry is included to encode punched paper tape format during readout, and to decode punched paper tape format during read-in.

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SERIES 3300 SYSTEM MEMORY Unit

The System Memory Unit is a coincident current magnetic core type. Its function is to store data supplied by System Data Acquisition Units, or other external sources, and to supply this data for either further processing or readout upon command. Storage capacity can be either 4096 twenty-bit words, 16,384 eighteen-bit words, or 16,384 twenty-bit words, as specified when ordered. The time required to complete a full read-add one-write storage cycle for one word of data is four microseconds.

Included in the System Memory Unit are a magnetic core stack, memory drive circuitry, and associated address selection circuitry. Straight binary address and arithmetic coding are used to achieve the most efficient utilization of the core stack and associated binary circuits.

Number of Words (Channels)

The memory can store up to 4096, 8192, or 16,384 words of binary data, as specified when ordered.

Word Length

4096 -- Up to twenty binary bits of information can be stored at each word location. This provides a maximum capacity of 1,048,575 counts for totalization of data.

16,384 -- Either eighteen or twenty binary bits of information can be stored at each word location, as specified when ordered. This provides a maximum capacity of 262,143 or 1,048,575 counts for totalization of data.

Storage Cycle Time

One word of data is extracted from the memory, modified, and then re-inserted within four (4) microseconds (Read, Add-1, Write).

Sense Amplifiers and Strobe

4096 -- The memory contains twenty sense amplifiers and strobe circuitry used in reading information from the magnetic core stack.

16,384 -- The memory contains either eighteen or twenty sense amplifiers and strobe circuitry used in reading information from the magnetic core stack, as specified when ordered.

Inhibit Circuits

4096 -- The memory contains twenty inhibit circuits used in writing information into the magnetic core stack.

16,384 -- The memory contains either eighteen or twenty inhibit circuits used in writing information into the magnetic core stack, as specified when ordered.

Word Selection

The memory contains the word selection circuitry used in writing information into and reading information out of the magnetic core stack.

Data Retention

No more than one word of data will be dropped if a power failure occurs, or if the power is turned off when the system is not in the STOP mode.

Temperature Range

The memory will operate satisfactorily within the range of 15° to 35° Centigrade.

Size

14" high x 19" wide x 22" deep.

Weight

35 pounds.

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SERIES 3300 SYSTEM POWER SUPPLY

The Series 3300 System Power Supply provides all necessary voltages for operating the Series 3300 System analyzer. Features include a meter for monitoring all voltages and indicator lamps for overload conditions, high temperature conditions and A.C. line. Automatic shutoff is provided when overload or high temperature conditions are encountered. All voltages are screwdriver adjustable from the rear panel.

Power Requirements

Approximately 760 watts.

Line Voltage Requirements

115 volts A.C. ±10%, 60 Hz.
220 volts A.C. (available upon request), 50 or 60 Hz.

Outputs

+6 volts D.C. at 12 amperes.
−6 volts D.C. at 6 amperes.
+15 volts D.C. at 2 amperes.
−15 volts D.C. at 2 amperes.
+22 volts D.C. at 2.5 amperes.
−22 volts D.C. at 2.5 amperes.
+48 volts D.C. at 1.5 amperes.
−48 volts D.C. at 0.5 amperes.

Ripple

Less than 10 millivolts peak-to-peak on all outputs.

Temperature Range

The power supply will operate satisfactorily within the range of 0° to 50° Centigrade.

Regulation

Output	Load	Line	Output	Load	Line
+6 VDC	0.5%	0.25%	+22 VDC	0.1%	0.1%
−6 VDC	1.0%	0.5%	−22 VDC	0.1%	0.1%
+15 VDC	0.2%	0.1%	+48 VDC	0.1%	0.05%
−15 VDC	0.2%	0.1%	−48 VDC	0.1%	0.05%

Fusing

The line input is fused with two 10-ampere slow blow fuses. All outputs are electronically fused.

Weight

Approximately 67 pounds.

Dimensions

Approximately 17" wide x 7" high x 21" deep.

Part Number

74-0064

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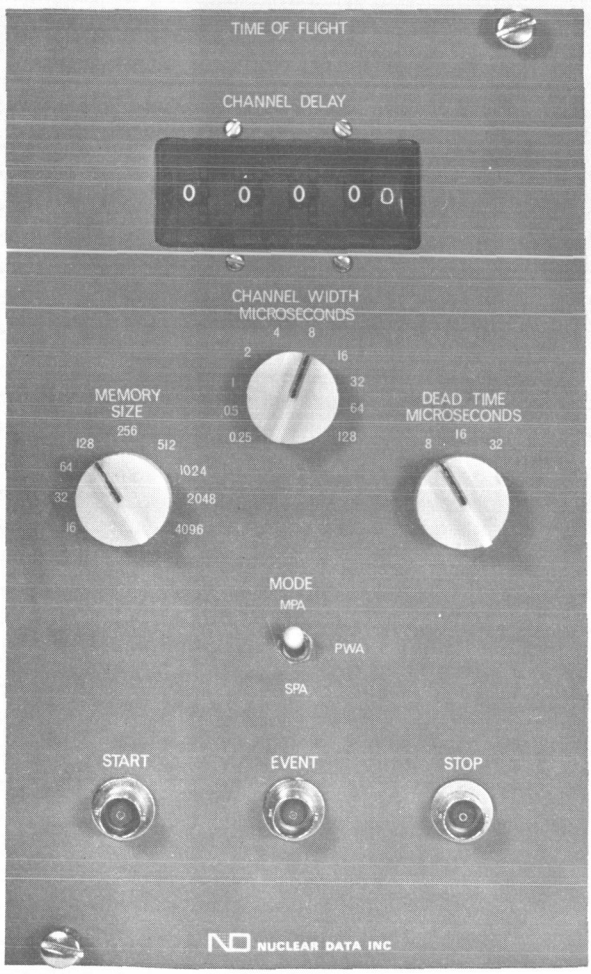

SERIES 2200 OR 3300 TIME OF FLIGHT

This NIM compatible Digital Time of Flight Module is a highly accurate and versatile unit that can be used with the Series 3300 or 2200 System Analyzer (as specified when ordered) to measure one-quarter microsecond minimum channel widths when performing operations such as encountered in neutron time of flight measurements. Pulse width analysis and single pulse analysis experiments may also be performed as selected by a front panel switch. A 32 MHz, crystal controlled oscillator minimizes channel time jitter and insures long term stability. A switch selectable, delay time control is included that incorporates no fixed internal delay and can be used to delay the start of analysis for up to 99,990 channels. A variable dead time, and memory capacity switch completes the complement of controls.

Start Input

Pulse Requirements
- Amplitude: 2 to 20 volts.
- Polarity: Positive.
- Rise Time: Noncritical; should be uniform.

Input Impedance — Approximately 2000 ohms.

Event Input

Pulse Requirements
- Amplitude: 2 to 20 volts.
- Polarity: Positive.
- Rise Time: Noncritical; should be uniform.

Input Impedance — Approximately 2000 ohms.

Stop Input

Pulse Requirements
- Amplitude: 2 to 20 volts.
- Polarity: Positive.
- Rise Time: Noncritical; should be uniform.

Input Impedance — Approximately 2000 ohms.

Input Signal Attenuation

None required as long as signal returns to less than one volt prior to completion of operation.

Clock Oscillator

32 MHz, crystal-controlled.

Channel Width (Time Duration)

0.25 to 128 microseconds switch selectable in binary increments.

Channel Time Jitter

$\pm 1/64$ microsecond.

Delay Time

0 to 99,990 channels thumbwheel switch selectable in 10 channel increments.

Fixed Delay

No fixed delay is incorporated in this unit. Delay times are as selected.

Dead Time

8, 16 or 32 microseconds, switch selectable.

Memory Size

16 to 4,096. Channels switch selectable in binary increments. 8192 or 16,384 sizes optional.

Power Requirements

+12 volts D.C. at 1 ampere.
−12 volts D.C. at 250 milliamperes.

Size

8.71" high x 5.36" wide x 9.7" deep (equivalent to four standard AEC single width modules).

Part Number

Series 2200; 74-0145
Series 3300; 74-0146

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