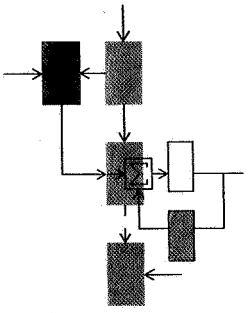
JANUARY, 1968

REPORT ESL-SR-337
M.I.T. PROJECT DSR 76152
NASA Research Grant NsG-496 (Part)



PART I
COMPUTER-AIDED ELECTRONIC CIRCUIT DESIGN

PART II
THIN-FILM ACTIVE DEVICE INVESTIGATIONS

Status Report

June 1, 1967 - November 30, 1967

Electronic Systems Laboratory

MASSACHUSETTS INSTITUTE OF TECHNOLOGY, CAMBRIDGE, MASSACHUSETTS 02139

Department of Electrical Engineering

January, 1968 Status Report ESL-SR-337 Copy 11

(PART I)
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and

(PART II)
THIN-FILM ACTIVE DEVICE INVESTIGATIONS

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The preparation and publication of this report, including the research on which it is based, was sponsored under a grant to the Electronic Systems Laboratory, Massachusetts Institute of Technology, DSR Project No. 76152. This grant is being administered as part of the National Aeronautics and Space Administration Research Grant No. NsG 496 (Part). This report is published for information purposes only and does not represent recommendations or conclusions of the sponsoring agency. Reproduction in whole or in part is permitted for any purpose of the United States Government.

Approved by John E. Ward

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ABSTRACT

This report describes progress and plans in the areas of On-Line Computer-Aided Circuit and System Design, and thin-film active device investigations.

Specific topics in the area of on-line design include (i) the tearing of networks into subnetworks, for improving computational efficiency; (ii) the development of a function-algebra and network production rules for making possible the noniterative solution of nonlinear resistive networks; (iii) progress in the CIRCAL-II on-line circuit-design program and data structure; and (iv) progress in LOTUS, an on-line program for block-diagram-system design.

Research in thin-film active devices has been directed towards an investigation of the structural and electrical properties of evaporated gallium arsenide films. The objective of this research is to develop a coplanar-electrode, space-charge-limited triode. An initial structural study has used transmission electron microscopy of GaAs films evaporated on NaCℓ substrates over the temperature range 270°C to 550°C. Electrical measurements have been on films evaporated onto amorphous glass and quartz substrates. Films in the resistivity range 10^3 to 10^7 ohm-cm have shown space-charge-limited current behavior of the form $V^{(T_c + T)/T}$. Doping studies have been made by diffusing from ultrathin evaporated layers of dopant. The effects of alloying of various metal contact films with the GaAs films have been observed.

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PART I

COMPUTER-AIDED ELECTRONIC CIRCUIT DESIGN

A. INTRODUCTION

Progress in On-Line Computer-Aided Circuit and System Design proceeded along several directions: Theoretical work involved continuation of research on the tearing of networks and on the functional algebra. Under "tearing", we have continued our study of the computational implications of separating the solution of a large network into the solution of smaller or "torn" subnetworks, and the subsequent interconnection of these solutions for the entire network; the main question here is "when and how" a network should be torn, in order to minimize computational effort. Under "functional algebra", we have continued to exploit the structure inherent to every network, by solving or "inverting" the characterizing systems of nonlinear equations through noniterative means; once again the motivation for this research is the reduction of computational effort involved in the solution of nonlinear networks and systems. Work also continued on the implementation of the CIRCAL-II program which is intended to serve as a general-purpose on-line network simulator for use in circuit design and in testing algorithms that evolve from our theoretical investigations. The executive, input-edit and data-structure-creating portions of this program have been implemented and are operating at this writing. Finally, work continued on the general-purpose, on-line system simulator LOTUS, a working version of which has been implemented. LOTUS differs from CIRCAL-II, in that it is intended for the simulation of block-diagram systems rather than of networks.

Progress and work outstanding in each of these areas of research are discussed in greater detail below.

B. TEARING OF NETWORKS

Professor M. L. Dertouzos

Mr. C. W. Therrien
Research Assistant

Work has continued on the use of tearing techniques for the solution of linear and nonlinear networks.

Some time was spent in formulating Kron's method of tearing* in graph-theoretic terms, and in applying the results to nonlinear resistive networks. Here, two distinct cases are considered. In the first case, the subnetworks resulting from tearing of the original network are assumed to be current-controlled at their ports of tearing. This formulation when applied to strictly linear networks yields Kron's result. In the second case, some of the subnetworks are current-controlled while others are voltage-controlled or mixed. Here, the equations for solution by tearing are derived together with the associated conditions for existence and uniqueness of solutions. When all subnetworks consists of a single element and (possibly) a source, these conditions guarantee the existence of unique solutions for a class of nonlinear resistive networks that includes that of Desoer and Katzenelson.**

Once the mechanics of solving networks by tearing are known, the question arises as to the way in which a network should be torn so as to yield the solution with the least computational effort. In order to answer this question for a very general class of networks, a tearing model has been formulated. The model postulates the existence of a computation function associated with each method of network analysis. This computation function has as its argument a measure of the size of the network graph and represents the computational complexity of the solution, which may be, for example, the number of computer operations required to produce the network solution. The computational complexity for any tear can then be expressed and compared, and some general results can be stated about the tearing of networks. These results indicate that the "optimal" tear splits the networks into approximately equal-size subnetworks with "few" interconnections. The results also indicate the best alternative tears when

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* Kron, G., "A Method for Solving Large Physical Systems in Easy Stages," Proceedings of the IRE, April, 1954.

** Desoer, C. and Katzenelson, J., "Nonlinear RLC Networks," Bell Systems Technical Journal, January, 1965.

an optimal tear does not exist. Moreover, quantitative results are possible when the precise form of the computation function is known for some specific method of network analysis. A computer program was used to evaluate the percent reduction in computational complexity when a linear network of 36 nodes is torn into two subnetworks. The graph of Fig. 1 illustrates the results by showing lines of equal computational complexity (equicomputation lines). Here m is the number of nodes in one subnetwork and k is the number of nodes at the port of tearing. Note that the physical constraint $2 \leq k \leq \min [m, 36-m]$ defines a triangularly shaped region in the k-m plane. The number next to each equal-complexity line is the percent reduction of arithmetic operations for tears mapping into points on that line. The shaded region indicates tears that increase computational complexity, i.e., where no savings are realized.

Although the kinds of tears which are most effective in reducing computational complexity have been determined, there is yet no satisfactory method for determining if good tears exist in a given network. Various topics in the realm of combinatorial mathematics are currently being explored in order to establish algorithms that locate optimal or "near-optimal" tears for any network.

C. FUNCTIONAL ALGEBRA

Professor M. L. Dertouzos

Mr. H. L. Graham,
Research Assistant

Research in this area involves continuation of the development of methods for nonlinear network analysis. The methods being investigated differ from the normal iterative techniques in that an initial computing effort is spent to "construct" the desired network response functions from which, for any given excitation, the response can be thereafter easily obtained.

First, an algebra of functions was developed by which the network-response functions can be represented in terms of the basic network-element functions. General algebraic techniques have been developed for obtaining the function representation from the nonlinear network equations. However, representations obtained in this manner

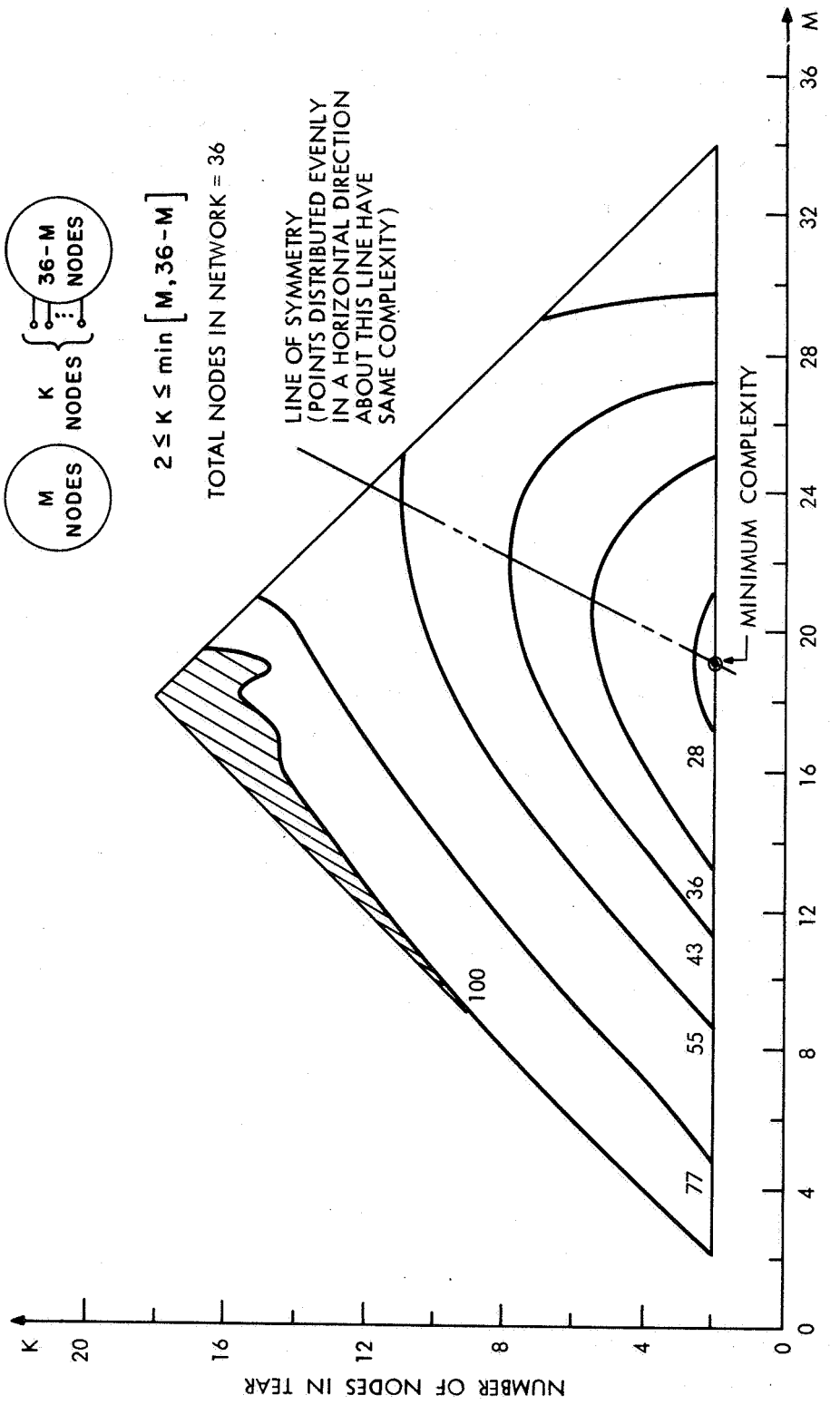

Fig. 1 Equicomputation Lines for Tears of a Linear Resistive Network

generally contain operations on functions of n-1 variables, where n is the number of network nodes. Since the computational effort expended in solution depends directly on the order (number of variables) of the functions being manipulated, practical considerations dictate the need for representations containing functions of the lowest possible order. For this reason, the concept of "network order" was established, and is explained below.

Define as members of class N_1 those networks that can be generated from two-terminal elements (generally nonlinear) by the set of Productions shown in Fig. 2. (Networks of this class are commonly known as series-parallel networks.) The driving-point, voltage-current response functions of networks in N_1 can always be represented in terms of first-order functions. This structural concept of networks can be extended to higher dimensions by defining as members of class N_2 those networks generated by the Productions of Fig. 3. Similarly, by defining as members of class N_k those networks that can be generated by combinations of networks in lower classes and other members of N_k, the response functions of any network contained in N_k can be represented in terms of functions of order k or less. Thus, we define the order of a network N to be k, if $N \in N_k$ and $N \notin N_{k-1}$. (Note that $N_1 < N_2 < N_3 \ldots$ etc.)

Present research is concerned with the development of techniques for determining network order so that it is, in turn, possible to construct network response functions, based on the associated network production rules.

D. CIRCAL-II: GENERAL

Professor M. L. Dertouzos

Mr. G. P. Jessel,
Research Assistant

CIRCAL-II is intended as a general system for the on-line analysis of networks. It consists basically of a number of files which are loaded (a subset at any one time) into the analysis portion of the system to produce results in the form of a graphical or tabular output.

Since the last report, most of the supervisory software of CIRCAL-II has been implemented. The file system is in operation and

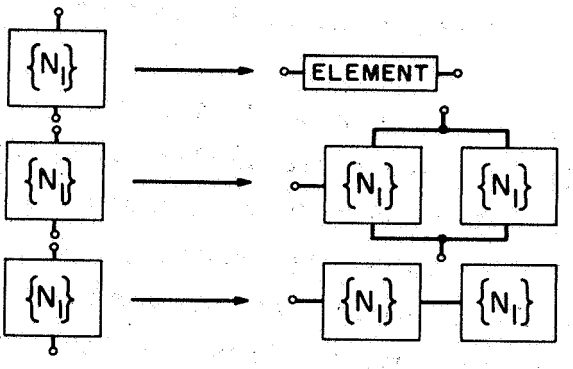

Fig. 2 Productions of class N_1

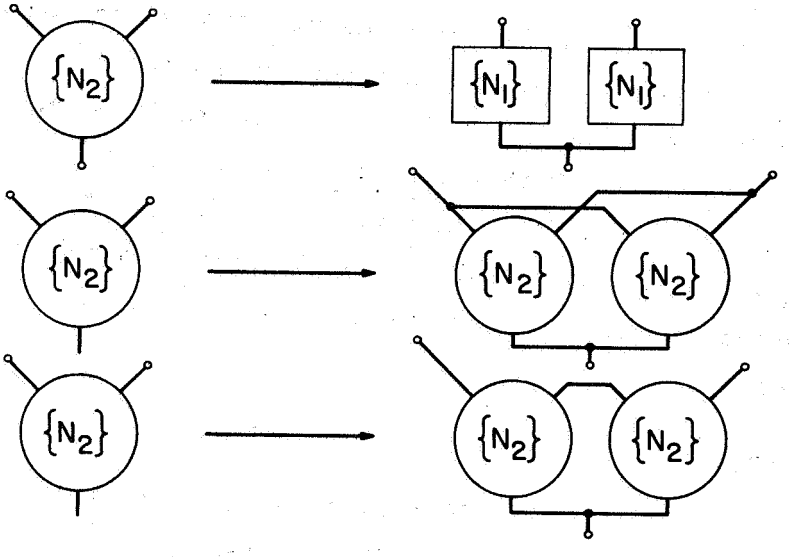

Fig. 3 Productions of class N_2

resembles that of the M.I.T. Compatible Time-Shared System (CTSS) used on the IBM 7094 at Project MAC. Each user is allocated a certain amount of storage, which will be used in conjunction with CIRCAL-II. All information needed by CIRCAL-II is stored in the form of files, regardless of the nature of such information. The types of files allowed include: circuits, nested elements, functions, functionals, and defined commands. A user may create new files or modify an already existing file by employing a single command. This command is a modified version of the CTSS INPUT/EDIT command which has been specifically oriented to the type of files and modifications encountered in network analysis.

The command structure of CIRCAL-II is geared toward user convenience. Considerable effort has been devoted to developing a set of commands which are both complete and concise. Since CIRCAL-II is intended for a wide range of users, two modes of operation are provided. The first has a minimum amount of interaction, while the second is oriented toward the less experienced user and provides numerous diagnostic and instructional aids. The commands of CIRCAL-II can be grouped into two sections. The first group deals with file operations such as printing, deleting and listing of all or part of the file directory contents. The second group deals with all phases of analysis.

A user initiates execution of analysis by simply providing the name of the circuit (file) under investigation and the types of analysis which are to be undertaken. A data structure compatible with this multiple-analysis format has been designed (see next section) so as to permit efficient network representation and application of each analysis algorithm. Values of program variables are saved in the form of a mode file and may also be stored in the file directory. Thus for re-analysis of a particular circuit, only those variables to be changed, (e.g., a parameter or time increment) need be specified. The topology of the network can be modified by employing a command which edits the data structure. For efficiency in computation, the data structure of a nested element may be stored in the file directory and reloaded whenever that nest is used in a circuit. In addition, a copy of the modified circuit under investigation may be stored at any time of the design process.

Present work has centered both on the development of the CIRCAL-II package and on the more theoretical foundations of the program. An output routine is currently being written which will be capable of displaying any function of the network variables resultant from any of the analysis routines. In addition, several existing analysis routines are being converted for use with the CIRCAL-II system. Finally, the formal structure of networks is under study for the purpose of representing in a most fundamental and efficient way the basic elements and operations that make up CIRCAL-II.

E. THE CIRCAL-II DATA STRUCTURE

Professor M. L. Dertouzos

Mr. J. Stinger,
Research Assistant

Work on the CIRCAL-II data structure for the period covered by this report was divided approximately equally into a development phase and an implementation phase. The data structure is of a general form: a list structure consisting of element beads, (a bead is a block of contiguous memory registers), node beads, and a network bead. The element and node beads, one for each element and node in the circuit, contain all the information necessary to completely describe that circuit.

Other features to be included in the data structure, such as the stringing together of all element beads, have been resolved. Especially helpful in this regard was a study of the data structures used or potentially usable among existing circuit analysis programs. The result of this study was a chart listing the proposed data structure features versus those of the various programs studied. Entries were divided into two groups: (1) features which the program must have to perform the analysis; and (2) features which would make the analysis more efficient. Those features which were most used by the programs were then included in the data structure of CIRCAL-II.

Since only a subset of all the features of this general data structure are needed by any given analysis routine, it was decided to make the data structure variable in size so that only the needed subset would be created for analysis purposes. If a designer decides to

use more than one analysis routine on a circuit, the data-structure is automatically adjusted to reflect the union of the features desired by each such analysis. In order that the data structure be amenable to future analysis programs with new features, provisions were made in the data-structure formulation that allow its expansion by the designer.

Implementation of the data structure followed the definition of a set of allowable standard CIRCAL-II elements. The Generalized String Package of AED was used to create the necessary data-structure portions. In addition, various functions (such as a search function) had to be defined for each type of string. A listing of the functions allocated to each type of string is contained in a gtc (generic type component) bead which is consulted by the programs before attempting an operation on a string of that type.

Currently, the data structure can be created directly from any circuit file in the user's directory. This process is recursive in that whenever a nest (an element consisting of other elements) is encountered, a data structure is created for it, unless it already exists. The data structure of a nest is identical in form to that of the main circuit.

Current work is centered on the user-controlled operators which edit the data structure. Allowed modifications are the addition or deletion of circuit elements, the changing of element values, and the replacing of one element with another element which has the same number of nodes. These modifications are easily executed regardless of network size due to the list-structure form of the data structure. Future work on the data structure involves implementation of that operator which stores data structures in the user's files.

F. LOTUS: ON-LINE SIMULATION OF BLOCK DIAGRAM SYSTEMS

Professor M. L. Dertouzos

Mr. M. E. Kaliski,
Fellowship Student
Mr. K. E. Polzen,
Research Assistant

LOTUS is a digital computer program for on-line analysis and simulation of block-diagram systems. These systems may be analog, digital, or hybrid; with or without memory; explicit or implicit

(i.e., having loops); vector or scalar valued; or of a more specialized nature, such as dynamic systems with integrators as memory elements. Simulation may be conducted in one or more dimensions such as time and/or space.

At the beginning of this research period, an extensive survey of existing simulation programs was made, and a set of system-representation fundamentals was established. Work was then concentrated on three major aspects of the program: (1) clarification of the system-modeling process and its simulation capabilities, (2) developing algorithms for realizing the system data-structure, and (3) implementation of these algorithms in the AED-0 language to obtain the first operating version of LOTUS. These three areas are described below.

The basis of the system-modeling process is the LOTUS sorting algorithm. This procedure rearranges the user's description of the interconnected system elements into an ordered list which allows the evaluation process to make a single pass through the system from inputs to outputs. The sort algorithm detects loops (memory and memoryless) and breaks the memoryless loops (in implicit systems) by inserting a fictitious "vacuous" element which acts as a bookkeeping mechanism for a subsequent iterative evaluation process. Optimal behavior in removal of all loops in this manner was shown to be equivalent to the optimal selection of a set of prime implicants that realize a given Boolean function; a problem for which general nonexhaustive algorithms do not exist. Thus, only a "locally optimal" sort is performed in LOTUS.

Limitations on the generality of the systems to be simulated by LOTUS are imposed by the numerical techniques which will be used for systems evaluation. Systems with loops cannot be nested, since such systems would require multidimensional iteration schemes which are impractical and inefficient. Similarly, in order to simulate simultaneous differential equations, all integrator elements must be "visible", i.e., integrators are not allowed to be "wrapped up" in nests.

The efficient organization of computer memory into an appropriate data structure has been dictated by (1) the need to model the

recursive aspects of system representations,* (2) the desire to edit system parameters and/or topology through the interactional nature of on-line simulation, and (3) the requirement to provide an efficient evaluation process. The recursive LOTUS data structure has been implemented, and a model for any one of the system-types mentioned in the introduction can be created.

The evaluation process involves (1) the definition of a finite domain over which the independent variable(s) will vary, (2) incrementing these variables in a user defined manner, and (3) making a single pass through the data structure to evaluate all system elements for each simulation point. The actual execution of the evaluation process is a recursive procedure which traces through the various sub-data-structures, transferring appropriate arguments, until it reaches a primitive evaluator, i.e., a precompiled machine-code subroutine.

For the past few months, work has centered on making operational the first version of the LOTUS program. The list-processing and free-storage capabilities of the AED-0 language have been extensively used. At this writing, explicit memoryless systems can be simulated and it is expected that systems described by ordinary differential equations will also be analyzed within a short time. Several programming problems are still to be solved, and timing studies must be performed to assess the time spent in (1) inputing a system description, (2) sorting the system elements, (3) creating the data structure, and (4) evaluating the system. Finally, the major programming problem which needs additional investigation is to determine how much more efficient the data structure creation process would be if data structures were saved on disc and called in as needed, rather than created each time that they are required by some system.

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* "On-Line Simulation of Block-Diagram Systems," by M. L. Dertouzos, M. E. Kaliski, K. P. Polzen (to be published), November, 1967.

G. PUBLICATIONS OF THE PROJECT

1. Current Publications

a. Reports

"Computer-Aided Electronic Circuit Design," Part I, Status Report ESL-SR-322, September, 1967.

b. Technical Papers and Conference Participation

Dertouzos, M. L. "An Introduction to On-Line Circuit Design," Proceedings of the IEEE, Vol. 55, No. 11, November, 1967, pp. 1961-1971; also Proceedings of the Fifth Allerton Conference on Circuit and System Theory, October 4-6, 1967 (Invited Paper).

Dertouzos, M. L., "Panel Discussion on Computer-Aided Design," Proceedings of the IEEE, Vol. 55, No. 11, November, 1967, pp. 1777-1778.

Dertouzos, M. L., Chairman of Session "Computer-Aided Circuit Design; A Critical Appraisal," NEREM 1967, Boston, November 3, 1967.

Dertouzos, M. L., Co-chairman of and Lecturer at Industrial Liaison Symposium on "Computer-Aided Circuit Design," M.I.T., October 3, 1967.

Dertouzos, M. L., Co-chairman of and Lecturer at M.I.T. Summer Course 6.56S on "On-Line Circuit Design," M.I.T. July 6-July 13, 1967. (One set of Proceedings issued at that course.)

Dertouzos, M. L., Talks and Demonstration on On-Line System and Circuit Simulation to:

a. EE Department, Catholic University of America, Washington, D.C., November 10, 1967.

b. IEEE Computer Group, Boston, October 11, 1967.

2. Past Publications

a. Reports

"Computer-Aided Electronic Circuit Design," Part I, Status Report ESL-SR-225, December, 1964.

"Computer-Aided Electronic Circuit Design," Part I Status Report ESL-SR-245, June, 1965.

Dertouzos, M. L. and Therrien, C. W., "CIRCAL: On-Line Analysis of Electronic Networks," Report ESL-R-248, December, 1965.

Dertouzos, M. L. and Santos, P. J., Jr., "CADD: On-Line Synthesis of Logic Circuits," Report ESL-R-253, December, 1965.

"Computer-Aided Electronic Circuit Design," Part I, Status Report ESL-SR-256, December, 1965.

"Computer-Aided Electronic Circuit Design," Part I, Status Report ESL-SR-274, June, 1966.

"Computer-Aided Electronic Circuit Design," Part I, Status Report ESL-SR-298, January, 1967

b. Technical Papers and Conference Participation

Reintjes, J. F. and Dertouzos, M. L., "Computer-Aided Design of Electronic Circuits," WINCON Conference, February, 1966, Los Angeles, California

Reintjes, J. F., "The Role of Computers in Modern Design Technology," Conference on Computer-Aided Design, University of Wisconsin, May 3 - 4, 1966.

Dertouzos, M. L. and Graham, H. L., "A Parametric Graphical Display Technique for On-Line Use," presented at Fall Joint Computer Conference on November 8, 1966. Published in the Conference Proceedings of the FJCC.

Therrien, C. W. and Dertouzos, M. L., "CIRCAL: On-Line Design of Electronic Circuits," presented at the NEREM Show and published in NEREM record November 9, 1966.

Notes: (1) Professor Dertouzos was Chairman of the Computer-Aided Electronic Circuit Design Session at the NEREM 1966 Conference, Boston, Massachusetts.

(2) CIRCAL-I was used from Munich, Germany via TELEX, June, 1966, in connection with a series of ten lectures by Professor Dertouzos at Siemens, Halske.

Katzenelson, J., "AEDNET: A Simulator for Nonlinear Networks," Proceedings of the IEEE, Vol. 54, No. 11, November, 1966, pp. 1536-1552.

Therrien, C. W., presentation on CIRCAL at N.Y.U. conference on "Network Analysis by Computer Symposium," New York University, January, 1967.

Dertouzos, M. L., Panelist in panel discussion, "On-Line Versus Batch," held at the NASA Computer-Aided Circuit Design Seminar, April 11-12, 1967, Cambridge, Mass.

Dertouzos, M. L., "PHASEPLOT: An On-Line Graphical Display Technique, "IEEE Transactions on Electronic Computers, Vol. EC-16, No. 2, April, 1967, pp. 203-209.

Dertouzos, M. L. and Fluhr, Z. C., "Minimization and Convexity in Threshold Logic," Seventh Annual Symposium on Switching Circuit Theory and Logical Design, Berkeley, California, 1966; IEEE Transactions on Electronic Computers, Vol. EC-16, No. 2, April, 1967, pp. 212-215.

Dertouzos, M. L. "CIRCAL: On-Line Circuit Design," Proceedings of the IEEE, Vol. 55, No. 5, May, 1967, pp. 637-654.

Dertouzos, M. L. and Graham, H. L., "A Parametric Graphical Display Technique for On-Line Use," M.I.T. Project MAC Seminar, May 19, 1966.

Evans, D. S. and Katzenelson, J., "Data Structure and Man-Machine Communications Problems," Proceedings of the IEEE, Vol. 55, No. 7, July, 1967, pp. 1135-1144.

c. Theses

Dvorak, A. A., "An Input-Output Program for Electronic Circuits Using a CRT," Bachelor of Science Thesis, Electrical Engineering Department, June, 1965.

Santos, P., "CADD, A Computer-Aided Digital Design Program," Master of Science Thesis, Electrical Engineering Department, June, 1965.

Therrien, C. W., "Digital-Computer Simulation for Electrical Networks," Master of Science Thesis, Electrical Engineering Department, June, 1965.

Fluhr, Z. C., "Single-Threshold Element Realizability by Minimization," Master of Science Thesis, Electrical Engineering Department, August, 1965.

Olansky, K. J., "A Low-Cost Teletype-Operated Graphical Display," Master of Science Thesis, Electrical Engineering Department, August, 1965.

Gertz, J. L., "A Graphical Input-Output Program for Digital System Simulation," Master of Science Thesis, Electrical Engineering Department, June, 1966.

Graham, H. L., "A Hybrid Graphical Display Technique," Master of Science Thesis, Electrical Engineering Department, June, 1966.

Meltzer, J. R., "CIRCAL: An Input for Nonlinear Elements," Master of Science Thesis, Electrical Engineering Department, June, 1966.

Taubman, C. N., "Computer Analysis of Electrical Analog Distribution Systems," Master of Science Thesis, Electrical Engineering Department, June, 1966.

Walpert, S. A., "An Output Program for Representing Electrical Signals," Master of Science Thesis, Electrical Engineering Department, June, 1966.

Edelberg, M., "A Dual Approach to Threshold Decomposition of Boolean Functions," Master of Science Thesis, Electrical Engineering Department, June, 1967.

Willems, J. D., "Synthesis of Logical Functions with Restricted Threshold Elements," Electrical Engineer Thesis, Electrical Engineering Department, June, 1967.

Smith, T., "Nesting of Networks for Computer-Aided Circuit Design," Bachelor of Science Thesis, Electrical Engineering Department, June, 1967.

d. Motion Picture

CIRCAL: Computer-Aided Electronic Circuit Design, January, 1966.

PART II

THIN FILM ACTIVE DEVICE INVESTIGATIONS

A. INTRODUCTION

The overall goal of these investigations is to obtain a useful active device in thin-film form. The primary advantage of such a device would be the potential for economical batch fabrication, together with other passive elements, by evaporation techniques. There is also potential for reduced size of circuits, greater tolerance to severe environmental conditions such as temperature and radiation, and very high gain-bandwidth products.

During previous reporting periods, work concentrated on space-charge-limited triode structures consisting of aluminum grids imbedded between layers of evaporated CdS films. As previously reported, problems were encountered with breakdown of the oxide layer insulating the grid which cast doubt on the feasibility of this approach, and no further investigations have been made during the present reporting period. A discussion of the thickness variation of breakdown field strength found for our plasma-oxidized aluminum films has been submitted to the IEEE Proceedings Letters, and will be published in January, 1968.

A more promising approach, on which work has concentrated during this reporting period, is a coplanar-electrode triode structure operated in a space-charge-limited mode. Gallium arsenide is a most attractive material for this purpose, since it has a fairly wide energy band-gap, can have a high charge carrier mobility (in bulk form), and should be capable of operation at high temperatures. Primary work to date has been in the investigation of structural and electrical conduction properties of GaAs films, and is reported in the following sections.

Work on coincident-radio-frequency techniques for writing and nondestructive readout of thin magnetic-film memories was inactive during this period, except for the writing of a final report. A draft has been completed, and the report should be published shortly.

B. STRUCTURE OF EVAPORATED GALLIUM ARSENIDE FILMS

Mr. W. S. Nicol
Staff Member
Mr. M. Blaho
Technician

1. Objective

The investigation of the crystalline structure of evaporated films is complementary to the measurement of electrical properties. Since no measured mobilities exceeding 1 cm^2/volt-sec have been reported for polycrystalline thin GaAs films, it seems likely that higher values should be achieved with ordered crystalline films. The surface properties (crystal structure, lattice constant, orientation, adsorbed impurities, temperature, etc.) of the particular substrate used largely determine film texturing and crystalline structure. The evaporation conditions of the sources (in our case, separate gallium and arsenic sources) are, however, also important.

Initial work with GaAs films has made use of rocksalt (NaCℓ) substrates. Although it is recognized that rocksalt would not be used as a substrate material for device purposes, it has been used in this phase of the work because it provides a convenient substrate for the examination of gallium arsenide films by transmission electron microscopy. Rocksalt has a cubic structure of lattice constant 5.64 Å (close to that of gallium arsenide--5.653 Å) and is easily cleaved. The gallium arsenide films are subsequently easily separated from the rocksalt by floating off in distilled water.

2. GaAs Films on NaCℓ Substrated over the Range 270°C to 550°C

The evaporation source used was described in the previous status report (ESL-SR-322, September, 1967), and has proved highly satisfactory. Evaporations are made from 99.9999% purity gallium obtained from Alcoa and 99.999+% purity arsenic, obtained from American Smelting and Refining Company. The substrates were 13 mm diameter cleaved NaCℓ slices, 2 mm thick. The slices were enclosed within an aluminum heater block, and were placed on an apertured plate which formed the lower side of the block. The apertures were 6 mm in diameter so that the lower (substrate) surface of each NaCℓ

slice was in contact with the plate over a substantial area. A thermocouple measurement of the temperature of the plate adjacent to an NaCℓ slice was taken as the value of the NaCℓ surface temperature.

Typical transmission electron diffraction patterns for GaAs films evaporated on NaCℓ at temperatures of 270°C, 330°C and 550°C are shown in Fig. 4a, b, c. Diffuse rings are observed at 270°C which correspond to the three most intense lines of α-Ga_2O_3. This is believed to be the result of the formation of free gallium which subsequently oxidized on exposure to the atmosphere. At 330°C, some texturing is observed as shown by weak arcing of the (111) and (220) reflections. At 550°C, the crystallite size was found to lie in the range 1000 Å to 3000 Å, as measured from transmission micrographs. Also, although the structure was still polycrystalline it was quite distinctly textured [100] as shown in Fig. 4c. It was expected that a much larger crystallite size and greater orientation would be observed at 550°C, than is seen in Fig. 4c, since single crystal epitaxial films have been formed by coevaporation by Steinberg and Scruggs.[1*] However, variable surface properties are almost certainly presented by rocksalt at temperatures approaching its melting point (800°C). This is also borne out by our observation that different growth rates were found for several rocksalt slices used during one evaporation.

The use of NaCℓ has helped establish the source conditions for satisfactory film evaporation. Future investigations will use sapphire and spinel as single crystal insulating substrates. Spinel has the advantage over sapphire of having a cubic structure. Samples of artificially grown spinel have been obtained for these investigations. Where semi-insulating substrates can be used for electrical measurements on lower resistivity GaAs films, these will be of single-crystal GaAs and Ge. Film structure will be studied by reflection electron diffraction.

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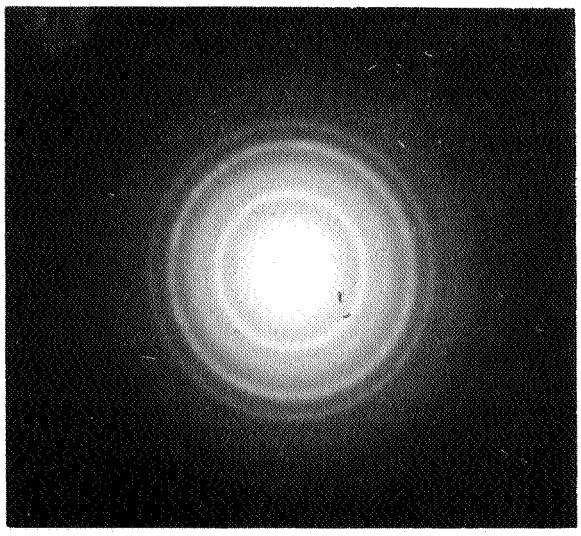
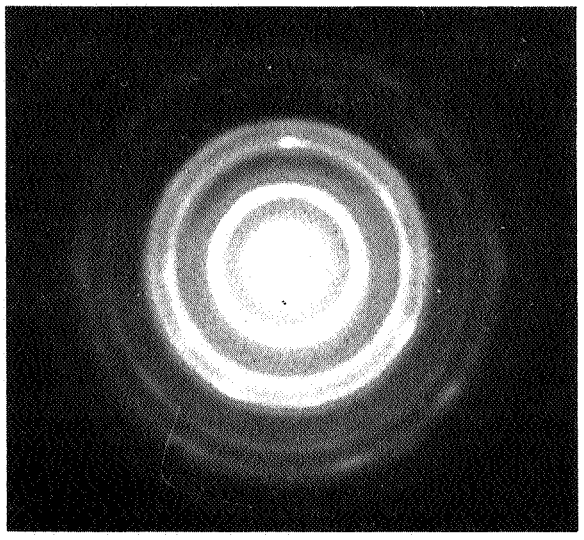
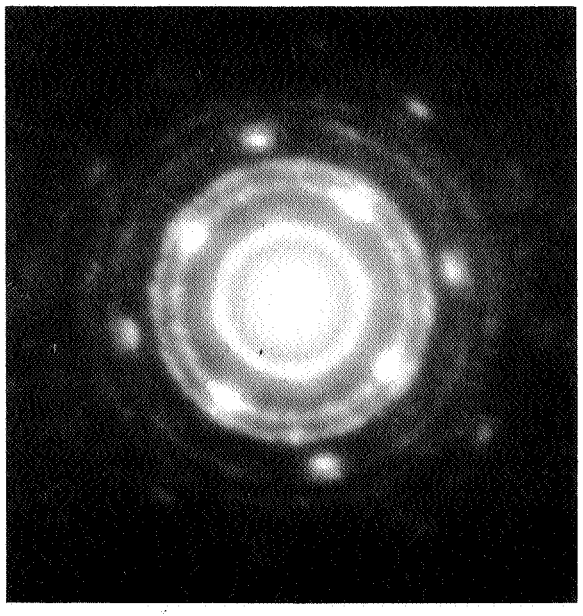
* Superscripts refer to the numbered items in the Bibliography.



(a)



(b)



(c)

Fig. 4 Transmission Electron Diffraction of GaAs Films Evaporated on Rocksalt Substrates, (100 kV)

a. Substrate Temperature 270°C

b. Substrate Temperature 330°C

c. Substrate Temperature 550°C

C. ELECTRICAL CONDUCTION IN GaAs FILMS

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1. Objective

For the satisfactory fabrication of a thin-film active device it is necessary to measure both the conduction properties of the films under various evaporation conditions and the influence of evaporated contacts on conduction. The conditions required to form both ohmic and Schottky barrier contacts are extremely important in this respect.

2. Evaporation Conditions Used

The modified Gunther crucible arrangement developed during the previous reporting period has enabled GaAs films of thicknesses up to one micron to be grown uniformly over 3" x 1" substrates. The gallium source temperature range used is 940°C to 980°C. With the higher gallium source temperatures it is necessary to increase the rate of arsenic evaporation to maintain the much higher impinging rate for the arsenic than for the gallium.

The substrate temperature range investigated was from 270°C to 550°C. Amorphous substrates of Fisher microscope glass slides, Corning 7059 Pyrex glass, and quartz were used. These were heated within a hollow aluminum block which contained a series of ceramic tubes heated by tungsten filaments. Based on the uniformity of evaporated film thickness, this arrangement has been shown to be very successful in providing uniform substrate temperatures. Pressures during evaporation were in the range 1×10^{-5} torr to 3×10^{-5} torr. The pressure measurements were made near the vacuum system baseplate and do not indicate the impinging rates of the evaporants. Residual gas pressures were in the range 5×10^{-7} torr to 3×10^{-6} torr.

3. Influence of Metal Films as Substrates and Counter-electrodes

Thin films of aluminum, gold, and silver were evaporated onto glass and quartz substrates at ambient temperature. These films

generally between 500 Å and 1000 Å thick. Gallium arsenide films up to one micron thick were then evaporated over the metal films at temperatures of either 270°C or 330°C. Finally, counter-electrodes of either aluminum, indium, gold, or silver were evaporated at ambient temperature; the complete structure being evaporated during one pumpdown of the vacuum system.

In the case of gold and silver substrate films, a reaction was observed to occur between the metal and gallium arsenide in that the reflectance of the metal films (observed through the quartz or glass substrate) decreased and the resistance of the metal films increased. It is believed that these effects are the result of alloying of the metals with the impinging gallium atoms. (It is well known that, similar to the case of mercury, gallium alloys readily with gold and silver.[2]) The resistance of the metal films increasing by at least an order of magnitude corresponds to the higher resistance of gallium alloys. A marked decrease in the reflectance of gold or silver films is observed with the addition of a small percentage of gallium. The aluminum films did not undergo any such changes, possibly due to passivation of the aluminum by the formation of a thin layer of aluminum oxide. However, the presence of any such layer was not detected during subsequent conductivity measurements.

The counter-electrodes were of thickness 200 Å to 500 Å. A few aluminum counter-electrodes were observed to have a bluish-white appearance over parts of the surface, although most films were highly reflecting. Several gold films, however, were observed to disintegrate several days after evaporation, with the appearance of a white film. On the assumption that any excess gallium occurs at the surface of the gallium arsenide films,[3] films were evaporated with gold counter-electrodes over GaAs films having an excess of gallium. The presence of a reaction was obvious. GaAs films were then evaporated with a prolonged arsenic evaporation after the gallium source was switched off. During the As evaporation the substrate remained at the GaAs evaporation temperature. No visible reaction was then found with gold counter-electrodes, even on heating the completed structure in air to 200°C.

As described in the following section, it is significant that the diode structures thus formed generally had ohmic contact properties, even after the prolonged arsenic evaporation described above.

4. Current-Voltage Characteristics of Metal-GaAs-Metal Films

Current-voltage characteristics of Al-GaAs-Al, Al-GaAs-In, Al-GaAs-Au diodes all showed ohmic injection up to a critical voltage. Above this critical voltage the characteristics displayed a variation $I \sim V^{(T_c+T)/T}$ as shown in Figs. 5 and 6. This has been

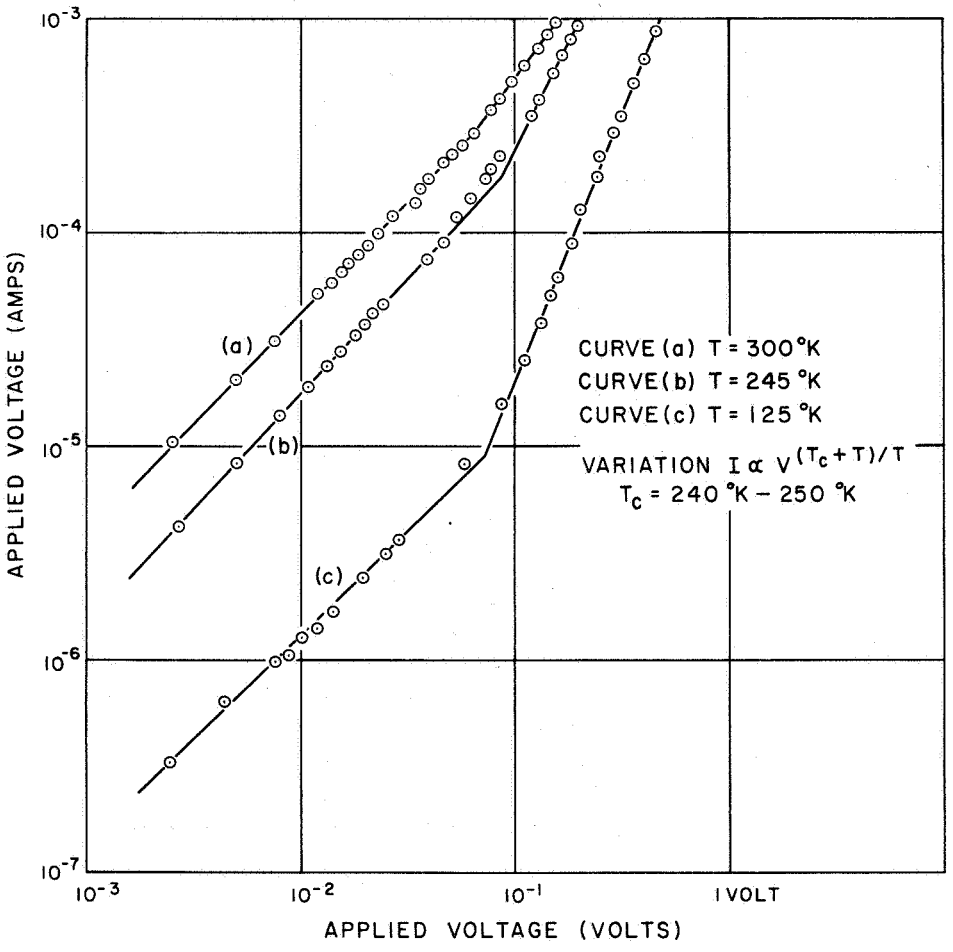

Fig. 5 Current-Voltage Variation of Aℓ-GaAs-In Diode

discussed by Rose[4] and Lanyon[5] as corresponding to space-charge-limited currents modified by the presence of an exponential distribution of trapping levels. For our films more than one value for

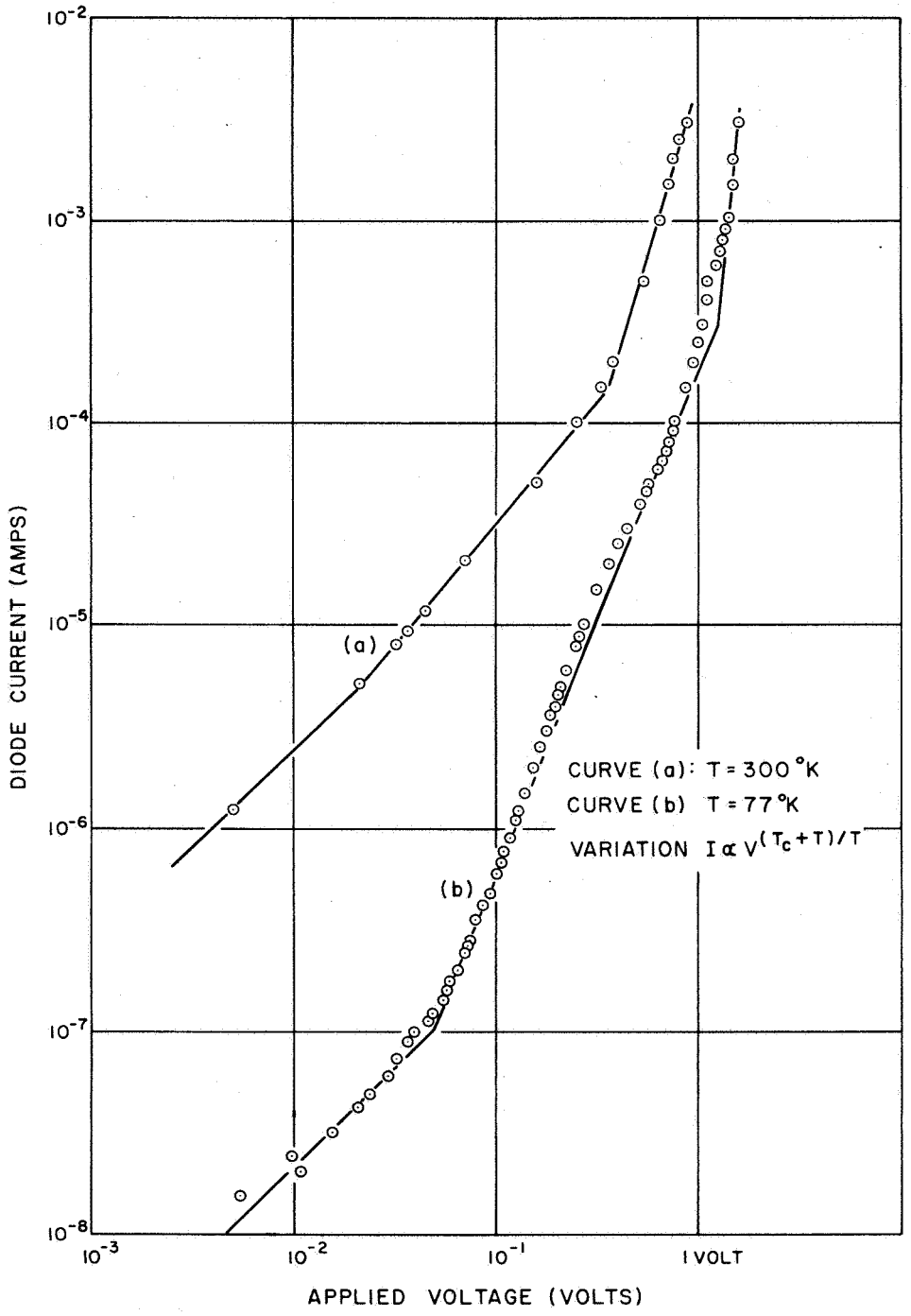

Fig. 6 Current-Voltage Variation of Aℓ-GaAs-Au Diode

T_c was observed. It was somewhat surprising that there was no evidence of Schottky barrier formation, since single crystal gallium arsenide forms Schottky barriers with all the metals investigated. Simple low-resistance paths, for example along grain boundaries or along diffused metal short-circuits, can be ruled out as giving rise to the region of ohmic conduction. This reasoning is based on the observation that several diodes did exhibit purely high-current short-circuit characteristics which were verified as being linear over several orders of magnitude of current. On increasing the voltage, breakdown occurred, after which the current dropped to the level obtained for the diodes in general. The $V^{(T_c+T)/T}$ variation was then observed for the nonohmic parts of the characteristics.

It is believed that alloying, as described in Section 3 above, may be responsible for the ohmic contacts on both sides of the GaAs films. If this is so, it may well be true that the presence of very thin surface films of free gallium can be detected by ohmic contact behavior of the counter-electrodes. On the other hand, it may also be true that alloying occurs during evaporation of the counter-electrode. It is planned to study the surfaces of GaAs films, in which visible reaction with the counter-electrodes occurred, by reflection electron diffraction. In this way the presence of free surface gallium will be detected.

Film resistivities measured in the ohmic region were found to lie in the range 10^3 to 10^7 ohm-cm. Longitudinal resistivities, measured between electrodes on the same surface of the GaAs film were found to be lower than those measured between electrodes on opposite sides.

5. Activation Energy Measurements in GaAs Films

Activation energies were measured over the range $77^{\circ}K$ to $400^{\circ}K$. These were generally close to 0.06 eV or 0.13 eV, which were the dominant conduction levels regardless of whether conduction took place in the plane of the GaAs film or normal to it. The effects of annealing and doping on these levels are not yet known.

A more complete description of the conduction behavior observed for the gallium arsenide films will be given in a thesis which is in preparation.

D. DOPING STUDIES IN GaAs FILMS

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1. Objective

It is anticipated that GaAs films of both p and n type may be required in an active device. In addition the influence of doping on mobility is not known for the films. Thus, an investigation of doping the films by diffusion from evaporated layers of dopant material was begun.

2. Diffusion from Evaporated Layers

Diffusion studies thus far have used copper and tin as dopant materials. The use of a large source-to-substrate distance (24 cm) allows control of the degree of doping to be made, even though relatively large amounts of dopant (1-10 mgm) are evaporated. The GaAs films are evaporated in two stages with the dopant film evaporated between the stages. Finally, the whole structure is heated to 500°C for 30 min. After cooling to room temperature an aluminum electrode is evaporated at each end of the film. The GaAs films are mask-evaporated in the shape of Hall samples. However, due to the extremely low mobilities of polycrystalline GaAs films, verification of the charge carrier sign is by thermoelectric power measurement. The apparatus which has been constructed for this measurement has aluminum blocks which make pressure contact with the aluminum electrodes. Aluminum wires are connected to these blocks to eliminate thermocouple effects. A tungsten heater imbedded in a ceramic tube is placed close to one of the aluminum blocks. The thermoelectric voltage is measured with a Keithley 603 electrometer amplifier.

This work will be extended to other dopant materials and to observation of the effects of various amounts of doping on conduction. The use of large-area films will permit optical absorption measurements to be made on the films used for electrical measurements of doping.

E. FUTURE INVESTIGATIONS

Structural studies of GaAs films will be pursued using reflection electron diffraction and possibly X-ray diffraction. Insulating single-crystal substrates of spinel and sapphire will be used. Where semi-insulating substrates can be used, single-crystal GaAs and Ge will be used.

The emphasis of the research on conduction will be in two main areas: an attempt to achieve useful Hall mobilities and a study of the formation of Schottky barriers. Both will be the subject of thesis investigations. The effect of long-term annealing and doping on mobility will be studied still using amorphous quartz and glass substrates, but emphasis will be placed on obtaining larger crystallite growth with single-crystal substrates.

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F. PUBLICATIONS OF THE PROJECT

1. Current Publications

a. Reports

"Computer-Aided Electronic-Circuit Design," Part II, Status Report ESL-SR-322, September, 1967.

b. Technical Papers

Nicol, W. S., "Thickness Variation of Breakdown Field Strength in Plasma Oxidized Aluminum Films," (To be published in January, 1968 issue of the IEEE Proceedings Letters.)

2. Past Publications

a. Reports

"Conduction Processes in Thin Films," Part II, Status Report ESL-SR-225, December, 1964.

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b. Article

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c. Theses

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Jenssen, H. P., "De-excitation of CdS Films by High Electric Fields," Bachelor of Science Thesis, Department of Electrical Engineering, June, 1965.

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