THE DESIGN OF A NEW SOLID STATE ELECTRONIC ITERATIVE DIFFERENTIAL ANALYZER MAKING MAXIMUM USE OF INTEGRATED CIRCUITS

by

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ABSTRACT

This dissertation describes the third generation of high-speed iterative differential analyzer systems designed and built in the Analog/Hybrid Computer Laboratory at The University of Arizona. The APE II system, a new hybrid computer for laboratory instruction, served as a test vehicle for new shielding and packaging techniques and the use of current-mode integrated-circuit logic for digital control of computer operations.

LOCUST, an all-solid-state iterative differential analyzer employs ± 10-V, 30-mA amplifiers with 30 MHz unity-gain bandwidth and can operate at iteration rates as high as 2,000 analog computer runs per second as well as in real time. Computing elements are plugged directly into the rear of a modified inexpensive patchbay which has removable patchboards. Subroutines are controlled by a flexible digital control unit as well as by patched digital logic or by an associated digital computer. New linear and digital monolithic integrated circuits along with a novel patchbay shielding system and computing-element packaging techniques have enhanced computer performance and reduced costs.

This description of the LOCUST system includes performance data, circuit diagrams, examples of applications and an instruction manual.

Chapter 1

INTRODUCTION

This dissertation describes the design and development of a "third generation" of iterative differential analyzers at the Analog/Hybrid Computer Laboratory of The University of Arizona. These computers include the APE (Arizona PEdagogical) II system, a small solid state iterative computer for laboratory instruction and the LOCUST (LOw CoST) system, a larger, more sophisticated iterative differential analyzer; both employ integrated circuits.

It is the purpose of the Analog/Hybrid Computer Laboratory to provide students with engineering experience related to their academic work and yet comparable to industrial experience. In accordance with this policy, the writer, as part of his Ph.D. research assignment, coordinated and supervised the development of these two computer systems, which draw on the experience of numerous graduate M.S. theses and student term-paper projects. The M.S. theses and term papers which contributed directly to the APE II and LOCUST projects are listed in Table 1.1. The writer acted as project engineer, under the direction of Professor G. A. Korn, with responsibility for design, construction and testing for the LOCUST system and for much of the APE II project, the supervision of student technicians and of student projects. In addition, a maintenance manual and an instruction manual were prepared.

Table 1.1

Student Contributions to APE II and LOCUST

Naylor, J. R.,	"A New High Performance Computer D-C Amplifier," M.S. Thesis, 1967.
Shick, L.,	"A Simplified Dual-slope Digital Voltmeter," M.S. Thesis, 1968.
Pracht, C. P.,	"A New Digital Attenuator System for Hybrid Computers," M.S. Thesis, 1967.
Belt, J.,	"An Integrated-circuit Binary Noise Source," Term paper, 1968.
Goltz, J. R.,	"A New Low-cost Analog-to-digital Converter for Hybrid Computers," Special course project, 1968.
Mueller, J. D.,	"An Overload Circuit for Iterative Differential Analyzers," Honors project, 1967.

1.1 Iterative Differential Analyzers

An analog computer with integrator-mode and program switches controlled by sequence-controlling digital clocks, analog-comparator outputs, and/or other digital logic is called an iterative differential analyzer (Eckes and Korn, 1964). Such machines can automatically perform successive analog computer runs utilizing stored results of previous runs and can, therefore, implement iterative computations converging to a desired solution. The automatic programming features have many other applications as well (Korn and Korn, 1964).

Iterative differential analyzers are programmed through a series of subroutines, such as an analog computer run or a number of repetitive-analog-computer runs. Each subroutine is controlled by its associated

digital control variable U_i (Fig. 1.1). The subroutine proceeds when $U_i = 1$; $U_i = 0$ "resets" the computing elements (e.g., integrators, counters) for a new subroutine sequence. Note that $\bar{U}_i$, the logical complement of U_i, may also define a subroutine. Subroutines may be "nested", i.e., a subroutine may have component subroutines; branching and loops are possible.

Typical analog-subroutine changes are combinations of the following operations:

1. Switching a group of integrators from RESET to COMPUTE, or from RESET (TRACK) to HOLD.
2. Switching to new values of parameters or to new initial conditions (e.g., parameter optimization, automatic scale factor changes).
3. Switching interconnections to produce computer-setup changes.

Subroutines begin and terminate when their corresponding control variables change state as logical functions of (1) external control (switches and/or relays controlled by external devices), (2) the states of timers or event counters, and (3) analog-comparator decisions. Boolean functions of such control inputs are implemented by patched digital logic, or by an associated digital computer.

The interplay of analog and digital variables gives the computer its hybrid structure. Relays, electronic mode-control switches, D/A switches, D/A and A/D converters and analog comparators are the interface elements of the system.

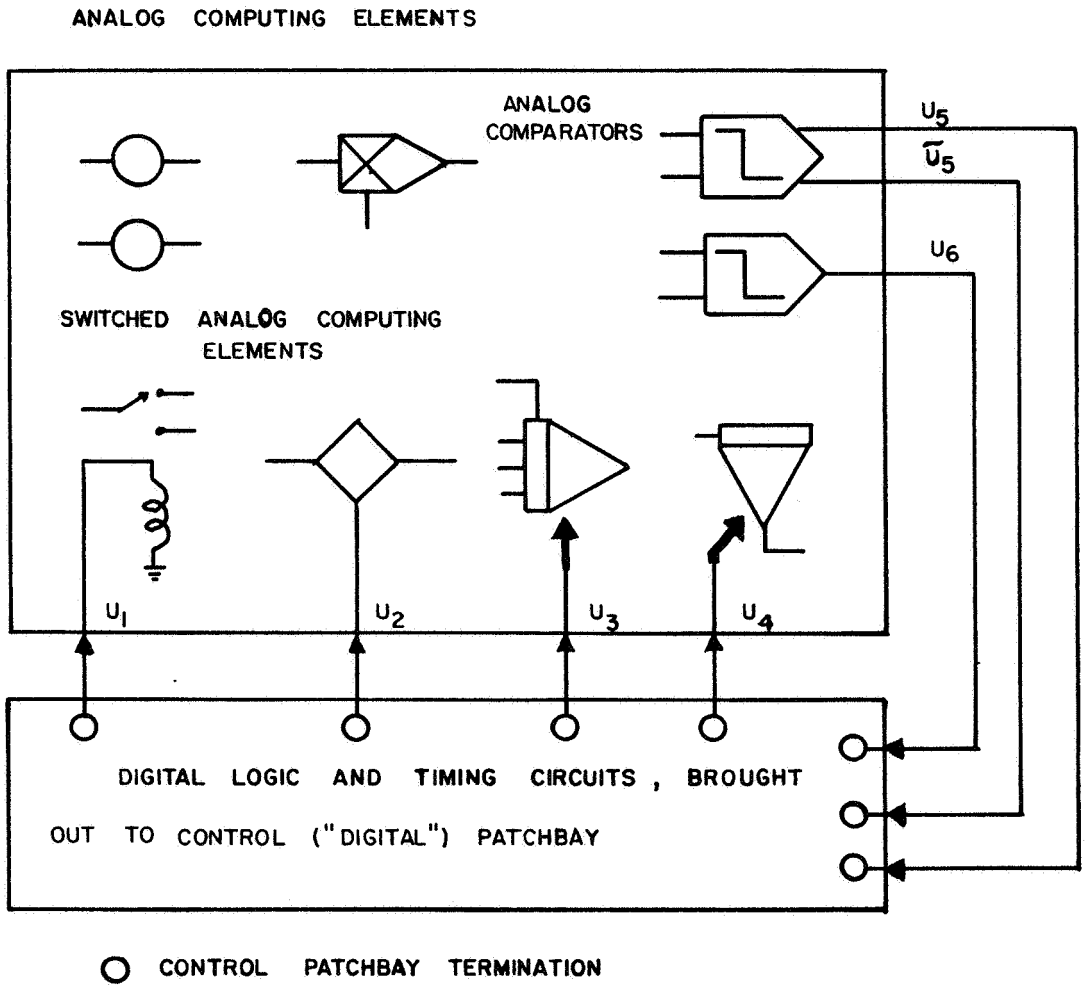


Fig. 1.1 Iterative-differential Analyzer System

The high-speed iterative differential analyzer and the small general purpose digital computer are particularly well suited to operate together (Korn, 1966a). Since most analog-to-digital and digital-to-analog exchanges between the two occur only once or twice per analog-computer iteration, the digital computer has ample time to perform many logical and computational operations (e.g., memory storage, function generation, statistical computation). The digital computer may also provide timing and mode-control functions and perform housekeeping functions such as setting potentiometers (in modern computers, digital attenuators) and static checks.

1.2 Iterative Differential Analyzer Applications

High-speed iterative differential analyzers can implement much more sophisticated models than ordinary analog computers and at the same time still retain much of the intuitive appeal of the familar "slow" analog computer.

The iterative differential analyzer is particularly well suited to the following applications:

1. Iterative parameter optimization (Maybach, 1966). The computer varies parameters of a simulated system to improve some performance criterion measured and/or computed in successive computer runs.
2. Monte Carlo studies of random processes (Handler, 1967). The computer computes statistics over many computer runs at very fast repetition rates simulating systems with random inputs.

3. Simulation of sampled-data systems. High-speed integrator mode switches and D/A switches with convenient patchable digital control logic permit the simulation of various sampling and data-reconstruction schemes.

High-speed repetitive analog computation is a necessity for Monte Carlo and parameter-optimization studies if computation is to be completed in a reasonable amount of time. An additional feature is that the operator receives practically immediate feedback of the effects of system parameter changes on statistics, and automatic optimization of statistics is possible (Korn, 1966b).

Other interesting applications include:

4. Automatic sequencing of computations for plotting families of curves, special displays, etc.
5. Introduction of artificial errors into alternate computer runs for purposes of error analysis, sensitivity studies, etc. (O'Grady, 1967).
6. Automatic scale-factor changes.
7. Special simulation and data processing circuits, e.g., patchbay-assembled time-division and sampling multipliers, sampled-data-reconstruction units, digital voltmeters, special function generators, etc.

1.3 The Impact of Integrated Circuits

The impact of integrated circuits on the design, performance and cost of iterative differential analyzers has been great. Reductions in size and cost afforded by integrated circuits have made it possible to

design truly producible high-speed iterative differential analyzers at moderate cost.

The digital control section of a hybrid computer has been most radically affected by integrated circuits. Integrated-circuit flip-flops and gates have replaced discrete-component logic cards, resulting in a size reduction of an order of magnitude. Single logic cards now contain complete logic functions such as a master timer, auxiliary timer, subroutine counter, shift registers, binary noise sources and free logic. Small size allows these cards to be plugged directly into the rear of the digital patchbay system, reducing construction costs and eliminating long interconnections, which might radiate digital noise throughout the computer.

Digital integrated circuits, which are ten times faster than their older discrete counterparts, also reduce delay errors, an important consideration in high-speed iterative computers.

Parts costs have been reduced to one-third that of a discrete system by using fast emitter-coupled logic. Costs could be reduced even further if one were willing to accept the noise associated with larger logic-level swings and unbalanced-current operation of RTL, DTL, or TTL logic families.

The impact of integrated circuits on analog computing elements has been less dramatic than that on the digital elements, because the performance of integrated-circuit linear elements cannot yet match that of a discrete-component element. Both performance and cost can be improved, however, by combinations of linear integrated circuits and discrete components.

APE II and LOCUST analog comparators utilize commercial integrated-circuit comparators which have been provided with input circuit protection and output logic levels compatible with the digital control logic. These inexpensive analog comparators have only one-tenth the cost of comparable high-speed comparators made from wide-band operational amplifiers.

The LOCUST wide-band operational amplifier also includes two integrated circuit modules plus a discrete-component output stage. The conventional chopper stabilizer is replaced with a novel hot-substrate, integrated-circuit input stage, which provides much better drift performance than a high-quality non-chopper-stabilized amplifier. The mid-frequency stage of the amplifier employs an integrated-circuit amplifier, which is an operational amplifier in its own right! Designing high performance amplifiers in this manner eliminates the problems of transistor matching necessary with totally discrete-component amplifiers.

In addition to reduced parts costs and improved performance, integrated circuits reduce construction costs of computer systems; there are by far fewer parts to mount, fewer connectors, less cabling and wiring and less cabinet space required. The cost of separately testing and hand-picking critical components such as input-stage matched-transistor pairs is completely eliminated.

1.4 APE II and LOCUST

The feasibility of really high-speed hybrid computation with realistic accuracy (0.2 percent of half-scale component accuracies up

to 10 kHz) was demonstrated by the development and application of The University of Arizona's ASTRAC II (Eckes, 1967). As yet, no computer commercially available has the required mode-control switching speed and low-impedance computing networks. Most computers do not have the required amplifier bandwidth. Development of the APE II and LOCUST iterative differential analyzers was, then, undertaken with the specific objective of demonstrating the design of truly producible high-speed hybrid computers at moderate cost.

Several new design features are of special interest:

1. Maximum use of both linear and digital monolithic integrated circuits enhances computer performance and still reduces parts and assembly costs.
2. New techniques of mounting printed-circuit cards and shielded components directly to low-cost computer patchbays were developed, as was a new simple technique for shielding low cost unshielded patchbays.
3. Low level integrated-circuit, current-mode logic has practically eliminated digital noise in the analog computer.
4. The amplifier and mode-control switch designed for LOCUST were substantially improved by the use of new solid state devices.

Table 1.2 shows engineering data for the two new computers and compares them with ASTRAC II and with commercially available hybrid computers.

Chapter 2 contains a description of the APE II system. The LOCUST system design, which includes accuracy requirements, mechanical

Table 1.2 Comparative Computer Specifications

	Commercial Computers 1967	ASTRAC II 1965	APE II 1967	LOCUST 1967
D-C AMPLIFIER (±10V)				
Output Current	25-50 mA	30 mA	20 mA	30 mA
Max. frequency for full output	50 kHz	1 MHz	1 MHz	5 MHz
Small-signal OdB bandwidth (1V p-p)	100 kHz to 10 MHz	20 MHz	20 MHz	30 MHz
Drift vs. temp.	0.5μV/degC 0.05nA/degC*	10μV/degC 1nA/degC*	10μV/degC 0.2nA at 25degC**	2.5 μV/degC 0.05nA/degC
INTEGRATOR/TRACK-HOLD SWITCH				
Turn-off time	500-1000ns	80 ns	200 ns	40 ns
Differential turn-off time	125-250 ns[μ]	20 ns	50 ns	10 ns
Drift vs. temp. (RESET/TRACK)	negligible	50μV/degC 30nA/degC	100μV/degC 10nA/degC	100μV/degC 1 nA at 25degC**
Drift Current (COMPUTE/HOLD)	0.5 to 0.1nA	1 nA	0.1 nA	0.05 nA
Turn-off charge	negligible	50 pC	50 pC	10 pC
Max. frequency for full output	10 kHz[μ]	50 kHz	25 kHz	40 kHz
Small-signal TRACK error at 10 kHz	--	0.25%	--	0.2%
MULTIPLIER				
Static error (% of half scale)	0.05	0.1	0.25	0.25
Freq. for 0.5% of half scale dynamic error	0.5-2 kHz	10 kHz	10 kHz	10 kHz

*chopper stabilized **doubles every 10 degC [μ] estimated

layout and shielding, patchbay system and costs, is discussed in Chapter 3. Chapter 4 contains a description of LOCUST analog computing elements, and Chapter 5 describes special-purpose computing elements. Chapter 6 discusses the LOCUST digital system and digital control of iterative differential analyzers. Applications of the APE II and LOCUST systems are the subject of Chapter 7.

Chapter 2

THE APE II SYSTEM

In view of the increasing use of analog computers for teaching at the college sophomore level, a need has developed for introducing more sophisticated analog/hybrid computation and techniques into senior-level analog computer courses. At The University of Arizona, this need led to the development of the APE II (Arizona PEdagogical) system, a small solid state iterative differential analyzer designed for laboratory instruction.

The author carried out the design and development of the APE II digital control module (Conant, 1967) while the analog portion was designed by Professor G. A. Korn (Korn, 1967); the machine was built with the aid of undergraduate student technicians. The APE II system also served as a test vechicle for the digital techniques used in the larger and more advanced LOCUST system.

APE II (Fig. 2.1) is comprised of a twelve-amplifier analog computer with track-hold circuits and integrators permitting digital mode-control and repetitive operation, analog comparators, multipliers, patchable zener-diode limiters and diode bridges. Removable patchboards permit problem storage and efficient machine utilization.

The APE II digital module contains free logic (gates and flip-flops) as well as a flexible digital clock and counters capable of controlling analog subroutines. Shift-register modules and modulo-2

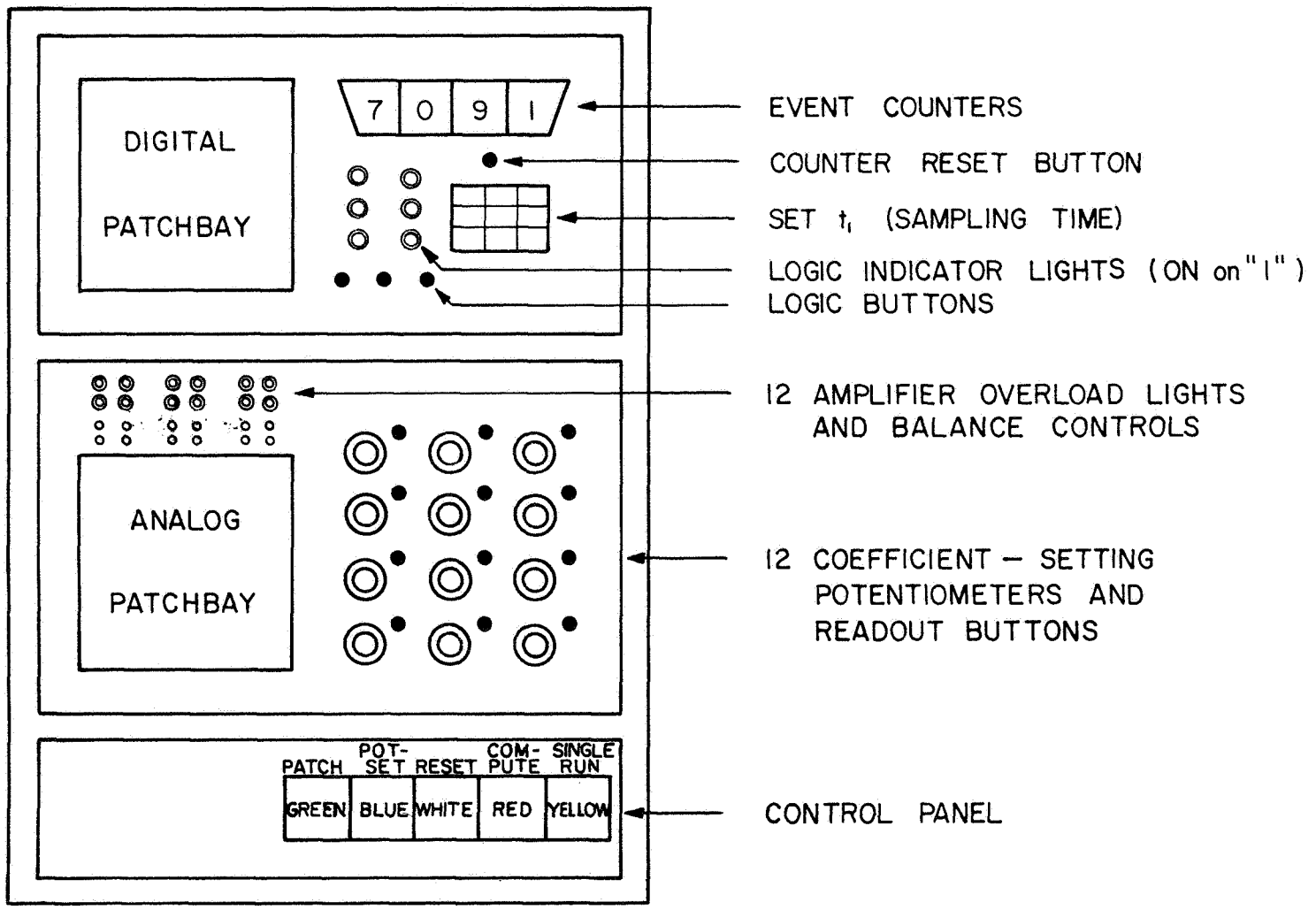


Fig. 2.1 APE II Front Panel

adders (exclusive OR circuits) permit generation of pseudo-random shift register sequences. A sampling-type noise generator provides a clocked digital noise source for Monte Carlo experiments.

These features, when combined with a novel packaging technique, result in a versatile hybrid computer permitting a wide variety of analog and hybrid experiments at minimum cost. A list of suggested APE II experiments is contained in Table 2.1 (Korn, 1967).

2.1 Packaging

The APE II packaging design (Fig. 2.2) has done away with all signal and power-supply wiring to a card cage. The use of small transistor amplifiers and all-integrated circuit logic has made it possible to plug circuit cards directly into the rear of the inexpensive patchbay receivers. Ground planes on one side of the double-sided printed circuit cards (Fig. 2.3) serve as shields between adjacent cards (Korn, 1967).

Each amplifier card holds two $\pm$ 10-V, 20-mA transistor amplifiers with field-effect transistor input stages (Burr-Brown Model 9877), an electronic mode-control switch (Burr-Brown Model 9580), a potset relay, overload indicators and amplifier balance controls. Power-supply and logic inputs are supplied from the patchbay receiver, which furnishes all electrical connections to the cards. Similar cards hold summing resistors and other computing elements.

The same type of construction also accommodates all digital components in a separate patchbay receiver, with the exception of a set of in-line readout counters, and the front-panel pushbutton control logic.

Table 2.1 Suggested APE II Experiments
(Korn, 1967)

Simulation Techniques

1. Bouncing-ball Simulation Using Analog Memory
2. Study of Steepest-descent Optimization
   (a) Steepest-descent Division
   (b) Linear Regression by Steepest Descent
   (c) Simulation of a Simple Optimizing Servo
3. Solution of a Simple Problem in the Calculus of Variations Using Pontryagin's Maximum Principle
4. Solution of Difference Equations and Simulation of Digital-differential-analyzer Integration with Track-hold Circuits
5. Simulation of a Simple Sampled-data Control System
6. Automatic Solution of a Two-point Boundary-value Problem by Iteration
7. Computation of Parameter-influence Coefficients (Solution of Sensitivity Equations)
8. Computation of a Satellite Trajectory of a Simple Perturbation Method
9. A Simple Model-matching Experiment
10. Study of a Maximum-effort Servo

Hybrid-computer Hardware Techniques

1. Study of Fast Diode Circuits and Precision Limiters
2. Study of a Simple Analog-to-digital Converter
3. Accurate Signal Generators and Pulse-width Modulators
4. Study of Track-hold Operation and First-order Hold Circuits
5. Simulation of Combined Analog-digital Computation - Error Compensation

Statistical Measurements and Communication/Detection System Simulation

1. Statistical Measurements
   (a) Measurement of Continuous and Sampled-data
   (b) Measurement (Estimation) of Correlation Functions
   (c) Measurement (Estimation) of Probability and Probability Density
2. Coarse-quantization Measurements; Polarity-coincidence Correlation
3. Monte Carlo Computation of a Definite Integral
4. Measurement of Mean-square Filter Output and Filter Optimization
   (a) Direct Method
   (b) Modified-adjoint-system Method
   (c) Monte Carlo Method
5. Study of Ballistic-trajectory Errors
6. Demonstration of Modulation Waveforms with and without Noise
7. Simulation of a Superheterodyne Receiver

Table 2.1 (Continued)

8. Simulation of an FM Communication System
9. Simulation of a Phase-lock Loop
10. Simulation of Matched-filter Detection Using Pseudo-random Signals (Shift-register Sequences)

A low-cost MAC PANEL 440 point patchbay receiver having the necessary low-leakage (diallylpthallate) base and gold-plated spring construction was used for both digital and analog patchbays. Direct plug-in connections to the rear of each patchbay are implemented with special screw-machine fabricated, gold-plated taper pins terminated into plugs of standard 0.080 in. test-probe diameter (Fig. 2.4). These plugs mate with inexpensive test-point jacks mounted on the circuit cards. Gold-plated MAC PANEL shorting strips interconnecting patchbay points are inserted and held by the taper pins. All wiring from power supplies, coefficient potentiometers, and between digital and analog patchbays is soldered directly to the taper pins.

2.2 The Analog Module

One of the two amplifiers on each amplifier card can be patched as an electronically switched integrator or track-hold circuit as well as a summing amplifier (Fig. 2.5). Integrating capacitances of 5 μF, 0.5 μF, 0.05 μF and 0.005 μF are employed together with summing resistors of 200 kΩ and 20 kΩ to permit both real-time and repetitive analog computation. A reed-relay, which shorts amplifier output and summing junction under logic control, serves as a POTSET relay and for starting certain iterative procedures. The lower amplifier on each card is

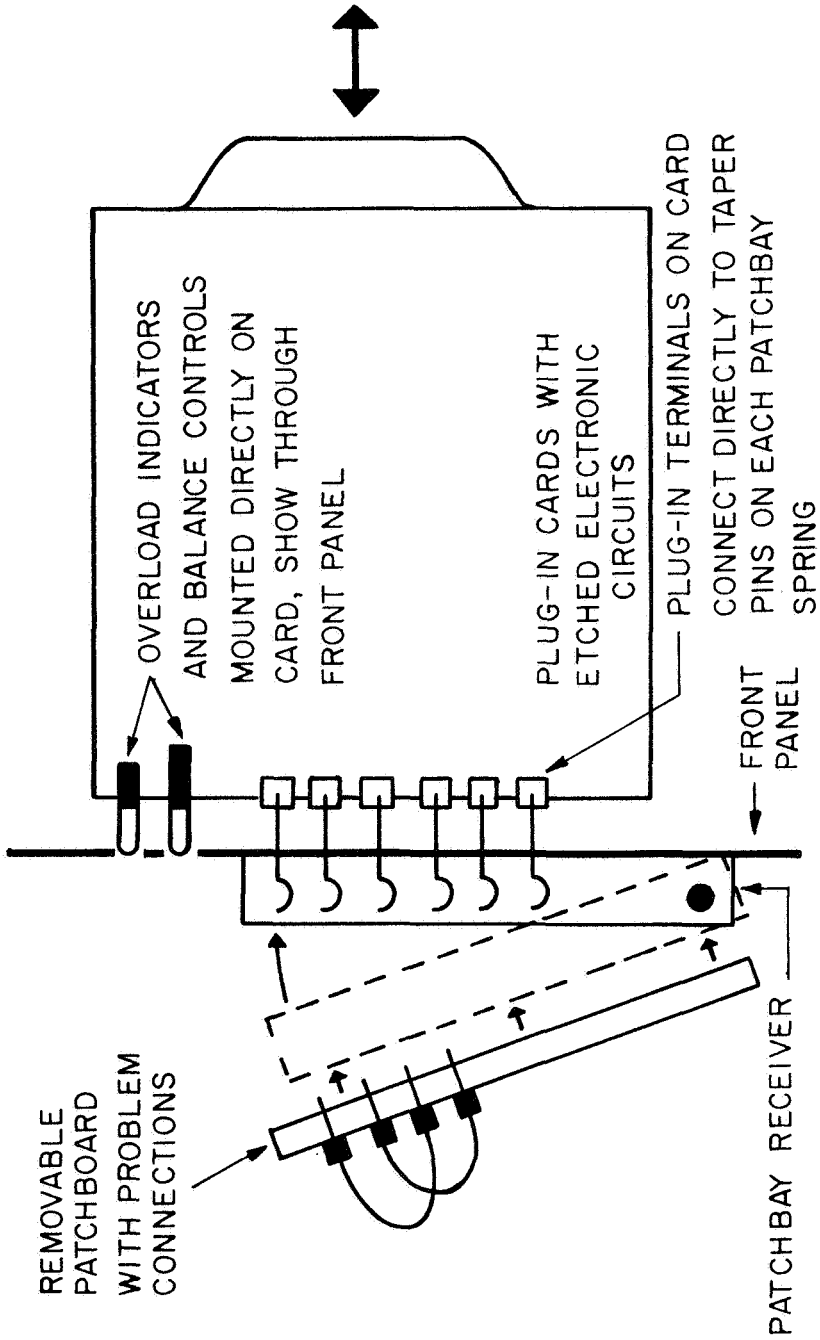


Fig. 2.2 APE II Packaging System

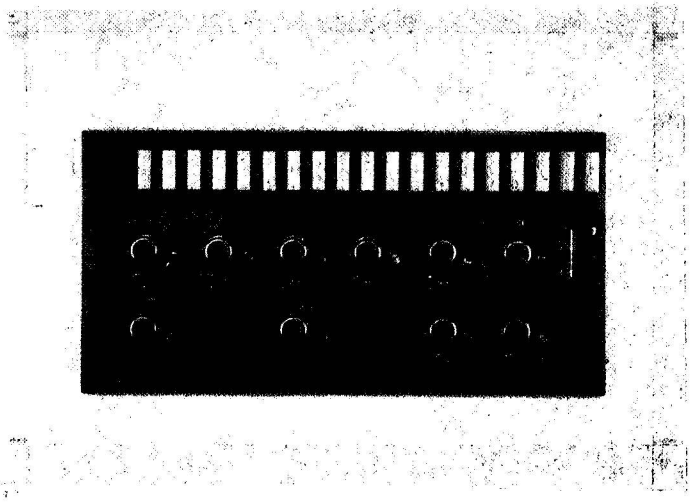
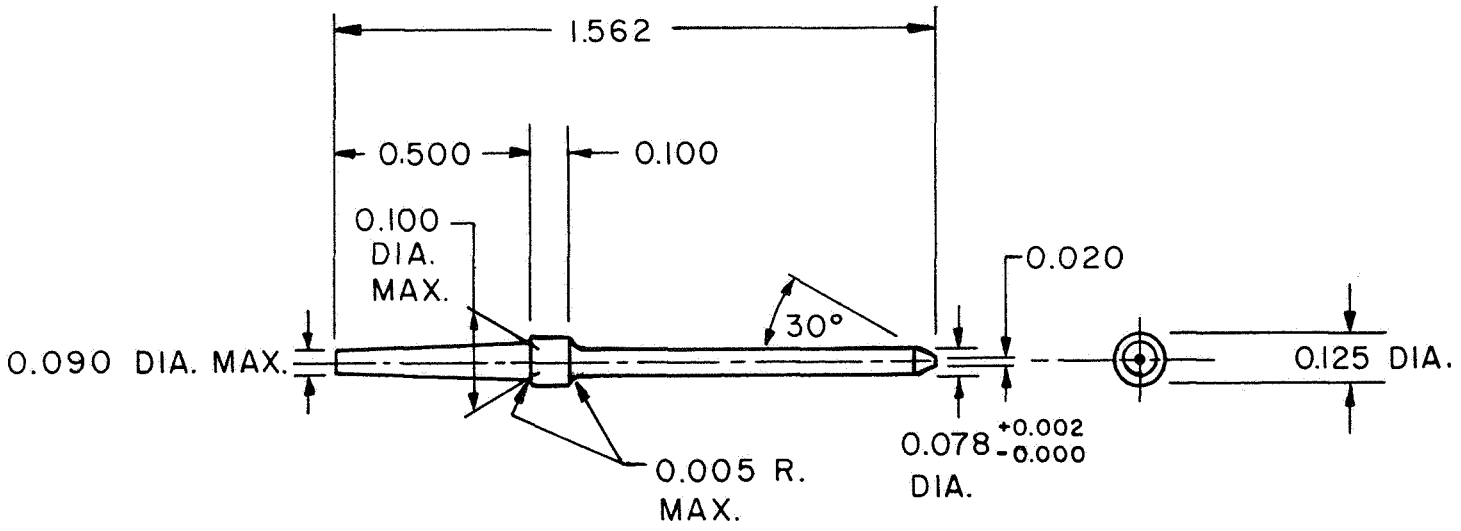


Fig. 2.3 Ground planes on one side of double-sided printed circuit boards serve as a shield between cards.



MATERIAL: 0.125 DIA.
HARD BRASS

FINISH: 0.00003 HARD GOLD
OVER 0.0001 NICKEL

SCALE: 2 : 1

Fig. 2.4 Specially fabricated taper pins permit direct plug-in connections to the rear of the patchbay.

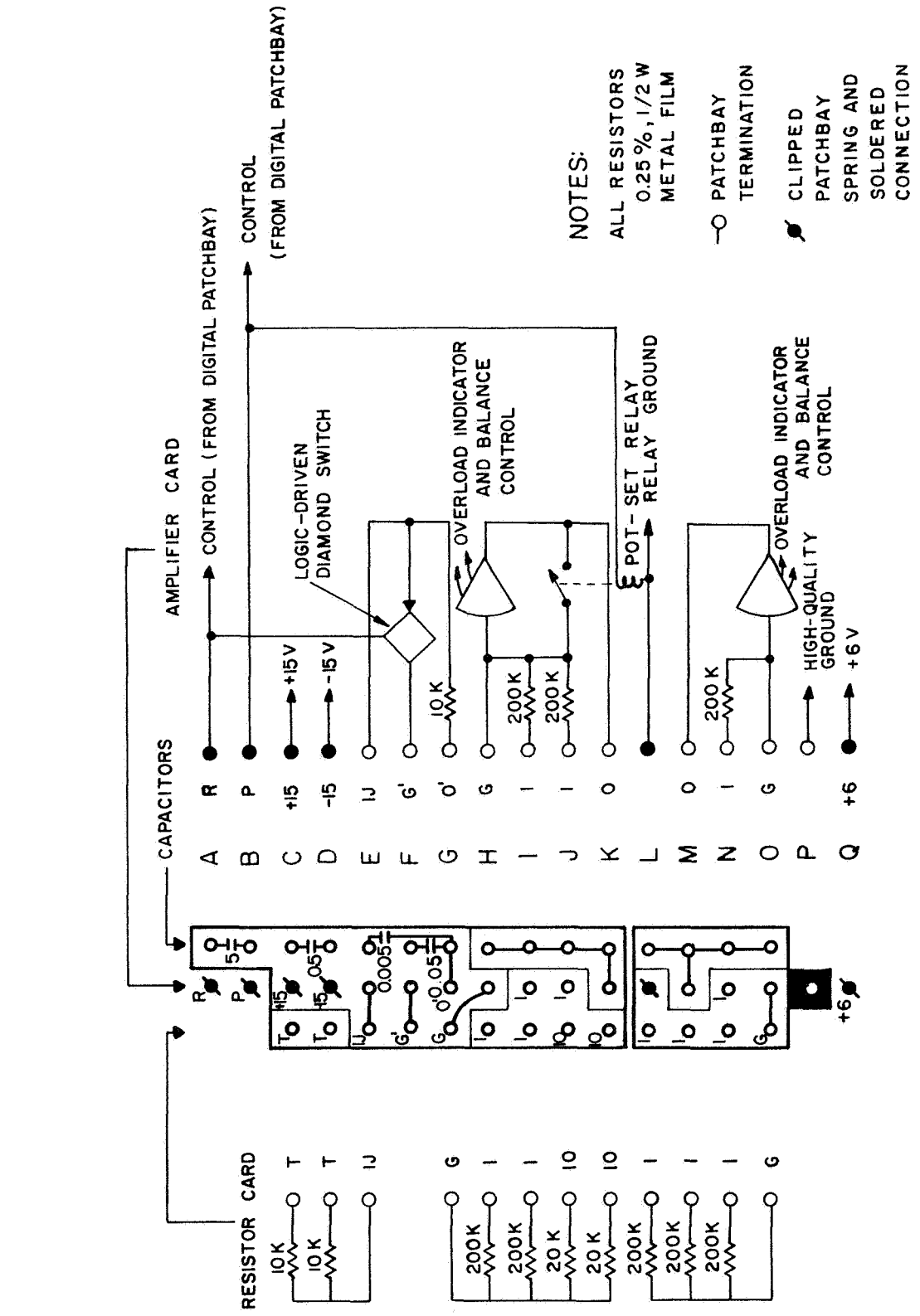


Fig. 2.5 APE II Switched-Integrator/Summer Module

intended to serve as a simple summing amplifier with only gain-of-one inputs.

The analog module also contains wide-band quarter-square multipliers, diode bridges, analog comparators (with outputs on the digital patchbay), zener-diode limiters, free diodes, and twelve 5 kΩ coefficient potentiometers.

2.3 The Digital Module

The digital module consists of the following cards:

1. Front-panel pushbutton-logic card.
2. Master clock card which provides all computer reset, sampling and timing pulses.
3. Five free-logic cards, each containing a J-K type flip-flop and two three-input OR/NOR gates.
4. Four shift register cards, each with five stages and special reset/set logic, which can be patched for pattern generation, memory, and pseudo-random shift-register sequences.
5. A card containing 4 modulo-2 adders (exclusive OR's) used for pseudo-random sequences, digital correlation and digital comparison, and a sampling-type binary noise generator.
6. A counter card with 4 free decade counters intended for additional program timing and statistical experiments.
7. A 4-decade readout counter with in-line display for counting events.

Other digital module features include 3 front-panel pushbutton-switch outputs for manually setting or resetting flip-flops and counters,

6 logic-state lamp inputs for visual determination of the state of any digital logic output, and digital outputs of 2 analog comparators (inputs on the analog patchbay).

The digital-logic cards, designed and constructed at The University of Arizona, are made with 1/16 in., two-sided, 1 oz., copper-clad, glass-epoxy printed-circuit board. To reduce cost, connections from one side of the PC board to the other are made with small wire. The component side of the board is mostly ground plane to reduce radiation and interference.

Motorola MECL integrated-circuit current-mode logic is employed throughout the digital module. The low-level logic swings (0.8V) and the balanced current-mode operation, producing negligible power-supply-line transients during switching times, combine with ground-plane shielding and L-C decoupling of the power supply leads of each card to reduce the digital noise coupled to the analog module. This is a critical factor in view of the wideband analog-computer amplifiers (0 dB at 20 MHz) used in the APE II system.

2.4 Digital Control of Analog Computer Operations

Figure 2.6 illustrates the design of the APE II control unit, which is a simplified and improved version of that used in The University of Arizona's ASTRAC II. A 100 kHz crystal-controlled clock and counter chain provides timing pulses (100 kHz, 50 kHz, 25 kHz and 10 kHz) which are always available on the patchbay for various control and display purposes. The desired computer repetition rate (100, 50, 25, or 10 runs per second) is obtained by patching to the above timing pulses. All

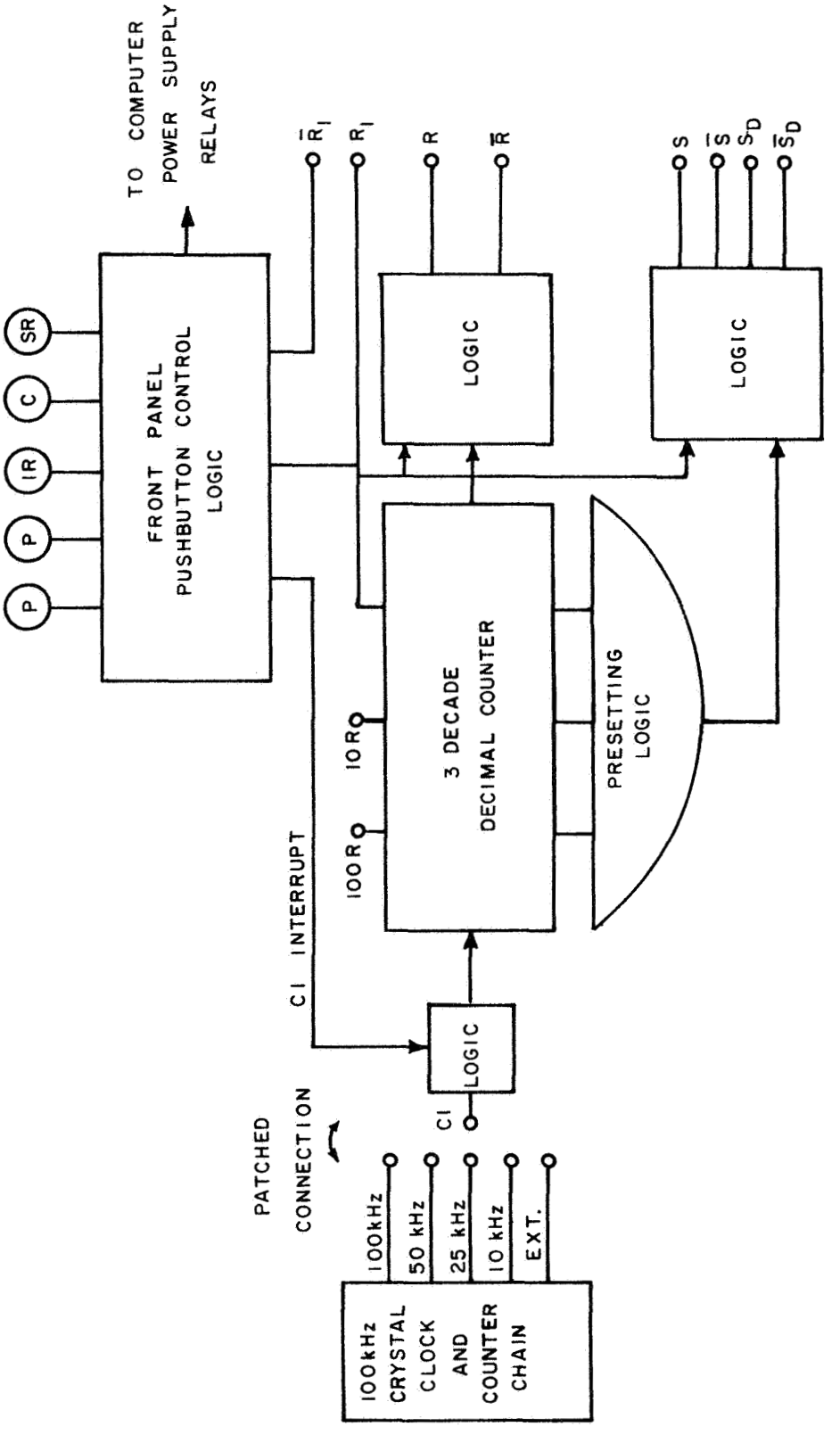


Fig. 2.6 Block Diagram of APE II Control Unit

other timing is performed in terms of these "C1" pulses (1000 per computer run), so that the time scale of all counting and timing operations changes automatically with the repetition rate $f_R = 1/T_R$.

The master timing counter C_1 is a three-decade decimal counter with a preset output designed to perform the following timing functions:

1. Counts down by 1000 to mark the start of periodic COMPUTE periods.
2. Produces timing markers at 10 and 100 times the computer repetition rate f_R (e.g., for oscilloscope displays).
3. Produces sampling pulses S (set by convenient rocker-type thumbwheel decimal switches in steps of $T_R/1000$) at $t = T_1$ seconds after the start of each COMPUTE period (Fig. 2.7).

In normal repetitive operation (Fig. 2.7), R is "1" (logical one, not voltage) at t (computer time) = 0 and "0" at $t = 0.9\ T_R$ to produce periodic reset pulses R, so that COMPUTE periods of length $T = 0.9\ T_R$ alternate with RESET periods of length $T_S = T_R/10$. The preset output at T_1 feeds a flip-flop timing-logic block to produce periodic sampling pulses S and delayed sampling pulses S_D of length T_S. Note that R, S and S_D (and hence also their complements) are clocked by C1 in order to eliminate timing errors and coincidence-gate output spikes due to ripple-through delays in C_1.

The front-panel controls are PATCH, POTSET, INITIAL RESET, COMPUTE and SINGLE RUN. The master clock is controlled by a pushbutton-logic card (see state diagram Fig. 2.8). In addition, the COMPUTE button puts the computer into INITIAL RESET when depressed and into

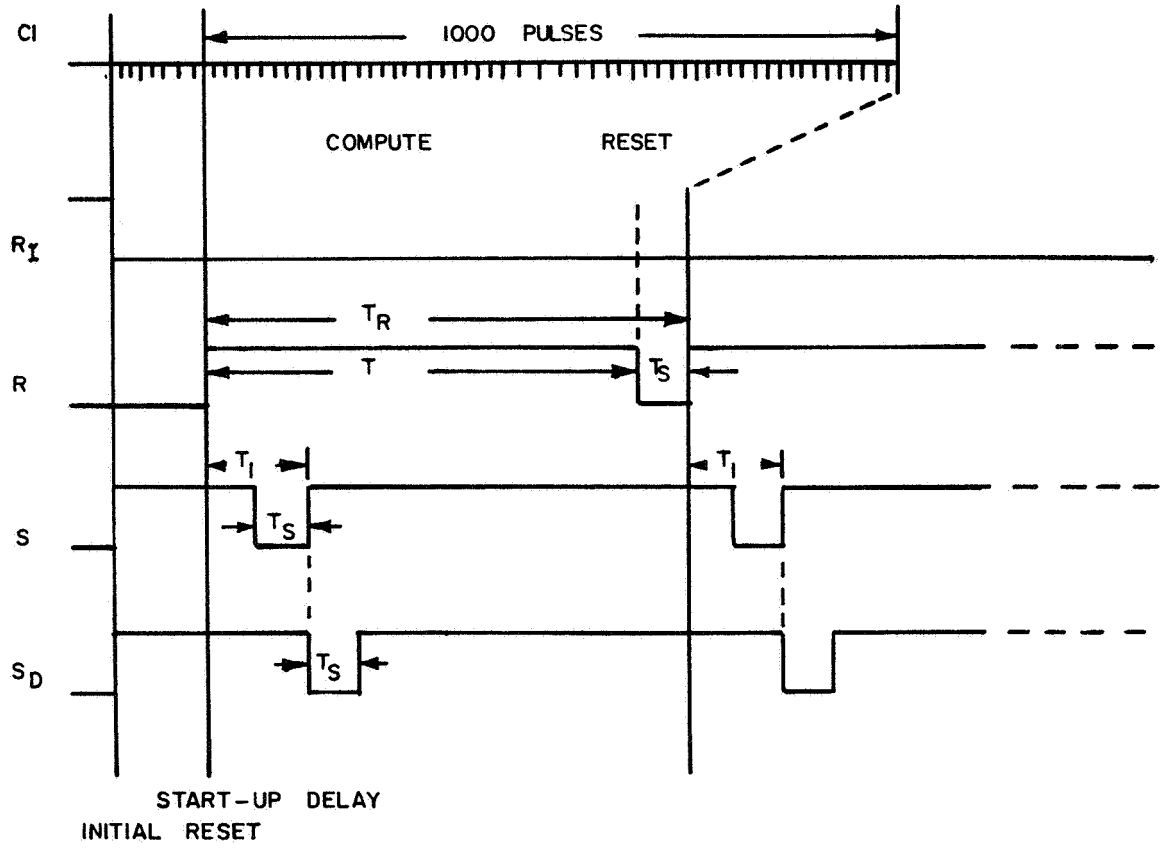


Fig. 2.7 APE II Timing Diagram

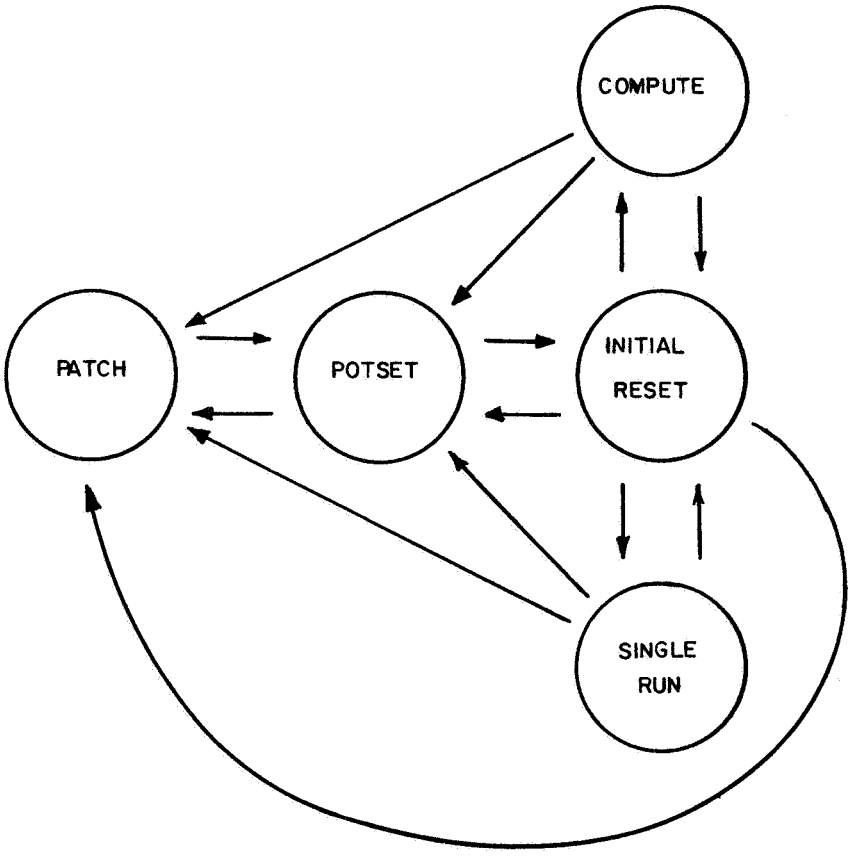


Fig. 2.8 Pushbutton Control State-diagram

COMPUTE when released. The pushbutton-logic card provides an INITIAL RESET pulse R_I and POTSET pulse P, available on the digital patchbay, a Cl-interrupt pulse which gates the Cl pulses into C_1 and other pulses to front panel pushbutton indicator lights, amplifier, reference and potset-relay power supplies.

2.5 Operating Conditions

When the computer is turned on, a special RC delay circuit places the machine into the PATCH mode. In this mode:

1. Amplifier and reference power is OFF.
2. Counter C_1 is reset to zero.
3. R, S, and S_D are "0" (RESET/TRACK).
4. INITIAL RESET R_I and POTSET P are "1".

From PATCH, one goes to POTSET, where the following conditions are established:

1. Amplifier power is ON, but reference power is still removed from the patchbay.
2. Counter C_1 is reset to zero.
3. R, S, and S_D are "0" (RESET/TRACK)
4. R_I and P are "1".
5. The digital voltmeter (DVM) is connected to the potentiometer readout bus.
6. Amplifier overload lights are reset.

Before one begins to compute, one depresses the INITIAL RESET button to produce the following conditions:

1. Amplifier and reference power is ON.
2. Counter C_1 is reset to zero.
3. R, S, and S_D are "0" (RESET/TRACK).
4. R_I is "1", P is "0".
5. DVM is connected to an analog-patchbay point.

All integrators and track-holds and digital logic are now reset to suitable initial conditions, ready for computation. This state is maintained until one depresses and releases the COMPUTE button. Then R_I goes to "0", S and S_D go to "1", and a delay of 10 ms (to allow any special relay circuits to operate), due to a one-shot multivibrator on the push-button-logic card, runs out. Then the Cl-interrupt pulse gates Cl pulses into counter C_1 which counts 101 pulses before starting the first COMPUTE period. The periodic reset pulses R and sampling pulses S and S_D will then continue on, as illustrated in Fig. 2.7. For single-run operation, one must begin in INITIAL RESET (going from COMPUTE to SINGLE RUN is prevented by the logic design) and depress the SINGLE RUN button. At the end of one run, only the Cl pulses are interrupted, and the computer stands ready for another single run obtained by depressing the SINGLE RUN button again; this permits one to check the progress of iterative routines computer run by computer run.

In normal repetitive operation, the integrators are controlled by R, and selected track-hold circuits can be controlled by S. Track-hold pairs are controlled by R and S, or by S and S_D by digital readout of solution values x(t) at an accurately present computer sampling time $t = T_1$.

Different patching connections can employ R, S and S_D for flexible memory control, including three-period control (Eckes and Korn, 1964).

2.6 Free Logic

The free-logic circuits, namely J-K type flip-flops, OR/NOR gates, modulo-2 adders and decade counters, are of straightforward design and need no detailed description. The APE II shift-registers have some extra features, which are worth explanation.

Each shift-register card contains five stages, with each stage conveniently patchable to the following stage by a single connection; this is made possible by an extra input gate for each stage (Fig. 2.9). A one-shot multivibrator (using a MECL R-S flip-flop) provides a delayed set pulse, 100 ns wide, immediately after a reset pulse (usually R_I), patched to the common reset line, goes to "0". Each stage patched to this delayed set pulse is, thus, ready for computation. This scheme is especially useful in setting up the shift register for pseudo-noise sequences. The one-shot circuit can also be used by itself as a source of delayed pulses.

Four decimal in-line readout counters have their individual input, reset lines, and outputs available on the digital patchbay. In addition, a RESET button common to all four counters is provided on the front panel near the display unit. Each counter has a forbidden-code gate to prevent the simultaneous appearance of two numbers when the computer is turned on, or when some interference accidentally triggers the counter into an unwanted state.

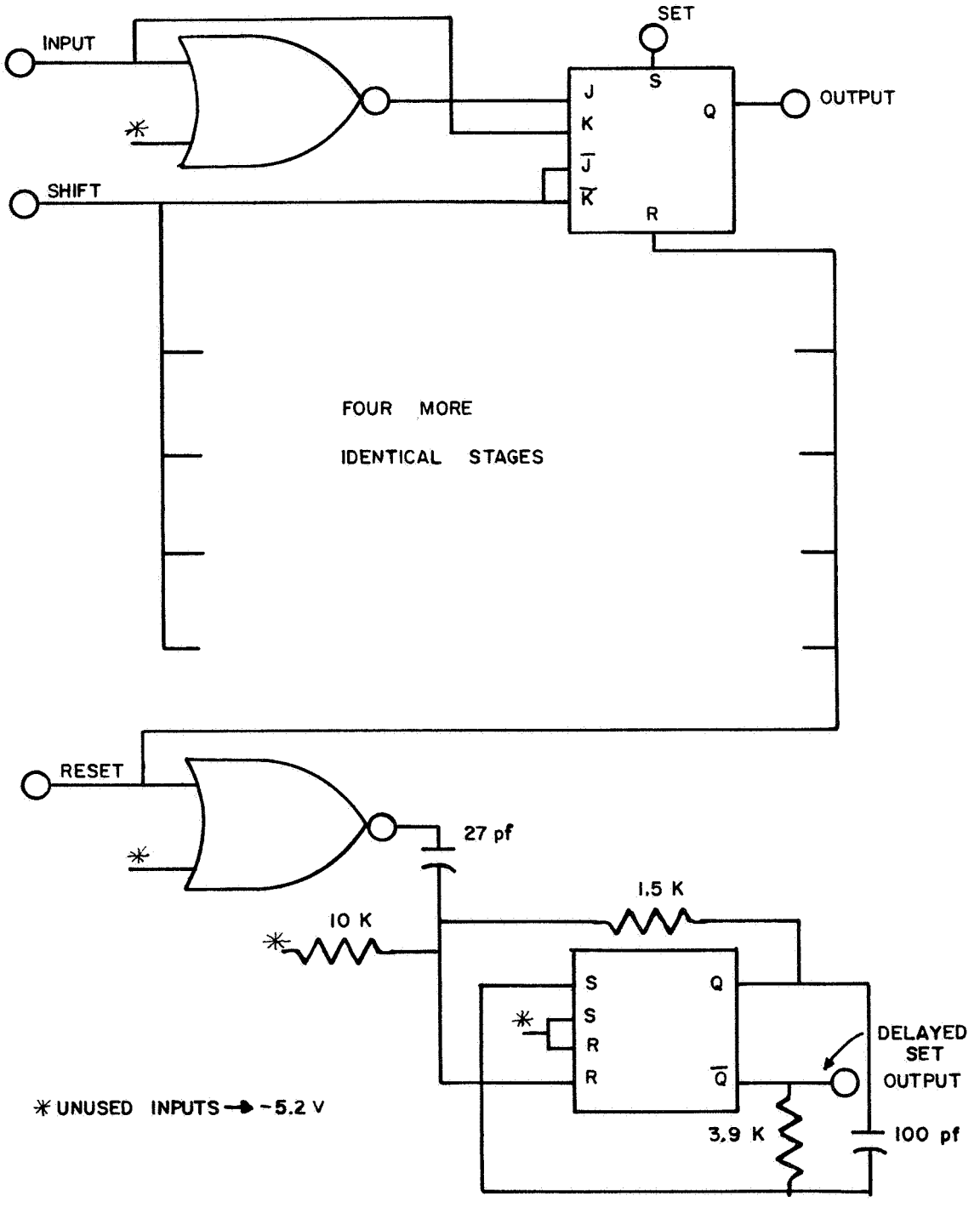


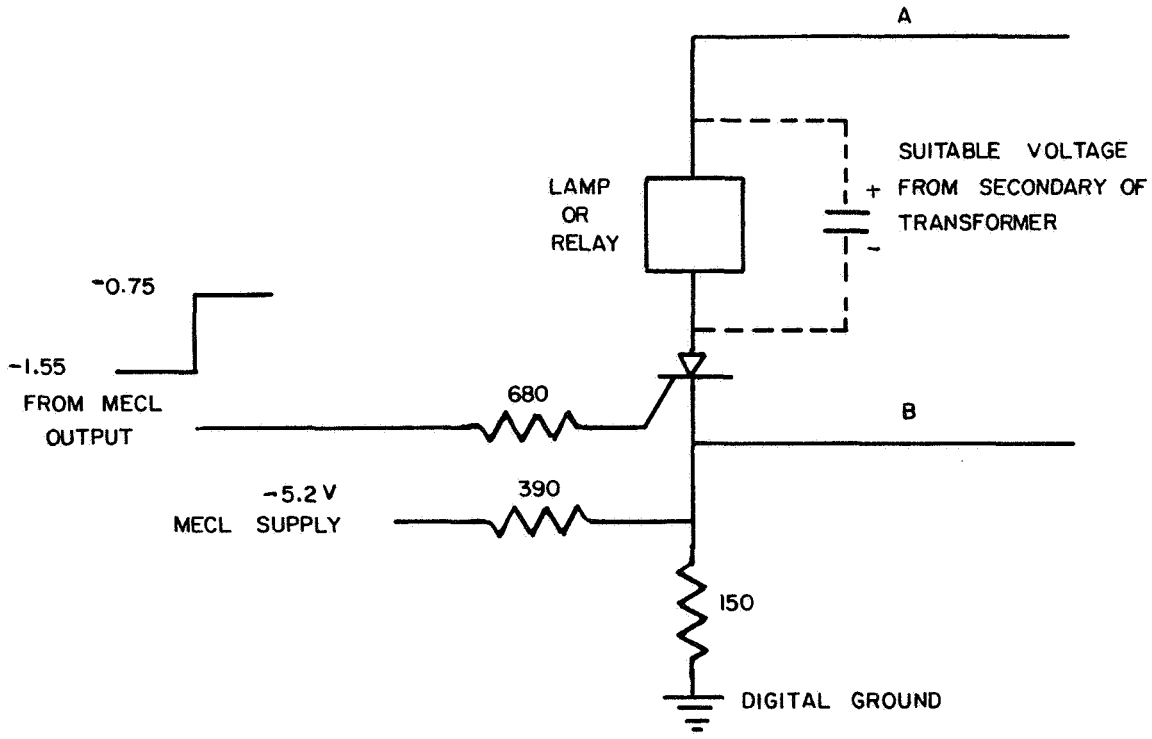
Fig. 2.9 APE II Shift Register Card Schematic

Incandescent lamps in the counter readout display unit (I.E.E., Inc., Series 20), control-panel pushbutton lamps, relays (paralleled by a filter capacitor) and logic-state lamps, are driven by a novel inexpensive driver circuit employing a silicon controlled-rectifier (SCR) actuated directly by MECL logic levels (Fig. 2.10).

2.7 Discussion

The new APE II system provides a small flexible differential analyzer intended for laboratory instruction in analog and hybrid computation. Total parts cost is estimated to be $4,500. Two APE II systems have been in use by students one semester and have worked out quite well. The results of an experiment using APE II are detailed in Chapter 7.

Experience with APE II has demonstrated that the packaging techniques and the use of low-level current-mode logic to be very worthwhile. This provided experience and more confidence for the design of LOCUST.



NOTE: TRANSFORMER SECONDARY WINDING IS APPROXIMATELY AT -1.45 VOLTS WITH RESPECT TO GROUND.
SEVERAL CIRCUITS MAY BE CONNECTED TO THE SAME TRANSFORMER AT A AND B.
FILTER CAPACITOR IS USED WITH RELAY ONLY.

Fig. 2.10 Indicator Lamp and Relay Driver Circuit

Chapter 3

THE LOCUST SYSTEM

The feasibility of really fast hybrid computation was demonstrated by the development and application of The University of Arizona's ASTRAC II (Eckes, 1967). But, as noted earlier, no machine commercially available to date has the required mode-control switching speed and low-impedance computing networks; and most computers do not have the required amplifier bandwidth. The development of the LOCUST system represents an attempt to design a truly producible very fast hybrid computer at moderate cost.

The LOCUST system is an all solid-state iterative-differential-analyzer making maximum use of integrated circuits (Fig. 3.1). The machine comprises 34 free amplifiers of which 16 can be used as integrator/track-hold circuits, plus 18 amplifiers permanently committed to 6 high-speed multiplier/dividers, and 4 comparators (56 amplifiers total). It is capable of computation at iteration rates up to 2 kHz; linear-component errors are within 0.2 percent up to 10 kHz. Special "slow" summing networks also permit operation as a slow analog computer. The following design features are of special interest:

1. Maximum use of both linear and digital monolithic integrated circuits enhances computer performance and still reduces parts and assembly costs.

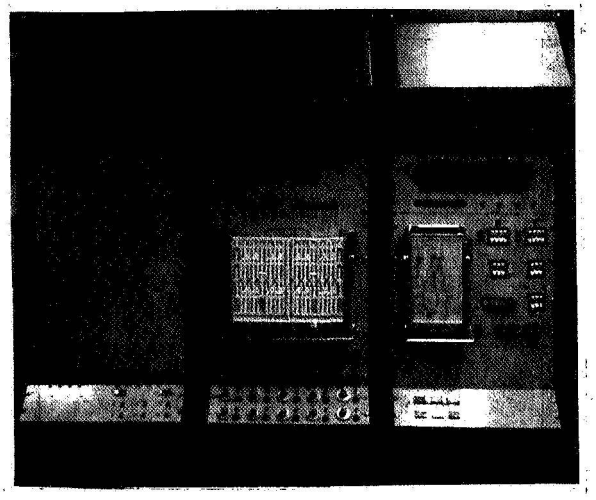


Fig. 3.1 The LOCUST System

2. New mounting and shielding techniques, including a technique for shielding low cost unshielded patchbays, were developed.
3. Low-level current-mode digital logic modules have essentially eliminated digital noise in the analog portion of the computer.
4. New solid-state devices have substantially improved amplifier and mode-control switch performance.
5. Free digital logic has been made more convenient as a result of ASTRAC II experience; and the LOCUST digital-computer linkage is designed as an integral part of the logic-control system.
6. New patchpanel design affords exceptional convenience for setup and logic control.

The LOCUST system equipment complement is listed in Table 3.1.

3.1 High-speed Computing Requirements

To appreciate the technical problems associated with fast computation, consider the following requirements:

1. To obtain a dynamic error (phase-shift error) of 0.1 percent of half scale at 10 kHz in an ordinary phase inverting amplifier, the amplifier gain-bandwidth product must be greater than 10 MHz.
2. To prevent dynamic errors due to distributed capacitances, computing resistances (summing resistors in summing amplifiers and integrators) should be low, less than 10 kΩ. Such low impedances require high-current amplifier output stages.
3. The voltage rate of change of a 20-volt peak-to-peak 10 kHz sine wave is $2\pi \times 10^5$ volts per second. To insure a track-hold

Table 3.1 LOCUST System Equipment Complement

Analog Elements

16	Integrator/Track-hold Summing Circuits
4	Summing amplifiers
8	2-input summing amplifiers
6	Phase inverters
6	Quarter-square multipliers
4	General-purpose diode function generators
4	Sine generators
40	Coefficient potentiometers
4	Diode bridges

Digital Elements

12	MECL J-K type flip-flops
12	3-input OR/NOR gates
6	4-input OR/NOR gates
5	6-stage shift registers with a one-shot multivibrator reset circuit and a modulo-2 adder (exclusive-OR) circuit
6	Decade counters with in-line readout
12	Logic-state lights
1	Digital control module

Hybrid Elements

4	Comparators
4	D/A multipliers (to be added later)
4	A/D converters
4	D/A level changers (noise drivers)
6	D/A electronic switches
4	D/A relay switches

Auxiliary Elements

1	Electronic Digital Voltmeter
1	Oscilloscope
1	Power supply balance indicator and control panel

sampling accuracy of 0.1 percent, mode-control and track-hold timing must be within 15 nanoseconds.

When such high-speed computing elements are placed in a hybrid computer system, other considerations become important:

1. Added stray capacitance due to wiring and patchbay system can reduce computing bandwidth.
2. Crosstalk between computing elements through patchbay capacitances and through the analog power supply can reduce accuracy.
3. Wideband analog elements pick up switching noise from mode-control switches and from the digital control module.

In the LOCUST system all analog computing elements are housed in aluminum cans and plugged directly into the rear of a modified low-cost patchbay system. Analog amplifier and all mode-control switch power supply lines are decoupled with a CLC pi-network filter in each amplifier and switch module.

Digital noise is minimized through the use of Motorola Emitter Coupled Logic (MECL). The low-level logic swing (0.8V) along with the balanced-current nature of the non-saturating current-mode logic serve to reduce radiation and, more importantly, computer ground-system disturbances.

Good computer-system design requires that all ground returns terminate at one point in order to eliminate ground loops which pick up signals and thus cause ground system noise. The LOCUST analog patchbay serves as the common ground point for the system.

3.2 LOCUST Integrator/Track-hold Module

The heart of an iterative differential analyzer is an amplifier/electronic-switch combination, the integrator/track-hold circuit. The LOCUST integrator/track-hold circuit block diagram is illustrated in Fig. 3.2. A single high-speed electronic switch, which is controlled by signals from the digital control module, suffices for each integrator, and the same switched-integrator circuit is used for both integration and track-hold (sample-hold, zero-order hold) operation. A complete description of the circuit and its operation is included in Chapter 4.

The feedback capacitors (0.01, 0.1 and 1.0 μF) for integration and track-hold operation, and one feedback resistor (10 kΩ) for summing amplifier or switched-amplifier operation are selected by relays driven by digital logic from the digital patchbay. A "slow" summing network is connected, when the 1.0 and the 0.1 μF capacitors are used, to permit real-time integration.

3.3 LOCUST Analog Patchbay System

Analog computing elements whose input and output voltages may contain frequency components as high as 10 to 20 kHz make it mandatory to use shielded patchbay systems with shielded patchcords in spite of their added shunt capacitances. Shielded patchbay systems are also needed to reduce leakage when computing-elements impedances are high, say, greater than 100 kΩ. Low-impedance levels of 1 kΩ to 10 kΩ used

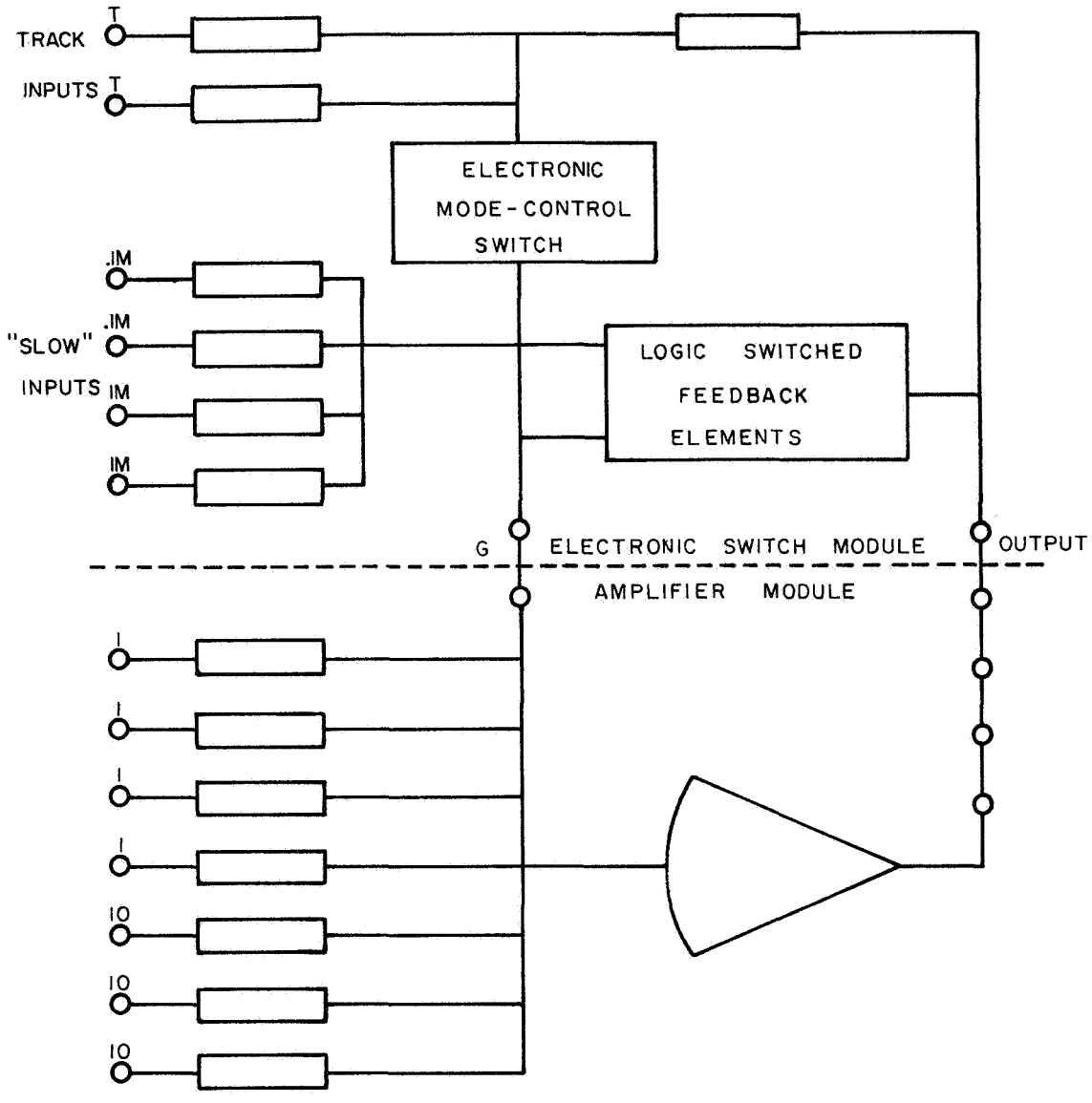


Fig. 3.2 Block Diagram of LOCUST Integrator/Track-hold Module

in LOCUST are low enough that surface leakage is a minor problem. Nevertheless, a low-leakage material, such as diallylpthallate, must be used for the patchbay receiver.

Crosstalk between patchbay terminations can be a major problem in high-speed analog computers. Capacitive coupling between patchbay receiver springs and patchcord-tip combinations cause undesirable coupling between the connected and unconnected inputs of a particular amplifier, and between the output of an amplifier and the inputs of the amplifier located next to it. The capacitance of unshielded patching systems may be as high as 5 to 10 pF between holes, which can cause an error of from 0.3 to 0.6 percent at 10 kHz if the summing resistors are 10 kΩ (Fig. 3.3).

The price of totally shielded patchbay systems is considerable, $2,000 to $4,000 for a system with enough holes (1,000 to 2,000) for a small-to-medium size analog computer. An unshielded patchbay system of the same size costs only about $350 to $500.

The LOCUST analog patchbay system represents a compromise in terms of crosstalk, leakage and cost. It comprises a low-cost MAC Panel 1,600 hole unshielded patchbay receiver having the necessary diallylpthallate base for low leakage, and gold-plated springs for low contact resistance and corrosion protection.

Suitable rows and columns of patchbay receiver springs are connected to the computer system-ground using gold-plated shorting strips held in by taper pins to provide shielding between analog

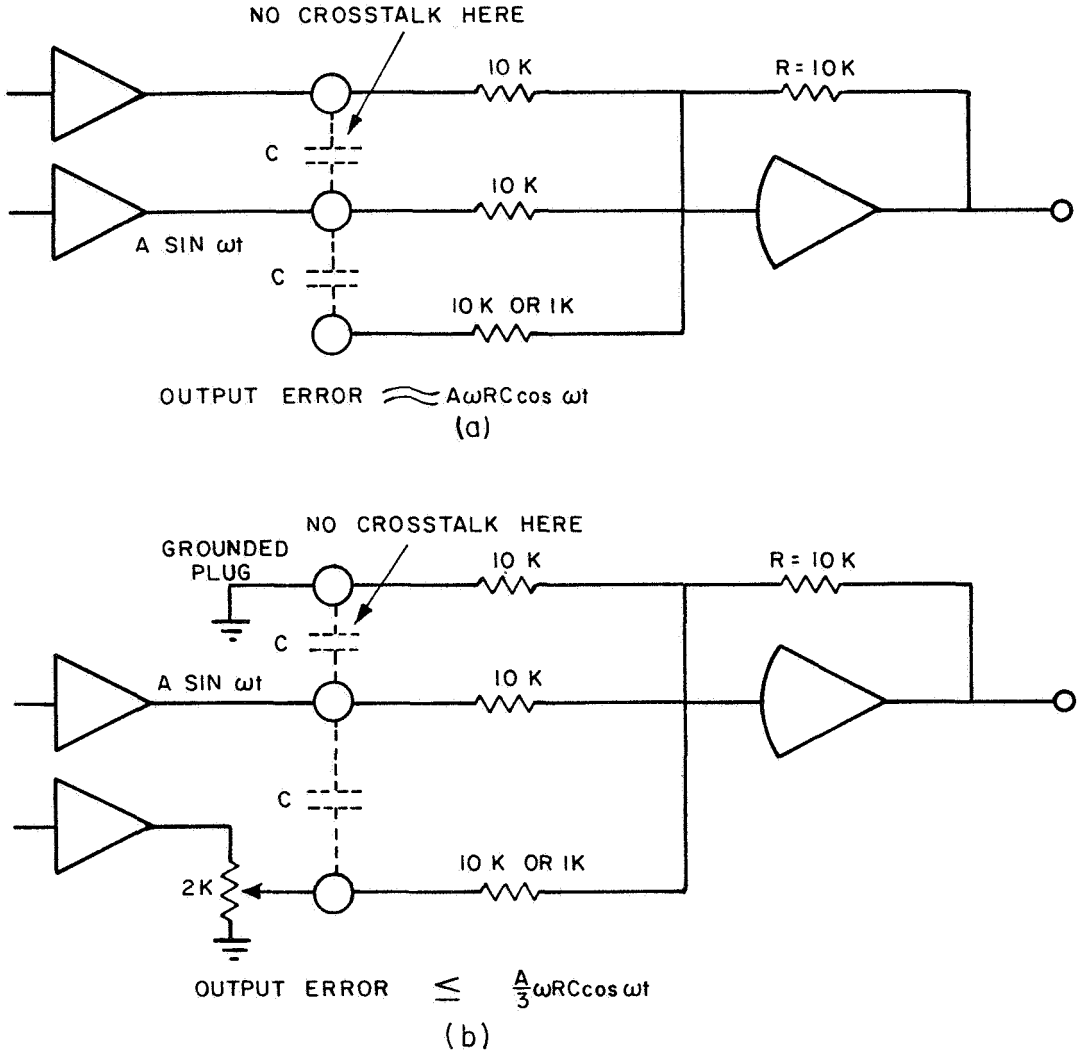


Fig. 3.3 Patchbay capacitances between inputs cause gain errors.

(a) Open inputs contribute ARC ω cos ωt volts error (0.3% for $\omega = 2\pi\ 10^4$, $R = 10^4$, $C = 5 \times 10^{-12}$). (b) Grounded gain-of-one input eliminates crosstalk to that input at the expense of open-loop gain; grounded gain-of-ten inputs would seriously affect amplifier performance. Potentiometer connection reduces error to at most one-third that of an open input.

computing elements (Fig. 3.4). This "wastes" about 400 holes. About 500 other patchbay terminations are used for all power-supply and logic-control wiring for the analog computing elements so that the latter has no other connections whatsoever.

An analog module covers a field as shown in Fig. 3.5. Inputs and outputs are separated as much as possible by locating power supply and control connections in the center column. These low-impedance terminations supply additional shielding between analog terminations.

Amplifiers, mode-control switches, multipliers, D/A switches, phase inverters etc., are housed in aluminum cans plugged directly into the rear of the analog patchbay (Fig. 3.6). These direct plug-in connections are implemented with special screw-machine-fabricated gold-plated taper pins terminated into plugs of standard 0.080 in. test-probe diameter. These are a shortened version of those used in APE II (Fig. 2.4). These plugs mate with standard press-fit test-probe jacks on the computing element cans. The cans are held at the rear by simple frames with swing-out bars which permit easy removal for maintenance.

All power supply, digital control, potentiometer, and reference-supply wiring is soldered directly to the patchbay-receiver solder-cup taper pins or to the special taper-pin plugs. As noted earlier, the computing elements do not require rear connectors.

All aluminum patchboards, fabricated at The University of Arizona's Electrical Engineering Shop, replace the plastic patchboards usually provided with unshielded patchbays. The finished aluminum

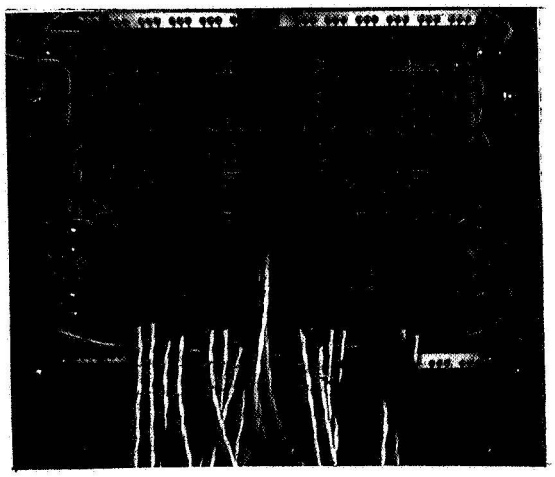


Fig. 3.4 Rows and columns of terminations provide shielding between modules. Power-supply and logic-control wiring is made directly to the patchbay receiver.

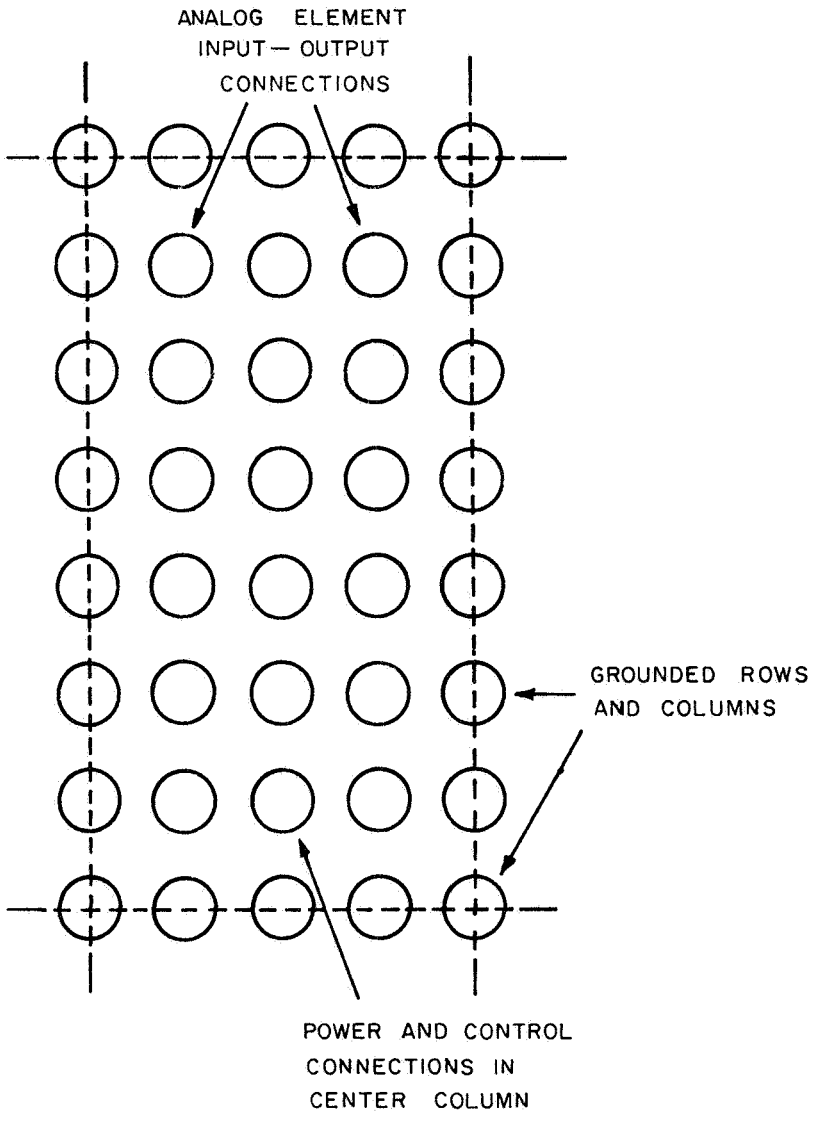
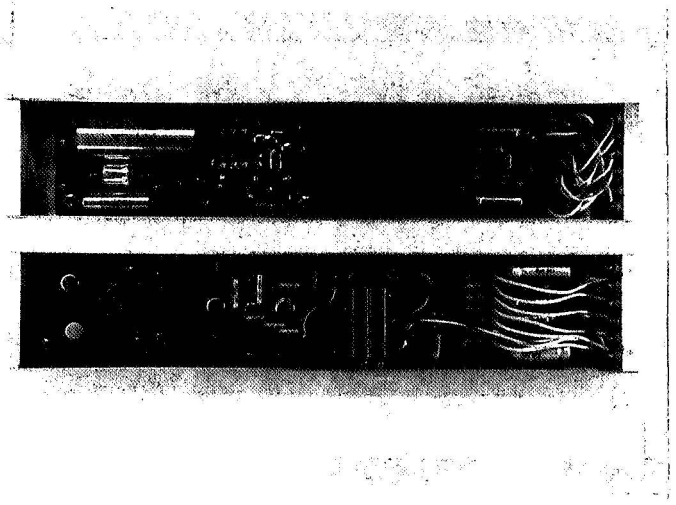
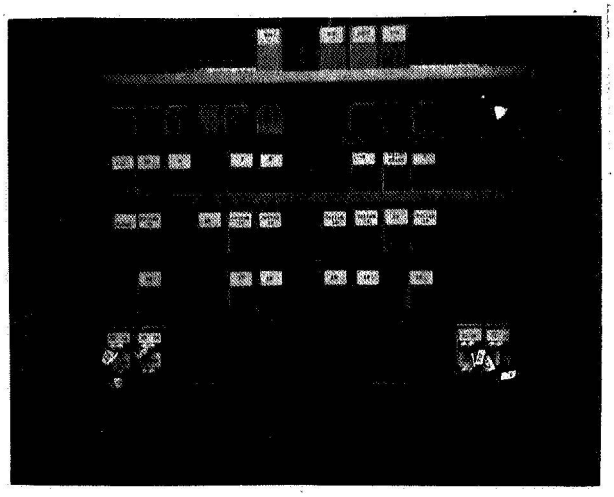


Fig. 3.5 LOCUST Analog Module Patchbay Field



(a)



(b)

Fig. 3.6 (a) Analog elements are housed in aluminum cans and (b) plugged directly into the rear of the patchbay receiver and held by simple frames.

patchboards, which are drilled for standard commercially available Electronic Associates or Virginia Panel shielded patchcords, have patch holes only for the patchbay terminations actually used (Fig. 3.7).

These patchbay-system construction techniques yield a good measure of shielding against crosstalk at relatively low cost. Crosstalk error between amplifiers was measured and found to be less than 0.01 percent for all computing frequencies. This indicates the effectiveness of the inexpensive shielded patchbay system and of the power supply filters in each analog module. Capacitance between adjacent patchbay terminations has been reduced by one-half to about 3pF. Capacitance between adjacent patchcords has been eliminated by using shielded patchcords. Leakage currents through the removable patchboard portion of the system have been eliminated. The total cost has been reduced to one-third to one-half that of a commercial shielded-patchbay system.

3.4 Analog-patchpanel Layout

The layout design of a patchpanel is a human-engineering task as well as an electrical and mechanical design task (Fig. 3.7).

The patching of an integrator/track-hold circuit is convenient because there are no bottle plugs required to implement a switched integrator; scale changing and mode control are more conveniently patched on the digital patchpanel. Inputs of computing elements are located on the left of a patchfield and outputs on the right.

The technique of bringing power supply and control lines directly to the patchbay receiver puts additional constraints on layout,

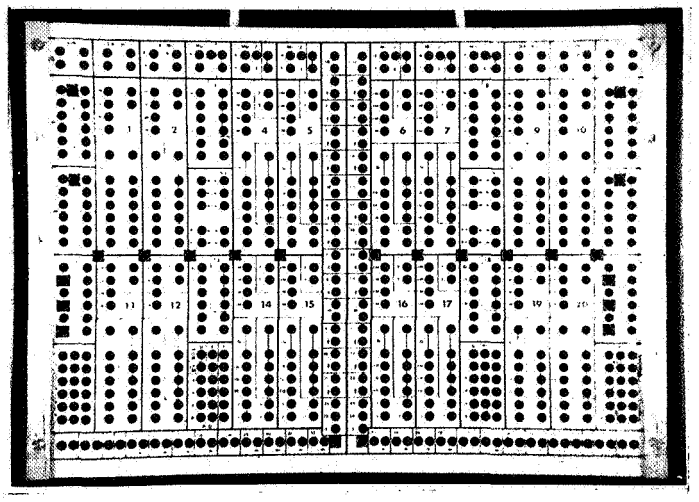


Fig. 3.7 All aluminum patchboards are drilled only for the terminations used and silkscreened and color-coded for identification.

since it could, conceivably, increase the problem of leakage currents from power supply lines causing undesirable voltage offsets at computing element outputs. On the other hand, as mentioned earlier, these low impedance lines in the center column provide added electrostatic shielding between analog inputs and outputs.

Because patchboards have patching holes only for patchbay terminations actually used for patching, they have a relatively wider hole spacing which permits more patching room and presents a much more uncluttered appearance than the original unshielded patchboards.

The patchpanel contains, in addition to patchfields for integrator/track-hold computing elements, patch fields for summing amplifiers, comparators, phase inverters, multipliers, sin-generators, D/A multipliers, and D/A switches. Additional patch fields provide connections to interface equipment linking LOCUST to a PDP-9 digital computer and to readout trunk-lines. A number of patching setups are described in the LOCUST instruction manual (Appendix).

Since the analog module cans cover the entire patching field associated with each particular element, coefficient-setting potentiometers and 10-volt reference points are located around the edge of the patchpanel.

The patchboards are silkscreened white with black letters and symbols. Inputs, outputs and potentiometers are color-coded with transparent ink for identification.

3.5 Costs

New packaging techniques, the modified patchbay system and the use of integrated circuits have reduced parts and assembly costs of LOCUST to one-half that of ASTRAC II at no sacrifice in performance. The most striking savings were made in the digital section, $3,000, one-third of ASTRAC II digital-module cost, and the analog patchbay system, about $1,000, one-half of ASTRAC II patchbay system cost. Total parts cost for the system is about $13,000.

Chapter 4

LOCUST ANALOG COMPUTING ELEMENTS

To exploit the possibilities of fast iterative computation, wide-band analog computing elements are mandatory. Gain and phase shift of operational amplifiers must be controlled well beyond the actual working frequency range in order to maintain stability and to insure the specified accuracy in operational-amplifier feedback circuits. Impedance levels in analog computing elements are quite low (10 kΩ or less) to reduce the effects of stray capacitance. Low impedances, in turn, require more current, and so the LOCUST amplifiers are designed to supply 30 mA. The switching times of electronic mode-control switches, D/A switches, and the comparison delay of analog comparators are designed to be as short as possible.

The resulting design problems are extremely difficult and, for some computing elements, they have never been wholly satisfactorily solved. The Analog/Hybrid Computer Laboratory at The University of Arizona has pioneered in the design of high-speed computing elements, beginning as early as 1961 with ASTRAC I, a 100-volt vacuum tube machine. Significant improvements in speed and timing resulted from the ASTRAC II project, a 10-volt all-solid-state machine. The LOCUST project is an attempt to further refine the design and to exceed the specifications of the ASTRAC II system by utilizing new packaging techniques, new solid state devices, and substantial improvements in the circuit design.

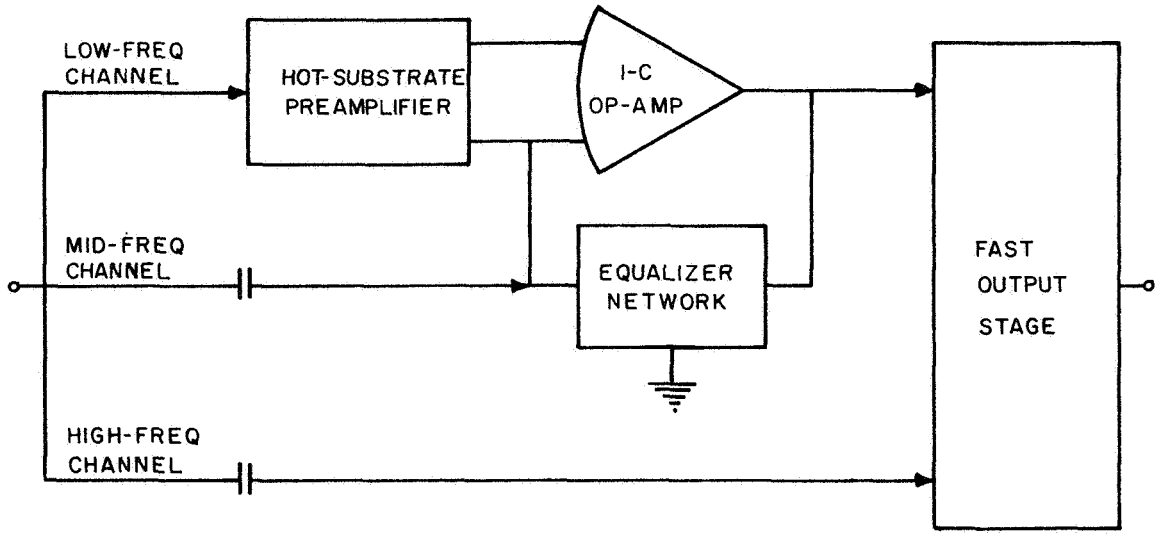
4.1 The LOCUST Operational Amplifiers

The LOCUST iterative differential analyzer satisfies the first two requirements of Section 3.1 with the aid of a new high-performance amplifier developed at The University of Arizona as an M.S. thesis project (Naylor, 1967); the reference describes its design in great detail. The performance of the new amplifier is summarized in Table 4.1.

The block diagram of Fig. 4.1(a) illustrates the basic amplifier design, which employs a three-channel feed-forward circuit. Beginning from the amplifier input, the channels are: the high-frequency channel directly to the wide-band class AB output stage, the intermediate-frequency channel through a Motorola MC1433 integrated-circuit operational amplifier, and the low-frequency channel through a Fairchild μA726C hot-substrate preamplifier.

The bandwidth and output-current limitations of the MC1433 integrated-circuit amplifier are overcome by cascading it with a high-current output stage and by feeding forward the high frequency signals directly to the output stage from the summing junction. Because of the low-offset, low-drift properties of a new integrated-circuit hot-substrate differential amplifier, a chopper stabilizer channel is unnecessary.

Figure 4.1(b) illustrates the frequency response of each channel and their combination. Dotted lines show the roll-off of a more conventional 6 dB/octave feed-forward amplifier; the "zero" needed at 40 kHz lowers the gain at 10 kHz. An improvement in the open-loop gain of only



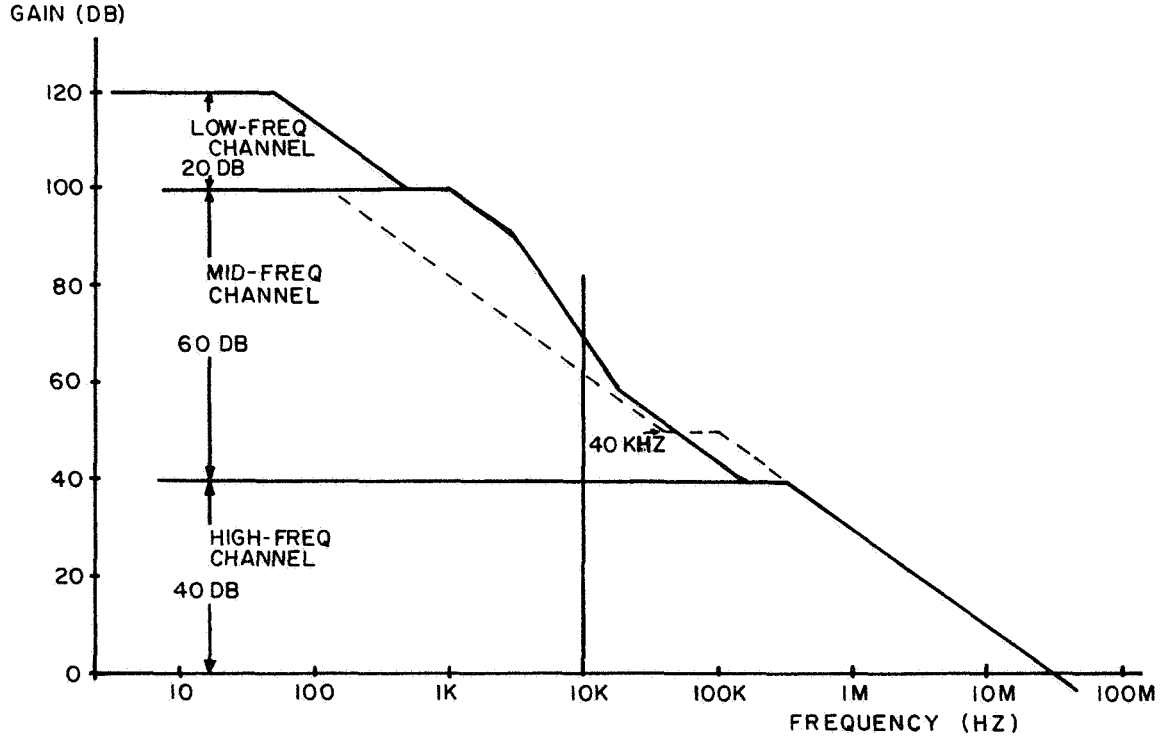


Fig. 4.1 (a) Block diagram showing signal flow through the three channels. (b) Open-loop Bode plot of the three channels and their combination.

Table 4.1 LOCUST d-c Amplifier Performance

Typical Performance at 25°C		Unit
Open-loop Gain	120	dB
Unity Gain Bandwidth	30	MHz
Rated Output		
Voltage	±10	V
Current	±30	mA
Max. Freq. (resistive load)	5.0	MHz
Input Offset		
Voltage	Adj. to zero	mV
Current	Adj. to zero	nA
Input Offset Drift		
Voltage	±2.5	μV/°C
Bias Current	±50	pA/°C
Input Noise	15	μVrms
Open-loop Output Impedance		
at 100 Hz	100	Ω
at 10 kHz	50	Ω
Unity-gain Inverter (no load)		
Freq. Response -3 dB	10	MHz
Error at 10 kHz	0.1	%
Capacitive Load without Instability	0.001	μF
Quiescent Current	20	mA

6 dB at 10 kHz will decrease the dynamic error of a phase inverter operating at 10 kHz by a factor of two.

Figure 4.2 is a complete schematic diagram of the new amplifier.

The unity-gain phase-inverter performance of the amplifier is illustrated in Figs. 4.3 and 4.4. These data were obtained with the amplifiers installed in the computer with various amplifier loads. The

Fig. 4.2 Circuit Diagram of the Computer d-c Amplifier

(a) The wideband class AB output stage has low open-loop output impedance, full ± 10-V, 30-mA output to 5 MHz, and provides two convenient input points for the summation of the signals from the high-frequency channel and the intermediate-frequency amplifier.

(b) The intermediate-frequency integrated-circuit amplifier accurately controls the gain and frequency response of the intermediate-frequency signals by feedback through the three-terminal equalizer network.

(c) The hot-substrate differential preamplifier provides low-offset/low-drift amplification of low frequencies down to d-c.

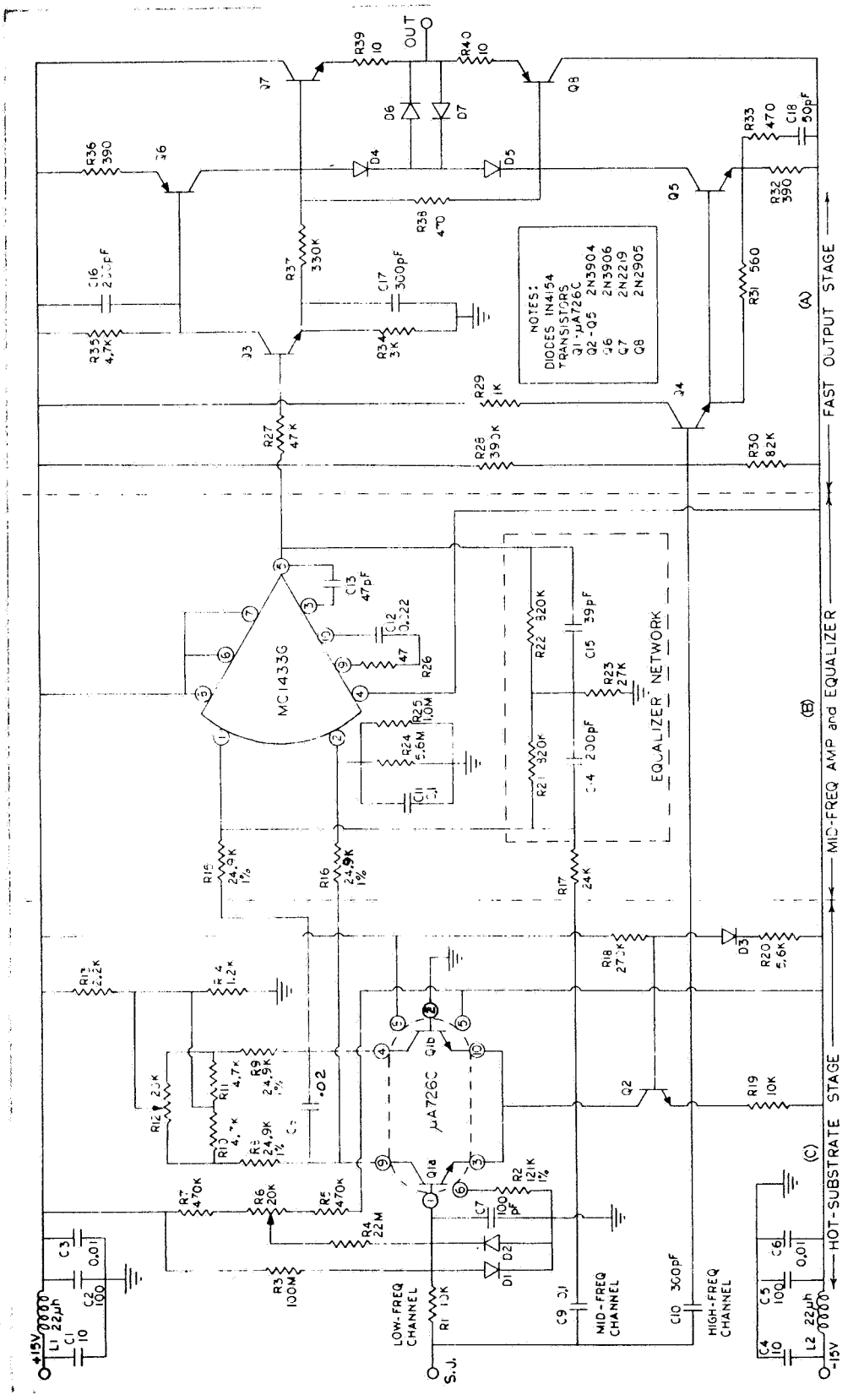
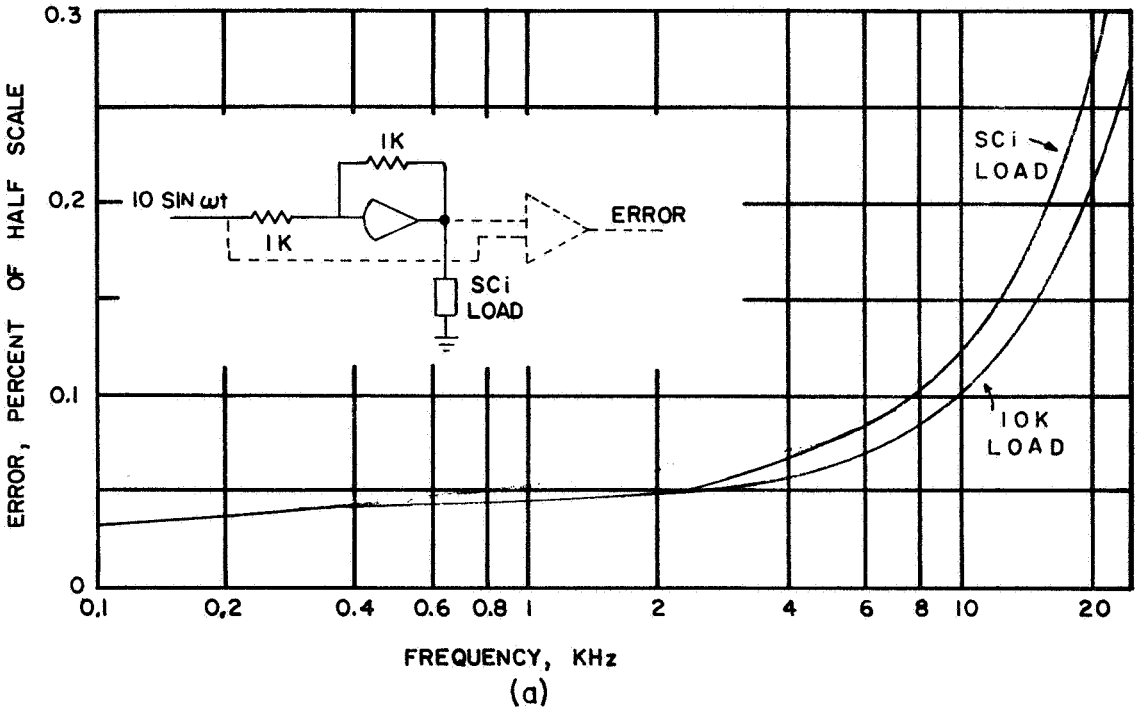


Fig. 4.2 Circuit Diagram of the Computer d-c Amplifier



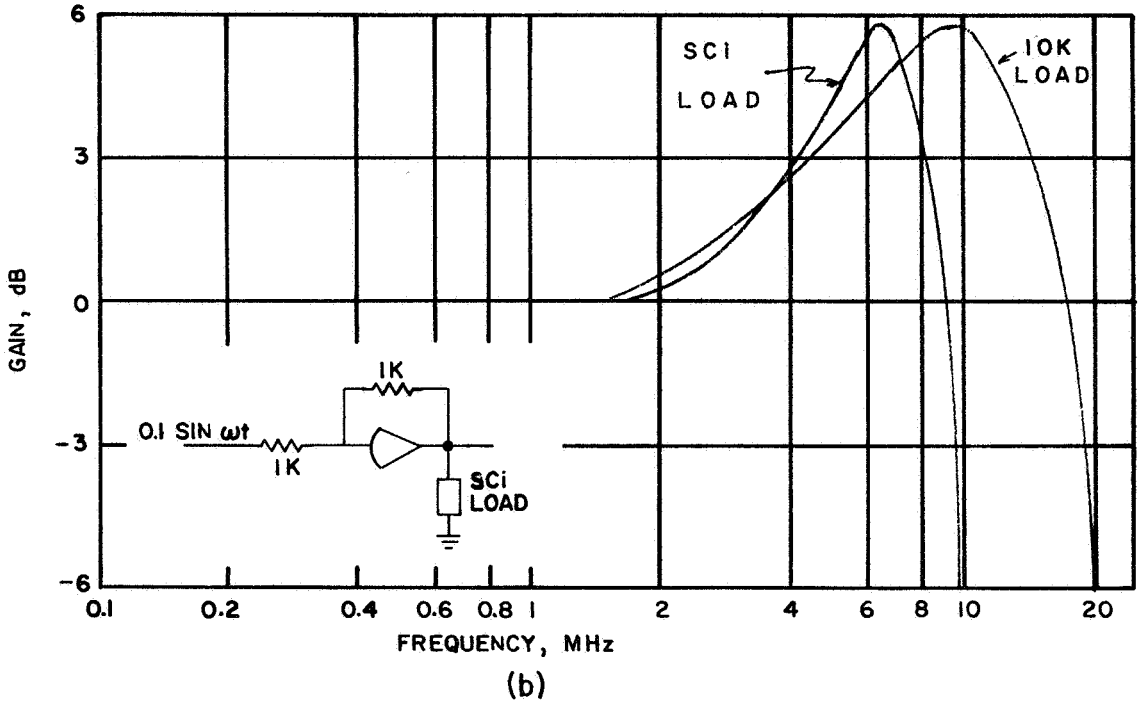


Fig. 4.3 (a) Unity-gain Phase-inverter Response (1 kΩ input and feedback resistors) (b) Small-signal Frequency Response

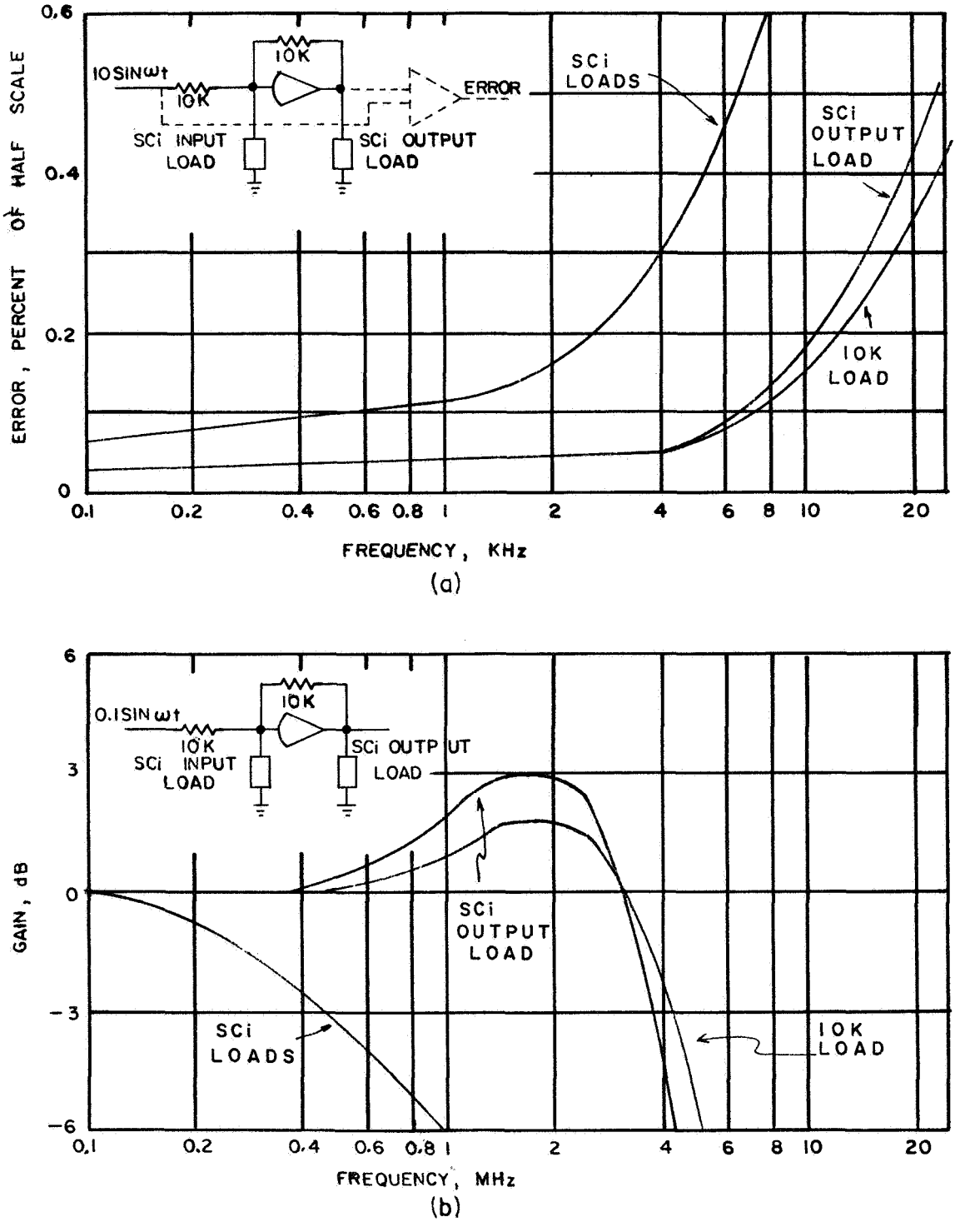


Fig. 4.4 (a) Unity-gain Phase-inverter Response (10 kΩ input and feedback resistors) (b) Small-signal Frequency Response

SCi (Simulation Councils, Inc.) standard input load (Simulation, 1963) consists of two gain-of-ten inputs grounded with the test signal applied to a gain-of-one input. The SCi output load is that presented to the computing element under test by three computing potentiometers with the LO terminals grounded and each ARM set at 0.500 and connected to a gain-of-one input. This load includes at least 300 pF of stray capacitance to ground.

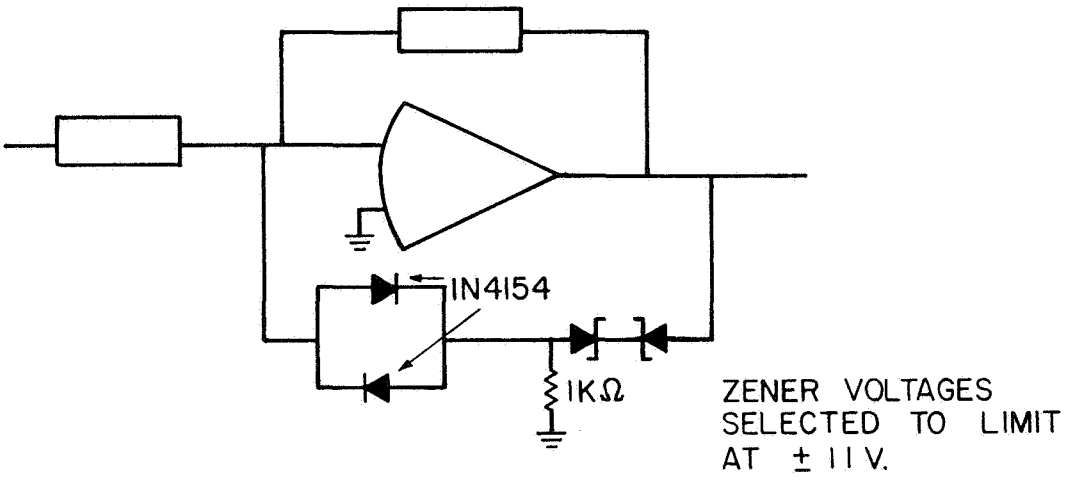
A limiter circuit [Fig. 4.5(a)] is included in the LOCUST amplifier to insure quick recovery from overload, prevent the summing junction from leaving virtual ground when an overload occurs, and thus completely eliminate the need for amplifier POTSET relays. The combination of resistor R and the parallel diodes reduces the effect of the capacitance of the zener diodes.

The amplifier has a novel silicon-controlled rectifier overload-indicator circuit [Fig. 4.5(b)]. Positive or negative voltage levels which exceed the threshold level of the SCR will fire the SCR and thus light the overload lamp. The lamp stays lit until the SCR is reset by the front-panel pushbutton logic. A logic output on the digital patchpanel goes to "1" when an overload occurs.

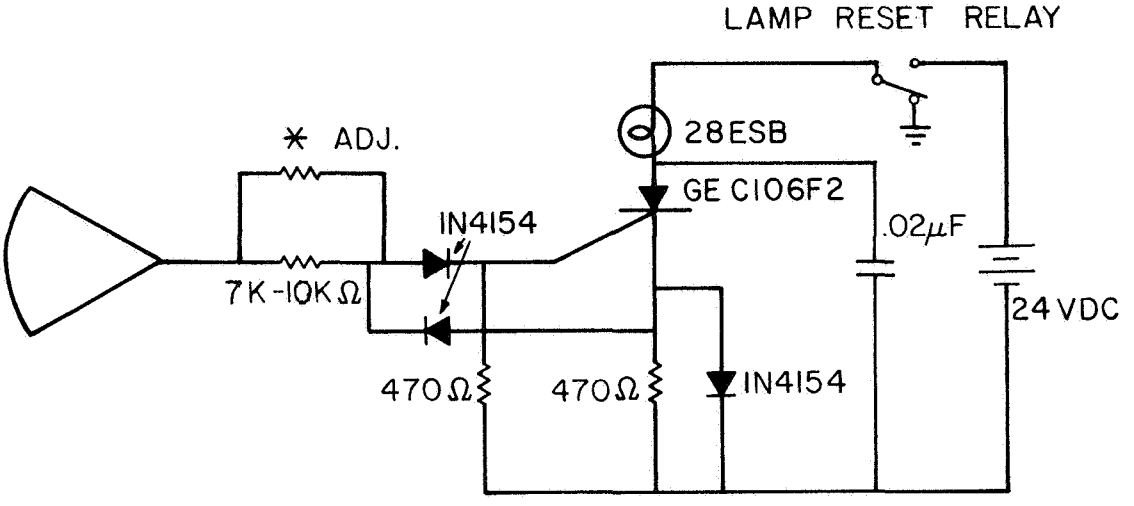
The entire amplifier is intended for easy assembly on a printed-circuit board with a minimum of adjustments; this is a necessary requirement for The University of Arizona's Analog/Hybrid Computer Laboratory, which utilizes student technicians for the assembly and testing of the completed amplifiers.

4.2 Integrator/Track-hold Circuit

The LOCUST integrator/track-hold module comprises the LOCUST amplifier described in Sec. 4.1 and the Burr-Brown Model 9944, a special



(a) HIGH-SPEED LIMITER CIRCUIT



(b) LOCUST OVERLOAD INDICATOR CIRCUIT

Fig. 4.5 (a) LOCUST High-speed Limiter Circuit and (b) New LOCUST Overload-indicator Circuit

purpose electronic switch module designed especially for the LOCUST system (Fig. 4.6). The Model 9944 consists of a Model 4010 high-speed (nonsaturating) electronic switch circuit, suggested by G. A. Korn (Korn, 1966c) and designed by J. Naylor, having a FET input stage for low current drift (Fig. 4.7), integrating capacitors (0.01, 0.1 and 1.0 μF), a high-impedance summing network for "slow" (real-time) simulation, relays with MECL input-level drivers for time-scale changing relays, and track-hold summing and feedback resistors. The important specifications of the integrator/track-hold combination are summarized in Table 4.2.

Figure 4.8 illustrates the operating modes of the integrator/track-hold circuit. In HOLD or COMPUTE [Fig. 4.8(b)], the switch is effectively out of the circuit when the integrator inputs are not used, or integrates the voltages on the integrator inputs.

In TRACK or RESET [Fig. 4.8(c)], the track inputs are connected and the integrator inputs are shorted out by the internal impedance Z_s of the switch. Z_s must be small compared to the parallel combination of integrator inputs so that signals at the integrator inputs essentially do not appear at the output. If <u>one</u> integrator input of 10 volts is to contribute less than 10 mV error in RESET, one must have

$$\frac{Z_s}{R'} < \alpha\ 10^{-3}\left(1 + \frac{R_o}{Z_1}\right)^{-1}$$

where α is the voltage gain of the switch and Z_1 is the parallel combination of R_1 and R_2 [Fig. 4.8(c)]. In LOCUST the smallest computing resistance is 1 kΩ. Therefore,

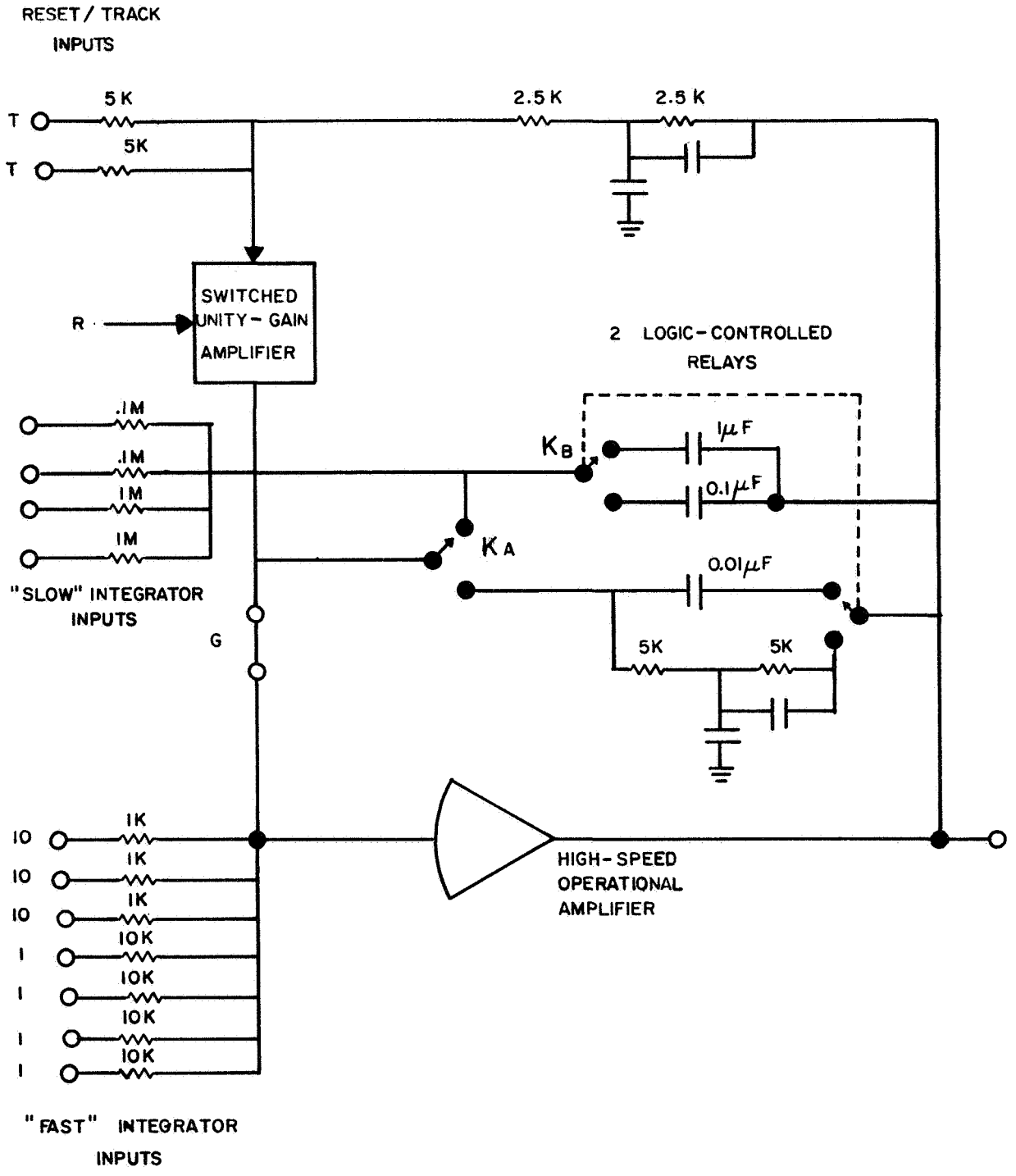


Fig. 4.6 LOCUST Integrator/Track-hold Circuit Schematic Diagram

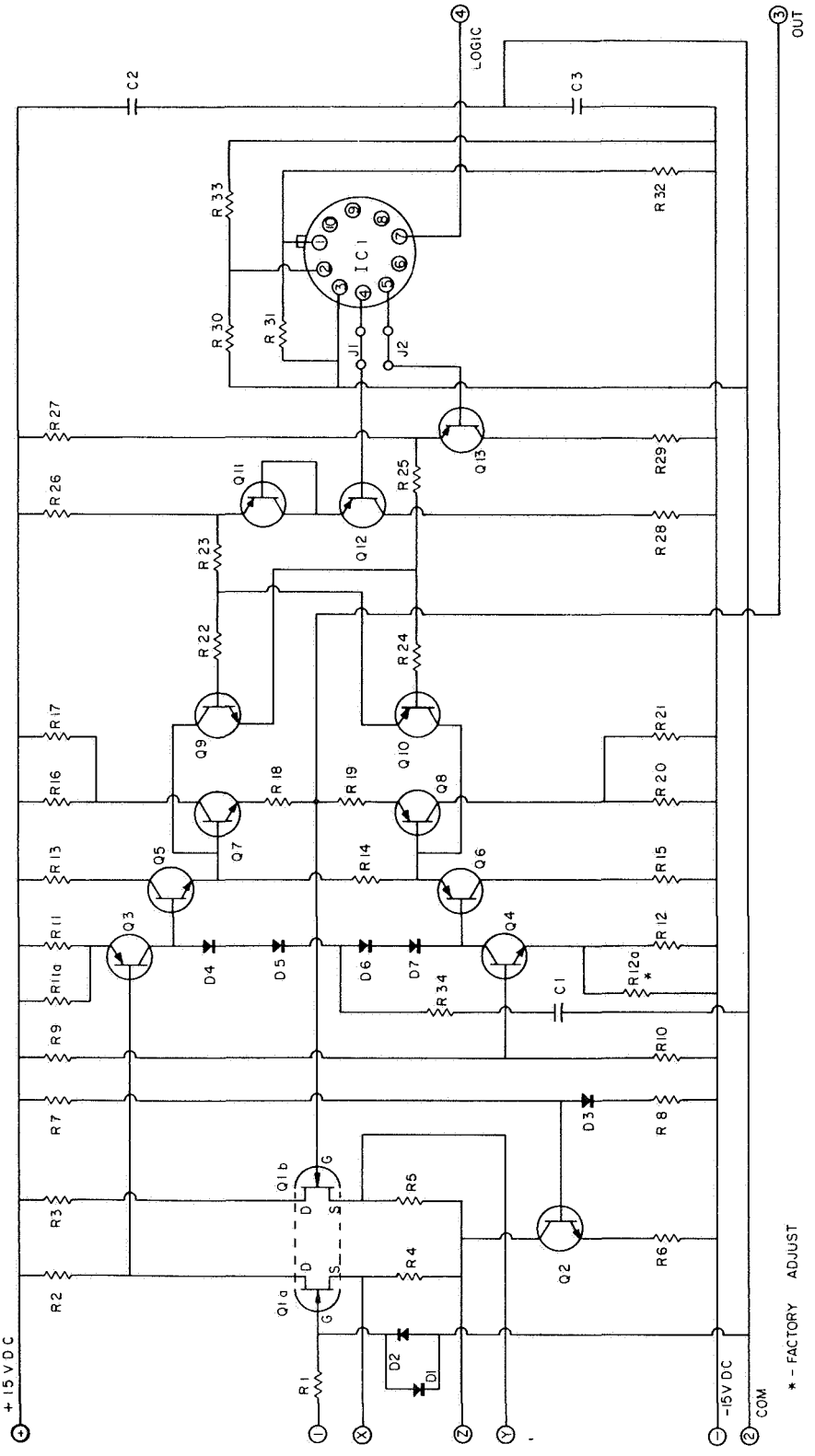


Fig. 4.7 New LOCUST FET Input-stage Electronic Mode-control Switch Schematic Diagram

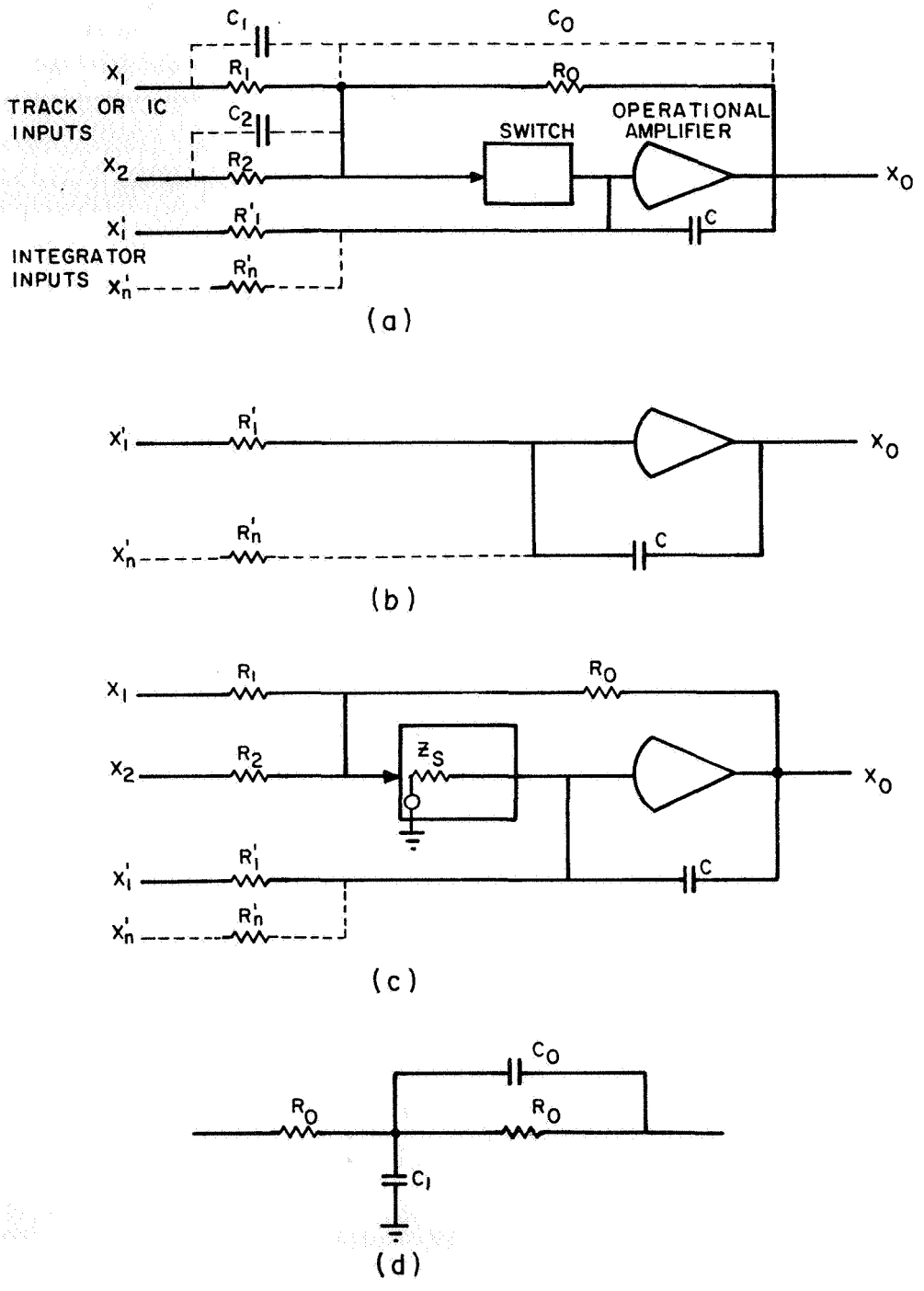


Fig. 4.8 (a) Integrator/Track-hold Circuit
(b) Equivalent Circuit in HOLD or COMPUTE
(c) Equivalent Circuit in TRACK or RESET
(d) Modified Feedback Network Replacing Impedance R_o of (a)

Table 4.2 LOCUST Integrator/Track-hold Circuit Performance

Typical Performance at 25°C		Units
TRACK HOLD		
Voltage Gain	-1.0	ratio
Gain Accuracy at d-c	±0.1	%
Small Signal Freq. Response -3 dB(0.01 μF holding capacitor and no load)	2	MHz
Rated Output		
Voltage	±10	V
Current	±20	mA
Max. Freq. (resistive load)	40	kHz
Output Impedance (at 100 Hz)	0.1	Ω
Output Voltage Drift		
In HOLD (for 10ms and 0.01 μF holding capacitor)		
nominal	±0.2	mV
vs. temperature	±0.05	mV/degC
In TRACK		
vs. temperature	±100	μV/degC
Aperture Time	40	ns
Acquisition Time (settling to 0.1% for 10V input step)	10	μs
SWITCHED INTEGRATOR		
Voltage Gain	10^5, 10^4, 10^3, 10^2, 10, 1	1/s
Gain Accuracy	±0.1	%
Integrator Input Feedthrough in RESET (for ±10V, 100 Hz, 1 kΩ input resistor, and 0.01 μF capacitor)	±1	mV
Rated Output		
Voltage	±10	V
Current	±20	mA

Table 4.2 (Continued)

Output Impedance (at 100 Hz)	0.1	Ω
Output Voltage Drift in COMPUTE (for 10 ms, 10 kΩ input resistor, 0.01 μF capacitor)	± 0.3	mV/degC
Switching Times		
Compute	40	ns
Reset (to within 0.1% of initial condition inputs)	10	μs

$$Z_s < 0.33 \text{ ohm.}$$

To allow for paralleled integrator inputs Z_s should be less than 0.1 ohm.

Referring again to Fig. 4.8(a), the size of the storage capacitor C is determined by two conflicting requirements:

1. Input errors due to voltage and current offset, integration and switching spikes decrease with increasing C.
2. The small-signal frequency response in TRACK and also the maximum voltage rate of change in TRACK improve as C decreases.

Resistors R_0 and R_1 are low resistance (5 kΩ) to minimize stray capacitance effects. Capacitor C_0 is required to decrease amplitude peaking in TRACK; the system might even become unstable if C_0 is omitted. When small values of R_0 and R_1 are used, C_1 is usually not required.

The circuit of Fig. 4.8(d), suggested by R. Whigham, can be used to reduce the dynamic tracking error at higher computing frequencies.

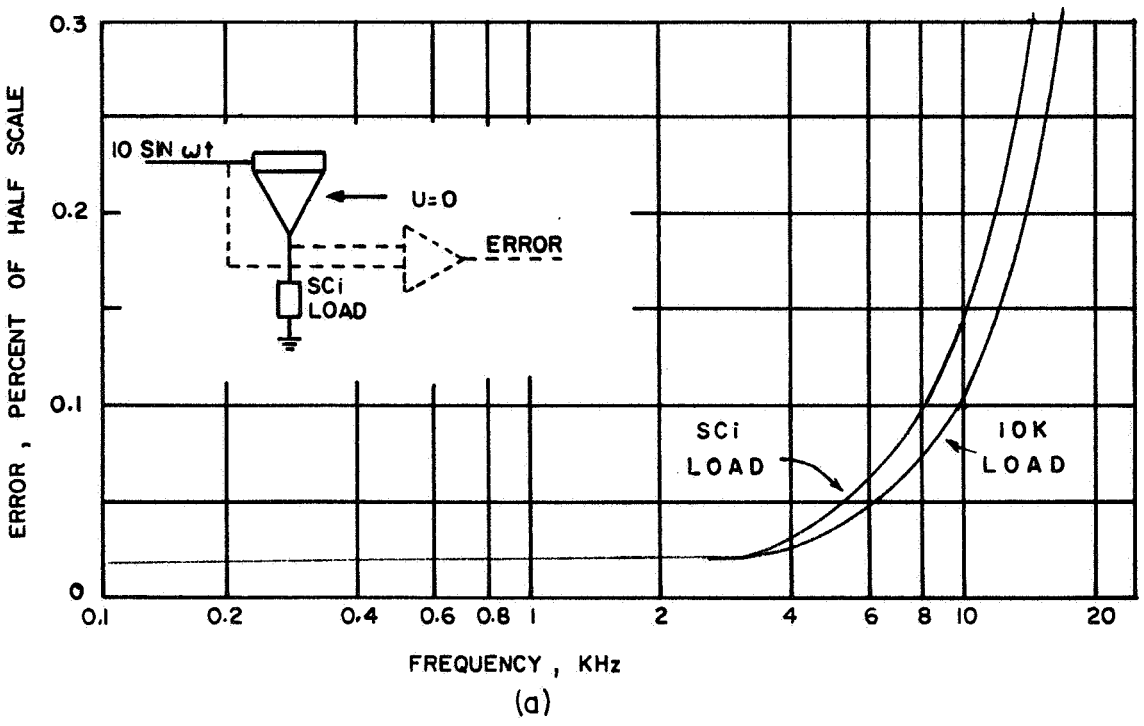
The performance of the integrator/track-hold circuit with the unit installed in the LOCUST patchbay is illustrated in Fig. 4.9. The circuit switches into COMPUTE (HOLD) in typically 40 ns, and two integrators switch within 10 ns of each other, thus meeting the third requirement of Sec. 3.1; the LOCUST mode-control switch is, to the best of the writer's knowledge, faster than any commercially available mode-control switch by a full order of magnitude.

4.3 Digital Attenuator System

Digital attenuators are simple multiplying digital-to-analog converters used to replace coefficient-setting potentiometers in modern hybrid computers (Fig. 4.10). The LOCUST digital attenuator system, designed and tested by Pracht (Pracht, 1967), utilizes miniature metal-film ladder networks switched by latching reed-relays. It is programmed automatically by a digital computer or manually by front panel addressing switches.

The new digital attenuator has a number of interesting features:

1. Latching reed-relays give the system a non-distructive coefficient memory even when the computer is switched off.
2. New digital control logic employs serial data transmission, which not only permits one to set all 200 attenuators of a typical hybrid computer installation within 20 ms, but also requires only one address line per attenuator.
3. Attenuator/relay networks can be plugged directly to the rear of the analog patchbay receiver, thus reducing stray capacitance considerably.



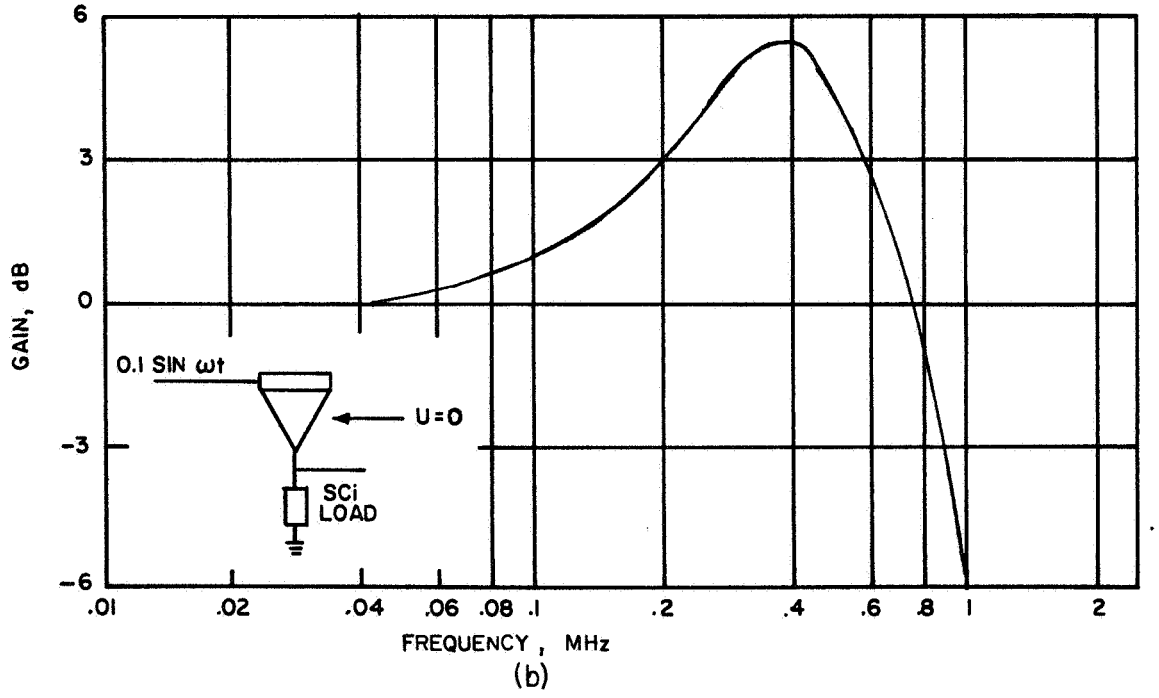


Fig. 4.9 (a) Tracking Error of the Integrator/Track-hold Circuit
(b) Small-signal Frequency Response in TRACK

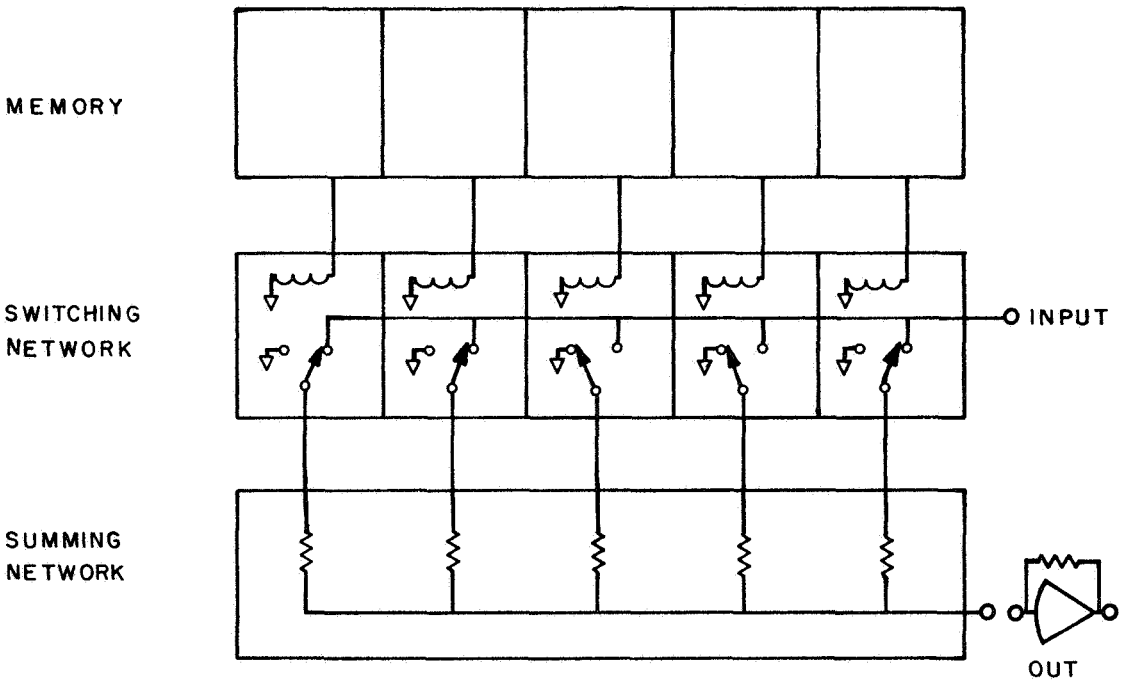


Fig. 4.10 A Typical Digital Attenuator

A block diagram of the digital-attenuator system is shown in Fig. 4.11. When used with a digital computer in the AUTOMATIC mode, a binary word representing the coefficient setting is loaded into the BUFFER REGISTER and at the same time an address representing which attenuator network is to be set is loaded into the ADDRESS REGISTER. Under control of the digital computer, or the analog computer master timer, the TIMING LOGIC shifts the binary coded coefficient setting into the DIGITAL ATTENUATOR REGISTER selected by the ADDRESS TREE.

In the manual mode, the coefficient is programmed by the front panel thumbwheel binary-coded decimal (BCD) switches. The PRESET BCD COUNTER and the BUFFER REGISTER (now serving as a straight binary counter) are permitted to count the clock until the number in the PRESET BCD COUNTER equals the number set on the thumbwheel switches. The BUFFER REGISTER now contains a binary word corresponding to the decimal setting of the thumbwheel switches. The subsequent steps are the same as those in the AUTOMATIC mode.

Specifications of the digital attenuator are summarized in Table 4.3.

Table 4.3 Digital Attenuator Specifications

Number of Bits	14
Static Accuracy	0.02% of half scale
Resolution	0.01%
Gain Range	0.0002 - 3.2767
Feedback Resistance	10 kΩ
Ladder Resistance	2.0514 kΩ
Maximum Load on Input	13.3 mA
Setting Time per 200 Attenuators	20 ms

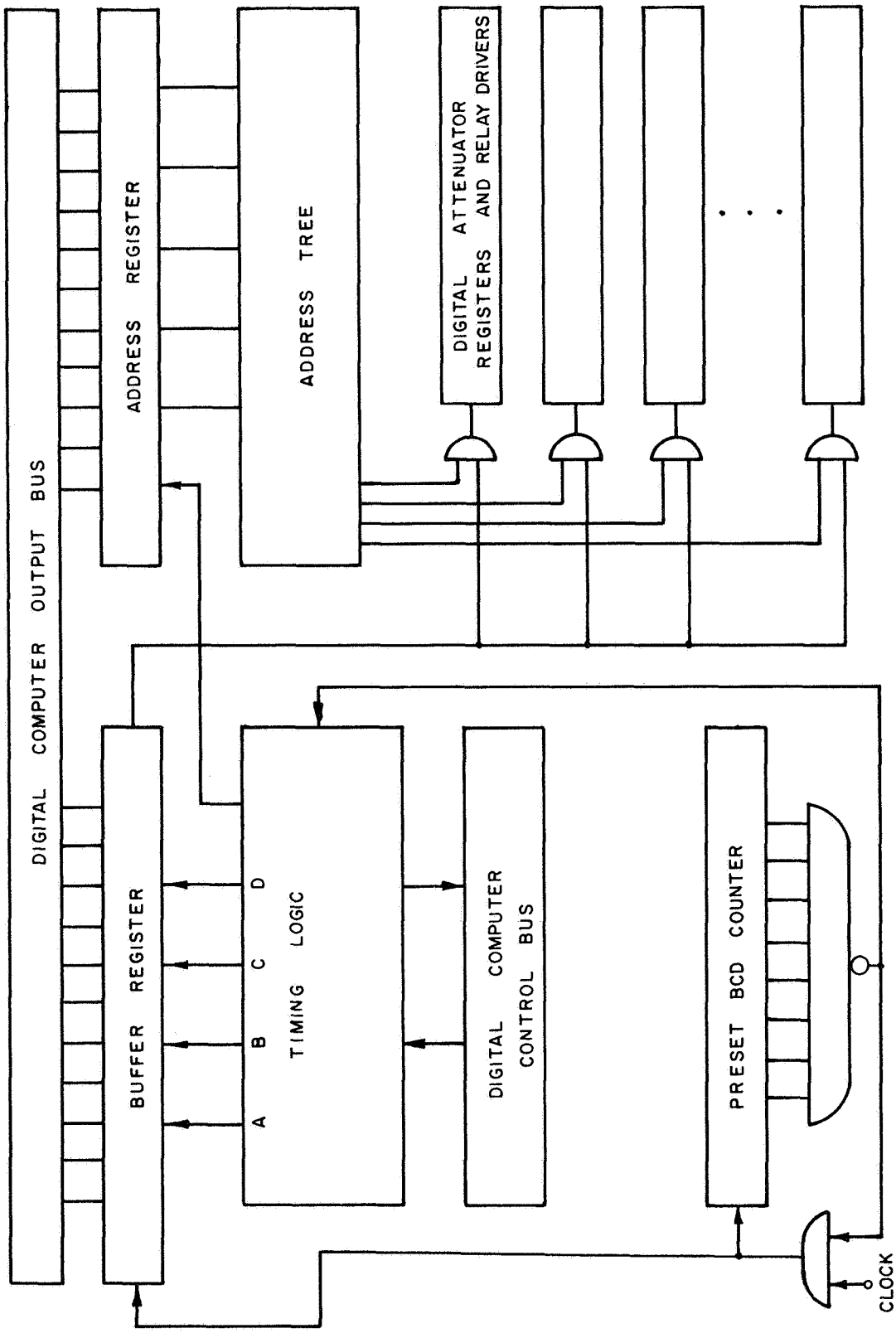


Fig. 4.11 LOCUST Digital Attenuator Control Block Diagram

4.4 Analog Multiplier/Divider

The LOCUST analog multiplier divider is a Burr-Brown Model 9943 Fast Quarter-square Multiplier/Divider very similar to that designed by R. Whigham for ASTRAC II (Whigham,1965a).

The multiplier contains five submodules; three wide-band amplifiers, and two precision absolute-value complementary squaring networks. The diode function-generator type squaring modules are temperature compensated and have internal Zener-regulated reference voltages to eliminate the need for adjustments.

The multiplier/divider is installed in a LOCUST analog-module can and plugged directly into the rear of the patchbay. The patching field permits the unit to be patched as a 4-quadrant multiplier or as a 2-quadrant divider.

Performance curves are presented in Fig. 4.12, and specifications are listed in Table 4.4.

Table 4.4 Multiplier/Divider Specifications

Typical Performance at 25°C		Units
Input Signal Levels	±10	V
Rated Output		
Voltage	±10	V
Current	±20	mA
Output Impedance	10	Ω
Static Accuracy		
Multiplication	±0.15	% of 10V
Division	±1.5/Y	% of 10V
Frequency Response	See Fig. 4.12	

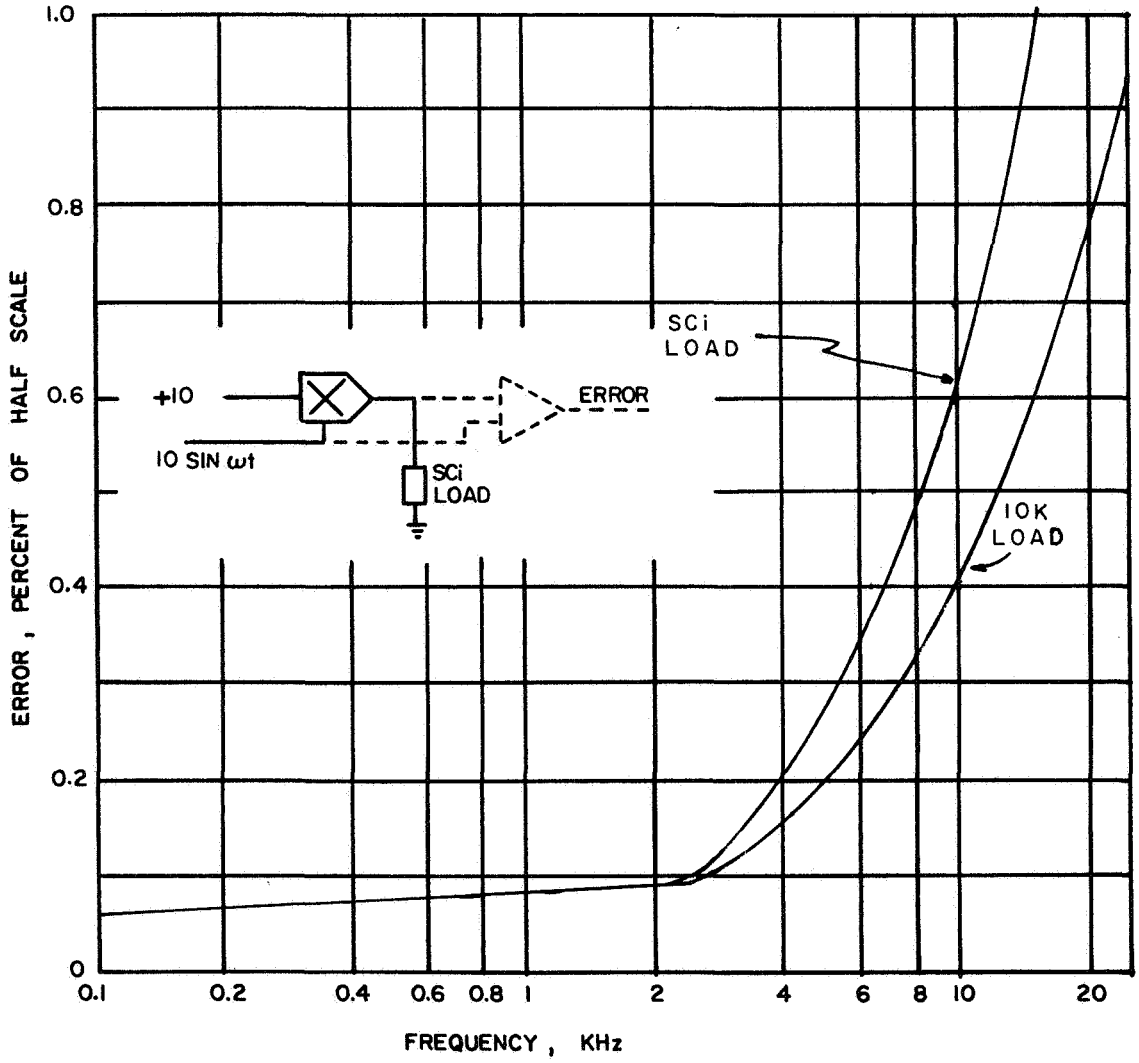


Fig. 4.12 LOCUST Multiplier Performance

4.5 General-purpose Diode Function Generator

The LOCUST plug-in diode function generator [Fig. 4.13(a)] (Whigham, 1965b) plugs into the front of the analog patch panel and covers the patching field of an associated dual-amplifier module. The circuit [Fig. 4.13(b)] utilizes two amplifiers to provide both positive and negative slopes. Six breakpoints are fixed at approximately ± 1, ± 3 and ± 5.5V. Slopes and d-c level (parallax) are set by means of eight 15-turn wire-wound potentiometers. Input diodes D1 and D2 reduce input loading while shunt diodes D3 and D4, together with the low impedance levels used throughout LOCUST, improve frequency response. The maximum current load presented to an amplifier is 18 milliamperes.

The error for a given frequency depends on the function set up. In general, the error is less than 0.5 percent of half scale for input frequencies below 5 kHz with slopes less than 2 volts per volt. The large-signal amplitude frequency response for an SCi standard straight-line function (Simulation, 1963) exceeds 1 MHz. Function-generator voltage drift is approximately 2 mV/degC.

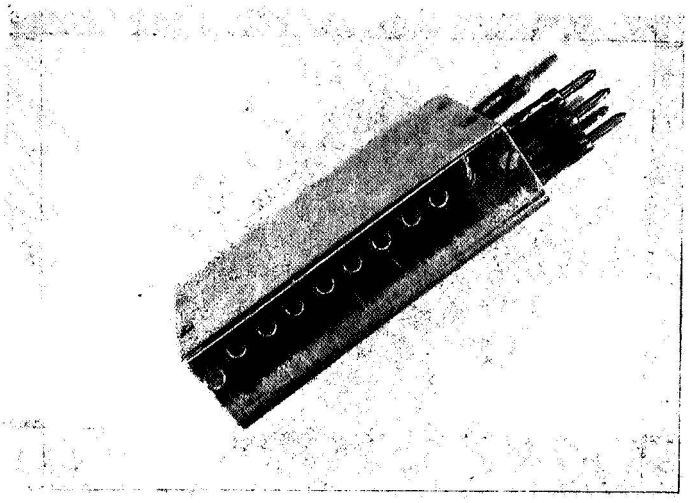
4.6 Circle-test Performance

The combined effects of phase shift in computing elements can be measured by applying the circle test (Korn and Korn, 1964). The actual computer solution to the ideal harmonic-oscillator equation

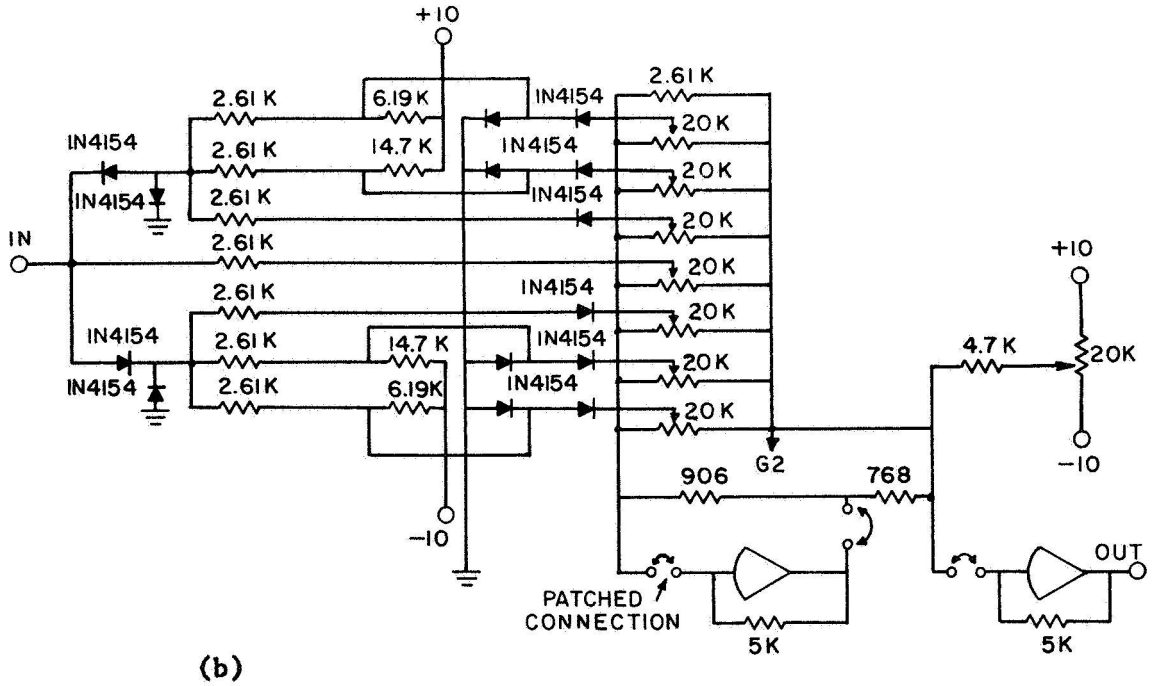
$$(p^2 + \omega^2)Y = 0 \qquad Y(0) = 0,\ \dot{Y}(0) = B$$

is

$$Y = Be^{-\omega\,\delta(\omega)\tau} \sin \omega\,\tau$$



(a)



(b)

Fig. 4.13 (a) LOCUST Plug-in Diode Function Generator and (b) its Schematic Diagram

where $\delta(\omega)$ is the phase shift due to the integrator, phase inverter and coefficient potentiometer. The solution amplitude decays exponentially with time for a positive net phase error (lead), while a negative net phase error (lag) causes the amplitude to increase exponentially. Figure 4.14 illustrates the computer setup and the combined phase shift for the LOCUST elements.

One of the potentially largest sources of error in the solution of differential equations is the error due to inaccurate gains of the individual computing elements. For instance, the computer solution to the harmonic-oscillator equation is

$$Y = B \sin \omega \tau \quad ;$$

assume the phase shift $\delta(\omega)$ is zero. The change in Y due to a change in the gain of the two integrators (and hence ω) is

$$\frac{dY}{d\omega} = B\tau \cos \omega \tau$$

giving a maximum change in Y of $2\pi B/\omega$ per cycle. For small changes in ω the fractional change in Y per cycle is

$$\frac{\Delta Y}{B} \approx 2\pi \frac{\Delta \omega}{\omega} \quad .$$

As an example of the importance of this relationship, assume that each integrator has a gain error of 0.1 percent and the phase inverter has zero phase error. The maximum error in Y is then 2π x 0.1 percent per cycle. This point stresses the desirability of specifying very accurate element gains.

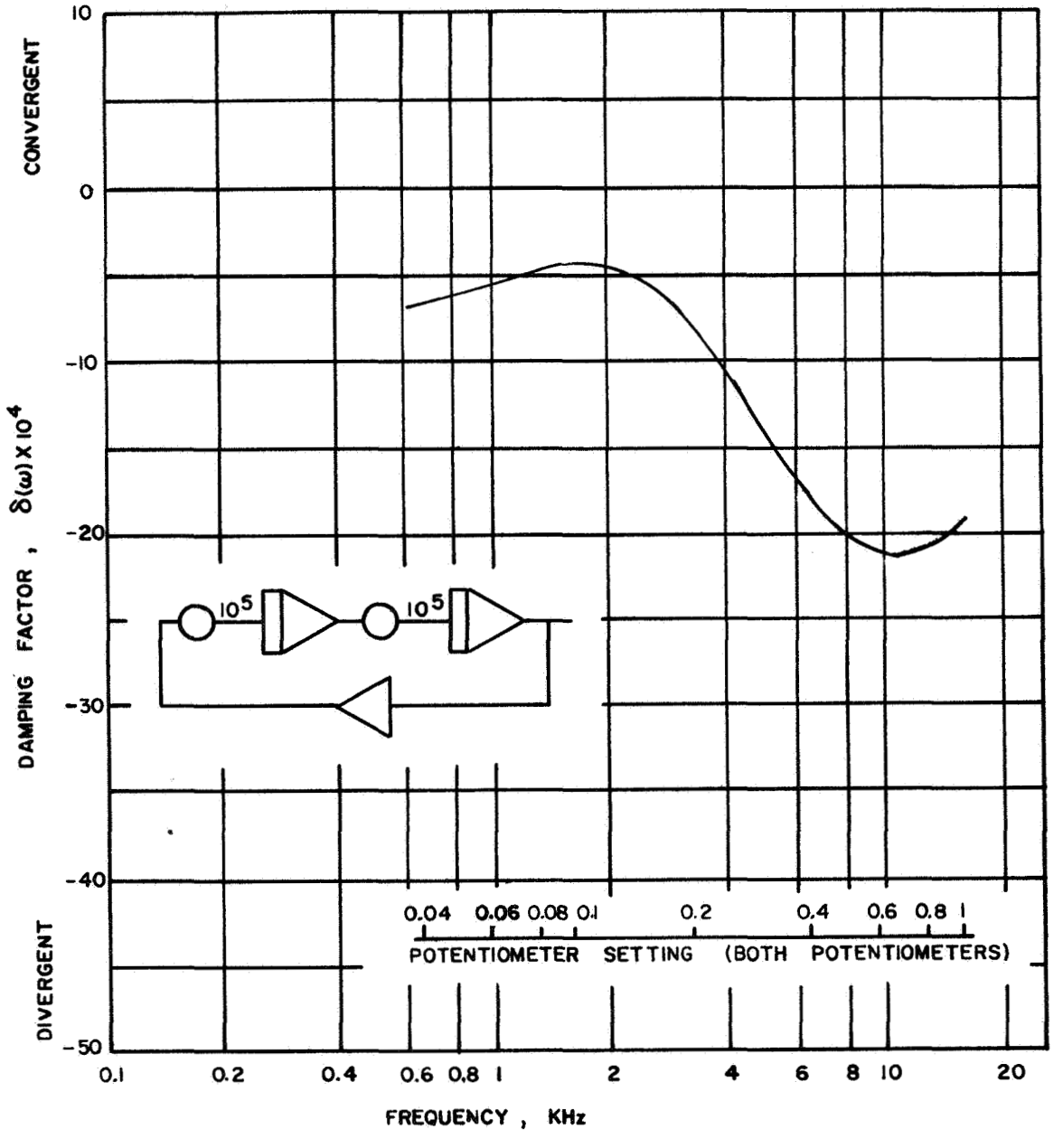


Fig. 4.14 Circle Test Data

Chapter 5

LOCUST DIGITAL SYSTEM

Basic iterative differential analyzer control requires periodic RESET pulses to control switches and integrators. More flexible control circuits permit one to change repetition rates, to vary the length of the COMPUTE and/or RESET period, and to select the timing of sampling pulses for accurate analog/digital conversion readout and analog storage. Subroutine counters may also be used to change the computer program after a preset number of iterations or other events.

The LOCUST digital system provides many of these functions in the form of "packaged" subroutines selected by front panel control (Fig. 5.1). This feature liberates the operator from designing and patching his own subroutines with the patchable digital logic and leaves him free to concentrate on a much wider class of operations, for detailed iterative subroutine control design is far from easy for most analog computer users. Less frequently employed subroutines can still be patched on the digital patchbay, which contains free logic gates, flip-flops, decade counters and shift registers. A list of the digital logic cards is presented in Table 5.1.

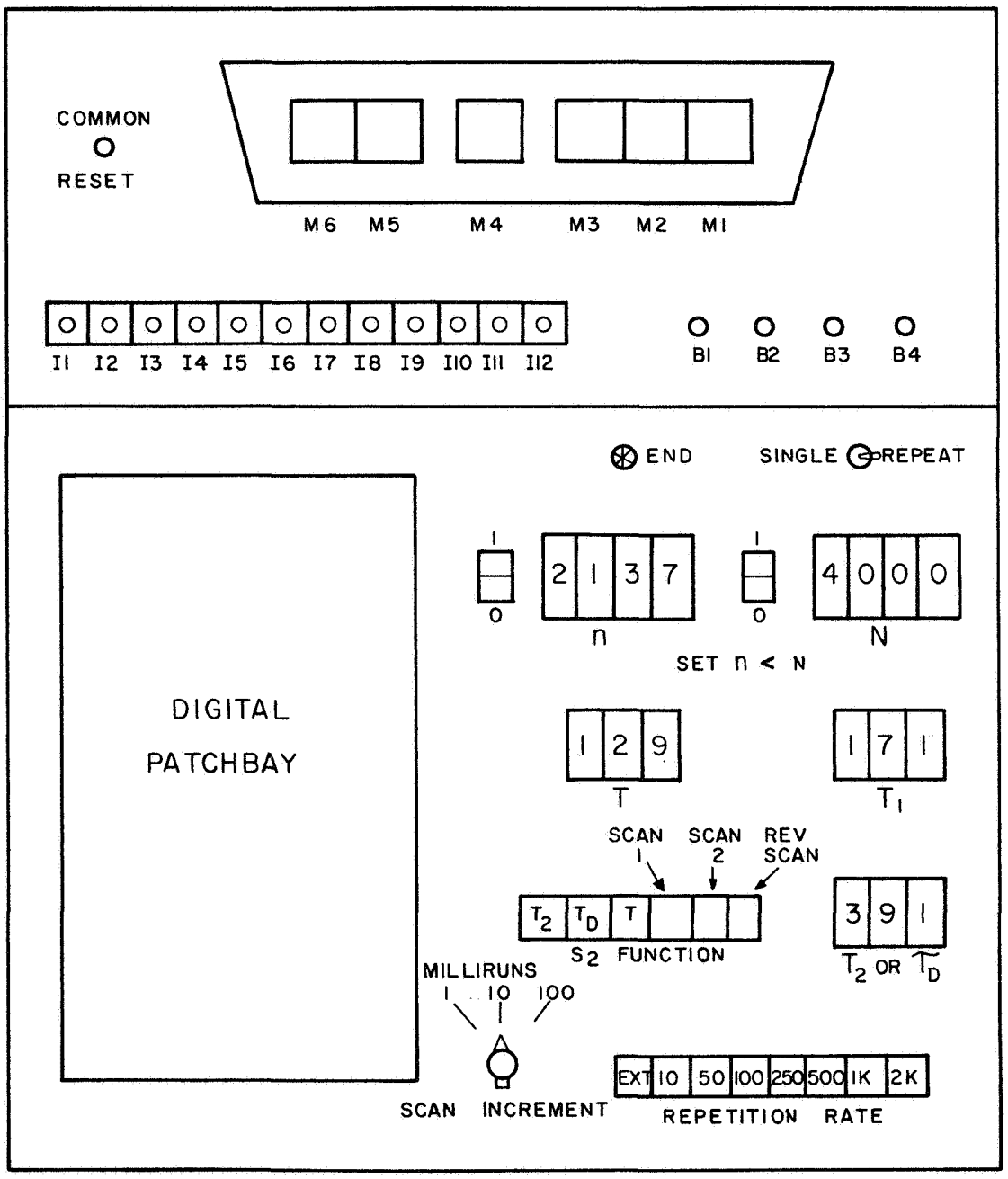


Fig. 5.1 LOCUST Digital Control Module

Table 5.1 LOCUST Digital System Logic Cards

1. A front panel pushbutton logic card provides computer initial reset pulse R_I and a clock interrupt signal to the master timer logic.

2. A master timer card provides periodic computer reset pulses, a presettable sampling pulse and several other timing pulses.

3. An auxiliary timer card provides a presettable sampling pulse whose timing relative to the master timer reset and sampling pulses is selected by a front panel switch; it also provides scan modes whereby the sampling pulse is timed to move forward or backward with respect to the computer reset pulses one step each computer run or N computer runs.

4. A subroutine counter card provides an output pulse every n and N computer runs (or other events) preset by front panel decade switches.

5. Six free logic cards each containing 2 J-K type flip-flops, two 3-input OR/NOR gates and one 4-input OR/NOR gate.

6. Four shift register cards each with 6 stages and special reset/set logic (which can also be used as a fixed-delay one-shot multivibrator), and a modulo-2 adder all of which can be patched for computation, memory, and pseudo-random sequence generation (see APE II shift register discussion, Chapter 2).

7. A sampling-type Zener-diode noise generator card with 2 noise generators.

8. Six BCD decade counter cards with associated in-line readout.

The LOCUST digital system also includes digital patchbay terminations for:

1. Inputs for individual integrator/track-hold capacitor and feedback resistor selection.
2. 4 analog comparator outputs
3. 12 logic-state lamp inputs
4. 4 free pushbutton logic outputs
5. A logic output common to all simplifier overload circuits
6. Inputs to level changers (noise drivers) which provide ±10-V outputs under logic control.
7. Trunk lines to a PDP-9 digital computer interface equipment.
8. A/D converter control inputs.

These digital system features incorporate some new operator conveniences not found in ASTRAC II: (1) each integrator or track-hold capacitor selection requires only a single patch connection, (2) digital system logic levels can also control capacitor selection, (3) free fixed-delay (100 ns) one-shot multivibrators associated with the shift registers are available, (4) front-panel pushbuttons with digital-system-logic-level outputs are available, (5) an overload logic output common to integrator/track-hold and summing amplifiers, (6) three switch-selected SCAN FORWARD and REVERSE SCAN rates. In addition, trunk, interrupt and control terminations enable LOCUST to interface directly with a digital computer. For the same reason, INITIAL RESET, COMPUTE and SINGLE RUN modes can be controlled by signals on the digital patchbay.

Motorola Emitter Coupled Logic (MECL), an extremely fast current-mode logic family is used throughout the LOCUST digital system. Extremely fast logic (faster than 5 MHz) is not as such necessary for the

digital control logic, but the balanced-current nature of current-mode logic and the low logic level swing (0.8 V nominal) are necessary to minimize digital noise in the analog system, where it might cause false initial conditions, incorrect sample values and spurious analog-comparator operation.

A block diagram of the design of the LOCUST digital control system is presented in Fig. 5.2. Control functions are divided among a master timer, an auxiliary timer and a subroutine counter. Modular design permits one to build the master timer first and add the other functions as needed.

5.1 Clock and Repetition-rate Selection

A frequency-dividing counter chain receives 4 MHz pulses from a crystal-controlled clock and delivers timing pulses whose frequencies are 4 MHz, 2 MHz, 1 MHz, 500 kHz, 100 kHz, 50 kHz and 10 kHz for control and display purposes. From these, the repetition-rate selector switch selects a clock pulse train (C1) which has exactly 1,000 times the desired computer repetition rate $f_R = 1/T_R$ = 2,000, 1,000, 500, 250, 100, 50 and 10 computer runs per second (Fig. 5.2). All subsequent analog-hybrid-computer timing is performed in terms of these C1 pulses (1,000 per computer run), whose duration is called 1 millirun. This permits the repetition-rate selector to automatically change the time scale of all timing and counting operations. The repetition rate selector can also change integrator capacitors through relays to provide completely automatic time scale changes; this automatic capacitor selection can be overridden with patched logic connections.

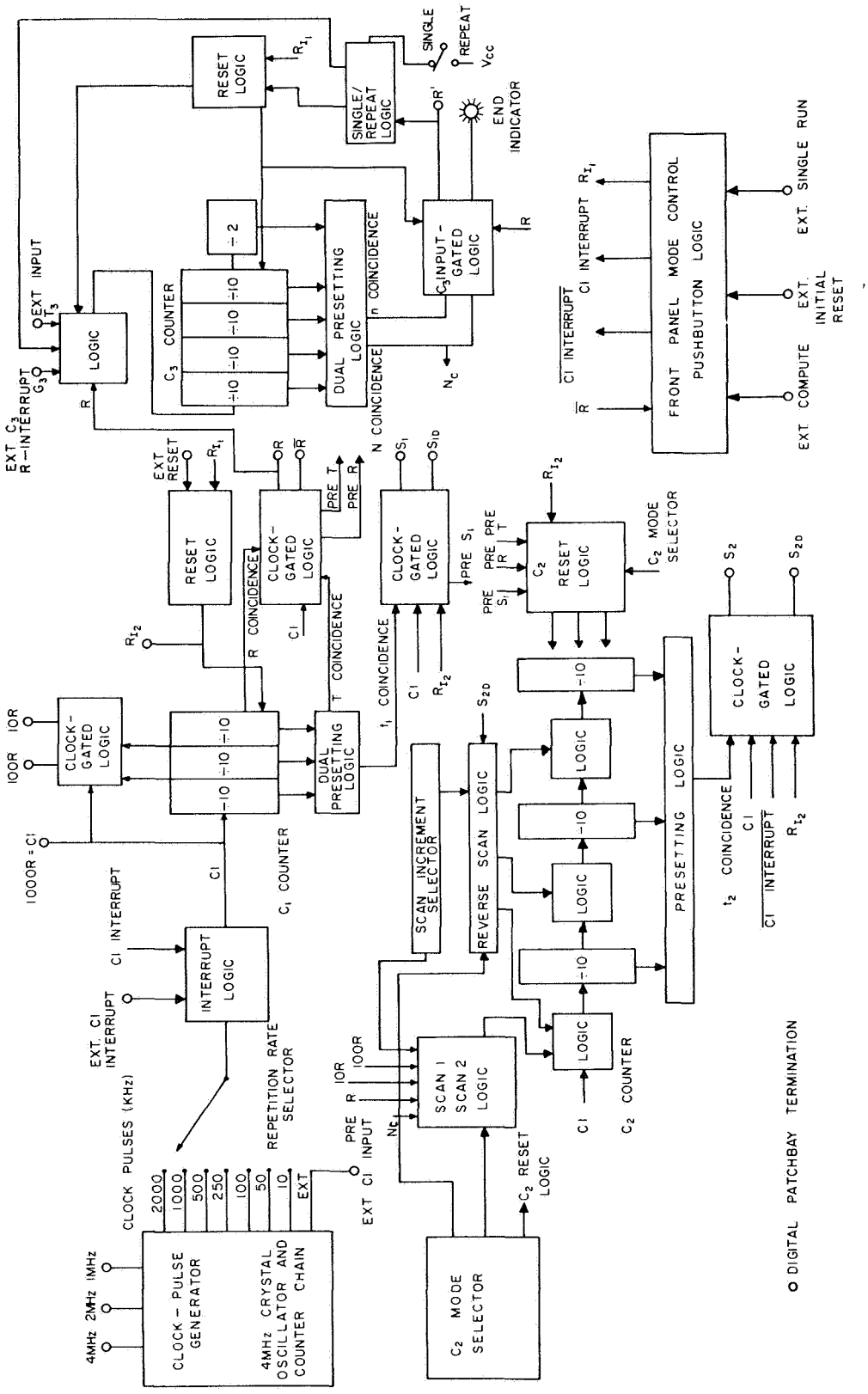


Fig. 5.2 Block Diagram of the LOCUST Digital Control System

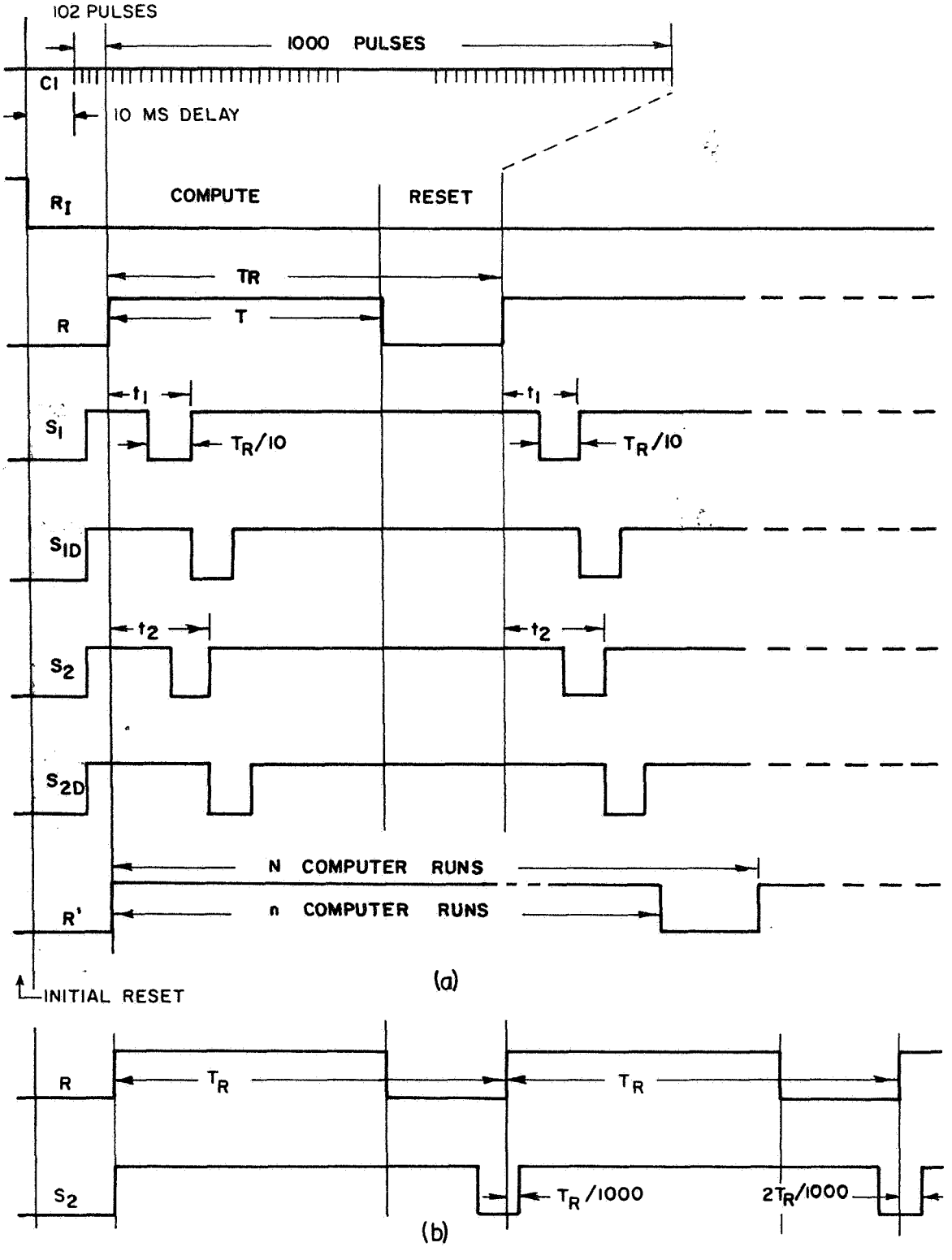


Fig. 5.3 (a) Timing and Control Signals for Normal Repetitive Operation and (b) Control Signals for SCAN 1 Operation

5.2 The Master Timer

The master timer (C_1 counter, Fig. 5.2) fed by C1, is a three-decade decimal counter with dual thumbwheel-switch preset outputs designed to perform the following timing functions:

1. It counts down by 1,000 to mark the start of periodic COMPUTE periods [t = 0, Fig. 5.3(a)].
2. It produces accurate timing markers at 10 and 100 times the computer repetition rate.
3. Thumbwheel decade switches select counter outputs at t = T and t = t_1 milliruns after the start of each COMPUTE period in steps of 1 millirun.

In normal repetitive operation [Fig. 5.3(a)], the integrator control pulse R is equal to logical 1 at t = 0 and a logical 0 at t = T thus producing periodic pulses so that COMPUTE periods of length T alternate with RESET periods of length T_R - T. Note that one can independently select T_R (with the repetition rate selector) and T (with the thumbwheel decade switches). The output at t = t_1 milliruns feeds a timing logic block to produce periodic sampling pulses S_1 and also delayed sampling pulse S_{1D} of length $T_S = T_R/10$ for special track-hold-pair operations (Eckes and Korn, 1964). A track-hold circuit controlled by S_1 will periodically TRACK for T_S milliruns and then switch into HOLD at t = t_1 milliruns. S_{1D} switches T_S milliruns later than S_1 for memory pair or memory triplet (when used with R) operation.

All timing pulses, RESET pulses and TRACK-HOLD control pulses are available on the digital patchbay for flexible control and timing of

individual integrators, switches and digital operations. In normal repetitive hybrid-computer operation integrators are controlled by R, and the track-hold circuits are controlled by S_1 for digital readout of sample values $X(t_1)$ at the accurately set computer time t_1. Different patching connections can employ R, S_1 and S_{1D} to produce very flexible memory and timing control.

A patchable master timer-reset input allows one to reset C_1 and permits finer control of the computer-run period than is possible by the normal coarse repetition-rate selection. For instance, one can use S_1 to reset C_1 at t_1; this will reset integrators for 102 milliruns and then start a new COMPUTE period of duration t_1 milliruns. Many other possibilities exist. One may also patch to an external clock. One can also interrupt the Cl pulses with a digital-computer control signal. It is also possible to control the length of individual computer runs with patched comparator logic to conserve time in long computations.

5.3 The Auxiliary Timer

The auxiliary timer (C_2 counter) is another three-decade counter with a thumbwheel decade-switch preset output. The S_2 function switch controls the operation of the C_2 counter and its associated logic. For the different S_2 function switch settings, the thumbwheel switch, "t_2 or τ_D", functions as follows (refer to Fig. 5.3):

1. T_2 position -- The trailing edge of S_2 (TRACK to HOLD) occurs t_2 milliruns after the start of each COMPUTE period.

2. τ_D position -- The trailing edge of S_2 occurs at $t_1 + \tau_D$ **milliruns** after the start of each COMPUTE period. Thus the "t_2 or τ_D" thumbwheel switch directly sets a delay interval of length τ_D between the S_1 and S_2 sampling pulses. When S_1 and S_2 are used to control track-hold circuits, the sample pairs $X(t_1)$, $Y(t_1 + \tau_D)$ are produced, e.g. for correlation and prediction studies.

3. T position -- The trailing edge of S_2 now occurs at $T + t_2$ milliruns after the start of each COMPUTE period. S_2 and S_{2D} then serve for readout during the RESET period, as S_1 and S_{1D} serve during the COMPUTE period. This is useful for "alternating" differential analyzer runs using integrator groups controlled by R and $\tilde{R}$.

4. SCAN 1 position -- C_2 recycles after 1,000 + M milliruns where M is 1, 10 or 100 milliruns selected by the scan increment switch. On the first run, the trailing edge of S_2 occurs at t_2 milliruns; on the second run S_2 occurs at t_2 + M milliruns; on the third at t_2 + 2M milliruns, etc. [Fig. 5.3(b)]. Track-hold circuits controlled by S_2 and S_{2D} will then "scan" periodic computer runs for readout into slow recorders, printers, or digital computers. With the repetition rate switch set at 100 and M set to 1, for instance, a complete solution scan requires 10 seconds.

5. SCAN 2 position -- The subroutine counter (C_3 counter) permits the scanning S_2 to step forward by M milliruns only after a

preset number, N, computer runs or N other events. This feature is used for automatic computation of random-process statistics (correlation functions, delay errors) over samples of N computer runs (Fig. 5.4).

6. REVERSE SCAN position -- On the first run, the trailing edge of S_2 occurs at t_2 milliruns; on the second run S_2 ends at t_2 - M milliruns and continues to scan backwards in steps of M milliruns.

The SCAN modes are useful for slow recording of repetitive solutions (X vs. t, of Y vs. X), but also for automatic parameter changing (new values of a repetitive-analog-computer solution are used in successive computer runs, for multiple-solution oscilloscope displays and for solution checks with slow computers. The REVERSE SCAN mode is useful for computing convolution integrals, for backward integration (e.g., in boundary-value problems), for modified-adjoint-system techniques, and for controlling delay-line-memory read/write cycles. The SCAN 2 mode is, as noted earlier, intended for automatic computation of statistics over N computer runs.

5.4 Subroutine Counter

The subroutine counter C_3 (Fig. 5.2), is a four-decade counter with dual thumbwheel switch preset outputs and is patched to count computer runs, comparator output steps or other events. C_3 produces preset counter outputs after n and N events (n N 20,000), (Fig. 5.3, p. 82). This counter output R' is used to terminate and/or start subroutine sequences. The repeat switch (Fig. 5.1, p. 77) permits C_3 to be

Fig. 5.4 Random Process Simulation.

The high-speed iterative differential analyzer implements Monte-Carlo techniques by simulating a random-input dynamical or communication system 10 to 2,000 times per second.

Digitally controlled track-hold units read out samples of dynamical variables X(t) and Y(t) at thumbwheel-switch-selected times t_1, t_2 after the start of each computer run. The statistics computer (e.g., a digital computer with A/D-D/A interface equipment) averages functions of successive sample values to produce estimates of mean-square values, correlation functions, probabilities for nonstationary as well as stationary processes.

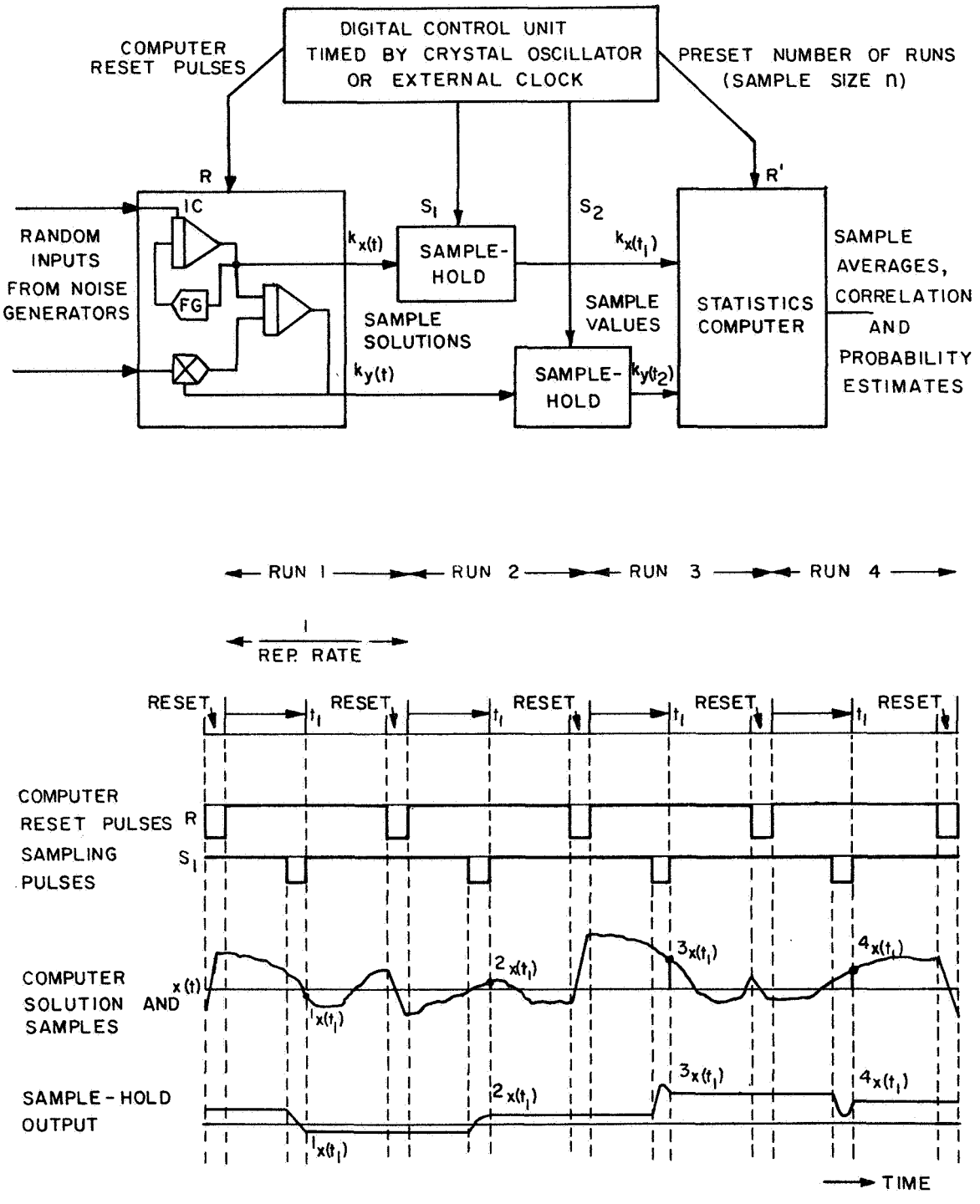


Fig. 5.4 Random Process Simulation

reset after N events and to recycle the entire sequence. In particular, one can control fast integrators with R and slow integrators with R' (two-time-scale operation), thus producing "nested" iterative subroutines.

5.5 Starting and External Control

Before computation, one depresses the INITIAL RESET button momentarily or holds the COMPUTE button down to produce the following conditions:

1. The pushbutton control-logic establishes the initial reset mode (R_I = "1").
2. The subroutine counter C_3 is reset (R' = "0").
3. The master timer C_1 and the auxiliary timer C_2 are reset; output logic is set to produce R = "0" and the correct initial values of the control pulses S_1, S_{1D}, S_2 and S_{2D} ("0" TRACK, Fig. 5.3).

It follows that all integrators, memory pairs and other devices controlled by R, R', S_1, S_{1D}, S_2 and S_{2D} are now reset to suitable initial conditions (RESET or TRACK) ready for computation.

This state is maintained until one releases (or depresses and releases) the COMPUTE button. Then a delay of 10 ms occurs (determined by a one-shot multivibrator in the pushbutton-logic-control circuit). Then S_1, S_{1D}, S_2 and S_{2D} are set to "1" (HOLD). Next C_1 runs through 102 C1 pulses and then R and R' are set to "1" (COMPUTE) thus beginning the first COMPUTE period (Fig. 5.3).

The SINGLE RUN button produces a single computer run without resetting C_1, C_2 or C_3, so that one can check the progress of iterative subroutines computer run by computer run.

External control inputs are available on the digital patchbay and perform the following functions:

1. C_1 RESET -- permits finer control of the repetition rate.
2. C1 INTERRUPT -- permits interruption of C1 pulses into C_1 and C_2.
3. EXTERNAL INITIAL RESET -- permits logic, perhaps from a digital computer, to switch the computer into INITIAL RESET.
4. EXTERNAL COMPUTE -- permits logic to start the computer.
5. EXTERNAL SINGLE RUN -- External logic can initiate a single computer run.

These logic functions are intended mainly for control of iterative analog/hybrid computation by an associated digital computer.

Chapter 6

SPECIAL COMPUTING ELEMENTS

To make maximum use of the LOCUST computer system, a number of special digital and hybrid computing elements are needed. Noise generators, digitally controlled analog switches (D/A switches and D/A "noise drivers" or reference switches) multiplying digital-to-analog converters (MDACS), analog comparators, shift registers and modulo-2 adders permit computer implementation of random-process studies, sampled-data systems and various optimization schemes. Multiplying digital-to-analog converters interface with a small digital computer for computation of statistics, function generation and parameter adjustment.

6.1 Analog Comparator

The LOCUST and APE II analog comparators supply a digital output whose logic levels ("1" or "0") depend upon the sign of an analog input or on the sign of the sum of two analog inputs. In modern iterative differential analyzer applications, comparators are used in two different ways. The first mode of application involves the changing of a computer program between computer iterations, and the second requires the changing of the program during the computation period. The requirement for speed (rise-time plus delay) is not critical in the first case, because the comparator is driven by a track-hold circuit whose output is essentially constant during the voltage comparison. But comparators which must detect sign changes during the computation period must be

extremely fast, because at iteration rates of 2000 runs per second, voltage change rates of up to 20π volts per second can occur in LOCUST. To remain within 0.2 percent comparator-timing error computation, full-scale sinusoids would have to be held below 3 kHz for 100 nanosecond conversion delays.

The LOCUST/APE II comparator utilizes the Fairchild μA710C integrated-circuit comparator (Fig. 6.1). The input circuit is designed with very low impedance to reduce offset-current errors and is diode-protected to handle 10-V analog computing voltages. The output circuit is a MECL gate, which acts as a buffer and logic-level changer. Free patched logic serves for comparator latching (Korn and Korn, 1964) and strobing, if desired.

Table 6.1 summarizes the performance of the integrated-circuit analog comparator (Conant, et al., 1967).

The comparators are housed in analog-module cans and plugged directly into the rear of the analog patchbay.

6.2 Digital-to-analog Switch and Logic-controlled Relay

The LOCUST digital-to-analog switches can be thought of as one-bit digital-to-analog multipliers, which are used to switched analog variables ON and OFF, to the switch between two analog variables (SPDT action) in response to digital commands. The switches are housed in analog-module cans and plug directly into the rear of the patchbay.

The LOCUST D/A switches are dual-transistor shunt switches (Fig. 6.2) similar to those used in ASTRAC II. Two sets of switches are digitally driven in pairs to implement a SPDT switch. Figure 6.3

Table 6.1

Analog Comparator Performance Specifications

Input Signal Range	± 10V
Input Impedance	750 ohm
Output Levels (complementary)	MECL logic levels
D-C (static) Switching Accuracy	adj. to ± 1 mV
A-C (dynamic) Switching Speed	
Rise-time	20 ns
Delay*	80 ns
Hysteresis	± 10 mV
Drift of Threshold with Temperature	100 μV/degC

*Measured with 0.1 peak 500 kHz sine wave input; delay is less than 40 ns with fast rise time inputs. With very slow inputs, additional delay will result from the time required for the input to pass through the 20 mV hysteresis interval.

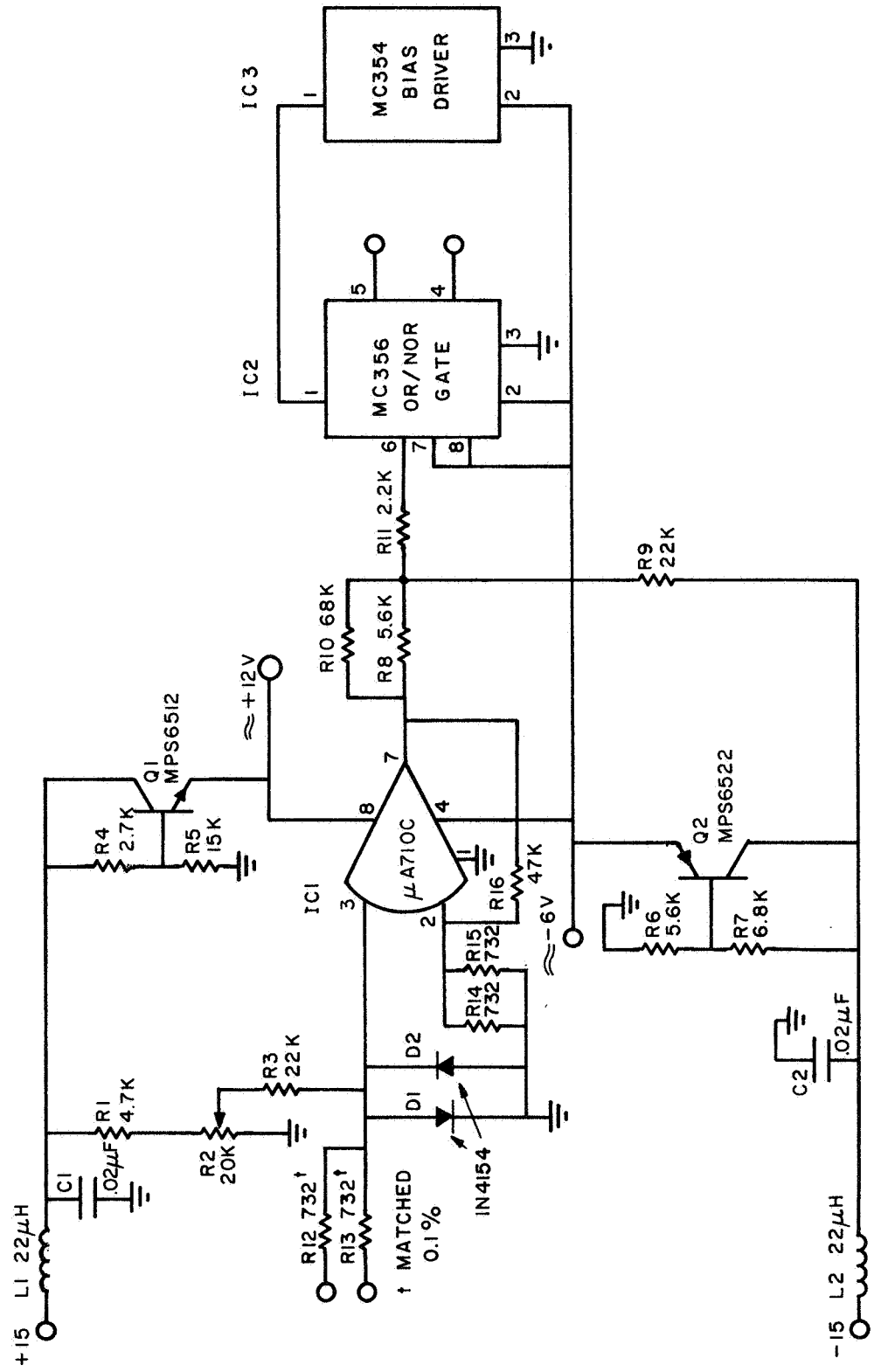


Fig. 6.1 LOCUST/APE II Analog Comparator Schematic Diagram

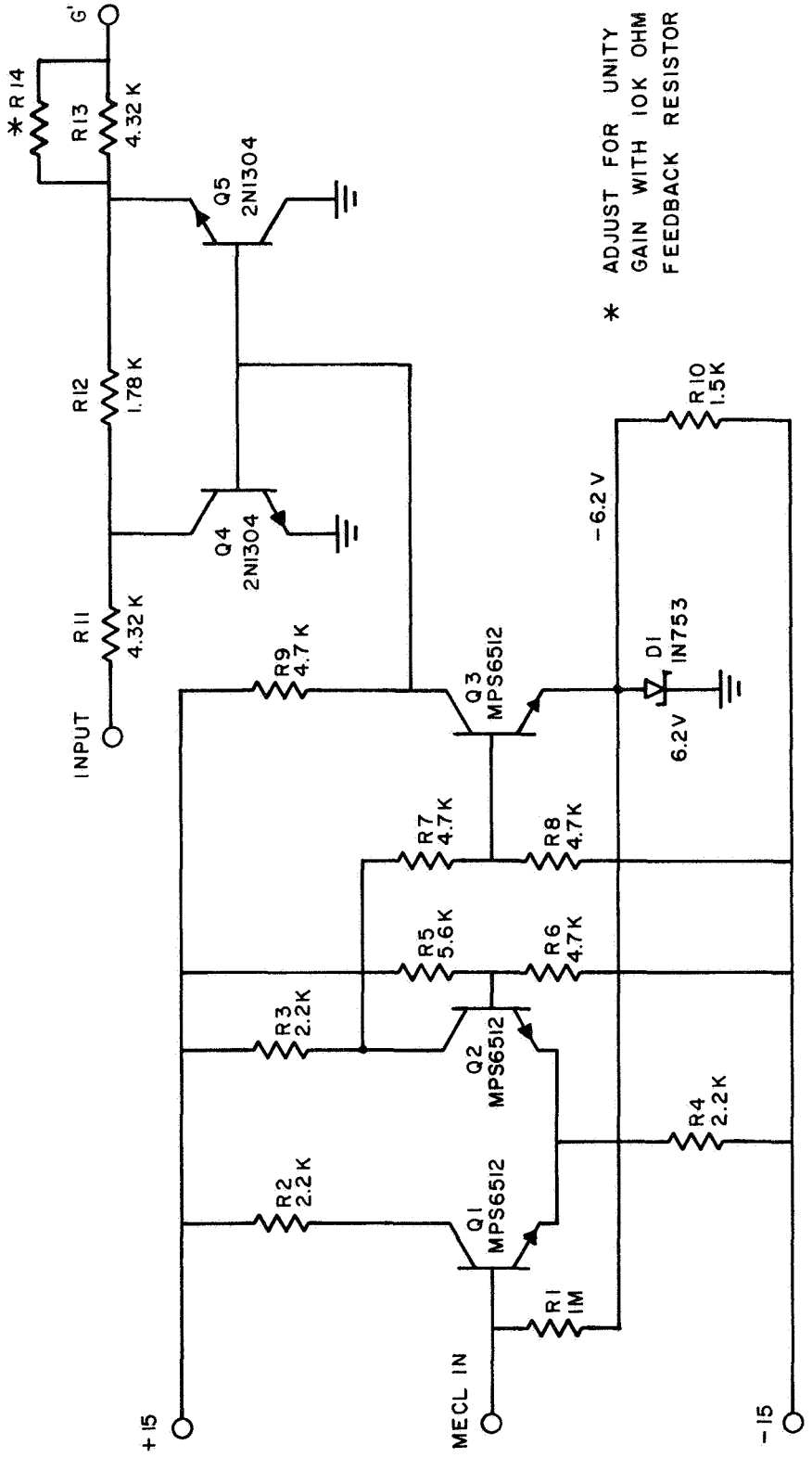
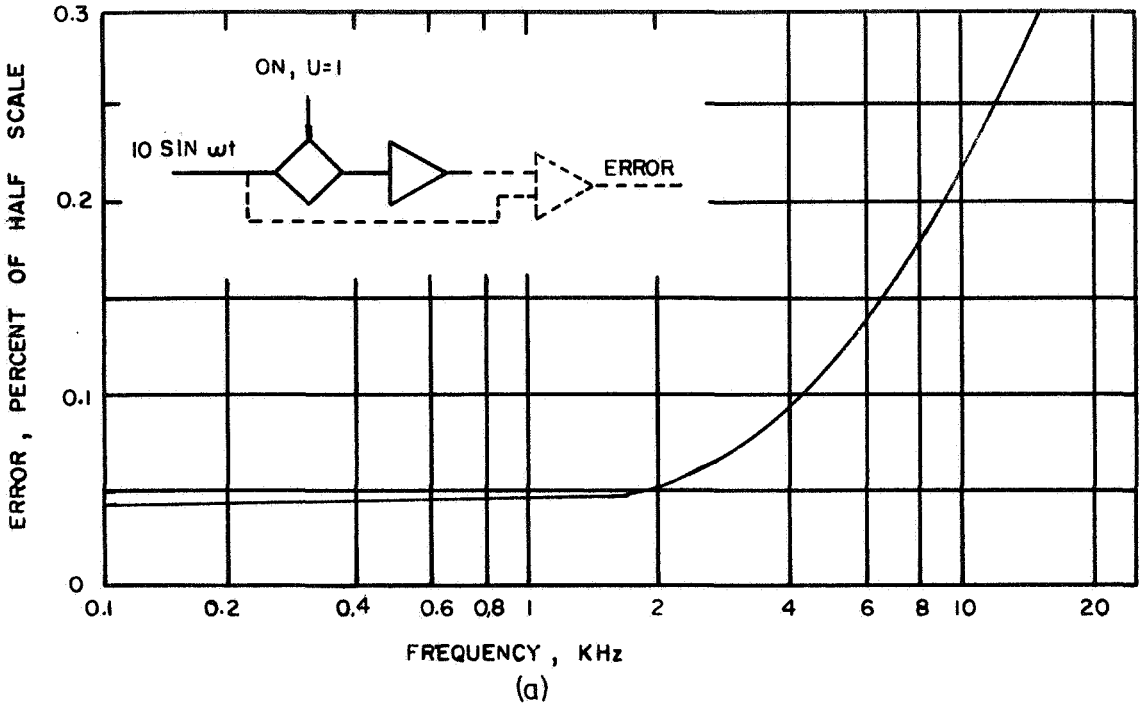


Fig. 6.2 D/A Dual-transistor Shunt Switch Schematic Diagram



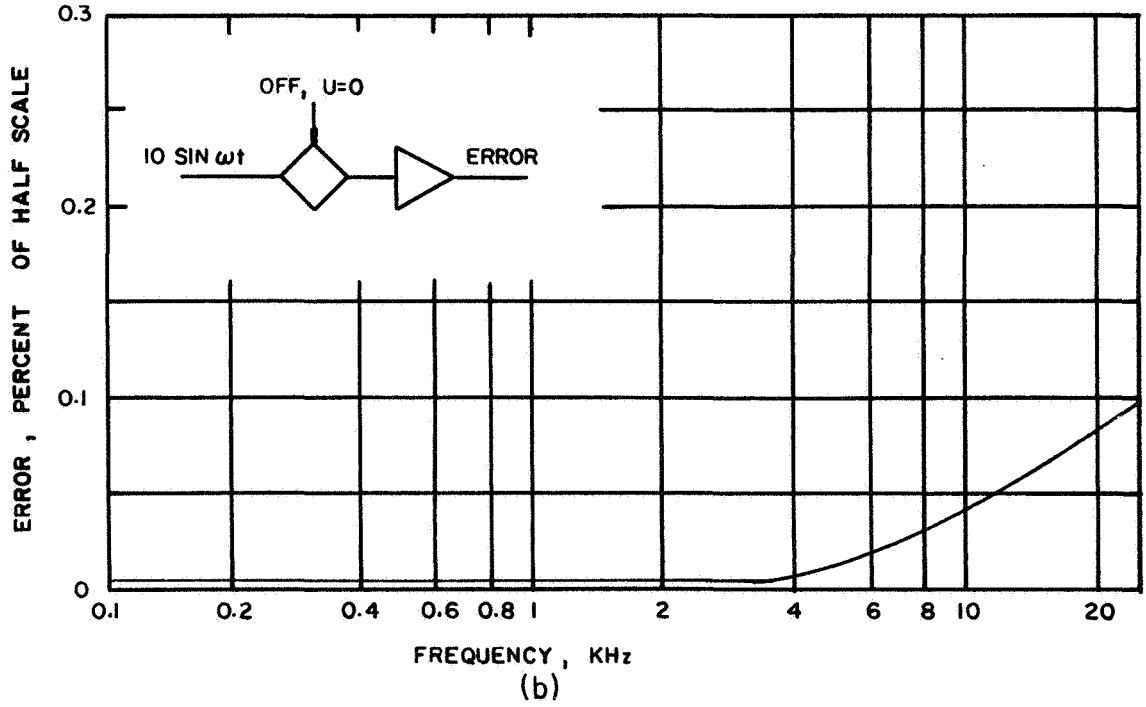


Fig. 6.3 (a) D/A Switch Dynamic Error (ON state) and (b) Feed-through Error (OFF state).

illustrates the analog performance of the switch. Switching times are 400 ns turn OFF and 600 ns turn ON.

Logic-controlled reed relay switches (Fig. 6.4) are included in each D/A switch module for use in setting up initial conditions for recursive computations in the INITIAL RESET mode, or for switching analog variables in the "slow" mode of operation.

6.3 Diode Bridge and Diode Pair

Four diode-bridges and six diode-pairs are available on the analog patchpanel for use in types of nonlinear analog setups such as precision limiters and dead-space circuits, maximum-value detectors, absolute-value circuits etc. (Korn and Korn, 1964).

6.4 Shift Register and Modulo-2 Adder

The LOCUST logic patchpanel contains twenty-four shift register stages, divided into four groups of six stages each (Fig. 6.5). Each group has a common reset, initial-condition-setting one-shot multivibrator and shift inputs. Each stage output is patched to the next to connect any number of stages as a shift register.

Shift registers are used in digital sequence generators, ring counters, switch-tail counters, pseudo-random noise generators and digital-delay networks. An individual stage can be used as a digital sample-hold and the one-shot multivibrator is often useful in other digital circuits.

Six modulo-2 adders (exclusive-OR circuits) are available for use in pseudo-random noise generator circuits for digital correlation

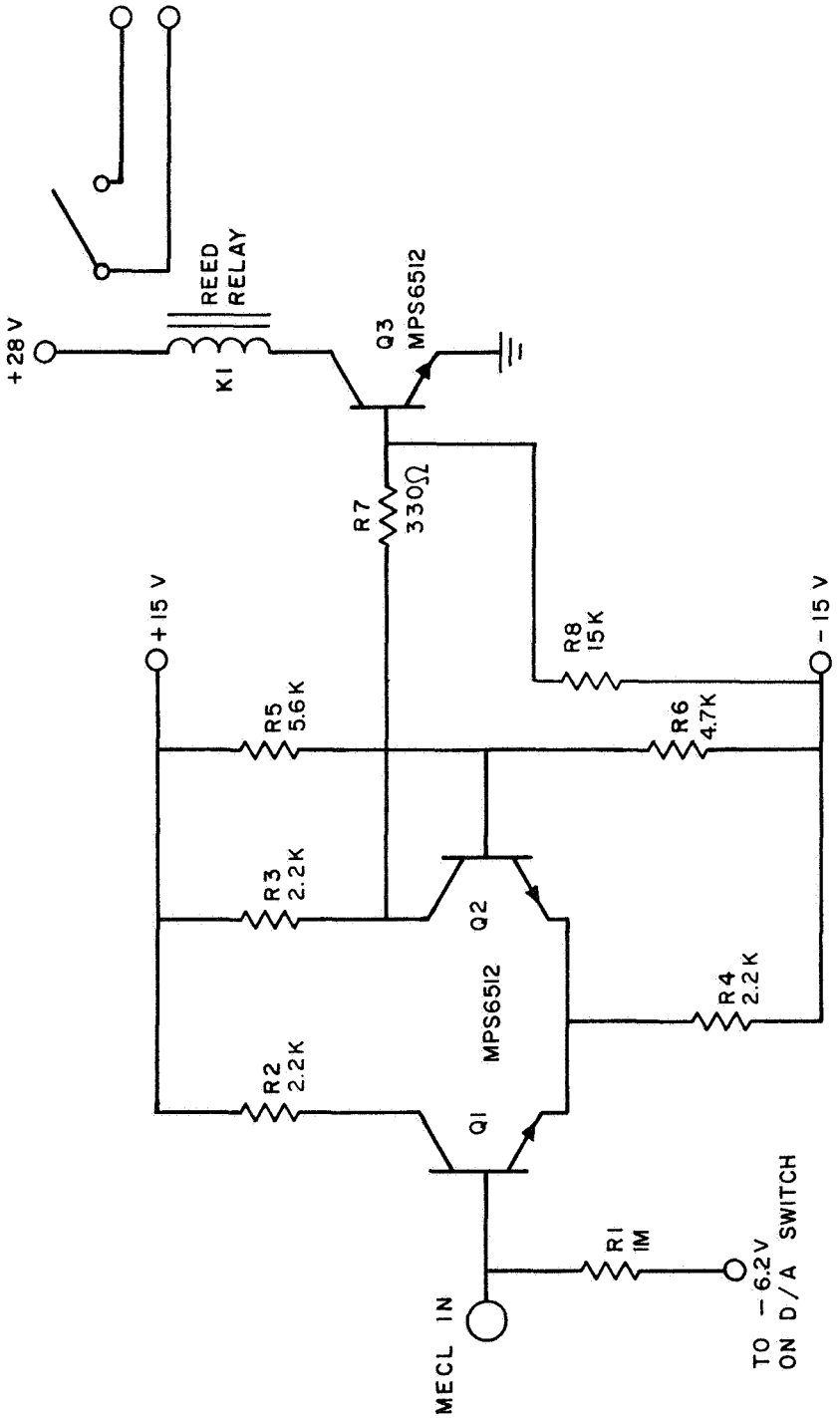


Fig. 6.4 Logic-controlled Relay Switch Schematic Diagram

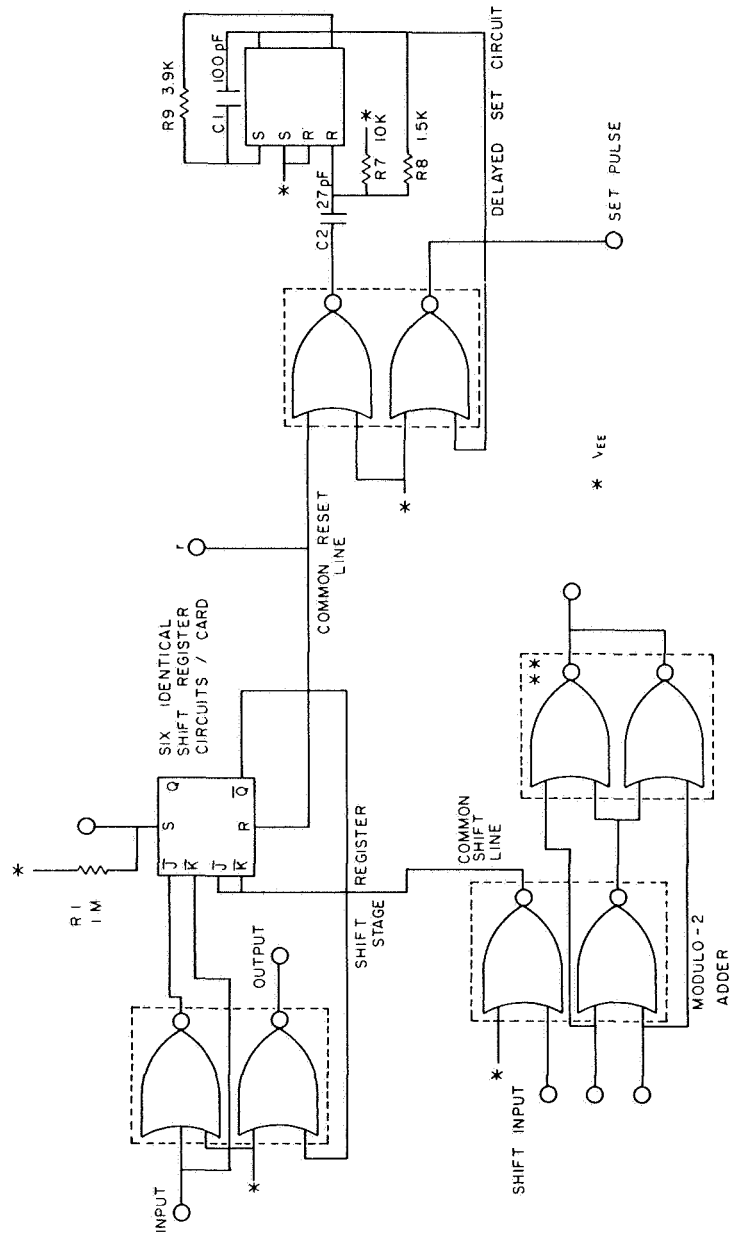


Fig. 6.5 LOCUST 6-stage Shift Register Schematic Diagram

and, of course, for performing the exclusive-OR operation. By inverting the output with a gate, one has a 1-bit digital comparator or a 1-bit multiplier.

6.5 Sampling-type Binary Noise Generator and Noise Driver

Requirements on a noise generator for analog computation are rather stringent with respect to the stability of its statistics (mean, mean square, and spectral density), and these are often difficult to control. The LOCUST binary noise generator of the type described by Kohne, Little and Soudak (1965) and is an improved version of the one used in ASTRAC II (Handler, 1967). The noise generator (Figs. 6.6 and 6.7) provides a clocked binary waveform whose statistics are essentially independent of the fluctuations in the statistics of the noise source and the drift of the Schmitt-trigger level. The key to the stability lies in the fact that flip-flop F0 has a probability of 1/2 of being either a "1" or a "0", regardless of input probability variations, when the flip-flop is sampled periodically with a sufficiently large intervening number of state changes. One has, of course, sacrificed one-half of the spectral content of the original noise source because the flip-flop divides the mean zero-crossing rate by two.

In order to use a clock frequency of 1 MHz, one requires a low-quality noise source having a flat spectrum (uncorrelated noise samples) to beyond 10 MHz so as to ensure a sufficient number of state changes between clock pulses. The noise is derived from a noise Zener diode biased near the breakdown knee of its characteristic curve. The digital logic is implemented with MECL integrated circuits.

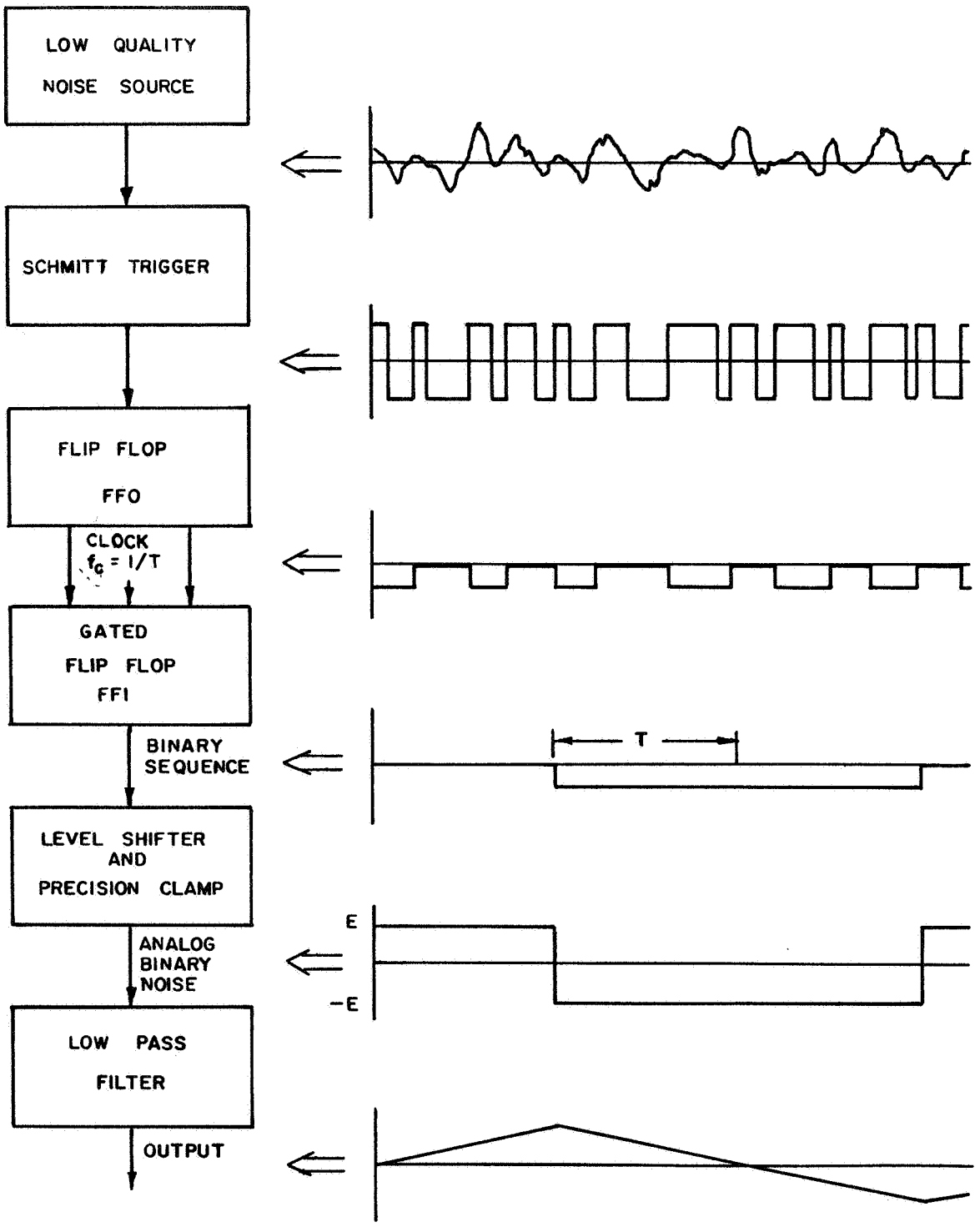


Fig. 6.6 Sampling-type Binary Random-sequence Generator

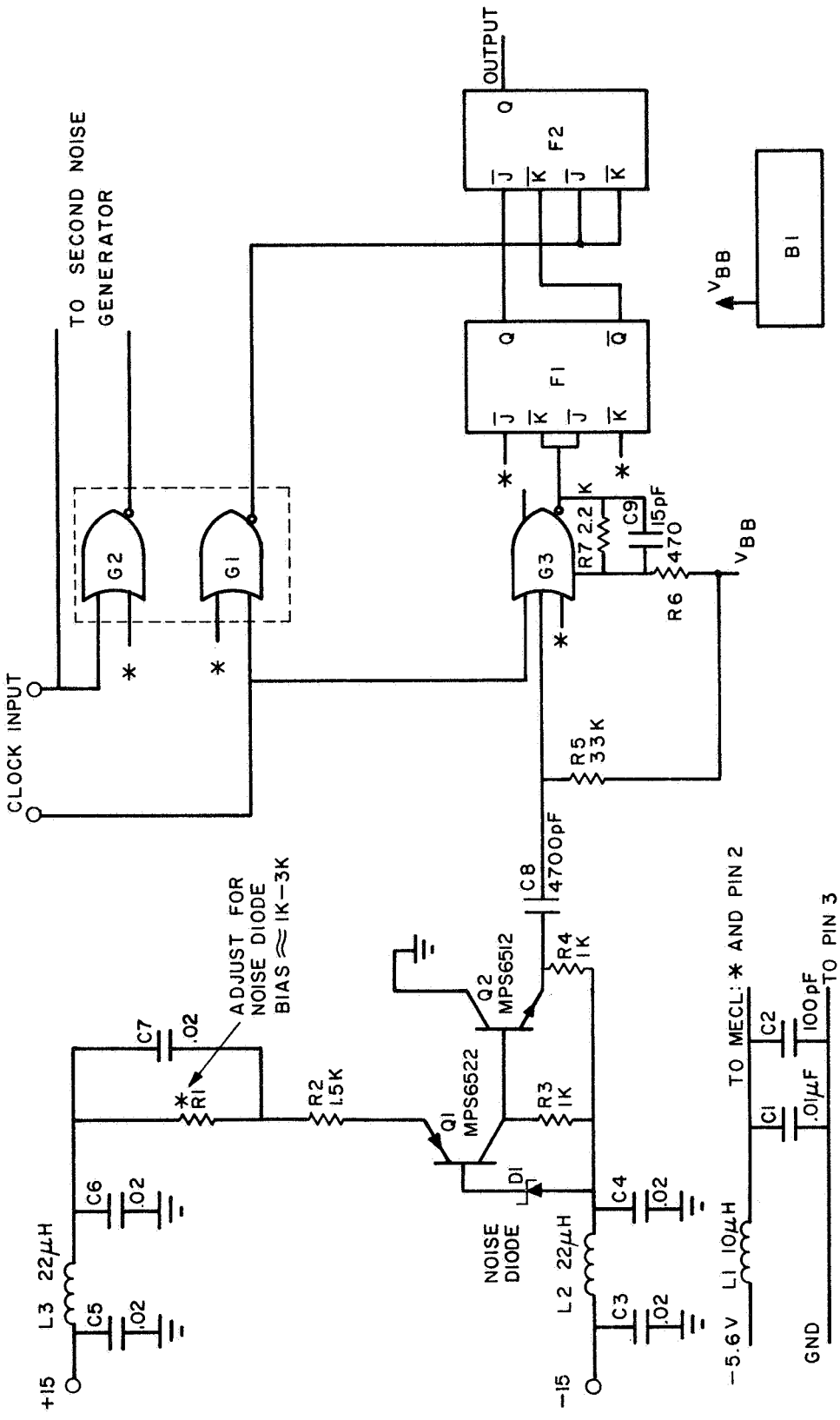


Fig. 6.7 Sampling-type Binary Random-sequence Generator Schematic Diagram

The autocorrelation function of such a noise source (Korn, 1966b) is

$$R_{YY}(\tau) = E^2\left(1 - \frac{|\tau|}{\Delta t}\right), \quad |\tau| \leq \Delta t$$

$$= 0, \quad |\tau| > \Delta t$$

The power spectral density of the noise source is then

$$G_{YY}(\omega) = \int_{-\infty}^{+\infty} R_{YY}(\tau)\, e^{-j\omega\tau}\, d\tau$$

$$= \frac{2E^2}{\Delta t}\left[\frac{1 - \cos \omega\Delta t}{\omega^2}\right]$$

$$= E^2\Delta t\left(\frac{\sin \frac{\omega\Delta t}{2}}{\frac{\omega\Delta t}{2}}\right)^2$$

By filtering the output of the binary noise source with an R-C filter whose time constant is large compared to the clock period, one may obtain approximately Gaussian noise, which is useful for many simulation experiments (Korn, 1966b).

To utilize binary noise on the analog portion of the computer, one must increase the voltage swing and provide accurate output levels. This is accomplished by a driver circuit (Fig. 6.8) which switches between the plus and minus 10-volt computer reference voltages under digital control. The drivers are housed in aluminum analog module cans and mounted on the analog patchbay. All power supply lines are CLC decoupled to reduce voltage and current spikes in power supply lines.

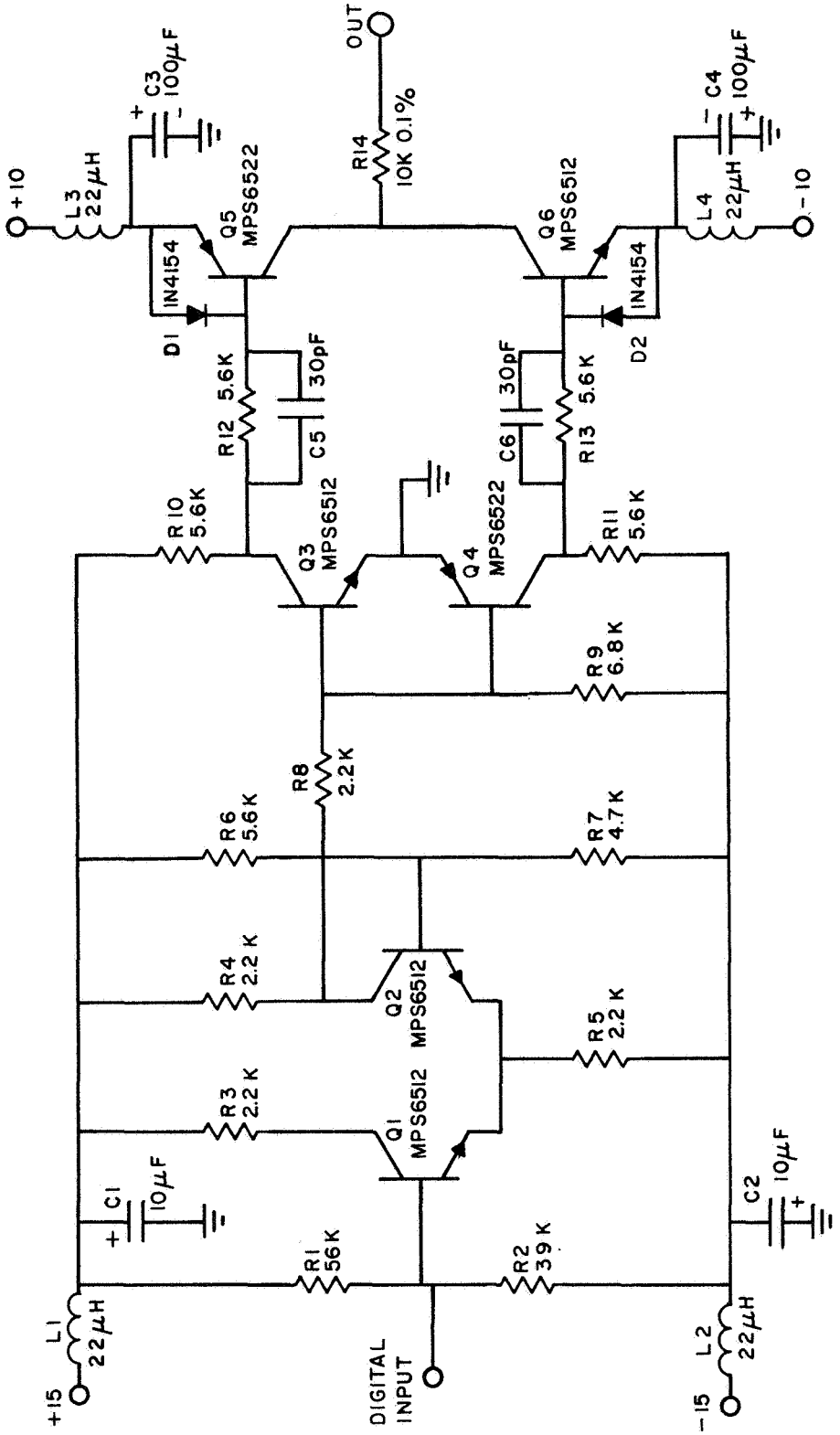


Fig. 6.8 Noise Driver Schematic Diagram

The output contains a summing resistor which is patched to the summing junction of an amplifiers; this technique protects the output transistors from an accidental short to ground while the output is being patched.

6.6 Multiplying D/A Converter

An interface element between LOCUST and the Analog/Hybrid Computer Laboratory's PDP-9 digital computer will be a 12-bit multiplying D/A converter (O'Grady, 1968). The schematic diagram of the D/A ladder network and its associated dual-shunt switches are shown in Figs. 6.9 and 6.10. A switch is connected at each A-B node on the ladder network. The ladder network is patched to a LOCUST amplifier.

The converter required both X(t) and -X(t) analog inputs and a 12-bit 2's complement digital-word input. The most significant bit (sign bit) is switched at the +X(t) input. Thus for a digital word 100 --- 0, the output is X(t) and for 011 --- 1, -X(t).

6.7 Analog-to-digital Converters

The four LOCUST A/D converters (Fig. 6.11) are of a novel type utilizing a ramp-type voltage-to-time converter implemented with LOCUST integrator/track-hold units patched on the analog patchpanel (Goltz, 1968). The output is an 11-bit 2's complement-code digital word.

A conversion begins when sampling signals, patched on the digital patchpanel, switch the switched-integrator from RESET to INTEGRATE and also gates an 8-MHz clock into an 11-bit binary counter which has been preset to 100 --- 0. An output flag signals the end of a

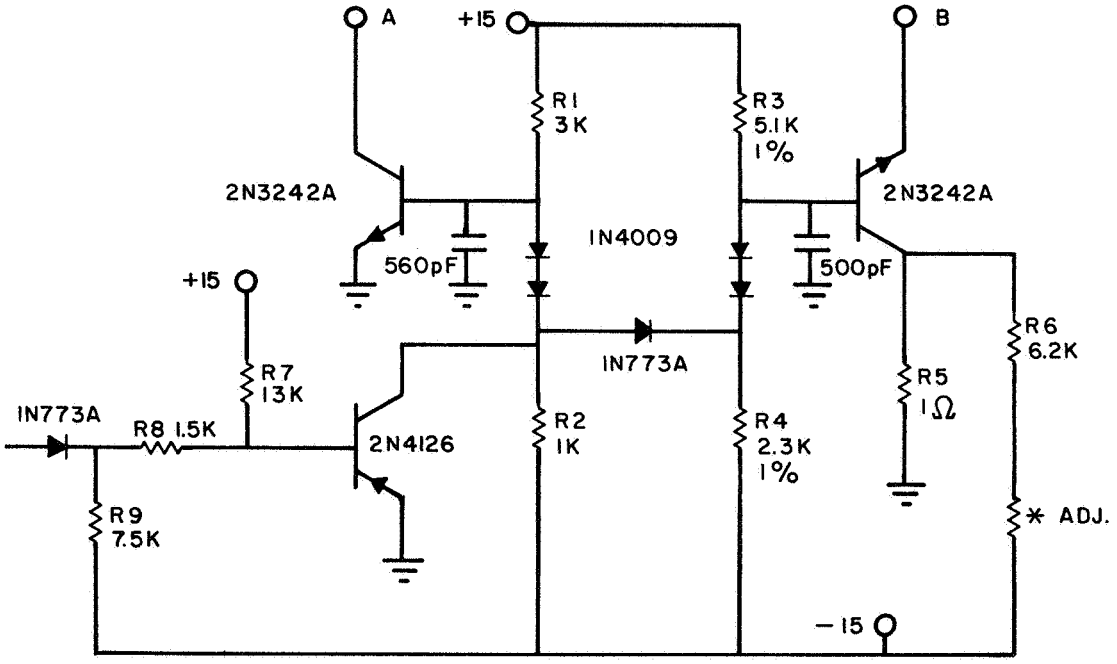


Fig. 6.9 D/A Multiplier Switch Schematic Diagram

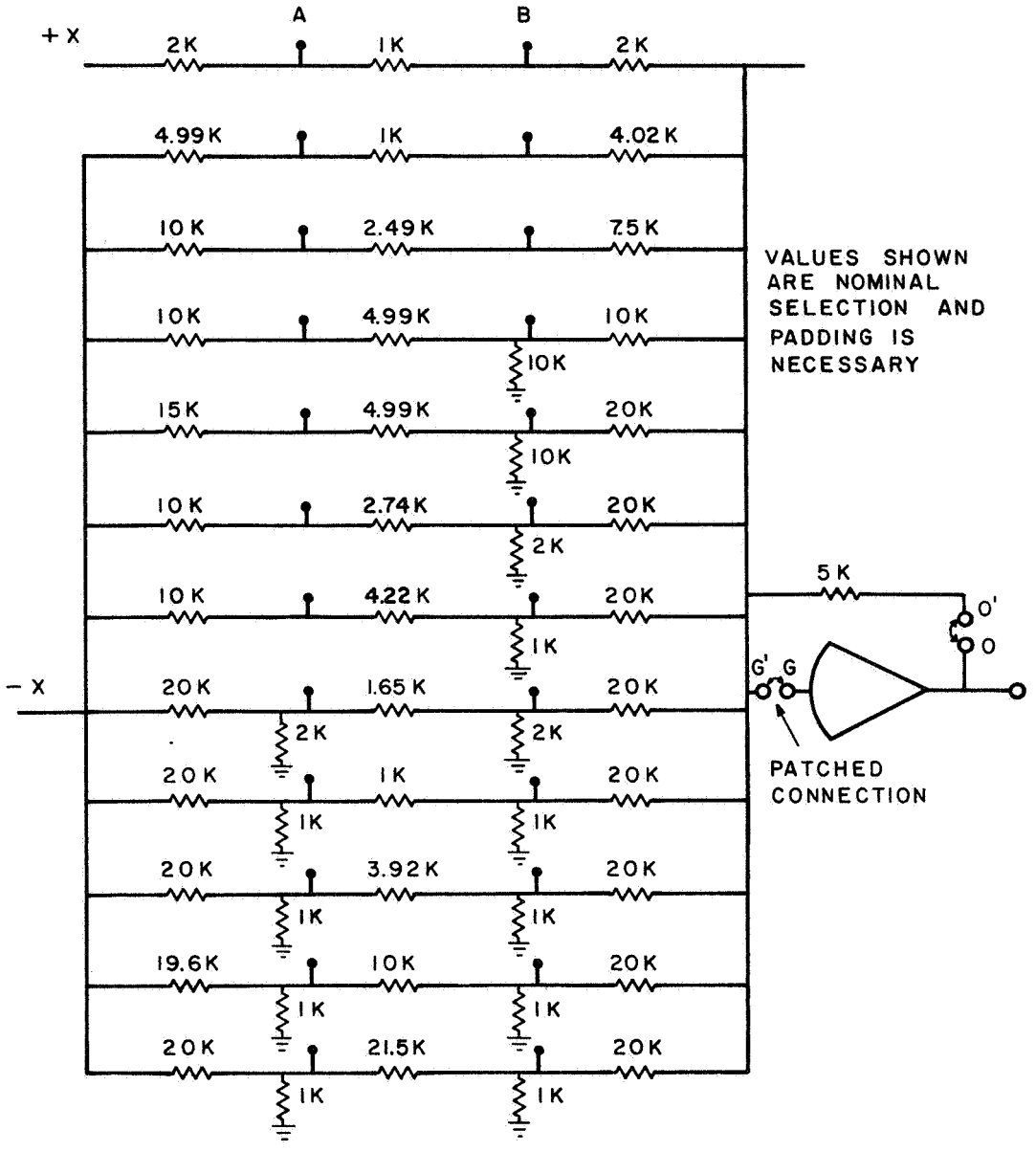


Fig. 6.10 12-bit D/A Multiplier Resistor Network

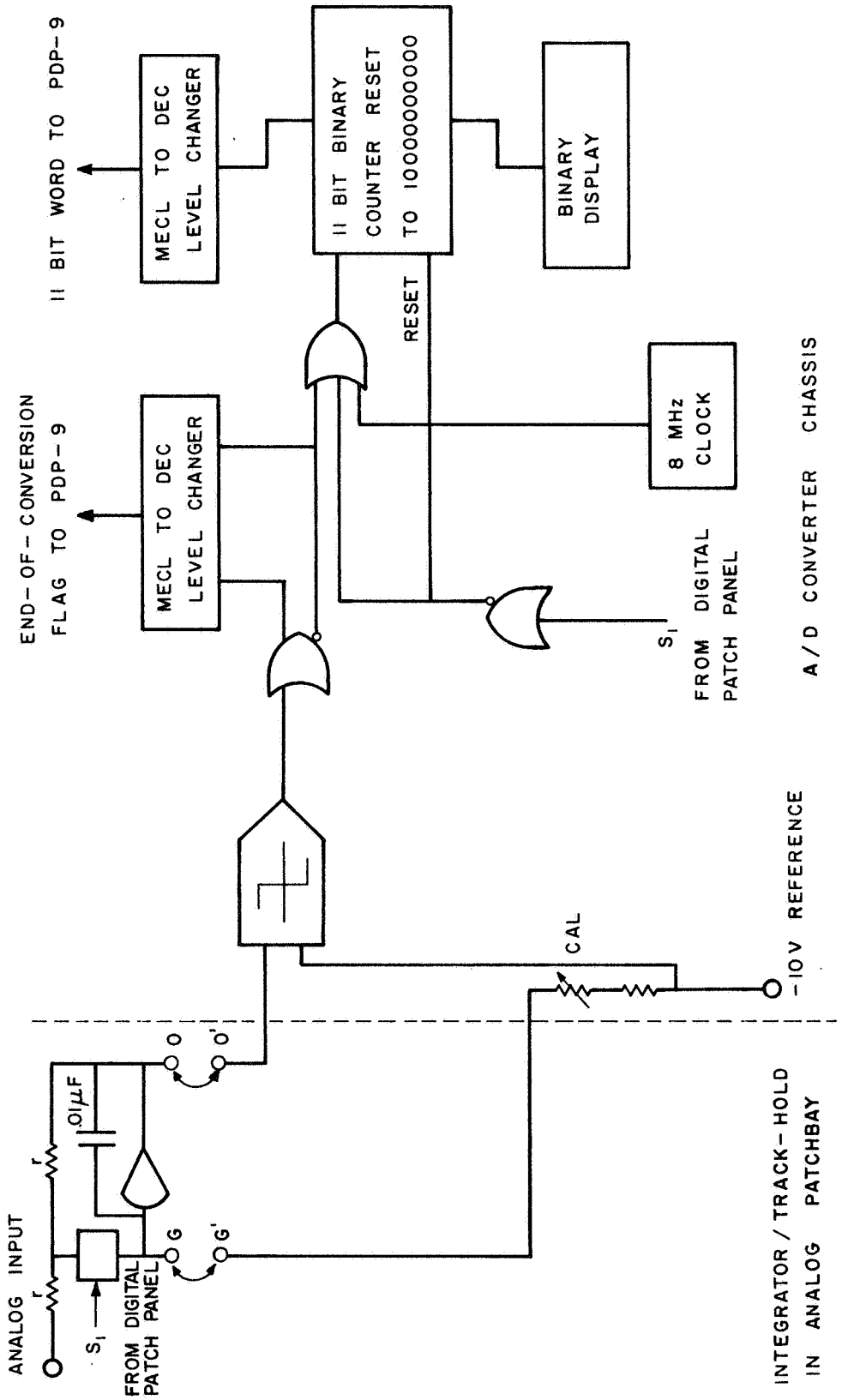


Fig. 6.11 A/D Converter Block Diagram

conversion which takes at most about 250 μs. While each individual conversion is relatively slow, this inexpensive system requires no multiplexing and becomes very advantageous if many A/D channels are needed.

Digital outputs are at the DEC logic levels (0, -3 volts) for interfacing with the PDP-9 digital computer.

6.8 LOCUST/PDP-9 Interface

The LOCUST/PDP-9 analog-digital computer interface hardware will consist of the following units in addition to the D/A multipliers and the A/D converters mentioned above:

1. Sense lines (flags) to sense logic states in the analog computer.
2. PDP-9 interrupt lines which can change the digital computer program in response to LOCUST logic signals.
3. A jam-transfer control register from the PDP-9 to set-up logic levels in LOCUST for control purposes (analog program changes, etc.).
4. Counters preset under control of the PDP-9 to act as C_1, C_2, and C_3 counters so that LOCUST sampling times and sample sizes can be controlled by the PDP-9.

Chapter 7

APPLICATIONS AND CONCLUSION

The versatility of a hybrid iterative differential analyzer system permits many new methods of problem solution. In addition, the extreme speed of differential-equation solution possible with the new wideband system itself makes previously unpractical computations (involving large numbers of computer runs) possible.

In this chapter two examples, Monte Carlo solution of a partial differential equation and automatic parameter optimization, are discussed. The chapter concludes with a summary of the improvements and features which have resulted from the LOCUST project.

7.1 Monte Carlo Solution of a Partial Differential Equation

The observation that the conditional probability density function of a Markov process satisfies a second-order elliptic or parabolic differential equation led early investigators to suggest a so-called Monte Carlo method for the solution of such partial differential equations.

If one generates a Markov process (random walk) by implementing the Langevin stochastic differential equations of motion

$$\frac{dx}{dt} = G\,N(t)$$

where $N(t)$ is white Gaussian noise with zero mean and power spectral density $2D_N$ and G is a constant (Fig. 7.1), then the corresponding

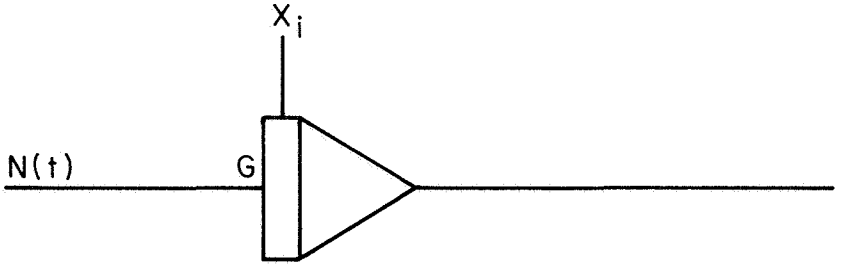


Fig. 7.1 A Markov Process Generated by Excitation of a First-order System with White Gaussian Noise

differential equation satisfied by the conditional probability density function of x, and therefore the equation which is to be solved by Monte Carlo methods is

$$G^2 D_N \frac{\partial^2 U(x,t)}{\partial y^2} = - \frac{\partial U(x,t)}{\partial t}$$

(Little, 1965).

For partial differential equations with specified boundary values (Dirichlet's problem), random walks obtained as solutions to the Langevin equations are initiated from the point X_i in space where the solution is desired. In the case of elliptical partial differential equations, the walks are continued until the boundary is crossed; then the given function value at the boundary is tallied. In the case of parabolic partial differential equations, the walks are allowed to continue for a fixed time, and then one tallies the value of the function at the boundary crossing point if indeed the boundary was crossed within the time interval allotted for the random walk; if the walk terminates before the boundary is crossed, one tallies the value of the initial condition function at that internal point where the walk is terminated. In both cases, the sample average over a suitable number of random walks will be an unbiased estimate of the solution at that point. This technique suggested many years ago has been made practical only by the development of very fast analog computing elements (Handler, 1967).

Using the LOCUST system, one can generate 2,000 random walks per second. So fast is the generation of statistics, that one may use these statistics as feedback in the simulation or control of larger

systems of which the partial differential equation solution is only a part!

The example problem set up on LOCUST is the following (Handler, 1967):

Statement of Problem: Region of Definition:

$$\partial^2 U(x,t) = \frac{\partial U(x,t)}{\partial t} \qquad 0 < x < +10$$

$$0 < t$$

$$\left.\frac{\partial U(x,t)}{\partial t}\right|_{x=0} = 0$$

$$U(10,t) = 10$$

$$U(x,0) = 0$$

Desired Solution:

$U(x,t)$ for all $0 < x < +10$ and for $t = 4$, 22, 44, and 70 seconds.

Exact Solution:

$$U(x,t) = 10 - \frac{40}{\pi}\sum_{n=1}^{\infty}\frac{(-1)^{n+1}}{2n-1}\exp\left[\frac{(2n-1)\pi}{20}\right]^2 t \cos\frac{(2n-1)\pi x}{20}$$

Langevin Equation:

$$\frac{dy}{dt} = G\,N(t) \qquad G = 10^5$$

Time Scale Factor:

$T_s = t/\tau = 7 \times 10^4$ where t is real time and τ is computer time

Sweep Speed:

0.1 volts/second

Averaging Time Constant:

1 second

Since LOCUST has binary random noise generators, it is more convenient and desirable to use binary noise rather than Gaussian noise (see Sec. 6.5). Because the input to the integrator (Fig. 7.1) is now binary with independent states, the integrator output is a binomial process. For a sufficiently large number of independent binary distributed events, the binomial distribution approaches a normal distribution. Therefore, one must choose the integrator gain so that a large number of binary noise states is required to complete each random walk (Handler, 1967).

Since the solution is to be obtained throughout the range of x, it is necessary to sweep the starting point of the random walks over its range of definition and develop Monte Carlo estimates of the solution in this range.

Figure 7.2 illustrates the hybrid-computer setup for the solution of the example problem. The output of the integrator is the random walk signal. The absolute value circuit and the comparator comprise the boundary conditions. When that voltage crosses the boundary voltage (detected by the comparator), F2 is SET thus setting up F3 so that the crossing is tallied and averaged (in the filter) during the next random walk. If the boundary is not crossed in the required time T (set by thumbwheel switches), the random walk is terminated (by $\overline{R}$ through G1

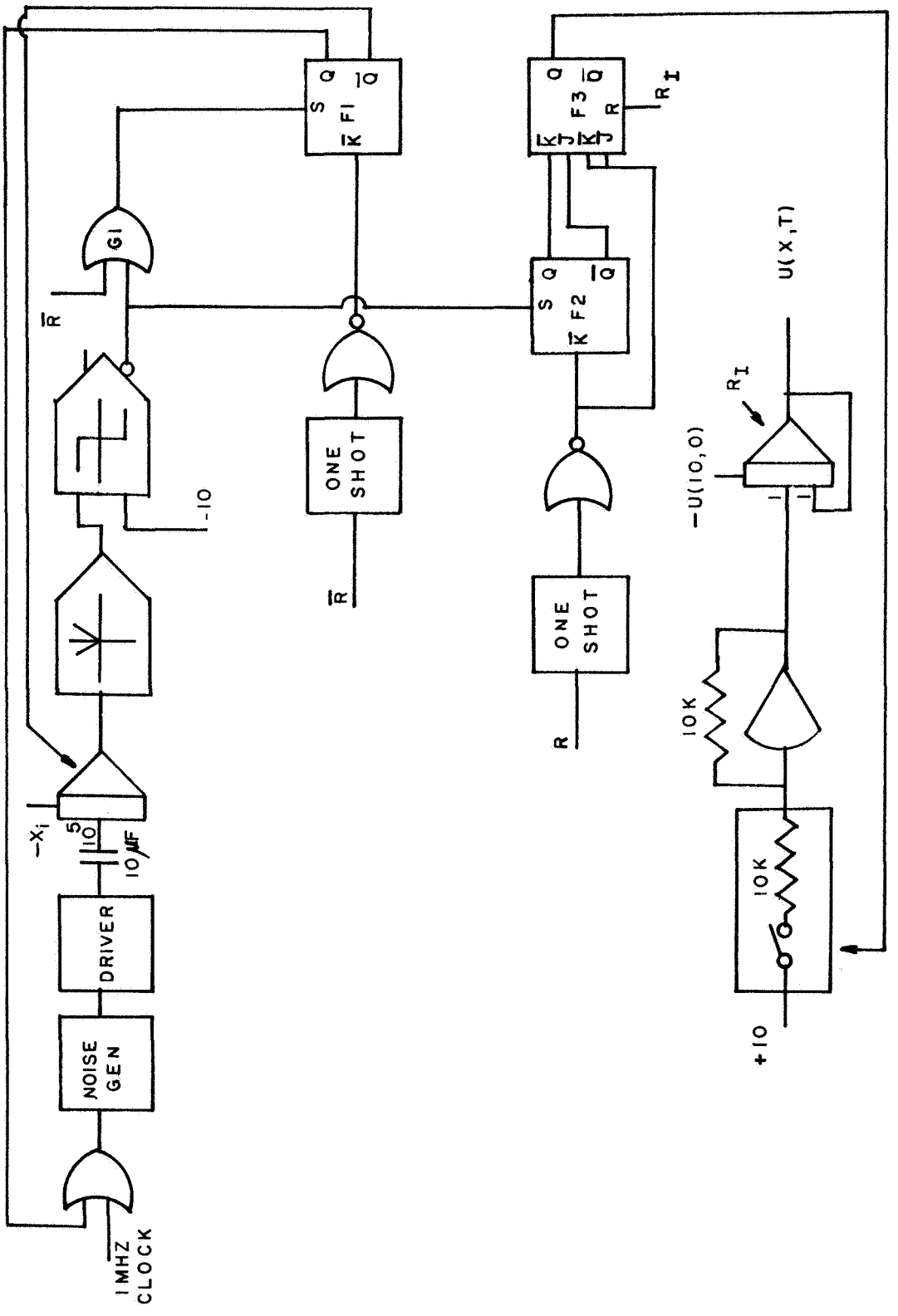


Fig. 7.2 Hybrid Computer Diagram for Monte Carlo Solution of Example Problem

and F1), and the initial function at that point (in this case zero; F2 is not SET) is tallied. At the end of the computer run, the integrator is RESET to X_i. F1 and F2 are RESET and another random walk begins.

X_i is scanned slowly enough throughout its range (0, +10) so that several thousand random walks are taken and averaged in a short interval, thus producing only small errors due to the scanning process.

The solutions are plotted in Fig. 7.3. A complete solution (one scan of x) requires about 100 seconds.

7.2 Parameter Optimization

Another important and interesting application of a high-speed iterative differential analyzer is automatic parameter optimization. The following problem is an example of an APE II experiment (Korn, 1967).

Given a system

$$\frac{d^2y}{dt^2} = -\omega^2 y \qquad \text{with } y(0) = 0,$$

determine the unknown parameter $\alpha = \dot{y}(0)$ so that $y(T) = y_T$.

This is to be accomplished by the steepest descent technique by minimizing the functional

$$F(\alpha) = \frac{1}{2}\,(y(T) - y_T)^2 \quad .$$

$F(\alpha)$ is minimized by finding the α which causes $\partial F(\alpha)/\partial\alpha$ to go to zero. If α is the output of an integrator (Fig. 7.4) its input must be driven such that

$$\frac{d\alpha}{dt} = \frac{-K\partial F(\alpha)}{\partial \alpha} \qquad K > 0.$$

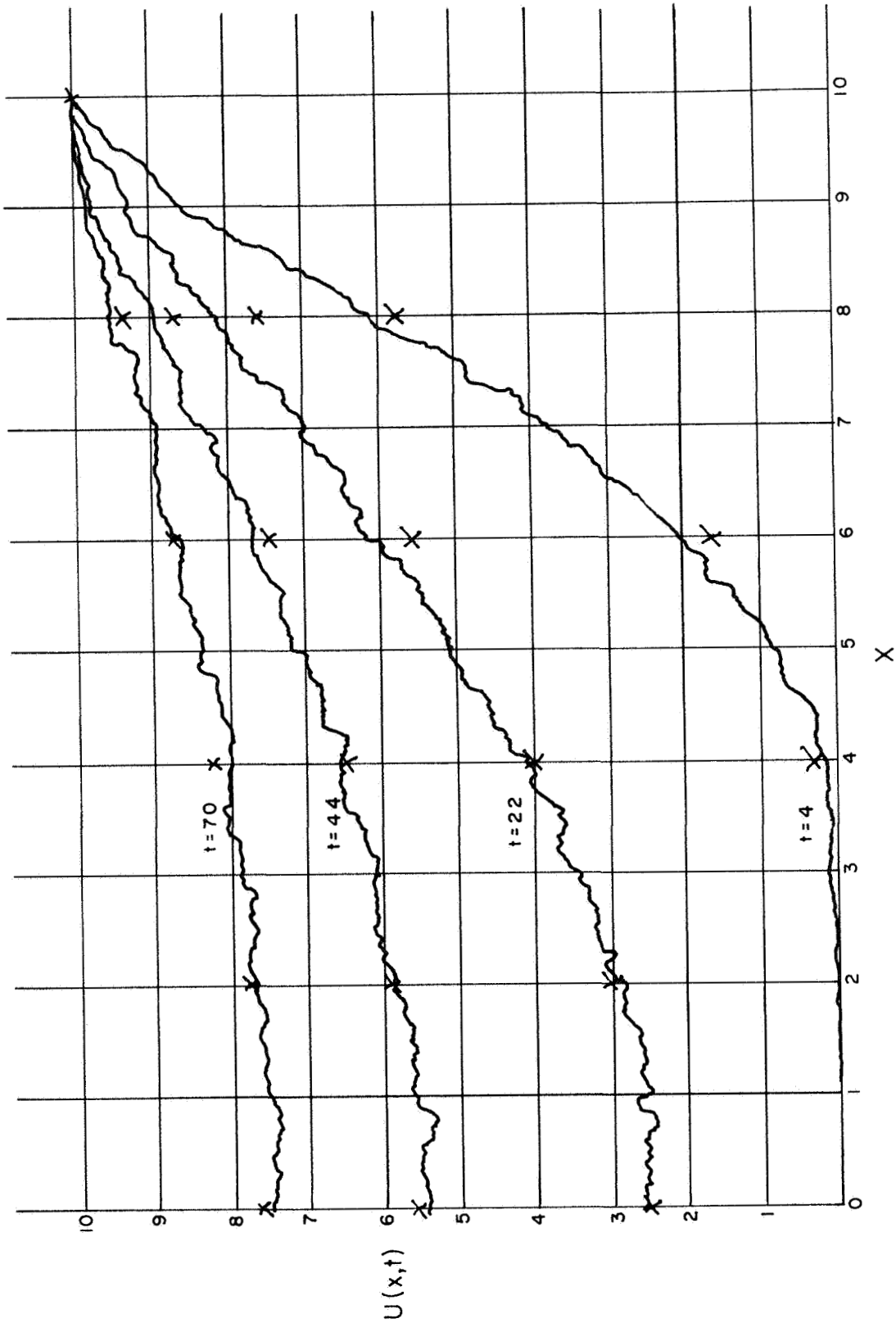


Fig. 7.3 Monte Carlo Solutions of Example Problem

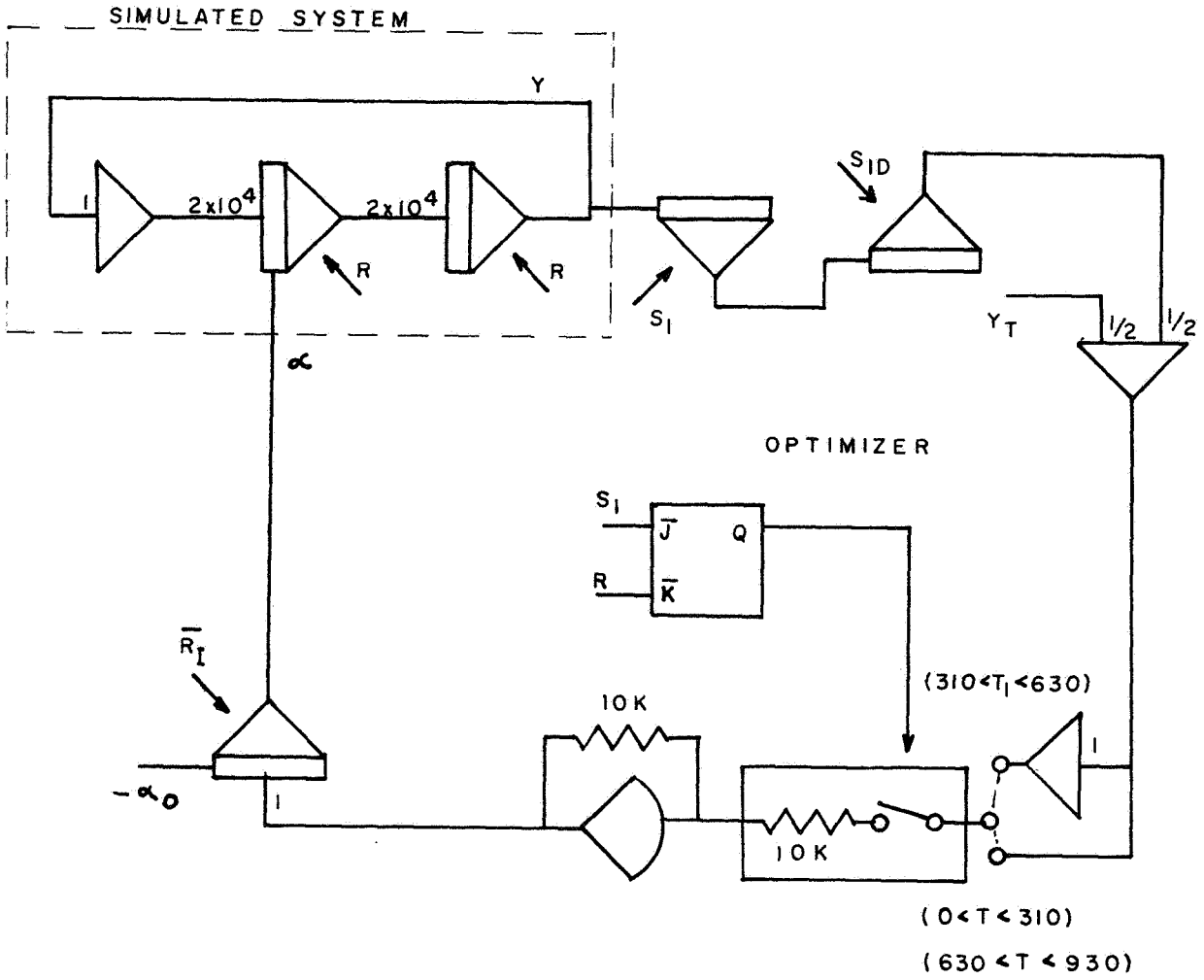


Fig. 7.4 Hybrid Computer Diagram for Parameter Optimization Problem

α will move so as to decrease F along a line of steepest descent (gradient line). F will decrease until either a minimum of F on a boundary of admissible values for α is reached or until it reaches an interior minimum with

$$\frac{\partial F(\alpha)}{\partial \alpha} = 0.$$

Now

$$\frac{\partial F(\alpha)}{\partial \alpha} = (y(T) - y_T) \frac{\partial y(t)}{\partial \dot{y}(0)} = (y(T) - y_T) \frac{\sin \omega T}{\omega} \quad ,$$

which yields the equation to be implemented for steepest descent optimization (Korn and Korn, 1964). Note that $(\sin \omega T)\omega$ can be replaced by a constant whose sign changes with T. $(\sin \omega T)/\omega$ is only a multiplying constant; giving it a permanent value of $\pm$ 1 does not affect the optimum value of α since $\partial F/\partial \alpha$ goes to zero at the optimum value.

7.3 Conclusions

The development of the LOCUST system has produced a low-cost very fast iterative differential analyzer of modest accuracy capable of implementing many sophisticated computational techniques not practical on the better known "slow" machines.

The LOCUST system incorporates new features and considerable improvements on its predecessor ASTRAC II: (1) integrated circuits have greatly reduced the cost, interconnecting wiring between digital circuits and digital noise coupled into the analog system, (2) a simple technique for mounting printed circuit cards and shielded components on low cost patchbays was developed, (3) a new simple technique for shielding low cost unshielded patchbays was developed, (4) circuit improvements in

bandwidth and switching speed, voltage and current drift and offsets have been made through the use of newer high speed transistors, field effect transistors and heated substrate differential amplifiers, (5) improved system design has produced new operating conveniences (no analog bottle plugs, automatic solution scanning, logic control of time scaling). The APE II system served as a testing ground for many of the techniques used in the LOCUST system.

Two example problems were discussed which demonstrated the versatility and usefulness of the LOCUST system for high speed iterative computation.

Appendix

LOCUST INSTRUCTION MANUAL

LOCUST, an all-solid-state iterative differential analyzer making maximum use of integrated circuits, employs ± 10-V, 30-mA amplifiers with 30 MHz unity-gain bandwidth and can operate at iteration rates as high as 2,000 analog computer runs per second as well as in real time. Computing elements are plugged directly into the rear of a modified inexpensive patchbay which has removable patchboards. The novel analog patchbay arrangement is uncluttered because the LOCUST system requires virtually no bottle-plug control of amplifier operation. Subroutines can be automatically controlled by a flexible digital control unit as well as by patched digital logic or by an associated digital computer. Low-level current-mode integrated-circuit logic has virtually eliminated digital noise coupling into the analog portion of the computer.

I. COMPUTER CONTROL

Mode Control Panel

The mode control panel (Fig. A.1) bears lighted push-button mode switches color-coded for easy identification. The control logic is designed so that the control buttons may be safely depressed in any sequence without damage to the computer (Fig. A.2).

POWER OFF (green)

When the POWER OFF button is illuminated, power is only supplied to the power-off-button light; this gives a positive indication

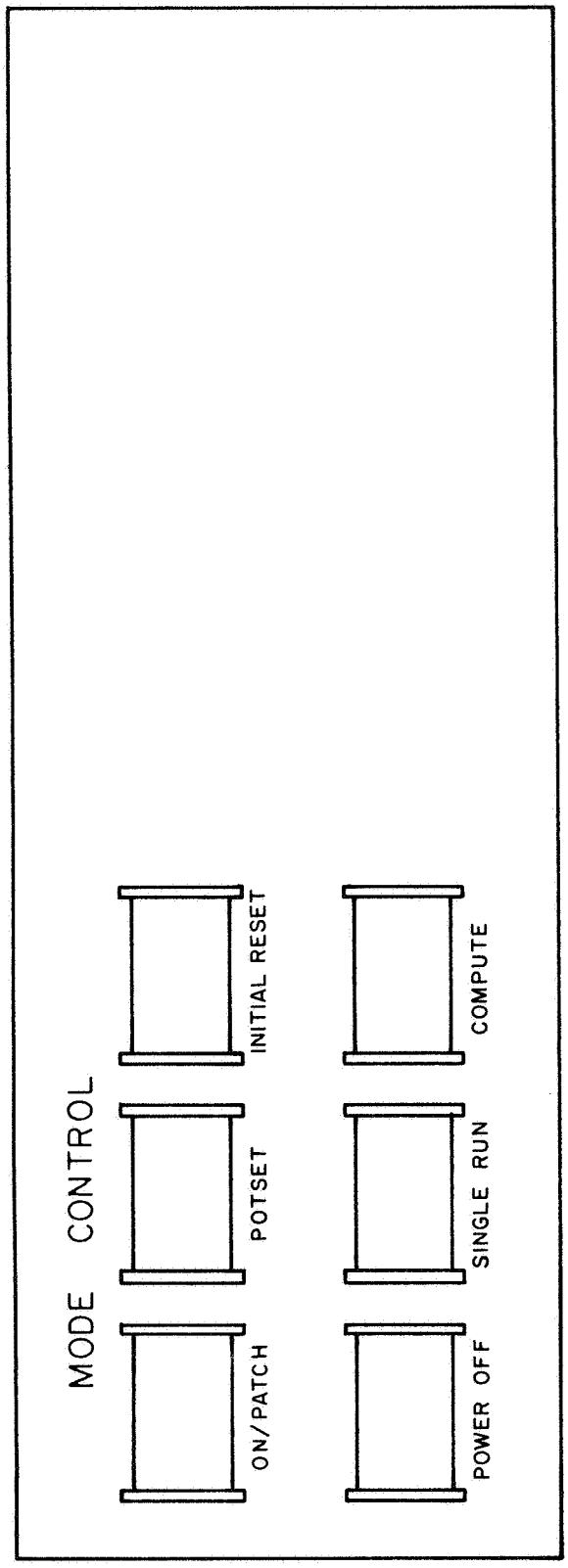


Fig. A.1 LOCUST Mode Control Panel

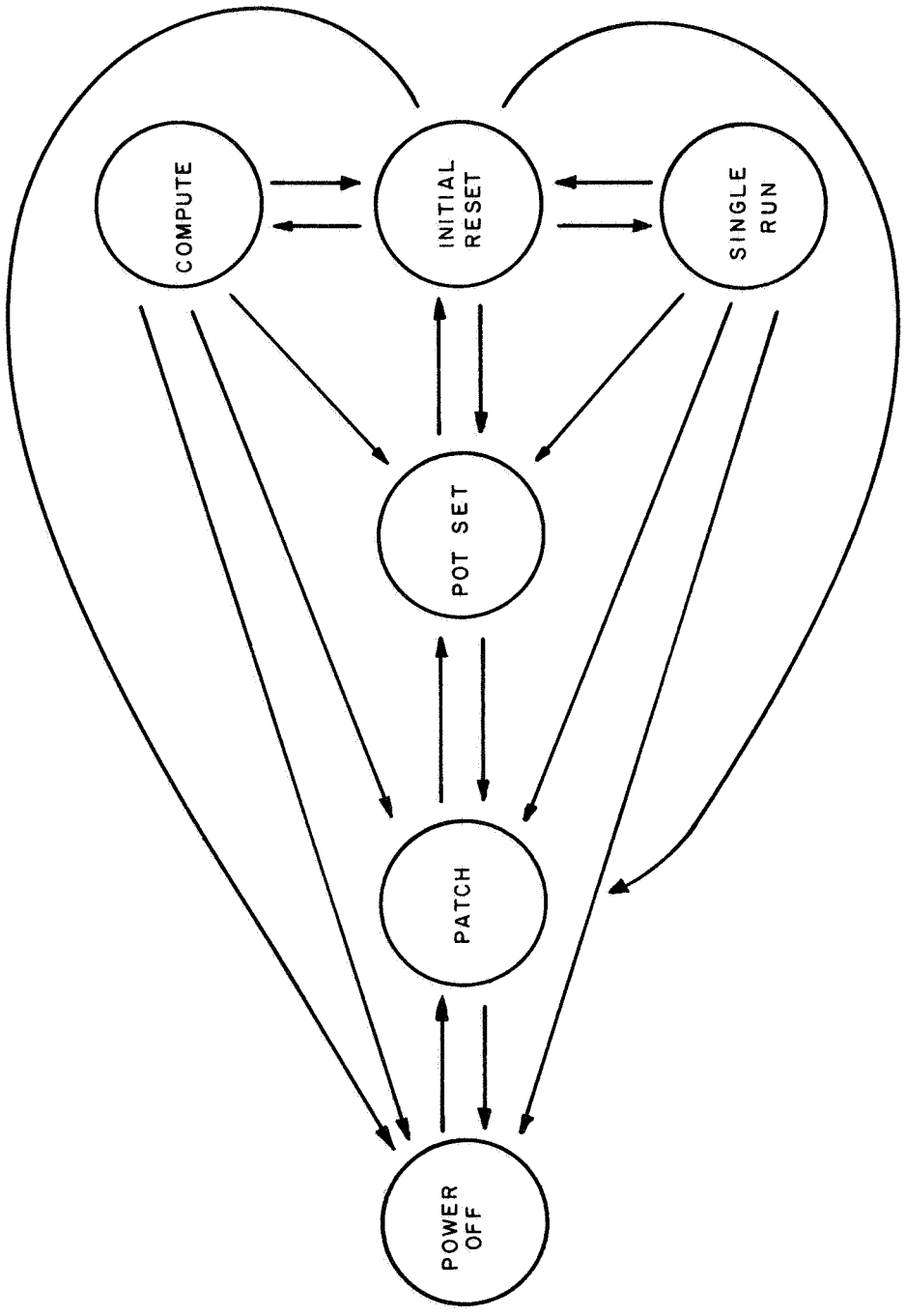


Fig. A.2 Mode Control Logic State Diagram

that all power supplies are OFF. The computer can be switched into this mode from any other computer mode.

ON/PATCH (red)

In the ON/PATCH mode, a-c power is supplied to the analog power supplies, digital equipment, DVM, scope, fans, and the external outlets but not to the analog computing elements or patchbay ± 10-V terminals. Switching to this mode can be accomplished directly from any other computer mode. The computer must be patched in this mode or in the POWER OFF mode.

POTSET (blue)

The digital voltmeter (DVM) is connected to the potentiometer readout bus. In addition to those units powered in the ON/PATCH mode, the analog computing elements are supplied ± 15-V power. Coefficient potentiometers are set in this mode. Amplifier overload lights are not enabled in this mode. Switching to this mode can be accomplished directly from all other modes except POWER OFF.

INITIAL RESET (white)

The DVM is connected to the analog patchbay DVM point (VM), and all computer units receive power, including the ± 10-V reference voltage points on the patchbay. The amplifier overload lights are enabled in this mode; to reset them, depress the INITIAL RESET button for about one-half second or, switch to POTSET. Switching to INITIAL RESET can be accomplished directly from all other modes except POWER OFF. The computer also may be put

in INITIAL RESET by a logical "1" applied to EXT. IR on the digital patchpanel (Fig. A.15, p. 148). The logic state of the computer control signals in INITIAL RESET are shown in Fig. A.3.

COMPUTE (red)

To start iterative computation depress and release the COMPUTE button when the computer is in the INITIAL RESET, COMPUTE or SINGLE RUN modes, or apply a logical "1" to EXT. CP on the digital patchpanel. Amplifier overload lights are enabled in this mode; to reset them, depress the COMPUTE button for about one-half second or switch to INITIAL RESET or POTSET.

SINGLE RUN (yellow)

To operate the digital control module through one cycle of the computer reset pulse R, push the SINGLE RUN button or apply a positive logic transition (dynamic "1") to the EXT. SR point on the digital patchbay. Each time the SINGLE RUN button is depressed an additional run occurs. One can switch to SINGLE RUN only from INITIAL RESET.

Power Panel

The power panel contains pushbutton switches which connect the DVM to the $\pm$ 15-V and $\pm$ 10-V power supplies for readout in the POTSET mode. BALANCE meters are provided for balancing and monitoring the difference between the plus and minus 15-V and plus and minus 10-V supplies. The power supplies are set periodically by a technician and should not be adjusted by the operator.

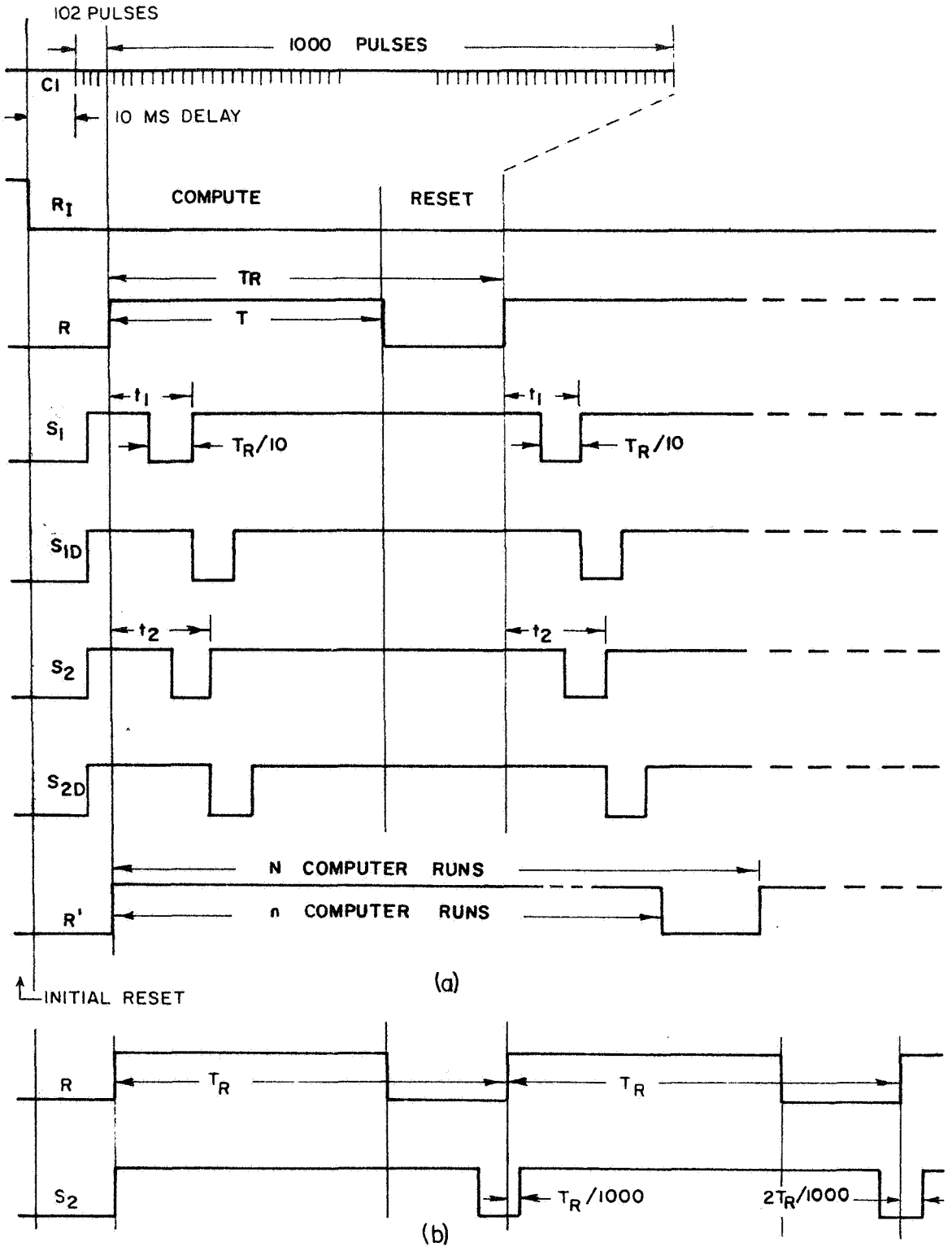


Fig. A.3 (a) Timing and Control Signals for Normal Repetitive Operation and (b) Control Signals for SCAN 1 Operation

Overload Lights and Limiters - When the output voltage of an integrator/track-hold computing element or a summing amplifier (in INITIAL RESET, COMPUTE or SINGLE RUN modes) exceeds the ± 10-V computing range slightly, a latching circuit is triggered; this turns on an overload light located above the analog patchpanel, and a logic "1" appears on the digital patchpanel terminal OL (in the COMPUTE and SINGLE RUN modes). To reset the overload lights, depress the INITIAL RESET or COMPUTE buttons for about one-half second. PATCH and POTSET also reset the overload lights.

Integrator/track-hold computing elements and the four uncommitted summing amplifiers have high speed limiter circuits limiting the output to about ± 10.5 volts. These are required in applications where quick recovery from overload is necessary, such as in A/D converter operation.

Digital Control Module

The Digital Control Module (Fig. A.4) produces the control signals for repetitive computer operation. The module comprises the clock-pulse generator, master timer, auxiliary timer and the subroutine counter (Fig. A.5).

The digital logic is Motorola Emitter-coupled Logic (MECL). A logical "0" corresponds to approximately -1.55 volts, and a logical "1" to approximately -0.75 volts. These levels may be slightly different in LOCUST. The d-c fanout of a MECL output is 25 unit loads (a gate input is one unit load, a flip-flop dynamic input is 1.5 unit loads). There should be no d-c loading problems on the digital patchpanel. When driving several dynamic (a-c) inputs, it may be necessary to separate

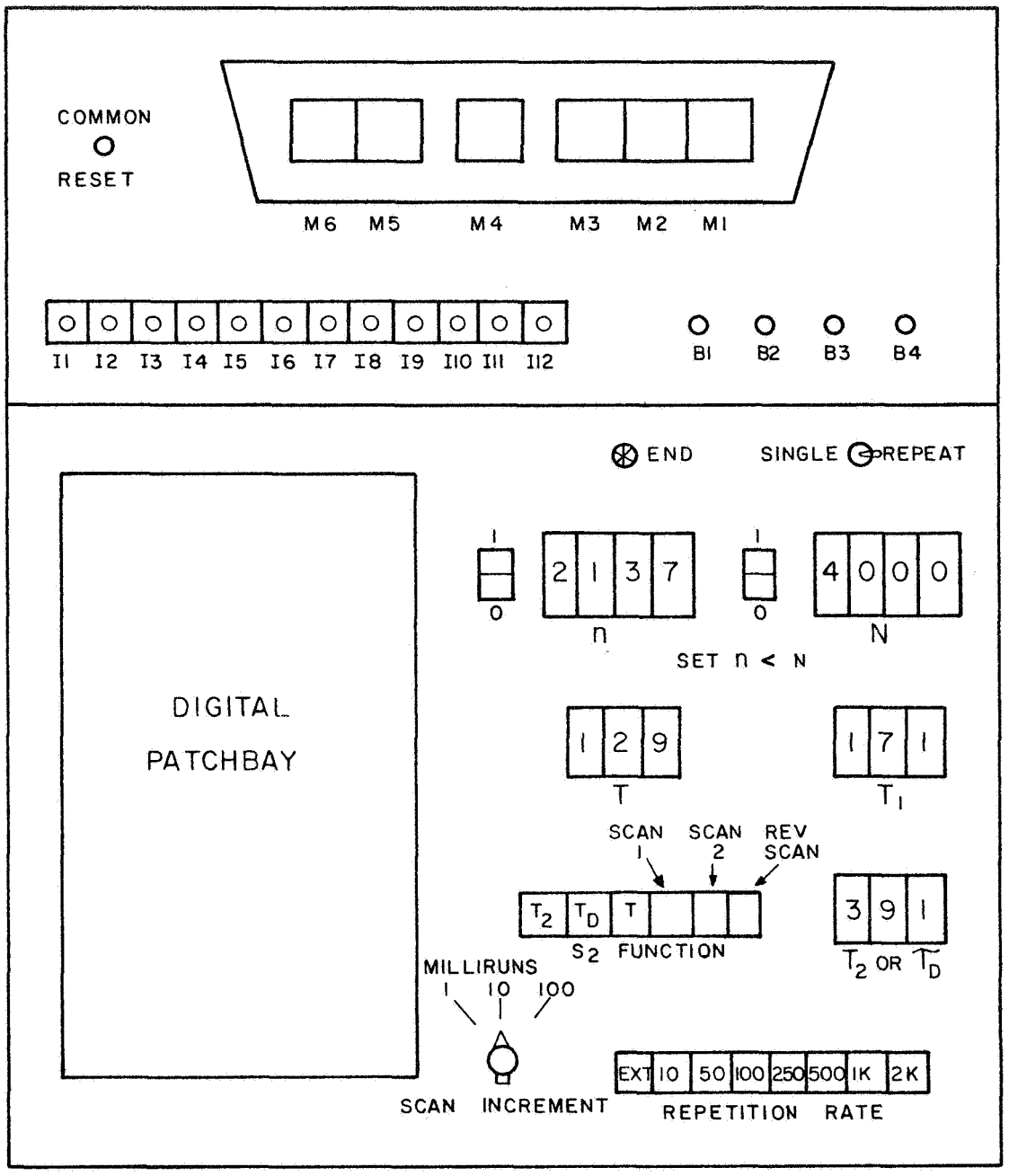


Fig. A.4 LOCUST Digital Control Module

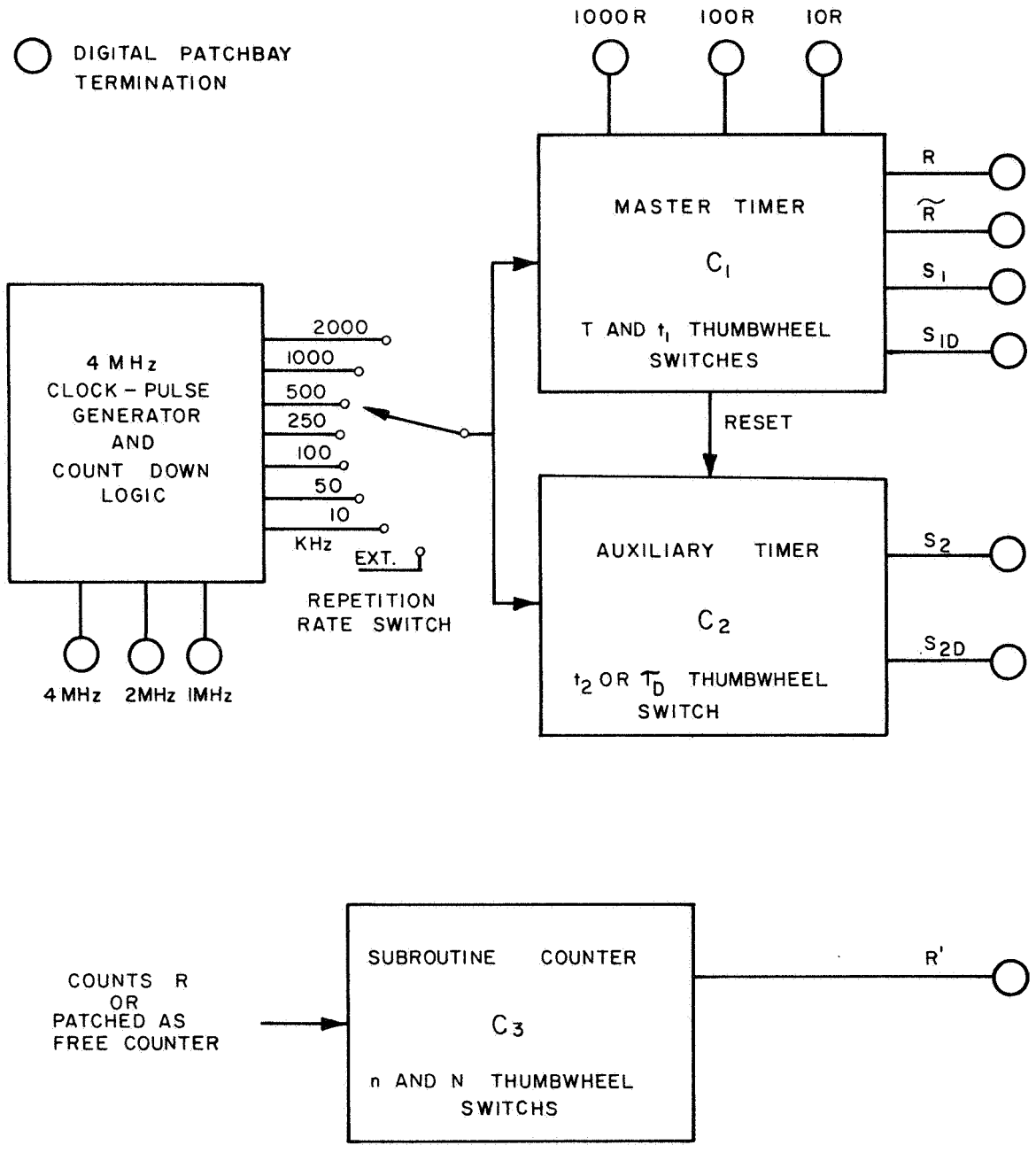


Fig. A.5 Simplified Block Diagram of LOCUST Digital Control Timers

the load by using gates as drivers to preserve the fast rise-time needed for proper operation.

Clock Pulse Generator - The generator (Fig. A.5) starts with a 4 MHz crystal clock and counts down to obtain timing pulses of 4 MHz, 2 MHz and 1 MHz (available on the digital patchbay; Fig. A.16, p. 150) 500 kHz, 250 kHz, 100 kHz, 50 kHz and 10 kHz. The repetition rate selector switch selects the desired clock rate, which is 1,000 times the computer repetition rate (2,000, 1,000, 500, 250, 100, 50 and 10 computer runs per second) or selects an external clock input (EXT.C1 on the digital patch panel; Fig. A. 15, p. 148). All further timing is performed in terms of these pulses (1,000 per computer run) whose duration is called 1 millirun = (T_R/1,000) seconds.

Master Timer - The master timer (C_1 counter) is a three-decade dual-preset decimal counter designed to perform the following timing functions:

1. It counts down by 1,000 to mark the start of periodic COMPUTE periods [Fig. A.3(a)].
2. It produces timing markers at 10 times (10R), 100 times (100R) and 1,000 times (1,000R, the C1 pulse rate) the computer repetition rate.
3. Thumbwheel decade switches allow the operator to select the event times t = T and t = T_1 milliruns after the start of each COMPUTE period with a resolution of 1 millirun [Fig. A.3(a)].

In normal repetitive operation COMPUTE periods of length T milliruns alternate with RESET periods of length (1,000 - T) milliruns. The thumbwheel switch T_1 feeds a timing-logic block to produce periodic sample-hold control pulses S_1 and delayed pulses S_{1D} of length $T_R/10$ seconds = 100 milliruns. A track-hold circuit controlled by S_1 will periodically TRACK for 100 milliruns and switch into HOLD at t_1 milliruns. S_{1D} occurs 100 milliruns later than S_1 [Fig. A.3(a)].

A logical "1" applied to terminal EXT.R on the digital patch-panel (Fig. A.15, p. 148) resets the C_1 (and C_2) counter and triggers a fixed RESET period of 102 milliruns; the T thumbwheel switch controls the COMPUTE period length.

Auxiliary Timer - The auxiliary timer (C_2 counter) is a three-decade single-preset decimal counter. The S_2 function switch controls the operation of the C_2 counter and its associated logic. For the S_2 function switch settings the thumbwheel switch "T_2 or τ_D" functions as follows:

1. T_2 position - The trailing edge of S_2 (TRACK to HOLD) occurs at t_2 milliruns after the start of the COMPUTE period.
2. T_D position - The trailing edge of S_2 occurs at $t_1 + \tau_D$ milliruns after the start of the COMPUTE period. Note that in this position the "T_2 or τ_D" thumbwheel switch sets the interval between the S_1 and the S_2 pulses.
3. T position - The trailing edge of S_2 occurs at $T + t_2$ milliruns after the start of the COMPUTE period. S_2 and S_{2D} then serve

for readout during the REST period as S_1 and S_{1D} serve during the COMPUTE period.

4. SCAN 1 position - On the first run the trailing edge of S_2 occurs at t_2 milliruns; on the second it occurs at t_2 + M milliruns (M is selected by the scan increment switch); on the third, at t_2 + 2M milliruns, etc. [Fig. A.3(b)]. Track-hold circuits controlled by S_2 and S_{2D} will then "scan" periodic repetitive-computer solutions once every 1,000/M computer runs for readout into slow recorders. With the repetition rate selector set at 100 and M set at 1, for instance, a complete solution scan requires 10 seconds.
5. SCAN 2 position - The auxiliary timer (C_3 counter) permits the scanning pulse to step forward by M milliruns only after a preset number N of events (usually computer runs). Note that n must be set at a smaller number than N on the subroutine counter thumbwheel switches.
6. REVERSE SCAN position - On the first run, after the START button is pushed, the trailing edge of S_2 occurs at t_2 milliruns; on the second run, it occurs at t_2 - M milliruns and continues to scan backwards in steps of M milliruns.

Scan Increment Selector - This switch selects the scan increment 1, 10 or 100 milliruns. In SCAN 1 and REV. SCAN the scan rate is M milliruns per run. In SCAN 2 the scan rate is M milliruns per N runs.

Subroutine Counter - The subroutine counter C_3 is a dual-preset 4-decade computer which counts computer runs. It may also be patched as a free counter. C_3 produces R' a digital signal whose state depends on the n and N thumbwheel switch settings [Fig. A.3(a)]. C_3 is reset in the INITIAL RESET mode or may be reset by applying a logical "1" to R3 on the digital patchpanel (Fig. A.16, p. 150).

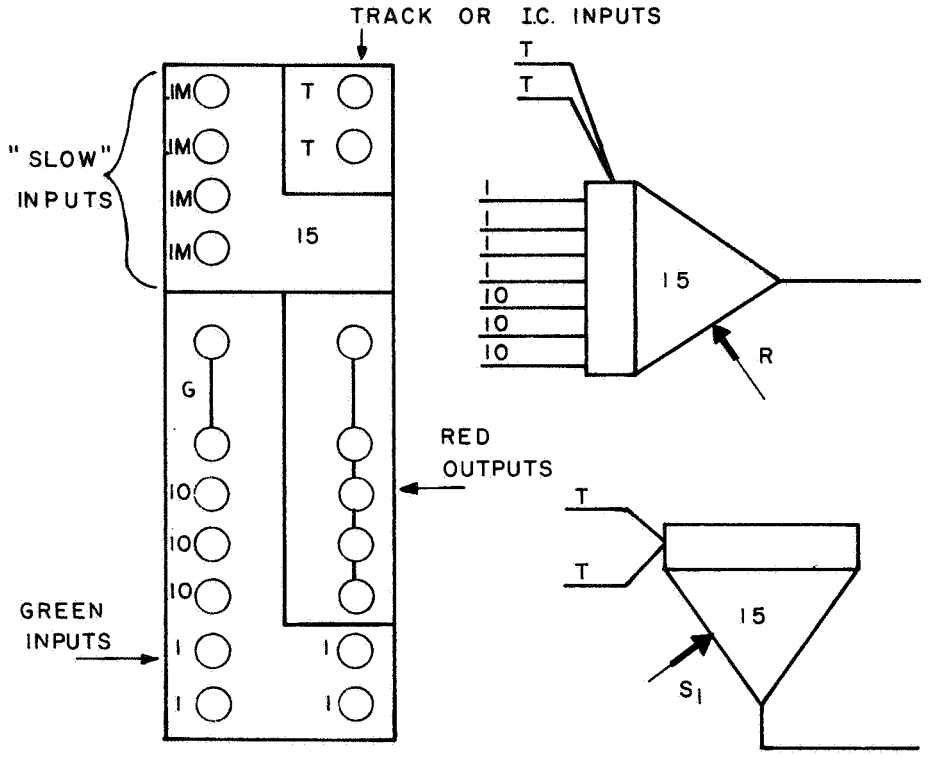
To use C_3 as an uncommitted counter, apply a logical "1" to G3 (a "1" is conveniently available to the right of G3) and apply the input signal ("0" to "1" transitions) to T3. R' will always be set to "1" at the beginning of the first computer run no matter how it is used. In the uncommitted mode, one must not have an input pulse occur within 150 ns after the beginning of the first computer run. If one does, the pulse will not be counted.

The "END" light turns on when R' is "0" (i.e., at the end of the subroutine COMPUTE period, n). For proper operation be sure to set N to a greater number than n.

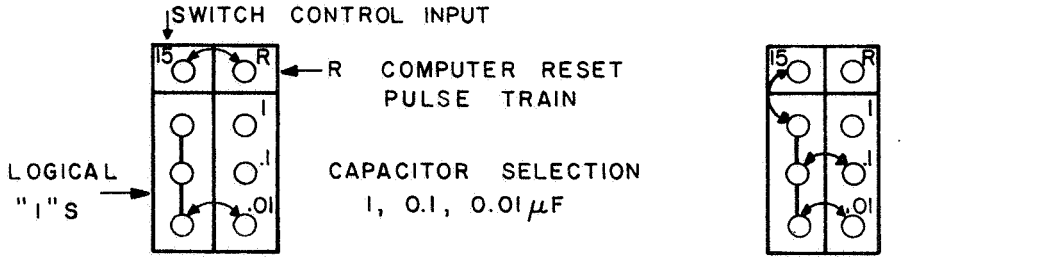
II. COMPUTER PATCHING

The computer must be patched only in the POWER OFF or ON/PATCH modes. Patching in any other mode may cause damage to the computing elements.

Integrator/Track-Hold Patching - Figure A.6(a) illustrates the analog and digital patch-fields associated with an integrator/track-hold computing element. No patching connections are necessary on the analog patchpanel to implement integrator, track-hold or summing amplifier operation. Digital patching for the above modes is illustrated in



(a)



NORMAL OPERATION AS A TRACK/HOLD OR A SWITCHED INTEGRATOR

OPERATION AS A SUMMING AMPLIFIER. "SLOW" INPUTS ARE NOT CONNECTED

(b)

Fig. A.6 (a) Integrator/Track-hold Patchfields
(b) Digital Patchpanel Patching

Fig. A.6(b). The digital control signal is connected to the upper left hole of the patching field. The computer reset pulse R is conveniently available in each field, so that a bottle plug may be used. Other signals require a patchcord. Note that three bottle plug connections are necessary for operation as a summing amplifier.

Selection of integrator/track-hold feedback networks is performed in the patchfield associated with each integrator/track-hold computing element. Selection holes are labeled 1, .1 and .01 for 1, 0.1 and 0.01 μF capacitors. By patching a logical "1" to one of these terminals the corresponding capacitor is placed in the feedback network of the associated amplifier. Logical "1"'s are conveniently located to permit the use of a bottle plug. When a 0.1 or 1 μF capacitor is patched, the "slow" summing network (Fig. A.7) is connected to permit slow (real time) integration. Calculate the integrator gain by referring to Fig. A.7.

If no capacitor is selected by patching on the digital patchpanel, the capacitors are selected by the repetition rate selector as follows:

0.01 μF for 2K, 1K and 500 runs per second

0.1 μF for 250, 100 and 50 runs per second

1.0 μF for 10 and EXT. runs per second.

The integrator/track-hold circuit is in COMPUTE (HOLD) when its control input is "1" and in RESET (TRACK) when it is "0". The circuit is unstable in TRACK when patched as a summing amplifier and so cannot be used as a switched amplifier. All integrator/track-hold circuits have limiters and overload lights.

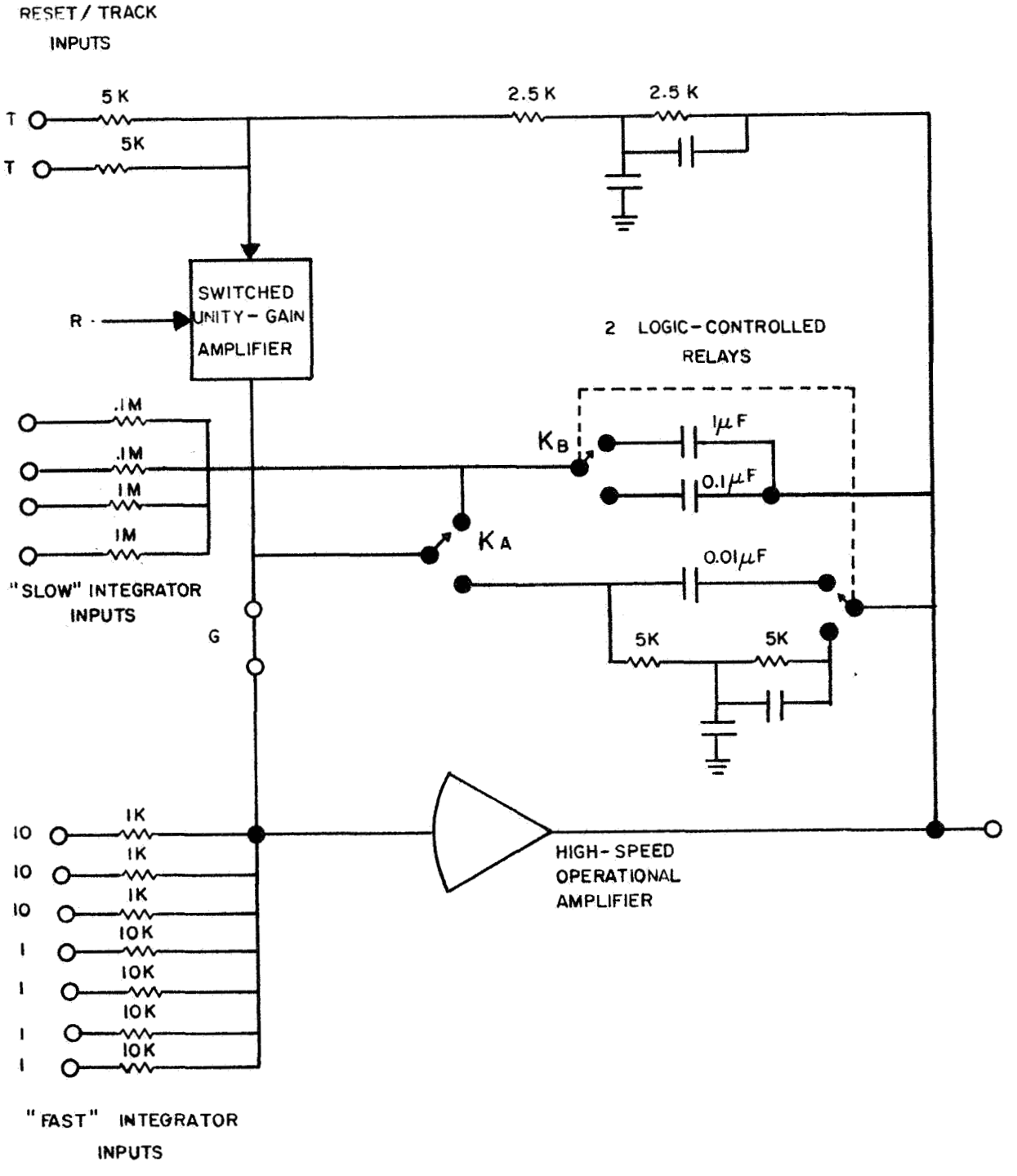


Fig. A.7 LOCUST Integrator/Track-hold Circuit Schematic Diagram

Summing Amplifiers - Analog computing elements 3, 8, 13 and 18 are uncommitted (no feedback resistor) amplifiers with patch fields identical to the lower portion of an integrator/track-hold element (Fig. A.8). These amplifiers have limiters and overload lights. These amplifiers must have a feedback resistor connected even when they are not in use.

2-Input Dual Amplifiers - Eight 2-input dual-amplifier modules [Fig. A.9(a)] are provided for phase inverting and limited summing amplifier applications. The patch field also has terminations for ± 10-V reference and for signal ground. A 2-input dual amplifier module is used with the plug-in diode function generator. These units have no overload lights.

Phase Inverters - Six unity-gain phase-inverters [Fig. A.9(b)] are provided for high speed phase inversion applications. No overload lights are provided.

Analog-to-Digital Converters - A/D converter patching is illustrated in Fig. A.10. The A/D converters require an integrator/track-hold element with a 0.01 μF capacitor for operation and two digital control signals from the digital patchpanel as shown.

The analog input is patched to a TRACK input. Thus, the A/D converter performs its own sampling operation at the time the digital control signal goes to "1". The converter takes about 250 μs to convert and then presents an eleven-bit 2's complement code along with a flag signal to indicate that conversion is finished at its output.

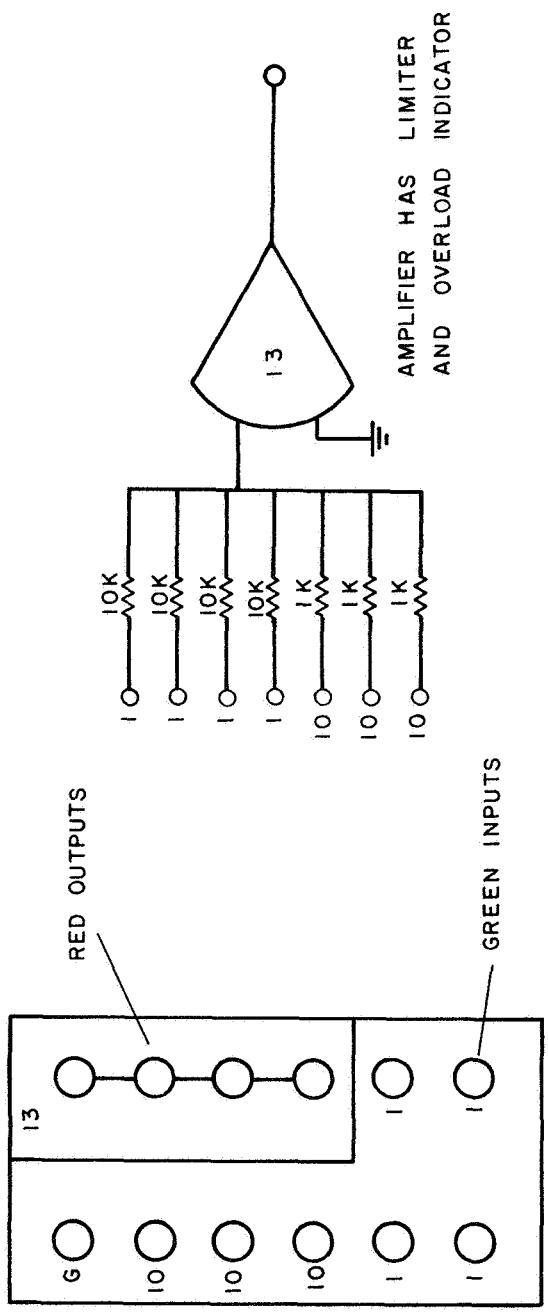
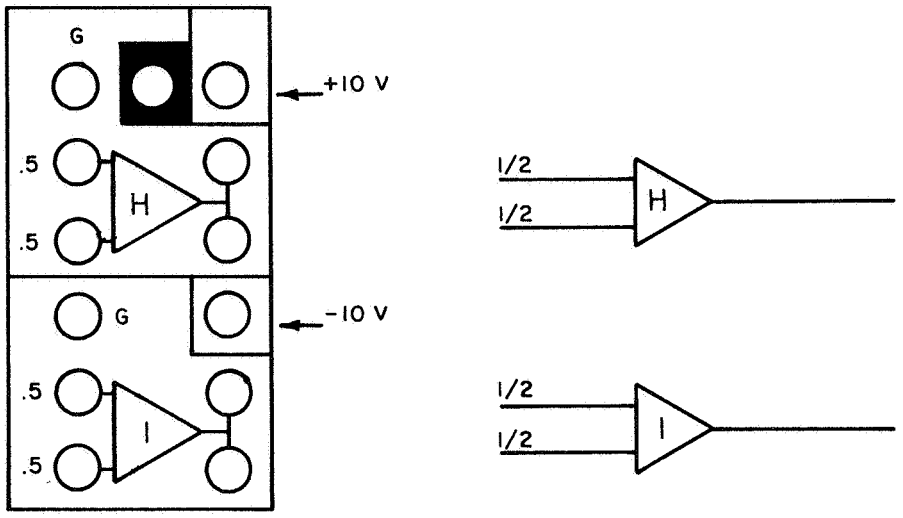
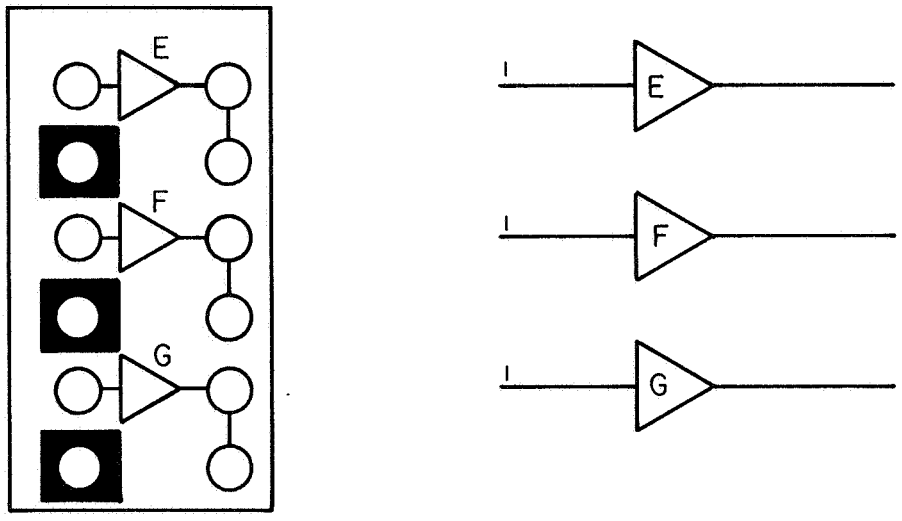


Fig. A.8 Uncommitted Amplifier Patching



(a)



(b)

Fig. A.9 (a) 2-input Dual Amplifier Patching
(b) Phase Inverter Patching

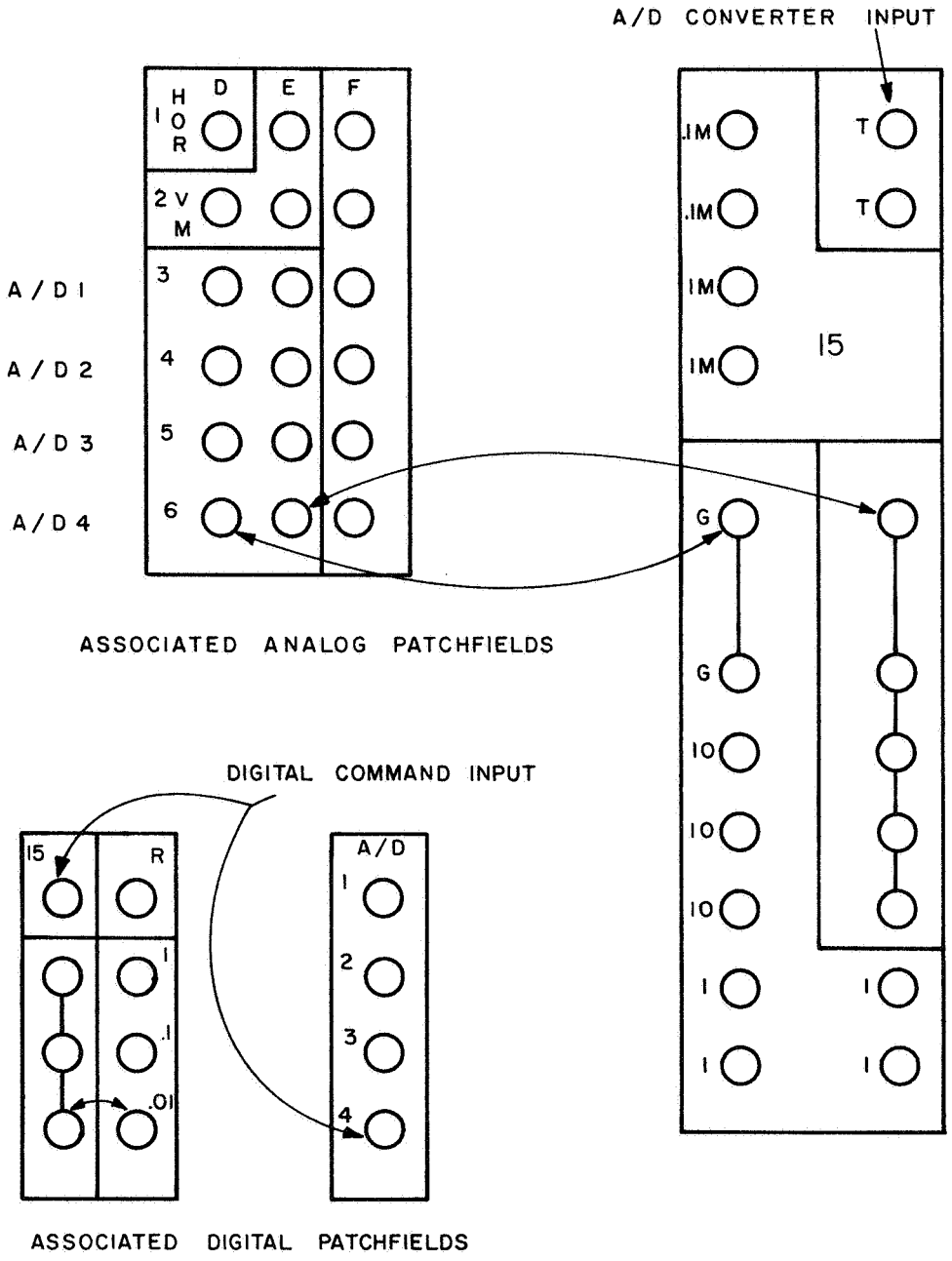


Fig. A.10 A/D Converter Patching

A/D1, A/D2, A/D3 and A/D4 are calibrated to go with integrator/track-hold elements 11, 12, 14 and 15 respectively and use the top input.

Analog Multiplier-Dividers - Patchfields for six high-speed four-quadrant multiplier/divider elements [Fig. A.11(a,b)] are located at the top of the analog patchpanel. The multiplier/divider elements are self-contained and need no external amplifiers. These elements must be driven only from a low impedance amplifier output.

Sine-Function Generator - Two sine-function generators are located in the upper right and left hand corners of the analog patchpanel. A sine-function generator is patched as shown in Fig. A.11(c) with the aid of a summing amplifier with no feedback resistor (amplifiers 3, 8, 13 and 18). Nine volts input corresponds to 90 degrees or $\pi/2$ radians. The cosine can be generated using the sine-function generator. Apply a constant nine volts to one input and let the variable input represent a minus input angle.

Digital-to-Analog Multipliers - The LOCUST D/A multipliers are patched as illustrated in Fig. A.11(d). A D/A multiplier utilizes a summing amplifier which has no feedback resistor (amplifiers 3, 8, 13 and 18). The D/A multiplier accepts a 12-bit 2's complement digital code as one input variable and an analog variable as the other input. Note that both X and -X are needed.

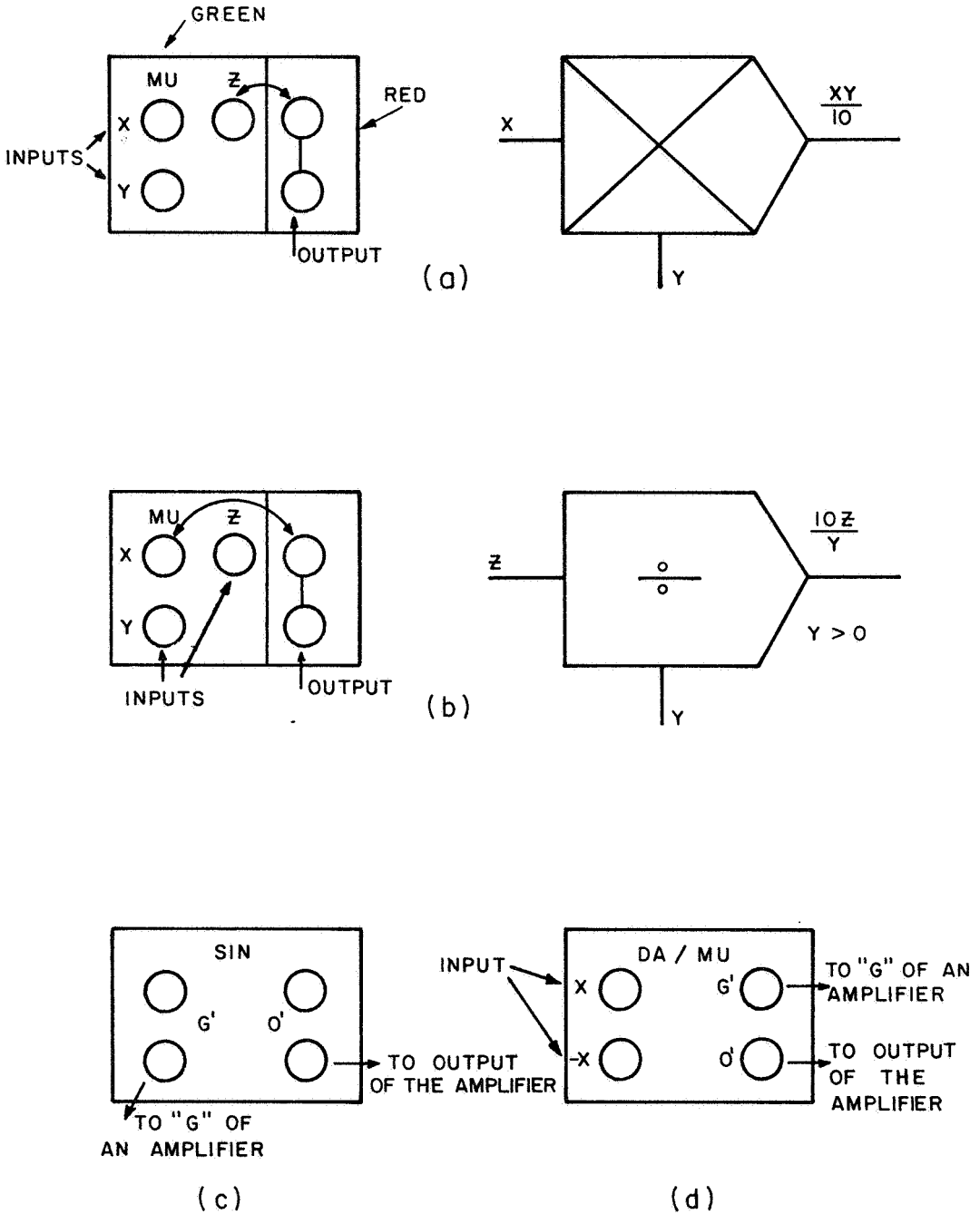


Fig. A.11 (a) Analog Multiplier Patching (b) Analog Divider Patching (c) Sine-Function Generator Patching (d) D/A Multiplier Patching

Analog Comparator - Analog comparator inputs [Fig. A.12(a)] appear at the lower right and left hand corners of the analog patchpanel. Two inputs may be summed, yielding a comparison when the input sum is zero. Complementary MECL-level outputs appear on the digital patchbay [Fig. A.12(a)]. The upper output (red) represents the "inverted" output with respect to the analog input; hence, the minus signs on the comparator inputs. In some circumstances the comparator output rise-time may not be fast enough to trigger a J-K flip-flop. In this case it may be "buffered" by connecting its outputs to the s and r inputs of a J-K flip-flop.

D/A Electronic Switches - Figure A.12(b) illustrates two D/A electronic switch configurations. S1 (also S3) is comprised of two switches, one normally OFF, one normally ON, both controlled by the same digital input for operation as a SPDT switch. The associated amplifier must have a 10 kΩ feedback resistor for unity-gain operation. S2 and S4 are single normally OFF electronic switches. Control inputs appear on the digital patchpanel labeled D/A1, D/A2, D/A3 and D/A4 for S1, S2, S3 and S4 respectively. A logical "1" turns a normally OFF switch ON.

D/A Relay Switch - Switches K1-K4 [Fig. A.12(c)] are reed relays controlled by digital logic signals from the digital patchbay. The relays operate in less than 5 ms and are used for "slow" computation and for initial condition setup in INITIAL RESET. A logical "1" closes a normally open relay contact. Digital inputs are on the digital patchpanel labeled K1, K2, K3 and K4.

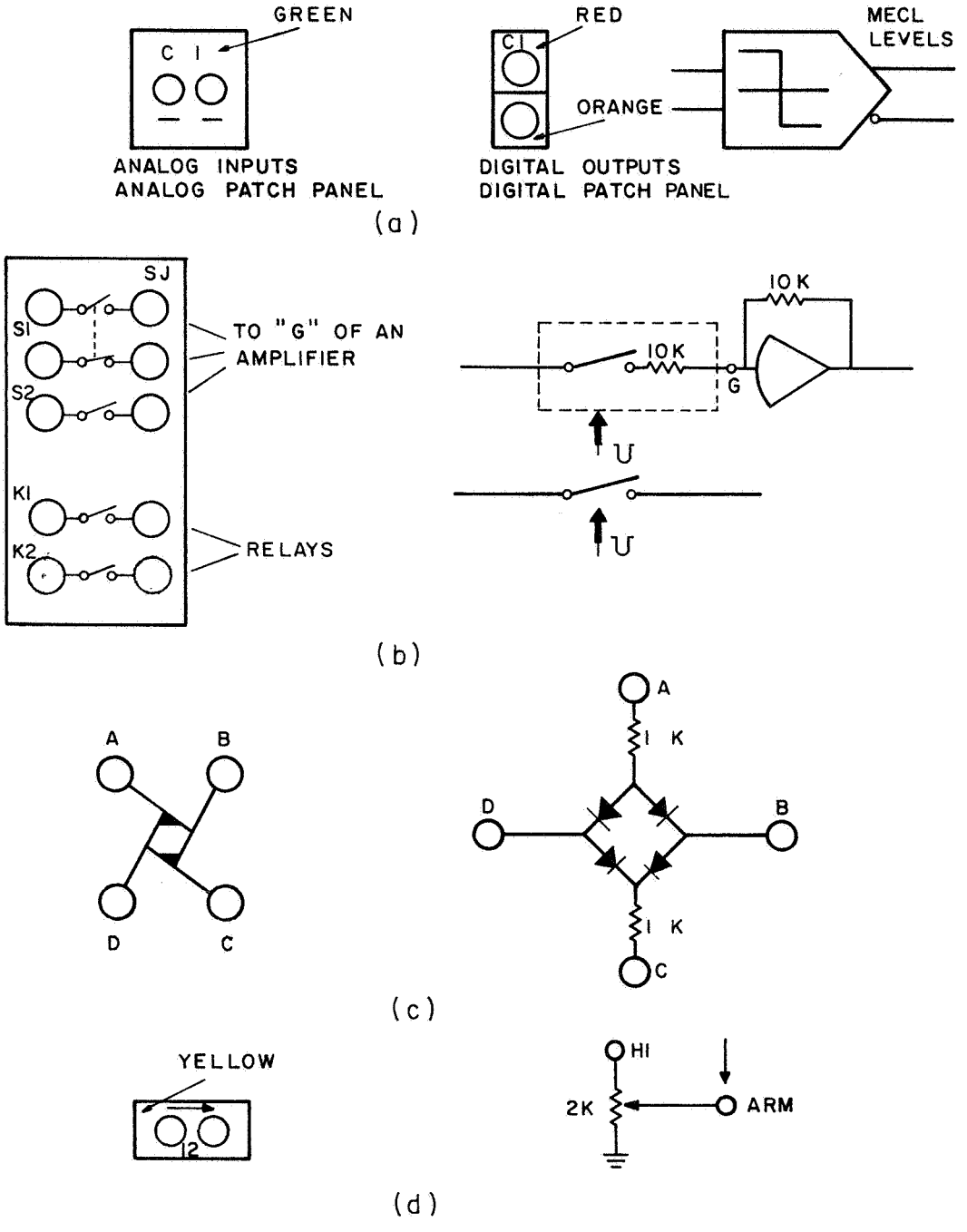


Fig. A.12 (a) Analog Comparator Patching (b) D/A Electronic Switch Patching (c) Diode Bridge Patching (d) Potentiometer Patching

Diode Bridges - Four diode bridges [Fig. A.12(c)] are available for use in nonlinear computer circuits. These are available at the lower right corner of the analog patchpanel.

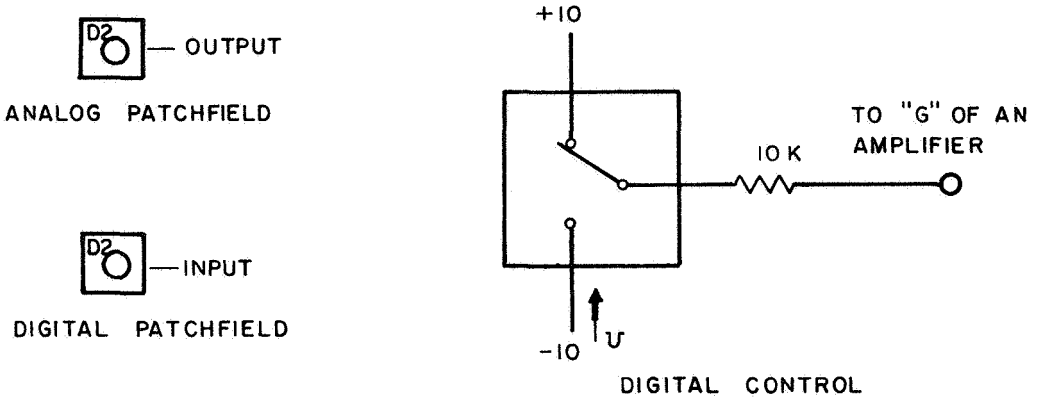
Coefficient Potentiometers - Figure A.12(d) indicates the patching connections for coefficient potentiometers. Pressing the button adjacent to a potentiometer with the computer in the POTSET mode connects the +10-V reference voltage to the potentiometer HI input and the ARM to the digital voltmeter so that the potentiometer can be set while loaded using the digital voltmeter. Note that two potentiometers (12, 24) located at bottom-center on the analog patchpanel have their LO terminals available. Potentiometers are fused with 1/32 amp fuses on the HI side.

Caution. Do not press more than one potentiometer button at a time.

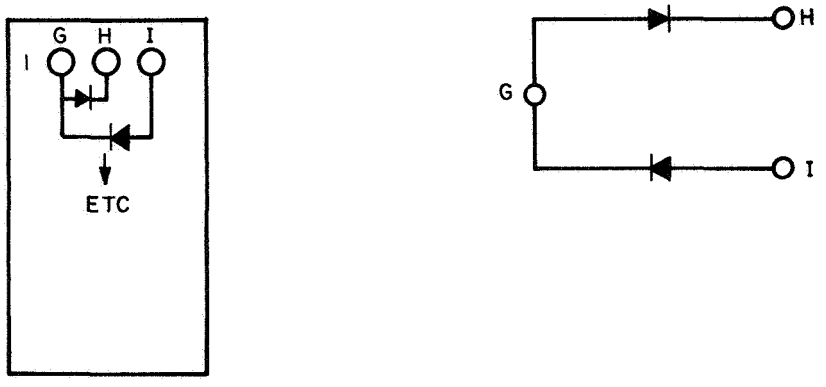
Potentiometer fuses have about 40 ohms resistance. Therefore, even if the potentiometer is set all the way at the HI end, the coefficient will be about 0.98 with no load connected to the ARM.

Noise Drivers (reference switches) - Four noise driver outputs D1-D4 are located in the lower row of the analog patchpanel [Fig. A.13(a)] with corresponding digital inputs located conveniently next to the sampling-type noise generators on the digital patchbay. A noise-driver provides accurate, switched $\pm$ 10-V levels to an internal 10 kΩ resistor. The driver output is patched to the summing junction G of an amplifier (usually an integrator).

Free Diodes - Six silicon diode-pairs [Fig. A.13(b)] are available on the analog patchpanel for use in nonlinear networks. Amplifiers 3, 8,



(a)



(b)

Fig. A.13 (a) Noise Drive Patching
(b) Free Diode Patching

13 and 18 have no committed feedback resistors in order that they can be used for setting up these networks.

Plug-in Diode Function Generators - The diode function generators consist of a plug-in module which covers the patching area of a 2-input dual-amplifier computing element to provide positive and negative slopes. Six breakpoints are fixed at $\pm$ 1, $\pm$ 3, and $\pm$ 5.5 volts. The slopes and a d-c adjustment (parallax) are set by means of eight screwdriver adjust potentiometers located on the top side of the module. The input and output are on the front of the module. It is not possible to plug the module into the patchbay incorrectly.

Digital Clock Patchfield - The digital-clock patchfield is illustrated in Fig. A.14 and A.15 along with an explanation of each input and output. For more details of the operation of the digital timer circuits, see Part I of this instruction manual.

Shift Registers and Modulo-2 Adders - The LOCUST digital patchpanel contains four groups of shift-registers for pattern generation, memory, delay, pseudo-noise generation and counting. Each group (Fig. A.16) of six stages has common reset r and shift-command SH inputs. Each shift register column also contains a modulo-2 adder for use with the shift registers in generating pseudo-random noise. They also can be used for performing the exclusive-OR function

$$Y = A \cdot \overline{B} + \overline{A} \cdot B$$

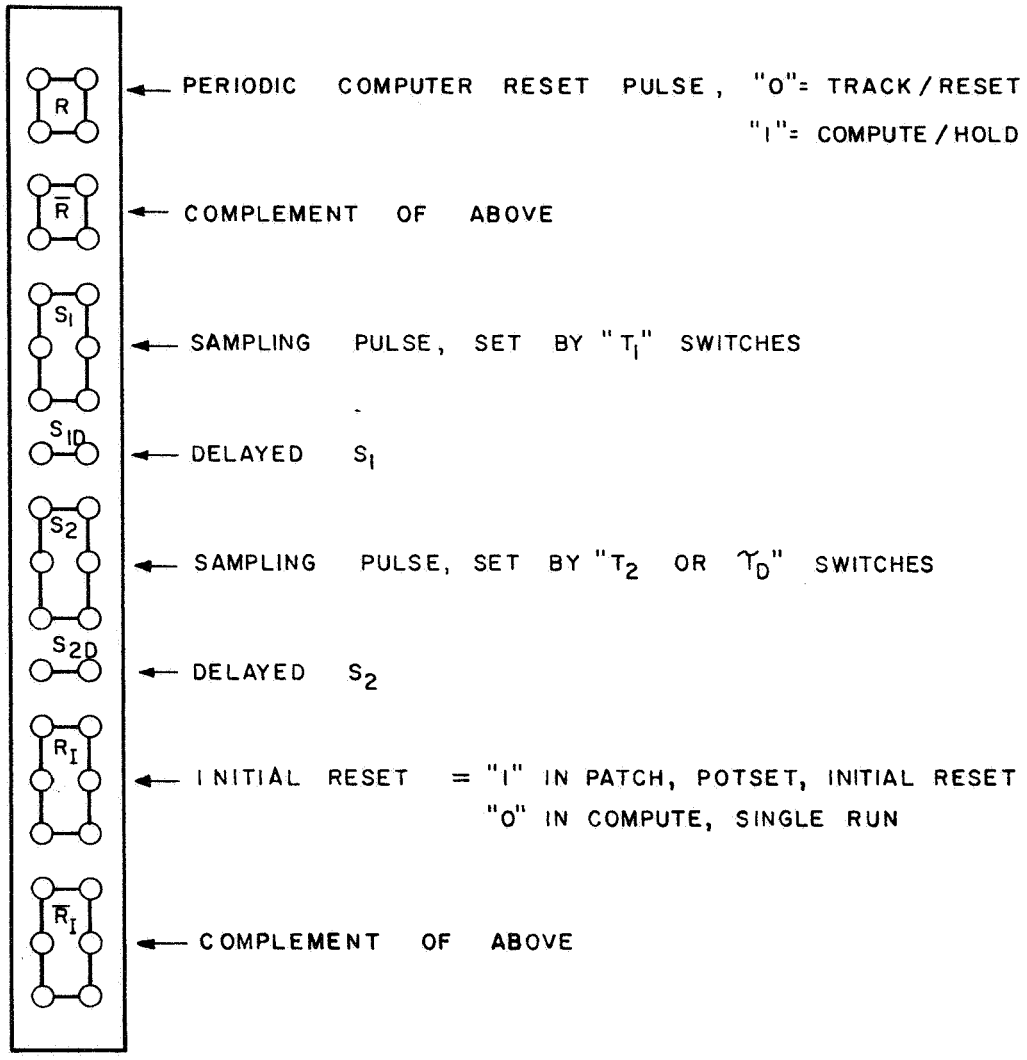


Fig. A.14 Master and Auxiliary Timer Patchfields

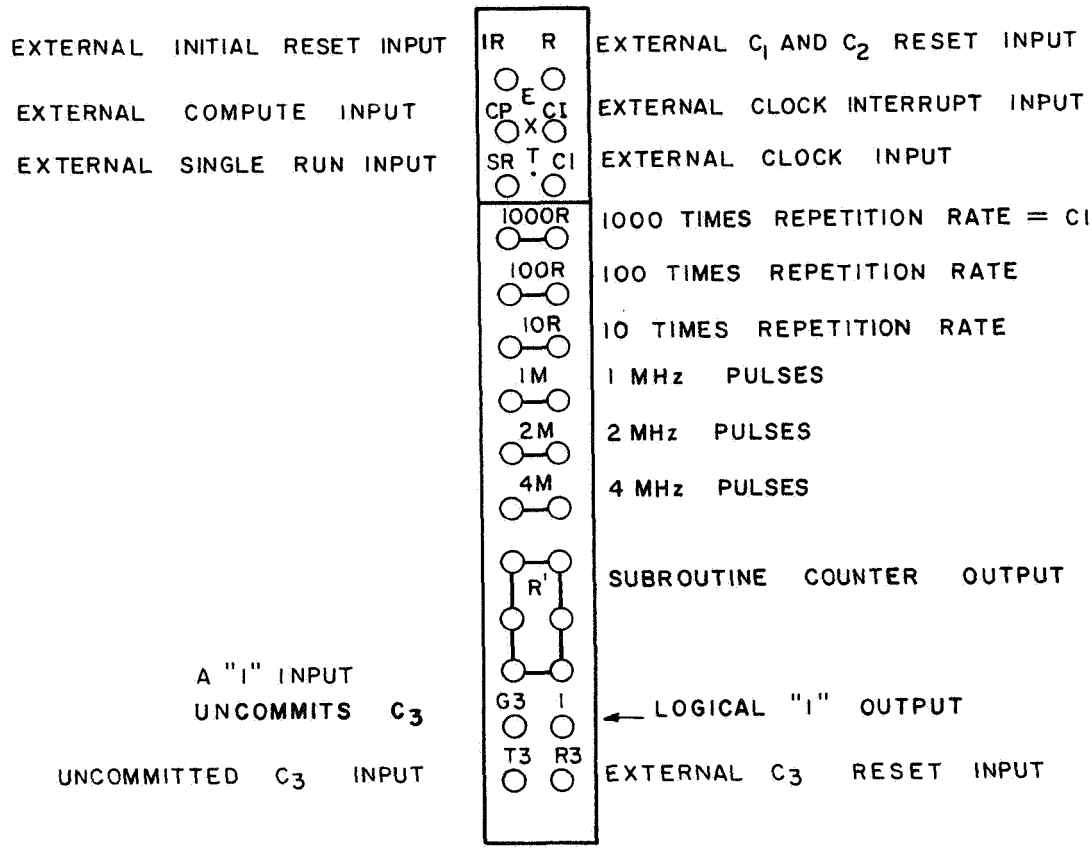


Fig. A.15 External Control and Subroutine Counter Patchfields

or, with the aid of an output inverting gate, the 1-bit comparator function

$$Y = A \cdot B + \overline{A} \cdot \overline{B}$$

The shift registers are operated in the following manner. Each stage is patched to the next as shown (Fig. A.16) for as many stages as are needed. Outputs are available with the use of a multiple-junction connector. A RESET signal is applied to r (usually R_I) and a SHIFT pulse train to SH. The SET inputs to the stages which are to be set to a "1" at time t = 0 are bottle-plugged to s as shown. When the COMPUTE button is depressed and released, R_I goes to "0" and a positive pulse 250 ns wide is applied to the patched SET inputs s; a shift command applied during this time will be ignored. The shift register is now ready for operation and will shift on a negative-going transition (dynamic "0") of the shift-command input signal.

A pseudo-random noise generator is set up as illustrated in Fig. A.17. Feedback connections using one-modulo-2 adder are tabulated in Table A.1.

The delayed set pulse (fixed duration, 250 ns) can also be used as a one-shot multivibrator in other logic schemes.

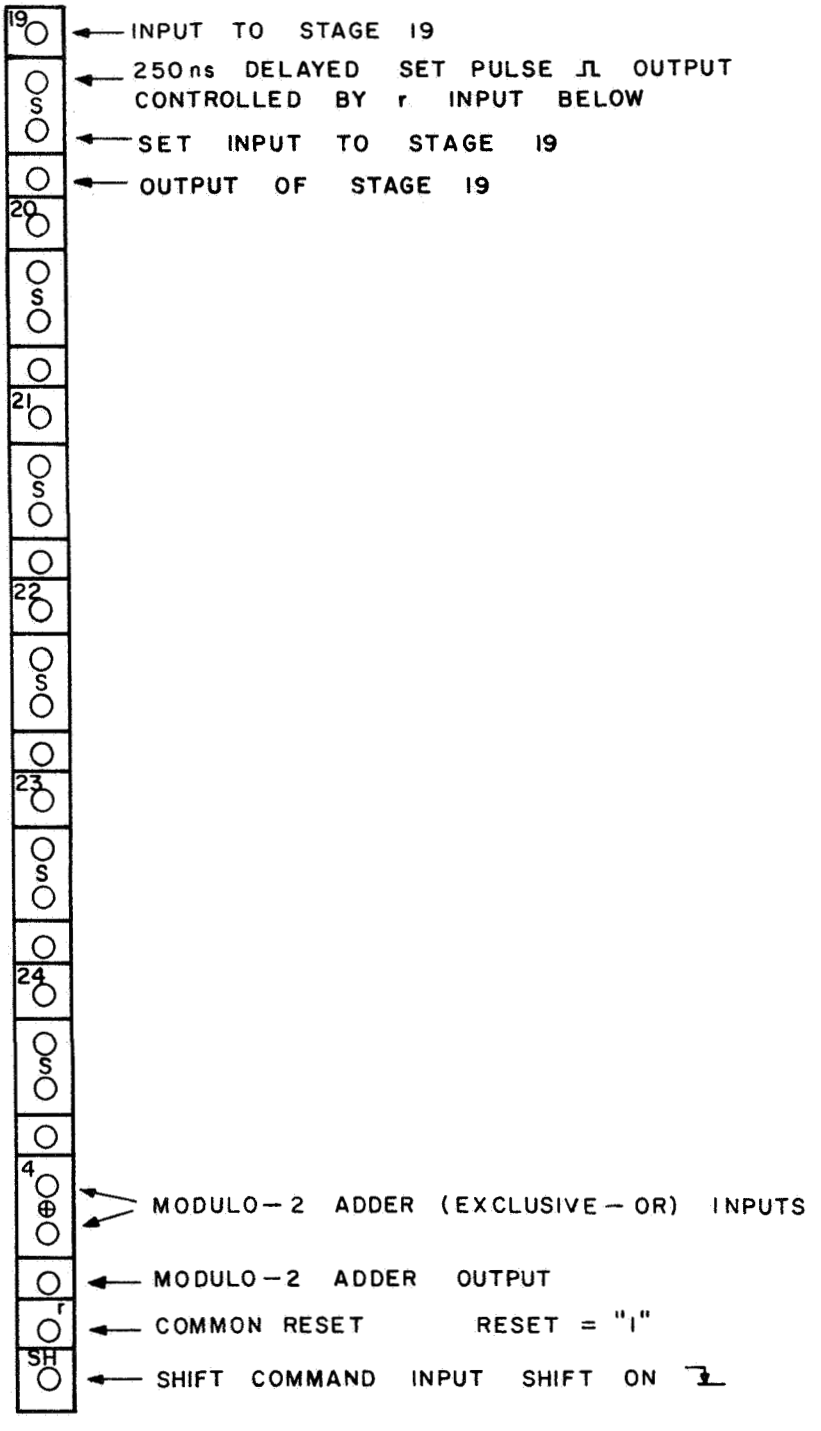


Fig. A.16 Shift Register and Modulo-2 Adder Patchfields

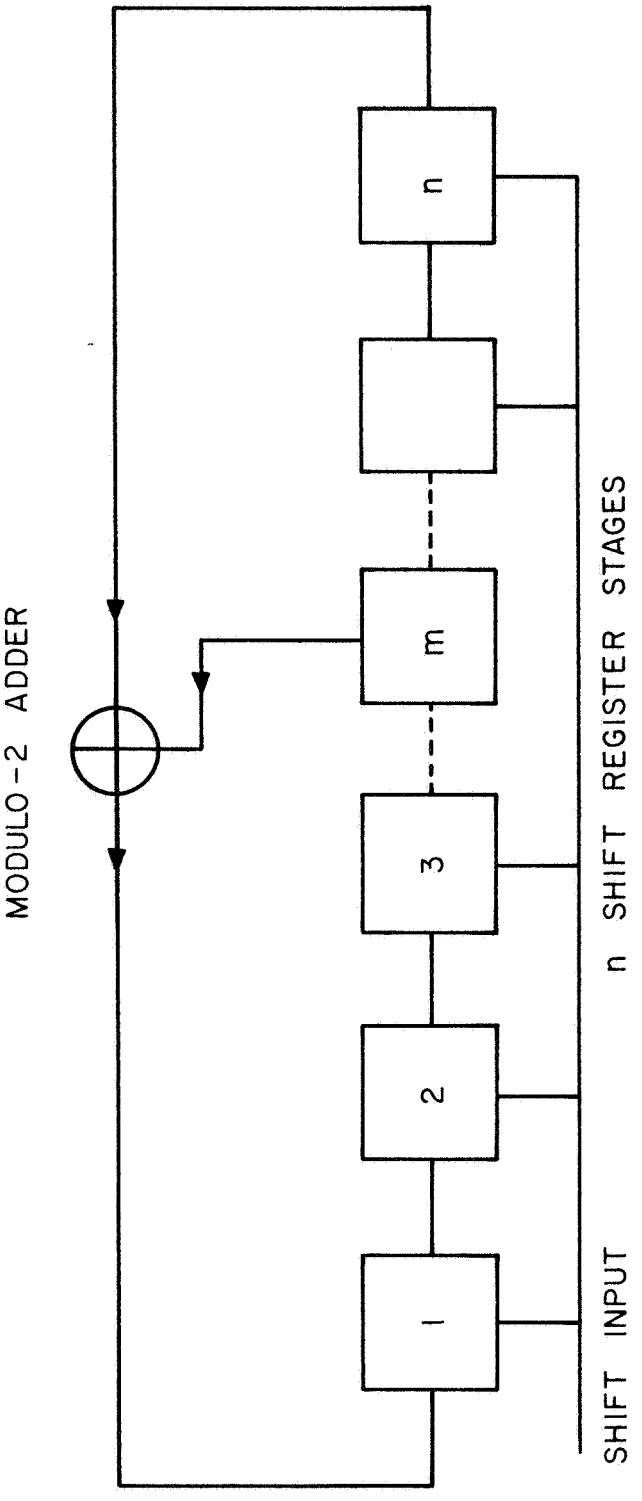


Fig. A.17 Pseudo-random Noise Generator Block Diagram

Table A.1

Pseudo-random Noise Generator Feedback Connections

Number of Shift Stages	Modulo-2 Feedback from Stages
3	1,3
4	1,4
5	2,5
6	1,6
7	1 or 3,7
9	4,9
10	3,10
11	2,11
15	1 or 4, or 7,15
18	7,18
20	3,20
21	2,21
22	1,22
23	5 or 9,23

J-K Flip-Flops - Figure A.18(b) illustrates patching connections for the LOCUST J-K type flip-flop. The complete truth table for the flip-flop is listed in Table A.2. $\overline{J}_s$ and $\overline{K}_s$ inputs refer to logic levels while the $\overline{J}_d$ and $\overline{K}_d$ inputs refer to dynamic logic swings. Either $\overline{J}$ input

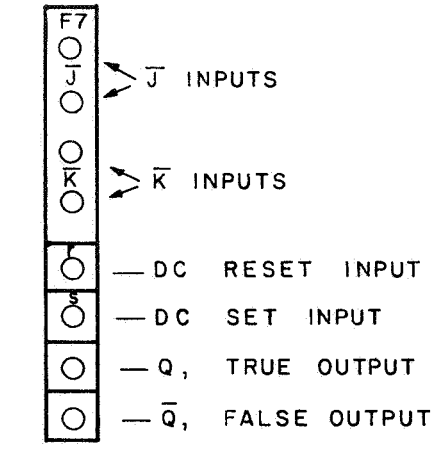
(and $\overline{K}$ input) may be designated as $\overline{J}_s$ or $\overline{J}_d$ ($\overline{K}_s$ or $\overline{K}_d$). Note that the flip-flop is not a true J-K flip-flop because its inputs are the complement of those of the standard J-K flip-flop. This rather complicated truth table can be reduced to simpler ones because the flip-flop is usually used in three different ways.

Table A.2

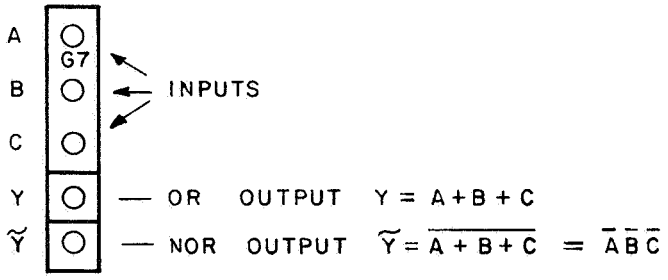
LOCUST Flip-flop Truth Table

$\overline{J}_s$	$\overline{K}_s$	$\overline{J}_d$	$\overline{K}_d$	Q^{n+1}
0	0	0	0	Q^n
0	0	0	1	0
0	0	1	0	1
0	0	1	1	$\overline{Q}^n$
0	1	0	0	Q^n
0	1	0	1	Q^n
0	1	1	0	1
0	1	1	1	1
1	0	0	0	Q^n
1	0	0	1	0
1	0	1	0	Q^n
1	0	1	1	0
1	1	ø*	ø	Q^n

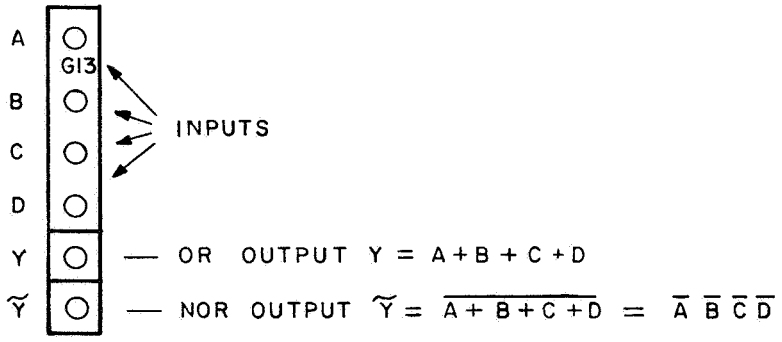
*Don't care.



(a)



(b)



(c)

Fig. A.18 (a) J-K Flip-flop Patchfield
(b) 3-input Gate Patchfield
(c) 4-input Gate Patchfield

D-c Set and Reset Operation [Fig. A.19(a)] -

1. "1" applied to the flip-flop "d-c set" input (white s) produces the output Q = "1", no matter what levels or pulses are applied to the $\overline{J}$ and $\overline{K}$ inputs (overriding d-c set).
2. A "1" applied to the flip-flop "d-c reset" input (white r) produces the output Q = "0", no matter what levels or pulses are applied to the $\overline{J}$ and $\overline{K}$ inputs (overriding d-c reset).
3. A "1" applied to both r and s simultaneously is an undefined state and should not be allowed.

D-c set and reset inputs are used to establish initial states, to "arm" logic circuits, and to inhibit their operation when desired.

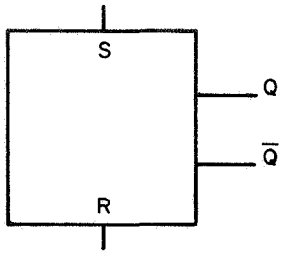
Toggle Operation [Fig. A.19(b)] - A simultaneous dynamic "1" on the $\overline{J}_d$ and $\overline{K}_d$ results in $Q^{n+1} = \overline{Q}^n$ (toggle operation, binary counting).

Clocked Operation [Fig. A.19(c)] - $\overline{J}_s$ and $\overline{K}_s$ are level inputs. $\overline{C}_d$ is applied to both $\overline{J}_d$ and $\overline{K}_d$ inputs. Changes in the levels of $\overline{J}_s$ and $\overline{K}_s$ are allowed only when $\overline{C}_d$ = "1" for operation in agreement with the truth table.

Output-state changes (if any) take place only when a dynamic "1" is applied to $\overline{C}_d$. The n^{th} such pulse may be regarded as a sampling pulse which "tests" the then existing levels $\overline{J}_s^n$, $\overline{K}_s^n$ and Q^n and produces a new output level Q^{n+1} as a logical function of these levels:

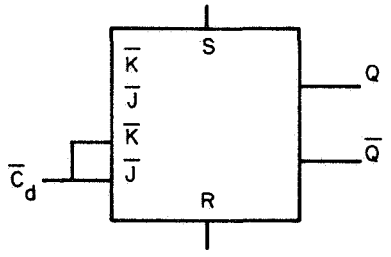
$$Q^{n+1} = \overline{K}_s^n Q^n + J_s^n \overline{Q}^n$$

The output Q^{n+1} is maintained until a new $\overline{C}_d$ pulse produces a new sample (digital storage).



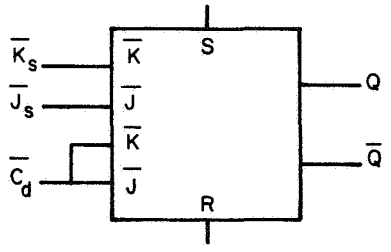
D-C SET-RESET		OPERATION
S	R	Q^{n+1}
0	0	Q^n
0	1	0
1	0	1
1	1	?

(a)



TOGGLE	OPERATION
$\overline{C}_d$	Q^{n+1}
0	Q^n
1	$\overline{Q}^n$

(b)



CLOCKED J-K			OPERATION
$\overline{J}_s$	$\overline{K}_s$	$\overline{C}_d$	Q^{n+1}
ø	ø	0	Q^n
0	0	1	$\overline{Q}^n$
0	1	1	1
1	0	1	0
1	1	1	Q^n

$$Q^{n+1} = (Q^n \overline{K_s \overline{C}_d} + \overline{Q}^n J_s \overline{C}_d)\overline{S}\,\overline{R} + S\overline{R}$$

ø = DON'T CARE

(c)

Fig. A.19 Flip-flop Operation (a) D-C Set and Reset Operation (b) Toggle Operation (c) Clocked J-K Operation

Asynchronous Operation (Table A.2, p. 153) - Output-state changes (if any) will take place only when $\overline{J}_d$, $\overline{K}_d$, or both have a dynamic "1" applied. If the output states before and after such a transition are respectively denoted by Q^n and Q^{n+1}, then

1. A dynamic "1" on $\overline{J}_d$ alone results in Q^{n+1} = "1"
2. A dynamic "1" on $\overline{K}_d$ alone results in Q^{n+1} = "0"

no matter what the levels of $\overline{J}_d$, $\overline{K}_d$ and Q were before the dynamic "1" occurred ("a-c set and reset" operations).

For more sophisticated applications, one can have two dynamic or sampling-pulse inputs, $\overline{J}_d$ and $\overline{K}_d$ as follows:

3. For Q^n = 0, a dynamic "1" applied to $\overline{J}_d$ along produces Q^{n+1} = "1" if and only if $\overline{J}_s$ = 0
4. For Q^n = "1", a dynamic "1" applied to $\overline{K}_d$ alone produces Q^{n+1} = "0" if and only if $\overline{K}_s$ = "0"

Otherwise, dynamic "1"'s applied to only one of the dynamic inputs leave the output state unchanged.

Gates - Twelve 3-input and six 4-input OR/NOR gates are available on the digital patchpanel [Fig. A.18(b,c)] and perform the logic functions as shown. Note that to perform the AND function, one merely applies the complements of those variables to the inputs of a NOR gate.

In-line Readout Counters - Six separate uncommitted decimal counters with in-line readout are controlled at the digital patchbay [Fig. A.20(a)]. The readout units are arranged so that they can be conveniently grouped as 1, 2, or 3-decade units, or, all six can be connected

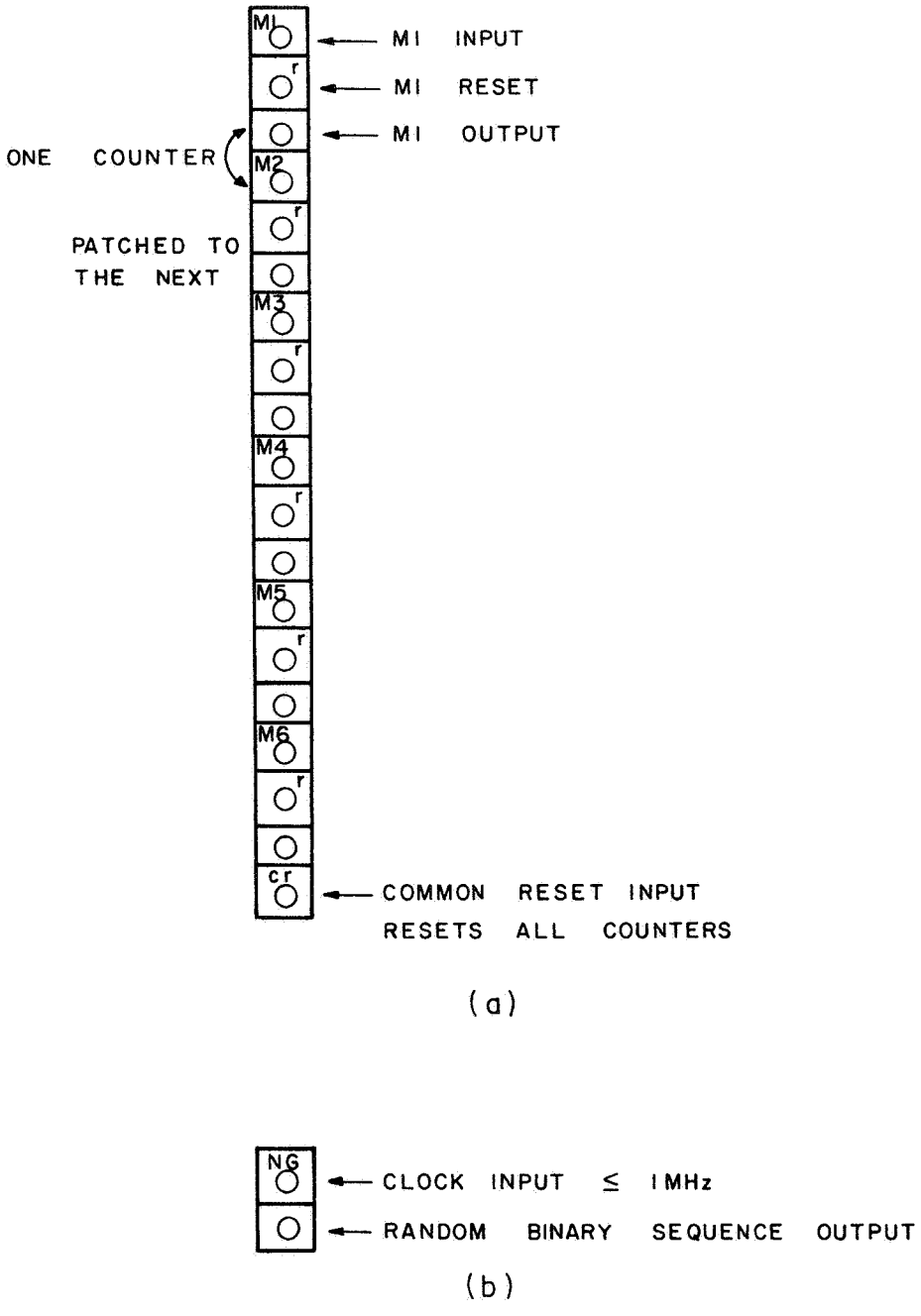


Fig. A.20 (a) Readout Counter Patchfield
(b) Sampling-type Noise Generator Patchfield

together. Triggering is accomplished by a dynamic "1" applied to the inputs (green) and reset by a logical "1" applied to the individual reset inputs (white r). A common reset line is located at the bottom of the counter field (white cr) and a common reset pushbutton is located at the left side of the display unit. The output of a single counter changes to a logical "0" on the eighth count and back to "1" on the tenth count. These units are used to display event counts, and as divide-by-ten counters.

Noise Generators - Two sampling-type digital noise generators are provided [Fig. A.20(b)]. The output is a random binary signal which changes state randomly only at clock intervals.

The autocorrelation function of the output is

$$R_{YY}(\tau) = E^2\left(1 - \frac{|\tau|}{\Delta t}\right) \quad |\tau| \leq \Delta t$$

$$= 0 \qquad\qquad |\tau| > \Delta t$$

where E is the amplitude of the output pulse train and $\Delta t = 1/f_c$ is the period of the input clock.

The power spectral density is

$$G_{YY}(\omega) = E^2\ \Delta t \left(\frac{\sin \frac{\omega\ \Delta t}{2}}{\frac{\omega\ \Delta t}{2}}\right)^2$$

The noise generator should not be clocked at frequencies greater than 1 MHz to insure uncorrelated output states.

The noise drivers mentioned earlier are to be used with the noise generators when accurate switched levels are desired on the analog patchpanel.

Manual Pushbuttons - Four manual pushbuttons [Fig. A.21(a)] are provided to give logical complementary outputs on the digital patchpanel when a button is pushed. The switches are buffered by R-S flip-flops to eliminate effects of switch-contact bounce.

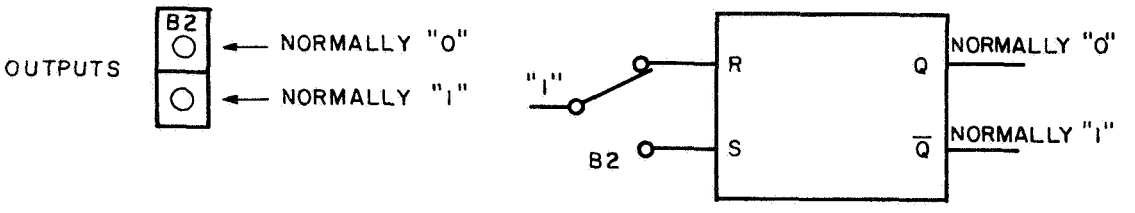
Logic-State Indicator Lamps - The logic-state indicators are located above the digital patchbay. Each one lights when a logical "1" is applied to the corresponding input which is located at the bottom of the shift register patchfield and labeled I1 through I12 [Fig. A.21(b)].

Readout Trunks - Four trunk lines are available on the digital patchpanel to permit connections to external devices, in particular, the oscilloscope. The scope sync input SC is one of these trunks.

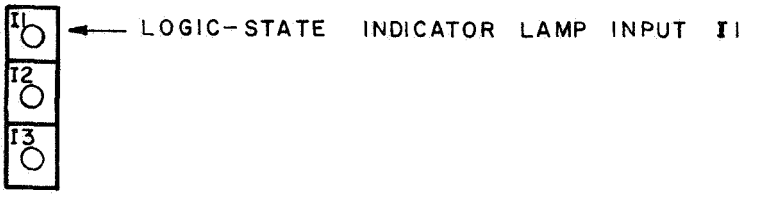
Six analog readout trunks are located in the D, E, F trunk-block field in column F. Outputs terminate in BNC coaxial connectors above the power supply monitoring panel.

Trunk Lines - Thirty-four trunk lines (right column) are provided to permit patching of interface equipment to the PDP-9 digital computer. There are no trunk lines connecting the analog and digital patchpanels.

Caution - Never connect any patchcord between analog and digital patchbays.



(a)



(b)

Fig. A.21 (a) Manual Pushbutton Patchfield
(b) Logic-state Indicator Inputs

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