RAYTHEON COMPANY
SPACE AND INFORMATION SYSTEMS DIVISION

FINAL REPORT

AUXILIARY MEMORY
FOR APOLLO GUIDANCE COMPUTER

CONTRACT NAS 9-5994

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APPENDICES A, B, C, F, AND G

PREPARED FOR

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
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FOREWORD

This document is the final report submitted in accordance with the requirements of Contract NAS-9-5994.

The program conducted under this contract began as a feasibility exercise to demonstrate that the Apollo Guidance Computer (AGC) could be augmented with additional fixed memory, supplemented by a tape recorder.

Subsequent redirection to configure the system for possible use on an early flight resulted in the Auxiliary Tape Memory (ATM) being fabricated to standards much higher than a feasibility demonstration would require.

As work progressed, additional requirements were imposed on the system, principally the augmentation of AGC erasable memory.

This report contains a description of the hardware designed and developed under this contract, together with a description of the system design leading up to the hardware.

Material has been included which describes the operation of the system from a software point of view; a "programmer's guide" to the AM.

Demonstration of the system was an important contract milestone; the test objectives, configuration, and method of accomplishing the objectives have been incorporated in the report.

Several appendices contain significant supplementary information, including (in a separate volume) complete listings of the demonstration test programs.

SECTION 1

UNIT DESCRIPTION

The Auxiliary Memory (AM) system is composed of three units: the Auxiliary Core Memory (ACM), Auxiliary Tape Memory (ATM) and the Interface Module (IM). In addition, a portable control panel is used for monitoring and testing purposes.

The engineering model of the ACM is of brassboard construction with the logic modules, memory electronics modules and the power supply modules mounted on the same tray.

The ATM, supplied by Raymond Engineering Laboratory, Inc., Middletown, Connecticut, includes a magnetic tape transport with motor drive electronics, record/playback electronics and a self-contained power supply.

The IM is of open breadboard construction, although the printed circuit boards incorporated are suitable for flight use. The breadboard version of the IM includes not only circuits to service the ACM in flight, but also the circuits required for operation of GSE; these additional circuits would not be included in flight but would be contained in a separate piggy-back adapter.

The Control Panel (CP) is to be used as a monitoring device, particularly in the area which is inaccessible to the AGC; as a debugging aid; and as a tape preparing device for loading programs and the initial ID words. The panel with its electronics (which are easily removable for maintenance) fits in a suitcase type cabinet ("Transicase").

1.1 AUXILIARY CORE MEMORY

1.1.1. LOGIC

The logic elements used in the AM system are composed of a readily available family of Signetics low power (NE 400 series) and medium power (NE 100 series) monolithic integrated circuits. The units

in the engineering model are a commercial quality and operate over a temperature range of 0^{o} to 70^{o}C. Over 90 percent of the logic will utilize the NE 100 series while the NE 400 series line driver will be used mainly for ACM to AGC line drivers. The NE 100 series employs diode transistor (DTL) inputs for fan-in expansion capabilities, both active outputs (transistor pull-up) for driving high capacitive loads such as signal layer and multilayer boards, and resistor pull-up outputs for allowing the use of collector logic. The various members of the 100 series offer medium power, high speed and logic flexibility. The NE156 line driver is being used in the IM to interface with the AGC blue-nose gate (1006394) which offers greater speed for the AGC output signals.

All digital functions of the ACM are mechanized with integrated circuits. The micro-circuits are packaged in the familiar flat pack unit with 14 connector pins. The flat pack units are organized in three different kinds of modules; the low header, the extended low header, and the Deep Submergence mother-board header. See Table 1-1 for a listing of the logic modules.

The extended header is similar to the low header shown in Fig. 1-1 except that one half of the module has been extended to expose the signal layers on both sides for quick repair. The flat pack units are organized in sub groups of 19, arranged in a single row so that the gates are interconnected with a Signal Layer Matrix. Two rows are arranged on the module side and 276 module connector pins are made available to the 76 flat packs. The flat packs are mounted directly to the heatsink frame with 0.004 inch thick epoxy resin adhesive. The leads are parallel gap soldered to conductor pads on a universal Printed Circuit Board which is mounted to the opposite side of the heatsink frame. The Signal Layer Matrix assemblies are parallel gap soldered to the printed circuit board on the side opposite to the flat packs, and welded jumper wires accomplish the connection from the Printed Circuit Board to the module connector pins. It is essential to high speed computer operation that capacitances are minimized. The largest contributor to

TABLE 1-1

LOGIC MODULES

Module No.	Schematic No.	Logic Half Module No.	Type	Function
A02	194858	13	Extended Header	Tape Data Transmitter, TW Parity Gen
	366152	14		GSE Interface Line Drivers
A03	194835	11	Extended Header	Tape Data Receiver; Input Buffer
	194982	12		Tape Data Receiver; Agreement Det.Voters, Output Buffer
C04	-	-	DS Motherboard	Control-mastercounter, RATM, WATM, AMLDCH, POWER SUPPLY CONTROL, AMRDCH, MSTRT, COIN04
C05	-	-	DS Motherboard	Control-CONOUT REG, NBL GAP, IDREC, INST.COUNT., TIME COUNT, TRNSIP, WRITE-COUNT, TRSN, FF's., GoFWD/REV, READ, WRITE, INCID, END, EOBNKFL.
A06	194764	3	Low Header	IDREAD, IDSTART, IDSTOP, COMPARATOR, STOPWT, STOPRD, RD=ST, WIDST
	194771	4		COMPARATOR, CHOOO, IDREAD, IDSTART, IDSTOP, RD≷ST, AMADDR, WGAMWL
A07	194553	5	Extended Header	RL DRIVERS, RLWLCOMP. COIN 12, 13, 14
	194570	6		RL DRIVERS, RLWLCOMP. RCH20, 21, 25, 23
A08	365733	9	Extended Header	RGAM GENERATION, COIN 5, 6, 7,8,9,10,15 SSAM 9-12, WGAMATM, NBLATMFLI, RCHAM
	194459	10		ATM, TADDR, TW PARITY GEN.
A09	194467	1	Extended Header	GAM,GAM PARITY,WCHAM,SAM, EBAM,FBAM, FEAM, CHANNEL ADDRESS DECODER
	365322	2		

TABLE 1-1 (Continued)

LOGIC MODULES

Module No.	Schematic No.	Logic Half Module No.	Type	Function
T10	-	-	DS Mother-Board	MEMORY TIMING, PH1, PH2, & 12.8 kHz frequency generation. Tape Deskewing Logic.
All	194635	7	Low Header	MEMORY ADDRESS DECODERS, INHIBIT DRIVERS
	194679	8		MEMORY ADDRESS DECODERS, INHIBIT DRIVERS

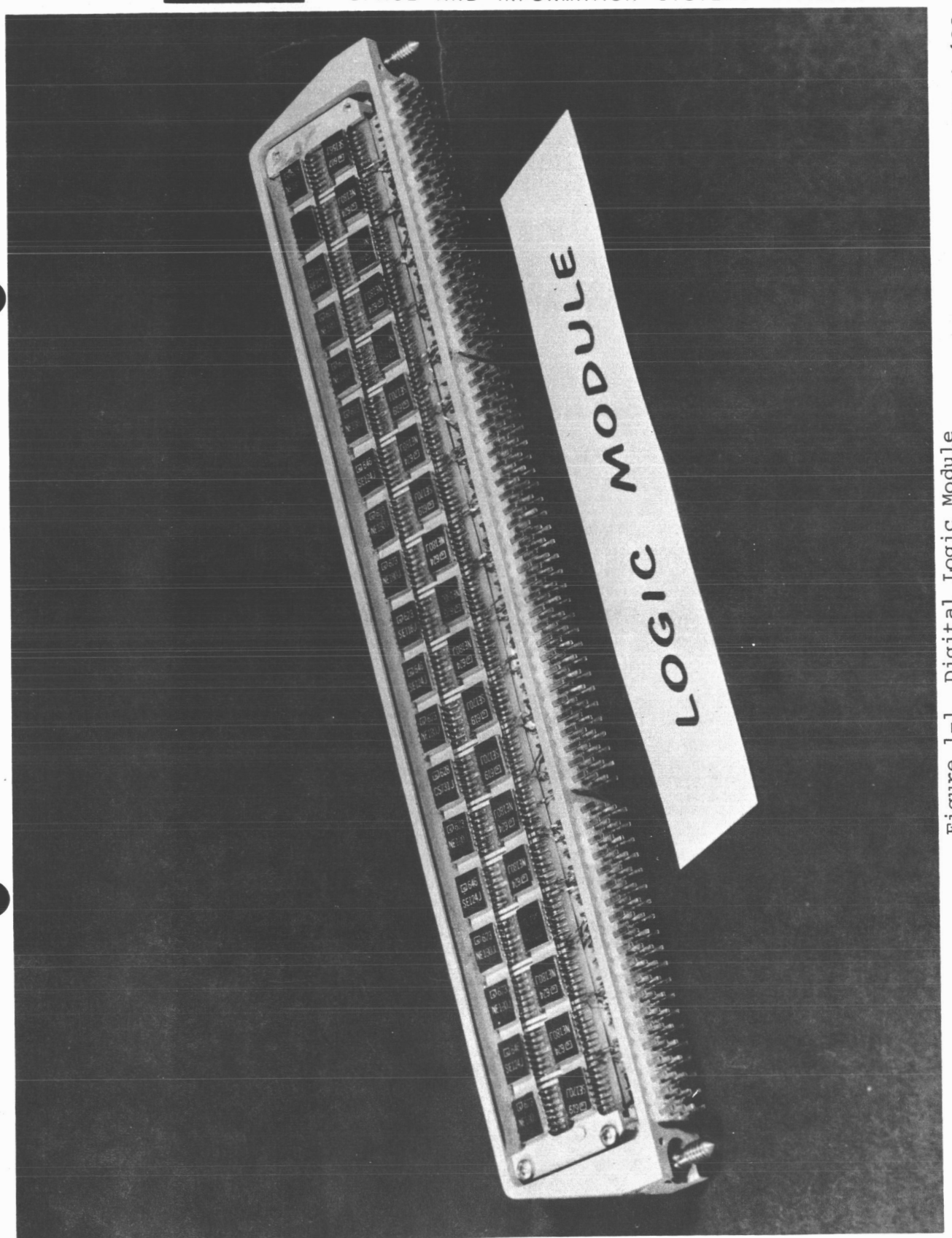

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Figure 1-1 Digital Logic Module

the total capacitance on any one signal is the path length, a function of how the flat packs are connected. Signal Interconnections within the module are incorporated with a Signal Layer Matrix and a universal Printed Circuit Board. The matrix assembly consists of "signal layers" of nickel, machine stamped from nickel strip to the required network configuration. The strips are positioned as layers in a plastic case or envelope and insulated from each other with mylar tape. Studies and worst case analysis tests evaluated the capacitances of a Signal Layer Matrix assembly as under the limit required for high speed operation of the logic devices selected. The signal paths from the flat pack connector pins and the module connector pins to the Signal Layer Matrix are accomplished with a universal, etched nickel, double sided Printed Circuit Board utilizing plated through holes. This item is simple in construction, uses generally standard fabrication techniques, can be inspected easily and is reliable and inexpensive.

The universal module mounting frame is a magnesium alloy structural member which supports heat transfer by conduction and holds the 276 module connector pins. Captive jacking screws, one at each end, mount the module to the chassis forcing engagement of the module connector pins with mating connector pins in the chassis. A high-dielectric coating is applied to all parts of the frame requiring electrical isolation from the electronic and signal carrying components. All electronic components receive a 15 mil thick conformal coating to provide environmental protection. It is apparent that all connections are readily accessible, a prime factor in diagnosis, repair, and replacement producing a low cost and highly reliable Digital Module design.

For a detailed description of the pin and flat pack configuration on the low and extended header logic modules see ACM dwg. 189623.

Control Modules C04, C05, and the ACM Timer T10 were built on a mother board side plate and mounted to an ACM header. Twelve printed circuit boards each containing 6 flat packs are soldered to one side of the side plate; interconnections are made on the reverse side with wire

wrap connections. The flat pack layout and pin configuration of these modules is shown in Fig. 1-2.

1.1.2 MEMORY SYSTEM

The Memory System consists of two Core Stack Modules, two Sense Amplifier Modules, and four Memory Electronics Modules. Expansion of the Memory System to twice its current capacity is possible by doubling the above complement of modules. The memory system is capable of receiving or returning data to the GAM register as instructed by Auxiliary Memory logic.

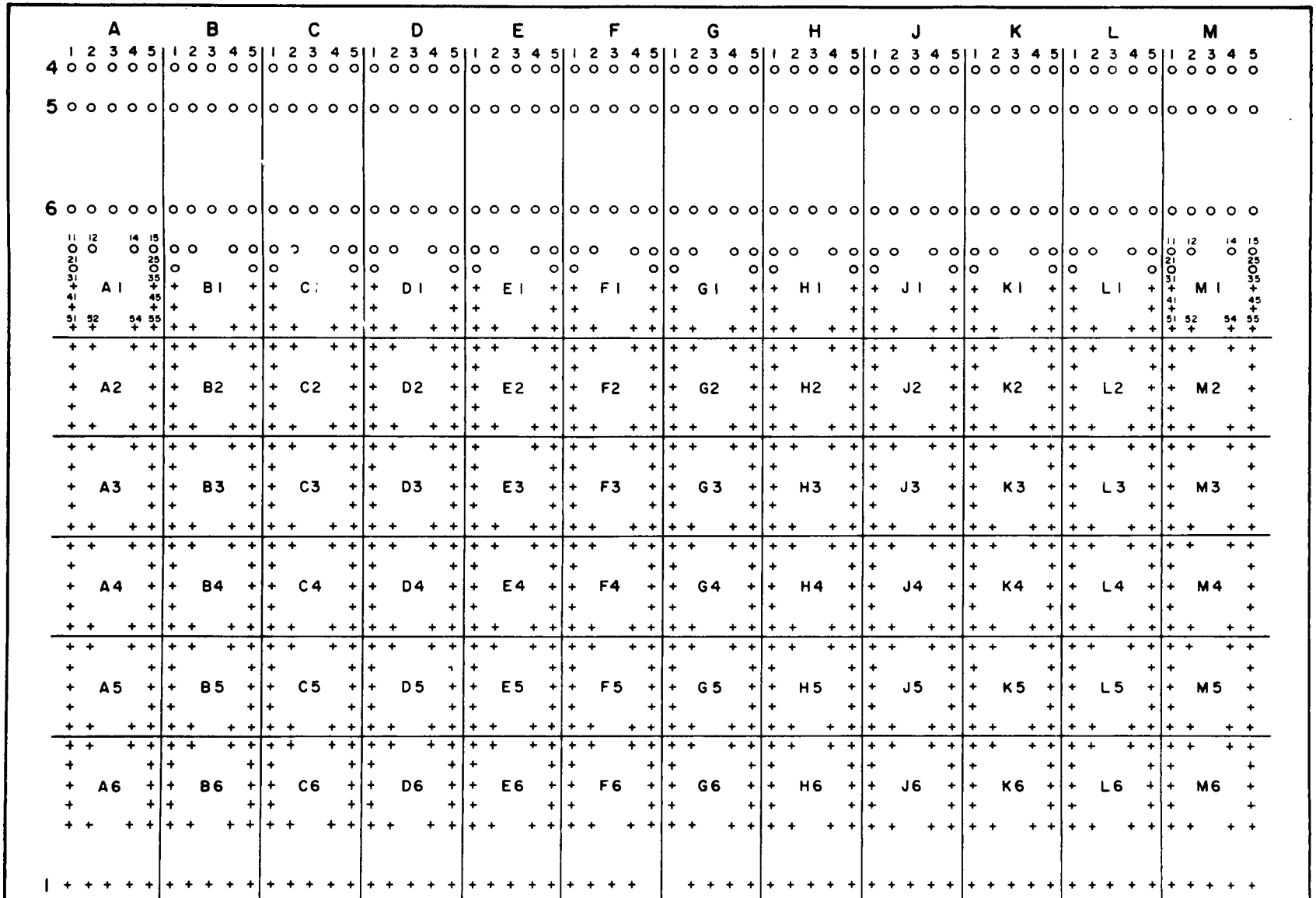
1.1.2.1 Core Stack Module

The Core Stack Module consists of a magnesium header shaped as a square box, in which the memory Core Stack is contained. The sides of the header are stepped, and on three sides resistor blocks containing a total of sixty-four resistors are located within the step. The stack also includes diode boards mounted on top and bottom containing a total of 256 diodes. The module is mounted on the ACM tray, making contact only at the four corner points of the step in the module header.

The cores selected for use in this array are 30-mil lithium ferrite with fast switching time, wide temperature range ($-55^{\circ}C$ to $+100^{\circ}C$), and low temperature coefficient.

Each core stack contains 4096 16-bit words (see figure 1-3). This stack is organized as a 3-D coincident current, 4-wire (x, y, sense & inhibit) memory. The array is configured as a 64 x 64 x 16 matrix mounted on eight double-sided planes. Each plane provides two word-bits of storage with a given side containing a single word bit for the entire 4096 words.

The basic stack configuration is packaged in a 4 inch x 4 inch frame to which mount two mats of 4096 cores, one mat per side. Eight frames are stacked vertically along with a top and bottom end frame (Figure 1-4). The device is then sandwiched together with four tie bolts, one in each corner. The required diode decoding matrices are mounted on


MOLDOUT FRAME
A
B
C
D
E
F
G
H
J
K
L
M
1 2 3 4 5
4
5
6
A1
B1
C1
D1
E1
F1
G1
H1
J1
K1
L1
M1
A2
B2
C2
D2
E2
F2
G2
H2
J2
K2
L2
M2
A3
B3
C3
D3
E3
F3
G3
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K3
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M3
A4
B4
C4
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M4
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K6
L6
M6
1

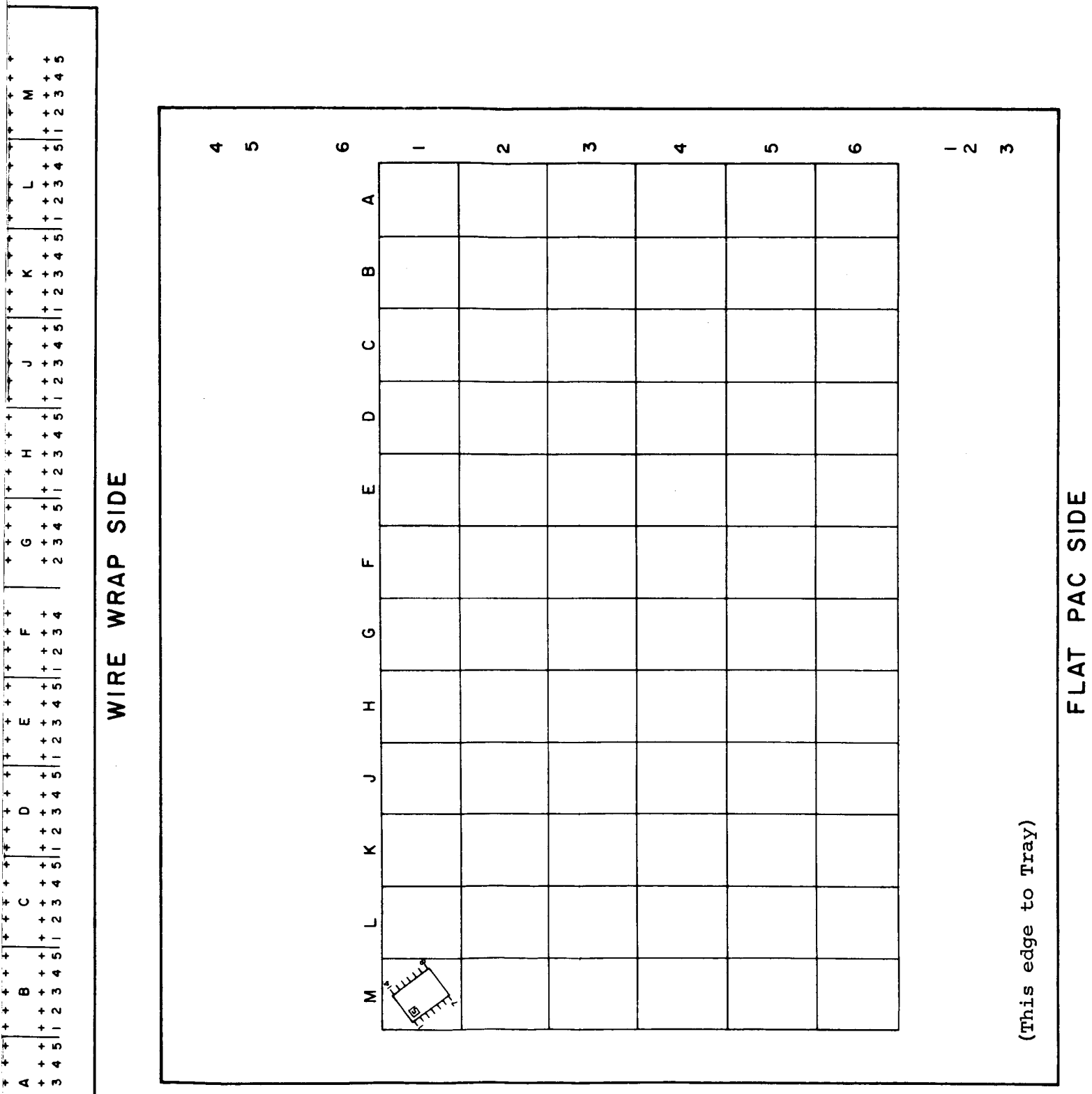
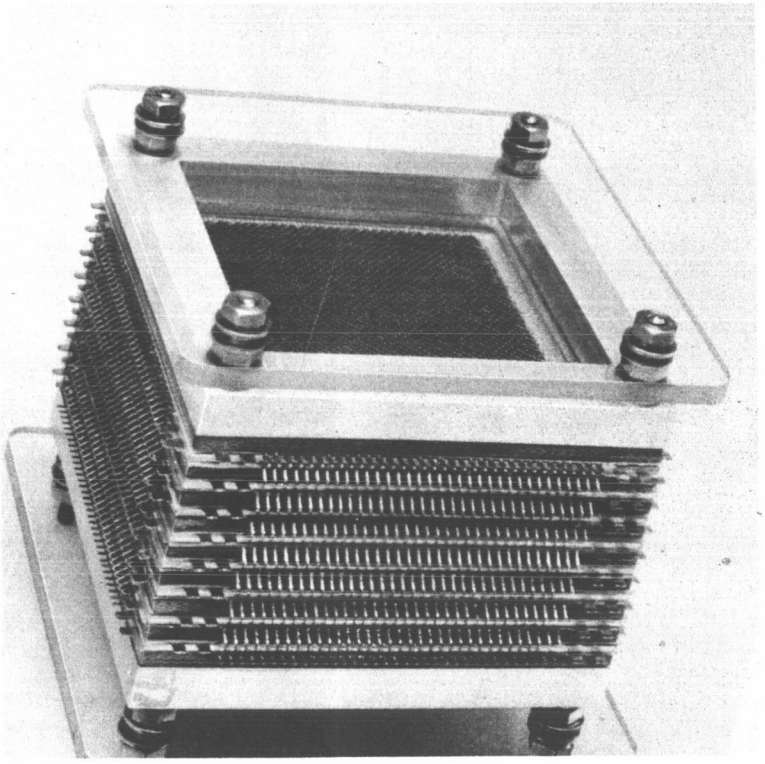


Figure 1-2 ACM LHM Breadboard Sideplate Layout

Figure 1-3 Auxiliary Memory Core Stack Module



Militarized Stack for
Military/Aerospace Applications

Figure 1-4 Militarized Stack for Military/Aerospace Applications

printed circuit boards within the top and bottom end frames respectively.

1.1.2.2 Sense Amplifier Module

This module contains sixteen amplifier circuits and a voltage regulator circuit. The electronic parts are staked into the cavities of a magnesium header with RTV-11 epoxy.

The sense amplifier circuit shown in Fig. 1-5 discriminates between "ones" and "zeros" read from the storage array. It uses a dual differential amplifier, threshold-detector combination. This approach has the advantage of eliminating many of the tolerance problems encountered in the design of a sense amplifier. The sense amplifier threshold is determined by external resistors and is practically independent of integrated circuit characteristics. The dual comparator (uA711) is an integrated circuit manufactured by Fairchild. External strobing of the sense amplifier is accomplished in the memory timing logic.

The output of the dual comparator is designed so that a number of them can be wire-OR'ed to provide a common data path from the memory to the GAM buffer register. Up to eight devices can be OR'ed, yet the outputs will still be compatible with the memory buffer logic. In order to make this OR'ing capability possible and hold the device dissipation to satisfactory levels, the sink current of the comparator must be reduced. As a result, at least four devices must be OR'ed before they can provide for a DTL fan-out of one. Two resistive termination blocks are provided in the ACM for reduction of sink current due to the absence of sense amplifier modules for Memory Units 2 and 3.

1.1.2.3 Memory Electronics Module

This module contains sixteen selection switch circuits (8 top, 8 bottom), two read/write drivers, eight inhibit drivers, three memory select circuits and two filter circuits. The electrical parts of this module are staked into the cavities of a magnesium header with RTV-11 epoxy. The relation of these circuits to an MU system is shown in Figure 1-6.

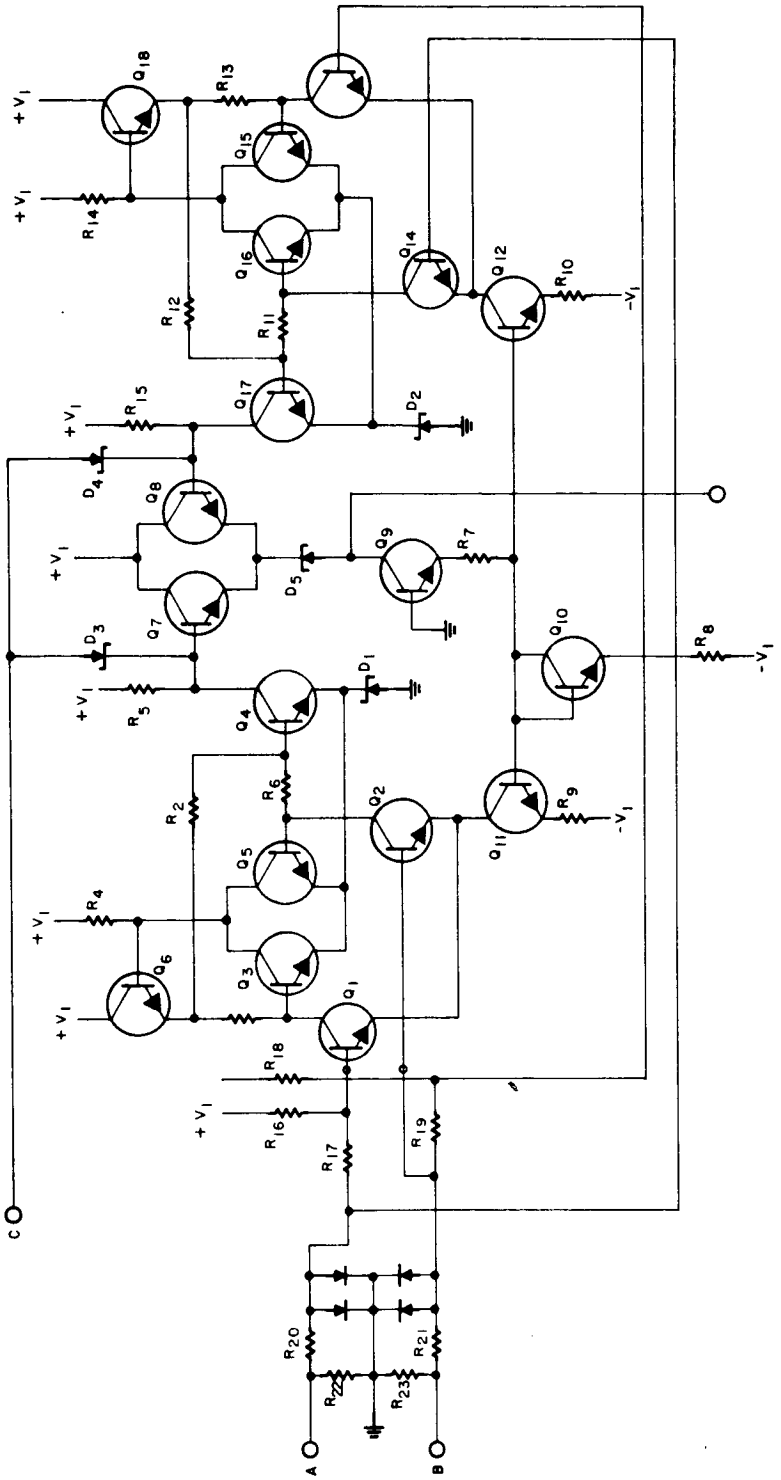
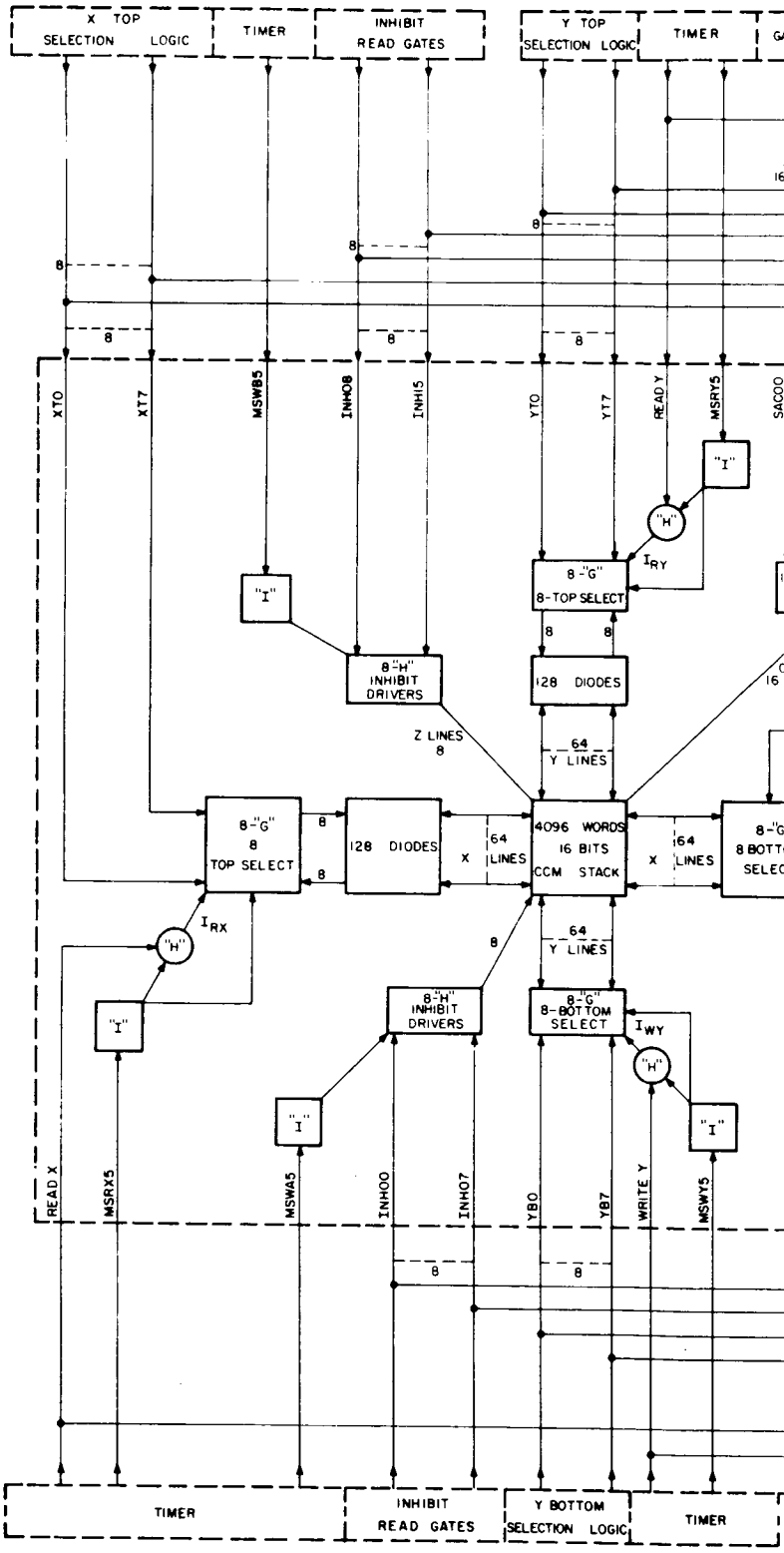
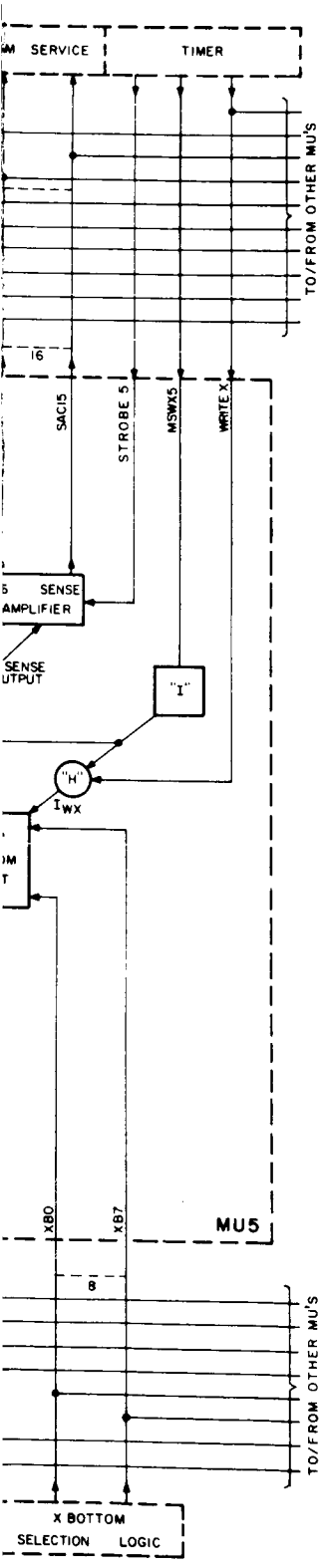
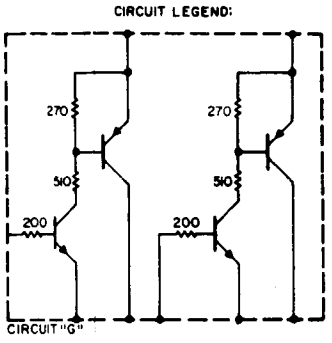


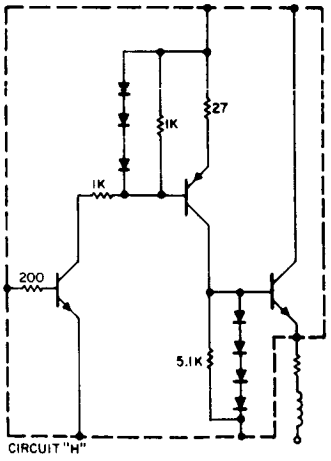
Figure 1-5 Sense Amplifier Schematic



FOLDOUT FRAME 1







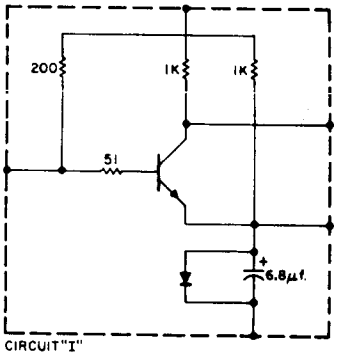


Figure 1-6 MU System

FOLDOUT FRAME 2

1.1.2.4 Mechanical Description of Sense Amp and Memory Electronics Modules

Discrete component modules do not lend themselves to the same kind of mechanized interconnection approach as do the digital type because of the random physical nature of electronic parts and their interconnection; therefore, a greater degree of design flexibility exists. This flexibility is limited somewhat by the size and shape of the digital module which was established in consideration of the many factors involved in packaging high speed, high power, integrated circuits.

The packaging design for the discrete component modules is an adaptation of the welded "cordwood" construction technique, a design governed by thermal considerations and the requirements of high density packaging of non-uniform discrete components. Figure 1-7 is an explanatory sketch of welded "cordwood" construction techniques applied to the Auxiliary Memory Sense Amplifier Module (Figure 2-4) and the Memory Electronics Module (Figure 2-5) manufactured by Raytheon. The component carrying frame is a magnesium alloy structural member that supports heat transfer by conduction. In essence the frame is of I beam construction with a web thickness determined by the thermal dissipation requirements. The frame is C. G. mounted with restraint on 3 edges, and features a high stiffness to weight ratio with resultant high natural frequency. Captive jacking screws, one at each end, mount the module frame to the chassis, forcing engagement of the module connector pins with mating connector pins on the chassis, and providing the necessary bearing pressure required to dissipate the heat to the heatsink.

The components are mounted in machined cavities in the web and the remaining volume is filled with a silastic potting compound to insure minimum thermal resistances between component and frame. This compound surrounds the component on all surfaces contiguous to the frame cavity surfaces. Electrical components having critical operating temperatures are positioned as near as possible to the heat sink. In most cases, signal interconnections are accomplished with two layers of

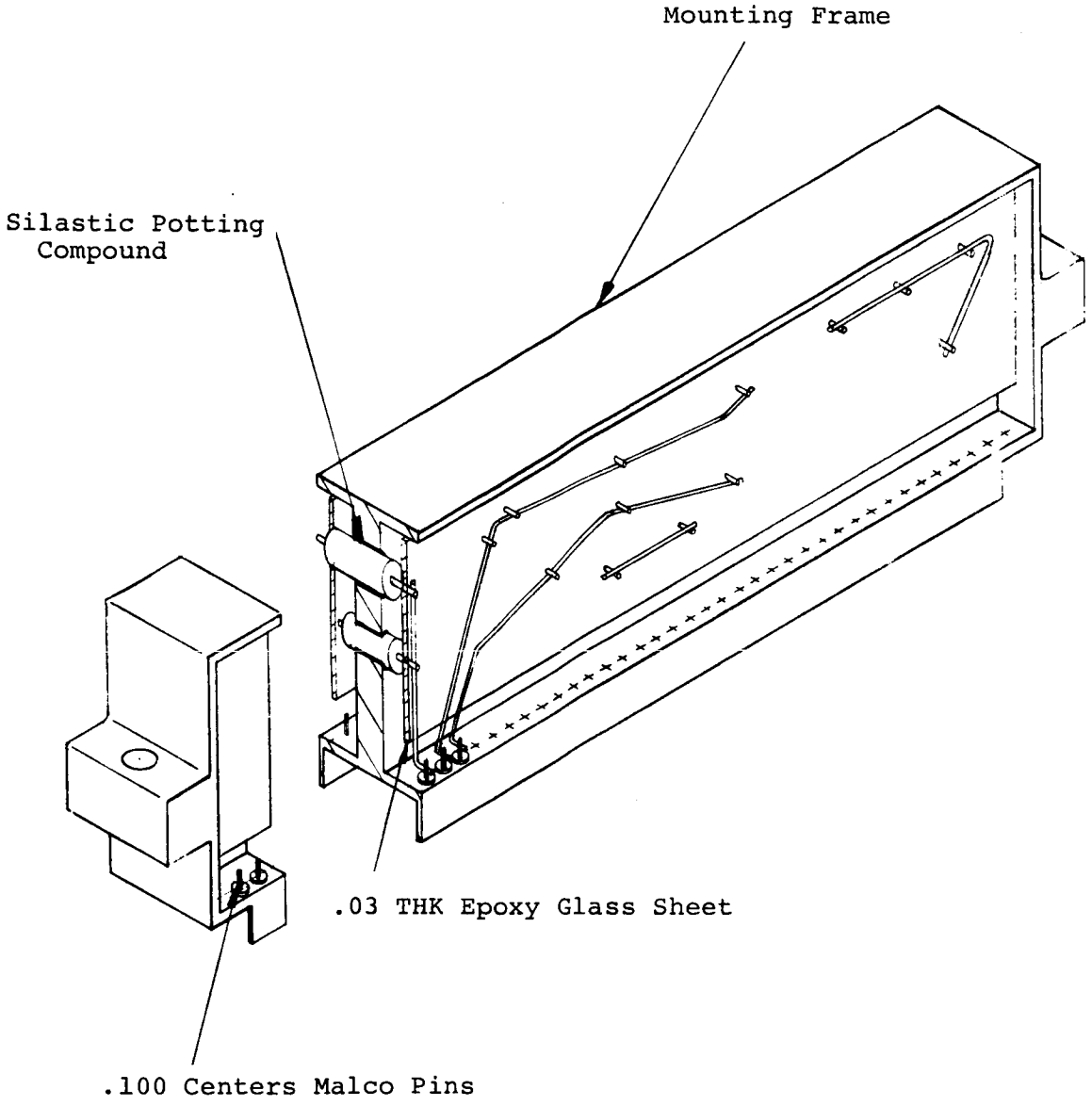


Figure 1-7 Discrete Component Module

point to point welded nickel wire interconnections on each side of the module. This technique has a considerable history of use on analog electronics designed and manufactured by Raytheon for the Apollo, Poseidon, and Polaris Guidance systems. Mylar sheets with photographically imprinted signal wiring patterns are used to position the leads of the components for welding and compensate for the random component lengths.

Nickel ribbon welded connections are made from the required circuit points directly to the module connector pins which are identical for all modules.

1.1.3 ACM POWER SUPPLY

The power supply consists of two magnetic amplifier controlled dc to dc Converter-Regulators, and three series regulators. It also includes the turn on-off circuitry (OUTCOM-4VSW), 28 Vdc Alarm circuit, ACMON (4.4Vdc logic detect circuit), and the 4.4 V Line Driver turn off circuit. The regulators furnish power to the ACM logic, line drivers, memory, and control functions.

Technical specifications and special features of the power supply include the following:

a. Regulated output voltage over a minimum input voltage range of +19 Vdc to 36 Vdc.

b. Current limiting on the +4.4 Vdc logic and +12 Vdc power supplies. Short circuit protection on the 4.4 Vdc, and +14 Vdc power supplies.

c. High impedance isolation between input and signal ground.

d. Output voltages and regulator specifications are as follows:

Output Voltage	Regulation	Average Power	Maximum Current	Maximum Ripple
+4.4 Vdc (Logic)	±5%	22 watts	8 amperes	5%
+12.0 Vdc	±5%	17 watts	2.5 amperes	5%

+ 4.4 Vdc (Line Driver)	± 5%	0.4 watts	0.1 amperes	5%
+14.0 Vdc	± 5%	28 watts	3.0 amperes	5%
-5 Vdc	± 2%	1.9 watts	0.7 amperes	2%

The power supply consists of two multivibrators which generate the driving square waves at a frequency of approximately 10 kHz. The multivibrators operate in a free running mode during power turn on and until such time as the ACM logic furnishes the necessary sync pulses. The multivibrator is then synchronized to 12.5 kHz, a countdown frequency of the 1.024 MHz frequency from the AGC. The multivibrator design features low power consumption and minimum change in frequency during variations of the 28 Vdc input.

A block diagram of the ACM power supply is shown in Figure 1-8.

With the exception of the magnetic amplifier circuitry, series regulators, and control circuits, the supply circuit configuration is that of a square wave driven dc to dc transformer coupled converter. Line and load regulation for 4.4 Vdc and 14 Vdc supplies is accomplished by generating a symmetrical pulsewidth control signal proportional to the difference between the output voltage (which is converted to current by a precision resistor) and the reference source.

The voltage control magnetic amplifier shunt modulates the base drive of the power amplifier stage, providing the pulsewidth control and summing function for regulation. Short circuit protection is achieved by a series limiting the base drive to the power amplifier stage with a magnetic amplifier which senses the output current.

This magnetic amplifier is normally saturated and has little effect on circuit operation except in the event of an overload condition. In an overload condition the magnetic amplifier regulates the pulsewidth to limit the base drive.

Regulation for the + 4.4 Vdc (Line Drivers), +12V and -5V

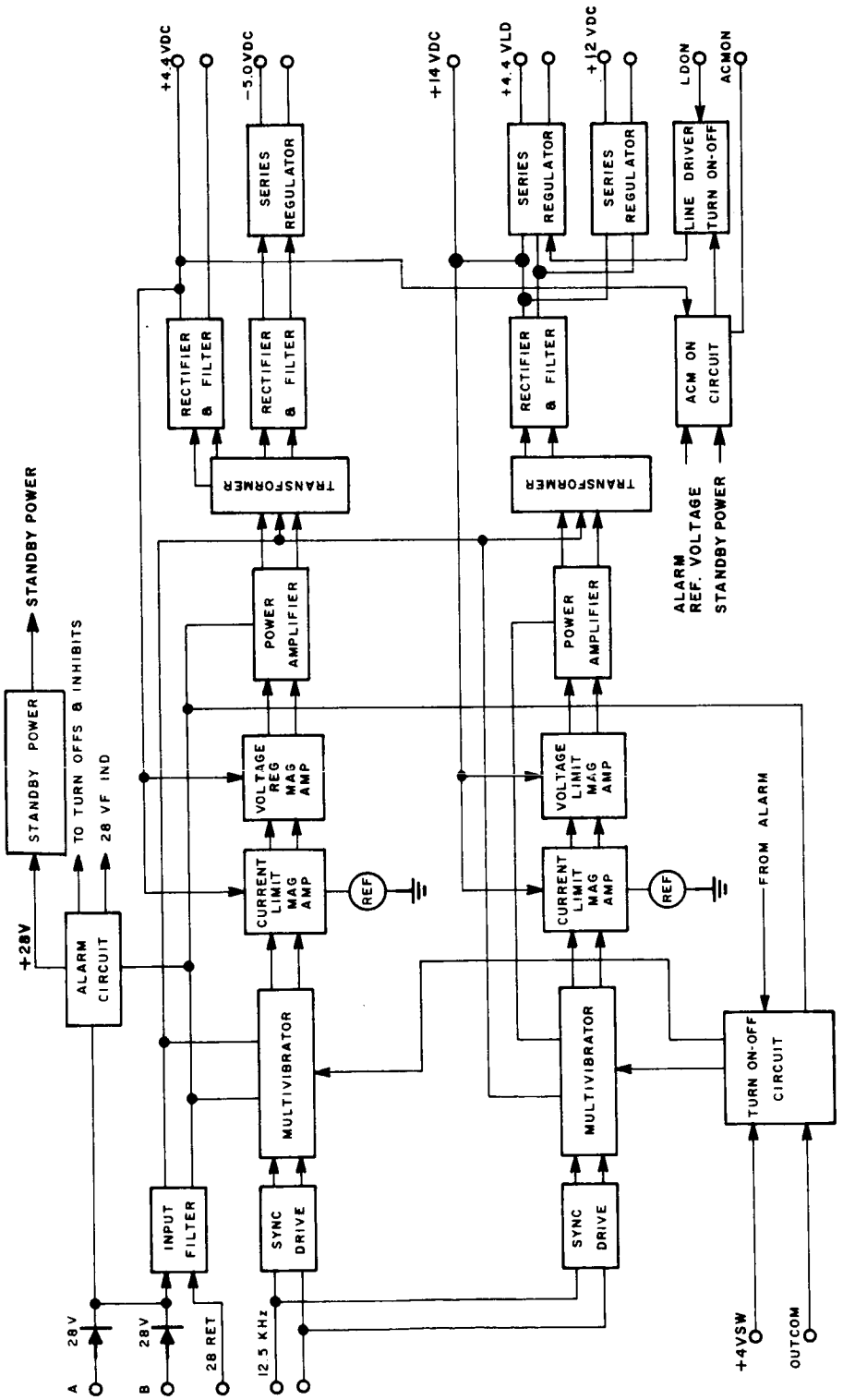


Figure 1-8 Power Supply Block Diagram

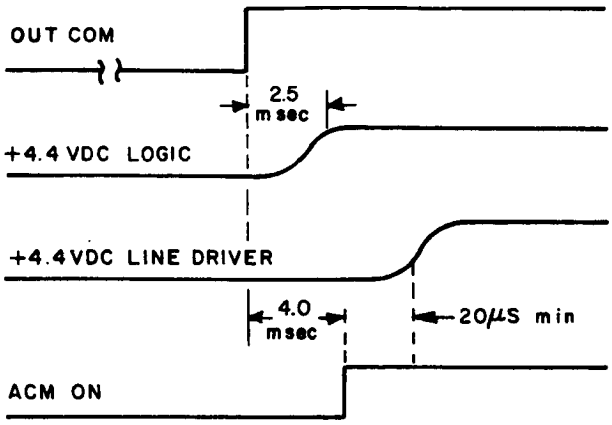
supplies is achieved by means of series type regulators. The transformers used to furnish the +4.4 VDC and +14 VDC also provide the necessary AC signals, which after rectification and filtering provide the power for the -5 VDC, +4.4 VDC and +14 VDC regulators. Some regulation for line changes is obtained by the magnetic amplifiers used to regulate the +4.4 VDC and +14 VDC supplies.

The input filter provides transient attenuation, power line isolation, and energy storage capability to furnish power to the ACM regulators during a short power failure. A failure period of 300 μsec can be tolerated with the filter design.

The turn on-off circuit (OUTCOM, +4SW) restricts the operation of the ACM power supply, and therefore the ACM, to only those periods when both a +4 SW and OUTCOM signal are present. The lack of either one or both signals turns off the power supply. A delay of approximately one hundred milliseconds is provided within the circuit for continuous operation of ACM power supply during short transients in the OUTCOM signal.

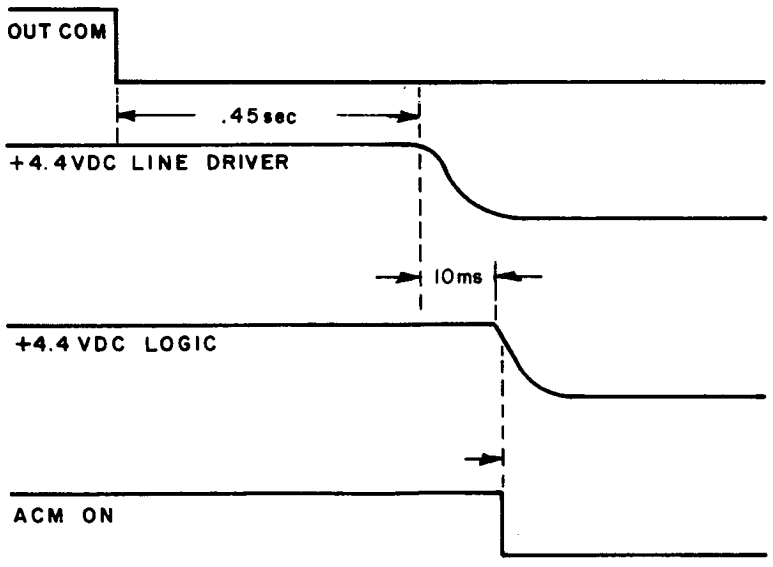
A 28V Alarm Circuit monitors the 28 VDC (at the input of the filter). The Power Supply is turned off by the alarm circuit when the 28 VDC line is reduced to a level of 19.9 VDC or less. A filter delay is provided to prevent premature alarms due to a transient loss of the input voltage. The circuit will also detect an increase in line level above 35.5 VDC and then turn off the power supply. An ACMON circuit is also utilized as a monitor and controlling circuit, regulating turn off timing between the 4.4 volt logic supply and the 4.4 volt line driver supply. It also monitors the 4.4 VDC (logic) for proper level.

Figure 1-9 shows the relative timing of ACMON with respect to the signal OUTCOM. This assumes LDON/ is controlled by the logic.



NOTES: ASSUMES 28 VOLTS IS ON, +4V SW ON, LD ON/ IS A "0"

TURN ON



LDON/ IS A "0" UNTIL OUTCOM GOES DOWN, LDON/GOES TO A "1."

Figure 1-9 Power Supply Characteristics

The ACM power supply module which mounts in position AØ1 on the ACM Tray is shown in Figures 1-10 and 1-11. This supply exhibits an overall efficiency in excess of 75%. The output voltages are +4.4 VDC, +12 VDC, +14.0 VDC, and -5 VDC. Power output capability for this power supply was a total of 76 watts. Regulation was better than ± 3% for all voltages.

1.2 INTERFACE MODULE

The IM provides buffering for AGC outputs and noise rejection for AGC inputs at the test connector. The major problem in interfacing the ACM with the AGC is the time delay and pulse waveform degradation resulting from the length of the connecting cable and its associated capacitance. The negate these effects, line drivers located in the IM and ACM are provided for each of the interfacing signal lines.

The IM is placed as close as possible to the AGC by plugging the IM directly into the AGC A52 connector to minimize cable effects.

AGC signals destined for the ACM are processed in the IM by Signetics type SE156J Line Drivers. These are low source impedance (100 ohms) devices with transistor pull-up and are capable of driving reasonably high capacitance loads.

The input current supplied from the line driver to the collector of the AGC Nor gate will not exceed 2 ma under all conditions of temperature and voltage. The IM line drivers for the ACM signals and GSE signals are powered separately. The GSE supplies +10 VDC power for the +4.4v zener diode supply which powers the GSE line drivers within the IM. External +4.4 VDC power must be supplied separately for powering the ACM line drivers within the IM.

1.2.1 ELECTRICAL DESCRIPTION

A total of 92 line drivers are provided for the AGC signals; sixty are shared by the ACM and GSE, including spares, while 32 are exclusively used by the GSE.

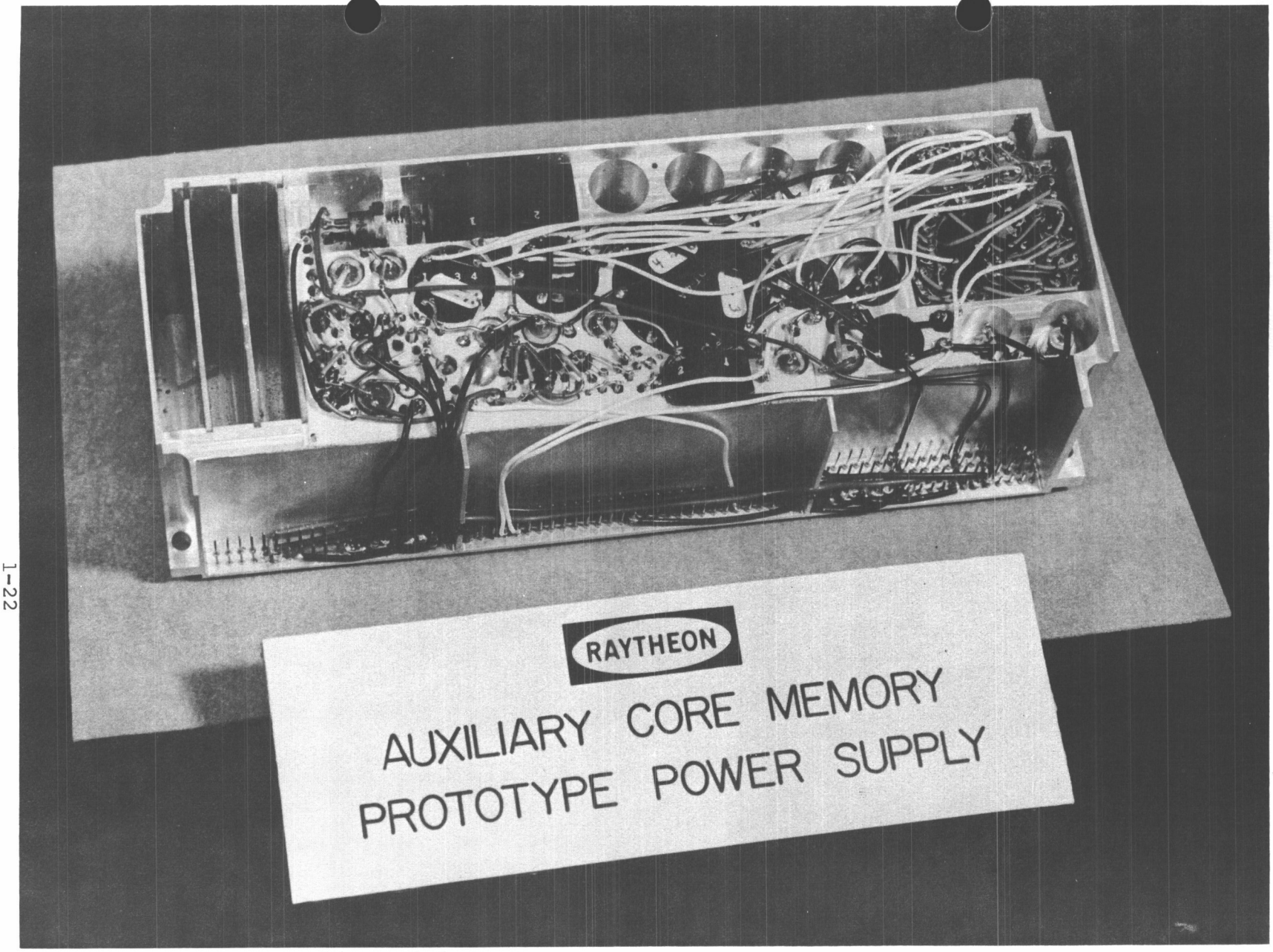


Figure 1-10 ACM Prototype Power Supply, Top View

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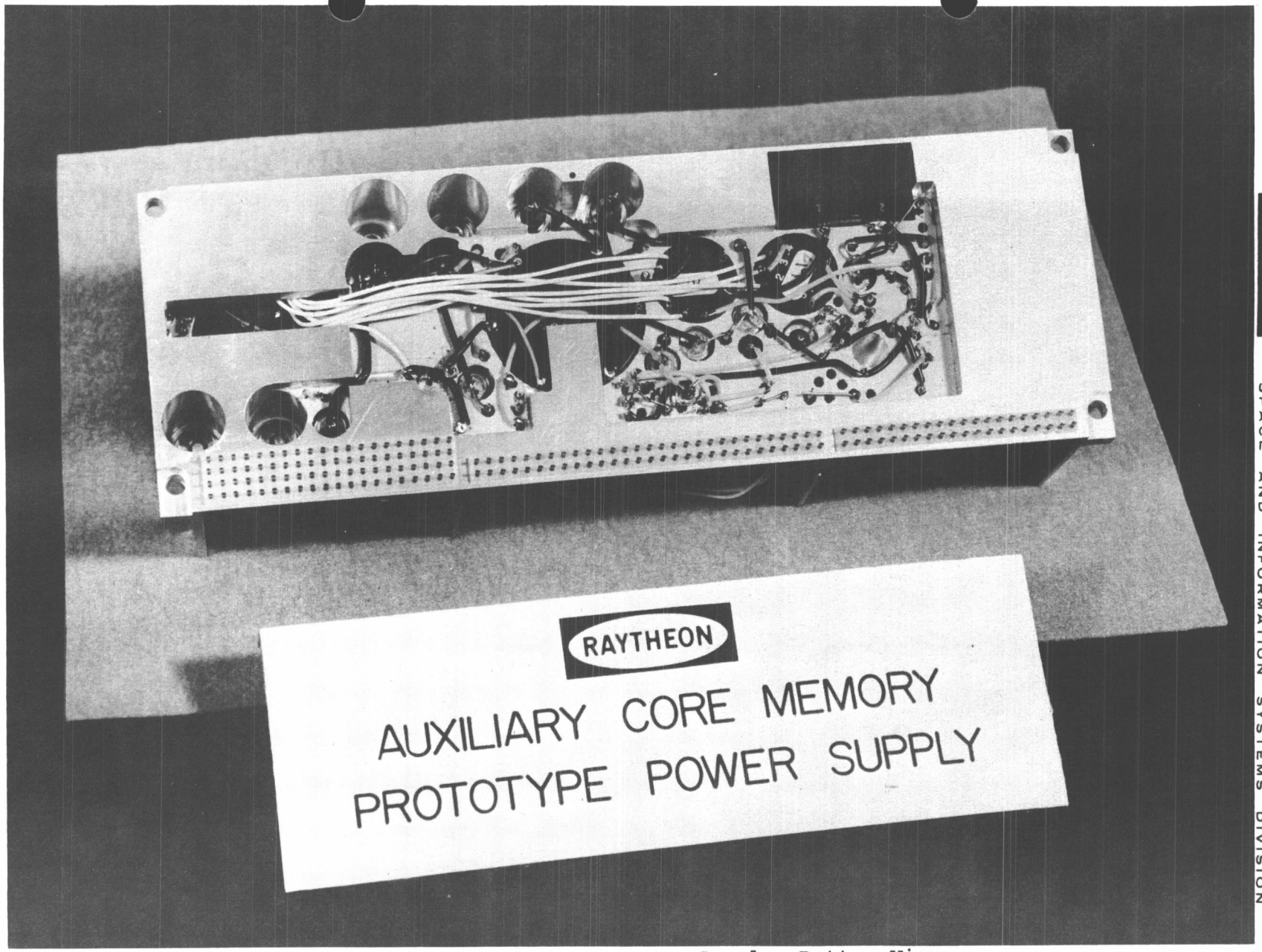


Figure 1-11 ACM Prototype Power Supply, Bottom View

CN-4-716

A total of 40 noise rejection circuits protect AGC input lines from noise introduced in the cables from the ACM and the GSE. The routing of wires through the connector and the isolating components are shown in Appendix C.

1.2.1.1 AGC-IM-ACM Interface

The configuration shown in Figure 1-12 is used for all AGC outputs. The cable length was maintained at five feet to minimize the delay between the AGC and the ACM.

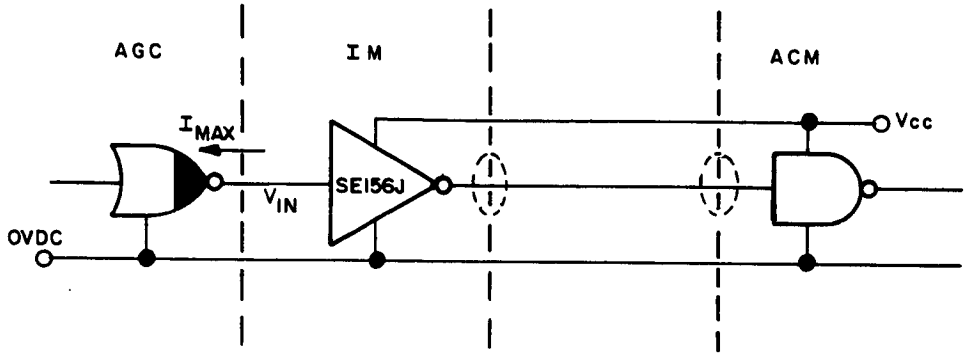
Two AGC output signals, OUTCOM and the 4.4v SWITCHED, are not serviced by line drivers: OUTCOM is handled as a wire connection and 4.4v SWITCHED is wired with a series current limiting resistor to protect the AGC.

Signals to the AGC from the ACM require noise rejection in the IM to provide noise immunity for the sensitive inputs of the AGC NOR gates. Each signal from the ACM as shown in Figure 1-13 passes through a diode for noise rejection. A resistor to ground provides a bleed path for the base current of the AGC NOR gate when it is turning off. Although the output impedance of the SE 455J line driver (200 ohms) is higher than the SE 156J, resulting in a slight reduction of speed, it has been chosen to provide output levels which will not be above 0.2 volts at the input to the AGC in the event of an ACM power failure.

The cable harness from the IM to the ACM includes individual shielded wires to minimize cross talk between signals, and an outer shield to provide RFI interference protection.

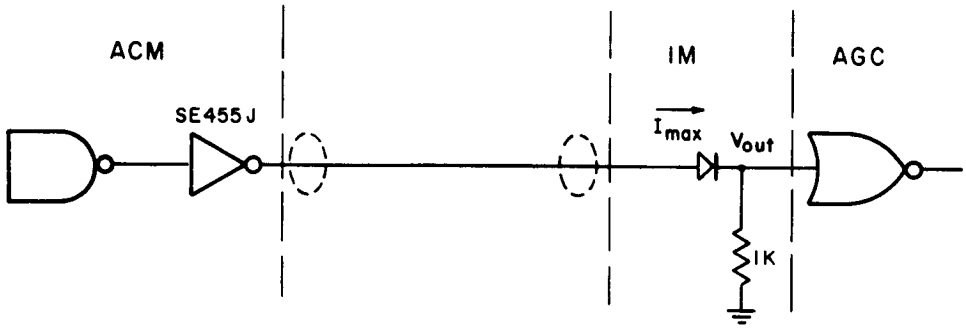
1.2.1.2 AGC-IM-GSE Interface

The present interface between the AGC and GSE is maintained by including a GSE section in the Interface Module (Figure 1-14).



	MAX	MIN
I_{MAX}	2.0 ma	
V_{IN} LOGIC 1	6 V	4.0 V
V_{IN} LOGIC 0	0.2 V	0.0V

Figure 1-12 AGC to ACM Signal Interface



	MAX	MIN
I_{max}	2.0 ma	
V_{out} LOGIC 1	3.0 volts	0.825 volts
V_{out} LOGIC 0	0.2 volts	0.0 volts

Figure 1-13 ACM to AGC Signal Interface

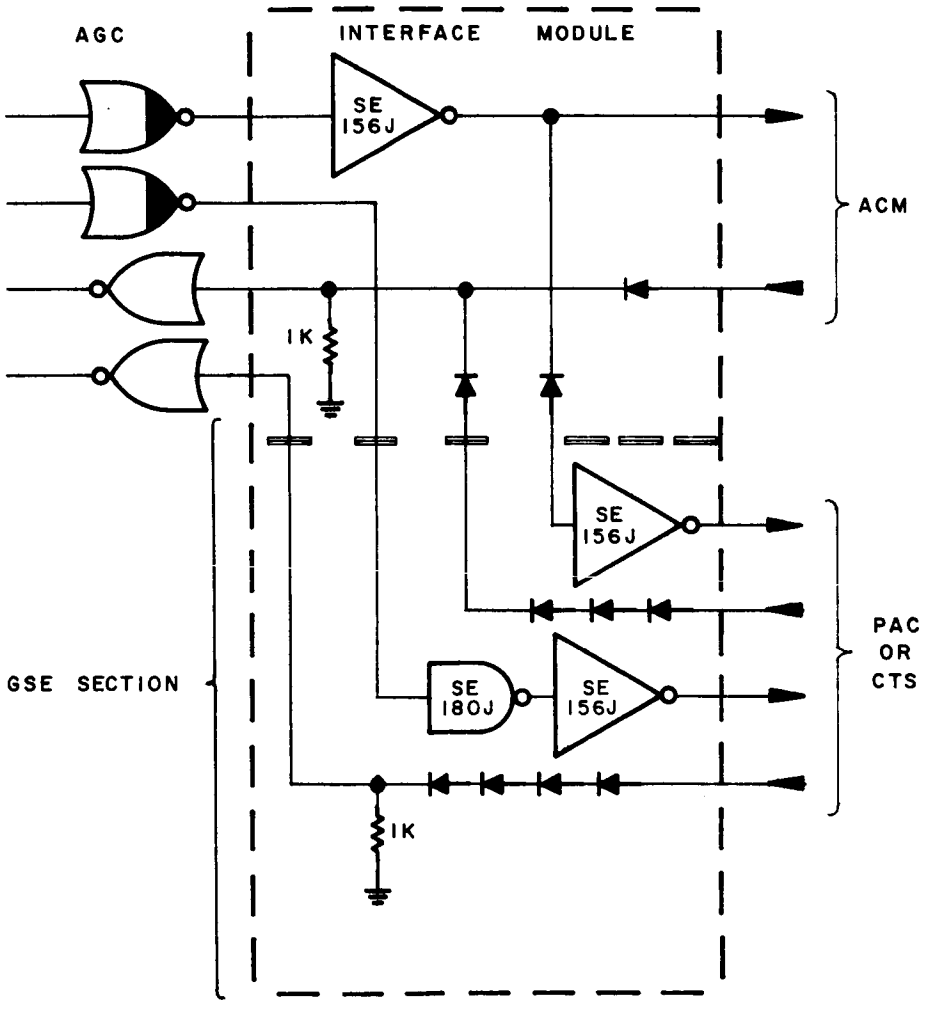


Figure 1-14 AGC to GSE Interface Signals

This technique replaces the present Buffer Circuit Assembly and its short cable (2 feet) between the AGC and the Buffer Circuits of the Program Analyzer Console (PAC) or Computer Test Set (CTS) when the AM system is installed. The GSE cables connect to the GSE section which mounts to the buffer circuit bracket assembly for strain relief. The current interface to the Program Analyzer Console (PAC), or the Computer Test Set (CTS) is preserved. The PAC, which has similar time delay problems as the ACM, achieves a significant reduction in delays now caused by the cable between the AGC blue nose and the buffer circuit.

1.2.2 MECHANICAL DESCRIPTION

The Interface Module (IM) is designed to be mounted to the AGC test connector, A52, by means of its own captive hardware. On top of the IM are connector receptacles for the GSE and ACM cables. The IM also provides those functions which are found on a GSE buffer circuit assembly such as: the ALGA switch, the STRT1/STRT2 switch and BNC connectors for MTHI and MTLO. There is no provision for exercising the self-test feature of the GSE with the Interface Module installed, because the GSE section is an integral part of the IM.

The IM consists of 24 printed circuit boards of seven types mounted in a common frame. The printed circuit boards are listed by type in Table 1-2.

The two cables between the IM and the ACM (See Figure 1-15) are connected by Deutsch connectors (44 pin connector on the ACM side and an 85 pin connector on the IM side; reference drawings 366048 and 366049. Low capacitance coaxial cable is used in the cables with each coax shield terminated at logic ground at each end. An outer electrostatic shield is also provided for RFI protection, with the termination made on the outer shield of the connectors at each end.

TABLE 1-2

IM PRINTED CKT BOARD TYPE

TYPE	QUANTITY	FUNCTION
A	4	AGC to GSE
B_1	2	ACM & GSE to AGC
B_2	2	GSE to AGC
C	4	GSE diodes only
D_1	5	AGC to ACM & GSE
D_2	5	GSE LD only
E	2	Discrete Components

1.3 AUXILIARY TAPE MEMORY

A simplified block diagram of the auxiliary tape memory is shown in Figure 1-16. The unit is a complete digital recorder system which contains all sections necessary for operation of the unit. This includes tape transport, read and write electronics, control logic, motor drive circuits, and power supply.

The recorder is an eighteen channel unit designed to record and reproduce digital information in parallel at 12.8 kiloframes per second. Five hundred-fifty feet of one inch heavy duty instrumentation tape yield a total information capacity of approximately 1×10^8 bits. The tape speed is fifteen inches per second and the digital packing density is 853 frames per inch or 853 bits per channel-inch.

Accurate tape speed is maintained by use of a hysteresis synchronous motor slaved, ultimately, to the guidance computer master clock. A photo-electric sensing mechanism limits tape travel, and provides end of tape information to the control circuit.

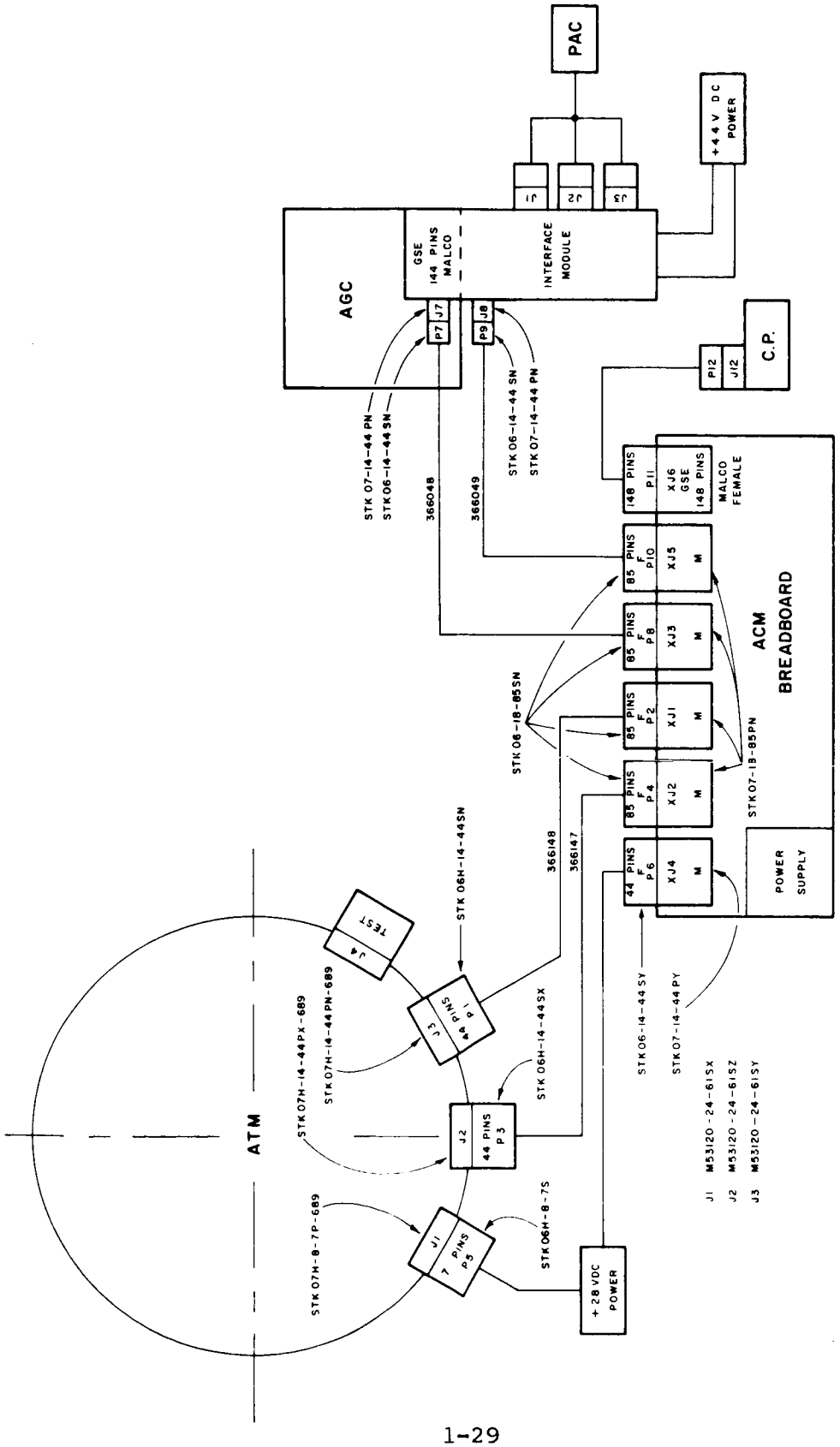
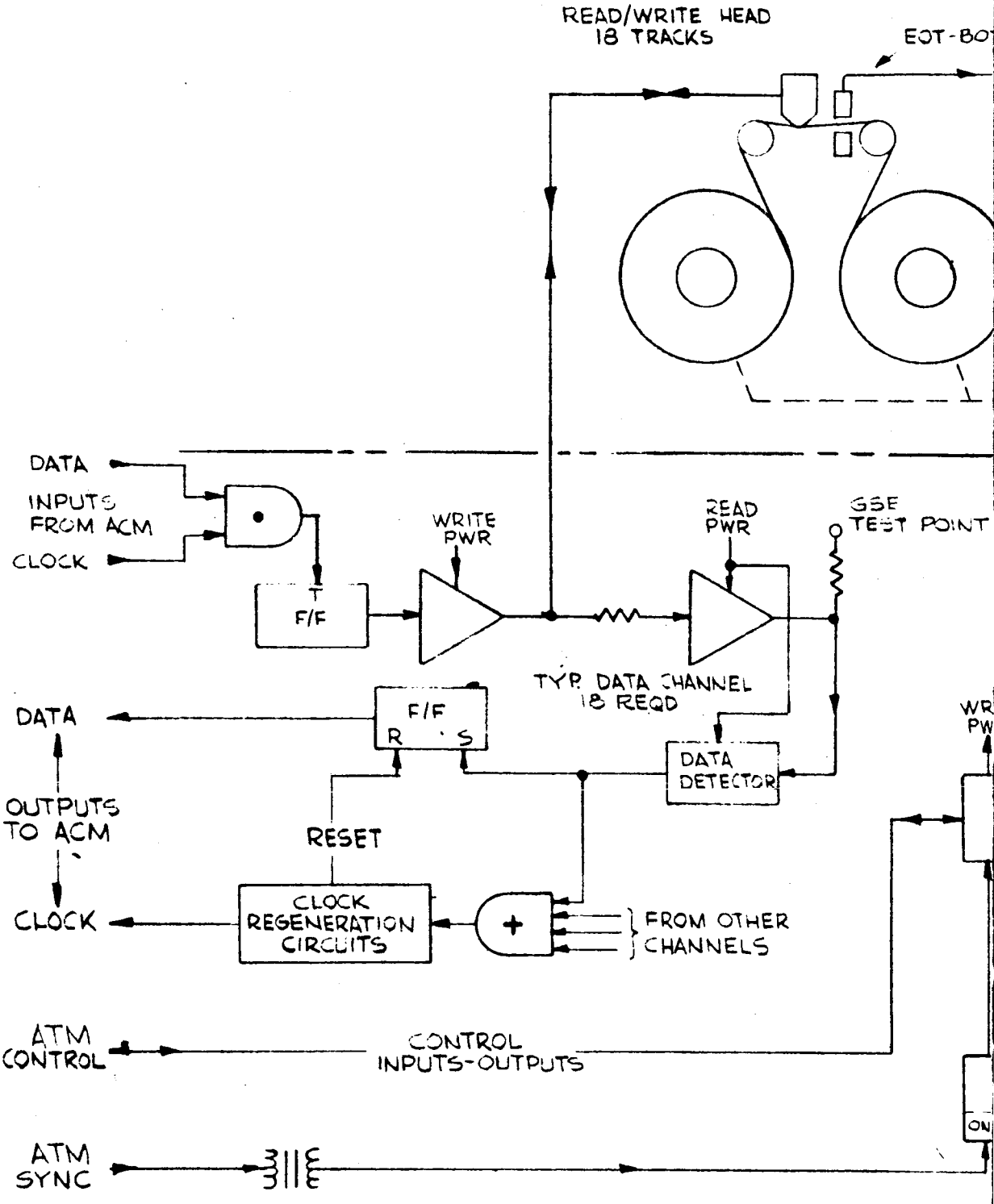


Figure 1-15 Wiring Diagram - ACM, ATM, and AGC



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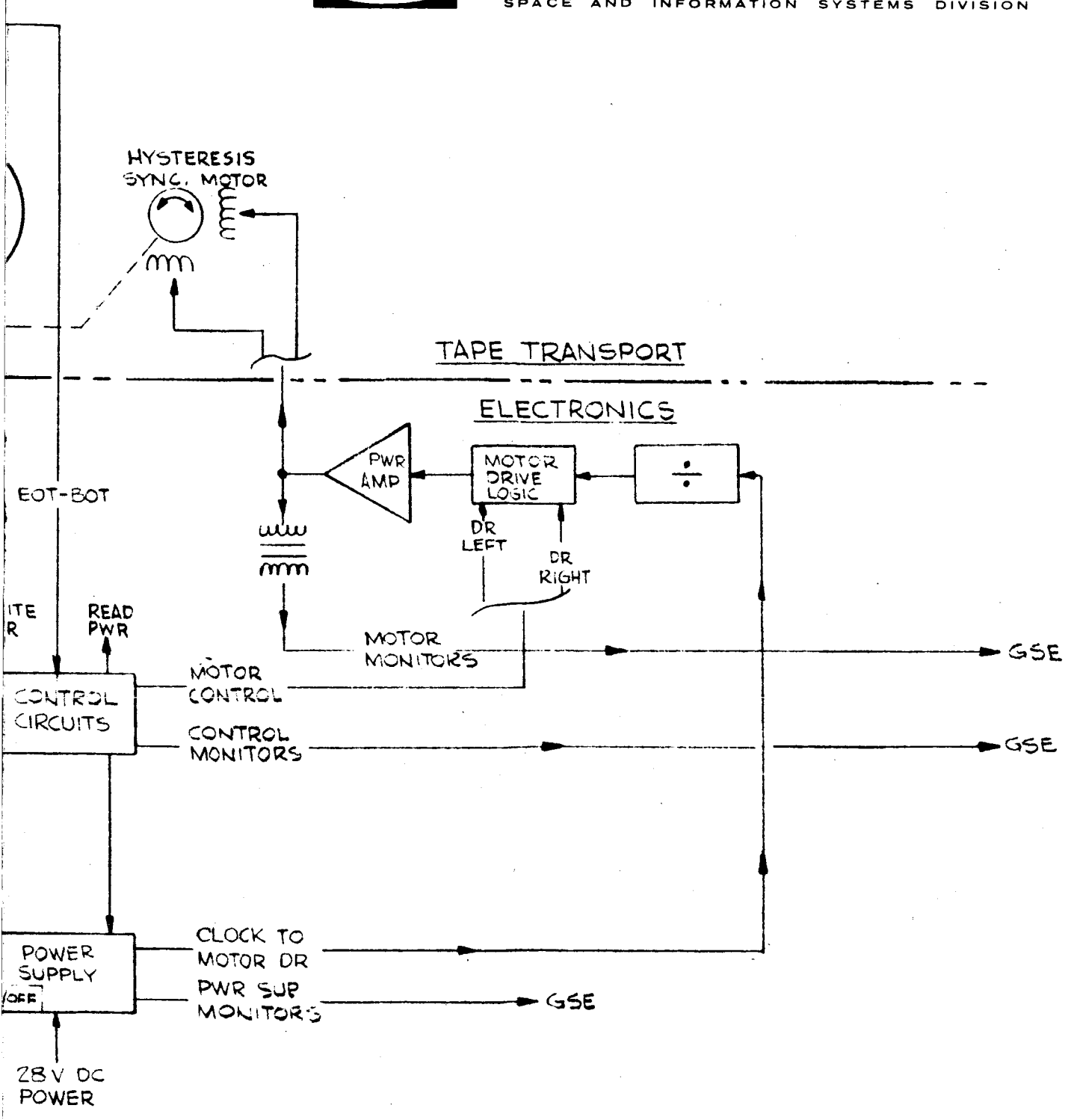


Figure 1-16 System Block Diagram: Apollo DVT/ATM

Control of the recorder is established by hybrid (logic element - discrete component) circuits especially designed to protect recordings from accidental erasure, prevent damage to components and interface with the ACM control section.

An integral power supply furnishes the various voltages used throughout the system. The power supply operates from the 28 VDC main bus. On-off control is achieved by sensing the presence or absence of a 25.6 KHz synchronizing signal from the ACM. A dc to ac power inverter and constant efficiency chopper regulator are each phase-locked to the ACM signal to assure stable operation and reduce line noise effects on the overall system. Because the power supply is synchronized to a frequency stable source, it is convenient to control the tape transport speed by dividing down the 25.6 KHz power supply signal to derive ac drive to the synchronous motor.

Various test points are provided to verify proper operation and to aid in locating trouble spots. Test connector outputs are provided for monitoring major parameters, including power supply outputs and amplified playback signals.

Characterists of the ATM-DVT system are:

a. Form Factor -Cylindrical, 9.8 inches maximum diameter x 8.0 inches maximum height

b. Weight -Approximately 18 pounds.

c. Power -28 VDC, 20 watts. Less than 20 watts in worst case operation mode.

d. Data Capacity -18 channels, 5.6×10^6 bits per channel or 1×10^8 bits total.

e. Bit Density -853 bits per inch per track.

f. Code Format -18 channel parallel format, channels arranged in three sets of six channels each. Each set has five data channels plus odd parity.

g. Data Rate -12.8 KBPS per channel.

h. Tape Speed - 15 ips.

i. Tape Length -550 feet.

1.3.1 ELECTRICAL DESCRIPTION

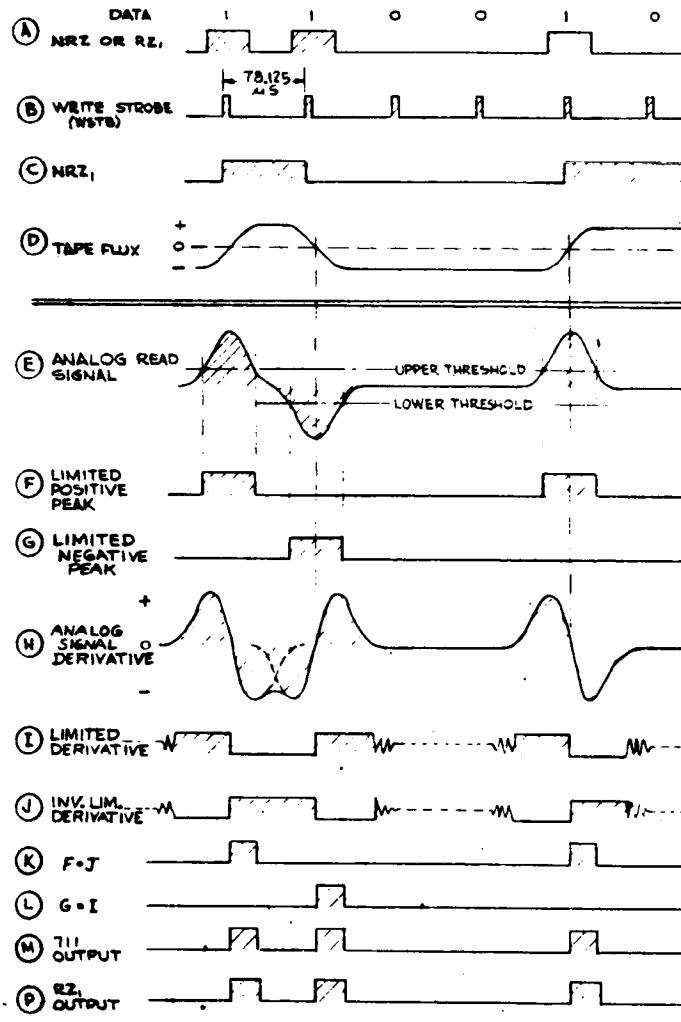
1.3.1.1 Read/Write Electronics

Figure 1-17 depicts a hybrid diagram and waveform chart for a typical read/write channel. Eighteen channels, identical to that shown, are provided.

Operation of the circuit may be best explained by considering the recording method. The code format selected for use in this system is NRZ_1 (sometimes referred to as NRZ1 or NRZ-MARK). This format is defined as a change-of-state or inversion of tape flux for each logical "one" to be recorded. Saturation recording is used, with overdrive sufficient to completely erase or rewrite previous recordings. The coding format, by definition, implies a system where only flux transitions are of importance; thus the direction of the tape flux is not controlled. It is important to consider that application and removal of head power, during the course of making a recording, will introduce flux transitions in an unpredictable manner because the flux state of both the previous and new recording is unknown and uncontrolled.

Because of this, the head power programming circuit was developed to prevent readable marks from appearing on the tape when record power was switched on or off. The circuit was set to provide a ramp increase/decrease of "write" voltage with a nominal transition time of 2.5 msec.

During the writing process, a direct current is applied to one or the other winding of the read/write head. The head driver is designed to be a constant current source to the head. The output of a T type flip-flop determines which head winding is receiving current. When a logical "one" is to be written, a pulse appears on the WTRK line, strobed in the center by a clock pulse, (write Strobe), which toggles the flip-flop to its complementary state. The head driver is disabled during



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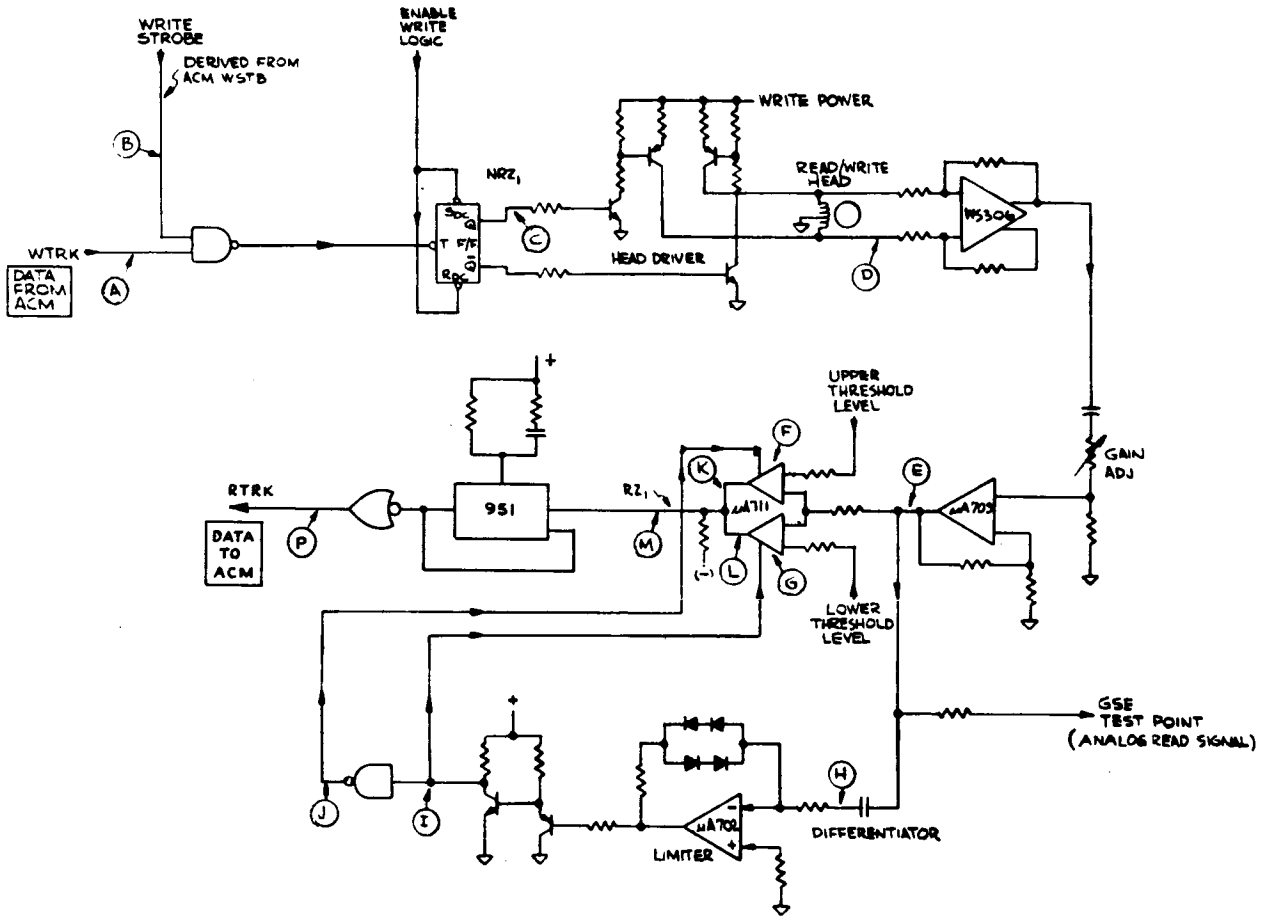


Figure 1-17 Read/Write Electronics: Apollo DVT/ATM

FOLDOUT FRAME 2

read operations by removal of write power and application of both a dc Set and a dc Reset to the flip-flop, causing both outputs to rise to an "up" level and saturate the NPN stages of the head driver. This precaution is taken to assure that noise pulses on the write lines will not couple through to the read amplifiers during tape reading operations.

The writing process results in the tape's saturation, approximately as shown in the waveform chart. The relatively poor flux transition definition is a characteristic of the tape itself, related to the oxide thickness and formulation. It is not affected by head current rise time provided that adequate design margins are used.

Once a recording has been made, the head, when passed by an NRZ_1 transition, will produce a push-pull analog signal which approximates the time derivative of the flux transition seen by the head gap. We use the term "approximate" because the head actually responds to the rate of change of the average flux seen by the gap. This fact is used to advantage in limiting the bandwidth of the head tape combination to the optimum point by increasing the gap dimension to the point of incipient pulse crowding at maximum packing density. In this system maximum packing density on any channel occurs when a series of logical ones is written.

The read amplifier consists of a differential preamp to ensure noise immunity, followed by a single-ended stage with gain adjustment provisions. Both stages are integrated circuit operational amplifiers adapted to the application by the addition of appropriate discrete components. Sufficient gain is thus available to allow for read-write head variations and to provide some design flexibility. The analog output signal is applied to a peak detector circuit for conversion to digital form.

Peak detection is accomplished by logically ANDing the selected amplitude limited peaks of the read signal with the appropriate (in phase or inverted) amplitude limited derivative of the same signal.

Pulses must exceed the threshold levels before detection can occur. The results of the ANDing processes are ORed together and appear at the output of the dual voltage comparator (μA711). The amplitude limited derivative of the analog tape signal is produced by means of a passive R-C differentiator followed by a symmetrical limiter and dc restorer. The waveform appearing at the output of the dc restorer is a standard logic signal compatible with the other logic elements. AND and OR functions occur within the dual voltage comparator and are not observed in actual practice. An additional AND function separates positive pulse and negative pulse outputs for application to the voltage comparator. The output of the comparator drives a one-shot which reproduces the waveform introduced to the head driver during the writing process.

1.3.1.2 Control and Signal Electronics

A functional description of each signal control interface between the ACM and the ATM follows to illustrate the features of ATM control. For a more detailed electrical description see Appendix A.

WNTRLK-Write Interlock

This line is provided so that the writing capability of the recorder may be inhibited, as the AM system requires, to improve operational reliability. Such a step might be taken where software or hardware confidence is not high and maximum protection of any programs stored in the ATM is desired. A switch on the control panel jumps the signal to ground to inhibit the write function and is left open for normal operation.

NBLWP, NBLWD-Enable Write

Write head power is applied when NBLWP or NBLWD is brought to an up level, provided other conditions are met. First, the ATM Enable Timer must have run down to produce a "1" at its output. Second, the

tape must be at operating speed, i.e., a forward tape motion command must be present and the One Second Timer must have run down. Third, there must be no read command present.

WOVRYD-Write Over-Ride

It is quite often necessary to completely erase sections of the tape which is difficult due to interlocking control features. Write over-ride is a highly noise immune test input which can force head power on regardless of whether the tape is in motion. The use of this function is restricted to GSE operations and a switch provides this function on the control panel.

RTAPE-Read Tape

The read tape line, when up, applies power to the read electronics. It is interlocked with the OR of the tape motion commands to conserve power when the tape is not being used and with the write override command to prevent overloading the power supply with both read and write electives on at the same time.

TMREV, TMFWD - Tape Moving

The output of the One Second Timer is sent to the ACM to indicate when a tape motion command has been received and acted upon. The timer is enabled when the ATM Enable Timer has run down and when either tape motion command is present.

EOT, BOT, COT - End-of-Tape, Beginning-of-Tape, Center-of-Tape

Whenever an end-of-tape or center-of-tape window is over its associated light sensor, the corresponding output to the ACM is at an up level.

GOFWD, GOREV - Go Forward, Go Reverse

These lines are the tape motion command lines for the ATM. The logic is arranged so that the system will respond to only one command at a time. Commands which would tend to drive the tape off of the

reels are inhibited by the end-of-tape circuits. A small delay is incorporated in each command line to allow the One Second Timer to reset in the event that a rapid change of command occurs.

ATMON-ATM Not On

An output status signal will be at "0" whenever the ATM is ready to provide and accept control signals. Otherwise the signal is at a "1" when the ATM is off, where the voltage is supplied to this circuit by the ACM.

ATMNBL-ATM Enable

The ACM may enable or disable the ATM by means of the ATM Enable line. In the event a rapid shutdown of the system is desired, a down level at the ATM Enable line will disable the ATM within a few microseconds. Enabling the system is delayed by the rundown of the ATM Enable Timer.

ATMVFL-ATM Voltage Failure

Qualitative ATM power supply status is conveyed to the ACM by means of the ATM Voltage Failure line. When the system is operating, an up level serves to warn the ACM that a disabling power interruption has occurred and that ATM self-shutdown is imminent.

ATMSNC & ATMSNC/ - ATM Synchronization

A dual polarity 25.6 Hz square wave input provides a synchronizing signal to the power supply and acts as the normal turn on-off function of the ATM.

WSTB-Write Strobe

An ATM input which strobes the incoming data (WTRK's) to the ATM.

RTRK01-18 Read Tracks

A parallel arrangement of 18 pulse output signals represents information read from the 18 separate tape track positions.

WTRK01-18 Write Tracks

A parallel arrangement of 18 pulse input signals will record in NRZ-1 format on 18 separate tape track positions. Each track will have corresponding read and write lines: WTRK01 corresponds to RTRK01, etc. The input data is strobed into the ATM via a pulse (WSTB) located central to the incoming data pulse.

1.3.1.3 Motor Drive

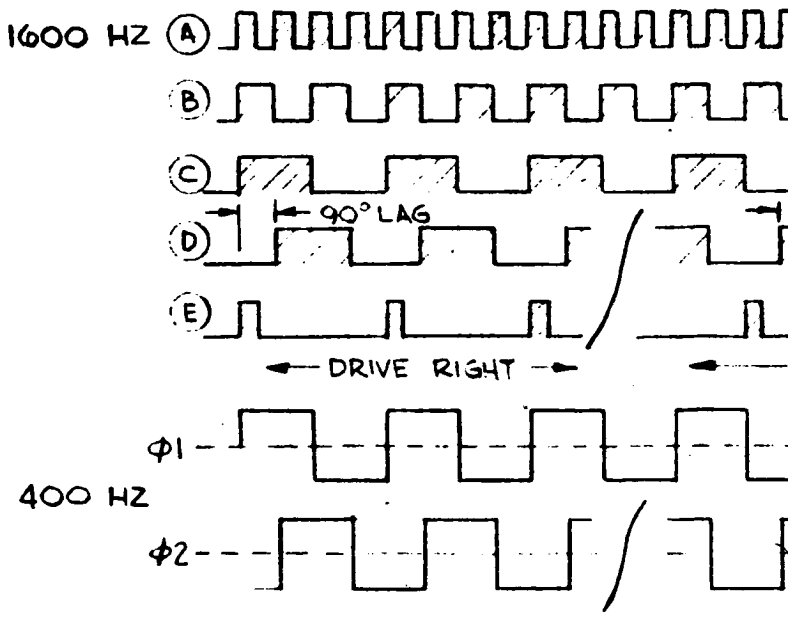
A block diagram encompassing the essentials of the motor drive and control electronics is shown in Figure 1-18.

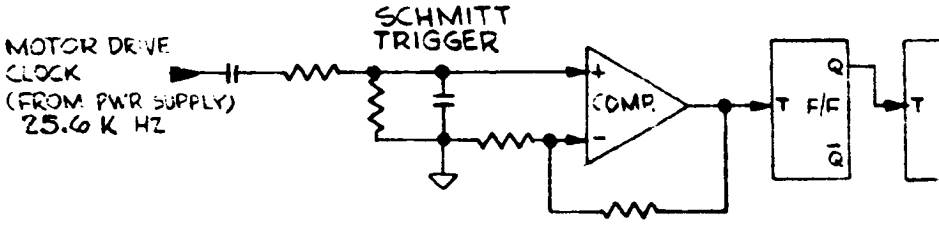
The motor drive logic circuitry and power amplifier was adapted from previously qualified recorder designs which have been proven highly efficient and reliable. The basic clock for the motor drive is obtained from the power supply, filtered and sharpened by a Schmitt trigger, and divided down before being applied to the phase splitter and direction control. The phase splitting and direction control circuits serve to transform the oscillator signal into two signals which are identical in frequency and shape but 90° out of phase. The relative phase between the two signals (i.e., $+90^{\circ}$ or -90°) can be selected by applying the proper direction logic to the circuit.

Two phase push-pull output signals are fed to two identical transformer coupled bridge type power amplifiers. This concept of motor drive has been used in many REL record systems. It has proven a highly stable and efficient drive which is well suited to applications where ease of control and manufacture and mandatory. Due to this system, tape speed stability problems are avoided.

1.3.1.4 Power Supply

A block diagram of the present Apollo ATM Power Supply is shown on Figure 1-19. This supply is especially designed for use in the Apollo ATM-DVT, and represents a significant improvement over previous recorder supplies. The Power Supply contains no relays. Control is by standard





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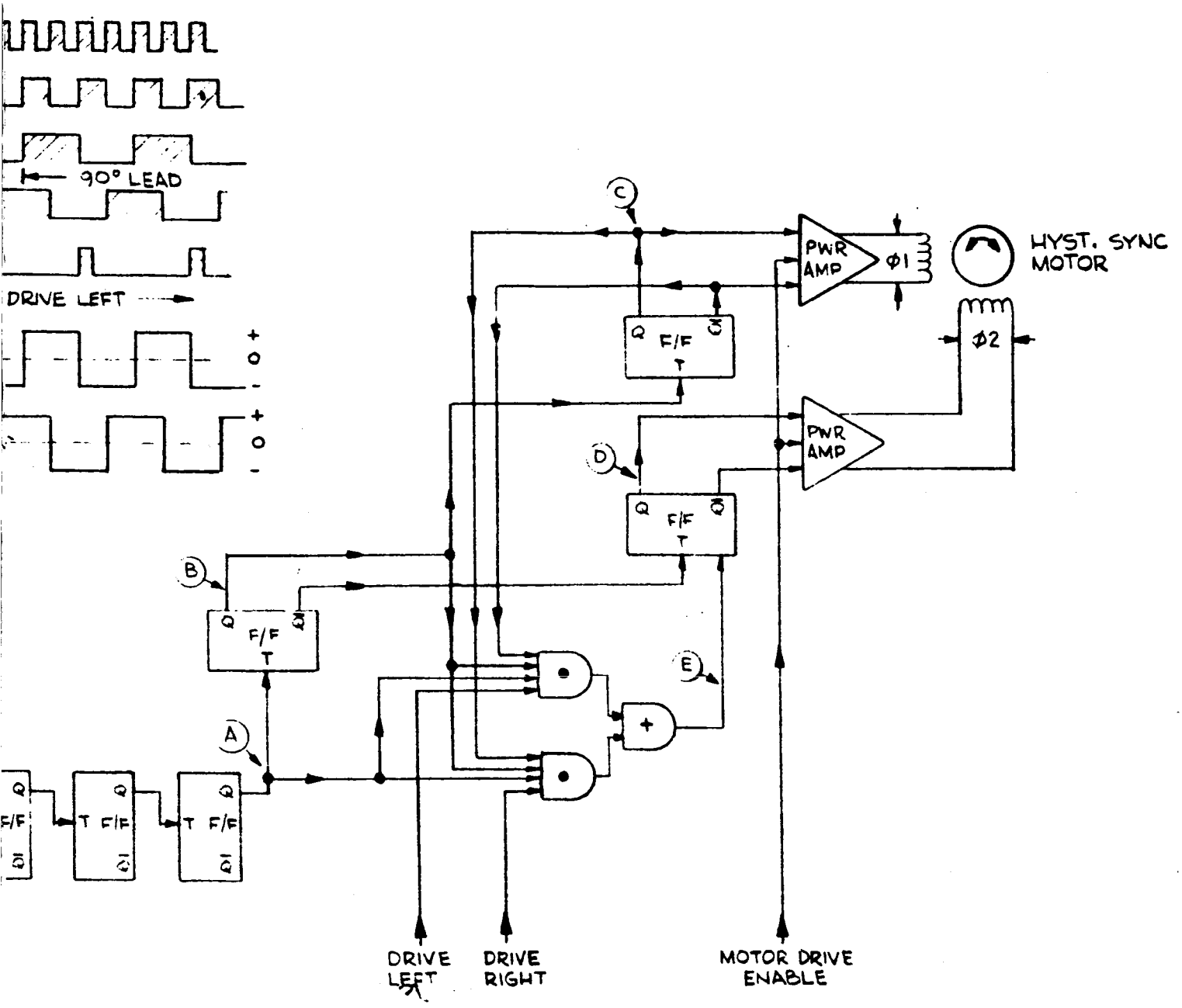

Figure 1-18 Motor Drive and Control: Apollo DVT/ATM

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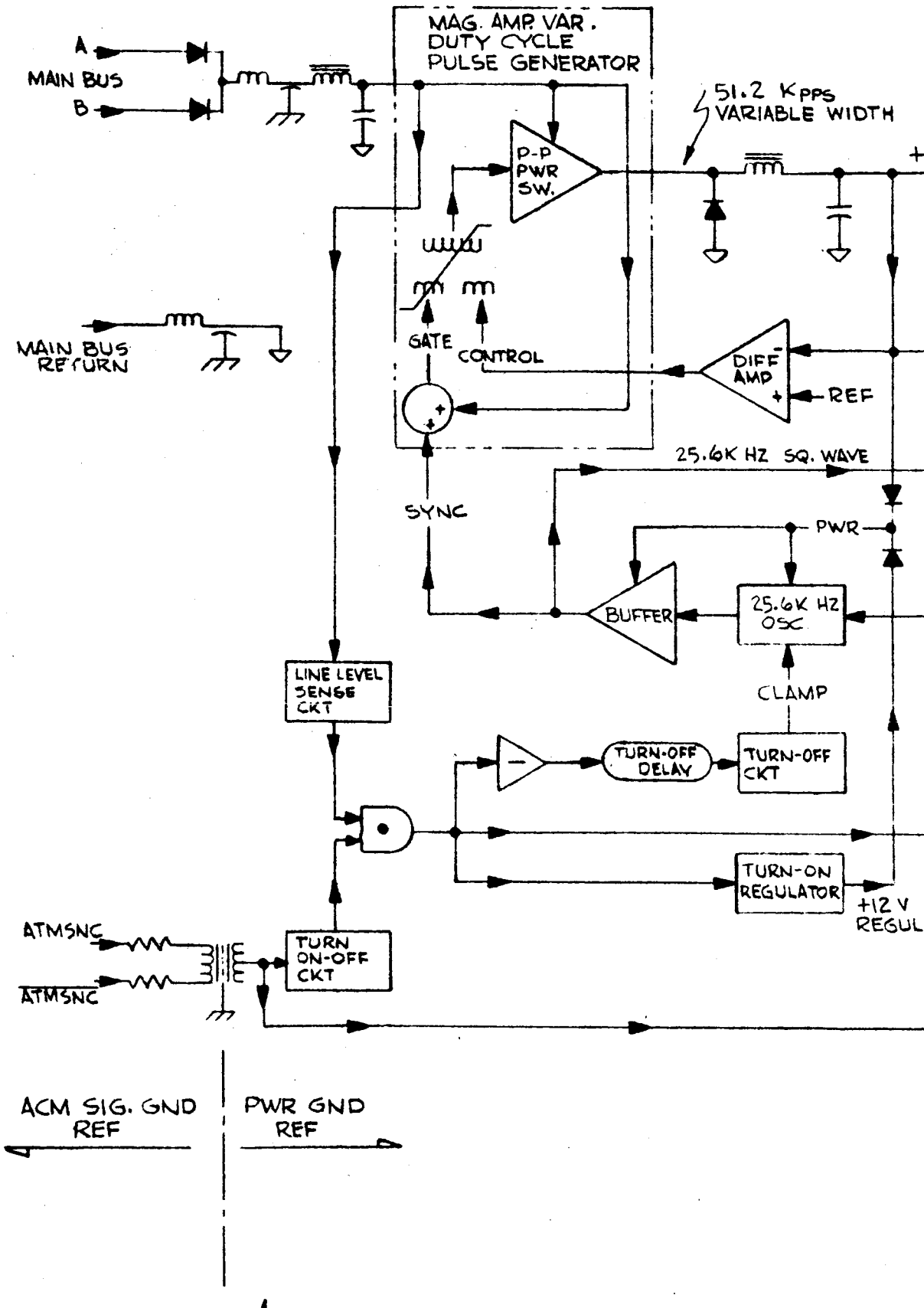

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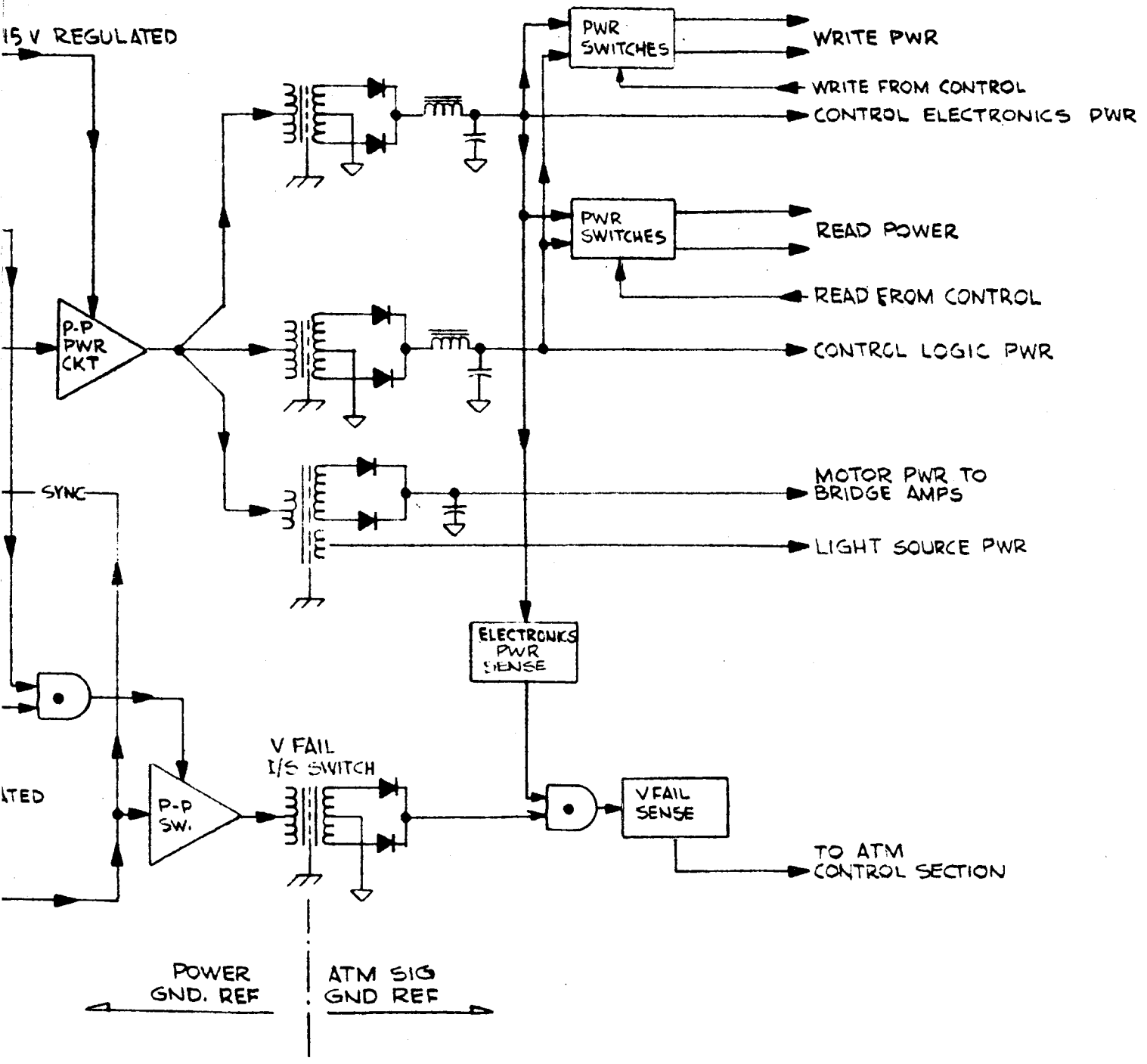

Figure 1-19 Power Supply: Apollo DVT/ATM

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logic elements. Power consumption in the power-down standby state is less than 25 milliwatts. Exclusive of the losses in the 28 VDC bus isolating diodes, the efficiency is as high as 80 percent depending on load conditions.

The power supply consists basically of a square wave power converter preceded by a constant efficiency regulator and various auxiliary circuits necessary for control and system interface.

The power inverter is a "master oscillator - power amplifier" circuit which drives three power transformers in parallel, with a 25.6 KHz, 15 volt RMS square wave. Separate transformers are used to improve isolation between logic, motor and electronics supplies. The voltage regulator, which furnishes 15 VDC to the power inverter, is a constant efficiency chopper type using magnetic amplifier pulse width control. This is a push-pull circuit which operates at twice the basic oscillator frequency or 51.2 KHz. A symmetrical multivibrator synchronized to the ACM clock supplies a timing reference and drive to both the regulator and power inverter, thus satisfying requirements of the predictable supply noise theory.

Auxiliary circuits function as turn-on and turn-off devices, and protect the system from low voltage conditions or power interruptions. A turn-on-off circuit senses the presence or absence of the ACM synchronizing signal and along with the line level sensor determines whether the power supply is energized or not. Because the regulator will not function unless driven by the master oscillator, a separate 12 VDC series regulator momentarily furnishes power to the oscillator until the 15 VDC regulated level is high enough to take over. It then reverts to an idle state with minimum power loss. Turn-off is accomplished by deliberately clamping the oscillator after a short time delay.

In addition to operating the turn-on circuit and synchronizing the master oscillator, the ATMSNC signal also operates the voltage failure I/S switch by chopping an ANDed result of the turn-on-line level sensor

and the 15 VDC regulator output. On the signal ground side of the I/S switch, the rectified resultant is further ANDed with the 12 VDC electronics supply and then applied to the VFAIL sense circuit. The VFAIL output is a dc level which indicates the condition of the power circuits to some extent, and the conditions of the main bus as seen by the ATM.

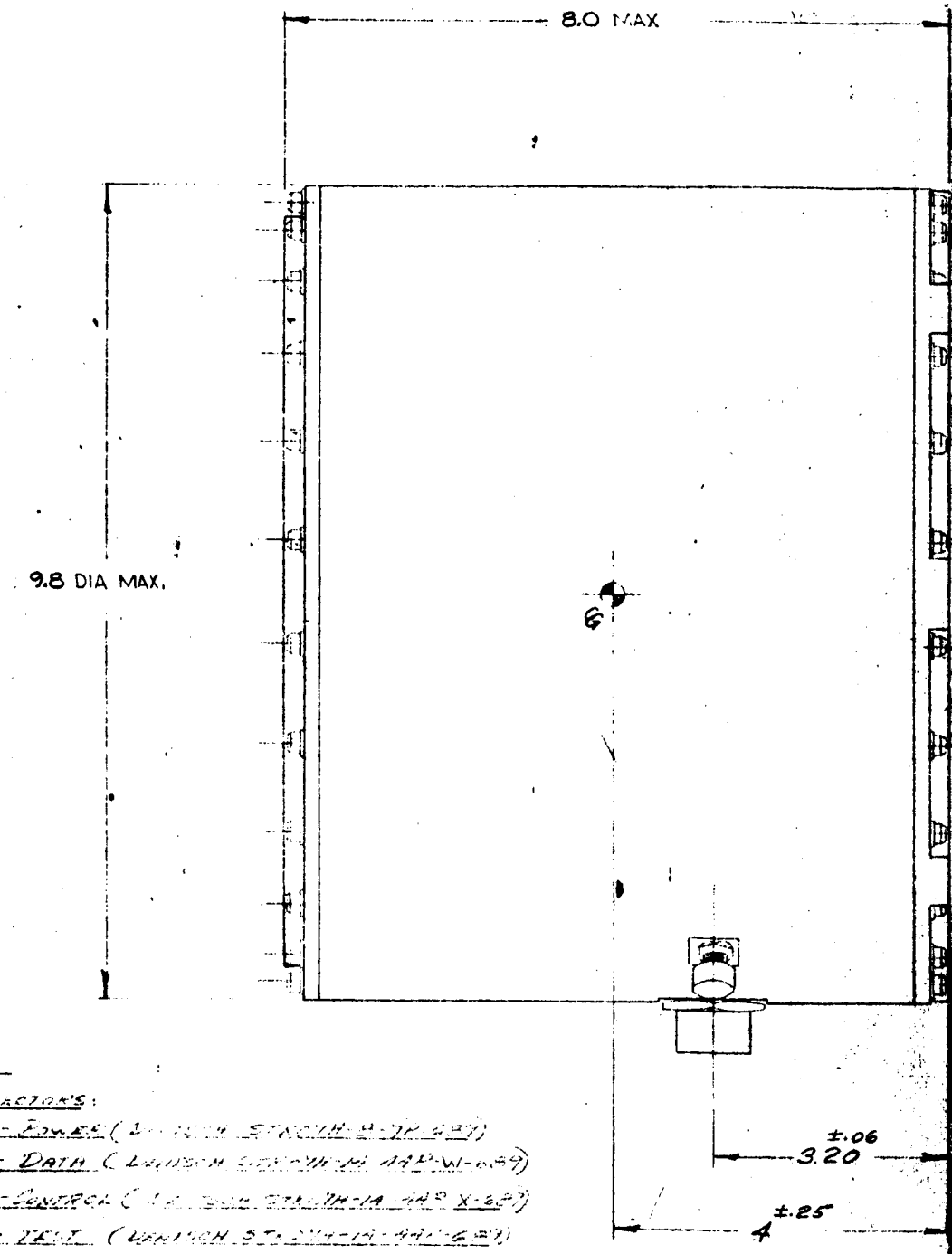
During a short power interruption, energy stored in the main bus L-C filter provides power to the supply. If the interruption is long enough to drain the storage bank to the minimum acceptable voltage level, then the line sensor will initiate a VFAIL sequence to warn the ACM of an impending shut down. A turn-off delay allows the supply to operate long enough after the VFAIL event to guarantee proper operation of the control electronics in the shut down process. Filters are inserted in the main bus and the main bus return to reduce conducted interference and susceptibility.

1.3.2 MECHANICAL DESCRIPTION

The complete assembly is of cylindrical form 9.8 inches in diameter 8.0 inches high, and with mounting provisions at 45° spacing on one end of the cylinder. (Figure 1-20.) The mounting surface must be attached to a coldplace for cooling. This approach gives maximum area of contact for heat transfer to or from the ultimate sink.

The electronic circuits are mounted in an area below the tape transport. All major electronic sections are contained in plug-in modules for ease of manufacturing, testing, and maintenance. Flight, test and power connectors are mounted on the side of the cylinder. Separate connectors are provided for power, signal, and test.

The transport and electronics are sealed and pressurized within separate compartments with provisions for pressure equalization incorporated in the design. Sealing and pressurizing the complete assembly assures reliable operation in a hard vacuum enviroment for at lea one year and provides protection from atmospheric contaminants. A nitrogen-helium-freon or nitrogen-helium atmosphere is used.



NOTE:

1. CONNECTORS:
   - J1- POWER (
   - J2- DATA (
   - J3- CONTROL (
   - J4- TEST (

2. C.G. POSITION SHOWN IS ESTIMATED.

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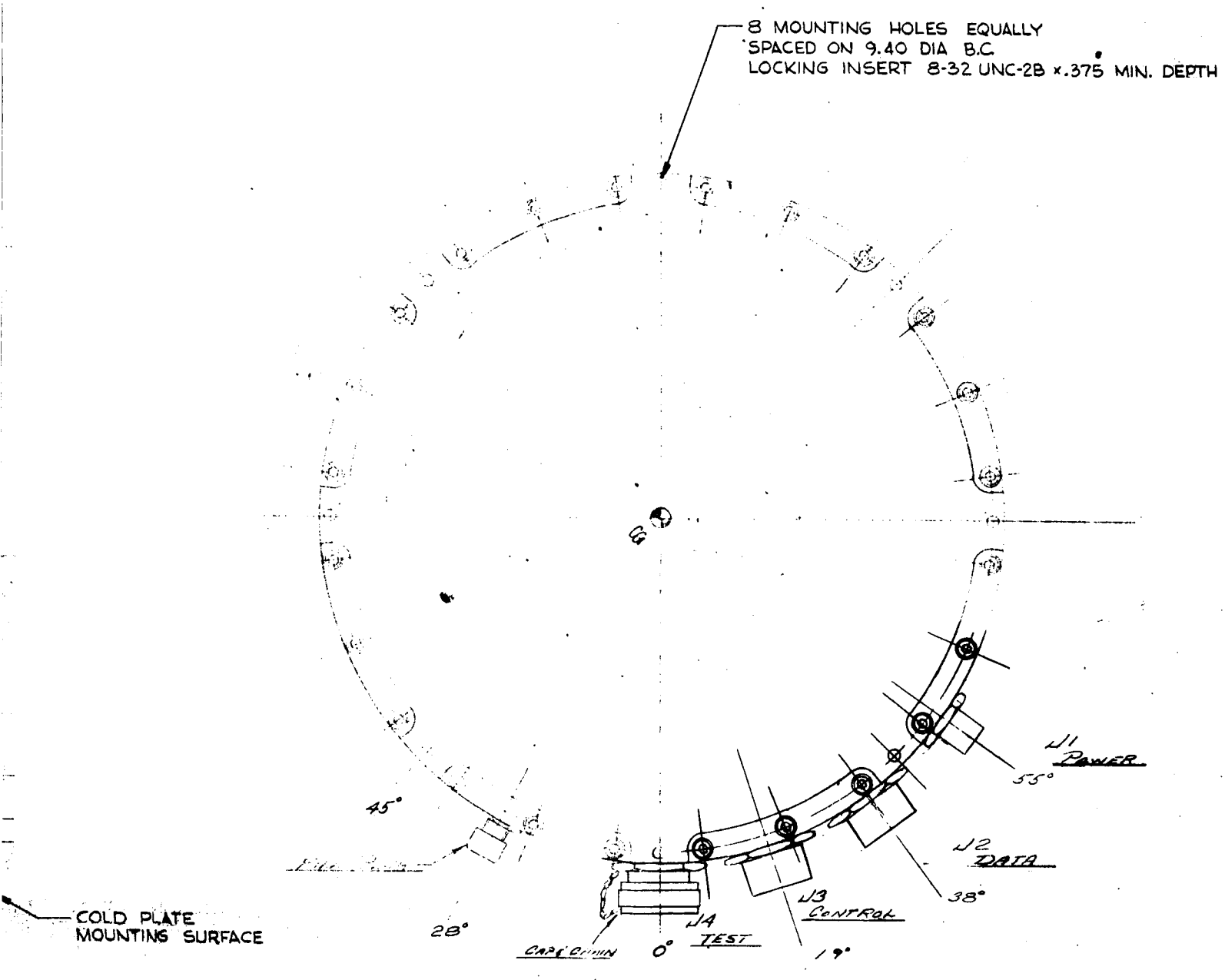

BOTTOM VIEW SHOWING COLD PLATE MOUNTING SURFACE

Figure 1-20 Outline and Installation: Apollo DVT/ATM

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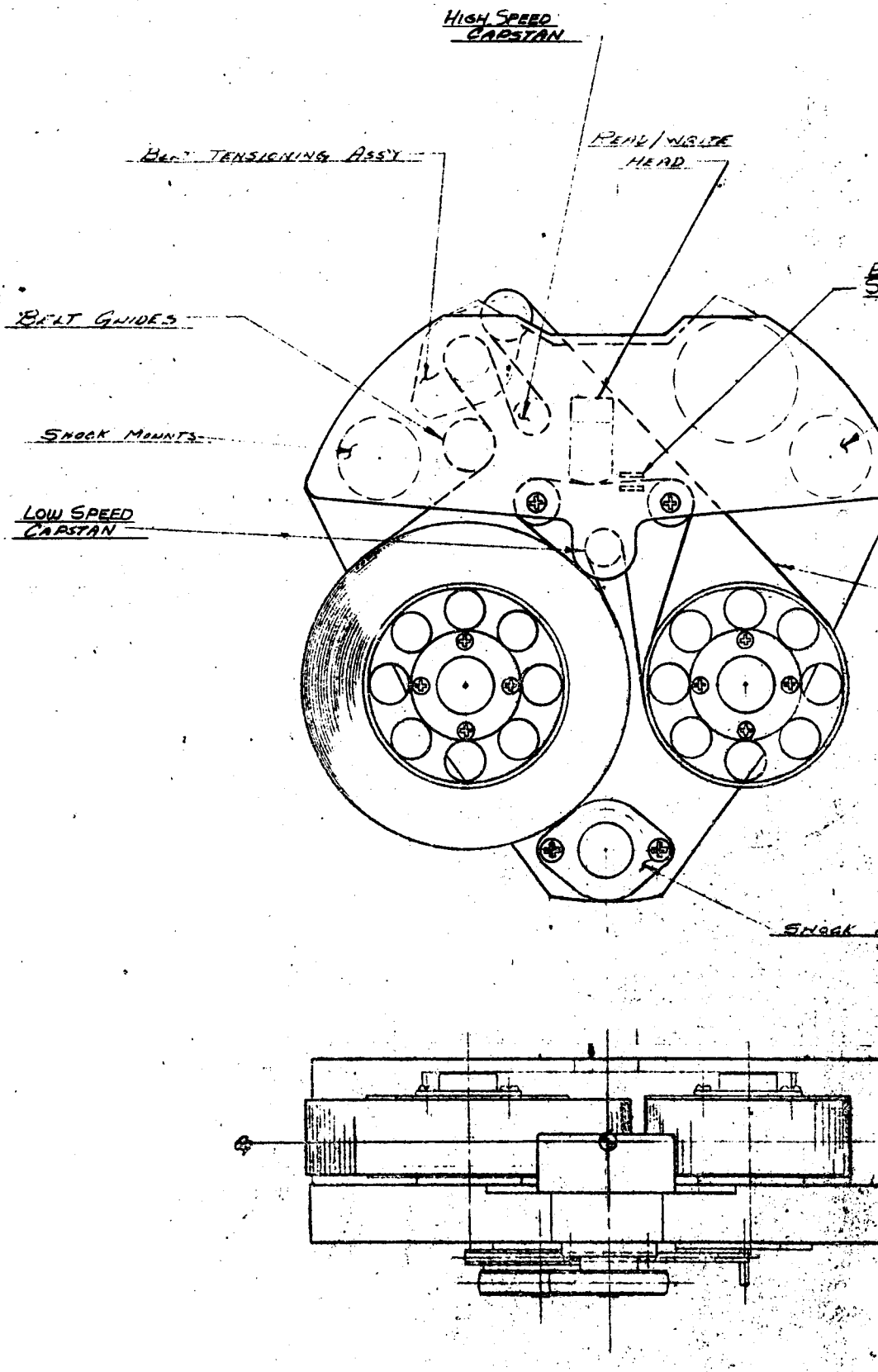
1.3.2.1 Tape Transport

As in the Gemini and Apollo ATM Systems, the transport consists of a peripheral drive system. It is powered by a single two-phase hysteresis synchronous motor having a shaft speed of 8000 RPM. A tape speed of 15 ips gives a time between tape ends approximately 440 seconds. Acceleration time is approximately 300 milliseconds from dead stop to synchronous speed.

Refer to Figure 1-21 depicting the basic transport layout. The drawing shows a single wide seamless Mylar belt which encircles the periphery of the two tape packs and is driven by a differential capstan system. The capstan, nearest to tensioning device, is driven at a slightly higher speed than the second capstan located in the peripheral drive belt path between the tape packs. The capstan speed differential causes an increased tension in the pressure belt on the take-up side of the system relative to the other half. The stretched section of the belt has a slightly reduced cross-sectional area and consequently travels at higher velocity. Thus the peripheral velocity of the belt is higher around the outer layer of the take-up side of the system than elsewhere. The fixed differential tension on the belt between the two tape packs creates tape tension across the head system as well as tape tension required to wind tape on the reels.

As the tape passes from one hub to the other, the length of the peripheral belt needed to encompass the tape packs changes slightly. A movable belt tensioning device compensates for this and applies the proper static operating tension in the peripheral belt.

Because the mechanical system is inherently symmetrical and the tape pack is under positive control of the peripheral belt at all times, extremely smooth tape handling results. This eliminates the need for an over-drive, take-up, and hold-back system and reel locking device to prevent tape spillage during non-operate transportation. Rapid start, stop, or reversal can be accomplished without danger of tape spillage or loss of tension across the read/write head.



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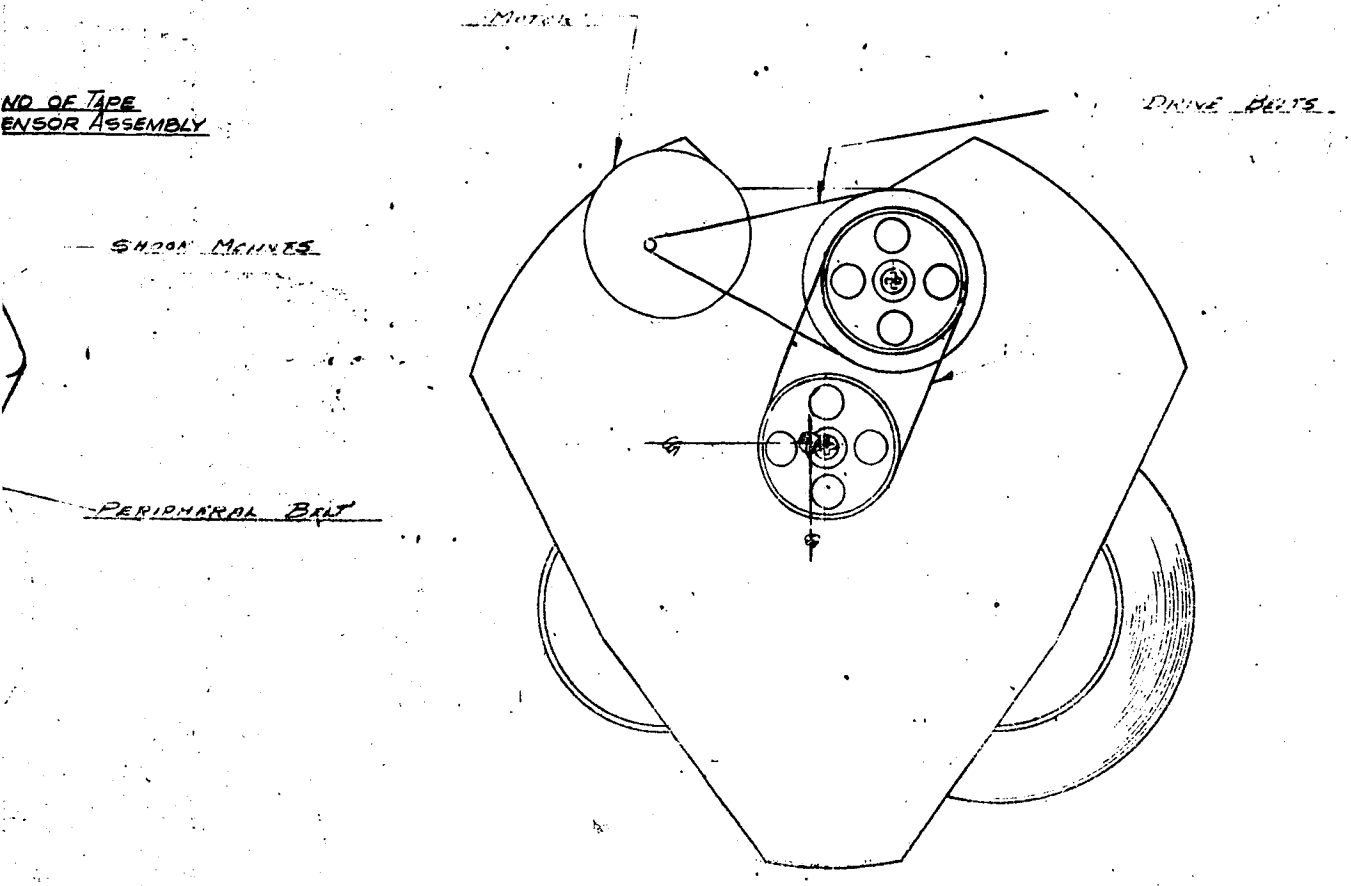


Figure 1-21 Transport Outline: Apollo DVT/ATM

An unusually high order of efficiency is obtained from this type of transport since there is virtually no wasted power in the differential tensioning system and there are relatively few rotating components in the drive train. There are no magnetic clutches, slip clutches, or torque motors.

The absence of reel flanges permits a reduction in the overall dimension normally required by a side-by-side, reel-to-reel configuration. Tape edge deformation caused by possible flange riding is eliminated.

Tape guiding is close to the head while the effective drive point is somewhat removed; thus tape motion across the head is less prone to skew effects than tape motion in transports where the principle tape drive point (capstan and pressure roller or pressure belt) occurs closer to the heads. Systems of the latter type are subject to lateral tape motion if all parts are not manufactured and maintained perfectly true and square. The side forces developed by such components can cause rapid tape guide wear, leading to excessive tape skew and rapid tape wear.

End-of-tape(EOT), Center-of-tape (COT), and beginning-of-tape (BOT) sensing is accomplished photo-electrically. Windows are formed in the magnetic tape. The tape passes between a light source assembly and photo-diode sensor assembly. The light source assembly consists of two gallium-arsenide light emitting diodes. Each diode is located at a level corresponding to the associated EOT, COT or BOT window in the tape. Two photo-diodes are arranged to sense the light from the light source assembly through the appropriate window.

1.3.2.2 Electronic Packaging

The electronics packaging approach selected for the engineering model ATM is basically a series of plug-in modules which mate with an interconnection plane. Module interconnections utilize a wire wrap plane. This plane is an 0.080 inch thick aluminum plate, with contacts inserted in nylon bushings on a 0.125 inch square grid. This design provides a high degree of flexibility and permits point to point

interconnection throughout the whole area of the plane. The contact termination is a 0.025 inch square tailpost for use with Gardner-Denver wire wrap connections. The reliability of this system has been proven in many military and flight programs.

The system electronic elements are housed in modules which plug into the plane assembly. The modules comprise almost the entire unit electronics with the exception of various miscellaneous items such as tape sensors, RFI filters, and main bus diodes.

The construction of all modules is similar with modifications as dictated by circuit or component requirements.

A T-section magnesium frame along the logitudinal axis forms the primary supporting structure of the module. Individual circuit cards are mounted back-to-back from the vertical web of this backbone. The upper horizontal face provides a mounting surface for test points if required. The vertical web provides shielding between circuits and also acts as a heat sink for higher power components. The outer face of the module also serves as shield attachment point where radiated energy problems occur.

The printed circuit cards are glass epoxy laminate, with two sided conductor layout. Interconnections through the board are made by plated through holes, or interfacial clinch. The card assembly terminates in a multi-pin right angle header which is mounted to the lower extremity of the vertical web. The upper section of the card is secured to the vertical web for additional vibration resistance.

Most electronic components such as integrated circuits, capacitors, diodes, etc., are mounted directly on the circuit cards. Bulky or high mass components such as transformers and chokes are mounted directly to the vertical web. The means of interconnection within the module is by flow or hand soldering process.

The completed module plugs into the interconnection plane and is secured by locating pins to the central web dividing the electronic and transport areas, and by captive screws to the auxiliary modules and main

flange of the unit case. This arrangement provides adequate support for the modules and acts to fasten the module backbone, interconnection plane, and dividing web into a highly resistant structure.

The read/write electronics is packaged in three modules: each module contains six complete read/write channels.

Each read/write channel is packaged as a submodule using a high density packaging technique developed for the Apollo ATM.

This method (illustrated on Figure 1-22), was used to eliminate stray capacitance and inductance caused by long component leads and excessive runs on printed wiring boards.

Interconnection of components in the submodule uses a combination of welding and soldering techniques.

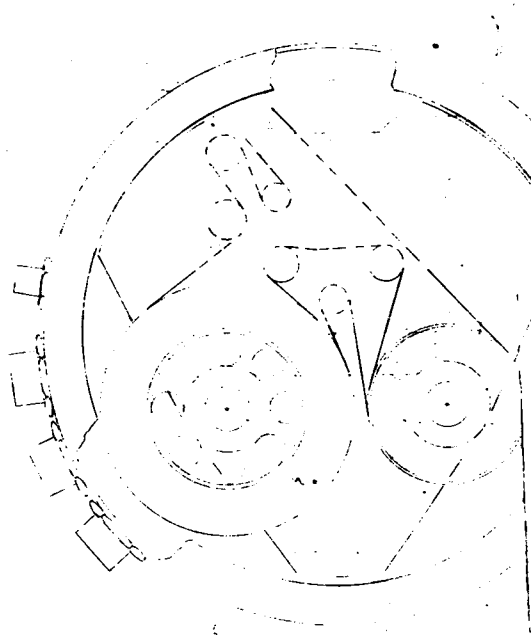
Flat packs are welded to pins embedded in a glass/epoxy carrier board. By means of a wire matrix, the pins and posts are interconnected. Heavy bus conductors are used to distribute ground and the various voltages to the wire matrix.

Electrically common discrete leads are soldered to a single post where possible, to eliminate excessive matrix wire. A printed wiring mother board is used for interconnecting the submodule and module headers.

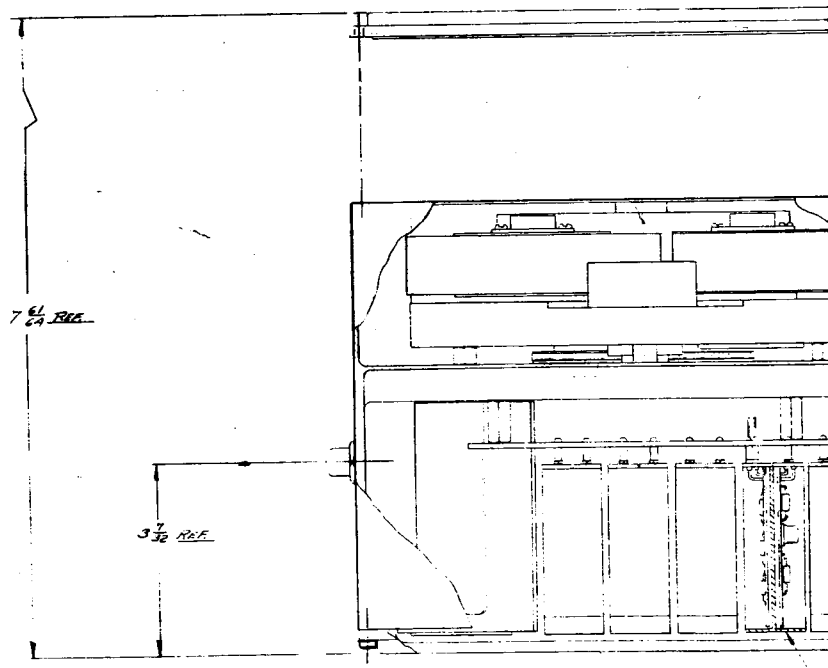
To provide heat sinking, flat packs in the submodule are adhered to a heat sink which is attached to the module frame. The frame is then secured to the walls of the case conducting heat directly to the unit mounting surface.

1.4 CONTROL PANEL

A portable control panel (see figure 1-23) is used with the Engineering Model Auxiliary Memory. The panel contains displays of ATM position and motion, ACM counter activity, alarm and status signals to the AGC via CONOUT and CONIN, and AGC interface line drivers. In addition, two comparators may be used to detect combinations of signal states during



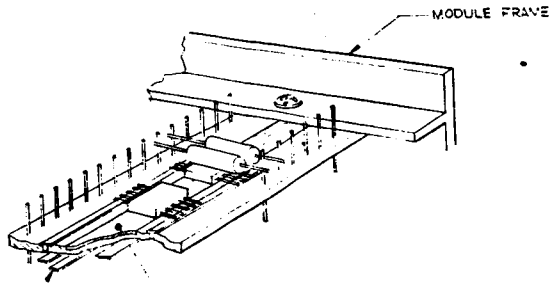
TOP VIEW
X PORT SIDE
SHOWN WITHOUT TOP COVER



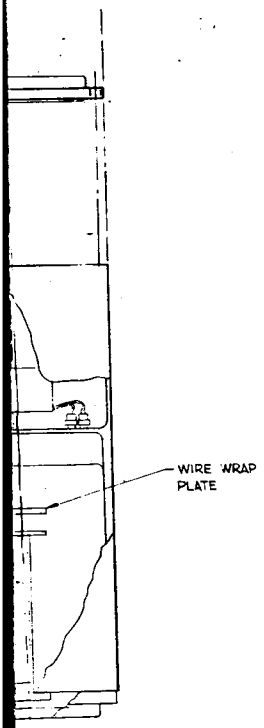
A

DIRECTION

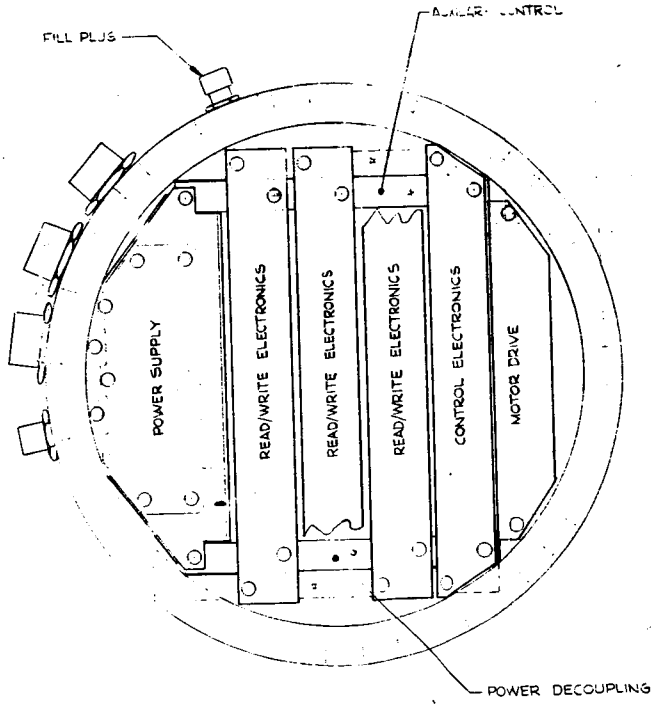
FOLDOUT FRAME 1



READ/WRITE CHANNEL



TYPICAL MODULE CONSTRUCTION



VIEW IN DIRECTION A SHOWN Figure 1-22a MODULE SIDE

ATM Internal Configuration

FOLDOUT FRAME 2

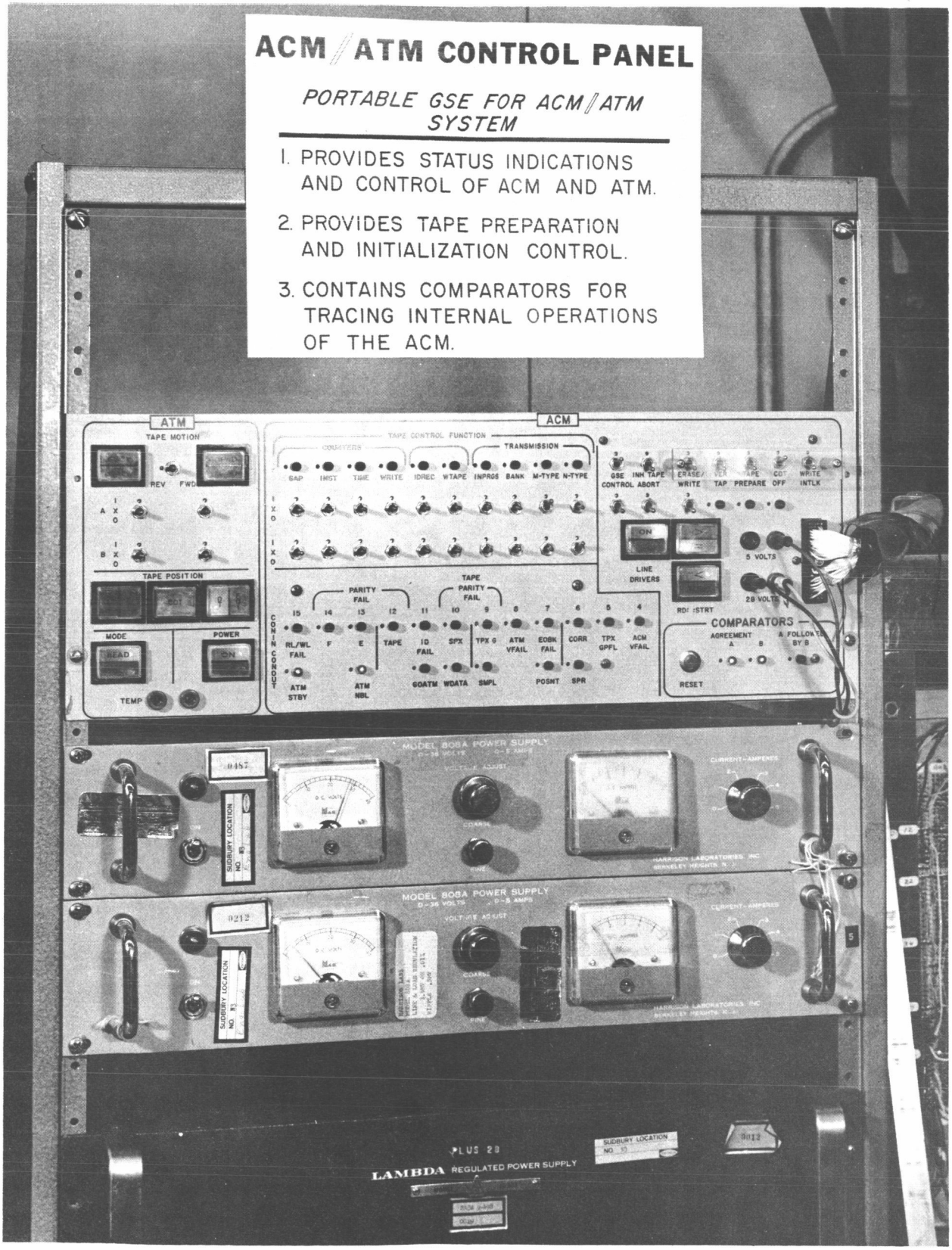


Figure 1-23 Control Panel

tape operations for analysis. Controls also provide a variety of operations related to tape initialization and loading.

1.4.1 ELECTRICAL DESCRIPTION

Power Supply

The control panel is designed to operate from an external DC supply which provides +5vdc and +28vdc via jacks on the front panel.

Displays

The panel contains two types of displays: large, rectangular indicators for signals frequently observed, and small indicators for signals occasionally referred to. These indicators are connected to lamp drivers, preceded by inverters where necessary for correct visual interpretation of a logic signal.

Comparators

Many of the signals displayed on the panel can be selected as input signals to either of the two comparator circuits. Toggle switches are provided adjacent to these indicators so that either the "one" or "zero" state of the signals may be chosen. When all of the A-selected conditions have been fulfilled, the A agreement indicator is illuminated. Similarly, the B agreement indicator independently shows that all of the B-selected conditions have been met. In addition, if the B agreement occurs within 50 msec of the A agreement, the A followed by B indicator is illuminated. All three indicators may be cleared by depressing a reset button.

Logic signals from the ACM comparator which relates c(IDREAD) and c(IDSTRT) are used to drive displays READ: STRT. The "<", "=", and ">" conditions are synthesized.

Other controls are provided for moving the tape, and enabling or inhibiting certain ACM/ATM functions.

1.4.2 MECHANICAL DESCRIPTION

The control panel includes a number of indicators and switches, attached to a standard 19-inch rack panel. The panel is mounted in a transportable case, and may be removed for installation in a rack.

Jacks are provided on the panel for DC power inputs; a connector located on the panel provides for attaching a test cable from the ACM. Test points are included for monitoring ATM temperature.

The logic circuits which mechanize the A and B comparators, the Read-Start comparator, and transistor switches for the large indicators are all mounted on an Augat board behind one end of the panel.

A protective barrier is located above the controls in the upper right corner of the panel which require protection from accidental operation.

1.4.3 CONTROLS AND INDICATORS

1.4.3.1 ATM Section Tape Motion Indicators

GOREV: displays that ATM has been commanded to move tape in the reverse direction.

TMREV: indicates ATM is moving tape in reverse in response to command GOREV. Is illuminated approx. 1 second after GOREV, but both are extinguished simultaneously.

GOFWD: displays that ATM has been commanded to move tape in the forward direction.

TMFWD: indicates ATM is moving tape forward in response to command GOFWD. Is illuminated approx. 1 second after GOFWD, but both are extinguished simultaneously.

Tape Motion Controls

FWD/REV: 3-position Toggle switch provides manual control of tape motion by switching commands GOFWD or GOREV. Neutral position is off (neither command issued). Switch operative only when ACM not commanding ATM (GOATM = 0).

Comparator Switches

"A" and "B" comparator inputs are provided for ATM feedback signals TMREV and TMFWD.

Tape Position Indicators

BOT: illuminated when the ATM tape is positioned in the beginning of tape window.

COT: illuminated when the ATM tape is positioned in the center of tape window.

EOT: illuminated when the ATM tape is positioned in the end of tape window.

PT: illuminated when the ATM tape is positioned between (but not in) the BOT and COT windows.

DT: illuminated when the ATM tape is positioned between (but not in) the COT and EOT windows.

Tape Mode Indicators

READ: illuminated when the ACM is requested to read the ATM tape (register CONOUT bit 10 = 0), the normal condition.

WRITE: illuminated only during the actual tape write sequence, and not during the preceding search sequence. This is not a display of the request posted in CONOUT by the AGC, but an indication that writing is presently in progress.

Tape Power Indicators

ON: iluminated when the ATM is in the power state (ATMON = 1).

FAIL: illuminated when an ATMVFL voltage failure has occurred, irrespective of tape motion.

Terminals are provided to monitor TEMP, a temperature sensor located within the ATM case.

1.4.3.2 ACM Section

Tape Control Function (Counters)

GAP Counter: illuminated when the tape is in motion and allows the ACM to count word times during a gap between ATM records.

INST Counter: Illuminated when the Instant Counter is enabled during the read sequence after a gap of 4.

TIME Counter: illuminated when the Time Counter is enabled to measure 1.2 sec. intervals at every tape reversal, and for the erase interval after a record is written.

WRITE Counter: illuminated when the Write Counter is enabled during the write sequence to measure intervals after the end of the record for which c(IDREAD) = c(IDSTRT). At a write count of 16, the head power is switched on, and the data is recorded commencing with a count of 64. This counter also times the strobing of data on to the tape.

Tape Control Function (Transmission)

INPRGS: displays signal TRNSIP (Transfer in Progress) when the record specified by IDSTRT is located until the requested tape operation is completed.

BANK: displays signal TRNSBNK up during the interval when data transfers between the ACM stack and the tape (in either direction) are taking place. For multibank operations, this signal is reset between each bank.

M-TYPE: displays signal NBLIDTRSM, which controls the recording of triplex ID words at the front of each record (leading IDs).

N-TYPE: displays signal NBLIDTRSN, which controls the recording of triplex ID words at the end of each record (trailing IDs)

Tape Control Function (Misc.)

IDREC: displays signal NBLIDREC which decodes the next word received as a triplex word, assumed to be an ID word.

WTAPE: repeats the ATM WRITE MODE indication in this region of the Control Panel.

Each of the Tape Control Function indicators described above is provided with toggle switch selection of inputs to both comparator A and B circuits in the Control Panel.

Tape Control Function CONIN and CONOUT

CONIN Indicators: provided for displaying 12 bits (CONIN 15 through CONIN 04) of this register, which are the ACM status and alarm inputs to the AGC.

RL/WL FAIL: Illuminated when a failure has been detected during the Read Line/Write Line Test. This should also cause ACM self-amputation and the Line Driver indicators should change from ON to OFF.

F PARITY FAIL, E PARITY FAIL, and TAPE PARITY FAIL: One of these three indicators is illuminated when a parity error is detected during an ACM Memory Cycle. The particular indication depends on the use to be made of the data; to AGC as fixed memory data, to AGC as erasable memory data, or to the ATM tape.

ID FAIL: indicates that the ACM has been unable to find the specified record on the tape, and that three reversals of tape motion have been performed between ID's greater than and less than the one specified.

SPX TAPE PARITY FAIL, and TPX G TAPE PARITY FAIL: These two indicators display parity errors detected while actually reading a record from the ATM tape, and do not relate to the ACM memory. One indicator displays errors located in simplex records, the other displays uncorrectable parity group errors for triplex records. In either case, the transfer is discontinued.

ATM VFAIL: Indicates that an ATM Voltage Failure has occurred while the tape has been commanded to move (including search sequences).

EOBK FAIL: Indicates that register TADDR does not contain zero when a gap is detected; the record being read from tape is either too short or too long.

CORR: Indicates that at least one (one or more) correction was attempted while reading a triplex tape record. The correction may have been a success or a failure; the TPX G Tape Parity Fail indicator must be examined.

TPX GPFL: This indicator also displays the same errors as COIN 09 (TPX G TAPE PARITY FAIL). In addition, this display includes errors (or glitches) detected in ID words during a tape search sequence.

ACM VAIL: Indicates that an ACM voltage failure has occurred since the AGC input register CONIN was last examined.

CONOUT: Indicators are provided for displaying 6 bits (and one spare) of this register, which are the AGC command inputs to the ACM.

ATM STBY: Indicates that the ATM has been requested to assume a standby condition.

ATM NBL: Indicates that the ATM power has been commanded on by the AGC (must be accompanied by ATM STBY).

GOATM: Indicates that a tape operation has been commanded by the AGC (tape moves initially in reverse except when at BOT).

WDATA: Indicates that the AGC has requested a record to be written on the tape. Absence of this indication when GOATM is illuminated implies a read (or position) request.

SMPL: Indicates that a simplex tape write operation has been requested by the AGC. Absence of this indication during a tape write operation implies that the record(s) are being written in the triplex mode.

POSNT: Indicates that a position tape operation has been requested by the AGC.

SPR: Spare indicator

Other ACM Controls and Indicators

LINE DRIVERS ON and OFF: These two indicators display the status of power applied to the interface between the ACM and the AGC.

RD::STRT: These three indicators display the outputs of the Read-Start comparator within the ACM. Logic internal to the control panel detects and stores the equal condition. An illuminated reset button is provided to erase the storage logic.

COMPARATORS: Two indicators are provided, one for each of the two Control Panel comparators (A and B). An additional indicator is provided for the sequential detection of both comparator outputs (A FOLLOWED BY B). A reset button clears both comparators.

CONNECTORS: Panel jacks are provided on the face of the Control Panel for 5-volt and 28-volt power inputs, so that the Panel may be operated in its protective case. A connector, also located on the face adjacent to the power jacks, is provided for attachment of the cable from the ACM.

GSE CONTROL: Allows all of the ACM Core Stack to be addressed using erasable addresses. Normally only MU5 and half of MU4 can be so addressed.

INH TAPE ABORT: Forces tape operation to proceed to completion in the presence of conditions which normally terminate the transfer.

PROTECTED CONTROLS: The following five controls are mounted beneath a shield bar which protects them from inadvertent operation.

ERASE/WRITE: Provides manual control of ATM write head power independent of the ACM control logic.

VER TAP: Provides manual control of ATM read amplifier sensitivity for test purposes.

TAPE PREPARE: Enables the ATM tape to be initialized (per Appendix C) by establishing a Tape Write mode, by disabling the ACM control logic, and by supplying the necessary time signals.

COT OFF: Disables the PT/DT relay within the ATM from throwing as the tape moves across the COT window. Permits tape to be moved to PT side while relay remains in DT position.

WRITE INTLK: When used, this switch prevents writing onto any part of the ATM tape by any source (AGC or GSE). Provided to simulate a possible flight requirement.

SECTION 2
SYSTEM ORGANIZATION

2.1 FUNCTIONAL SYSTEM DESCRIPTION

In the implementation of the AM Engineering System the following units, shown in the block diagram (Figure 2-1) can be identified.

a. A core memory subsystem consisting of up to four core stacks, (memory units), each having individual selection circuits, inhibit drivers and sense amplifiers. Two such memory units are provided in the Engineering System.

b. Two buffer registers, the GAM to service the AGC and the ATM to service the tape. The memory subsystem is time-shared between the two, so that the AGC and ATM are serviced independently.

c. Two prime address registers, one which mimics the AGC's address register (SAM) and one which keeps track of the tape address (TADDR) for tape/core stack transactions.

d. A core-address selector which selects either the AGC address (from SAM and the E and FBKAM registers) or the tape address (from TADDR) at different well-defined times and executes the appropriate memory cycle (for the AGC or the tape) if required. The requirements for an AGC-type memory cycle and a tape-type memory cycle are different and are discussed in Paragraph 2.3.2.

e. Duplicates and extensions of the AGC's EBANK, and FBANK, the contents of which are part of the AGC address. These bits are decoded along with the C(SAM) at the appropriate time during AGC cycles such that if the address so referred to is an ACM address, the ACM will execute a memory cycle and provide/accept data to/from the AGC.

f. Control, Alarm and Status registers which are addressable by the AGC as unused channel registers. These registers normally

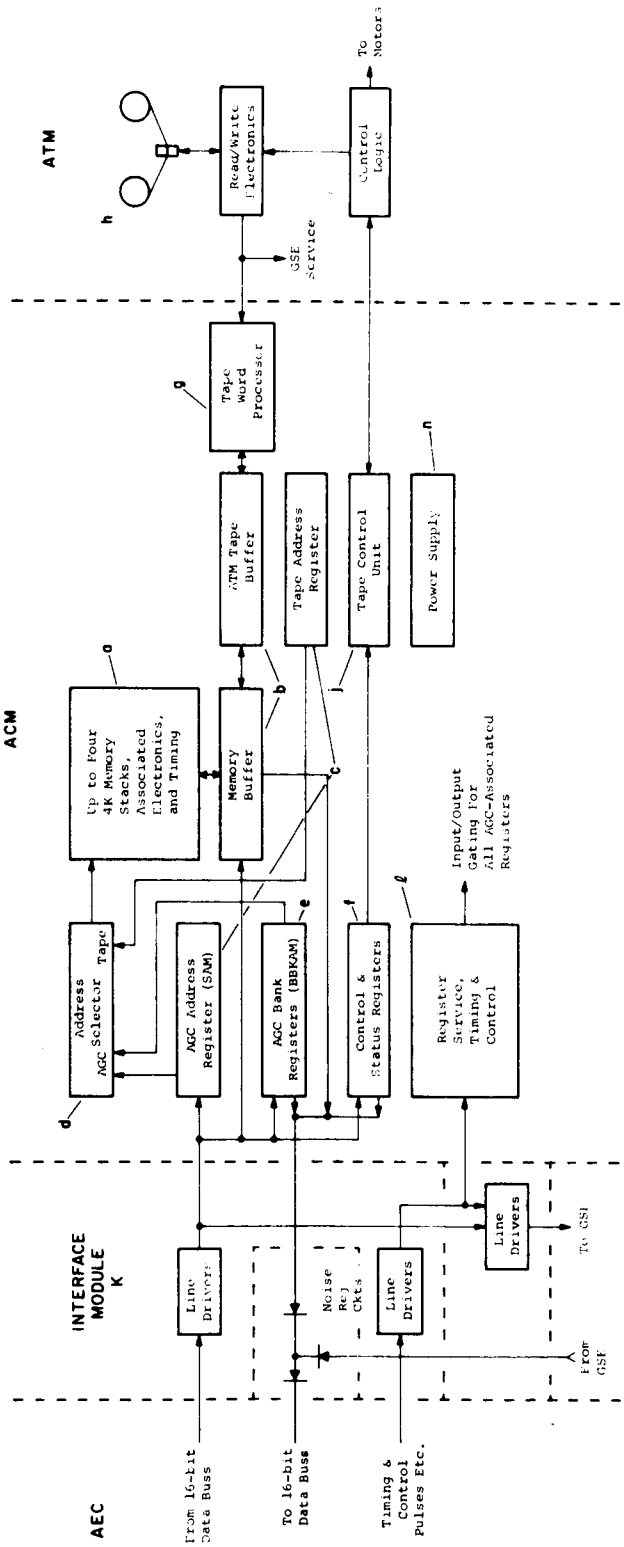


Figure 2-1 Functional Block Diagram

provide for AGC control of tape operations, but also allow the AGC to monitor the status and alarm conditions in the ACM.

g. A tape word processor which includes the ATM-ACM data transmitters, receivers, voters, group and word parity generators and checkers.

h. An integral ATM which responds to commands from the ACM and either reads or writes on the ATM magnetic tape.

i. A tape control unit which, depending on the operation specified in the control registers, will sequence the ATM power turn-on, locate the correct record (or space) and supervise the reading (or writing) from tape.

j. An Interface Module which buffers AGC signals and processes them for delivery to the ACM. For ACM signals sent to the AGC, noise rejection circuits are provided to enhance the noise immunity.

k. A register service unit which dictates the gating and clearing of registers (including channels), and supervises information transfer between internal registers as well as transfers to the AGC.

l. A power supply which converts nominal 28 volt spacecraft power into the voltages required for logic and memory circuits.

2.1.1 DETAILED DESCRIPTION OF SYSTEM ORGANIZATION

The attempt is made here to define the system organization from a physical point of view. The various registers, comparators, data busses, etc. that are necessary to implement the required functions are listed below. Figure 2-2 shows how the system is organized.

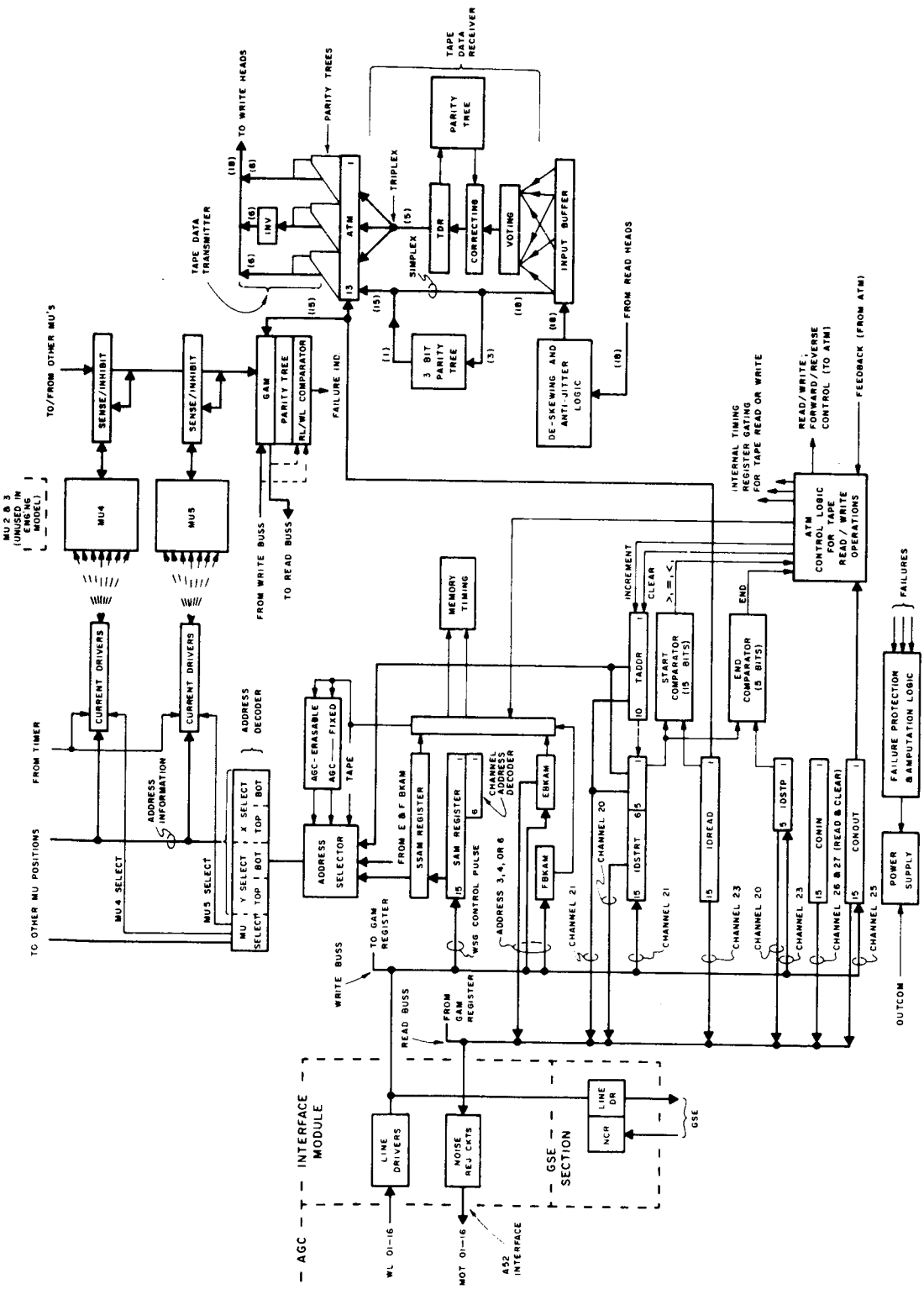


Figure 2-2 Detailed System Organization

REGISTER NAME	COMMENTS
GAM	Bidirectional memory buffer register. Services memory from AGC and ATM.
SAM	AGC address register. Maintains a copy of the AGC's address register (S). Word transfer into SAM occurs every WSG control pulse (i.e., every computer time T08 and sometimes at T01).
SSAM	Address register. Copies SAM every T01; SSAM always contains the "real" AGC address. Modifications to the address (in S and SAM) at T01 which occur as a result of quarter code instructions and INKL's are copied into SSAM and retained there for 12 μs, permitting ACM cycles to be completed with the correct address.
EBAM and FBAM	E and F bank registers. Contain copies and extensions of the AGC's E and F bank registers. Word transfer into E and FBAM occurs when the AGC address is 3, 4, or 6 (except, of course, TC3, 4, or 6). Word transfer to the AGC from EBAM is allowed when E bank or both bank is read as address 3 or 6, respectively.
IDSTRT	Register required for tape operations. When loaded by the AGC as channel 21 it contains the identification number of a record to be located on the tape. The AGC can read IDSTART as Channel 21 (bits 1-5 in locations 11-15, respectively) and as Channel 20 (bits 6-15 in locations 6-15, respectively).
IDREAD	Register contains the most recent ID found on the tape during the last tape operation. The AGC can read (as Channel 23) but cannot write into this register.

REGISTER	COMMENTS
IDSTP	Short (5 bit) register loaded by the AGC as Channel 23. Used during "multibank transfers" where more than one record is read or written on the tape. IDSTP may be read by the AGC as Channel 20.
CONIN	Alarm and status register. A read-only register whose bits are set by the results of various tests (parity, etc.). The AGC can read this register by addressing Channel 26, and can read-and-clear by addressing Channel 27.
CONOUT	Control register used by the AGC to initiate tape operations and control the ATM. The AGC has read/write access to this register by addressing Channel 25.
TADDR	Tape-address register. In the tape write mode, TADDR contains the address of the next word to be read from the ACM memory and stored on the tape. In the tape read mode, TADDR contains the address of the ACM location to which the last word from the tape refers. TADDR is cleared and incremented by the control logic; its contents can be read by the AGC as part of channel 21.
INPUT BUFFER	Eighteen-bit tape input buffer stores ATM data from the read heads and services the voters in the Tape Data Receiver. Word transfer into INBUF is under the control of the deskewing logic.
TDR	Six-bit output buffer which assembles in the ATM register, 1/3 of any AGC word for every triple Tape Word. Word transfers are exclusively under the control of the ACM Sequence Generator.

COMPARATORS	COMMENTS
START COMPARATOR	Compares c(IDREAD) with c(IDSTRT). Output is >, = ,< signal to the ATM control logic.
STOP COMPARATOR	Compares last 5 bits of IDSTRT with C(IDSTP). Output is an END signal to the ATM control logic.
RL/WL COMPARATOR	Compares data transmitted on read lines with data fed back on write lines. Output is a failure indication if one or more bits do not agree.

MISCELLANEOUS	COMMENTS
FAILURE PROTECTION AND AMPUTATION LOGIC	Contains all necessary circuits to monitor the ACM's influence on the AGC, and in the event of serious failures, will amputate the ACM from the AGC.
POWER SUPPLY	In addition to furnishing power to the ACM memory circuits and logic, the power supply contains special turn-on turn-off circuits that depower the memory gracefully and thus turn-off the ACM without introducing transients on the AGC's input lines.
INTERFACE MODULE WITH GSE SECTION	Contains noise rejection circuits for signals entering the AGC and Line Drivers for signals leaving the AGC. Also provides GSE breakout for all test connector signals.

2.2 GENERAL INFORMATION

2.2.1 INPUT-OUTPUT MECHANISM

The AGC interfaces with the ACM by means of the AGC test connector, A52. At this interface there exists enough information in the form of data buss signals, control pulses, etc., to unambiguously define the registers referred to in Section 2.1.1.

The registers in the ACM which receive information from the AGC are SAM, GAM, EBKAM, FBKAM, IDSTRT, IDSTP and CONOUT. The registers whose contents are transmitted to the AGC are the same as those above (with the exception of SAM) plus CONIN and TADDR.

The SAM register is written into at the occurrence of control pulse WSG; therefore SAM mimicks the S register in the AGC. Since the ACM SAM register contains address information, it is decoded in order to determine if the location currently being referenced is the E bank register, the F bank register, or both. (i.e., the octal value of S is 3, 4 or 6). If the location referenced is in fact one of these, the decoded address coincident with control pulse (WEBK, WFBK, or WBBK) will cause data on the write buss to enter the appropriate register (EBKAM, FBKAM, or both). The AGC simultaneously copies the contents of its own write buss into the AGC register (E bank, F bank or both). Therefore, the ACM contains a copy of the AGC's bank registers. The EBKAM register in the ACM contains additional bits (for which there is no AGC counterpart) to enable the ACM to be addressed as "switched erasable" memory. The details of the addressing scheme are discussed in Section 2.3.1.

Other registers which can be written into by the AGC are primarily intended for tape control. These registers are designated by channel addresses and are an extension of the normal AGC input-output. The address in SAM is decoded to detect these addresses and the control pulse WCH (Write CHannel) gates the data on the write buss into the appropriate channel in the ACM.

The channel assignments for the ACM are given in Table 2-1. Note that only three registers can be written into and six can be read.

Information transfer to AGC from the ACM is somewhat more restricted. Information in SAM, for example, is never transmitted to the AGC.

The transfer of information between GAM and the AGC is always the result of addressing the ACM as an extension of fixed or erasable memory. The circumstances surrounding this data transfer are explained in Section 2.3.

TABLE 2-1

ACM CHANNEL ADDRESSES

REGISTER NAME	CHANNEL ADDRESS	
	WRITE	READ
IDSTART	21	20, 21 (1)
IDSTOP	23	20, (1)
CONOUT	25	25
CONIN (Read Only)	-	26
CONIN (Read and Clear)	-	27
IDREAD	-	23
TADDR	-	21 (1)

NOTE: (1) Reading Channel 20 or 21 results in bit shifting. See Figure 2-3.

Of the two bank registers, EBKAM alone is capable of transmitting information to the AGC. (FBKAM is a five bit copy of the AGC's Fixed Bank register, so there is never a requirement to read this register.) The reading mechanism is identical to the write discussed previously, except control pulse REBK (Read Erasable Bank), coincident with the appropriate address (from SAM), causes data to be loaded on to the Read buss and from there through the interface module and onto the computer data buss.

The channels which can be read are IDSTRT, IDREAD, IDSTP, CONIN, TADDR, CONOUT and FEXT. Despite the bit manipulations which occur during reading, the basic AGC access to any of these channels is similar to the write operation discussed previously: i.e., the appropriate address, coincident with control pulse RCH (Read CHannel) causes information to be outputted through the read buss in the ACM to the AGC's data buss.

The ON-OFF information for the ACM is supplied by means of a direct wire (OUTCOM) from an AGC channel. This AGC output drives a circuit in the ACM power supply which causes the magnetic amplifiers and switching regulators to turn on providing the necessary voltages (+4.4V logic power and +14V, +12V, and -5V memory power).

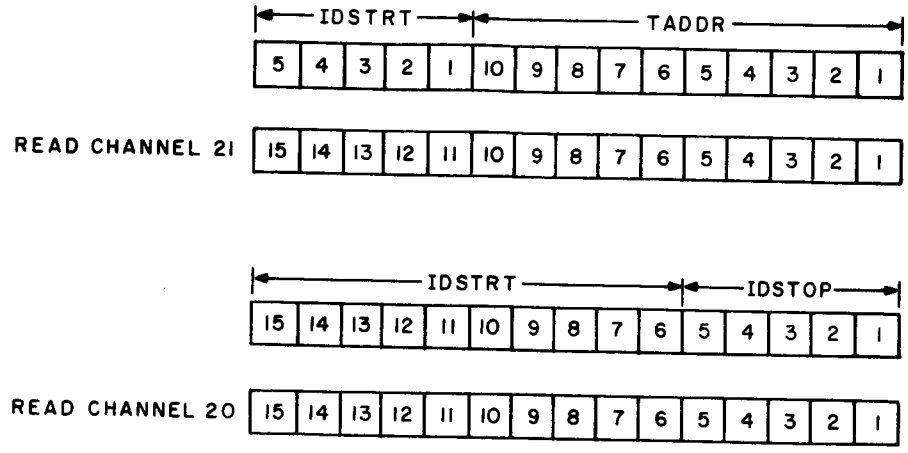


Figure 2-3 Bit Assignments When Reading Channels 20 and 21

2.2.2 MEMORY SUBSYSTEM

The Engineering System of the ACM contains two 4096 word memory stacks and supporting electronics, with space and wiring provided for an additional pair of identical stacks. Each stack with its electronics is referred to as a Memory Unit. These memory units are enumerated MU2 through MU5, where MU4 and MU5 are the memory units included in the Engineering System.

The supporting electronics included in each Memory Unit consists of sixteen sense amplifiers and inhibit drivers, sixteen x selection switches and sixteen y selection switches. The sense amplifiers are contained in a single module (see Figure 2-4 - picture of sense amplifier) and the remaining circuits are in two identical modules, each containing sixteen selection switches (eight top-select and eight bottom select) and eight inhibit drivers. (See Figure 2-5.)

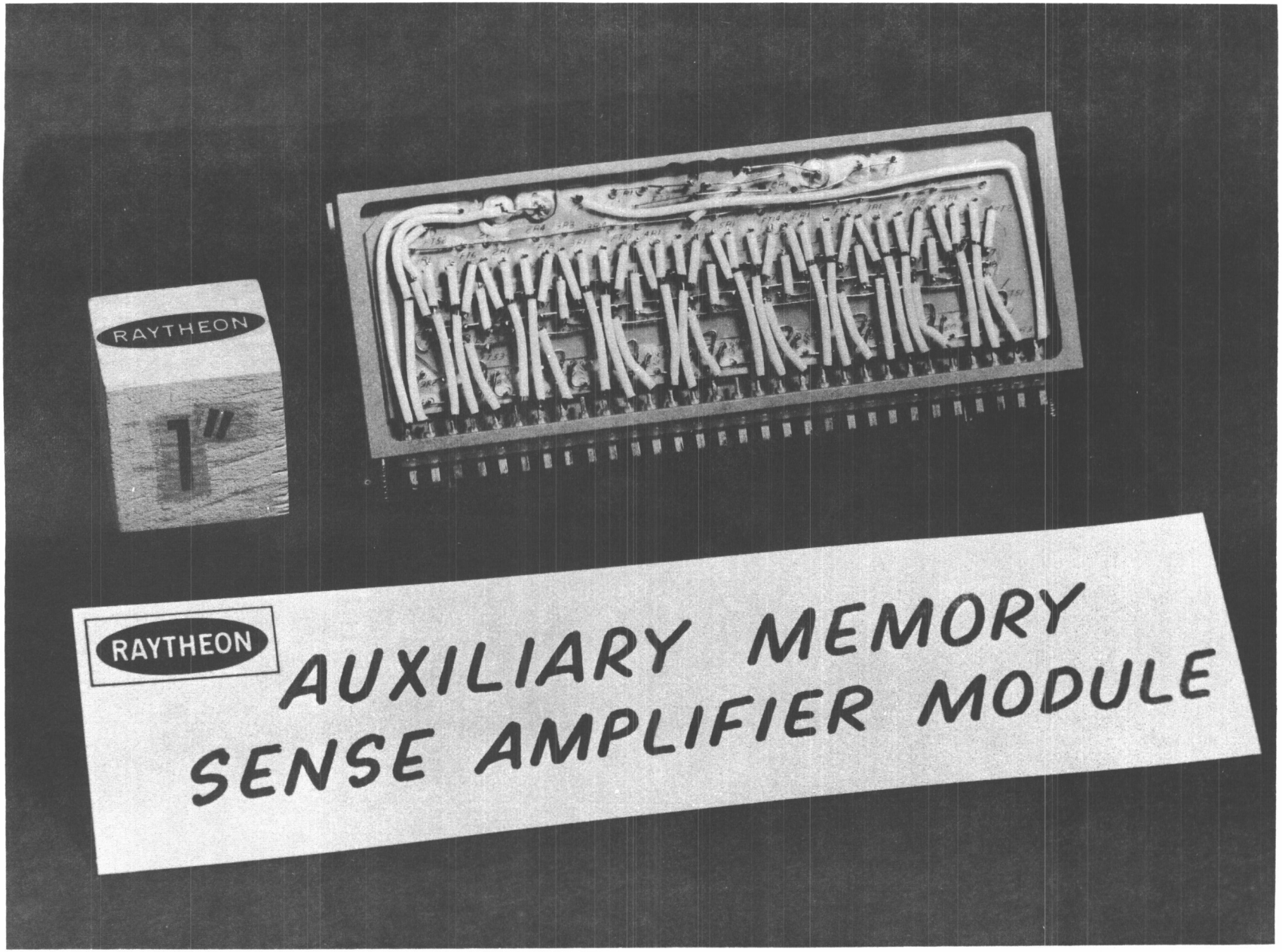
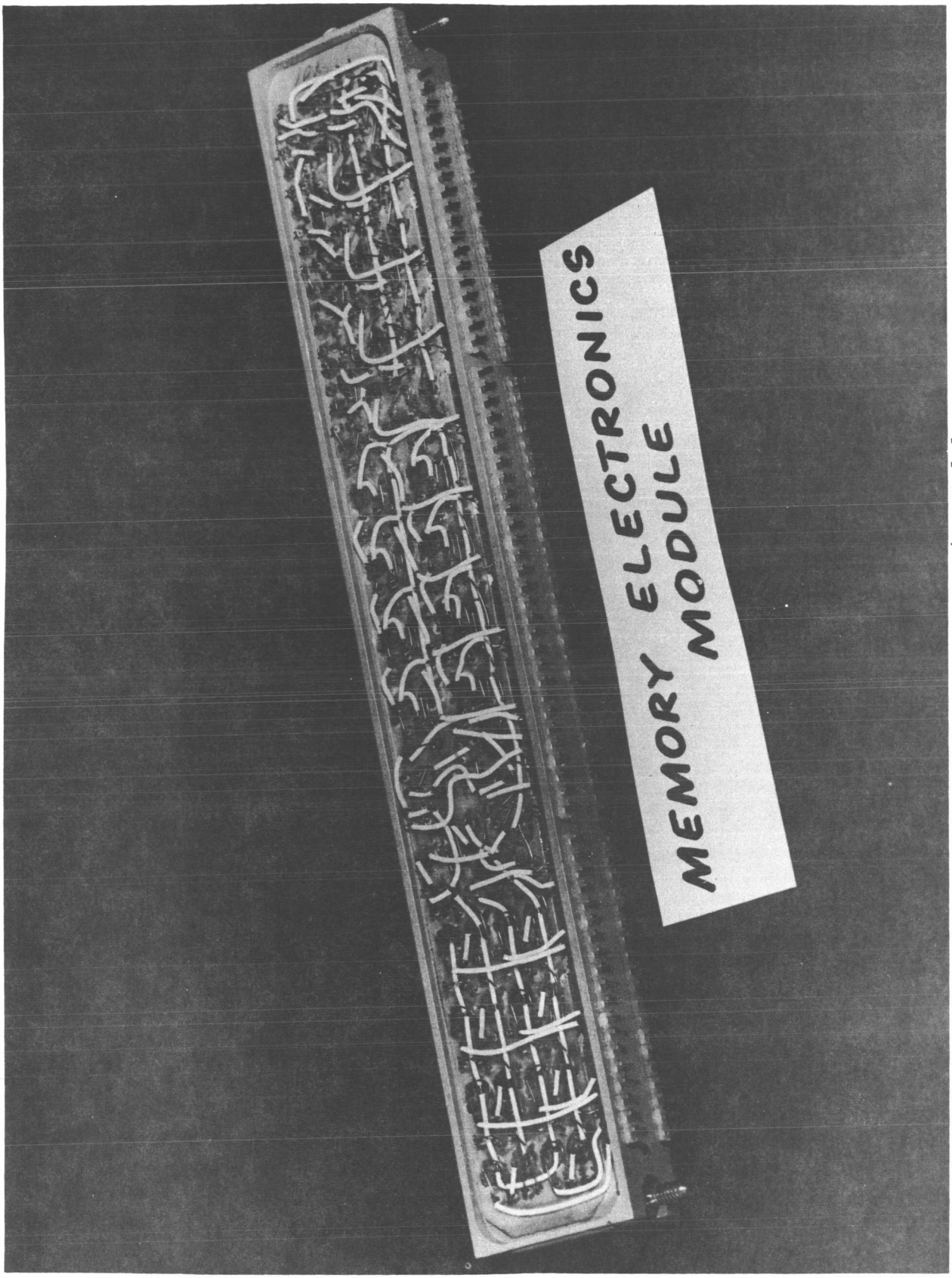


Figure 2-4 Auxiliary Memory Sense Amplifier Module

CN-4-648



CN-4-691

Figure 2-5 AM Electronics Module

The relationship between the address and the particular location referenced is different for each of the three address schemes (see Figure 2-6).

Without elaborating on the details presented in Figure 2-6, assume that a fifteen bit binary address is formed in order to select a word in memory. (Note that a 15 bit address provides access to 2^{15} or 32K words, so some bit combinations are redundant.) This address is decoded to form top and bottom selection signals, and a memory unit selection signal.

An example of memory operation is shown in Figure 2-7 with the associated timing diagram, Figure 2-8. For this example only, the YBO and YTO read/write current drivers are shown (referenced as G/2 circuits); there are seven additional drivers, plus sixteen x (bottom and top) drivers not shown. For these details, see Drawing No. 194790 (part of Acceptance Data Package).

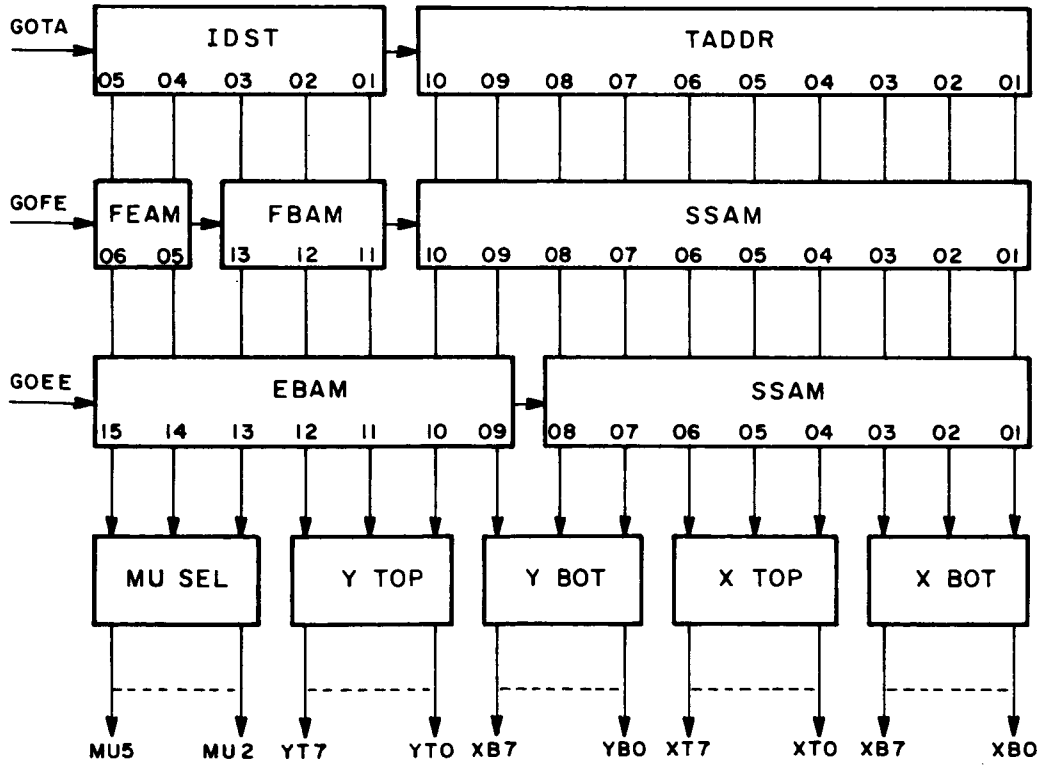


Figure 2-6 ACM Address Relationship for Tape, Fixed and Erasable Addresses

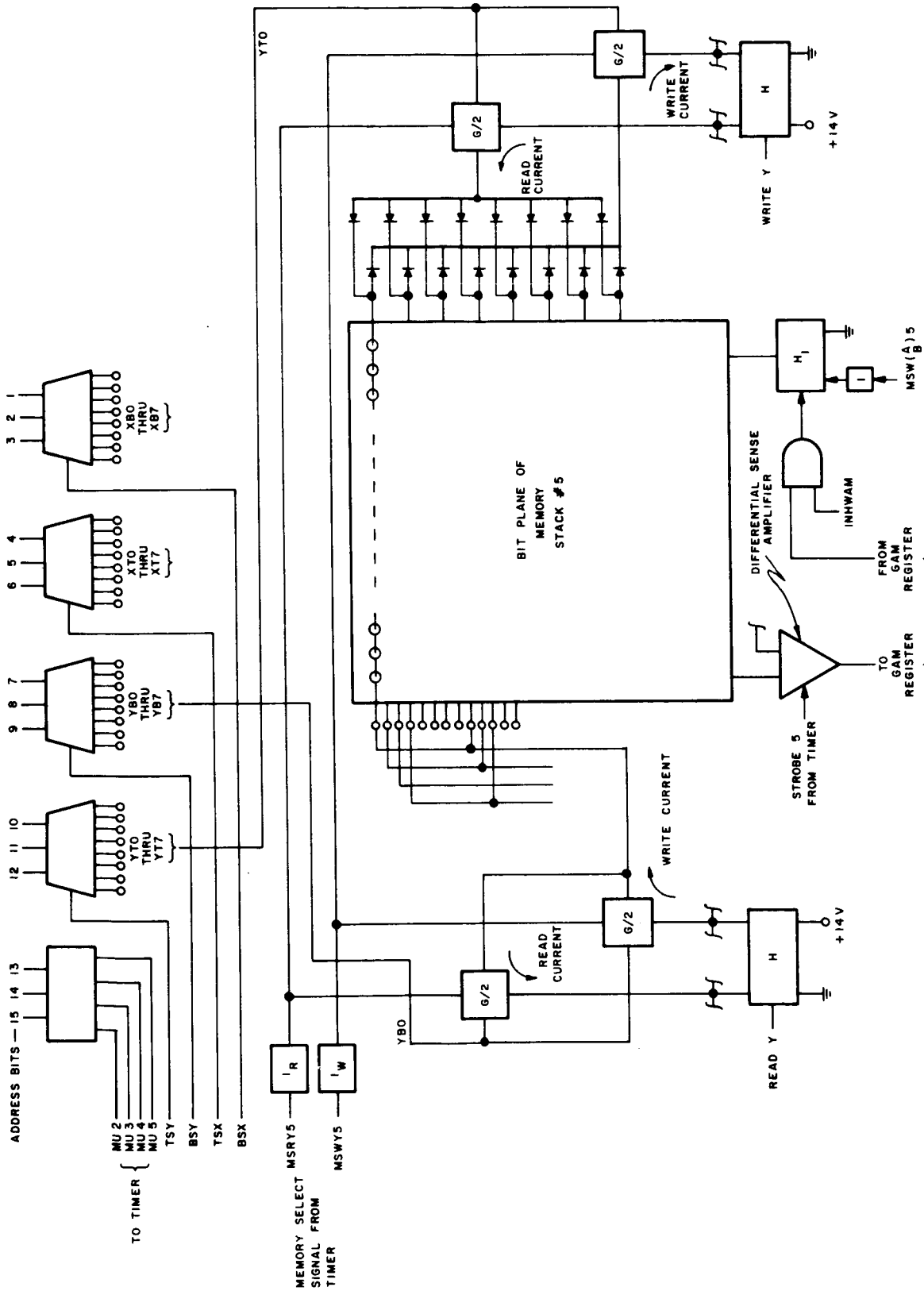


Figure 2-7 Memory Unit 5 - Typical Operation

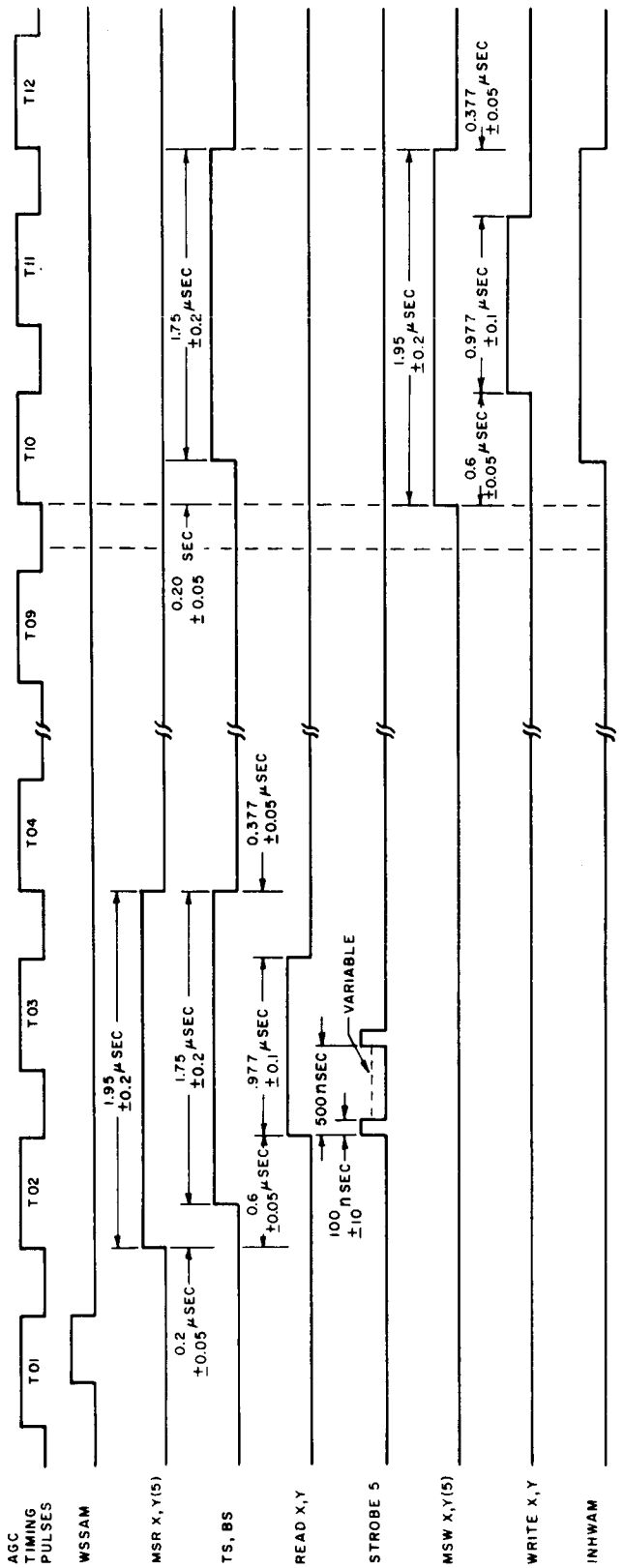


Figure 2-8 Memory Timing

The timing diagram of Figure 2-8 assumes that an MU5 address exists at T02 (from either the AGC or the tape address register, TADDR) and a Memory Select Read 5 pulse is emitted to select the MU5 Read electronics (MSRX5 and MSRY5). This pulse turns on the "I_R" circuits in Figure 2-7, and this enables the Read Drivers (G/2). The top select and bottom select signals (TSY, TSX, BSY, BSX) occur shortly thereafter and gate the top and bottom decoded address lines into the G/2 circuits.

Because the address decoder outputs are "one-out-of-eight," only one each of YT, YB, XT, and XB are ever excited at one time. In Figure 2-7, this is shown for the YBO and YTO case, and similar action takes place for an XB and an XT. The READY pulse gates the H circuits and read current flows in one of the 64 Y selection lines. Simultaneously, the READY pulse gates a similar amount of current in the X dimension.

In any bit plane, the currents converge at a particular core causing the core to switch if it contains a "1." The sense line threading the cores of the plane is connected to a sense amplifier which, when strobed by the STROBE5 pulse from the timer, will set the appropriate flip-flop in the GAM register.

Once information is strobed into the GAM register, the parity is tested and other operations cause the information to be transferred to the AGC, or on to the ATM register to be written on the tape.

The restoration of the memory begins at T10 with MSWX5 and MSWY5 which enable the G/2 writing current drivers, and MSW(A,B)5 which enable the MU5 Inhibit drivers (H_I circuit of Figure 2-7) TS(X,Y) and BS(X,Y) select the decoded address, and this enables "one-out-of-eight" of the groups of G/2 circuits. Simultaneously, the signal INHWAM gates information bits from GAM to the inhibit (H_I circuit of driver Figure 2-7).

The WRITEX and WRITEY pulses from the timer turn on the appropriate H circuits and the corresponding G/2 circuits switch on, causing the write current to flow in the X and Y directions. This write current flows in a direction opposite to that of the read current, and is always along the same path.

This basic cycle is used for any ACM address reference. If the reference is made for the AGC, then the address bits presented to the decoder come from some AGC oriented registers in the ACM (i.e., SSAM (SAM), EBKAM, FBKAM, FEAM); if the reference is made for serving the ATM, then the address bits are from internal ACM registers used for housekeeping the ATM operations (IDSTRT, TADDR).

2.2.3 VOTING AND CORRECTING PHILOSOPHY

2.2.3.1 Triple Modular Redundant Word Format

The process of storing an AGC 15 bit word on the ATM tape in the TMR mode involves unpacking the AGC word into 3 groups of 5 bits each. Each group is assigned a parity bit so that the sum (mod. 2) of all six bits is one. Any six bit group is written on the 18 channel tape in three places: in channels (tracks) 1-6 and 13-18, and in channels 7-12 inverted. A single 18 bit word so written on the tape is referred to as an ATM word and contains enough information (redundantly) to define one third of an AGC word.

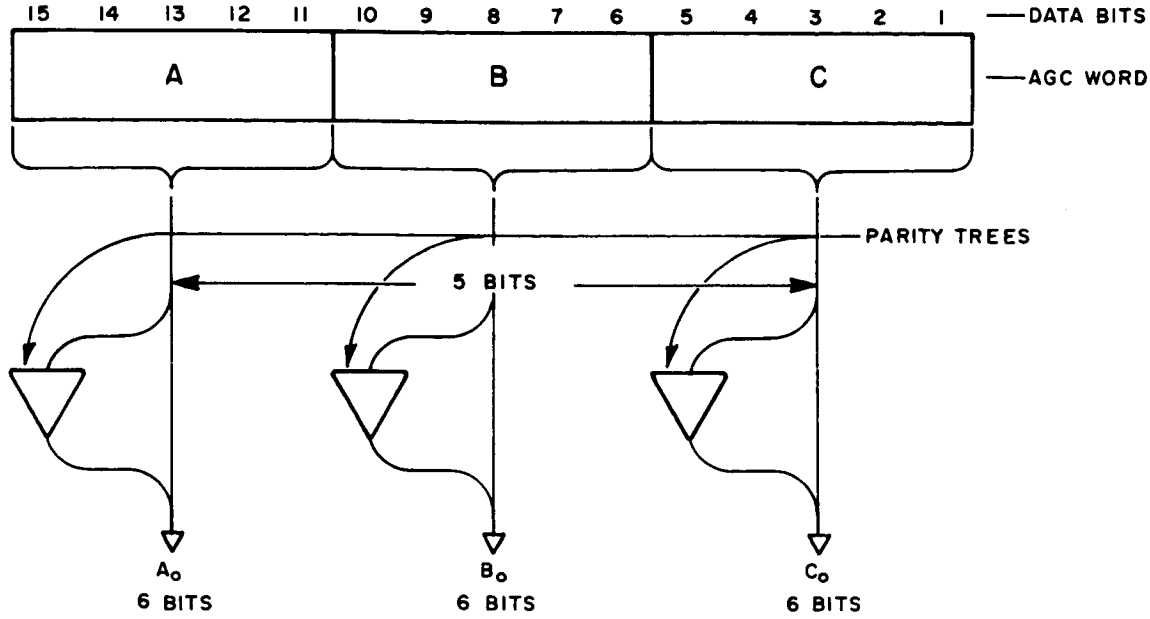
The relationship is perhaps made clearer by Figure 2-9. The first 5 bits of an AGC word (A) are fed into a parity tree generating a sixth bit; the six bits (A_o) are written on the tape as A_o, $\overline{A}_o$, A_o. This is followed by B_o, $\overline{B}_o$, B_o and C_o, $\overline{C}_o$, C_o completing the AGC word.

2.2.3.2 TMR Retrieval

The recovery of TMR information from the tape is significantly more complex due to the voting and correcting that must take place in order to decrease the composite error rate.

ATM words are received once every 78 μs (average) and they are successively unscrambled and compacted into a 5 bit group which represents a third of some AGC word.

When received, the 18 bit ATM word is first corrected for skew and jitter, then strobed into an input buffer register (see Figure 2-10).



WTRKS			ATM TAPE
1	P_3	P_2	P_1
2	11	6	1
3	12	7	2
4	13	8	3
5	14	9	4
6	15	10	5
	A_o	B_o	C_o
7	$\overline{P_3}$	$\overline{P_2}$	$\overline{P_1}$
8	$\overline{11}$	$\overline{6}$	$\overline{1}$
9	$\overline{12}$	$\overline{7}$	$\overline{2}$
10	$\overline{13}$	$\overline{8}$	$\overline{3}$
11	$\overline{14}$	$\overline{9}$	$\overline{4}$
12	$\overline{15}$	$\overline{10}$	$\overline{5}$
	$\overline{A_o}$	$\overline{B_o}$	$\overline{C_o}$
13	P_3	P_2	P_1
14	11	6	1
15	12	7	2
16	13	8	3
17	14	9	4
18	15	10	5
	A_o	B_o	C_o

3 ATM Words

Tape Motion

Figure 2-9 Triplex Word Generation

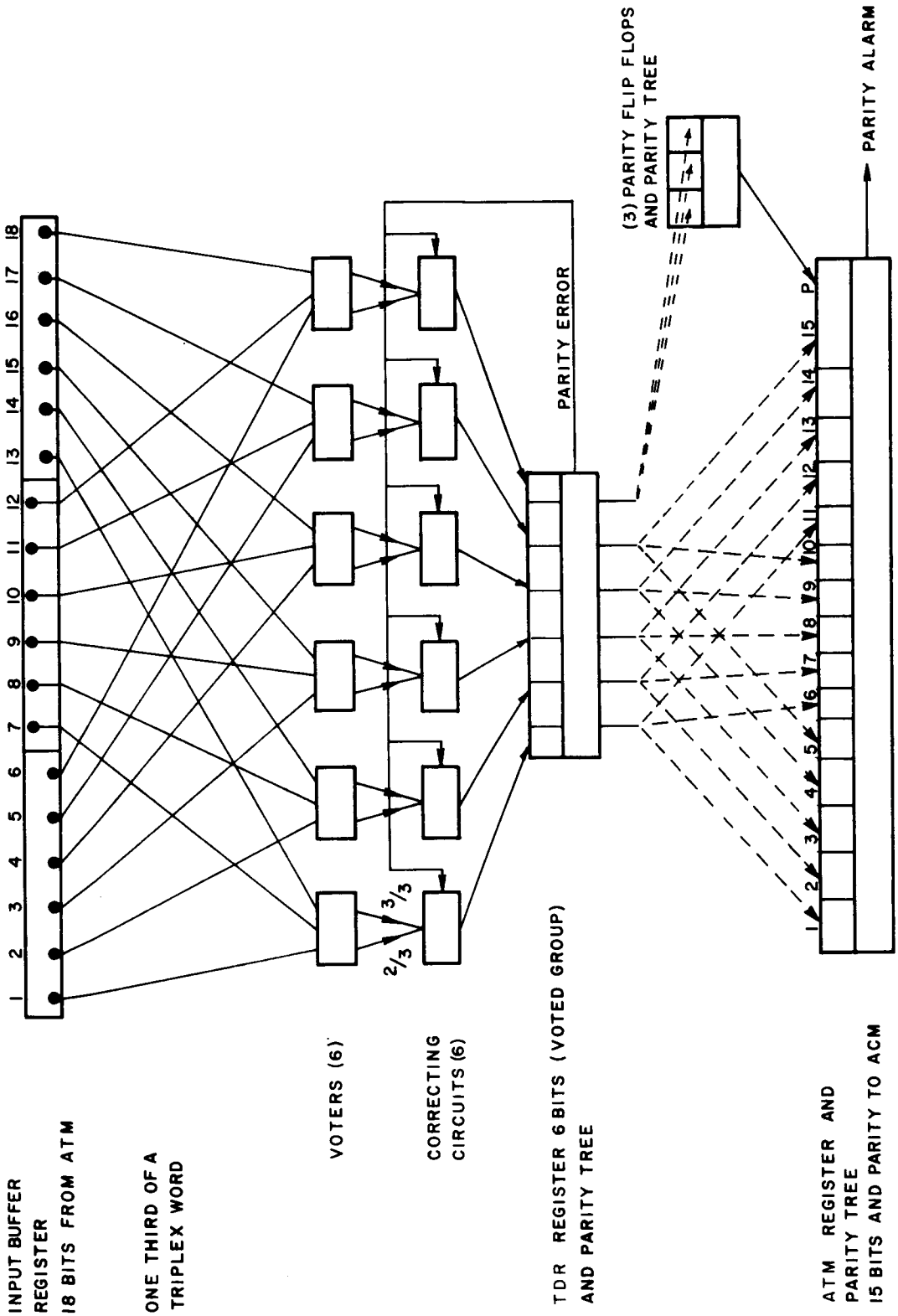


Figure 2-10 Voting and Correcting Algorithm

Bit positions 1, 7, and 13 of the input buffer register correspond to the first bit of a 6 bit group. Similarly, bit positions 2, 8, and 14 correspond to the second bit of that group, 3, 9, and 15 to the third and so on. The output of the input buffer (center inversion corrected) is majority voted in six groups of 3 bits each, and the voted information is stored in the 6 bit TDR register. If the parity tree associated with the TDR register detects a parity error, then the correcting circuits are interrogated to determine which voter had inputs which were not unanimous. The flip-flop in the TDR register corresponding to this voted set is toggled so that its state is changed. The parity is tested again and if correct, the 6 bit word in the TDR is "accepted"; the five information bits a r e steered to the appropriate sector of the ATM register and the parity bit stored separately.

After three such ATM words are accepted and unscrambled, the composite parity is formed by the three voted and corrected parity bits which were received in each voted group. This parity bit, along with the fifteen data bits in the ATM register, is checked again for parity. If the word is acceptable, it is eventually sent to the ACM register before the next ATM word comes from the tape.

2.2.3.3 TMR Correcting - Example

An 18 bit word containing errors is received in the Input Buffer register. Assume a single error in bit positions 2 and 8 is indicated in Figure 2-11. All voters except the second output their information due to unanimous voting. The second voter outputs a "0" due to a simple majority (2/3) and the parity in TDR is found to be wrong. This information causes the appropriate TDR flip-flops (the second, in this example) to change state; in this case, to a one. The parity is again tested and the word in TDR is found to be acceptable. The acceptable information (111000) is steered to the appropriate portion of the ATM register and parity flip-flop.

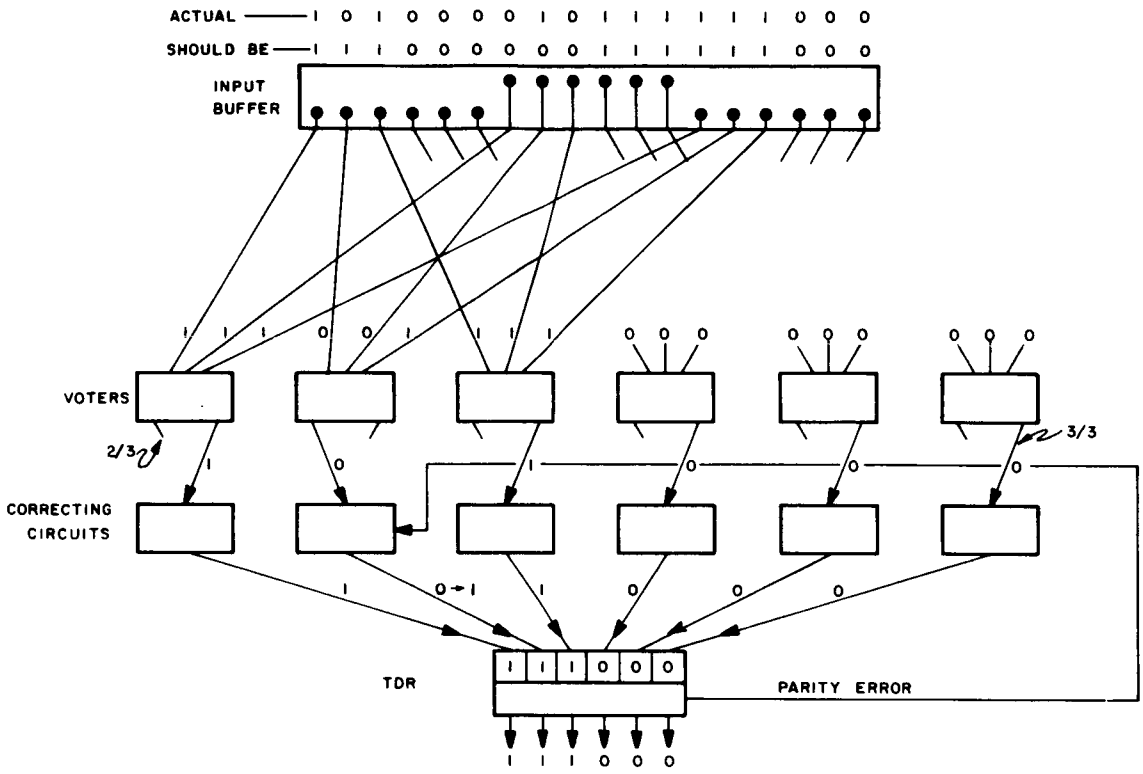


Figure 2-11 TMR Error Correcting Circuits

2.3 AGC MEMORY EXTENSION

2.3.1 MEMORY ADDRESS ASSIGNMENT

The contents of any location in the four core stacks can be obtained via 3 distinct addressing schemes. One scheme allows addressing every location as extended E memory, another as extended F memory. A third scheme only applies when the memory is addressed in conjunction with tape operations, and in general is not under AGC control.

When addressed as FIXED memory, the c(FBAM), c(FEXTAM), and c(SSAM) are decoded to select the appropriate memory unit (MU) and location within. When addressed as erasable memory, the c(EBAM) and c(SSAM) are decoded to select a location in a similar manner. Access via erasable addresses is restricted to 6144 words (half of MU4 and MU5) EBAM 10 through 37. MU2 through MU5 is addressable under GSE control. The GSE CONTROL switch on the control panel allows MU2, MU3, and half of MU4 (EBAM 40-107) to be addressed as erasable. When addressed for reading or

writing on tape, the lower five bits of IDSTRT are decoded to select a 1024 word sector in one of the four MU's; TADDR is decoded to select a word within that sector.

An address "selector" switches the appropriate bits of the above registers into the address decoder which selects the MU and the X and Y lines. The address bits chosen by the selector are a function of certain bits of SAM and the bank registers (to determine if the AM memory cycle is for reading or writing on the tape). This decision is made at TØ1 of every AGC cycle.

Table 2-2 describes the complete address scheme (including the AGC addresses) and relates these addresses to the memory units in the ACM.

2.3.2 ADDRESS DETECTION LOGIC

The AM SAM register is loaded (in parallel with the AGC S register) at TØ8 with the address of the next word to be provided by memory. This section describes the ACM logic which controls the operation of the ACM memory using this address.

The ACM must respond to AGC requests for information when the address generated by the computer lies within the AM address field. It is not possible to make this decision based solely on the contents of SAM and FBAM or EBAM at T08, because the next instruction may be a Quarter Code instruction which modifies bits 11 and 12 of S at TØ1 or an INKL or RUPT 0 which forces an E-cycle (which may be an ACM cycle). The ACM waits until this change to S is made at TØ1; data is read from ACM memory and available to the AGC.

The data can be sent to the AGC by means of two "routes": one in which the data from the ACM ends up in the AGC G register, and another in which the data ends up in another central register as if it had come from G. The implementation of these techniques is straightforward: simply insert the data on the write-line inputs (MDT01 through MDT16) at a time when the AGC executes a WG control pulse or whenever the AGC executes RG and W (any register).

TABLE 2-2

AGC and AM ADDRESSES

ACM REGISTERS

MEMORY UNIT	COMMENTS	MEMORY TYPE	ERASABLE BANK REG. (AM)	FIXED BANK REG. (AM)	FIXED EXTENSION BITS (AM)	SAME VALUE (SAME AS AGC S-REG.)
AGC MEMORY		Unswitched E	XXX	XX	X	0000-1377
		Unswitched E	0X0	XX	X	1400-1777
		Unswitched E	0X1	XX	X	1400-1777
		Unswitched E	0X2	XX	X	1400-1777
		Switched E	0X3	XX	X	1400-1777
		Switched E	0X4	XX	X	1400-1777
		Switched E	0X5	XX	X	1400-1777
		Switched E	0X6	XX	X	1400-1777
		Switched E	0X7	XX	X	1400-1777
ACM MU2	1. Addressable as E only on ground under GSE control. 2. MU2,3 not supplied in engineering model. 3. Contents cannot be transferred to tape.	Extended E	040	XX	X	1400-1777
		Extended E	041	XX	X	1400-1777
		Extended E	042	XX	X	1400-1777
		-- and so on through --				
		Extended E	053	XX	X	1400-1777
		Extended E	054	XX	X	1400-1777
		Extended E	055	XX	X	1400-1777
		Extended E	056	XX	X	1400-1777
		Extended E	057	XX	X	1400-1777

TABLE 2-2 (Continued)

AGC and AM ADDRESSES

MEMORY UNIT	COMMENTS	MEMORY TYPE	ERASABLE BANK REG. (AM)	FIXED BANK REG. (AM)	FIXED EXTENSION BITS (AM)	SAME VALUE (SAME AS AGC S-REG.)
ACM MU3	See MU2 Comments	Extended E	060	XX	X	1400-1777
		-- and so on through --				
		Extended E	077	XX	X	1400-1777
ACM MU4	1.Addressable as erasable only under GSE control.	Extended E	100	XX	X	1400-1777
		Extended E	101	XX	X	1400-1777
		-- and so on through --				
	2.Contents cannot be transferred to tape.	Extended E	107	XX	X	1400-1777
	3.2048 wds always available as erasable.	Extended E	010	XX	X	1400-1777
		Extended E	011	XX	X	1400-1777
		-- and so on through --				
	4.Contents cannot be transferred to tape.	Extended E	017	XX	X	1400-1777
ACM MU5	1.4096 wds always available as erasable.	Extended E	020	XX	X	1400-1777
		Extended E	021	XX	X	1400-1777
		-- and so on through --				
	2.Contents can be transferred to tape.	Extended E	035	XX	X	1400-1777
		Extended E	036	XX	X	1400-1777
		Extended E	037	XX	X	1400-1777

TABLE 2-2 (Continued)

AGC and AM ADDRESSES

MEMORY UNIT	COMMENTS	MEMORY TYPE	ERASABLE BANK REG. (AM)	FIXED BANK REG. (AM)	FIXED EXTENSION BITS (AM)	SAME VALUE (SAME AS AGC S-REG.)
AGC MEMORY (FIXED) OR PAC MEMORY		Fixed-Fixed	XXX	XX	X	4000-7777
		Switched F	XXX	00	X	2000-3777
		Switched F	XXX	01	X	2000-3777
		Fixed-Fixed	XXX	02	X	2000-3777
		Fixed-Fixed	XXX	03	X	2000-3777
		Switched F	XXX	04	X	2000-3777
		Switched F	XXX	05	X	2000-3777
		-- and so on through --				
		Switched F	XXX	26	X	2000-3777
		Switched F	XXX	27	X	2000-3777
		Super-Bank 0	XXX	30	0	2000-3777
		Super-Bank 0	XXX	31	0	2000-3777
		-- and so on through --				
		Super-Bank 0	XXX	37	0	2000-3777
		Super-Bank 1	XXX	30	1	2000-3777
		Super-Bank 1	XXX	31	1	2000-3777
		Super-Bank 1	XXX	32	1	2000-3777
		Super-Bank 1	XXX	33	1	2000-3777

TABLE 2-2 (Continued)

AGC and AM ADDRESSES

MEMORY UNIT	COMMENTS	MEMORY TYPE	ERASABLE BANK REG. (AM)	FIXED BANK REG. (AM)	FIXED EXTENSION REG. (AM)	SAME VALUE (SAME AS AGC S-REG.)
MU2	MU2 and MU3 not included in engineering model	Extended F	XXX	30	5	2000-3777
		Extended F	XXX	31	5	2000-3777
		Extended F	XXX	32	5	2000-3777
		Extended F	XXX	33	5	2000-3777
MU3	See MU2 (above)	Extended F	XXX	34	5	2000-3777
		-- and so on through --				
		Extended F	XXX	37	5	2000-3777
MU4	MU4 & MU5 included in engineering model	Extended F	XXX	30	6	2000-3777
		-- and so on through --				
		Extended F	XXX	33	6	2000-3777
MU5	See MU4 (above)	Extended F	XXX	34	6	2000-3777
		-- and so on through --				
		Extended F	XXX	37	6	2000-3777

The ACM makes use of both of these techniques to transfer data to the ACM, but since the AGC's control pulse sequence does not include WG at "convenient" times, in terms of the memory cycle timing, the control pulse WG must be forced to occur at a time when there is no other activity on the write lines.

Data from the ACM memory is either the argument of an arithmetic operation, or the next instruction to be executed. In cycles where the data is the next instruction, the AGC tests the c(G) at TØ7 for special operations (the so-called pseudo-instructions: INHINT, RELINT, and EXTEND). These cycles can be identified by the appearance of control pulse RAD at TØ8. During such cycles, it is necessary that the ACM data be inserted into the AGC's G register for testing at TØ7.

2.3.3 DATA TRANSFER

The ACM, if addressed, provides the data and forces it into G at any convenient time before TØ7 during these cycles. This is accomplished by the addition of a wire from the test connector to the WG/gate in the AGC. Such a signal from the ACM, if a "1", will force WGG = 1. This opens the G register to the write busses, thereby making possible a data transfer from GAM in the ACM, to G in the AGC.

For all other cycles (those which do not contain RAD), the control pulse RG is used to gate c(GAM) onto the read busses and then into whatever register the subinstruction requires. This is possible because these cycles do not test c(G) for TC3, 4, or 6 (INHINT, RELINT, or EXTEND) and the word in G (except in NDX1 and NDXX1) is the argument of an operation and not the next instruction to be executed.

The implementation of this technique involves decoding the present instruction in order to separate Instruction Fetch cycles from all others, and forcing c(GAM) into G at TØ4 during Fetch cycles addressing the ACM. TØ4 is selected because it is a common time of data buss inactivity in the AGC.

2.4 TAPE OPERATIONS

This section describes the operation of the ACM as it relates to processing requests by the AGC and sequencing the ATM to service such requests.

The ATM/ACM interface consists of three classes of signals; data lines for reading and writing, status and alarm signals, and command signals. The command signals are simply stated: forward/reverse, read/write, triplex/simplex.

Control of the ATM will be described for each of the operating modes in terms of these basic commands. Status and alarm signals and the data lines are introduced as circumstances warrant during the discussion.

2.4.1 READ TAPE INTO ACM

When the AGC requires access to tape-stored information (either program or data), it initiates a request to the ACM that the required information be read from the tape into an ACM core stack. This request takes the form of a sequence of channel write instructions (see Section 3.2, Tape Control). The channel address associated with the instructions is decoded for reference to those channels allocated to ACM tape control registers. When coincidence between an ACM channel address and control pulse MWCH occurs, subsequent tape control information flows between the AGC write busses and the appropriate control register specified by the channel address. The AGC may verify this process by reading back the contents of these control registers, again as channels.

The information loaded into tape-control registers consists of the following:

a. An ID Word, Stored in IDSTRT, Channel 21

This 15 bit word is used by the ACM to locate and identify the tape record containing the desired information. Bit 15 of the ID word is a tag designating the contents of the record as "program" or "data"; the other 14 bits are arbitrary as far as the reading mode is concerned. They do, however, have significance when discussing the organization of the tape.

b. A 5 Bit Word, Stored in IDSTP, Channel 23

This word is used only for multi-bank information transfers. Single record (bank) transfers do not require this information, and IDSTP is automatically cleared each time IDSTRT is loaded. IDSTP specifies the ID word which will terminate a multi-bank transfer.

c. Bit 10 in CONOUT, channel 25, indicating that the desired tape operation is writing, not reading, (a "one" here indicates the writing mode).

d. Bit 11 in CONOUT, which initiates the execution of any tape operation. This bit is known as command GOATM.

2.4.2 THE SEARCH SEQUENCE

To simplify the exposition, assume for the moment that the ATM control logic within the ACM was inactive while the AGC has been loading the control registers. When the execute command GOATM is received by the ACM, the following sequence of events occurs (see Figure 2-12).

The ATM is commanded to drive in reverse (tape command GOREV). After a 1-sec delay, the ATM replies with feedback signal TMREV (tape moving reverse). This delay allows the tape to accelerate to normal speed. The ACM rejects data read from the ATM tape until a hole in this data stream of at least 312 μsec (4 tape word times) flags the passage of an inter-record gap beneath the read head. The ACM now expects to receive the trailing ID of the next record toward the beginning of tape. Since all ID words are stored in triplex format, the next three tape words are processed as triplex in the Tape Data Receiver and the processed 15 bit word is stored in register IDREAD (channel 23). A 15 bit comparator examines the contents of IDREAD with respect to the contents of IDSTRT. The outcome of this comparison determines the action that follows.

If c(IDREAD) > c(IDSTRT), then command GOREV is maintained, the body of the record ignored, and a search instituted for the next gap and subsequently the next ID for comparison.

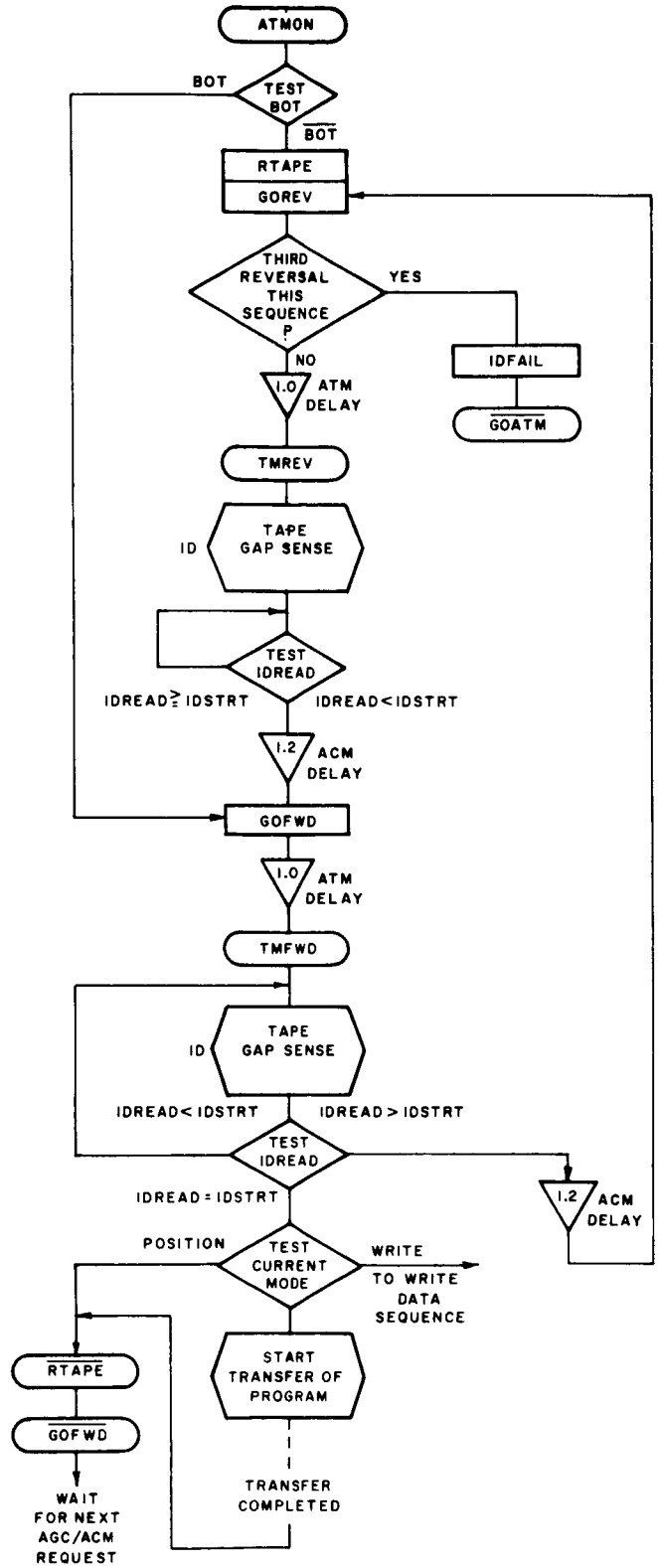


Figure 2-12 Tape Search and Read Sequences

If c(IDREAD) = c(IDSTRT), the desired record has been located. However, the data transfer must be performed in the forward direction since the tape address register can only be incremented. To assure that the read head does not pass over the desired record before the tape is up to speed after turnaround, the GOREV command is maintained until c(IDREAD) < c(IDSTRT) and for 1.2 seconds thereafter.

If c(IDREAD) < c(IDSTRT), the desired record is farther along the tape, or has just been detected and the direction of tape motion must be reversed. Command GOREV is maintained for 1.2 seconds after this condition is detected. Command GOFWD is substituted for GOREV, and the feedback signal TMFWD from the ATM awaited. Gap sensing is again instituted, and succeeding ID words compared until a match with c(IDSTRT) signifies that the desired record has been located. Since the tape is now moving forward, signal TRNSIP is posted in bit 8 of CONOUT as a flag to the AGC that a transfer is in progress.

The Search Sequence ends (by definition) when TRNSIP is set to "one."

2.4.3 DATA TRANSFERS WHEN READING PROGRAM TAPE

The read sequence begins with TRNSIP set to "one"; at this time signal TRNSBNK is also set to "one". TRNSBNK and TRNSIP are indistinguishable during single-bank tape reading transfers; only during multi-bank transfers is there a difference (TRNSIP remains set during the inter-record gap between successive banks, while TRNSBNK is reset to "zero" while these gaps are being sensed).

The Tape Data Receiver must decode tape words in one of two formats, simplex or triplex. During the search sequence, all reading is accomplished on ID words, which are always recorded in triplex. Bit 15 of IDSTRT is next examined to establish the format control for the body of the record. If bit 15 = "zero", the record is located on the program section of the tape, and all program tape records are recorded in the triplex format. If bit 15 = "one", the record is located on the data section of the tape, where either format may be used. Bit 3 of IDSTRT specifies the format in which the record was written.

When the appropriate format is established, the Tape Data Receiver will deposit 15 bit words into the ATM register every 80 μsec (simplex format) or 240 μsec (triplex format). When the ATM register has been filled, a request is forwarded to the AGC for a memory cycle; upon receipt of a feedback signal that the memory cycle has been released for AM use, the data word is transferred from the ATM register to the GAM (memory buffer) register. The memory address is composed from the 5 low-order bits of IDSTRT and the 10 bit TADDR (tape address) register. An AM memory cycle is initiated, transferring the tape word into the appropriate location within the ACM. Cycle stealing in this manner prevents conflict between the AGC and the ATM for ACM memory cycles at a cost of one memory cycle per transferred word. For a single bank transfer, this implies stealing 1024 x 12 μsec over a span of 1024 x 80 μsec or 1024 x 240 μsec (12.3 msec in 82 or 246 msec). Notice that no cycle stealing occurs during the search sequence, only during the actual data transfer.

The average rate at which words are available in the ATM register is fixed by format, tape speed, and bit density; skew and jitter introduce short-term variations about this average.

The long-term rate at which cycle stealing can be performed is well above the range considered here; however, the short-term response of the AGC to requests for cycle stealing is dependent on the instruction currently being executed, and the amount of counter increment and/or interrupt activity. The demonstration software included an exercise which repeatedly used the most critical instructions (divide and multiply) while tape transfers were in progress.

After each word is stored in the ACM memory, c(TADDR) is incremented to provide the storage address for the next word. When the last word has been stored, another increment returns c(TADDR) to its initial state of zero. The ID word found at the end of the record is ignored, and the inter-record gap is sensed. If the transfer includes only a single bank, it is now complete, and signals GOATM, TRNSIP (and incidentally

TRNSBNK) are reset to "zero" as flags to the AGC software. In the event of an error, (see 2.5) GOATM is reset to "zero" but TRNSIP is left at "one" as a failure indication to AGC software.

If a multi-bank transfer has been requested, TRNSBNK is reset to "zero," but not TRNSIP. After the inter-record gap has passed by the read head, the next ID word is processed by the Tape Data Receiver into the ATM register and stored in IDREAD. The start comparator examines c(IDREAD) and c(IDSTRT) as before. However, IDSTRT is incremented by one before this comparison is made. Thus, if the tape records contain consecutive ID words being scanned, the comparison will find equality between the (incremented) c(IDSTRT) and the current c(IDREAD) just read from the tape. TRNSBNK will be set, and the next record will be transferred into memory one word at a time using the cycle stealing technique exactly as before. Noitce that c(TADDR) begins again at zero, and that the incremented lower 5 bits of IDSTRT now refer to the next fixed bank within the ACM memory.

This process continues, bank by bank, until terminated by another comparison. At the end of each bank transfer, after IDSTRT is incremented and before c(IDSTRT) is compared with c(IDREAD), the incremented c(IDSTRT) is compared with c(IDSTP) in the stop comparator. IDSTP is a 5 bit register, channel 23, loaded by the AGC with a code such that this stop comparator can terminate the transfer after the appropriate number of records have been read. The stop code is thus the initial value loaded into IDSTRT, plus the number of records to be transferred. See Figure 2-13 for possible transfers.

A consequence of this implementation is that, if a multi-bank read is attempted spanning a set of consecutive ID words not all present on the tape, a failure will be reported (IDFAIL) only if the first record cannot be located. If a subsequent record cannot be located, the tape will continue moving forward until the EOT window is encountered. This condition will occur, despite the increasing sequence of ID words deposited in IDREAD, because the output of the comparator is ignored when TRNSIP is set to "one."

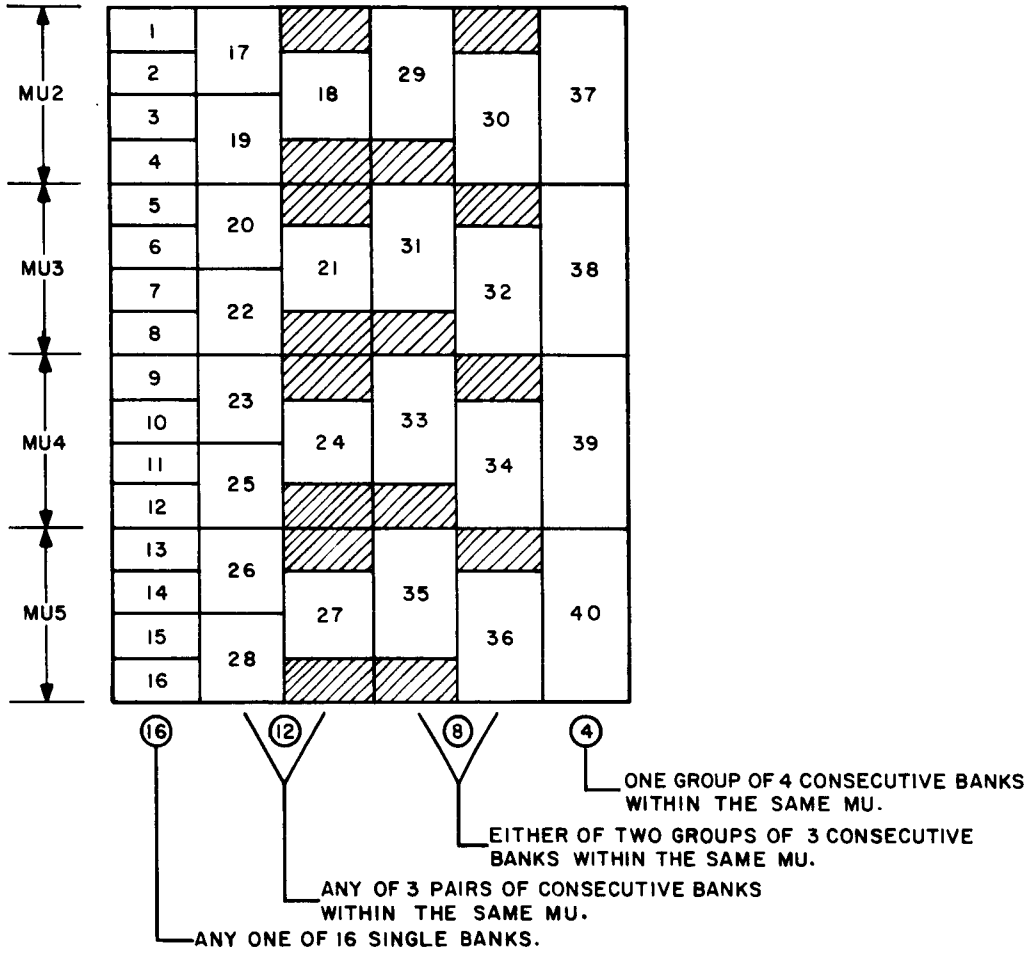


Figure 2-13 Possible Transfers from Program Tape to ACM Stack

The above discussion completes the analysis of the reading sequence for records from the Program Tape. The following material presents the reading sequence for records from the Data Tape.

2.4.4 DATA TRANSFERS WHEN READING DATA TAPE

The significant difference in reading records from the Data Tape is the use of IDSTRT in generating a memory address for use in storing the data word in the ACM core stack. Instead of using the 5 low-order bits of IDSTRT (and 10 bits from TADDR), only the two low-order bits are used (together with TADDR). The other three bits are replaced with the binary combination, "101."

This substitution restricts the transfer of information from the Data Tape to MU5, the last 4^k stack in the ACM. Up to four consecutive records can thus be stored in MU5; the possibilities are illustrated in Figure 2-14.

Words are stored in the ACM stack using the same cycle stealing technique as before, with TADDR incremented after each word has been stored.

2.4.5 WRITING ON THE DATA TAPE

The discussion of writing operations is restricted to the Data Tape since the Program Tape is loaded (written on) only under control of the GSE prior to a mission. In this context, it should be noted here that the ATM will not respond to a command to write on the program tape, without GSE control. Computer software will also refuse writing on the program tape if bit 15 of IDSTRT = "zero" (denoting a program ID) when GOATM is set (bit 11 of CONOUT). Writing on the Program Tape is described in Appendix C.

If bit 15 of IDSTRT = "one" (denoting a Data ID), then writing on the tape is permitted by the software.

2.4.5.1 The Search Sequence for Writing

The first requirement for writing on the Data Tape is that the tape be positioned correctly so that the desired information can be recorded

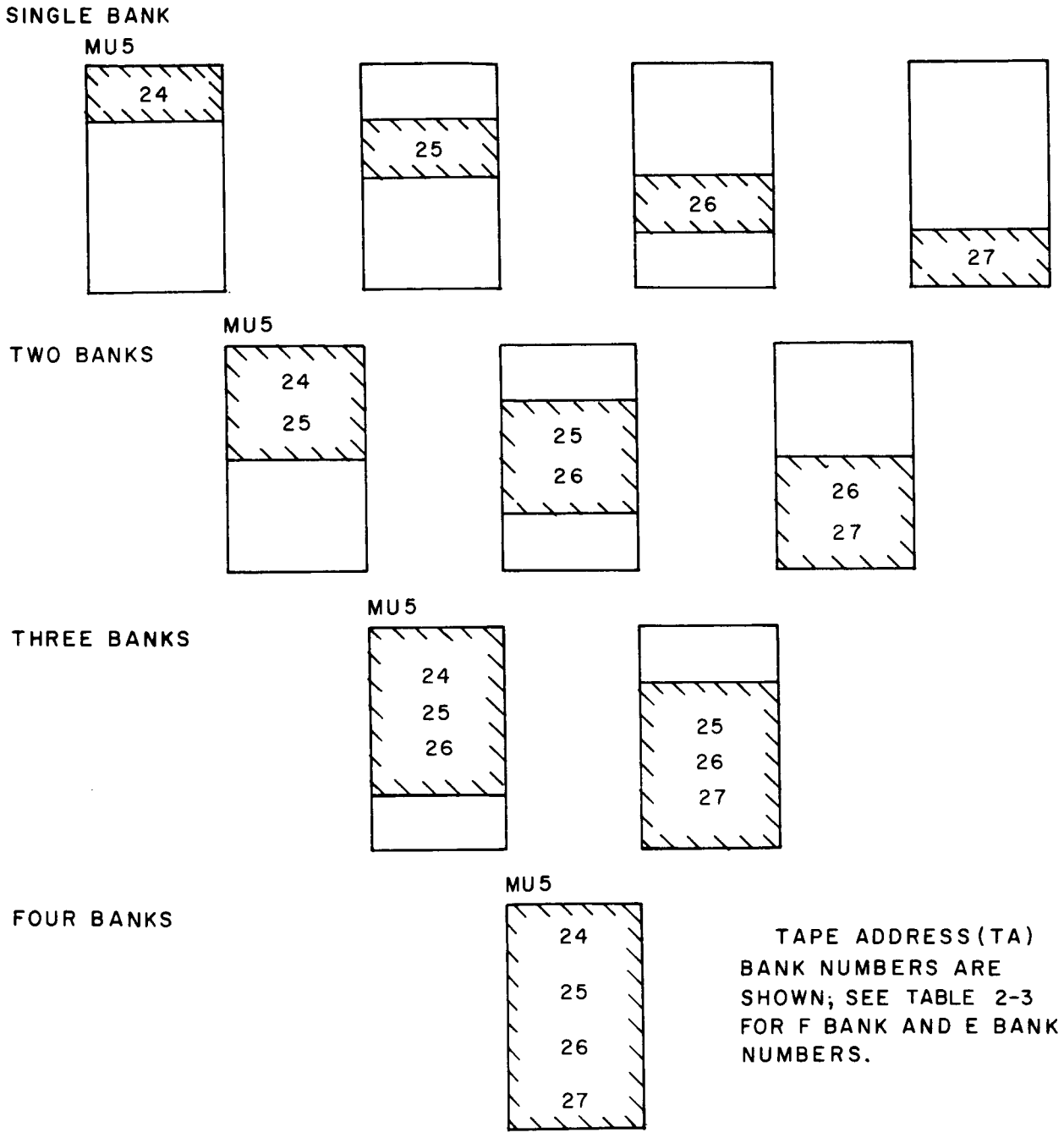


Figure 2-14 Possible Transfers between MU5 and the Data Tape

and identified for retrieval. This is accomplished through a search sequence almost identical to that employed for reading operations, the only difference being that the c(IDSTRT) now identifies the record after which the new information is to be recorded; that is, c(IDSTRT) is the last record written.

The AGC must, therefore, maintain a table of last ID words written on the Data Tape (see 3.2) for use in loading channel IDSTRT.

The search sequence is again initiated when the AGC sets GOATM to "one," the write command (bit 10 of CONOUT) previously (or concurrently) having been set to "one." The sequence proceeds as before until c(IDREAD) = c(IDSTRT) with TMFWD. At this point, instead of initiating a tape read operation, the write sequence takes place.

2.4.5.2 Tape Write Sequence

The write sequence (Figure 2-15) begins with the conditions just described. The record identified by c(IDSTRT) is allowed to pass beneath the read head, and gap sensing is instituted. As soon as a gap of at least 4 word times has been detected, the ACM assumes that the identified record has been completely by-passed, and the ATM is commanded to switch from the read mode to the write mode. (Command RTAPE is removed, and command NBLWDATA initiated.)

The memory address of the first word to be written (which will be the ID word) is composed as follows:

The most significant three bits are forced to be "101" by signal MU5SEL; the next two bits are taken from bit positions 4 and 3 of channel IDSTP, and the remaining bits from register TADDR. Since TADDR is initially zero, this composite address refers to the first word in one of the 4 fixed banks within MU5.

A memory cycle is requested from the AGC and, when acknowledged, the stolen cycle time is employed to exercise the ACM stack with the composite address. The data is transferred from the ACM memory buffer register (GAM) to the ATM register, and the AGC allowed to proceed.

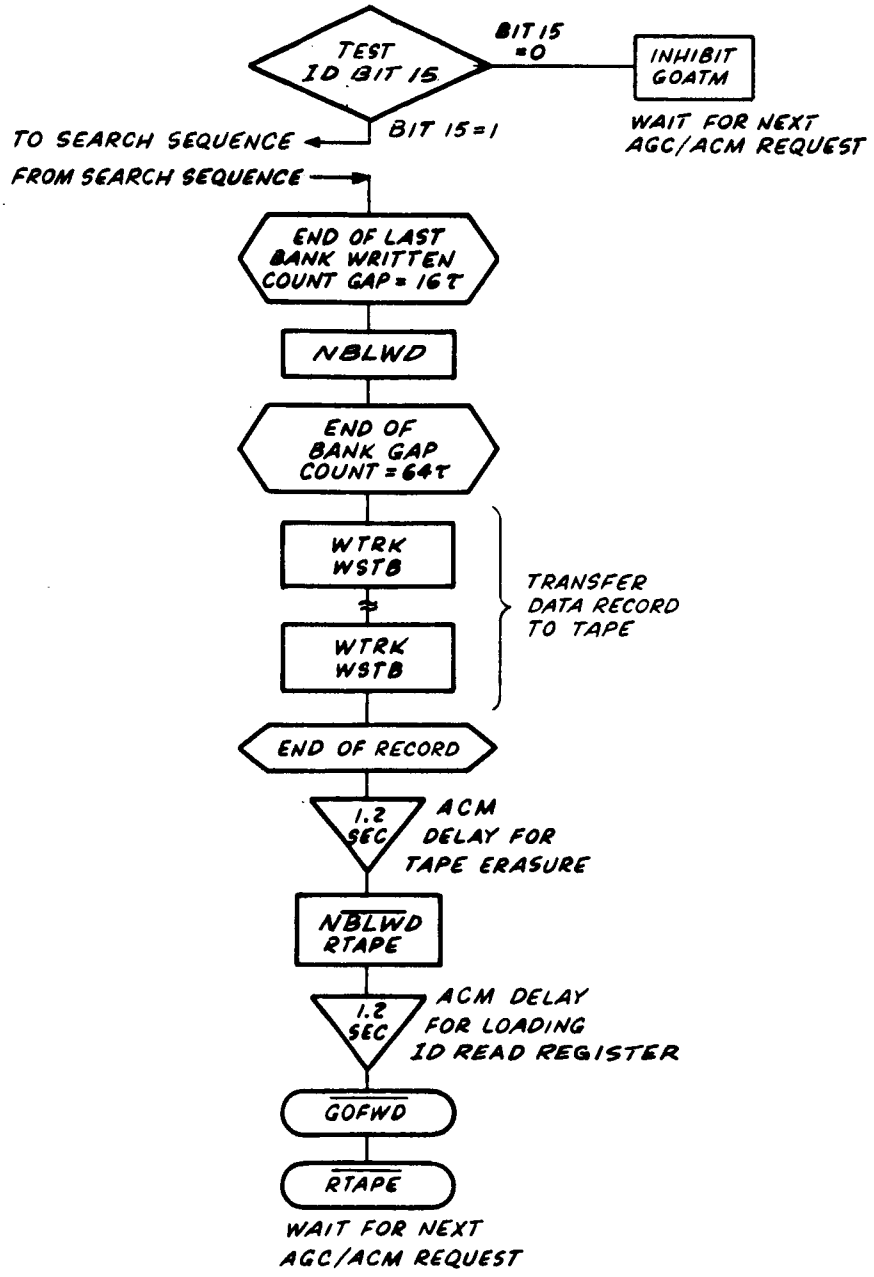


Figure 2-15 Tape Write Sequence

Since this word is the first to be written after an inter-record gap, it must be an ID word, and must also be written in triplex. Signal IDTRSM is used to notify the tape data transmitter that this is a leading ID word. The word is written on the tape in triplex, over an interval of 240 μsec. When the ATM register has been emptied, another AGC cycle steal request is made. This cycle, when acknowledged, is used to obtain the first data word in the body of the record. The word is again transferred to the ATM register, and the AGC allowed to proceed. Bit 9 of channel CONOUT is now examined so that the Tape Data Transmitter may write the body of the record in the appropriate format, triplex if "zero" and simplex if "one." Observe that while bit 9 of CONOUT controls the writing format, bit 3 of the ID word as read from the data tape controls the reading format. Note also that the contents of the first word in the specified bank from MU5 has now been written on the tape twice; once in triplex as the ID word, and again as the first data word (simplex or triplex, depending on CONOUT bit 9).

The Tape Data Transmitter processes the data word from the ATM register to the tape in the prescribed format. When the ATM register is available for the next data word, another cycle steal request is sent to the AGC. When the request is granted, the ACM core stack is exercised to obtain the next data word in the GAM register. Meanwhile, c(TADDR) has been incremented by one, so that the composite address now refers to the next location in the same bank within MU5. The word is stored in the ATM register, and the process continues as described until the last data word has been written on the Data Tape. The process of incrementing c(TADDR) returns it to all "zeros" and is represented by signal IDTRSN, which means that it is now time to write the trailing ID word on the tape immediately following the body of the data record. C(TADDR) having returned to zero, a cycle can be stolen using the current composite address to obtain the first location of the bank again. This is, of course, the same word that was used in writing the leading ID as well as the first data word. It is written again as the trailing ID, with the format forced to be triplex.

Following this trailing ID, the tape is allowed to move while the head erases the tape for 1.2 sec. This assures that a gap follows the record just written.

Meanwhile, IDSTRT is incremented by one, generating the composite address of the first word in the next bank within MU5. A comparator (stop comparator) examines the upper bits of this address with respect to bits 2 and 1 of IDSTOP, which must be loaded by the AGC with one more than the last bank to be transferred (see last column in Table 2-3). Equality will indicate a "stop write" condition; otherwise, writing of the next bank followed by another increment and comparison cycle will occur.

2.4.5.3 Read Sequence After Writing

When a "stop write" condition is detected, the NBLWD command is removed, and RTAPE reinstituted. This causes the ATM to switch from the write to the read mode.

The read mode is continued until the next ID word is found and stored in channel IDREAD; GOATM, TRNSIP, and GOFWD are reset to "zero," stopping the tape. This process permits the AGC to interrogate IDREAD and verify that there still remains sufficient tape to accomplish another write operation before reaching the end of tape.

2.4.6 POSITION TAPE MODE

The time required to shuttle across the tape from end to end is approximately 7 minutes. In order to avoid lengthy delays on the order of minutes while the tape is moving into position for a read or write operation, an additional mode, called the Position Tape Mode, has been provided. This mode enables the AGC to take advantage of any advance knowledge it may posses relative to the program or data required during the next phase of mission operations by prepositioning the tape. In this way, a minimum time interval will be occupied by the search mode when the actual information transfer is requested.

TABLE 2-3

BITS 15 AND 14 UNDER GSE CONTROL

	F EXT	F BANK	*E BANK	TA	F EXT 7,6,5	F BANK 15→11	E*BANK 15 → 9	PT ID 5 → 1	DT ID 2,1
MU2	5	30	40 ↓ 43	10	101	11000	0100000 ↓ 0100011	01000	---
	5	31	44 ↓ 47	11	101	11001	0100100 ↓ 0100111	01001	---
	5	32	50 ↓ 53	12	101	11010	0101000 ↓ 0101011	01010	---
	5	33	54 ↓ 57	13	101	11011	0101100 ↓ 0101111	01011	---
MU3	5	34	60 ↓ 63	14	101	11100	0110000 ↓ 0110011	01100	---
	5	35	64 ↓ 67	15	101	11101	0110100 ↓ 0110111	01101	---
	5	36	70 ↓ 73	16	101	11110	0111000 ↓ 0111011	01110	---
	5	37	74 ↓ 77	17	101	11111	0111100 ↓ 0111111	01111	---
MU4	6	30	100 ↓ 103	20	110	11000	1000000 ↓ 1000011	10000	---
	6	31	104 ↓ 107	21	110	11001	1000100 ↓ 1000111	10001	---
	6	32	10 ↓ 13	22	110	11010	0001000 ↓ 0001011	10010	---
	6	33	14 ↓ 17	23	110	11011	0001100 ↓ 0001111	10011	---

(Table Continued Next Page)

TABLE 2-3 (Continued)

BITS 15 AND 14 UNDER GSE CONTROL

	F EXT	F BANK	*E BANK	TA	F EXT 7,6,5	F BANK 15→11	E*BANK 15→9	PT ID 5→1	DT ID 2,1
MU5	6	34	20 ↓ 23	24	110	11100	0010000 ↓ 0010011	10100	00
	6	35	24 ↓ 27	25	110	11101	0010100 ↓ 0010111	10101	01
	6	36	30 ↓ 33	26	110	11110	0011000 ↓ 0011011	10110	10
	6	37	34 ↓ 37	27	110	11111	0011100 ↓ 0011111	10111	11

*Bits 15 and 14 under GSE Control

The Position Tape Mode is initiated by the AGC in a manner very similar to that for a reading operation. Channel IDSTRT is loaded with the ID word of the record near which the tape is to be positioned, and CONOUT is loaded with the GOATM Command (bit 11). In addition, bit 7 of CONOUT is set to "one", signifying to the ACM that a Position Tape operation is requested.

The search sequence proceeds exactly as described for a single-bank read (see 2.4.2) until c(IDREAD) = c(IDSTRT). Instead of continuing into the read sequence, the tape motion command (GOFWD or GOREV) is removed, and GOATM reset to "zero". The tape is positioned about one second away from the specified record, so that when the tape is driven in reverse as part of the search sequence when the actual transfer is requested, a minimum delay will occur between sensing TMREV and c(IDREAD) = c(IDSTRT).

2.4.7 TAPE FORMAT

Information is recorded on the tape as a sequence of records. Each record contains 1024 AGC words in the body of the record. These words may be recorded in one of two modes, simplex or triplex. In the simplex mode, each AGC word corresponds to a single tape word, while in the triplex mode each AGC word corresponds to three tape words. Thus, the body of a record will be either 1024 or 3072 tape words long, depending on the mode in which it is recorded.

2.4.7.1 Windows

The 550-foot tape is divided into two parts by a center-of-tape (COT) window. The window consists of an area several feet long from which the oxide coating has been scraped, leaving the polyester backing exposed. This window extends laterally over the center 6 tracks of the tape. Passage of this window is detected by a sensor which scans the central 6 tracks; a relay is provided to remember on which side of the window the head is positioned.

A similar window is provided at each end of the tape, using tracks one through six for one, and thirteen through eighteen for the other. These windows are referred to as beginning-of-tape (BOT) and end-of-tape (EOT), respectively.

The region between the BOT and COT windows is known as Program Tape (PT); the region between the COT and EOT windows is known as Data Tape (DT). All information recorded on the Program Tape is presumed to be of such significance that it warrants the extra confidence obtained in the triplex mode; no simplex recording is performed on the PT.

Indeed, no recording of any information is permitted on the PT during a mission; the PT is presumed to have been loaded from an external source (see Appendix C) prior to launch.

Recording on DT may be performed in either mode at the discretion of the AGC.

2.4.7.2 Record Identification

To uniquely identify each record on the tape from all others, additional information in the form of an "ID word" is associated with every record. For convenience in searching the tape in either direction, this ID word is recorded both at the beginning and at the end of a record. Since retrieval of the ID words is essential to location of a desired record, all ID words are recorded in the triplex mode, irrespective of the mode in which the body of the record is recorded. Thus, the ID word adds 3 tape words at each end of a record (total of 6) to the 1024 or 3072 words in the body of the record.

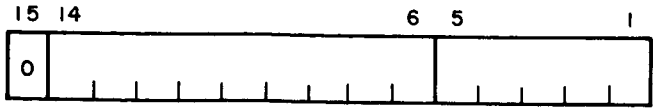
To enable detection of the beginning (or end) of a record, so that the ID word may be readily distinguished, records are separated by gaps. A gap is a group of at least four word times in which "all zeros" are read from the tape. Once this minimum gap length has been sensed, the ACM assumes that the next 3 tape words will define a triplex ID word.

Having thus provided for distinguishing and uniquely identifying each record, it now remains to describe the scheme for finding a particular record on the tape.

Since each record is associated with a unique ID word, this reduces to specifying the sequence of ID words on the tape. The tape search sequence that has been mechanized relies on a monotone increasing sequence of ID words for operation. Clearly there can be unused ID words, but all those present must be in an ordered sequence along the tape without repetition. (This last constraint is violated locally in certain exceptional circumstances to be noted later that will cause no difficulty.)

The ID words are arranged along the tape in sequence from 00000_8 to 77777_8. Since Bit 15 distinguishes program ID's from data ID's, ID words between 00000 and 37777 inclusive are found on the Program Tape, and ID words between 40000 and 77777 inclusive are found on the Data Tape.

The organization of a program ID word is illustrated here:



Bit 15 is "zero" indicating a program ID, and bits 5 through 1 specify the bank into which the record will be transferred when it is read. Since bit 15 is "zero" (program tape), the mode in which the body of the record has been written is always triplex. The remaining 9 bits provide for 777_8 or 512_{10} distinct records for each ACM bank. Considering that a triplex record occupies 3.6 inches of tape with a minimum gap (no provision for rewriting), this is adequate for a program tape roughly half the 550' total length.

This is also more than seems necessary even if programs are stored in several places along the tape under different ID's.

The regions in the vicinity of the BOT and EOT windows are prone to error, due to distrubing the oxide coating when forming the windows. Although the transport has interlocks which prevent unspooling of the tape in the pack, these interlocks depend on lamps for their operation. To provide assurance that a lamp failure does not ruin the tape by permitting unspooling to occur, the following shceme has been devised.

Certain ID words have been reserved for use as BOT and EOT markers. These ID words are not associated with the leading or trailing edge of a record, but exist as discrete records, each 3 tape words long (written in triplex).

These ID word markers provide the AGC software with clues as to how close to the end of the tape the head is positioned. For example, when a write sequence has been completed and the ATM reverts to the reading mode, as long as the AGC finds c(IDREAD) = 77776, it is assured that enough tape remains for at least one additional multi-bank record to be written before EOT is reached. If c(IDREAD) = 77777, there is no guarantee that any tape remains. This scheme is mechanized by filling the data tape with ID word markers containing 77776, until the vicinity of

the EOT window, where the content becomes 77777. If the AGC software interprets these ID word markers in this manner, the EOT sensor is not required, since the tape will never be driven far enough to expose the EOT window.

Similarly, proceeding in reverse toward the BOT window, a series of ID word markers containing 00000 indicates that the head is approaching the window. The number of such markers is sufficient to permit turn-around before exposing the window. No need for the equivalent of 77776 exists, since the Program Tape is always written forward out of BOT.

However, to facilitate the modification of records on PT via support equipment, it is desirable to provide file markers distributed throughout the PT. These file markers are additional ID word markers containing a uniform increasing set (00400, 01000, 01400, ..., 37000, 37400), spaced throughout the PT.

2.5 ALARMS AND FAILURE PROTECTION

2.5.1 ACM PARITY FAILURES

Every time a word is read from the ACM memory, its parity is tested in the parity tree associated with the memory buffer (GAM).

There are three ways in which a word is read from the memory:

a. AGC addresses ACM as E-memory, Figure 2-16
b. AGC addresses ACM as F-memory, Figure 2-16
c. Tape Processor requests a word to/from using the address in TADDR, Figure 2-17.

2.5.1.1 ACM to AGC as E-Memory

In case (a) above where the AGC addresses the ACM as E-memory, the E-memory cycle in the AGC is inhibited (via MAMU on A52) and consequently no parity test is made on the AGC G register by the AGC's logic. It is, therefore, up to the ACM to do a parity test and initiate the same alarm as the AGC would in the case of a parity error. This alarm is GOJAM, and is treated separately in Section 2.5.5.2. Bit 13 of CONIN is set.

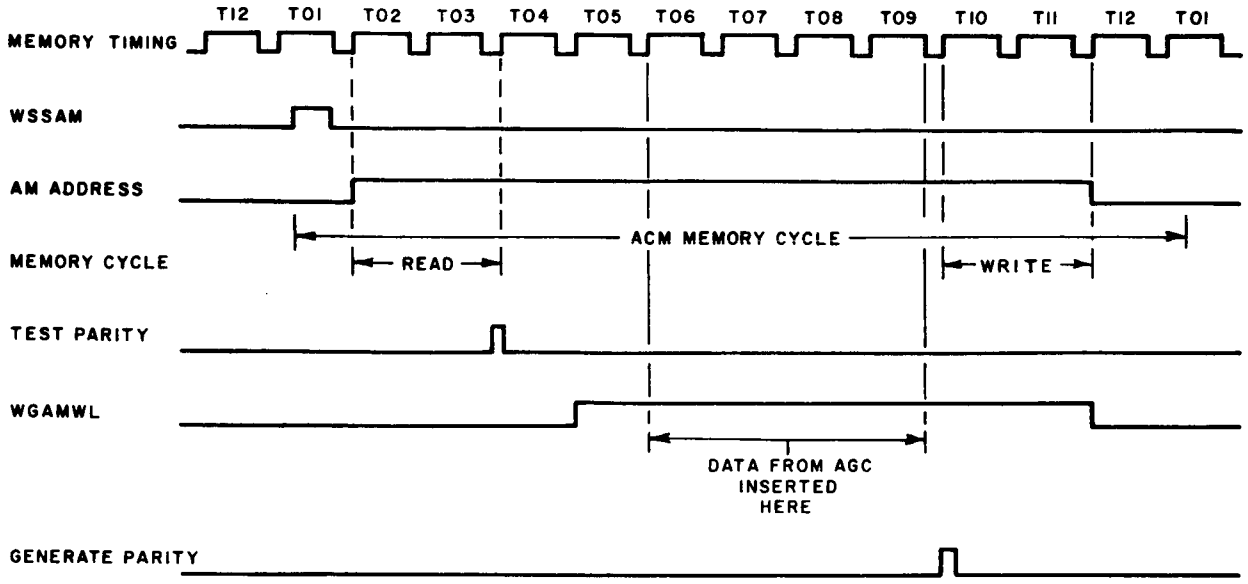


Figure 2-16 ACM/AGC E & F Memory Cycles

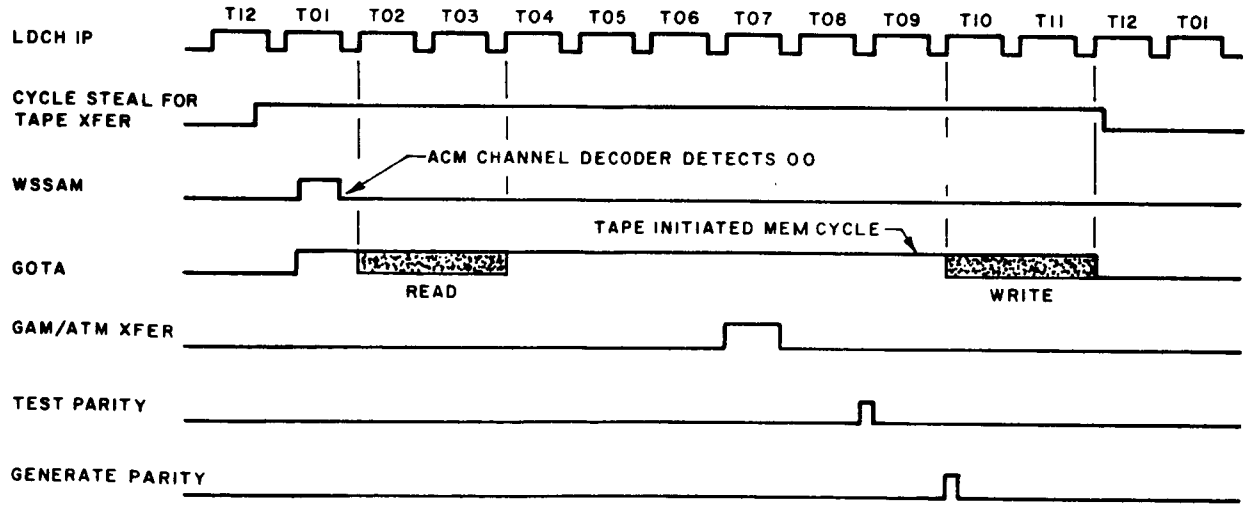


Figure 2-17 TAPE/ACM Memory Cycles

2.5.1.2 ACM to AGC as F-Memory

If the AGC addresses the ACM as F-memory, the ACM does not inhibit the parity test that the AGC normally performs at T08. The AGC F-memory cycle itself is not inhibited during corresponding ACM F-memory cycles; only the strobe is inhibited (via MNHSBF on A52). This forces the ACM to be responsible for setting the parity flip-flop in the AGC (via MONPAR, AMPAR in the ACM), so that if the transmission is successful, the AGC parity test will not fail. The ACM performs its own parity test on the word (in GAM) as received from the ACM memory and initiates a GOJAM in the event of an error (see Section 2.5.5.2). Bit 14 of CONIN is set.

2.5.1.3 ACM to Tape

When the ACM memory is read for tape operations (i.e., Write Tape), the word is stored in GAM and the parity is tested there. In the event of a parity error, bit 12 of CONIN is set and the tape transfer is aborted. GOJAM is not initiated since no AGC operation is affected. The tape abort may be over-ridden with the INH TAPE ABORT switch on the control panel. However, following the parity test, a new correct parity would be generated for the incorrect data word and the tape would store the bad data with good parity, and subsequent retrieval of this data would not detect any errors.

2.5.2 TAPE PARITY FAILURES

2.5.2.1 Group Parity Failures, Triplex

When triplex information is read from the tape, each word on the tape represents one-third (5 bits) of an AGC word. The information is stored triple redundant in groups, each group with its own parity bit. The groups (including parity) are voted and corrected, if necessary (for details, see Section 2.2.3). If correction is necessary, there must have been an error in one or more of the groups. This constitutes a failure, so a bit in the alarm register is set (TRPLX Correction, bit 6 of CONIN). No other action is initiated; this is merely an indicator to the AGC, and a diagnostic tool. On the other hand, if the group parity is still

wrong after correcting, the tape operation is aborted, and bit 9 of CONIN, "Group Parity Error, Triplex" is set. No GOJAM is initiated, since no AGC operation is affected. The AGC software, interrogating CONIN, will discover the error during T3RUPT or T4RUPT.

2.5.2.2 Group Parity Failures, Simplex

In the simplex mode, no voting takes place. The AGC word is still severed into 5-bit groups, but these groups, each with its own parity bit, are stored in the same 18 bit word (no redundancy). When a simplex word is read from the tape, each 6 bit group is tested for parity. If there are no parity errors in any of the 6 bit groups, the AGC parity is generated, and inserted into the ATM register. If a group parity error is detected, however, the tape operation is aborted, and bit 10 of CONIN (Group Parity Error, Simplex) is set. No particular AGC action is initiated, but the AGC software is expected to discover the error during periodic checks on tape activity (T3 or T4RUPT).

2.5.2.3 Tape to ACM Parity Failure

When the Word Processor completes the assembly of a word in the ATM Register and it is transferred to the memory buffer GAM, the parity of the assembled word is tested. This occurs regardless of the mode in which the tape-reading is done. For simplex reading, the three-group parity bits are used to generate the GAM parity bit. Similarly, in the triplex mode, the voted and corrected parity bit from each of the three tape words is used to generate the GAM parity. In the event of a failure, the tape operation in progress is aborted and bit 12 of CONIN (Tape Parity Fail) is set. No GOJAM is initiated since no AGC operation is affected.

2.5.2.4 Summary

To summarize, all cases of parity errors found when reading the tape cause the current tape operation to be aborted. This is done by resetting all the control bits (in CONOUT) which requested the tape operation. The status bit, Transfer-in-Progress, is not reset. The AGC makes periodic checks on the current status of each requested tape operation. It

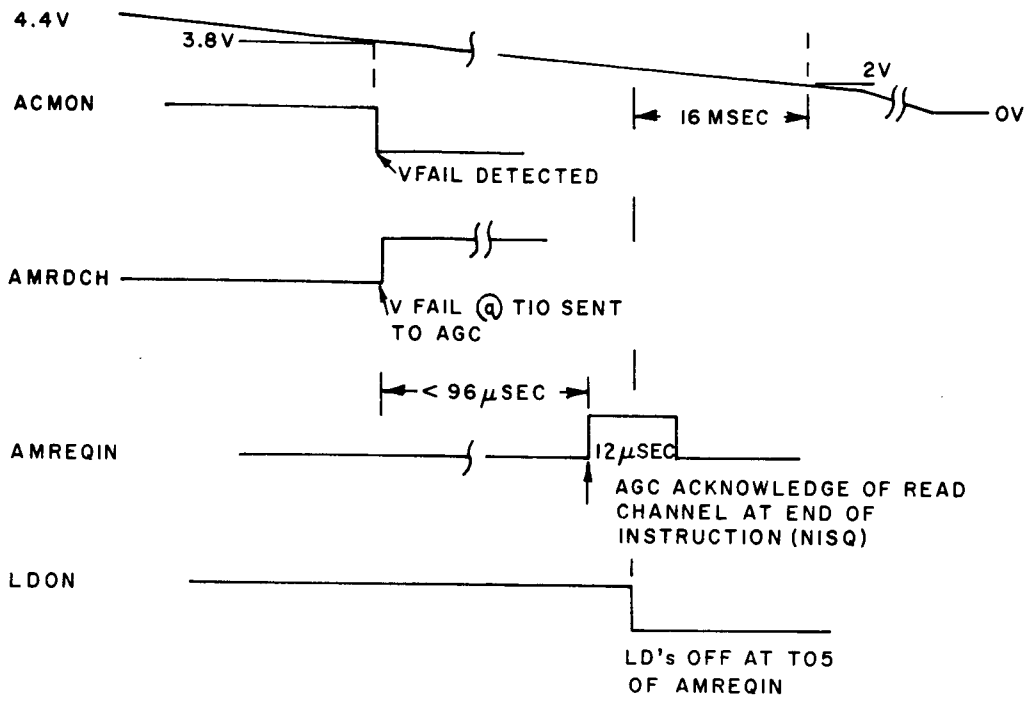


Figure 2-18 ACM Power Shutdown Sequence

operation last requested is in error. An ATM voltage failure which occurs at a time when no tape operation is in progress obviously does not have the same impact.

2.5.4 MISCELLANEOUS FAILURES

There is a class of "failures" which must be defined to take care of abnormal (but not cirtical) situations that can occur during a tape operation. The philosophy here is to make the AGC aware of these hazards so it can take appropriate action to prevent them from becoming serious later on.

One such situation occurs when the ACM is unable to locate the requested ID on the tape. This constitutes an ID Fail and is detected by the third GOREV command during the search sequence. A bit is set in the Alarm register (CONIN, bit 11), and the tape search is aborted.

does this by reading CONOUT and observing the state of only 2 bits: GOATM and Transfer-in-Progress. If GOATM is a "one" regardless of the Transfer-in-Progress bit, there have been no problems. If the Transfer-in-Progress bit is a "one," and GOATM a "zero," the operation underway has been aborted. The reason for the abortion can be found in CONIN. If GOATM and Transfer-in-Progress bits are both reset to "zero," then the tape operation has been completed successfully. This scheme minimizes the AGC housekeeping of a tape request, and its subsequent execution. Any of the tape aborts caused by triplex group parity fail (CONIN 9), simplex group parity fail (CONIN 10), or an AGC assembled word parity fail may be inhibited by the INH TAPE ABORT switch on the control panel.

2.5.3 VOLTAGE FAILURES

2.5.3.1 ACM Voltage Failure

The ACM power supply provides an indication of malfunction or failure in CONIN at bit 4. The indicator monitors loss of +28 volt power to the supply and loss of +4.4 V to the logic. Loss of memory voltage +14 V controlling the memory voltages, +12 V and -5 V and the logic voltage +4.4 V would result in a failure indication in CONIN. The failure detection circuit in the power supply is designed to detect a failure and to sequence a power shut-down that will not disturb the memory current drivers or send erroneous data to the AGC (see Figure 2-18). The read line drivers which provide the interface from the ACM to the AGC are powered separately by LD power so that voltage may be removed from the line drivers before the main logic power goes down.

2.5.3.2 ATM Voltage Failure

When a voltage failure in the ATM occurs, the AGC is so informed by bit 4 in CONOUT. Additionally, if a tape operation was underway (i.e., Transfer-in-Progress was a "one"), it is aborted and bit 8 of CONIN is set. This informs the AGC that the last requested tape operation was aborted because of a voltage failure within the ATM. This distinction is necessary because the AGC must be made aware of the fact that the tape

When a requested record is read from the tape to the ACM core stack, a test is performed to determine that a complete bank (1024 AGC words) has been transferred. If too many transfers (long bank), or too few transfers (short bank), have taken place, the End-of-Bank alarm bit (CONIN, bit 7) is set. The alarm aborts subsequent tape transfers and the AGC interprets the alarm and takes appropriate action.

The number of bits used to describe failures enables the AGC to diagnose and make simple decisions about the state of the ACM (ATM). These decisions fall into two categories: "don't try to use the ATM" or "try again." It is assumed that the AGC's T3 or T4RUPT programs will include a check on the ACM-ATM status and the housekeeping necessary to make such decisions.

2.5.5 FAILURE PROTECTION AND SELF-AMPUTATION

From a long list of possible failures in the ACM, some can be serious enough to warrant self-amputation of the ACM, and others only serious enough to initiate a GOJAM in the AGC. Some of the least significant failures only require informing the AGC, not necessarily by initiating a GOJAM.

The failure protection can be summed up in one sentence: If a failure occurs, the ACM should diagnose the failure, assess its seriousness, and report to the AGC with minimum impact.

Reporting the failure may be done by setting a bit in a channel register in the ACM which the AGC can read at its leisure, or initiating a GOJAM in the AGC. GOJAM must be initiated in those cases when it is known that the AGC either is doing, or will do, some erroneous operation due to a failure within the ACM. The AGC normally initiates its own GOJAM for exactly these reasons. The consequences of not forcing a GOJAM in the AGC depend on the particular program being executed and the particular ACM failure, both of which are, in general, random independent events. This impact can range from no-effect to mayhem.

The possible failures, their idiosyncrasies and impacts on the AGC, are discussed in detail in the following subsections. Table 2-4 summarizes these failures and their influence on the AGC, ACM, and ATM.

2.5.5.1 RL/WL Failure

When a word is sent to the AGC from GAM, the AGC's data busses respond by echoing the transmitted word. This echo can be detected and compared bit by bit with the intended word.

The hardware used to implement this is shown in Figure 2-19. A comparator constantly compares the data on the "return" lines MWLxx from the AGC with the data in GAM. The data is strobed onto the MDTxx lines and into the AGC. A short time thereafter the output of the comparator is strobed. If there is not a bit-for-bit agreement, the test fails.

There are three classes of RL/WL failures, each of which has a different impact.

2.5.5.1.1 Noise

If an RL/WL failure occurs due to noise being injected into the data busses crossing the interface, there is no way to verify whether the noise was picked up on the transmission or on the echo. For some types of transmissions, there is no way for the parity of the word sent to be verified (parity tesiing in the AGC is inhibited during ACM E-memory cycles). It is imperative, therefore, to initiate a GOJAM in this case (see Section 2.5.5.2, GOJAM Initiation).

2.5.5.1.2 Open Wire, Grounded Output, Etc.

If an RL/WL failure occurs due to an open transmission wire to the AGC, or any failure mechanism which would lead to a "zero" on the AGC data busses, this can be treated in the same manner as noise, and a GOJAM can be requested (see Section 2.5.5.2, GOJAM Initiation).

On the other hand, if an echo line is open, or a failure occurs which causes an echo line to be a logical "zero," then any addresses or data which are sent to the ACM are questionable (since data flow to the ACM

TABLE 2-4

ACM FAILURE CHART

Type of Failure (In ACM)	When Tested	Impact on AGC	Impact on ACM	Impact on ATM
1. RL/WL				
a. Normal Data Transfer	GAM to G Transfer	GOJAM	Sets Bits 15 & 1 of CONIN	None
b. Stuck "1"	Every 12 μsec	GOJAM	Amputation. ACM Shuts Itself Off. Line Drivers to AGC are Off when AGC Executes GOJ1.	Turned Off Due to ACM Self-Amputation.
2. Word Parity (From Memory)				
a. As E-Cycle	After Read Half Part of Memory Cycle	GOJAM	Sets Bit 13, CONIN	None
b. As F-Cycle			Sets Bit 14, CONIN	
c. As Tape-Cycle		None 1*	Sets Bit 12, CONIN	Current Tape Op. (Write) Aborted.
3. Voltage Failures				
a. ACM	Constantly Monitored	None 1*	Sets Bit 4, CONIN	Turned Off if Failure is Permanent
b. ATM			If Tape Operation in Progress, Sets Bit 8 of CONIN	Current Tape Operation Aborted.

(Table Continued Next Page)

TABLE 2-4 (Continued)

ACM FAILURE CHART

Type of Failure (In ACM)	When Tested	Impact on AGC	Impact on ACM	Impact on ATM
4. Tape Read Failures (Parity)				
a. Triplex, Group, Corrected	Every Tape Read, Trplx	None 1*	Sets Bit 6, CONIN	None
b. Triplex, Group, Uncorrectable				
(i) During Bank Transfer	Every Tape Read, Trplx	None 1*	Sets Bit 9, CONIN	Current Tape Operation Aborted
(ii) During Bank Transfer or ID Word Read	Every Tape Read, Trplx	None 1*	Sets Bit 5, CONIN	Current Tape Operation Aborted
c. Smplx, Group	Every Tape Read, Simplex	None 1*	Sets Bit 10, CONIN	Current Tape Operation Aborted
d. Assembled Word Parity Errors	During Tape Read Operation Prior to Memory Cycle	None 1*	Sets Bit 12, CONIN (See also 2(c))	Current Tape Operation Aborted

(Table Continued Next Page)

TABLE 2-4 (Continued)

ACM FAILURE CHART

Type of Failure (In ACM)	When Tested	Impact on AGC	Impact on ACM	Impact on ATM
5. Miscellaneous				
a. ID Fail	ID Sought is not Found. Fail ≙ 2 Pair Reversals in Search Mode	None 1*	Sets Bit 11, CONIN	Current Tape Operation Aborted
b. Bankfail	At End of Bank Read from Tape. Fail ≙ # Words Read From Tape ≠ 1024	None 1*	Sets Bit 7, CONIN	None - This Test is Done at End of Tape Read

Note: 1* No primary impact on AGC but AGC is expected to monitor CONIN during T3, T4RUPT (or other loop) and make decisions based on available information.

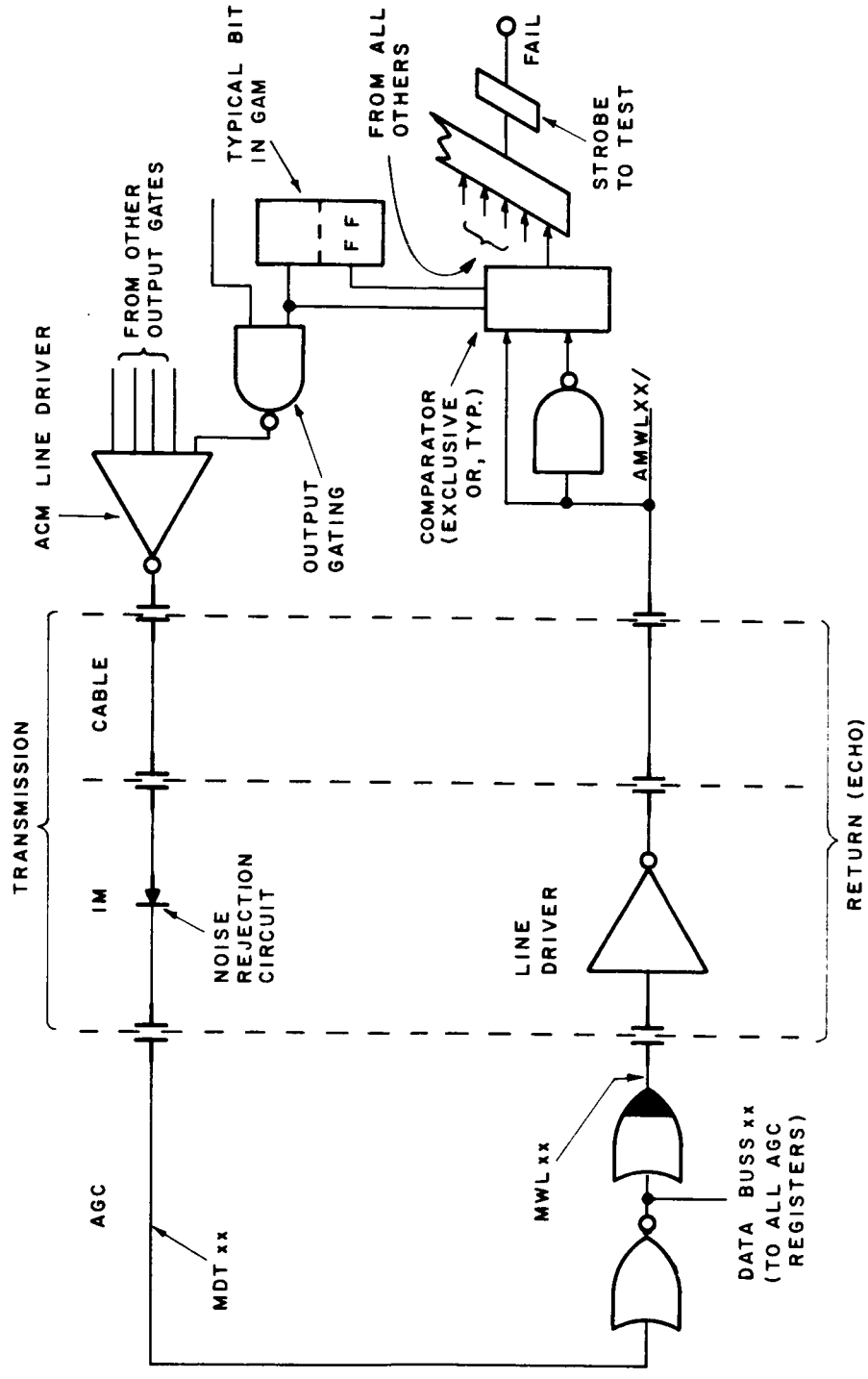


Figure 2-19 RL/WL Failure Detection

is via the echo lines). If the ACM data transmitted (in response to an address from which a "one" has been dropped) does not have a "one" in the bit position corresponding to the open (or grounded) echo line, then the RL/WL comparator does not fail, and no GOJAM is initiated. The ACM has supplied correct data from the wrong address. The AGC will proceed to compute using erroneous data or a bad instruction which is "good," i.e., no bits are missing, parity is OK, etc. This is a uniquely undesirable position in which to leave the computer. It could execute an indefinite number of cycles anywhere in the program (ACM memory, AGC F or E-memory) with unpredictable results.

Although not implemented in the engineering model, the following technique can be implemented to avoid this situation by taking advantage of the periods of AGC data buss inactivity and constantly verifying the integrity of the transmission-return echo loop. If a "one" is sent to the AGC on every data buss (MDTxx) during a normally inactive period, and if all "ones" are received from the echo line (MWLxx's) during that period, then there are no open or grounded lines in either direction. This can be done at any time in which there are no interferring AGC actions.

It would be desirable to perform this test during every AGC memory cycle. Since the AGC executes some instructions which have no periods of inactivity (e.g., DIVIDE), a reasonable compromise must be made. The sub-instruction STD2 (the "fetch" part of most instructions) occurs approximately 30% of the time and contains two large periods of inactivity: T03 through T05 and T09 through T11. The choice of which period to use for the test is arbitrary.

The implementation is shown in Figure 2-20. At T04, the MDTxx lines are impressed with "ones," and the test is made during the latter part of T04 (STROBE). A failure implies that at worst a line has become open or grounded, and the computer is made to GOJAM.

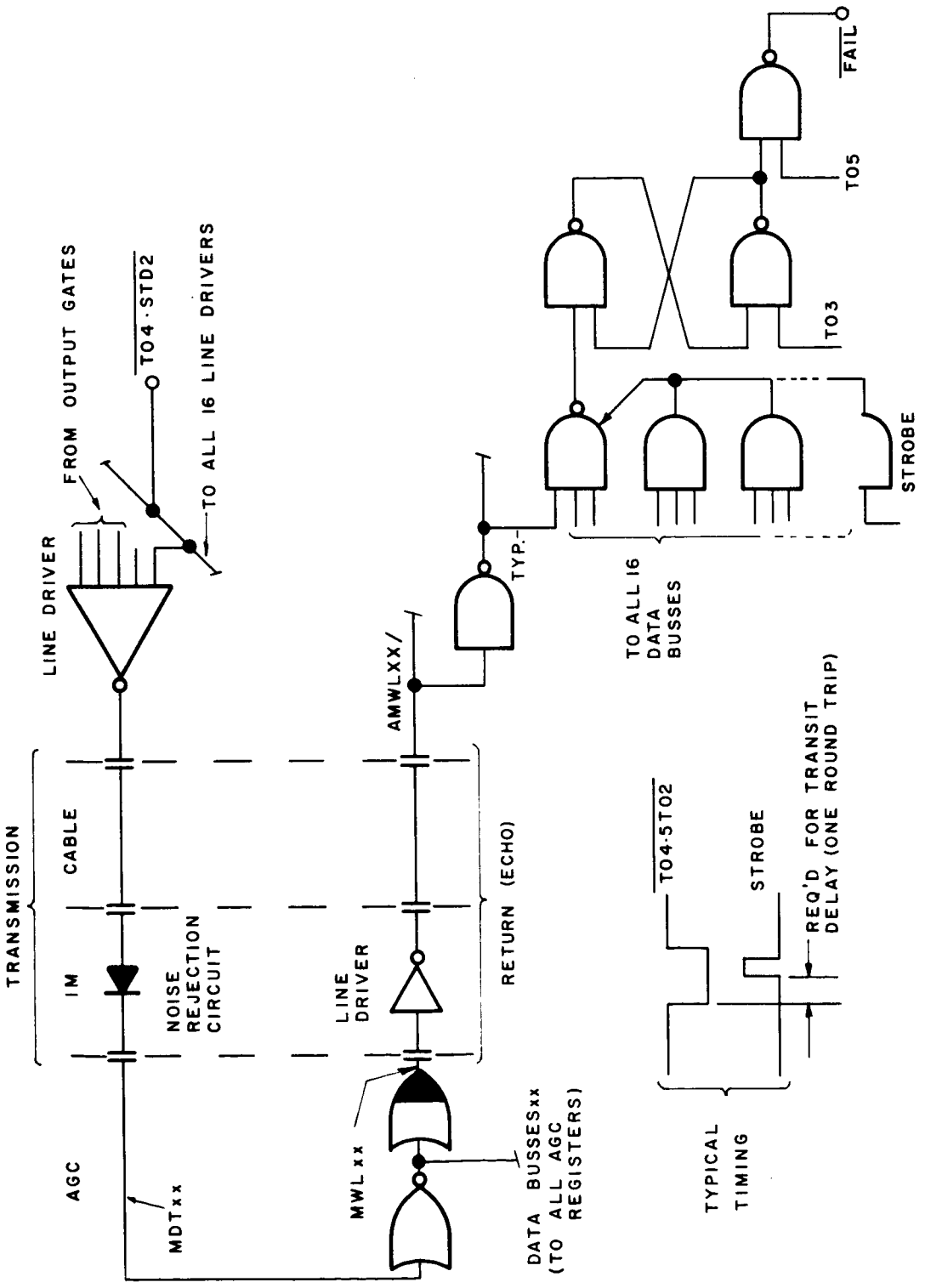


Figure 2-20 RL/WL "Ones" Test (Not Implemented in Engineering Model)

2.5.5.1.3 High Output, Constant "One"

If any transmission data line ever gets "stuck" at a "one" level, the AGC is incapable of performing even the most basic instructions. This "one" will eventually get into a given bit position of every register in the AGC. If any counter INKL's are executed, an unexpected bit in the requested E memory counter could be set[1]. It is imperative, therefore, to immediately initiate a GOJAM and amputate the ACM from the AGC. Since only the ACM can possess this failure knowledge and make use of it, it must initiate its own self-amputate routine. While executing this sequence, the ACM must guarantee that the AGC not perform any instructions because they would be invalid. Incapacitating the AGC during the self-amputate sequence (80 to 240 μs interval), preserves the integrity of the E memory and, in particular, the counters (Gyro, RCS, etc.).

The consequences of not executing a self-amputate are obvious; even the re-start routine following GOJAM could not be executed properly.

Fortunately, this is an easy condition to detect. During periods of data buss activity, there are 250 ns (nominal) of "dead" time between information pulses. If there are ever periods of time in which this dead time is missing, it can be assumed that either the AGC is not functioning properly, or the ACM is holding a particular line at a "one" constantly.

To detect this, the scheme shown in Figure 2-21 is implemented. A flip-flop, which is tested at T11 and reset at T01, looks for all zeros on the MWLxx lines. If there ever occurs an AGC cycle in which at least one MWLxx does not contain any zeros (thereby indicating a stuck "one" line), the flip-flop will not be set and the test at T11 will indicate a failure. This failure indication is used to initiate the required ACM self-amputation. Since the previous memory cycle contained questionable data, a GOJAM must be initiated.

The self-amputation routine and the GOJAM request are intimately linked and are discussed in Section 2.5.5.3.

[1]This would require coincidence of the "stuck one" line and an address bit of the counter requested.

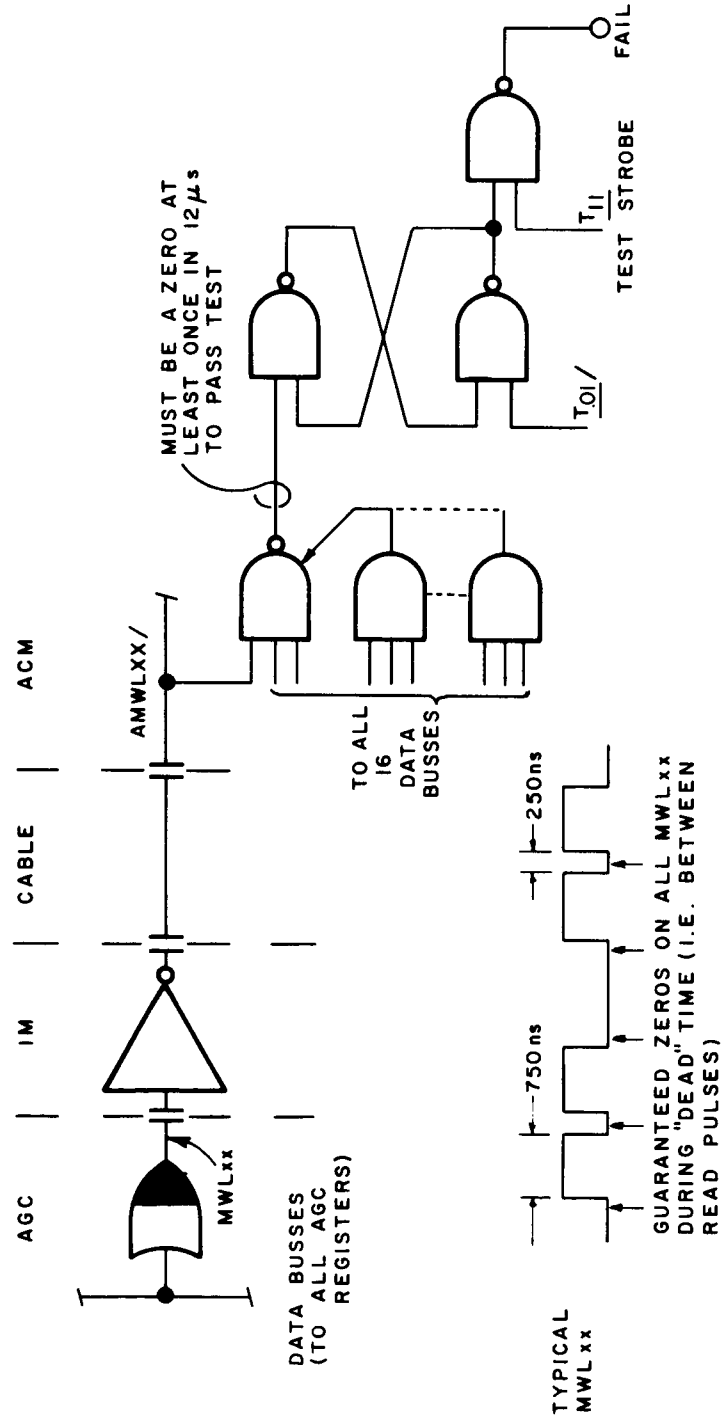


Figure 2-21 WL Stuck Test

2.5.5.2 GOJAM Initiation

There are several reasons for which the ACM must initiate a GOJAM in the AGC. These reasons have been outlined previously and no elaboration is necessary here. Assume that the task is simply to (a) initiate a GOJAM at the earliest possible time, and (b) if not immediately, then incapacitate the AGC for the waiting period.

The test connector signals are such that a GOJAM cannot be initiated immediately. The AGC has, as part of its test connector logic, a circuit which interrogates the MSTRT line every 160 μs. A GOJAM will be generated if this line is held at a "one" for more than 80 μs. This logic eliminates noise-generated GOJAM. The intent was that this signal come from a pushbutton (or flip-flop) in the GSE.

When the ACM requests a GOJAM, it is required to hold this line up until the GOJAM takes place. In the interim, several cycles of some possibly unknown program can be executed; this is an obvious hazard which must be avoided. In order to null these cycles, the ACM must force a nonsense cycle to be executed while waiting for the GOJAM to take place.

Five different kinds of cycles can be forced from the test connector. The READ-CHANNEL instruction (INOTRD initiated by MRDCH on A52) has the most desirable characteristics for use in incapacitating the AGC during the GOJAM waiting period; it does not refer to E or F memory, contains no WCH (Write Channel) control pulses, and is a one-cycle (12 μs) operation. It is important to choose an instruction which does not refer to core memory (AGC or ACM). If a data line is a constant "one," this could alter the contents of a location, depending on which particular line failed. Also, if there were any WCH control pulses, the contents of a channel could be altered in a similar manner.

To summarize, when the ACM initiates a GOJAM, the MSTRT and MRDCH inputs on the test connector are held at a "one" until MGOJAM is received by the ACM. MGOJAM is the AGC's acknowledgement that the GOJAM requested is in effect.

2.5.5.3 Self-Amputation Sequence

The shut-off sequence is implemented in a special manner (see Figure 2-22). The power to the line drivers for all outgoing lines except MSTRT and MRDCH is turned off immediately. Upon the receipt of MGOJAM, the MSTRT and MRDCH lines are reset and the power to the remaining circuits is shut off. This takes considerably longer (450 ms), and the computer will be able to proceed unhampered by any ACM failures upon the termination of MSTRT and MRDCH. At worst, power-down initiated transients on the MSTRT line could generate another GOJAM, or transients on the MRDCH line could generate a nonsense cycle, neither of which is critical at this juncture.

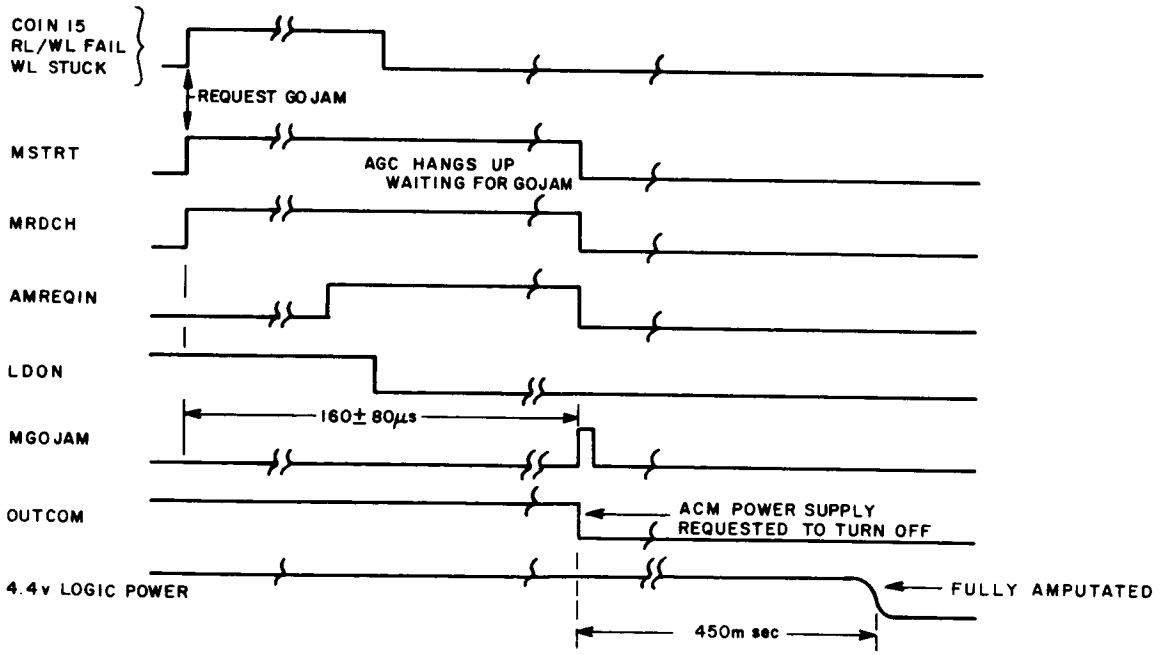


Figure 2-22 Amputate Sequence

SECTION 3

SOFTWARE CONTROL OF AUXILIARY MEMORY

3.1 ACM CONTROL

ACM power and addressing are controlled by the software. Causes of failures in the ACM are also determined by software.

3.1.1 POWER CONTROL

The TURN-ON/TURN-OFF of the ACM is accomplished by using AGC Channels. In order to turn the ACM on, OUTCOM (bit 9 of Channel 11) must be set. CONOUT should be interrogated after setting OUTCOM. Bits 14 and 4 of CONOUT should be on approximately 8 msec after setting OUTCOM. It should be noted that other bits in CONOUT may also be on at this time, indicating the status of unrelated conditions. Upon interrogating CONIN, only bit 4 should now be on; this bit, ACM VFAIL, indicates that the ACM was off initially. The TURN-OFF procedure is to clear OUTCOM and interrogate CONOUT one second later, at which time bits 15-7 should all be zeros. A spurious ACM VFAIL indication will also be displayed in bit 4 of CONIN; this should be ignored.

3.1.2 ADDRESSING

The ACM Memory may be addressed as fixed or as erasable. As fixed, the ACM banks are treated the same as AGC Super Banks. All banks may also be addressed as erasable; however, some of these banks are addressable as erasable only under GSE Control.

There is an addressing overlap between the AGC and the ACM when addressing locations in an E bank number ending in zero. Addresses 1400-1407 will refer to Special and Central Registers, as well as to ACM E Memory locations. All addressing of these locations should be avoided (with the exception of using a TS instruction to load location 1400). The use of the TS instruction is necessary to load location 1400 with the ID word, as is pointed out in Section 3.2.9. All addressing details, bank numbers, etc., are shown in Table 2-3.

3.1.3 FAILURE EFFECTS

Three types of ACM failures will have an impact upon both the AGC and ACM. These failures are:

a. Read Line/Write Line Failure;
b. F Parity Error;
c. E Parity Error.

These failures in the ACM cause the setting of bits 15, 14, and 13 in CONOUT, respectively. If the Read Line/Write Line failure was due to a stuck "1", self-amputation of the ACM results. All of these failures cause an AGC GOJAM, and the GOJAM causes OUTCOM to be cleared; therefore, the software must process the GOJAM, and either allow the ACM to turn off, or keep the ACM on by setting OUTCOM. The GOJAM is processed as shown in Figure 3-1.

It should be noted that any AGC GOJAM also causes OUTCOM to be cleared, and that if the ACM is to remain on, OUTCOM should be set before the time delay has allowed the ACM to turn off (see Section 2.5.5).

3.2 ATM CONTROL

ATM power and tape operations are controlled by the software. Causes of tape errors are determined by the software. Also, all file organization and "housekeeping" are managed by the software.

3.2.1 POWER CONTROL

In order to turn the ATM on, the ACM must be ON. To turn the ATM from OFF to STANDBY, set bit 15 of CONOUT. CONOUT should be interrogated 100 msec later, and at this time, bits 15 and 14 should be on, indicating that the ATM is in the STANDBY mode. In order to turn the ATM from OFF or STANDBY to ON, set bits 15 and 13 of CONOUT. Upon interrogating CONOUT 500 msec after the command, bits 15, 14, 13, and 12 should be on, indicating that the ATM is ON.

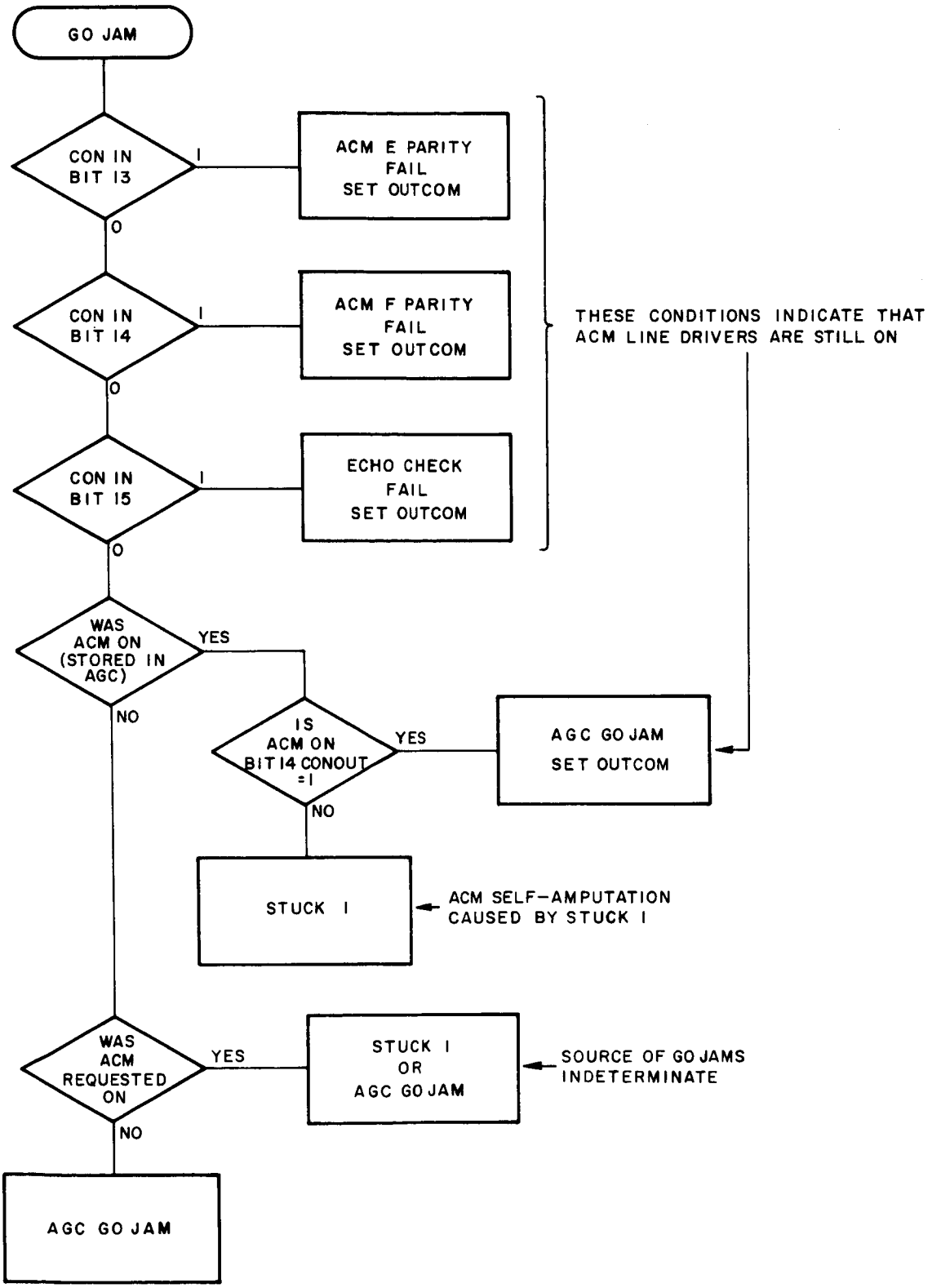


Figure 3-1 Software Logic for GOJAM Processing

The TURN-OFF procedure is as follows:

a. To turn the ATM from ON to STANDBY, bit 12 of CONOUT should be set and CONOUT should be interrogated 200 μsec later, at which time bits 15 and 14 should be on and bits 13 and 12 off, indicating that the ATM is in STANDBY mode;

b. To turn the ATM from STANDBY or ON to OFF, bits 14 and 12 of CONOUT should be set and 50 msec later, bits 14 and 4 of CONOUT should be on, indicating ATM OFF and ACM ON. Since the ACM must be on to control the ATM, OUTCOM must be maintained. See Figure 3-2 for power control sequence.

3.2.2 TAPE FORMAT AND FILE SIZE

The tape format is shown in Figure 3-3; the Program File Markers and Data File Markers are as indicated. ID word structure is shown in Figure 3-4. The tape format is prepared as discussed in Appendix A. Since the File Markers are placed twenty-five (25) seconds apart, they allow 80K words within each file. In order to insure that the end of

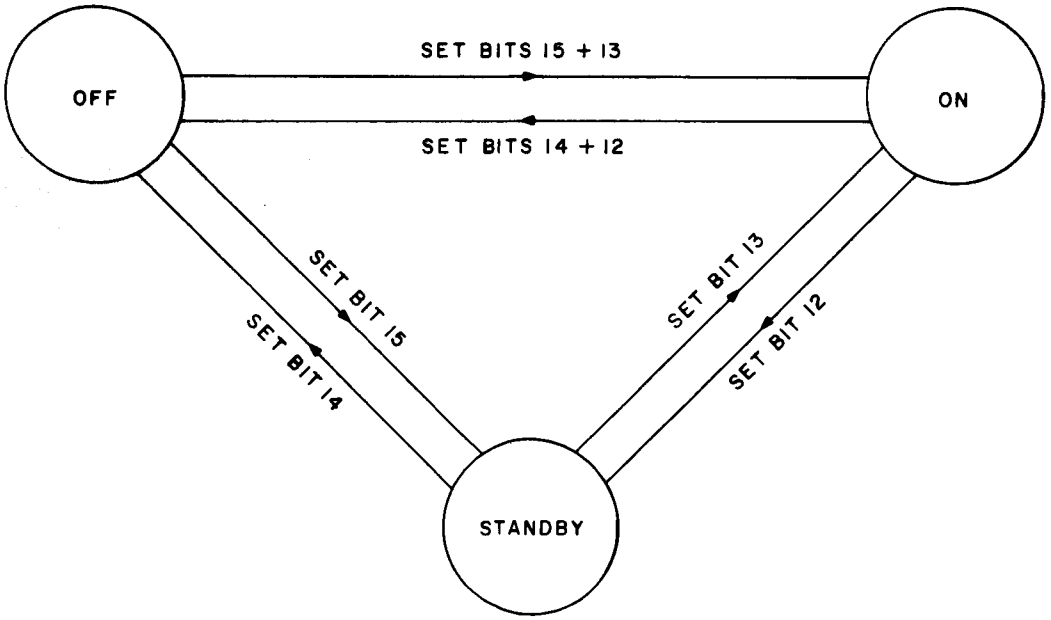


Figure 3-2 ATM Power Control Sequence

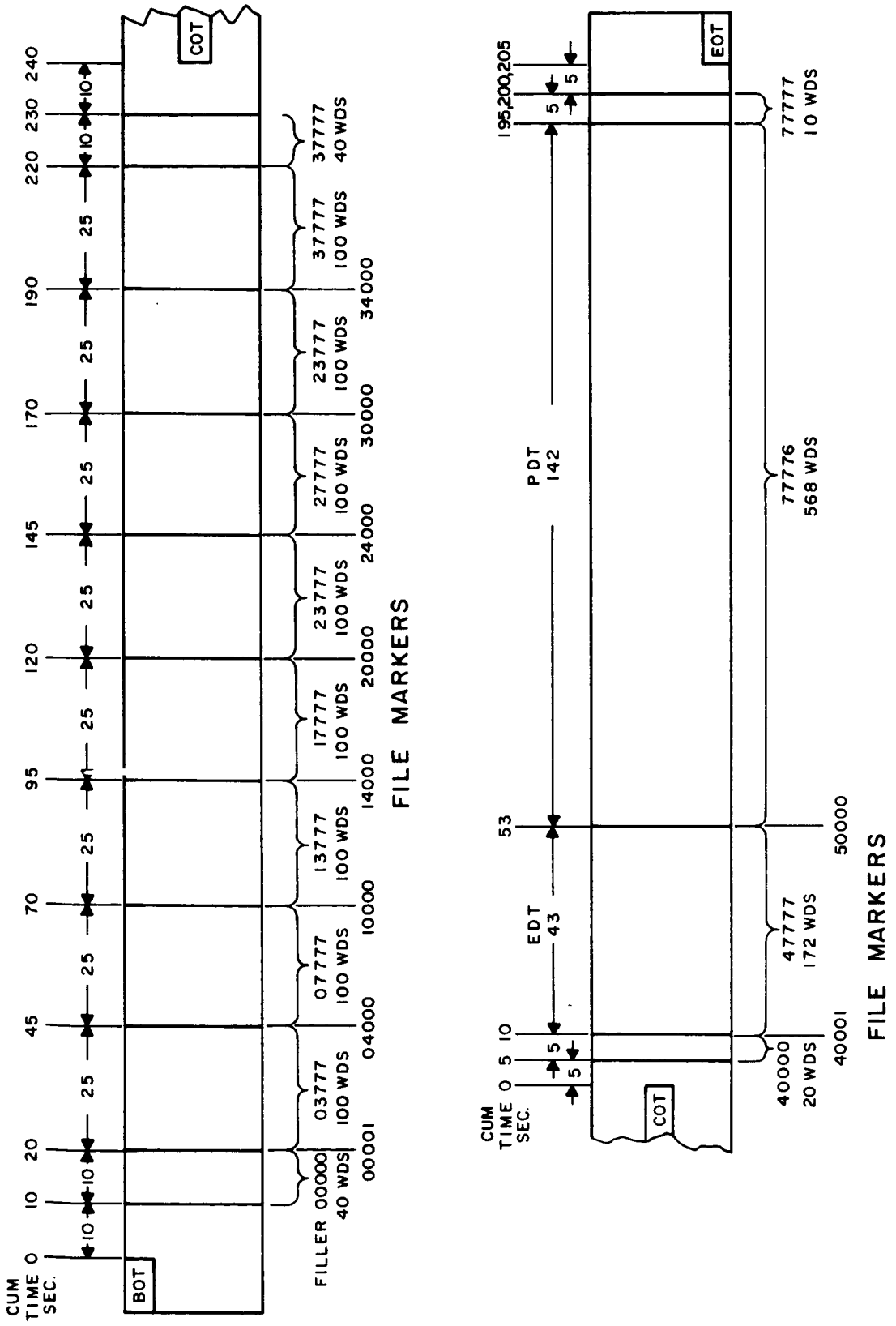


Figure 3-3 Tape Format

the data tape has not been reached, IDREAD should be checked after every write tape operation for 77777, indicating the end of the tape, or for 50000, indicating the end of erasable data tape.

3.2.3 MU ADDRESSING

The primary MU location is MU5. The data portion of tape can only communicate (read or write) with MU 5. The program portion of tape may be transferred to any MU, but the program portion of tape can be loaded only from MU 5 under GSE Control as described in Appendix C, even though the records may be destined for another MU on retrieval.

3.2.4 SIMPLEX/TRIPLEX

When reading a record on the Data portion of tape, bit 3 of IDREAD determines whether it is decoded as simplex or triplex. See Figure 3-4. When writing, bit 9 of CONOUT determines whether the record will be transferred to the tape as simplex or triplex. It is therefore possible to write a bank whose ID (bit 3) does not agree with the mode in which it is actually written, thus producing a non-retrievable record. It is the software's responsibility to prevent this.

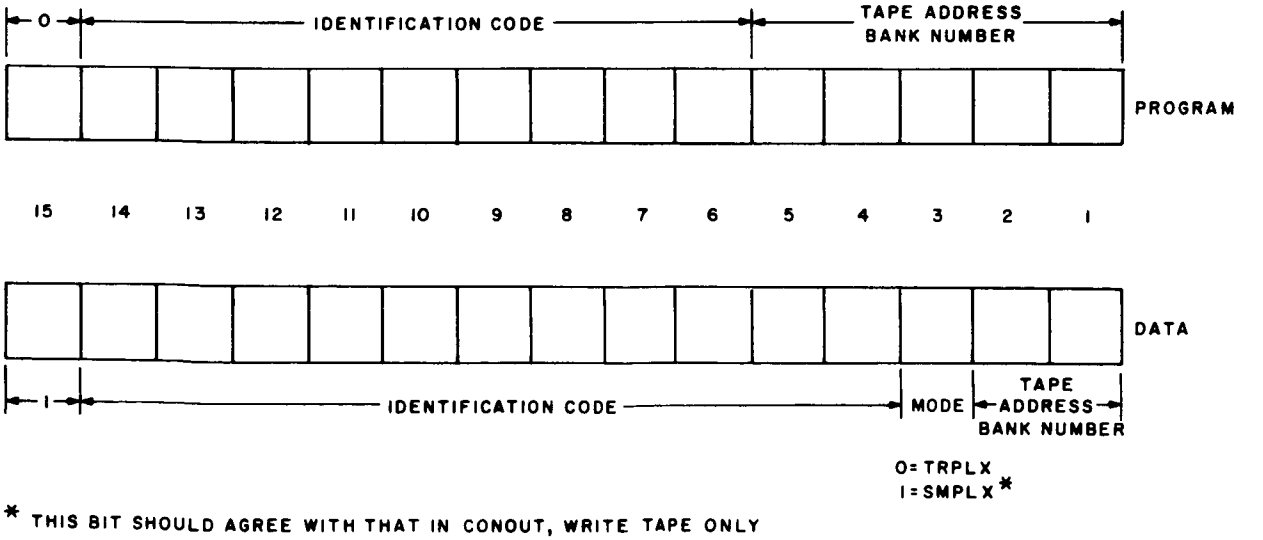


Figure 3-4 AGC/AM ID Word Structure

3.2.5 TRANSFER PROGRAM FROM TAPE TO ACM MEMORY

In order to transfer from the program portion of tape to ACM Memory, IDSTART must be loaded first. IDSTART is loaded with the ID of the first bank to be transferred from tape. IDSTOP is cleared to zeros by hardware when IDSTART is loaded; the condition and all zeros in IDSTOP are interpreted as a single bank transfer. Therefore, no further action is required for a single bank transfer. However, if the transfer is multibank, the last 5 bits (bits 1-5) of IDSTOP must be loaded with the last 5 bits of IDSTART incremented by the number of banks to be transferred. A program multibank read tape operation may start with any bank in any MU and will cycle to the next consecutive banks as requested. A transfer will not cycle to the beginning of MU 2 when it reaches the end of MU 5, but will attempt to load nonexistent MU 6. Therefore, the software should check IDSTOP so that the transfer will not extend beyond the last bank of MU 5: $11 \leq c\ (\text{IDSTOP}) \leq 30$.

IDSTART and IDSTOP should be verified to see that they are properly loaded. CONOUT should be verified as having bits 15-12 on, and CONIN should be verified as having all zeros. If CONIN is not zeros at this time, it should be cleared to zeros. CONIN is cleared for failure interrogation purposes.

In order to execute the tape read operation, GOATM must be set. The AGC may discontinue its request for a transfer at any time prior to the appearance of TRNSIP by clearing GOATM. A transfer is in progress when TRNSIP appears. The transfer is complete when TRNSIP and GOATM are both removed by the ACM.

Various error actions are possible during the transfer. If the transfer is aborted by the ACM, TRNSIP will remain set and GOATM will be cleared. At this time, AGC interrogation of CONIN will establish the cause of the tape abort. After determining the cause of the tape operation abort, the software may elect to repeat the operation or post the proper alarm to the DSKY.

3.2.6 TRANSFER DATA FROM TAPE TO ACM MEMORY

The procedure for transferring a data record from ATM to ACM is the same as that for program (Section 3.2.5) with the following exceptions. Since the data tape can communicate only with MU 5 (as described in Section 3.2.3), data multibank transfers may start with any bank in MU 5, and will cycle back through the beginning of MU 5 depending upon the number of banks to be transferred. When loading IDSTOP, this fact must be taken into account. All other procedures are the same as those for program tape.

3.2.7 TRANSFER DATA FROM ACM MEMORY TO TAPE

In order to transfer data from the ACM Memory to the ATM Data Tape, IDSTART must be loaded with the tape ID (or file marker) presently on the tape, after which the record is to be written. The last four (4) bits (4-1) of IDSTOP are loaded with the following:

a. In bit positions 4 and 3, the tape address of the first Data Bank to be transferred;

b. In bit positions 2 and 1, the tape address of the first transferred bank plus the number of banks to be transferred (two low order bits only). The remark of the preceding paragraph relative to cycling back through MU 5 applies to writing also.

IDSTART, IDSTOP, CONOUT, and CONIN should be verified as in Section 3.2.5. "Housekeeping" of ID words must be performed by the software as described in Section 3.2.9. The cautionary note in Section 3.2.4 should also be observed.

In order to execute the transfer, bits 11, 10, and 9 must be set in CONOUT for the simplex mode or bits 11 and 10 for the triplex mode. The transfer may be halted by the AGC at any time prior to the appearance of TRNSIP by clearing GOATM. Transfer is in progress when TRNSIP appears, and the transfer is complete when TRNSIP and GOATM are removed by the ACM.

Upon completion of the transfer, IDREAD should be checked as indicated in Section 3.2.2. Various error actions are possible during the transfer. These errors may be determined in the same manner as in Section 3.2.5.

3.2.8 TRANSFER PROGRAM FROM ACM MEMORY TO TAPE

The program portion of tape is not normally written on. Because of this, software should reject requests for writing on this portion. However, the program portion of tape may be written on using the same procedure as that for Data Tape, except for the following modifications. Software checks for bit 15 of the ID word and for agreement of bit 3 (the mode bit for data ID's), with bit 9 of CONOUT must be bypassed. GSE control must be used as described in Appendix C. A multibank transfer may start with any bank in MU 5, but will not cycle back to the beginning of MU 5; therefore, IDSTOP should not allow a transfer to exceed the last bank of MU 5. All other operations in the procedure are the same as those for Data Tape, Section 3.2.7.

3.2.9 ID WORDS

The ID's on the tape are required to be in ascending, but not necessarily consecutive sequence. However, all ID's used in multibank reads must be consecutive. See Section 3.2.11 about failures that can occur due to non-consecutive ID's. It is the responsibility of the software to have the ID of a bank loaded in the first location of the bank to be written (the hardware treats the first word as the ID of the bank). This is described in Section 2.4.5. Shown in Table 3-1 is a partial list of the Program ID's. The ID is required to have a zero in at least one of the following bit positions - bits 5, 4, or 3. The choice of Tape Address assignments provides for this zero bit in Program ID's; but, with Data ID's, the position of the zero is arbitrary. Requiring the zero bit avoids the paradox of a multibank transfer having IDSTOP bits 5-1 all zeros which would imply a single bank transfer. For example, if the last 5 bits of the ID were 11101 and a 3-bank transfer was requested, IDSTOP would be 00000, implying a single bank transfer,

TABLE 3-1

PROGRAM ID NUMBERS

MU 5

FILE MARKER	00001	04000	10000	14000	20000	24000	30000	34000
	24	4024	10024	14024	20024	24024	30024	34024
	25	4025	5	5	5	5	5	5
	26	4026	6	6	6	6	6	6
	27	4027	7	7	7	7	7	7
	64	4064	10064	14064				
	65	4065	5	5				
	66	6	6	6				
	67	7	7	7				
	124	4124	10124					
	125	5	5					
	126	6	6					
	127	7	7					
	164	4164						
	165	5						
	166	6						
	167	7						
	224	4224						
	225	5						
	226	6						
	227	7						
	264	4264						
	↓	↓	↓	↓	↓	↓	↓	↓
	03767	07767	13767	17767	23767	27767	33767	37767

MU 4

FILE MARKER	00001	04000	10000	14000	20000	24000	30000	34000
	20	4020	10020	14020	20020	24020	30020	34020
	21	2021	1	1	1	1	1	1
	22	4022	2	2	2	2	2	2
	23	4023	3	3	3	3	3	3
	60	4060	10060	14060				
	61	4061	1	1				
	62	4062	2	2				
	63	4063	3	3				
	120	4120	10120					
	121	1	1					
	122	2	2					
	123	3	3					
	160	4160						
	161	1						
	162	2						
	163	3						
	220	4220						
	221	1						
	222	2						
	223	3						
	260	4260						
	↓	↓	↓	↓	↓	↓	↓	↓
	03760	07760	13760	20760	23760	30760	33760	37760

not a 3-bank transfer. The ID determines the bank to which the record will be transferred during a tape read operation. The relationship between ID words and bank numbers is shown in Table 2-3.

3.2.10 POSITION TAPE

A Position Tape feature is provided in ATM control. This feature allows the tape to be positioned at any File Marker or ID; however, consecutive Position Tapes on the same ID or File Marker are not allowed because the tape will position to the next ID or File Marker each time.

To position the tape, IDSTART must be loaded with the ID or File Marker which corresponds to the desired position. IDSTART, CONOUT, and CONIN should be verified as in Section 3.2.5. To execute the Position Tape operation, bits 11 and 7 of CONOUT must be set. The Position Tape operation may be halted by the AGC at any time by resetting GOATM. The operation is complete when GOATM is removed by the ACM.

3.2.11 TAPE ERRORS

If an error is detected as a result of GOATM being cleared by the ACM and TRNSIP remaining set, the tape operation will have been aborted and the proper bit will have been set in CONIN (a bit between 12 and 7). Bits 6-4 in CONIN are used for additional information and do not indicate errors that cause tape aborts. Bit 6 denotes that a triplex correction took place, bit 5 signifies that a triplex group parity error occurred, and bit 4 indicates that the ACM has lost power since the last time CONIN was cleared.

Time checks should be performed by the software during a tape transfer. No search operation should take over seven (7) minutes. Seven minutes should be considered the maximum access time. After the appearance of TRNSIP, no transfer should last longer than four (4) seconds, unless gaps of extraordinary length are employed. This condition is possible if a multibank read on non-consecutive ID's (see Section 3.2.9) is attempted. After locating the initial record, the remaining records involved in the transfer must be consecutive. The hardware will not

revert to the search sequence if c(IDREAD) $\neq$ c(IDSTART), but will continue to scan the tape in the forward direction until EOT is reached (unless a time limit is imposed by software). If either of the preceding errors occurs, an alarm should be posted to the DSKY.

SECTION 4

DEMONSTRATION TESTS

4.1 TEST OBJECTIVES

The Test Plan outlines many objectives of the Demonstration Tests. These objectives are met by demonstrating the operation modes of the system.

4.1.1 POWER CONTROL

Acm Power Control - Program Control of the ON and OFF modes of the ACM.

ATM Power Control - Program Control of the ON, STANDBY, and OFF modes of the ATM.

4.1.2 PROGRAM OPERATIONS

ACM Program Load - Program loads from tape to both MU's. Verification of error detection/correction.

AGC Program Execution - Execution of a program out of AGC, F, and E Memory.

ACM Program Execution - Execution of a program out of the ACM using the AGC's E Memory.

4.1.3 DATA OPERATIONS

ACM Data Storage - The AGC transfer of information to the E Memory of the ACM.

ACM Data Load - Data loads from tape to MU 5.

ATM Data Load - Data transfers from MU 5 to tape.

ATM Data Verify - Verification of ACM loaded data against fixed memory loaded data.

ATM Data Reload - The "Write Over" feature of the Data Tape used to reload the tape.

4.2 TEST CONFIGURATION

The Demonstration Test Configuration consists of a PAC/AGC/DSKY combination along with the ACM/ATM equipment including the Control Panel.

The executive program is loaded via the PAC and is stored in the PAC. The PAC Memory is simply used to replace the AGC ropes. All displays such as success or failure, etc., are displayed on the DSKY (see Appendix G). The Test Configuration is shown in Figure 4-1.

4.3 DESCRIPTION OF TESTS

The ACM/ATM programs are called up from the DSKY using verb codes. The verb is selected by hitting the Verb key followed by the two digit number of the verb desired. Then the Enter key is hit upon completion of this procedure, and the supervisor transfers control to the verb sub-program selected. Each test consists of more than one task. This method of operation more closely approximates the condition under which the ACM/ATM would be used during actual flights. The Demonstration Test may be divided into four (4) sections - those tests demonstrating Power Control, Program Tape Operations, Data Tape Operations, and ACM - AGC Restart Relations. In addition to these Demonstration Tests, a Utility Verb (VERB 00) is also provided in order to check the Hardware operation. The Utility Verb is described in Appendix F.

4.3.1 POWER CONTROL TESTS

The ACM Power Control and the ATM Power Control modes are demonstrated with Verbs 01-05. In addition to Power Control, the execution of a program out of the AGC is also demonstrated, since the executive program is stored in PAC. A controlled TURN-ON and OFF is used to prevent contamination of AGC inputs.

VERB 01	Turns On ATM and ACM
VERB 02	Turns On ACM only
VERB 03	Turns ATM and ACM Off
VERB 04	Turns ATM Off
VERB 05	Turns ATM from On to Standby

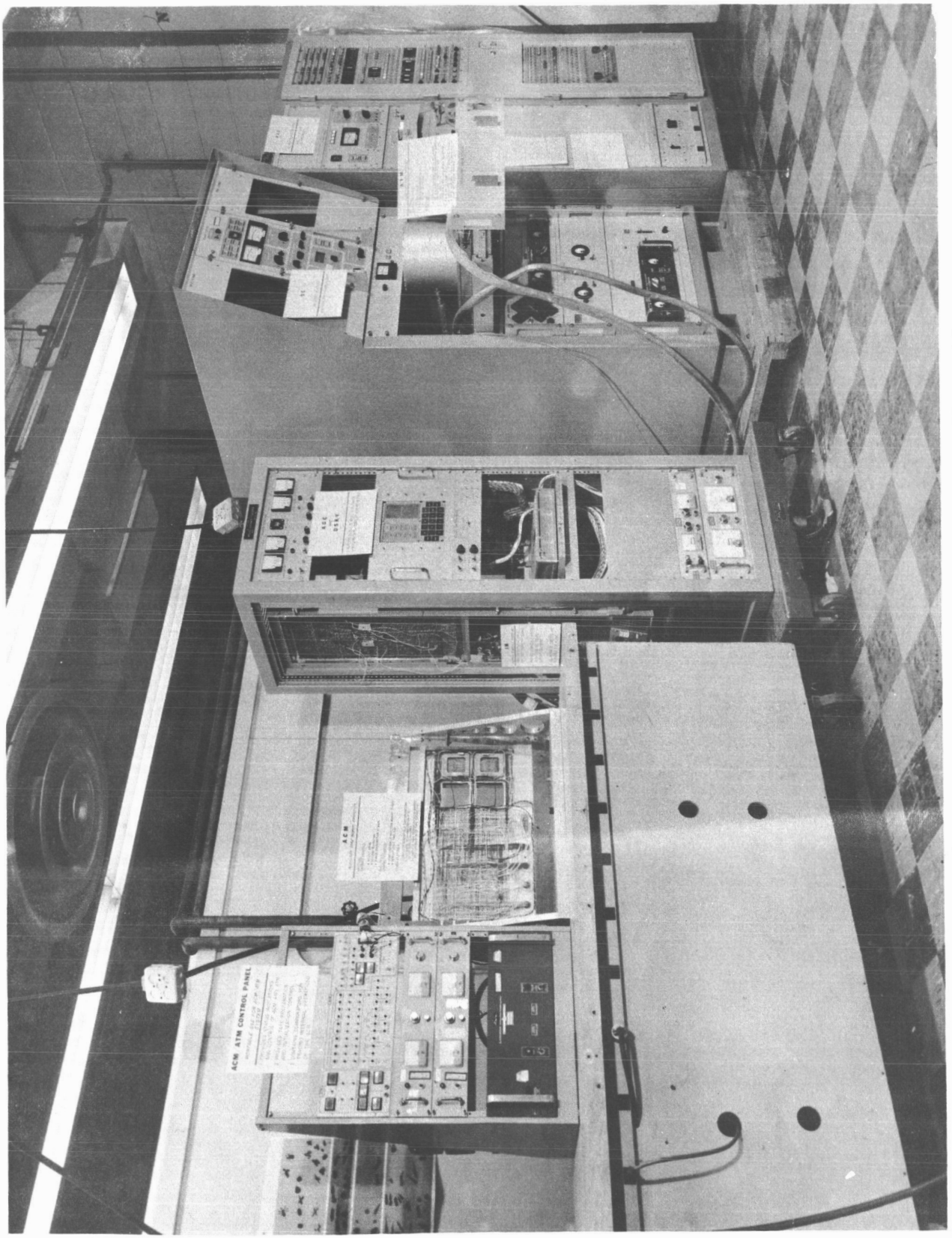


Figure 4-1 Demonstration Test Configuration

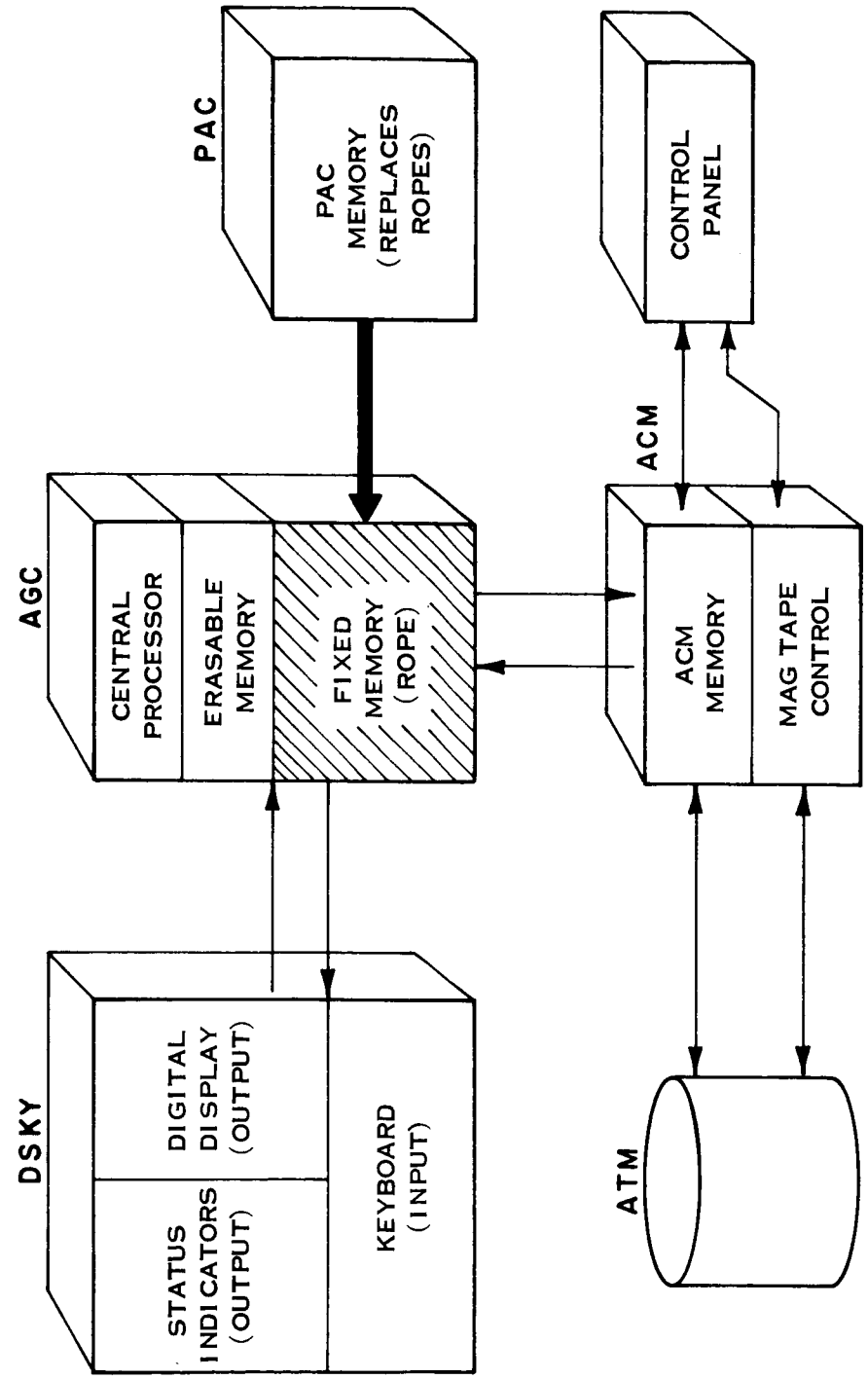


Figure 4-2 Test Configuration

4.3.2 PROGRAM TAPE TESTS

The ACM Program Load and Program Execution modes are demonstrated with Verbs 06-13 and 21. These verbs perform program loads from tape to both MU's, verification of error detection, and execution of a program out of the ACM using the AGC's E Memory. These verbs also execute a program out of the AGC (the Executive).

VERB 06 — Retrieves the DSKY Exerciser Program from tape and executes it from ACM memory. This uses the ACM as an extension of fixed memory and the ATM as a source of programs.
Note: See Figure 4-3 which illustrates how V06 is executed.

VERB 07 — Similar to Verb 06. Location and destination of Exerciser Program are different.

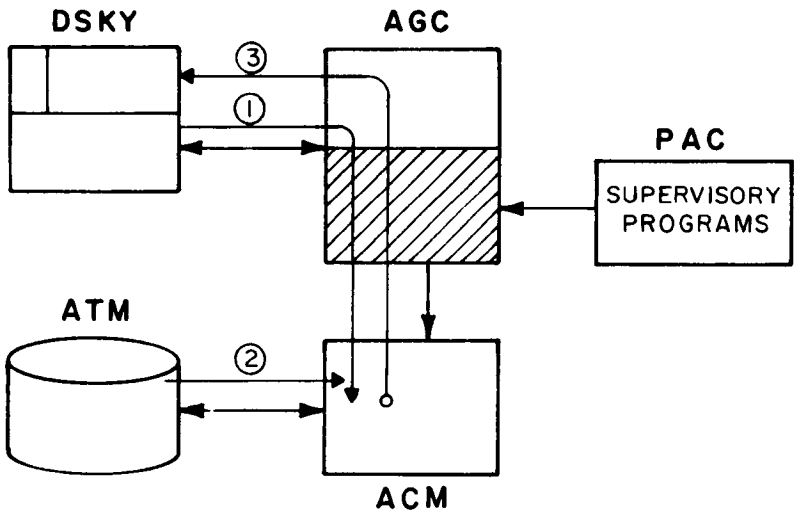
VERB 08 — Attempts to retrieve from the ATM Tape a record containing a deliberate uncorrectable error. The DSKY will display:

NOUN = 64 or 67 Indicating an aborted transfer
R1 = 55775 Address of error
R2 = 74200 CONOUT
R3 = 00420 CONIN

VERB 09 — Retrieves four consecutive records using "Banksum" technique to verify accuracy of transfer. The DSKY will display "All 7's" indicating successful Banksum.

VERB 10 — Retrieves from the ATM Tape a record containing 17 correctable errors. The record will be stored in the ACM Memory and the DSKY will display:

NOUN = 77
R1 = 00017 Indicating number of corrected errors



STEP

(1.) "VERB-0-6 ENTER"
Supervisor program
(In pac) specifies
location (on ATM tape)
of exerciser program.

(2.) Tape-stored program is
read and stored into ACM.

(3.) Program in ACM is executed.
Displays sequence on DSKY.

4. Upon completion, DSKY
display will be "all 7's"
indicating success.

Vigure 4-3 Execution of Verb 06

R2 = 77777 Part of "All 7's" Success Display

R3 = 77777 Part of "All 7's" Success Display

VERB 11 Attempts to retrieve a short record from the ATM Tape. The DSKY will display:

NOUN = 64 or 67 Indicating an aborted transfer

R1 = 24025 Identification code of offending record

R2 = 74200 CONOUT

R3 = 00100 CONIN

VERB 12 Similar to Verb 11 with a long record. The display is as above with R1 = 30026.

VERB 13 Attempts to retrieve a nonexistent record. The DSKY will display:

NOUN = 70 Indicating requested record does not exist

R1 = 37777 ID code of record found prior to abort

R2 = 74000 CONOUT

R3 = 02000 CONIN

VERB 21 Retrieves a four record program from the ATM tape and stores it in Memory Unit 4. The program is executed from this memory unit and the DSKY will display "All 7's" upon successful completion.

4.3.3 DATA TAPE TESTS

The ACM Data Storage, ACM Data Load, ATM Data Load, ATM Data Verify, and ATM Data Reload modes are demonstrated with Verbs 14-16 and 22. These verbs perform transfers from AGC Memory to the E Memory of the ACM, transfers of data from MU 5 to tape, transfers of data from tape to MU 5, verification of ATM data, and reloads of data from MU 5 to tape.

VERB 14 Words are copied from PAC and written on the tape, then read back and compared with the original set. A successful comparison is indicated by a display of "All 7's".

This uses the ACM as extensions of Fixed and Erasable Memory, and uses the ATM as a data recorder.

Note: See Figure 4-4 which illustrates how Verb 14 is executed.

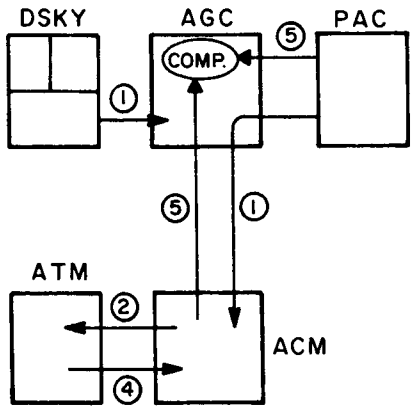
VERB 15 Similar to Verb 14 except data are written and retrieved in Simplex (Nonredundant) Format. Errors may occur using this mode. Upon detecting an error, the DSKY will display:

NOUN	=	56	Indicates Invalid Comparison
R1	=	xxxxx	Address of Error
R2	=	xxxxx	ACM Data
R3	=	xxxxx	PAC Data

If no errors are found, the DSKY will display "All 7's". This uses the ACM as an extension of fixed and erasable, and uses the ATM as a Simplex Data Recorder.

VERB 16 A record is written on the ATM tape, then a different record is written overlaying the first record. This record is read back from the ATM tape and compared with its original as in Verb 14.

This uses the ACM as an extension of fixed and erasable memory and demonstrates Rewrite or "Write Over" capability of ATM.



Step

1. "Verb-1-4-Enter" Causes Supervisor (In PAC) to Transfer 1024 Words from PAC to ACM.
2. The 1024 Words are Written on the Tape in Triple Redundant Format.
3. The Supervisor Clears the ACM Memory.
4. The Record just Written is Recalled into the ACM.
5. Each Word is Compared with the Original (In PAC).
6. Successful Comparison of All 1024 Words is Indicated by "All 7's" Display.

Figure 4-4 Execution of Verb 14

VERB 22 This verb uses the ACM Memory as an extension of Fixed and Erasable Memory, and uses the ATM as a data recorder. Verb 22 performs the following 4-bank transfers: PAC banks 12 through 15 to MU4, then from MU4 to MU5. From MU5 the data is transferred to ATM tape after which MU5 is cleared. The record just written is recalled into MU5 and the contents of MU4 and MU5 are compared. See Figure 4-5 which illustrates how Verb 22 is executed.

4.3.4 RESTART TESTS

The Demonstration Program includes a GOJAM routine which is responsible for determining the cause of a GOJAM; this routine is shown in Figure 3-1. In order to demonstrate the error detection circuitry, the following verb programs are provided:

VERB 17 This verb will cause the AGC to sequentially read every location in the ACM. This verb is used after errors have been deliberately inserted into the ACM. These errors cause ACM GOJAMS.

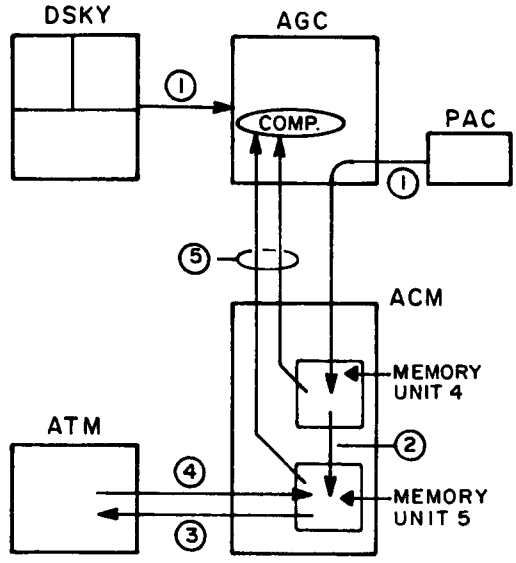
VERB 18 This verb causes an AGC GOJAM by producing a TC TRAP.

VERB 19 This verb causes an AGC GOJAM by producing a RUPTLOCK.

VERB 20 This verb causes an AGC GOJAM by producing a NIGHT WATCHMAN alarm.

The cause of a GOJAM is indicated on the DSKY by the left 4 digits of R1 as follows:

1's	E parity ACM
2's	F parity ACM
3's	ECHO check fail
4's	AGC failure
5's	Stuck 1
6's	Stuck 1 or AGC failure



Step

1. "Verb-2-2-Enter" Causes Supervisor to Transfer 4096 Words from PAC to Memory Unit 4.
2. Then from Memory Unit 4 to 5.
3. Then on to the ATM Tape.
4. Memory Unit 5 is Cleared and the Record Just Written is Recalled from the Tape.
5. The Contents of Memory Units 4 and 5 are Compared.
6. Successful Comparison of All 4096 Words is Indicated by "All 7's" Display.

Figure 4-5 Execution of Verb 22

The last digit of R1 indicates the status of OUTCOM after the GOJAM and before any setting of OUTCOM during the GOJAM. R2 displays CONOUT and R3 displays CONIN.

APPENDIX A

INTERFACE DEFINITION
AUXILIARY CORE MEMORY ACM—AUXILIARY TAPE MEMORY ATM

A.1 SIGNAL DEFINITION

A.1.1 ATM INPUT SIGNALS

Typical signal origination and termination configuration and characteristics are shown in Figures A1 to A5.

A.1.1.1 ATMSNC and ATMSNC/(25.6K Hz Power Sync and Return)

A pair of complementary square wave inputs operating at 25.6K Hz to provide a synchronizing signal to the ATM power supply for both the "STANDBY" and "ON" modes.

A.1.1.2 ATMNBL (ATM Enable)

A discrete input that will be continously at the logical ONE level whenever the ATM is required to operate. This signal turns the ATM from "STANDBY" to "ON".

A.1.1.3 GOREV (Go Reverse Tape)

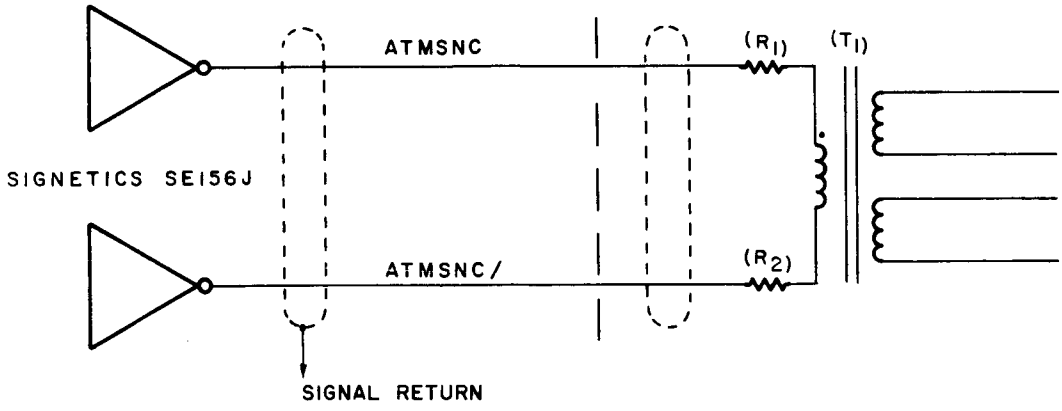
A discrete input that will be continuously at the logical ONE level whenever the ATM is required to move BOT towards the read-write head.

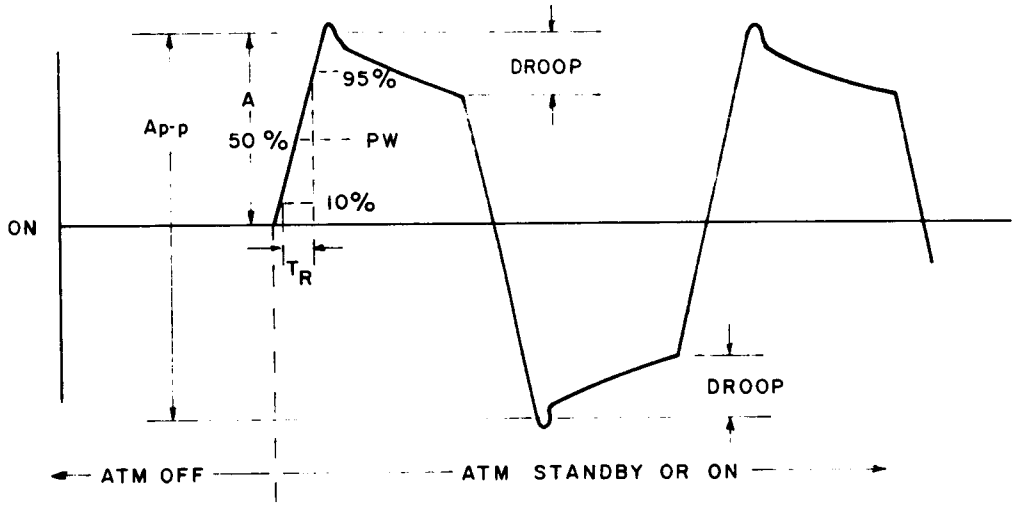
A.1.1.4 GOFWD (Go Forward Tape)

A discrete input that will be continuously at the logical ONE level whenever the ATM is required to move EOT towards the read-write head.

A.1.1.5 RTAPE (Read Tape)

A discrete input that will be continuously at logical ONE level whenever the ATM is required to read information from the tape.





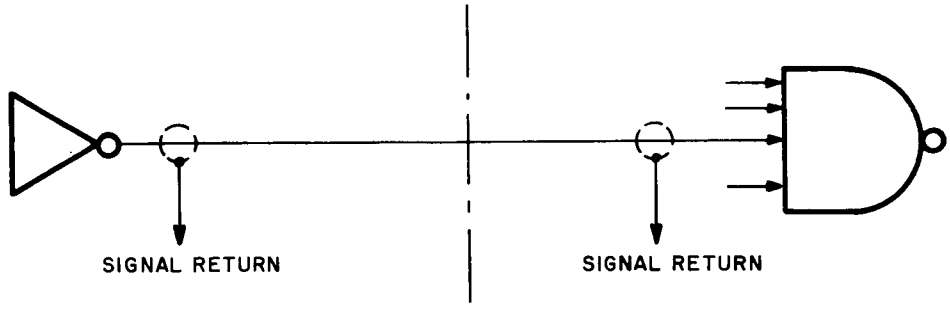
Pulse Frequency - 25.6 KHz ± Hz

P-P Amplitude 8 ± 2v Measured Differentially
Pulse Width (50% of A) - 19.5 μsec ± 2.0μsec.
Rise Time T_R (10% - 90% of A) MMT 0.2 μsec
Droop - NMT 20% of A P-P

When ATM power supply is switched off ATMSNC and ATMSNC/ will be at + V_{cc} with respect to signal return

Figure A-1 Interface Signals ATMSNC, ATMSNC/

TYPICAL ACM/ATM DISCRETE LEVEL OUTPUTS



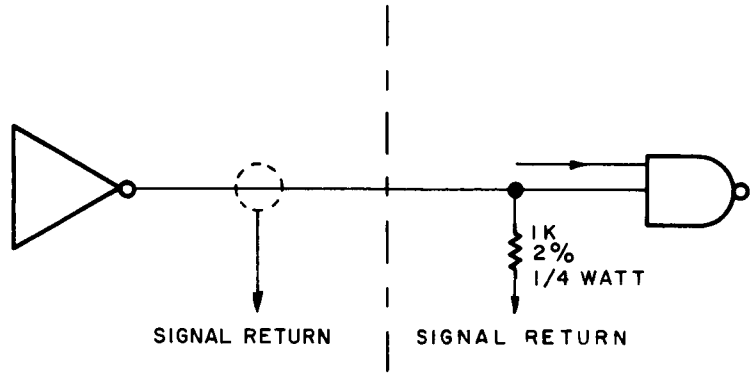
OUTPUT VOLTAGE LEVEL

	MAX	MIN
LOGIC LEVEL "1"	+ 6.0 VDC	+3.0 VDC
LOGIC LEVEL "0"	+ 0.3 VDC	0 VDC

REFERENCE

GOFWD
GOREV
RTAPE
NBLWD, NBLWP
BOT
COT
EOT
ATMON/
TMFWD, TMREV

Figure A-2 Typical ACM/ATM Discrete Level Outputs



OUTPUT VOLTAGE LEVELS

	MAX	MIN
LOGIC "1"	+6.0 VDC	+2.5VDC
LOGIC "0"	+0.3 VDC	0VDC

PULSE CHARACTERISTICS

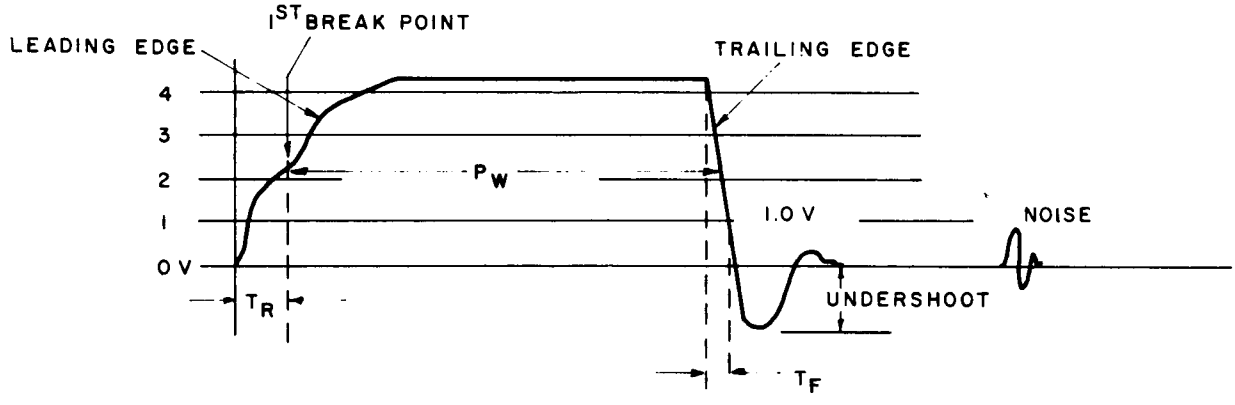


Figure A-3 Interface Signals ACM/ATM Read, Write and Strobe

Pulse Width (P_W) - Measured from the leading edge to the trailing edge at the amplitude of the first breakpoint.

Rise Time (T_R) - Measured on the leading edge of the pulse from the point of the first positive excursion to the first breakpoint (approx 2.0v).

Fall Time (T_F) - Measured on the trailing edge of the pulse from the point of the first negative excursion to the 1.0 volt amplitude line.

Undershoot - Measured as shown shall not exceed 1.5 volts.

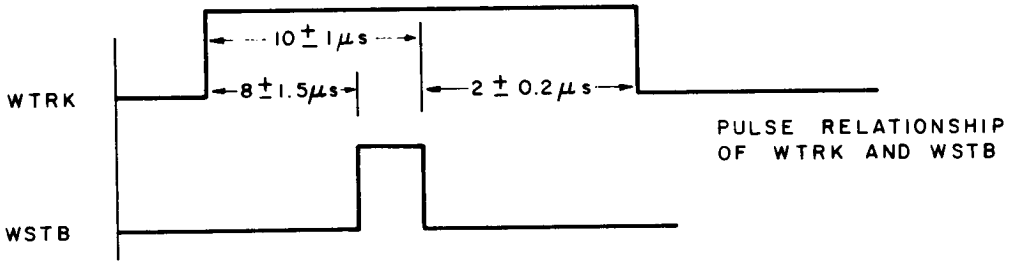
Noise - Not to exceed 1 v peak to peak.

WTRK 01 - WTRK 18

P_W = 20 μ sec $\pm$ 2
T_R = NMT 100 Msec
T_F = NMT 50 n.sec.

WSTB

P_W - 2 $\pm$ 0.5 μsec
T_R - NMT 100 Msec
T_F - NMT 50 n.sec.



RTRK 01 — RTRK 18

P_W = 38±2.0 μsec
T_R - NMT 100 n.sec
T_F NMT 50 n sec

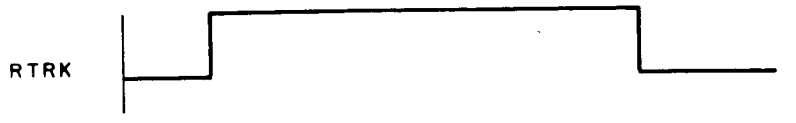
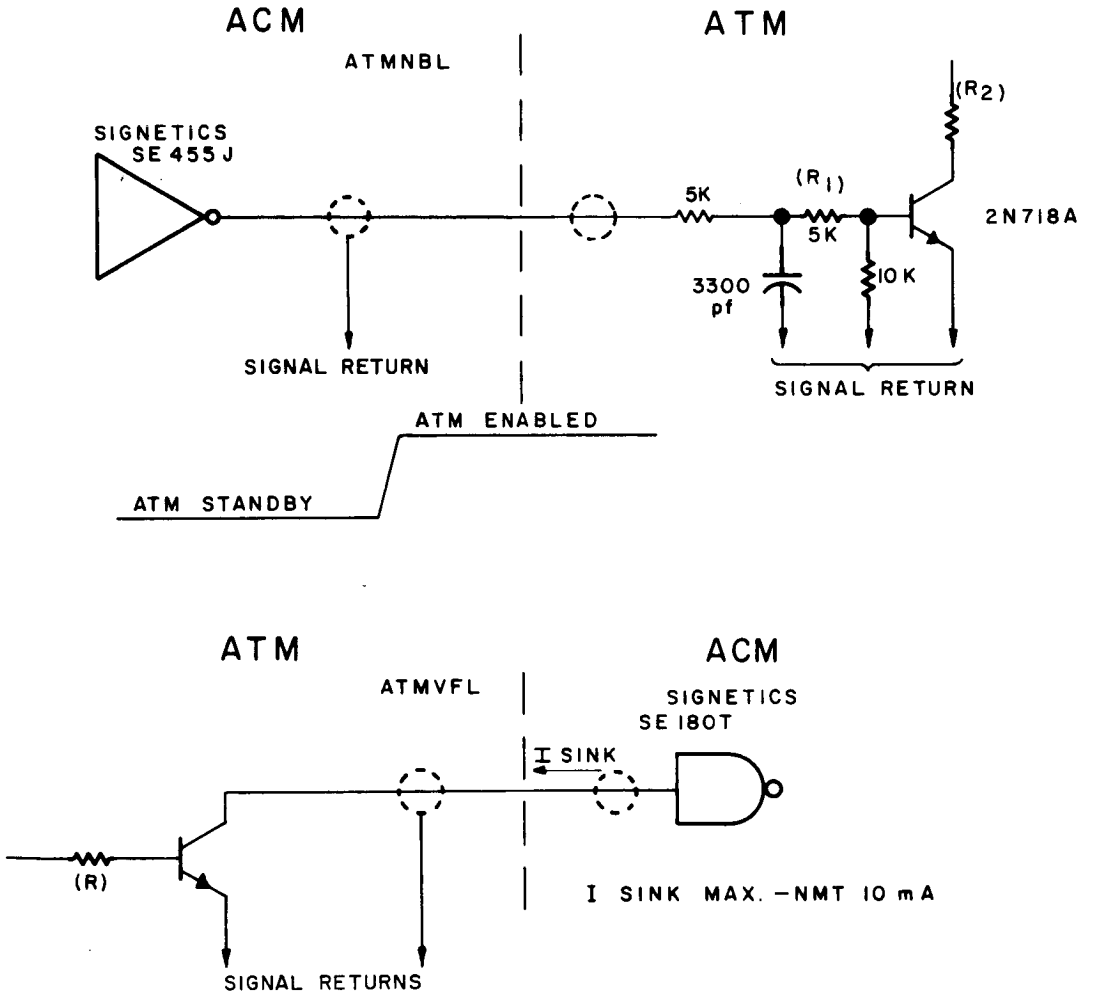
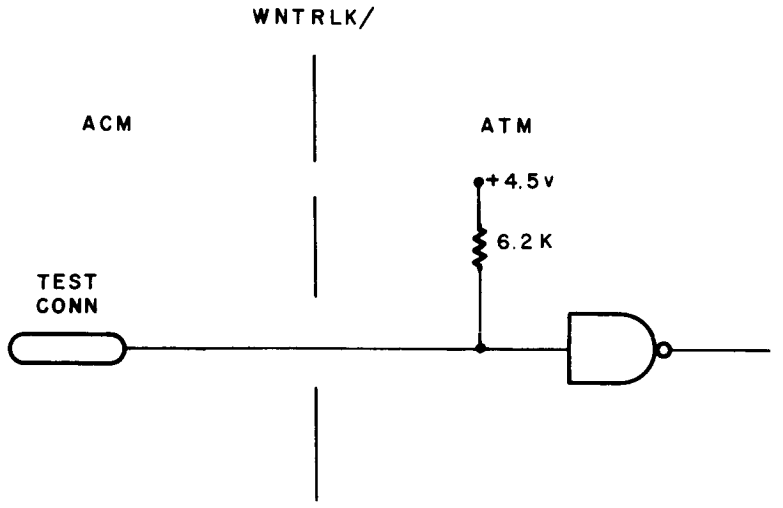


Figure A-3 Interface Signals ACM/ATM Read, Write and Strobe (Continued)



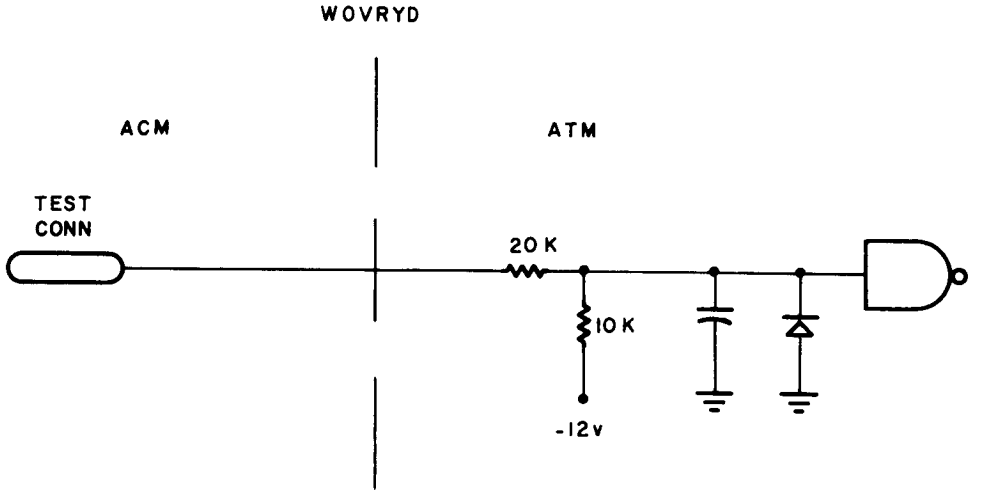
	MAX	MIN
LOGIC LEVEL "1"	+ 6.0 VDC	+ 3.0 VDC
LOGIC LEVEL "0"	+ 3.0 VDC	0 VDC

Figure A-4 Typical ACM/ATM Interface Signals



LOGIC LEVELS

	MAX.	MIN.
LOGIC 1	6.0v	3.0v
LOGIC 0	0.1v	0.0v



	MAX.	MIN.
LOGIC 1	33v	21.5v
LOGIC 0	1.0v	0.0v

Figure A-5 Interface Signals: WNTRLK/ and WOVRYD

A.1.1.6 WSTB (Write Strobe)

A pulse input that will be at the logical ONE level whenever the ATM is required to accept and write a single ATM word on the tape.

A.1.1.7 NBLW (Enable Write)

A discrete input that will be continuously at the logical ONE level whenever the ATM is required to write information on the tape.

A.1.1.8 WNTRLK/ (Write Interlock)

A discrete input signal which will prevent writing on the tape when grounded.

A.1.1.9 WOVRYD (Write Override)

A discrete input signal which when energized with a 28 volt discrete signal forces the write heads to write for tape erasure purposes (non flight).

A.1.1.10 WTRK01 Through WTRK18 (Write Tracks)

A parallel arrangement of 18 pulse input signals that will be at their respective logic levels for recording on the magnetic tape on eighteen (18) separate tape track positions.

The write line signals will have the same tape tracks as the corresponding read tracks, i.e., signal WTRK01 and signal RTRK01, WTRK02, and RTRK02, etc.

A.1.2 ATM OUTPUT SIGNALS

Typical signal origination and termination configuration and characteristics are shown in Figures A2 to A5.

A.1.2.1 BOT (Beginning of Tape)

A discrete output that will continuously be at a logical ONE whenever the beginning of the tape is reached.

A.1.2.2 COT (Center of Tape)

A discrete output that will be continuously at a logical ONE whenever the center of tape is reached.

A.1.2.3 EOT (End of Tape)

A discrete output that will be continuously at a logical ONE whenever the end of the tape is reached.

A.1.2.4 TMREV. TMFWD (Tape Moving)

A discrete output that will continuously be at a logical ONE whenever the tape is up to proper speed. This signal shall occur within one second ± 10% after the preceding motion commands GOREV and GOFWD, or the removal of status BOT, COT, or EOT, whichever comes last.

A.1.2.5 ATMON/ (ATM Not On)

A discrete output that will be continuously at a logical ZERO whenever the ATM is ready to properly provide and accept all control signals after ATMSNC, ATMSNC/ and ATMNBL are provided. A time period of not more than 500 milliseconds shall elapse for the removal of ATMON/ (logical ONE) after the application of ATMSNC/, and ATMNBL.

A.1.2.6 ATMVFL (ATM Voltage Fail)

A discrete output that will be continuously at a logical ZERO whenever the ATM Power Supply is normally operating. This discrete output shall change to a logical ONE following a disabling power interruption or an internal power supply failure. The ATMVFL shall occur at a time not less than 300 microseconds after the ATM suffers a disabling power interruption from the minimum steady state line voltage condition. The ATMVFL signal shall also precede by a time period not less than 10 microseconds the ATM's transmittal of erroneous outputs to the ACM due to the voltage failure.

A.1.2.7 RTRK01 Through RTRK18 (Read Tracks)

A parallel arrangement of 18 pulse output signals that will be at their respective logic levels representing information read from the eighteen (18) separate tape track positions. The read track signals will have the same tape tracks as the corresponding write line, i.e., signal RTRK01 and WTRK01, RTRK02, etc.

A.2 ON-OFF SEQUENCES

A.2.1 "TURN ON" SEQUENCES

A.2.1.1 "Off" to "Standby" Sequence

Upon receipt of a pair of signals ATMSNC and ATMSNC/, which are generated by the ACM and transmitted to the ATM, the ATM assumes the "Standby" condition (activates internal power supply). Furthermore, the ATM generates proper internal voltages and removes the ATMVFL signal (changes to a logical ZERO) within a time of approximately 100 milliseconds from the receipt of the ATMSNC and ATMSNC/ signals.

A.2.1.2 "Standby" to "On" Sequence

After the completion of the "Standby" sequence, the ACM generates the signal ATMNBL. At a time not more than 500 milliseconds after the receipt of this command, the ATM is ready to execute operational commands and signifies this by removing the signal "ATMON/" (ATMON/ at a logical ZERO).

A.2.2 "TURN OFF" SEQUENCE

A.2.2.1 "On" to "Standby" Sequence

Upon the removal of the signal ATMNBL, the ATM de-energizes its control logic with exception of the power supply. It signifies its "Standby" condition by generating the signal "ATMON/" (ATMON/ at a logical ONE) within a time not more than 50 μsec while maintaining ATMVFL at a logical ZERO condition.

A.2.2.2 ATM "Standby" to "Off" Sequence

After the removal of the ATMSNC and ATMSNC/ signals, the ATM reverts to the "Off" position (de-energizes the power supply) and transmits the ATMVFL signal at a logical ONE level.

A.2.2.3 Abnormal "Turn Off" Sequence

In the event of an external loss of power or a power malfunction within the ATM, the ATM is required to generate the signal ATMVFL at a logical ONE level. The ATMVFL shall occur at a time not less than 300 microseconds after the ATM suffers a disabling power interruption from the minimum steady state line voltage condition. The ATMVFL signal shall also precede by a time period not less than 10 microseconds the ATM's transmittal of erroneous outputs to the ACM due to voltage failure.

APPENDIX B

INTERFACE SIGNAL ROUTING

This appendix describes the AM utilization of AGC input and output signals at test connector A52, and gives a description of the pins being grounded by the test connector cover. Since an objective of the IM and piggyback adapter design is to maintain congruence with the GSE (W226 and Buffer Circuit Assembly), the disposition of each A52 pin in these elements of GSE is also included.

Signal Summary

Table B-1, A52 Pin Connections, presents every test connector pin, together with the name of the AGC signal appearing on each pin. If a signal is used by the ACM, a "yes" appears in the next column headed "ACM USAGE." Input signals to the AGC from the ACM are distinguished by "to AGC" in this column. For those pins connected to wires in cable W226, the Buffer Circuit Assembly termination is indicated (BC = buffer circuit, NRC = noise rejection circuit).

Pins grounded by the cover are identified by a "yes" in the "COVER GROUND" column. Finally, if a signal is renamed at the GSE side of the Buffer Circuit Assembly, the GSE name is given in the "GSE SIGNAL NAME"column.

Observations

Note that the total number of BC's and NRC's tabulated does not agree with the contents of a Buffer Circuit Assembly; the two spare BC's and one spare NRC are not included. Cable W226 does not pick up these circuits. Two Special Circuits, used only with Block I-100 Series AGC's, have also been excluded.

The test connector cover ties all pins it picks up into one group and connects them to the cover frame. Continuity to the AGC tray is made through contact at the cover face; the 10 milliohm requirement of the AGC assembly drawing applies at this face.

TABLE B-1

A52 PIN CONNECTIONS

A52 PIN	AGC SIGNAL	ACM USAGE	GSE USAGE	COVER GROUND	GSE SIGNAL NAME
101	MDT 01	Yes	NRC	Yes	
102	MDT 02	(All 16	(All 16	Yes } All 16	
=	=	To AGC	Use NRC)	= } Yes	
116	MDT 16	Yes	NRC	Yes	
201	MWL 01	Yes	BC		
202	MWL 02	Yes	(All 16		
=	=	(All 16)	Use BC)		
216	MWL 16	Yes	BC		
301	MT 01	Yes	BC		
302	MT 02	Yes	(All 12		
=	=	(All 12)	Use BC)		
312	MT 12	Yes	BC		
313	MRULOG		BC		
314	MWFBG	Yes	BC		
315	MWESG	Yes	BC		MWESG
316	MWBBEG	Yes	BC		MWBBG
401	MST 1	Yes	BC		
402	MST 2	Yes	BC		
403	MST 3	Yes	BC		
404	MTCSA/		BC		
405	MWSG	Yes	BC		
406	MWZG		BC		
407	MWYG		BC		
408	MWQG		BC		
409	MWBG		BC		
410	MSQ10	Yes	BC		
411	MSQ11	Yes	BC		
412	MSQ12	Yes	BC		
413	MSQ13	Yes	BC		
414	MSQ14	Yes	BC		
415	MSQEXT	Yes	BC		
416	MSQ16	Yes	BC		

TABLE B-1

A52 PIN CONNECTIONS (Continued)

A52 PIN	AGC SIGNAL	ACM USAGE	GSE USAGE	COVER GROUND	GSE SIGNAL NAME
501	MBR1		BC		
502	MBR2		BC		
503	MIIP		BC		
504	MCTRAL/		BC		
505	MTCAL/		BC		
506	MRPTAL/		BC		
507	ALGA		W226 Omits		
508	MPAL/		BC		
509	MSTPTT/		BC		
510	MGOJAM	Yes	BC		
511	MINHL		BC		
512	MINKL		BC		
513	MWLG		BC		
514	MONWT	Yes	BC		
515	MRSC	Yes	BC		
516	MRLG		BC		
601	STRT1		GRD thru S2		
602	STRT2		GRD thru S2		
603	MNHSBF	To AGC	NRC	Yes	
604	MNHNC		*NRC	Yes	
605	MNHRPT		*NRC	Yes	
606	MTCSAI		NRC	Yes	
607	MSTRT	To AGC	*NRC	Yes	
608	MSTP		NRC	Yes	
609	MSBSTP		*NRC	Yes	
610	MRDCH	To AGC	NRC	Yes	
611	MLDCH	To AGC	NRC	Yes	
612	MGP/		BC		
613	MSP		BC		
614	MRGG	Yes	BC		
615	MWAG		BC		
616	MRAG		BC		

*NRC has 1.0 uf capacitor to ground on GSE side.

TABLE B-1

A52 PIN CONNECTIONS (Continued)

A52 PIN	AGC SIGNAL	ACM USAGE	GSE USAGE	COVER GROUND	GSE SIGNAL NAME
701	CNTRL 1		Wire to GSE		
702	CNTRL 2		Wire to GSE		
703	MTHI		To BNC Conn.		
704	MTLO		To BNC Conn.		
705	MWCH	Yes	BC		
706	MRCH	Yes	BC		
707	MONPAR	To AGC	NRC	Yes	
708	MONWRK		NRC	Yes	
709	MWG	Yes	BC		
710	MNISQ		BC		
711	MREQIN	Yes	BC		
712	MWATCH/		BC		
713	MLOAD		NRC	Yes	
714	MREAD		NRC	Yes	
715	MON800	Yes	BC		
716	MPIPAL/		BC		
801	BPLSSW		Wire to GSE		PWR 1
802	+ 4SW	Yes No L.D.	Wire to GSE		PWR 2
803	NC		BC		MAL 13
804	SIGNY		BC		MAL 18
805	NC		W226 Omits	Yes	
806	NC		BC	Yes	MAL 14
807	NC		BC	Yes	MAL 15
808	MSCDBL/		BC		
809	NHALGA		To +3V thru 510 ohms & S1	Yes	
810	DOSCAL		*NRC	Yes	
811	DBLTST		NRC	Yes	
812	MWARNF/		BC		
813	OUTCOM	Yes	BC		MOUTCOM
814	MSCAFL/		BC		
815	MOSCAL/		BC		
816	MVFAIL/		BC		

*NRC has 1.0 uf capacitor to GND on GSE side.

TABLE B-1

A52 PIN CONNECTIONS (Continued)

A52 PIN	AGC SIGNAL	ACM USAGE	GSE USAGE	COVER GROUND	GSE SIGNAL NAME
901	OVDCA		W226 to BCA Only		
902	NC		W226 Omits		
903	OVDCA		Wire to GSE		GRD
904	NC		BC	Yes	Spare
905	OVDCA		Wire to GSE	Yes	GRD
906	MAMU	Yes	BC	Yes	Spare
907	OVDCA		Wire to GSE	Yes	GRD
908	NC		BC	Yes	Spare
909	OVDCA		Wire to GSE	Yes	GRD
910	NC		BC		MAL 17
911	OVDCA		Wire to GSE		GRD
912	NC		BC		MAL 11
913	OVDCA		Wire to GSE		GRD
914	NC		BC		MAL 16
915	OVDCA		Wire to GSE		GRD
916	NC		BC		MAL 10

Remarks

Examination of Table B-1 indicates that the following classification of pins can be made, in terms of the presence or absence of a wire in the AGC and GSE at each pin:

AGC A52	GSE	PIN NO.	SIGNAL	SUB-TOTAL
Wire	Wire	(See below for these)		132
Wire	No Wire	507	ALGA(AGC)	1
No Wire	No Wire	805, 902	---------	2
No Wire	Wire	803	MAL 13 (GSE)	
		806	MAL 14 (GSE)	
		807	MAL 15 (GSE)	
		904	SPARE (GSE)	
		908	SPARE (GSE)	
		910	MAL 17 (GSE)	

AGC	GSE	PIN NO.	SIGNAL	SUB-TOTAL
		912	MAL 11 (GSE)	
		914	MAL 16 (GSE)	
		916	MAL 10 (GSE)	10
				144

The first classification is now examined in more detail; the last three are of interest only in terms of preserving a degree of congruence between the IM and piggyback adapter combination and existing GSE.

The 132 signal-carrying pins in the first classification may be further subdivided according to the type of GSE circuit, (equivalent to partitioning AGC input and outputs). Pursuing this approach results in Table B-2, B-3, B-4, B-5 and B-6.

TABLE B-2

AGC INPUT SIGNALS, SHARED BY ACM and GSE

A52 PIN	AGC SIGNAL	ACM USAGE	GSE USAGE	COVER GROUND	GSE SIGNAL NAME
101	MDT01	To AGC	NRC	Yes	
102	MDT02	"	"	"	
103	MDT03	"	"	"	
104	MDT04	"	"	"	
105	MDT05	"	"	"	
106	MDT06	"	"	"	
107	MDT07	"	"	"	
108	MDT08	"	"	"	
109	MDT09	"	"	"	
110	MDT10	"	"	"	
111	MDT11	"	"	"	
112	MDT12	"	"	"	
113	MDT13	"	"	"	
114	MDT14	"	"	"	
115	MDT15	"	"	"	
116	MDT16	"	"	"	
603	MNHSBF	"	"	"	
607	MSTRT	"	NRC	"	
610	MRDCH	"	"	"	
707	MONPAR	"	"	"	
906	MAMU	To AGC	NRC	Yes	
611	MLDCH	"	"	"	
			TOTAL 22 pins		

TABLE B-3

AGC INPUT SIGNALS ORIGINATING IN GSE

A52 PIN	AGC SIGNAL	ACM USAGE	GSE USAGE	COVER GROUND	GSE SIGNAL NAME
604	MNHNC		NRC	Yes	
605	MNHRPT		NRC	Yes	
606	MTCSAI		NRC	Yes	
608	MSTP		NRC	Yes	
609	MSBSTP		NRC	Yes	
708	MONWBK		NRC	Yes	
713	MLOAD		NRC	Yes	
714	MREAD		NRC	Yes	
810	DOSCAL		NRC	Yes	
811	DBLTST		NRC	Yes	
			TOTAL 10 pins		

Table B-2 contains those pins with AGC input signals to be shared by NRC's in the IM and the GSE piggyback adapter.

Table B-3 contains those pins with AGC input signals originating in the GSE only, not in the ACM.

Observe that every pin in Table B-2 and B-3 is grounded by the test connector cover; this is to be expected, since these pins carry input signals to the AGC.

Continuing, Table B-4 contains those pins carrying AGC output signals to be shared by BC's in the IM and the GSE, while Table B-5 contains those pins with AGC output signals used only by the GSE and not the ACM, for which BC's have been provided in the piggyback adapter.

Tables B-2 through B-5 contain a total of 115 pins. The remainder of the 131 in this classification are contained in Table B-6 consisting of two power, eight ground, and seven other signal pins.

TABLE B-4

AGC OUTPUT SIGNALS SHARED BY ACM AND GSE

A52 PIN	AGC SIGNAL	ACM USAGE	GSE USAGE	COVER GROUND	GSE SIGNAL NAME
201	MWL01	Yes	BC		
202	MWL02	"	"		
203	MWL03	"	"		
204	MWL04	"	"		
205	MWL05	"	"		
206	MWL06	"	"		
207	MWL07	"	"		
208	MWL08	"	"		
209	MWL09	"	"		
210	MWL10	"	"		
211	MWL11	"	"		
212	MWL12	"	"		
213	MWL13	"	"		
214	MWL14	"	"		
215	MWL15	"	"		
216	MWL16	"	"		
301	MT01	"	"		
302	MT02	"	"		
303	MT03	"	"		
304	MT04	"	"		
305	MT05	"	"		
306	MT06	"	"		
307	MT07	"	"		
308	MT08	"	"		
309	MT09	"	"		
310	MT10	"	"		
311	MT11	"	"		
312	MT12	"	"		
314	MWFBG	Yes	BC		
315	MWEBG	"	"		MWESG
316	MWBBE(	"	"		
401	MST1	"	"		
402	MST2	"	"		
403	MST3	"	"		
405	MWSG	"	"		
410	MSQ10	"	"		
411	MSQ11	"	"		
412	MSQ12	"	"		
413	MSQ13	"	"		
414	MSQ14	"	"		
415	MSQEX T	"	"		
416	MSQ1€	"	"		
510	MGOJ/ M	"	"		
514	MONW]	"	"		
515	MRSC	"	"		
614	MRGG	"	"		
705	MWCH	"	"		
706	MRCH	"	"		
709	MWG	"	"		
711	MREQ :N	"	"		
715	MON8)0	"	"		
813	OUTC)M	"	"		MOUTCOM

TOTAL - 52

TABLE B-5

AGC OUTPUT SIGNALS USED ONLY BY GSE

A52 PIN	AGC SIGNAL	ACM USAGE	GSE USAGE	COVER GROUND	GSE SIGNAL NAME
313	MRULOG		BC		
404	MTCSA/		"		
406	MWZG		"		
407	MWYG		"		
408	MWQG		"		
409	MWBG		"		
501	MBR1		"		
502	MBR2		"		
503	MIIP		"		
504	MCTRAL/		"		
505	MTCAL/		"		
506	MRPTAL/		"		
508	MPAL/		"		
509	MSTPIT/		"		
511	MINHL		"		
512	MINKL		"		
513	MWLG		"		
516	MRLG		"		
612	MGP/		"		
613	MSP		"		
615	MWAG		"		
616	MRAG		"		
710	MNISQ		"		
712	MWATCH/		"		
716	MPIPAL/		"		
804	SIGNY		"		MAL18
808	MSCDBL/		"		
812	MWARNF/		"		
814	MVFAIL/		"		
815	MOSCAL/		"		
816	MVFAIL/		"		
				TOTAL - 31 pins	

TABLE B-6

MISCELLANEOUS AGC TEST CONNECTOR SIGNALS

A52 PIN	AGC SIGNAL	ACM USAGE	GSE USAGE	COVER GROUND	GSE SIGNAL NAME
601	STRT1				
602	STRT2				
701	CNTRL1				
702	CNTRL2				
703	MTHI				
704	MTLO				
801	BPLSSW				PWR1
802	+4SW	No L.D.	Wire to GSE		PWR2
809	NHALGA		Yes		
901	0VDCA				
903	0VDCA				
905	0VDCA		Yes		
907	0VDCA		Yes		
909	0VDCA		Yes		
911	0VDCA				
913	0VDCA				
915	0VDCA				

Summary

Having identified each of the four classifications of A52 pins, the following is provided to recapitulate what is diffused throughout Tables B-2 to B-6. It should be noted that the diode-resistor networks in Figure B-1 are the equivalent of NRC's, and that the LD's (line drivers) replace the BC's in the GSE. Also note that every NRC provides an input signal driving AGC micrologic (except signal MSBSTP, not supplied by the ACM), and that every BC buffers an output signal supplied by an AGC "blue nose" gate (except for SIGNY, not used by the ACM, and several pins not connected in the AGC). Certain other signals (ALGA, STRT 1, STRT 2, CNTRL 1, CNTRL 2, MTHI, MTLO, BPLSSW, +4SW,

NHALGA, and OVDCA) are either driven by or terminated in other circuits. Individual investigation is required if the use of any of these signals is contemplated.

Figure B-1 presents the results graphically; sheet 1 as derived in the foregoing analysis, and sheet 2 in a consolidated form with all circuits of a given type shown one in each module.

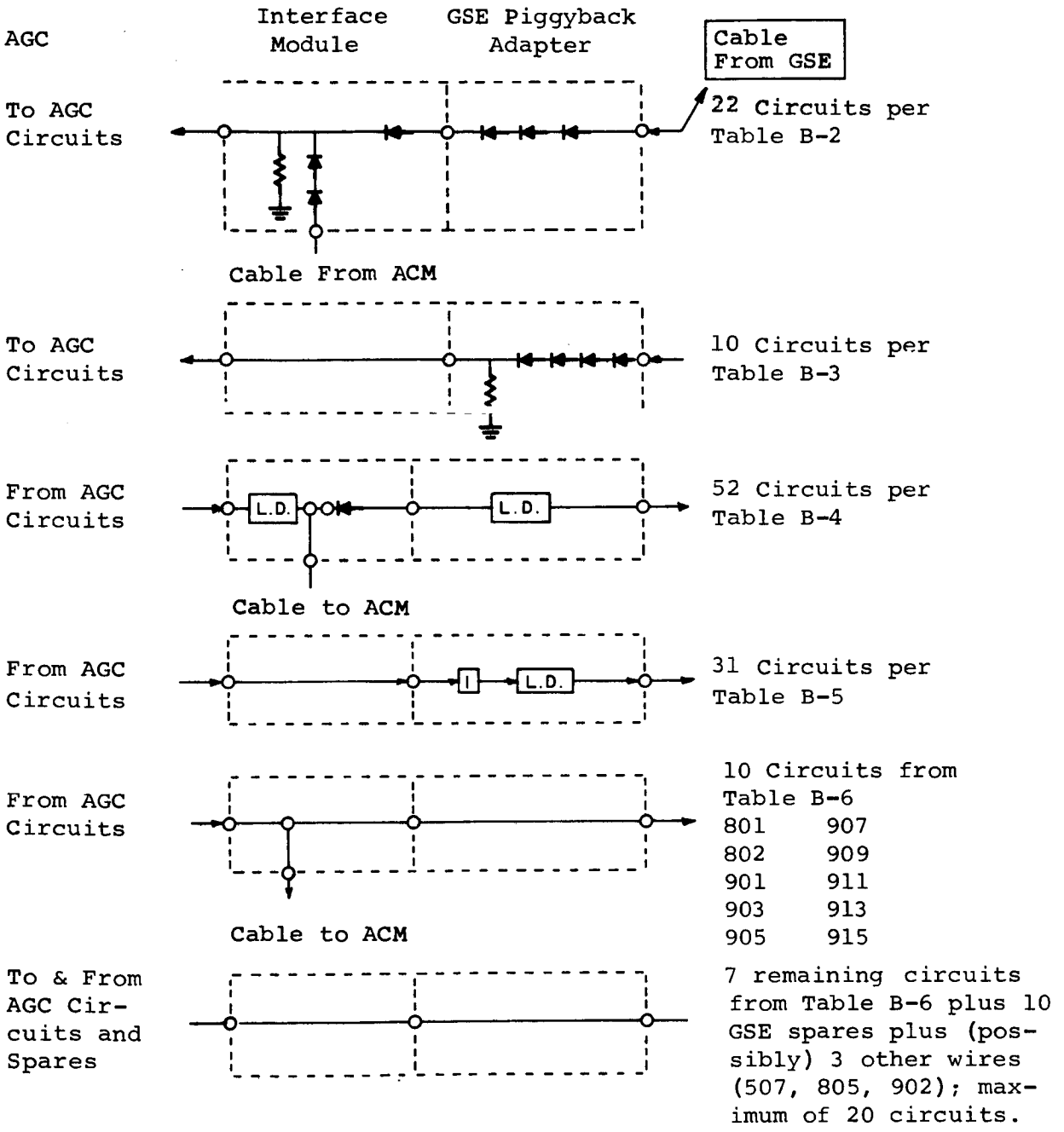
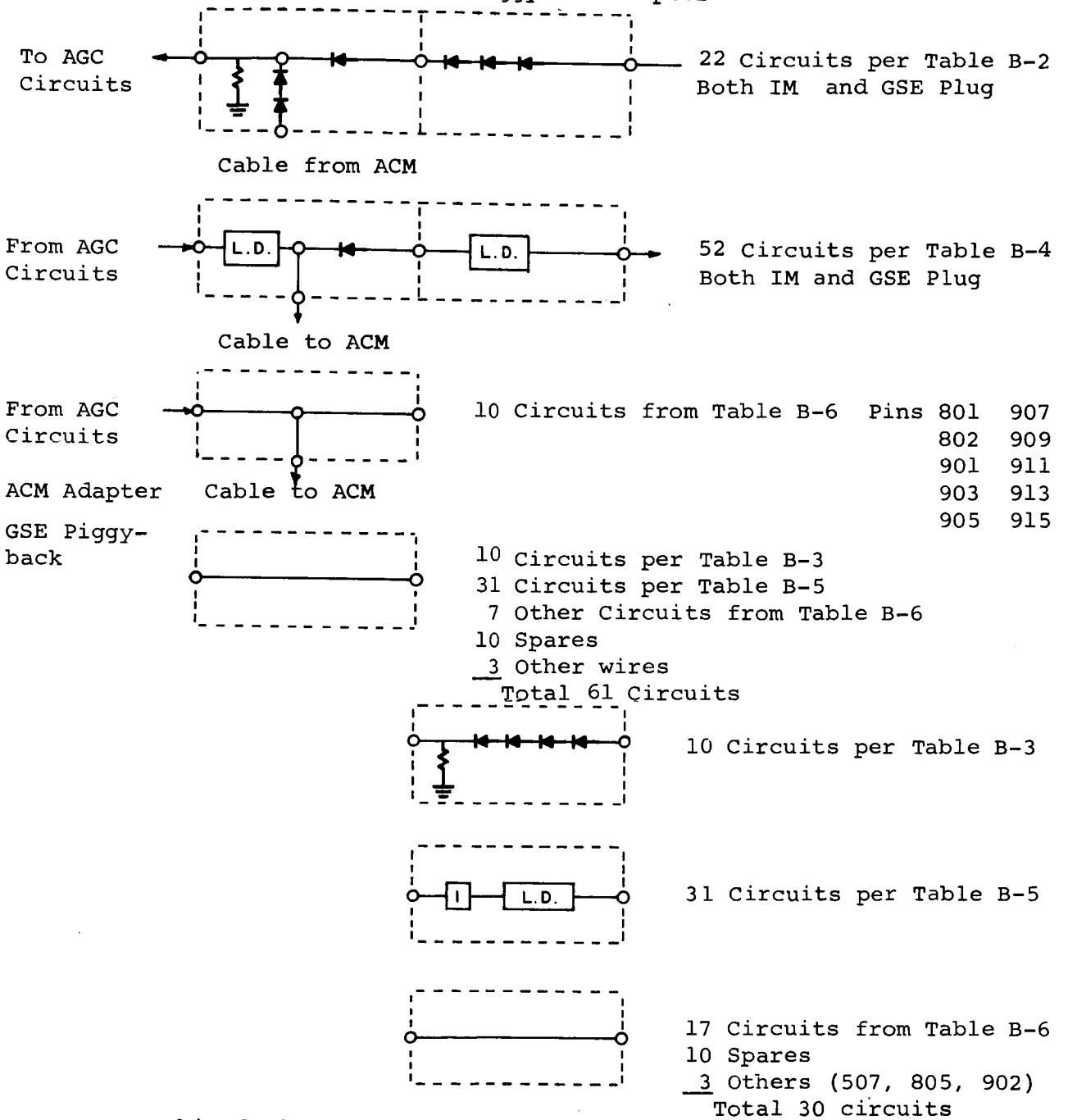


Figure B-1 AM Interface Module and GSE Adapter Design

Eliminating the duplication of circuit types yields the following final design.



This defines both adapters, with respect to interface signals; power and ground signals from the ACM and GSE must also be provided, although they have not been specified herein.

Figure B-1 AM Interface Module and GSE Adapter Design (Continued)

APPENDIX C

TAPE INITIALIZATION AND PROGRAM TAPE PREPARATION

In the event that large sections of the tape become erased and the tape ID's and fillers have been replaced, or if a requirement for a new set of tape ID's and fillers arises, the Control Panel has been designed to apply the ID's and fillers on the tape at the appropriate (1/4 sec.) intervals. The technique used to prepare a tape involves first filling an MU5 bank with a list of program tape or data tape ID's and then performing a Write Tape operation to load the bank on the tape.

During normal writing operations, cycle steal requests are issued periodically to gain access to the ACM core stack for successive words to be written on the tape. Simplex words are requested at a rate of 12,800/sec., while triplex words are requested at a rate of 4267/sec. Since the ATM cannot write the next word until it is available in register GAM at the completion of a stolen memory cycle, any condition within the AGC which delays the servicing of a cycle steal request will stretch the spacing of words on tape beyond the normal 78 μsec. As long as the stretch does not exceed 312 μsec between any two adjacent tape words, the gap-sensing logic will not declare that a gap has been detected (a gap, when detected, is assumed to be the end of a record, following which is the next ID word).

To write ID markers and filler words on the tape, we arrange to slow down the response of the AGC to cycle steal requests, so that words are extracted from the ACM core stack every 1/4 second. At this very low rate, a bank of 1024 words takes 256 seconds to be written; with a tape speed of 15 in/sec., a section of tape 320 feet long can be prepared with marker and filler words. Thus either the program or data sections of tape can be accommodated with this technique.

In order to space the ID's at 1/4 sec. intervals, the ACM is

fooled by the Control Panel into thinking there is activity in the AGC which is preventing tape memory cycle-steals. In Figure C-1 a load channel request (AMLDCH) is posted to the AGC, which in turn responds with an AMREQIN at the end of an instruction. By inhibiting the AMREQIN's from resetting the LDCH requests, the AGC is tied up indefinitely while trying to acknowledge the request. Therefore, the AGC will not be performing any meaningful programs (such as monitoring the ACM) while tape is being prepared. The Verb 00, Enter, 4 for writing tape may be used to initiate the writing process, but all DSKY and PAC displays must be ignored thereafter.

Every 250 msec, an AMREQIN is allowed to reset the LDCH request flip-flop, a stolen cycle is used to obtain the next word from the ACM Core Stack and the word is transferred to tape. Since ID's are being written, the triplex mode must have been selected, and the next cycle steal request will occur in approximately 240 usec. The control panel will prevent the next thousand or so responses to cycle steal requests from resetting the flip-flop. After 250 msec has passed, the resetting function is permitted to operate normally for one memory cycle. In this way, triplex words are spaced 1/4 sec. apart on the tape.

The ID and filler words must be available in MU5 to be written on the tape. These words are stored on the tape in condensed form, as a table together with a program which assembles them into a list in MU5. The table and the program are presently stored on the program tape in four different locations at ID's 00060 and 24160 (Data Tape ID table to be transferred to Tape bank 0, MU4) and at ID's 00061 and 24161 (Program Tape ID table to be transferred to Tape bank 1, MU4).

Accompanying each of the above ID tables to MU4 is the program which assembles the respective ID table into an ID list in an MU5 memory bank. Execution of the program must take place in an AGC unswitched erasable bank, and therefore the entire ID table and program must be transferred to AGC erasable memory.

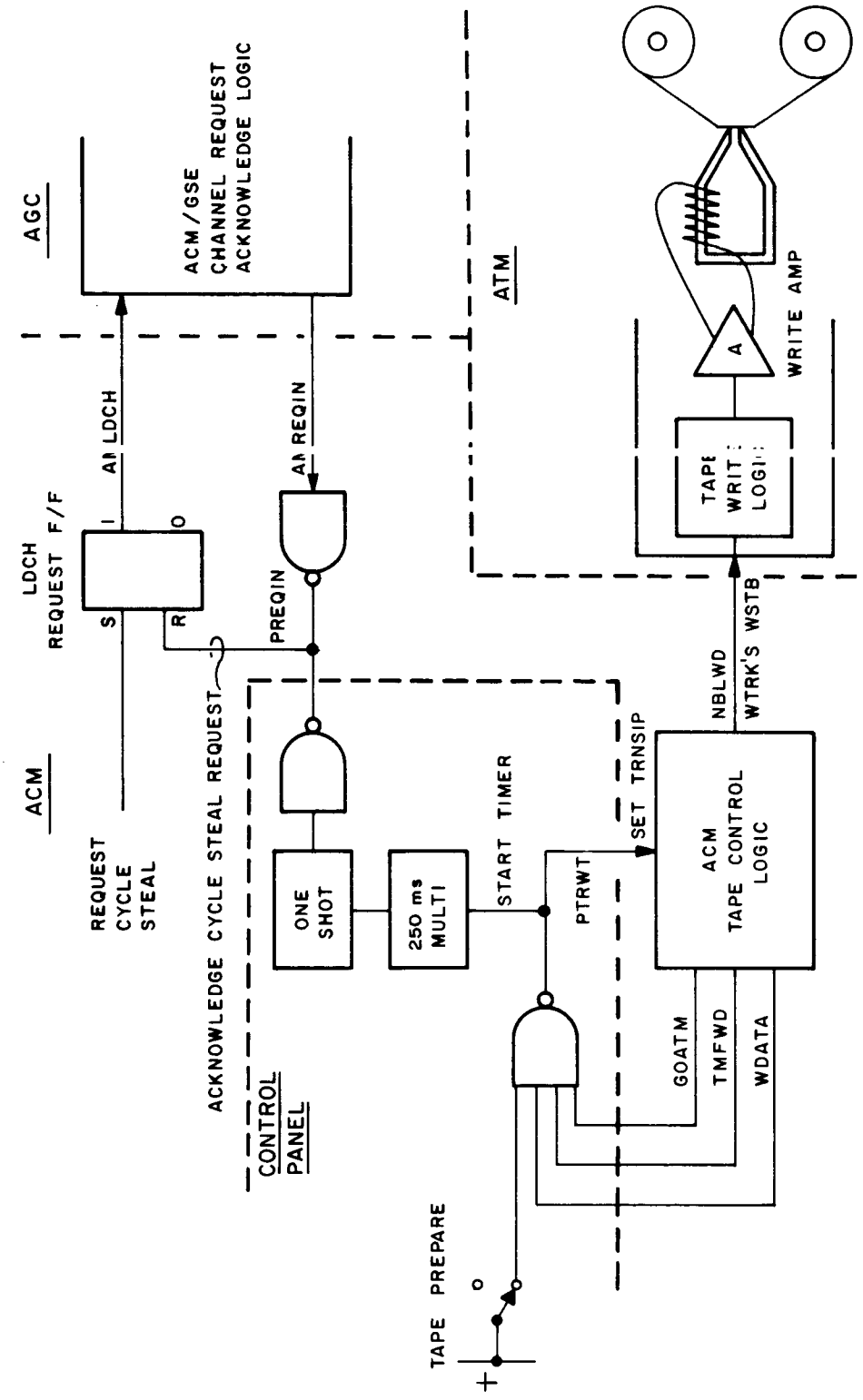


Figure C-1 Tape Prepare Block Diagram

The utility verb 00 (see Appendix F) may be used to transfer the MU4 bank to Bank 01 in the AGC. The program, moved with the table from the tape to MU4 to an AGC EBANK may now be executed by TC'ing to Address 700. The TC will assemble an ID list in MU5, EBANKS 24 through 27, ready to be written on the tape.

After the list has been assembled, the tape may be erased via the protected ERASE Switch on the control panel. By erasing from EOT to BOT, the tape will end up in a position to begin preparation of the Program Tape. Placing the ERASE Switch off and the TAPE PREP. switch on and executing the utility verb for writing, the tape will start in the forward motion out of BOT and assemble the ID's when the tape is up to speed. After 1024 transfers take place, the ACM control will sense EOBANK and reset CONOUT, stopping the tape motion. The tape will now be somewhere beyond COT, and the Data side will contain some Program Tape ID's which now must be erased. If the Data Tape is to be preserved, the writing may be prematurely terminated by switching the TAPE PREP. switch to off when the tape enters the COT window.

Preparation of the Data Tape is performed by transferring the appropriate tape ID Table to the AGC and proceeding in the same manner with the following exception: By starting in the COT window, the tape will first reverse looking for an ID. If the ACM is made to think that the tape is in BOT, a GOFWD command will be issued initially without the reversal and the tape will proceed as before. Grounding pin M2/45 on module CO5 will satisfy the above situation. The entries for the writing verb are as follows:

a. ID to be found -- any ID will do because TRNSIP is set immediately upon tape coming up to speed.
b. writing mode -- Triplex.
c. banks to-be-transferred-one, from Tape bank 1 MU5.

After the ID's are assembled on tape, to preserve the program and tables still in MU4, now transfer the banks in MU4 to banks in MU5 and write them back on the tape.

This now brings us to the next part of this appendix which deals with writing on the program tape.

To load the Program Tape with a series of records (for example, the routines used in the demonstration tests), the following changes must be patched into the supervisor programs. These changes bypass certain software interlocks.

Bank	Address	Modified Content	Check Being Bypassed
FF 03	6742	06762	Compares Bit 3 of ID to be writen with Bit 9 of CONOUT
FF 03	6246	06270	Assumption that PI operation is always reading

After these patches have been installed, a previously prepared PAC tape containing the desired programs should be read into PAC (AGC Fixed) Memory. The utility verb (VERB 00) may be used to perform a bank-to-bank transfer into MU5 of the PAC bank(s) to be placed on the tape. This function must be repeated once per bank to be transferred to MU5.

The load erasable function of Verb 00 may now be used if necessary to store the appropriate ID word into location 2000 of each ACM bank to be written (up to 4 for multi-bank transfers). This is not required if the PAC tape records contain the appropriate ID words.

The write tape function of Verb 00 is now used to perform the actual writing. MU5 is now loaded with the next records from PAC via the bank-to-bank transfer function of Verb 00; the process continues until all the desired programs have been loaded on the Program Tape in the prescribed locations.

APPENDIX F

UTILITY VERB

The utility verb, Verb 00, is able to perform the following functions with all inputs via the DSKY:

a. Read any fixed address (ACM, AGC, or PAC)
b. Transfer control to any fixed address
c. Read any erasable address (ACM or AGC)
d. Transfer control to any erasable address
e. Load any erasable address
f. Read the ATM tape (up to 4-bank transfer)
g. Write onto the ATM tape (up to 4-bank transfer)
h. Transfer any fixed bank to a bank in the ACM
i. Perform a word-for-word comparison between any two fixed banks.

The procedure for the use of the utility verb is outlined in Table F-1.

Note: Functions c, d, e and h all assume that the GSE switch is up on the Control Panel when EBanks in MU 2, 3 and half of MU 4 (Banks 40 - 107) are being addressed.

Verb 00 (all functions) loads FEXT with 6. To address MU 2 or MU 3, FEXT must be loaded with 5; this requires that location 6110 in bank 03 of fixed-fixed memory be loaded with (00120) via the PAC data entry switches.

TABLE F-1

PROCEDURE FOR USE OF VERB 0 0

FUNCTION	DSKY INPUT
Read fixed	V 0 0 E 0 XXX(FB) XXXX (ADDRESS) Y (1-7)
Transfer control to fixed	V 0 0 E 0 XXX(FB) XXXX (ADDRESS) X (0)
Read erasable	V 0 0 E 1 XXX(EB) XXXX (ADDRESS) Y (1-7)
Transfer control to erasable	V 0 0 E 1 XXX(EB) XXXX (ADDRESS) X (0)
Load erasable	V 0 0 E 2 XXX(EB) XXXX (ADDRESS) YYYYY(Data) Y (0-7)
Read tape	V 0 0 E 3 XXXXX(IDSTART) X (MODE)* X (no. of banks) E
Write tape	V 0 0 E 4 XXXXX(IDSTART) X (MODE)* X (no. of banks) X (1st TB) E
Bank to bank transfer	V 0 0 E 5 XX(FB) XXX (1st EB) E
Word for word check	V 0 0 E 6 XX(FB) XX (FB) E

*MODE 0 - TRIPLEX 1-7 - SIMPLEX

V - VERB 0-6 - 0-6 Y - digit (repeatable,
E - ENTER X - digit (non-repeatable) increments address)

Functions a through d

For purposes of discussion, the first four functions of Verb 00 may be combined; these functions, a through d above, are all executed with the same format. In order to use the utility verb, the verb must be selected by hitting VERB, 0, 0, ENTER on the DSKY. The next DSKY input is a 0 to read a fixed address or transfer control to a fixed address (function a or b), or a 1 to read an erasable address or transfer control to an erasable address (functions c or d). Next the bank number is put in as a three digit number for fixed (0XX) or erasable (XXX) bank numbers. After the bank number, a five digit address is put into the DSKY. In order to execute the specified operation, any digit from 1 to 7 is put in for a read operation. Before the operation is performed, DSKY display register R1 should be checked for the correct data to be stored in the Both Bank Register (BBK); R2 should be checked for the correct address to be read or transferred to by the program. If the operation was a read, the last digit may be repeated and will cause a read on the previous address, incremented by one. This procedure may be repeated until the end of the bank is reached. The data is displayed in R3 of the DSKY. Digit 0 is used when transferring control.

Function e

Load erasable is the next function which may be performed by the utility verb. Once the utility verb is selected by hitting VERB, 0, 0, ENTER, a 2 must be hit to select the "load erasable" feature. Next the erasable bank number is put in as a three digit number. After the bank number, a five digit

erasable address is put into the DSKY. The address is followed by the five digits of data to be loaded. In order to execute the operation, any digit from 0 to 7 is hit, but before the operation is performed, R1 should be checked to have the correct data for loading the Both Bank Registers (BBK); R2 should be checked for the correct data to be loaded. When the operation is executed, R1 will be changed to contain the data and will be the same as R3. R1 is the new data that has been read back after loading. The next consecutive address may be loaded by hitting another five digits of data to be loaded, followed by any digit from 0 to 7. This procedure may be repeated until the end of the bank is reached. The displays will continue in the same manner as when the first address was loaded.

Function f

The read ATM tape function is selected by hitting VERB, 0, 0, ENTER, 3. The next input is the 5 digit ID of the first record to be read. After the ID is entered, the mode, simplex or triplex, is indicated by hitting a 0 for triplex or any digit from 1 to 7 for simplex; this information is used to set bit 9 of CONOUT although this bit is not required for a read tape operation. See Section 3.2.4. The number of banks to be read, a number from 1 to 4, is entered. R1, R2 and R3 should now be checked to display IDSTART, IDSTOP, and CONOUT respectively. If the displayed data is correct, ENTER must be hit to execute the read tape operation. If a tape error occurs during the transfer, the same error indication will be displayed as in the demonstration tests (Section IV of Appendix G). Upon completion of a successful transfer, all 7's will be displayed in NOUN, R1, R2 and R3. Prior to

attempting to use the Write ATM function, location 2000 of every bank to be transferred must contain the ID word by which the bank is to be retrieved. Function e should be used for loading the ID's.

Function g

The write ATM tape function is selected by hitting VERB, 0, 0, ENTER, 4. The next input is the 5 digit ID (or File Marker)presently on the tape, after which the record is written. After the ID (or File Marker) is entered, the mode, simplex or triplex, is entered by hitting a 0 for triplex or any digit from 1 to 7 for simplex. The number of banks to be written, a number from 1 to 4, is entered. The number of the first tape bank (within MU 5) to be written is entered next; this is a number from 0 to 3. R1, R2, and R3 should now be checked to display IDSTART, IDSTOP, and CONOUT respectively. If the displayed data is correct, ENTER must be hit to execute the write tape operation. If a tape error occurs during the transfer, an error indication will be displayed as described in Section IV of Appendix G. Upon completion of a successful transfer all 7's will be displayed in NOUN, R1, R2, and R3.

Function h

The transfer of a bank to another bank is designed to transfer from any fixed bank (AGC, PAC, or ACM) to any ACM fixed bank. The bank being loaded must be addressed as erasable. If the transfer is to an ACM fixed bank for which the corresponding erasable bank numbers are XX0 through XX3, the first 10_8 locations are not loaded. See Table 2-3. The first 10_8 locations are not loaded in E banks ending in zero due to the Address Overlap feature; See Section 3.1.2. If the transfer is to an ACM

fixed bank for which the corresponding erasable bank numbers are XX4 through XX7, all 1024 locations in the bank are loaded. The bank to bank transfer function is selected by hitting VERB, 0, 0 ENTER, 5. The next input is the 2 digit fixed bank number corresponding to the bank from which the data is being transferred. After the fixed bank number, the 3 digit erasable bank number is entered corresponding to the first erasable bank in the fixed bank being loaded. ENTER will initiate the transfer.

Upon completion of a successful transfer, all 7's will be displayed in NOUN, R1, R2, and R3.

Function i

The word for word comparison of any two fixed banks is selected by entering VERB, 0, 0, ENTER, 6 on the DSKY. Next the fixed bank numbers are both loaded as 2 digits each. To execute the comparison, ENTER is hit. If the data in corresponding addresses does not agree, the DSKY will briefly display 56 in NOUN, the fixed address in R1, and the two non-agreeing data words in R2 and R3 for each disagreement. At the completion of the comparison, the DSKY will continue to display the last disagreement if any, or all 7's in NOUN, R1, R2, and R3 if no disagreements occurred.

APPENDIX G

DISPLAY AND I. D. INFORMATION

As was indicated, the verb sub-programs in the demonstration tests employ the DSKY to display information. This appendix lists the information which is displayed and the identification information used by the tape transfer subroutine in those programs which involve ACM and ATM data transfer.

During execution of the demonstration programs the two digit VERB register of the DSKY is always used to indicate which verb is being executed. The two digit PROG register on the DSKY is used to indicate the status of the AM.

ACM and ATM on = 11
ACM on only = 10
ACM off = 00

This display is updated during the idle loop.

The other four (4) registers of the DSKY - NOUN, R1, R2, and R3 are used as indicated below:

I. During VERB Execution

VERB	NOUN	R1	R2	R3
01 to 05	Blank	Blank	Blank	Blank
06 - 07	Blank	Cycling	Cycling	Cycling
08 to 16	Blank	Blank	Blank	Blank
17	Blank	FB-REG	Address (every 100)	Blank
18 to 22	Blank	Blank	Blank	Blank

II. Upon Successful Completion of VERB

VERB	NOUN	R1	R2	R3
01 to 07	7's	7's	7's	7's
08	64 or 67	CH21	CONOUT	CONIN
09	7's	7's	7's	7's
10	7's	Correctable Error Count (17)	7's	7's
11 - 12	(Same as Tape Transfer Error 64 or 67)			
13	(Same as Tape Transfer Error 70)			
14 to 17	7's	7's	7's	7's
18	(Same as GOJAM 4 with TC TRAP LIGHT on)			
19	(Same as GOJAM 4 with RUPTLOC LIGHT on)			
20	(Same as GOJAM 4 with NIGHT WATCHMAN LIGHT on)			
21 - 22	7's	7's	7's	7's

III. Error Indicators Other Than Tape Transfer Errors and GOJAMS

VERB	NOUN	R1	R2	R3	REASON
01	01	Blank	CONOUT	CONIN	CONOUT ≠ 20010*
	02	Blank	CONOUT	CONIN	CONIN ≠ 00000
	03	Blank	CONOUT	CONIN	CONOUT ≠ 74000*
02	01	Blank	CONOUT	CONIN	CONOUT ≠ 20010*
	02	Blank	CONOUT	CONIN	CONIN ≠ 00000
03	Blank	Blank	CONOUT	CONIN	CONOUT ≠ 00000
04	Blank	Blank	CONOUT	CONIN	CONOUT ≠ 20010*

VERB	NOUN	R1	R2	R3	REASON
05	Blank	Blank	CONOUT	CONIN	CONOUT ≠ 60000*
06 to 13	Blank	Blank	Blank	Blank	This error impossible
14 to 16,22	56	Address	ACM-Data	PAC-Data	ACM≠PAC
	57	Address	CONOUT	CONIN	ACM did not clear
17 to 21	Blank	Blank	Blank	Blank	This error impossible

* Bits 5 and 6 ignored.

IV. Tape Transfer Errors

CONOUT Displayed in R2 - CONIN Displayed in R3

NOUN	R1	REASON FOR ERROR
61	Overflow	Overflow part of sumcheck incorrect.
62	Sum	Sumcheck incorrect.
63	IDREAD	After both TRNSIP and GOATM disappeared, an abort was detected.
64	IDREAD*	Abort detected after TRNSIP was up.
65	IDREAD	Data transfer has not ended after 16 sec.
66	ID of bank	IDSTART greater than ID of bank or ID does not agree with CONOUT
67	IDREAD*	After both GOATM and TRNSIP up, one went down.
70	IDREAD	Abort detected before TRNSIP detected.

NOUN	R1	REASON FOR ERROR
71	IDREAD	TRNSIP not up 7 min. after GOATM.
72	IDREAD	CONOUT did not load correctly.
73	IDREAD	CONIN not zero.
74	IDREAD	CONOUT did not verify.
75	IDSTART	IDSTART did not verify.
76	IDSTOP	IDSTOP did not verify.

*See V08 Success Display

V. GOJAMS CONOUT Displayed in R2 - CONIN Displayed in R3

GOJAMS	NOUN	R1	REASON FOR GOJAM
1	AM-REQ	1111 X	E Parity
2	AM-REQ	2222 X	F Parity
3	AM-REQ	3333 X	Echo Check
4	AM-REQ	4444 X	AGC
5	AM-REQ	5555 X	STUCK 1
6	AM-REQ	6666 X	AGC or STUCK 1

AM-REQ = 01 = ACM requested on
AM-REQ = 10 = ACM on
AM=REQ = 00 = ACM off and not requested on

The last digit of R1 indicates the state of the OUTCOM bit immediately after GOJAM. It should always be a zero.

Verbs 06 to 16, 21, and 22 use the following data for loading IDSTART, IDSTOP, and CONOUT; or for writing new records on tape.

VERB	IDSTART	ID WRITTEN	IDSTOP	CONOUT
06	00024		00000	02000
07	04025		00000	02000
08	10026		00000	02000
09	14124		00030	02000
10	20024		00000	02000
11	24025		00000	02000
12	30026		00000	02000
13	34127		00000	02000
14	40001	41001	00006	03000
	41001		00000	02000
15	50000	51005	00006	03400
	51005		00000	02000
16	40001	41000,1,2,3	00000	03000
	40001	41001	00006	03000
	41001		00000	02000
21	14020		00024	02000
22	51005	51010,1,2,3	00000	03000
	51010			