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FINAL REPORT

THE INTERRELATION OF PROCESS TECHNIQUES AND SPACE RADIATION EFFECTS IN METAL-INSULATOR-SEMICONDUCTOR STRUCTURES

21 APRIL 1966 THROUGH 31 JULY 1967

CONTRACT NO. NAS5-10177

Prepared by

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NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND 20771

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PREFACE

This project was carried out at the David Sarnoff Research Center under the supervision of Mr. Martin Wolf, Manager, Physical Research Laboratory of the RCA Astro-Electronics Division, with assistance from Mr. Paul Rappaport, Associate Director, Materials Research Laboratory of RCA Laboratories. Technical supervision for NASA was by Messrs. Phillip Newman and Harry Wannemacher, Jr. (Technical Project Monitor) of the Radiation Effects Group, NASA Goddard Space Flight Center (Manager, Mr. Frederick Gordon). Other RCA personnel whose assistance is acknowledged are Mr. H. Harmon of Reliability Engineering, RCA Astro-Electronics Division, Hightstown, New Jersey (Manager, Mr. J. Kimmel) who assisted with some measurements; Messrs. C. Hanchett and P. Gardner of the Advanced Devices Group, RCA Electronic Components, Somerville, New Jersey, (Manager, Dr. R. Glicksman), who supplied samples of developmental ("Pattern 7") transistors and oxidized silicon wafers; Mr. T. Athanas, of Semiconductor Components Applications (MOS) of the same division (Manager, Dr. H. Veloric), who supplied samples of production transistors; and Dr. W. Kern and Mr. W. Schilp of the Process Research and Development Laboratory, RCA Laboratories (Director, Mr. G. Herzog), who supplied samples of chemically deposited insulators.

ABSTRACT

To find out how to minimize radiation sensitivity in MOS transistors, a study was made on the interrelation between sensitivity to space radiation in MOS devices and the method of fabricating the gate oxide film of these devices. Both MOS capacitors and transistors were studied using automatic plotting of capacitance-voltage and channel current-gate voltage characteristics. For both types of device, the oxides studied were fabricated under varied but closely controlled conditions. Both special laboratory furnaces and production types of furnace were used for oxide growth. A key item in the work was a controlled experiment in which the addition of phosphorus to the MOS insulator layer led to a true "radiation hardening". Radiation sensitivity is manifested as a negative shift in C-V and I-V characteristics. The main conclusions of the project were as follows:

(1) The gate oxide process technique used can change the sensitivity of MOS structures to high-energy radiation by an order of magnitude.

(2) The reproducibility of the degree of sensitivity to radiation is greater when steam-growth of oxides is used, rather than dry-oxygen growth.

(3) In general, the nearer the pre-irradiation C-V characteristic of an MIS insulator is to the ideal (charge-free) characteristic, the less sensitive is the MIS device to radiation.

(4) The coating of thermal oxides with a phosphosilicate layer appears to affect favorably the sensitivity of the resultant MOS device to radiation. This result can be described as a true "radiation-hardening".

(5) Several other process parameters can be ruled out as to their influence on radiation sensitivity.

(6) The present levels of radiation sensitivity in mass-produced devices can be improved by changes in process technique.

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I. INTRODUCTION

A. GENERAL

With increasing use of metal-oxide-semiconductor (MOS) transistors in satellite electronics, concern has arisen over the fact that virtually all the available varieties of MOS devices show a strong sensitivity to radiation arising from radiation-induced charges in the thin gate oxide layer[1]. In attempting to minimize this effect of radiation, it is clearly necessary to study first the basic character of the effect and, secondly, whether it can be minimized by some change in the oxide fabrication procedure or in the conditions under which the device is operated in satellite electronics.

The effect which is invariably observed in MOS devices when subjected to ionizing radiation is a shift in the capacitance-voltage (C-V_g) characteristic and/or the channel current-gate voltage (I_d-V_g) characteristic, along the voltage axis in the negative direction (Figure 1). This effect can be interpreted in terms of the trapping

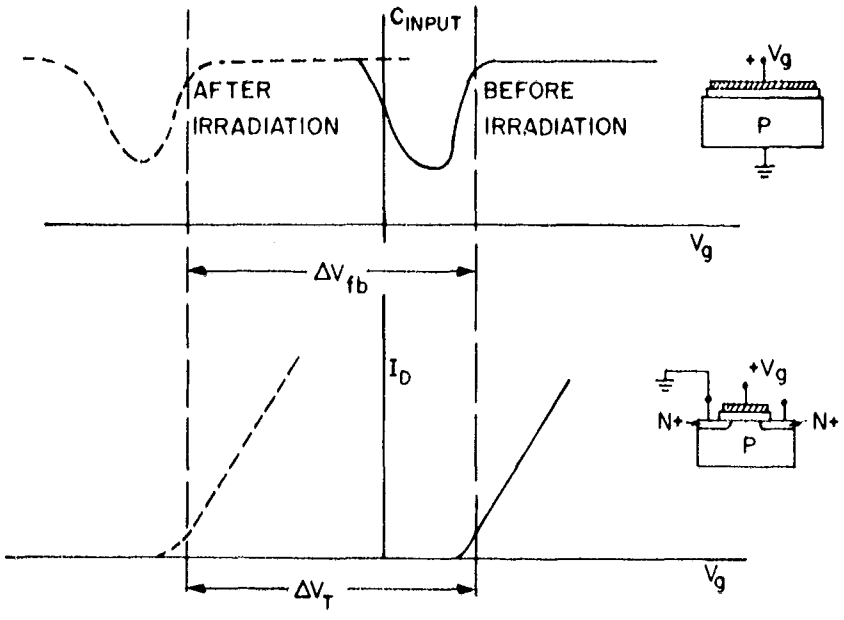

Figure 1. Changes in operating region of MOS device which are produced by ionizing radiation in the 10^4 to 10^6 rad absorbed dose region.

of holes (loss of electrons) in the insulator layer[2-4]. Thus, the degree of sensitivity of MOS devices to radiation should depend very strongly upon the defect structure of the oxide. The defect structure, in turn, should be strongly affected by the conditions under which the oxide is fabricated. For example, in the case of conventional MOS insulator layers, which are grown directly from the silicon by oxidation, it is to be expected that such variables as oxide growth rate, growth temperature, water-vapor concentration in the growth atmosphere, post-oxidation annealing temperatures, and annealing atmosphere should all be important in establishing the defect structure of the oxide.

The authors have thus undertaken a systematic investigation of the character of the radiation effect in MOS insulators and its variation throughout a wide range of fabrication conditions. At the same time, these conditions have been carefully characterized and have embraced the conditions likely to be found in practical high-performance MOS transistors used in space missions. Thus, the investigation has included not only tests of laboratory-grown oxides, where growth and contamination conditions can be varied at will, but also tests of oxides grown under device-development laboratory conditions and under MOS transistor production-line conditions.

B. BRIEF CHRONOLOGY OF RADIATION EFFECTS IN MOS AND MIS DEVICES

The effect of radiation on MOS devices was first noted by Hughes and Giroux[5]. This observation removed the earlier impression that, because surface-channel devices would not be affected by the production of minority-carrier recombination centers in the bulk silicon, they would be radiation resistant. Even though radiation-induced charge-trapping had long been recognized as the source of "color center" formation[6] in bulk silica and other insulators, it was not appreciated that similar effects would strongly influence the performance of MIS devices.

In early 1964, at about the same time that the MOS device data were obtained, unusual degradation effects were also observed in planar bipolar transistors under irradiation. Factual reports of this effect were made by Peden[7] and Peck and Schmid[8] in 1964. Clarifying experiments on the effect were made in late 1964 by Green et al.[9] and by Brucker, Dennehy, and Holmes-Siedle[10,11], which indicated that charge-trapping effects in the oxide were almost certainly the cause of the phenomena observed. These phenomena were strong changes in dc current gain and collector-base leakage current under ionizing radiation. It could be shown that the effect was a surface effect because it was produced by x-rays and by electrons of energy below the minimum needed for bulk silicon damage and because of the strong regular dependence of the gain degradation on injection level[11].

During 1965, Szedon and Sandor[12], Speth and Fang[13], Messenger et al.[14], Kooi[15], and Hughes[16] produced data on MOS devices which indicated that oxide charge buildup was clearly involved in radiation effects in grown oxides and that fields in the oxide during irradiation were vitally important in determining the amount of charge trapped. Zaininger's publication[17] of capacitor measurements gave the first evidence that a well-defined hole-trapping effect was involved and was accompanied by variable amounts of interface state production[18].

In 1966, Snow and coworkers[19] and Kooi[20] published confirmatory capacitor data; evidence was produced for strong interface state production in transistors by Dennehy and coworkers[21]; and studies of the practical aspects of the use of MIS devices under radiation were made by Gordon and Wannemacher[22] and Barry and Page[23]. New aspects of bias dependence of radiation-induced shifts on MOS and MIS devices were reported by Stanley[24]. At present, several more profound studies of mechanisms and process effects are in progress, with new techniques such as measurement of oxide charging currents[25,26], probing with fine electron beams of varied energy[27], and preparation and irradiation of high-purity samples of MOS structures, as in the project to be reported here.

The overall conclusion is that the production of significant amounts of trapped charge in the oxide is universal, while other effects, such as interface-state production, instability, and leakage, may or may not occur, depending on oxide structure.

C. RELATION OF OXIDE CHARGE AND VOLTAGE SHIFT

A relation which is used very extensively in this report will be explained briefly here. In an MOS device, either capacitor or transistor, the trapping of fixed charge in the oxide leads to a parallel shift in the drain-current vs. gate voltage or capacitance vs. gate voltage characteristic which is proportional to the amount of charge deposited. Thick oxides give larger shifts than thin oxides, the effect being inversely proportional to oxide thickness d_i. The following relation may be used to calculate charge density ΔN_{ss} from voltage shift (ΔV):

$$\Delta N_{ss} = 2.11 \times 10^{10}\left(\frac{\Delta V}{d_i}\right) \qquad (1)$$

where d_i is in microns. It is thus seen that, for d = 0.211 micron or 2110 Å, a fairly common thickness, a negative 1-V shift corresponds to

a positive charge density of $10^{11}/cm^2$, 10 V correspond to $10^{12}/cm^2$, etc. Two factors may modify this simple relation of fixed charge to shift; (1) If the charge is not within a few hundred angstroms of the silicon; (2) if the charge can exchange with the silicon, i.e., lies in interface states.

D. SPACE RADIATION LEVELS

The radiation conditions under which active semiconductors usually have to operate in space is very low-rate particle and Bremsstrahlung irradiation. For most orbits of importance, integrated dose levels are usually less than a megarad in magnitude. The only exceptions would be circular orbits matched precisely with the heart of the inner Van Allen belts, i.e., 1500 to 2500 miles altitude at low inclination to the plane of the geomagnetic equator. These orbits are not of strong operational interest.

A typical heavily used orbit with fairly high radiation fluxes is that being used by operational weather satellites, e.g., ESSA II and TIROS M (a 750 naut. mile altitude circular orbit of inclination 82° to the geographic equator).

Electronic devices such as transistors will usually be enclosed by the equivalent of 0.1 in. of aluminum or more. Estimates for ESSA II in the 1968-75 era are that, with the anticipated thicknesses of structural elements and packages, annual particle fluxes inside electronic packages will not impart ionization doses of more than 3×10^5 rads in the more exposed locations. A repetition of the enhancements in trapped electron flux experienced after the "Starfish" hydrogen bomb explosion could, of course, increase these ionization doses by a large factor and require extra shielding thicknesses (say 0.2 in. aluminum) to keep ionization doses in the ranges now anticipated.

It is thus assumed that the important radiation levels which should be considered in a study of the usefulness of MOS devices in space are 10^3 to 10^6 rads. It seems certain from all work to date that atom displacement damage does not play a major part in degrading MOS devices at the particle flux-levels anticipated; and, hence, all particles can be equated by normalizing factors which convert particle fluence to absorbed dose (e.g., 3×10^7 1-MeV electrons/cm^2 ≡ 1 rad (SiO_2) ≡ 10^6 10-MeV protons/cm^2).

Some assumptions are made in this report about the significance of dose rate when attempting to simulate space radiation effects in the laboratory. Several workers have determined that, for a wide variety of MOS device types, most of the positive charge deposited

remains firmly trapped in the oxide for months or years. Although no definitive experiments have been performed at a typical operational space dose rate, (usually less 10 rads per hour), no strong dose-rate dependence of the radiation effect has yet been observed in the laboratory. On the other hand, in a few types of device, a partial recovery of radiation-induced shifts is observed within a few weeks of the irradiation of an MOS transistor. In these latter cases, measurement of the device immediately after irradiation at a dose rate several thousand times that encountered in space would give a somewhat pessimistic answer as to the performance of that device in orbit after the same total dosage level had been reached. It still appears, however, that the major hazard to MOS devices in space radiation is the permanently induced, firmly "frozen" charge buildup which would not be subject to dose rate effects. Thus, in a study such as the present one, which has the main purposes of placing various process variables in order of merit in producing radiation resistance it is considered valid to perform irradiations at the usual laboratory rates (10^4 rad/sec or higher) which are, in any case, demanded by the time constraints of the project. An experiment which had the objective of accurate prediction of shifts to be encountered for a given device in a given orbit might, on the other hand, requires slower irradiation rates.

II. PHYSICS OF THE MIS SYSTEM AND MEASUREMENT CONSIDERATIONS

A. GENERAL COMMENTS ON SOLID-SOLID INTERFACES

An MIS structure consists of a semiconductor substrate covered by an insulator layer (between 50 Å and 5000 Å thick) upon which a metal electrode (gate) is deposited. Early work on semiconductor surfaces was mainly concerned with the semiconductor-vacuum and semiconductor-gas systems[28]. In the latter, fortuitous room-temperature air oxidation normally produced a 30 to 50-Å-thick oxide film that was considered part of the surface region. This could thus be regarded as a narrow region of discontinuity between the two media. The physics of such surfaces was reasonably well understood, and the localized electronic states associated with the surface region were called surface states. A distinction was made between fast and slow surface states, i.e., between states that could exchange charge with the semiconductor space-charge region rapidly or slowly, respectively. The slow states were generally thought to be at the outside of the oxide film, and the fast ones right at the boundary between the semiconductor and the oxide layer.

MIS physics is a natural extension of semiconductor surface physics into a system of two solid-solid interfaces separated by an insulating film whose thickness is no longer negligible. Because of the presence of this film and its two surface space-charge regions, MIS physics is more complicated than semiconductor surface physics[29]. Depending on the ratio of the insulator thickness to the extent of the space-charge regions, three different situations may arise.

(1) If this ratio is very large, then there is no interaction between the metal-insulator and insulator-semiconductor interface regions, and the voltage drops linearly across the oxide except in the two (relatively small) surface space-charge regions. This is the condition usually assumed but rarely justified in device calculations.

(2) If the ratio is in the order of unity, then the two surface regions in the oxide begin to interact. In this case the two interfaces cannot be separated, and the voltage profile is a complicated function of all the parameters involved.

(3) For a ratio much smaller than unity, the integrated space charge in the oxide can be neglected with respect to the surface charge in the metal, resulting in a linear voltage variation through the oxide film. The silicon surface potential in this case is essentially determined by the interaction between the metal and the silicon, and by the density of states at the interface.

The concepts and terminology used are mostly inherited from semiconductor surface physics dealing with a semiconductor-gas system. Thus, for example, the simple distinction between fast and slow surface states is not applicable in an MIS system. However, because of the widespread use of the term "surface states" we have retained this expression, but use it in an operational manner. In this usage, the term "effective surface states" lumps together the effect of work-function difference and both the charge configurations that can be defined for the MIS system, namely, interface states and oxide charge.

B. CHARGE RELATIONS IN THE MIS SYSTEM

The charge neutrality of an MIS system is frequently expressed as

$$Q_{ss} + Q_{sc} + Q_M = 0, \tag{2}$$

where Q_{ss}, Q_{sc}, and Q_M indicate charges in the effective surface states, semiconductor space-charge region, and metal electrode, respectively. In reality these quantities represent effective charges with considerable complexity as regards their distribution and energetics of formation[30]. Charge-exchange equilibria exist between each region, and several different types of charge can be distinguished within the insulator phase itself. A clear experimental separation of the charge in the effective surface states into its components, including their polarity, is difficult. Each measurement method can only distinguish between certain kinds of charge and, thus, classifications depend to a large extent on the method of measurement employed. Since high-frequency ($\sim$ 1 MHz) C-V measurements are relatively easily and rapidly carried out[31], and since it has been shown[32-33] that they can yield interesting, meaningful results if the proper experimental conditions are established and if care is taken in their interpretation, it is advantageous to classify the surface states in the MIS system on the basis of this measurement method. Thus, we have the following two categories.

(1) Interface states are stationary electronic states located right at the (Gibbsian) plane separating the semiconductor from the insulator. Interface states are analogous to the fast surface states mentioned above. Because the insulator has a wide forbidden gap, the energy levels of interface states can lie either within or outside the forbidden gap of the semiconductor. This will determine whether or not they change their charge state when a field is applied between metal and semiconductor.

(2) Oxide charge is charge that is trapped in the space-charge region of the insulator film and cannot communicate with the semiconductor surface. There are two forms of this charge, namely, mobile and immobile.

The immobile species is mainly held in traps that are part of the intrinsic defect structure of the insulator; the mobile charge is mostly due to ions that are capable of migrating through the insulator, especially during conditions of high field and elevated temperature.

C. MEASUREMENT METHODS

Several measurement methods are available that give certain distinctions between the various types of charge in the MIS system.

1. The High-Frequency MIS Capacitance (C-V) Method

The small-signal differential admittance of an ideal MIS capacitor with no surface states consists of the insulator capacitance, C_i, in series with the surface space-charge layer capacitance, C_{sc}[34-38]. C_i is independent of frequency. C_{sc} also is independent of frequency in the accumulation and depletion regimes (up to 10^{11} Hz), but in the inversion regime, C_{sc} takes on different forms depending on whether or not the minority carriers can follow the applied ac signal and/or bias. The dependence of this ideal MIS capacitance on effective bias is shown in Figure 2(a) for the case of a metal - SiO_2 - Si structure. In all cases, this capacitance is uniquely determined by the semiconductor surface potential, ψ_s. For an actual MIS diode in which surface states are present but in which loss mechanisms are neglected, the above equivalent circuit is modified by adding the surface state capacitance, C_{ss}, in parallel with C_{sc}. The dependence of C_{ss} on frequency and surface potential is a function of the density of surface states and their spatial and energy distribution[39]. Since this is, in general, not known, little information about the physical properties of the interface can be obtained from an analysis of the MIS C-V characteristics obtained at an arbitrary frequency. However, if the measurement frequency is sufficiently high so that surface states cannot follow, then the surface-state capacitance becomes zero and the MIS capacitance reduces to its high-frequency form, i.e., the series combination of C_i and C_{sc}. When this condition is satisfied, the MIS capacitance is unambiguously related to the semiconductor surface potential. However, there is a difference between an experimentally determined high-frequency C-V characteristic and one computed for an identical structure without surface states, and this is the voltage due to the total charge in surface states. By finding the difference, ΔV, between the measured voltage for a given capacitance value, say the "flat-band" capacitance, and its "ideal" value, one can determine the total charge that is trapped in surface states as a function of surface potential. The density of effective surface states for any particular value of capacitance, as reflected to the insulator-semiconductor interface, N_{ss}, is then given by

$$\Delta N_{ss} = \frac{C_{ox}}{q} \Delta V = \frac{\varepsilon_o K_i}{q\, d_i} \Delta V \qquad (3)$$

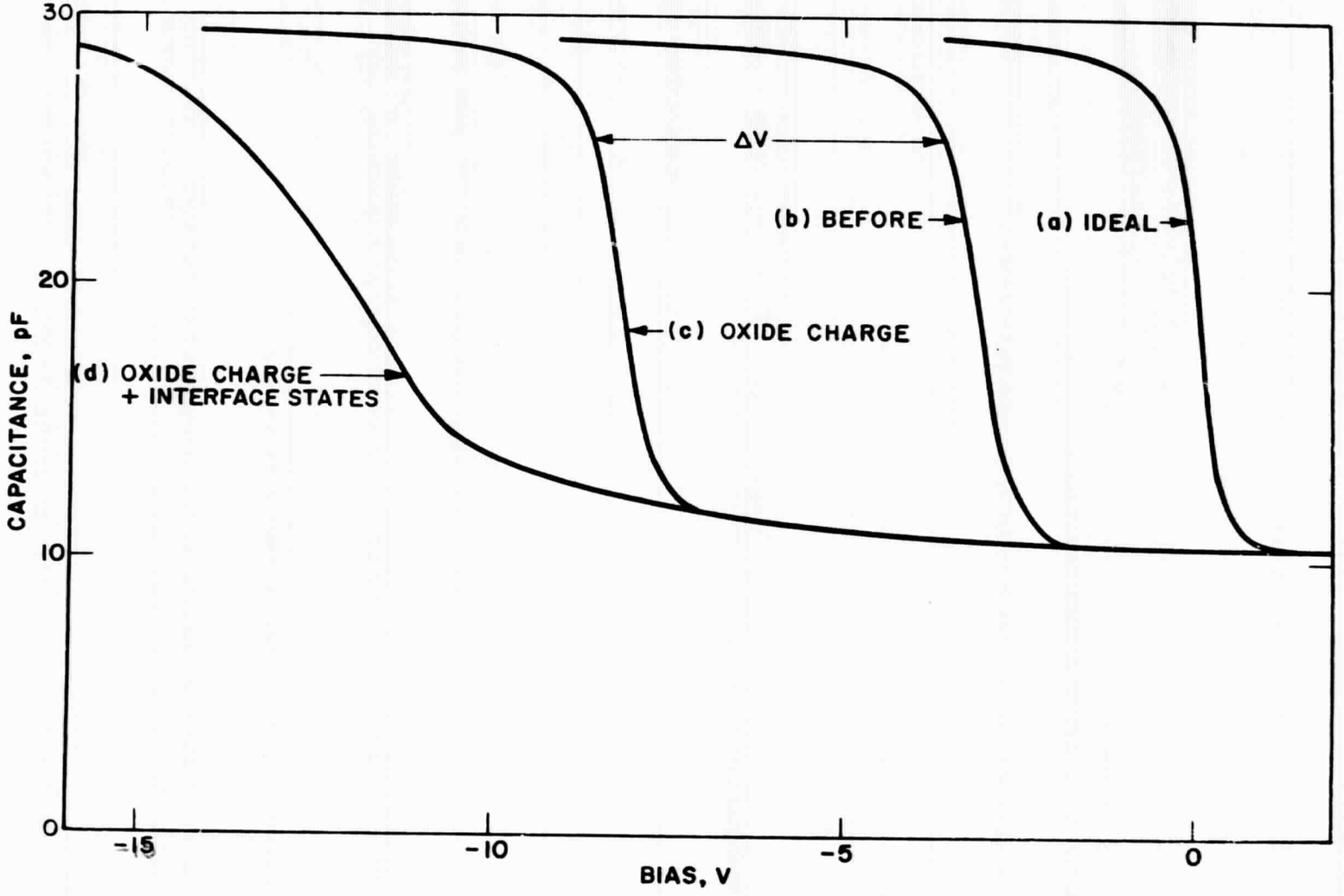

Figure 2. Typical MIS capacitance vs. bias characteristics for 10-ohm-cm p-type silicon with 0.010-in. nickel gates deposited on a 0.1-μm grown silicon dioxide film.

where C_{ox} is the insulator capacitance per unit area, q is the elementary electronic charge, ΔV is the shift in the C-V characteristic along the voltage axis, ε_o is the free space permittivity, and K_i and d_i are the dielectric constant and thickness of the insulator, respectively. For grown silicon dioxide layers, this equation has constants as follows

$$\Delta N_{ss} \text{ (states/cm}^2\text{)} = 2.11 \times 10^{10} \Delta V/d_i \text{ (micrometers)}$$

If the experimental C-V curve is to the left of the ideal curve, the charge in surface states is positive; if it is to the right, the charge is negative.

2. The MIS Conductance (G-V) Method

The small-signal differential ac conductance, G, of an MIS diode is essentially due to the exchange of charge between interface states and the bulk semiconductor. If this conductance is measured as a function of bias and frequency, information concerning the density distribution, time-constants, and capture cross section of the interface states present can be obtained[40].

3. The Channel Conductivity (I_d-V_g) Method

The property of MIS devices most commonly made use of in electronics is the modulation of channel conductivity g by gate bias V_g. Drain-to-source current I_d is, of course, controlled by g,

$$g = \frac{I_d}{V_{ds}} = \frac{W\mu C}{L}\left(V_g - V_T - \frac{V_{ds}}{2}\right) , \qquad (4)$$

where V_{ds} is the drain-to-source voltage, V_g is gate voltage, V_T is "pinch-off" or threshold voltage (here taken as a negative quantity as in n-channel depletion devices), μ is the carrier mobility, C is the gate-to-substrate capacitance per unit area, L is the channel length (i.e., source-drain separation), and W is the channel width. As "pinch-off" is a gradual phenomenon, the definition of V_T must include a statement as to the channel current or conductivity value chosen to represent the threshold between the turned-on and pinched-off conditions.

Under certain conditions, measurements of the shift in threshold voltage (ΔV_T) induced in an MIS transistor by radiation can be used to determine the density of charge ΔQ newly introduced into the oxide. The introduction of positive charge into oxide states and interface states induces a balancing increase of negative conduction electrons in the channel. The product of C

and ΔV_T represents the amount of electronic charge that must be suppressed in the channel in order to bring the conductivity back to the defined threshold level.

Particular care is needed, however, in interpreting such data. Gate-source capacitance must be eliminated from C; it must be assumed that semiconductor doping is not changed by the irradiation; and V_{ds} must be small enough to be insignificant in Eq. (4). If new interface states are generated by the irradiation (and several experiments discussed later suggest that they frequently are), the shape of the I_d-V_g characteristic will be affected, since changing the bias may now cause emptying or filling of these states. Thus, the calculated value of fixed oxide charge density from I_d-V_g characteristics will contain an uncertainty equal to the density of interface states created. Despite these limitations, the I_d-V_g characteristic is of use for studying the inversion regime, while the C-V characteristic gives more unambiguous data concerning the accumulation and depletion regime.

D. MECHANISMS OF RADIATION-INDUCED CHARGE PRODUCTION

1. "Fixed" Oxide Charge

The parallel shift in electrical characteristics that occurs in MIS devices under radiation appears to be the most significant effect as well as the most amenable to analysis by virtue of the static nature of the charge configuration. The degree of parallel shift observed in MIS devices varies very widely with the nature of the insulator film. Indeed, for the normal-grown silicon dioxide layers, it will be seen that there is a striking dependence on the conditions used for the growth process. The degree of parallel shift is also very strongly dependent on the field applied across the oxide during the particle irradiation. In this report, the applied field is usually given in terms of the bias applied to the metallic gate of the device during irradiation, and is called the *irradiation bias*, V_I. Figure 3 is a generalized form of the behavior of those MIS devices that undergo virtually parallel shifts. The form shown is common to most of the data published and encourages the view that a common process occurs in most MIS devices.

Several features are worth noting. There is a strong dependence of the threshold-voltage shift (V_T) on irradiation bias, negative bias having a smaller effect than positive bias. At certain dose levels, saturation occurs, and this saturation level is higher under high bias. These features indicate that bias must have a strong effect on the permanent space-charge region produced in the oxide. The variability of this bias effect is indicated in Figure 4, which shows the dependence of voltage shift (converted to radiation-induced oxide charge density) on irradiation bias for four samples of oxide, which were grown at different times and in different

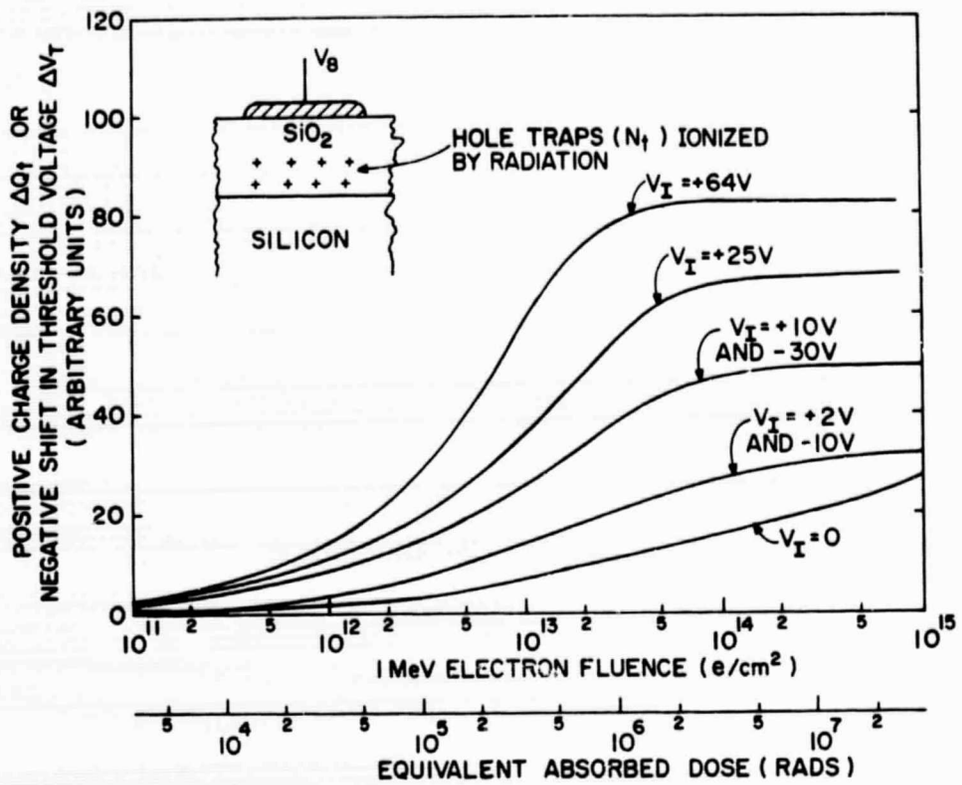

Figure 3. General form of shift in MIS characteristics as a function of integrated irradiation level. Gate bias during irradiation (V_I) is the parameter. The irradiation level is given in electron fluence and the equivalent dose in rads, absorbed from electrons.

atmospheres; and irradiated to 10^{13} 1-MeV electrons/cm^2. While the shapes of both quadrants are, in all cases, roughly parabolic, it appears that strong individual differences exist in the profile of space-charge per Å vs. depth in these oxides. In other words, the charge-trapping capabilities of the regions near each interface in which charge is trapped by radiation are, in some way, different in each oxide.

The fact that, at zero bias, positive charge is built up in the oxide despite the absence of field is of considerable interest. If the features of this radiation-sensitivity vs. dose characteristic can be interpreted correctly and are found to bear a predictable relation to the sensitivity of the same oxide irradiated under bias, then a very simple sensitivity test of oxides will be possible. It will be possible to test oxide layers for radiation-sensitivity without the previous deposition of a metal electrode (which brings with it possibilities of contamination and other oxide

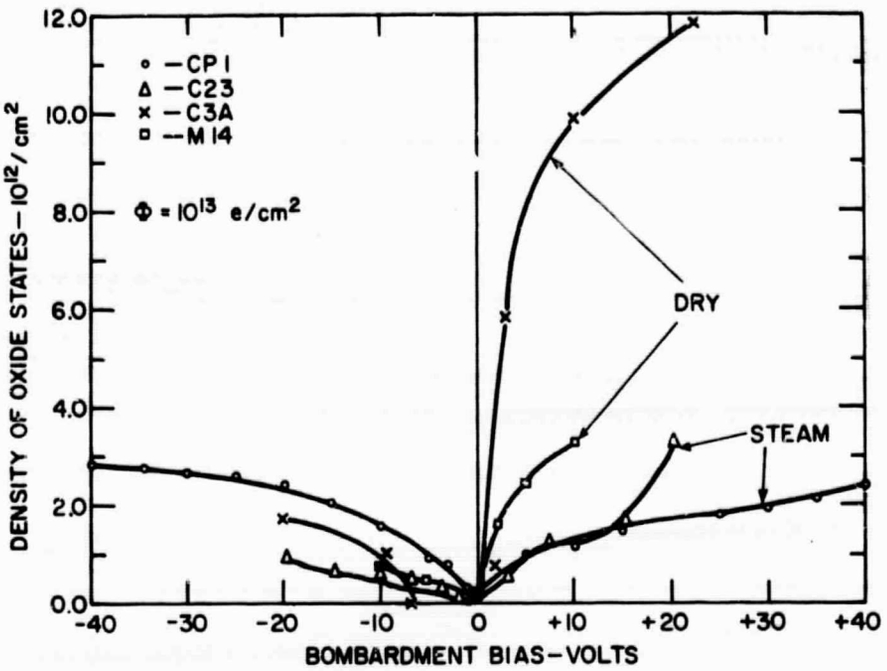

Figure 4. Radiation-induced shifts in MOS capacitor characteristics vs. irradiation bias, V_I, at a fluence of 10^{13} 1-MeV electrons/cm^2 (approx. 3 x 10^5 rads), for four different preparations of oxide. Shifts are normalized for thickness and expressed as oxide charge per cm^2.

stresses), while the need for the arrangement of biasing contact during irradiation, always inconvenient, will be removed.

Etching studies have thrown some light on the form of zero-irradiation bias characteristic. After zero-bias irradiation, almost all the positive charge is found within 100 Å of the Si-SiO_2 interface. This probably corresponds to the region from which radiation-excited electrons can diffuse from the oxide even in the absence of an applied bias.

The above observations have led to the physical model for fixed oxide charge production shown in Figure 5[1]. Radiation generates electron-hole pairs in the insulator which subsequently interact with trapping sites within the insulating film. The radiation-generated electrons either recombine with the holes or move out of the insulator. The radiation-generated holes may diffuse in the insulator, but are less mobile than the electrons; many stationary hole traps are also present. The result is the net positive charge profile shown on this model. The influence of irradiation bias on

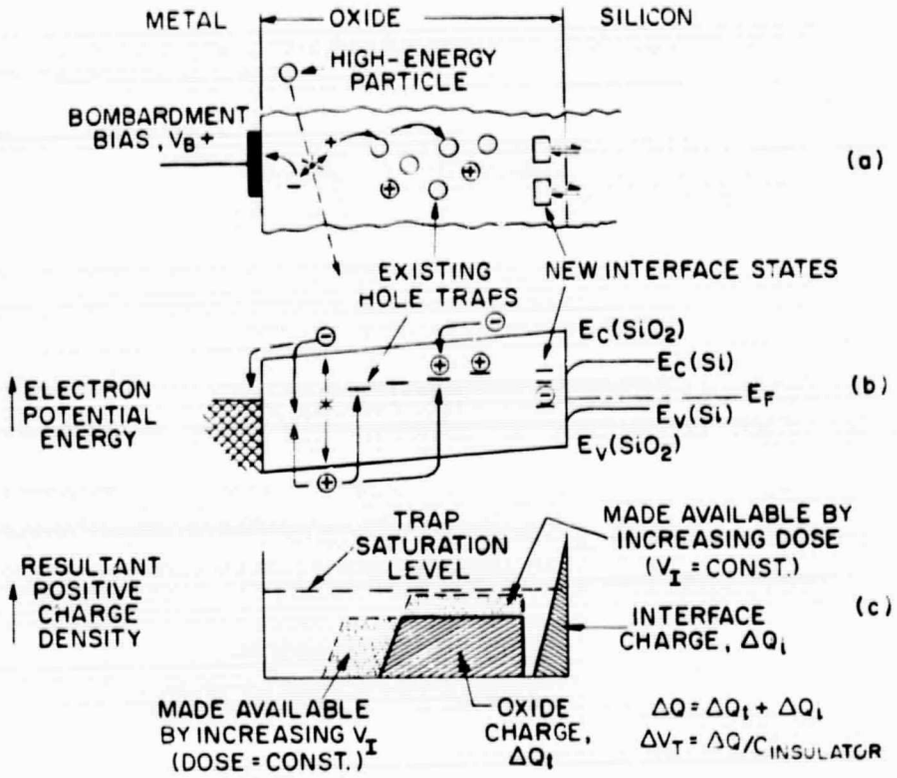

Figure 5. Model for the effect of high-energy radiation on MIS structures: (a) device cross section, (b) energy-band picture, and (c) oxide charge distribution.

the amount and location of the radiation-induced space charge is clear. If there is no electric field present in the insulator during irradiation, the major effect will be electron-hole recombination; only a relatively small number of holes will be trapped. If there is an electric field present, the electrons will readily move out of the insulator film, and the trapping of holes becomes significantly enhanced. Thus, a significant positive space-charge layer is built up at the insulator-semiconductor interface and moves into the insulator with continued irradiation. Most of this charge will be imaged in the semiconductor surface, and MIS measurements will show a large voltage shift.

If the gate is negative during irradiation, then in the simplest approximation one would expect the positive space-charge layer to be formed at the metal-insulator interface and to move into the insulator with continued irradiation. Most of the charge is imaged in the gate, and MIS

measurements will not show an effect until the width of the space-charge layer is a significant portion of the insulator film. This may account for the flat minimum seen in Figure 4 at low negative irradiation biases.

If, in addition to the capture of holes, a significant trapping of electrons takes place, or if the insulator is somewhat conductive (as is most probably the case for certain silicon nitride films), then no significant net space charge will be built up.

2. Interface States

The change in shape due to interface states shown in Figure 2(d) can be important in its effect on transistor operation, since a similar change in shape in the I_d-V_g characteristic corresponds to a reduction in gain. The generation of interface states by radiation is not well understood and varies from sample to sample less predictably than for fixed oxide charge.

The usual form, as shown in Figure 2(d), is the generation of a wide distribution of energy states throughout the silicon bandgap. This produces a smooth change in shape of the C-V or I_d-V_g characteristic. Occasionally, however, cases have been observed in which a defect is present that gives rise to a predominance of states concentrated around a single energy level. The states at this level appear to be enhanced by irradiation over and above the general background of other interface states at other energy levels. This leads to an unusual "stepped" characteristic which could cause unusual transistor characteristics[3].

In the early work on MOS capacitors, it was observed that the state of the silicon oxide interface before bombardment has a strong influence on the number of interface states produced by irradiation. A result like that of Figure 2(c) is produced if the degree of perfection of the interface is high. If, on the other hand, the original interface already has a high density of interface states, these states are usually enhanced. Most irradiations of mass-produced transistors involve some generation of distributed interface states, which are manifested as a change in the shape of the I_d-V_g curve and an increase in surface recombination velocity. In one experiment[21], a very strong generation of interface states actually reversed the direction of shift of the transfer characteristic of an n-channel transistor. In the experiment, the room-temperature transfer characteristic also became unstable under gate bias. The direction of the instability is such that if positive voltage is applied to the gate, the characteristic shifts toward more positive voltage; if negative voltage is applied, the shift is toward negative voltage. These shifts are opposite in direction to the temperature-bias instabilities observed in some devices, which are attributed to the motion of ionic species in the

oxide and occur only at elevated temperatures. The effect has, however, also been observed in unirradiated devices with large densities of interface states, such as many metal-silicon-nitride-silicon (MNS) devices. Kooi[15] also reported, but did not discuss, a slight instability of this kind in wet-oxygen-grown oxides irradiated by x-rays.

III. APPROACH IN PRESENT PROJECT

A. GENERAL APPROACH

The objective of the present work was to elucidate, by investigation of well-characterized metal-oxide-semiconductor (MOS) or other metal-characterized metal-insulator-semiconductor (MIS) devices, the reason for the degradation of MOS transistors under high-energy radiation such as that found in space; and to determine, in particular, how changes in the fabrication techniques used could affect this degradation. It was already well appreciated that another factor played an important role in the degree of degradation of MOS devices under radiation, namely the electric field strength and field direction in the oxide during irradiation. Since a satellite would be operating for all of its lifetime under low-rate radiation, the mode of operation of the device (enhancement vs. depletion, n- vs. p-channel, high vs. low logic voltages) during that time was also important in determining the best type of MIS device to use in satellite electronics.

It was realized that mass-produced MOS transistors were not ideal test vehicles for two reasons:

(1) Such devices are usually not well-defined as material systems; in mass-production semiconductor processing, little attention is paid to exact material compositions, especially with regard to trace impurities, so long as satisfactory device performance is achieved; in addition, the crucial gate insulator is frequently a layered structure.
(2) The presence of source and drain contacts, usually in geometrically complex configurations (see Figure 6, for example), introduces complexity in analyzing any electric-field effects observed and may also introduce extra impurities into the gate oxide region.

With this in mind, it was decided that, while it was important to evaluate the present state of the art in mass-production oxide technology and device geometry, detailed conclusions on the physics of radiation effects on MIS devices could only be obtained in cases where the investigators had full control over every step in the fabrication of the device. This is not a new situation in radiation effects research but the condition probably holds more strongly in the present case than in any known case to date. A close and truly analogous case is that of glasses, where small changes in composition and processing can affect the colorations produced by irradiation. There is, indeed, some likelihood that the effect of radiation on glasses and MOS insulators arises from the same

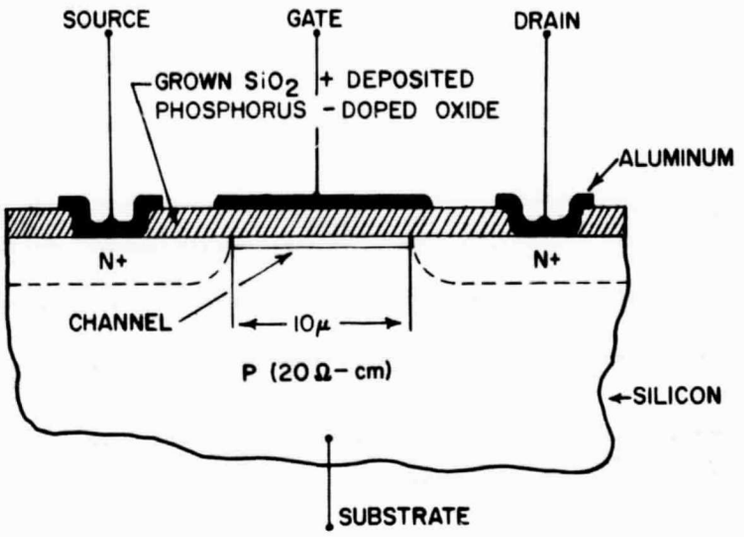

Figure 6. Structure of a typical high-performance MOS transistor.

cause, namely from positive charges (holes) trapped at interband defect levels between the valence and conduction band of the oxide structure.

It was thus accepted that there was a considerable gulf between the devices actually used in satellites and the ideal test device for physical studies, and it was decided that both classes of device would be studied and special efforts be made to bridge the gap between them. The basic list of devices given below was decided upon.

It should again be emphasized here that the data on oxide condition, which can be derived from C-V_g and I_d-V_g characteristics, are complementary. C-V data can be used to calculate interface state densities in the accumulation and depletion regions. In these regions, the channel is pinched off, and hence no information can be obtained from I_d-V_g characteristics. Conversely, the C-V technique is not useful in the inversion region because the frequency response of the inverted semiconductor space charge layer[41] is not simply determined; in this region, the MIS transistor is conducting and the variation of this channel conductance with bias can now be used to study interface states in the inversion region. Hence, the two methods can be combined to give information on the interface states throughout the bandgap. A particular example of this is discussed in the experimental section.

B. DEVICES STUDIED

1. Simple oxide films produced in steam and dry-oxygen furnaces used by RCA Laboratories' Electronic Research Laboratory or in other apparatus producing special insulating films, such as chemical vapor deposition reactors and anodizing chambers.

2. RCA "Pattern 7" transistors, a semi-integrated device of bar geometry suitable for the development of logic circuit designs, including complementary designs (see, for example, the recently released RCA TA 5361 complementary NOR gate and inverter combination). In this device, gate-substrate capacitance is small to allow for fast switching. The device is produced in a variety of forms as a part of the developmental work by RCA Electronic Components*. Complete details were available on small batches produced by this activity in very well-controlled furnaces.

3. Simple oxide films produced in the same furnaces as the above-mentioned two devices under the same processing conditions and passed on to the experimenters without further treatment for evaluation by the C-V technique.

4. Commercially available RCA TA 2578 transistors, which are designed for use in low-frequency amplification circuits. This device has a large gate-substrate capacitance and channel area and, hence, is suitable for comparative C-V and I_d-V_g measurements. Also, the gate is an enclosed structure and, hence, leakage effects should be minimized.

5. Other MOS transistors and arrays which had special properties likely to add information to the study (e.g., complementary MOS logic arrays and large-geometry transistors). The ability to evaluate unmodified films by the C-V technique and to obtain these from several different facilities was regarded as very important in the attempt to discover the important processing steps in determining radiation resistance.

C. MIS CAPACITOR SELECTION

One of the ways in which MOS capacitor study is particularly convenient is in the ability to study samples with known initial interface-state density. Oxides are grown on silicon wafers in conditions which give rise to very low interface-state density. Since the oxide thickness may be measured accurately by ellipsometry, the "ideal" C-V characteristic can be calculated and the interface-state density estimated by noting the deviation of shape from the ideal. In the present study, samples with high interface-state density were usually rejected.

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* Located at Somerville, N. J.

Preliminary observations[3] showed that samples with low interface-state density developed fewer additional interface-states under radiation. Thus, it was possible to find many samples in which interface-state production under irradiation could be neglected by comparison with the number of bulk oxide charges produced. This situation made it possible effectively to isolate, and to concentrate upon, the problem of bulk oxide charge in the present study.

The main processing parameters of the capacitor gate insulators to be varied were: crystallographic orientation of substrate, oxide growth atmosphere, growth temperature, post oxidation annealing temperature and atmosphere, and oxide thickness. As well as varying the above parameters for simple thermal silicon dioxide layers, some deposited insulators containing large amounts of dopant impurity were also to be studied for gross impurity effects.

D. MIS TRANSISTOR TEST VEHICLE CONSIDERATIONS

The MIS transistor is essentially an MIS capacitor in which contact to the semiconductor surface channel has been effected. "Active" operation of the device consists of control of the electric field at the surface of the semiconductor and consequent control of the density of charged carriers (electrons or holes) at this surface. It is, of course, still possible to measure capacitances, although with less accuracy than in a large-area capacitor. Figure 6 shows the construction of a typical high-performance device. For the device shown (n-channel) the starting material is a slab of p-type semiconductor into which n^+ regions are diffused (source and drain regions) forming two p-n^+ junctions with the substrate. An insulator is then placed between the two junctions and a metal electrode (the gate) is placed on top of the insulator. In operation the source and substrate are grounded and a voltage is applied to the gate in such a manner as to have the two p-n junctions back-biased. For the case shown in Figure 6, a positive voltage applied to the gate causes the semiconductor surface to become electron-rich. Consequently, the two n^+ regions are connected by a surface channel and conduction occurs. The exact value of the gate voltage at which conduction begins is determined by such factors as the insulator thickness, the doping density of the substrate and the density of oxide charge and interface states. Since the dependence of device parameters on insulator thickness and substrate doping density can be calculated, the gate voltage at which conduction begins in an MIS transistor can be used to characterize the surface states. Hence, an analysis of the transfer characteristic, drain current vs. gate voltage (I_d-V_g), of an MIS transistor is a convenient way to characterize the effects of space radiation.

Figure 1 shows a plot of the C-V and transfer characteristics of an MOS transistor with no surface states (solid line) and the shift one sees in these characteristics when a fixed positive charge is introduced in the insulator (dashed line). The introduction of this fixed positive charge is typical of what happens in a radiation environment. As can be seen in the illustration, both characteristics shift by the same voltage, and either can be used to characterize the surface states.

The density of interface states can be calculated by measuring the widening of the C-V characteristic. This is accomplished by taking the difference between the shift in flat-band voltage and the shift in the gate voltage for, say, $I_d = 1 \times 10^{-5}$ A, and making appropriate normalizing corrections.

E. RELEVANCY OF MOS CAPACITOR DATA TO TRANSISTOR PROBLEM

It has been stated earlier that the MOS transistor is not an ideal vehicle for determining the basic principles of charge buildup in the gate oxide of the MOS structure. It must likewise be stated that the simple MOS capacitor cannot simulate all the conditions present in an MOS transistor. The most important of these is probably the asymmetry of the electric fields in the gate oxide of an operating MOS transistor. If the device is "off," then different fields exist between the gate and the source and drain electrodes. Also, the source and drain diffusions in the oxide may cause an unintentional doping of the gate oxide (which is usually grown after source-drain diffusion).

Summarizing, the gate oxide of a practical MOS transistor device may contain several complexities, in lateral fields, lateral doping profiles, and stratification of the insulator which complicate the analysis of radiation effects in the gate oxide. However, the basic oxide structure is the same in MOS capacitors and transistors, and many conclusions on capacitors can be transferred to the transistor case.

F. SPECIAL EXPERIMENTS

In addition to varying materials and processes to determine the influence of fabrication parameters on radiation sensitivity there are some special, but important experiments that will help in confirming and extending the existing physical model for the effect of ionizing radiation on MIS structures.

Experiments of type 1, below, formed a part of the present project. Experiments of types 2 and 3 were not performed but data from earlier tests[3] provided general guidance in analyzing the data produced during

this project. It is suggested that experiments of the latter types should also form a part of future work and they are cited below to indicate their relation and importance to the present study.

(1) The spatial location of the charge induced by the radiation in the insulator is of particular interest and can be ascertained by a so-called dissolution experiment. This can be achieved by a stepwise removal of an insulator layer, subsequent thickness determination by ellipsometry, and measurement of the remaining charge by the C-V technique.

(2) Temperature annealing of the radiation-induced damage can provide additional information concerning the physics of the mechanism of degradation. The annealing of radiation damage is usually complicated and not well understood, and in many cases it does not appear that annealing is the reverse of irradiation. Nevertheless, in a basic study of the radiation physics, annealing experiments cannot be neglected.

(3) Energy-level spectroscopy is the study, by means of optical absorption, of the energy distribution of the radiation-induced defect levels within the forbidden gap of the insulator. Again, this type of investigation can shed considerable light on the nature of the defects and thus on the process of radiation damage.

IV. EXPERIMENTAL DETAILS

A. IRRADIATION SOURCES

1. 1-MeV Van de Graaff Generator

The most frequently used source of radiation in this study was the RCA Laboratories' Van de Graaff generator. Bare MOS devices were irradiated in air at the exit window of the accelerator beam tube. The devices were removed at various intervals in the exposure and their characteristics were recorded. The beam current was checked at the beginning of the exposure and at various intervals during the exposure with a vacuum Faraday cup. In almost all exposures the electron beam energy was kept at 1 MeV. It has previously been shown[2,3,10] that such conditions produced essentially the same results as irradiation to the same ionizing dose under vacuum or in typical transistor encapsulant atmospheres (dry nitrogen, etc.). The electron beam current was measured with a vacuum Faraday cup. The irradiation was interrupted at various fluence levels, and the characteristics of the MOS device were measured.

2. Cobalt-60 Gamma Ray Source

Experiments requiring low dose rates were performed in a 3000-curie Cobalt-60 chamber located at Evans Signal Corp. Laboratories, Belmar, New Jersey. Various dose rates were obtained by placing the sample at different distances from the source. Calibration of the source was accomplished by means of a Victoreen chamber. As in the case of the Van de Graaff experiments, the exposure was interrupted at various intervals and the characteristics of the device were recorded.

B. TEST EQUIPMENT

1. Automatic C-V Plotter

C-V measurements are normally carried out on a point-by-point basis using a capacitance bridge. Then the data have to be plotted. Such a procedure is extremely cumbersome, time-consuming, and subject to frequent error. To eliminate this problem an experimental arrangement has been developed* which allows the automatic and rapid measurement of C-V characteristics of MIS structures at 1 MHz over a wide

*Funded by RCA.

range of bias and sweep speed and under a variety of experimental conditions. The apparatus consists of standard laboratory equipment, provides a graphical output, and makes possible the rapid study of certain problems in MIS physics. For the comparison between experimental and theoretical C-V curves a computer program in FORTRAN has been developed. A detailed description of the measuring circuit and a discussion of the various applications have been published elsewhere[31]. We shall outline here only the principle of operation of this apparatus and its main applications.

In this circuit, the actual quantity measured is an impedance. Hence, the need for a phase-sensitive detector is eliminated. A sawtooth voltage is applied to the MIS capacitor to provide a smoothly varying bias, and a 1-MHz oscillator is used as the signal source. The basic measuring circuit is shown in Figure 7. If the conditions

$$R_M << 1/\omega C_x \text{ and } C_b >> C_x \tag{5}$$

are satisfied, the magnitude of the ac voltage appearing across the measuring resistor R_M is

$$|v_M| = |v| \ \omega R_M C_x.$$

Here, C_x is the MIS capacitance, C_b a blocking capacitor, and ω the frequency of operation. The magnitude of the ac signal from the oscillator is $|v|$, and it is adjusted so that the signal across C_x is never larger than 20 mV. If the reactance of the capacitor is much larger than 50 ohms, then $|v|$ is essentially constant and $|v_M|$ is proportional to C_x and can be used as a measure of C_x. Bias is applied to the MIS capacitor through a parallel branch which is ac-shorted by the series combination of C_b and R_M. If v_M is displayed as a function of the applied bias, then the envelope of the resulting curve is the C-V characteristic. Since $|v_M|$ is only about 0.2 mV, amplification is necessary. This is achieved by the amplifier indicated, which has a gain of about 100 dB. The amplified signal is detected and the dc voltage, which is proportional to capacitance, can then be exhibited as a function of the applied bias on either an x-y recorder or x-y oscilloscope, depending on the rate of change of bias.

This apparatus allows the so-called three-terminal measurement of a capacitor. In this circuit, neither terminal of the test capacitor, C_x, is at ground potential. Shunting to ground by lead capacitance and other stray capacitances that may exist to other parts of the diode structure is thereby eliminated. The losses associated with the MOS

device may introduce an error in the measured capacitance. However, these can be kept below 5 percent if the Q of the device is somewhat better than 3. Using present-day silicon dioxide technology, such low loss levels are easily obtained. The range of measurable capacitance is 100 pF/inch to 0.1 pF/inch and the maximum accuracy is 2 percent. The excellent agreement with bridge measurements is shown in Figure 8.

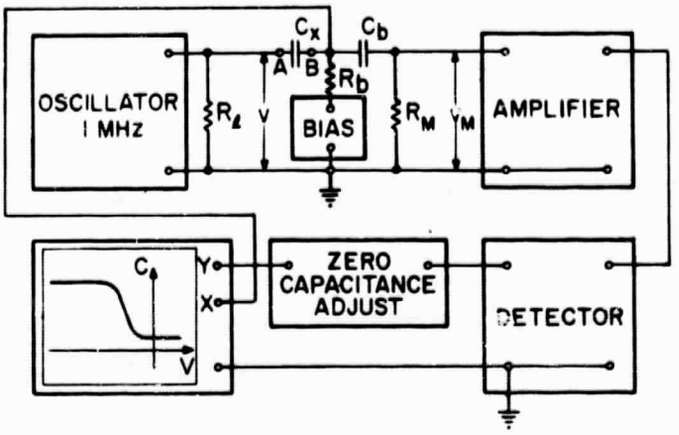


Figure 7. Simplified schematic of the C-V measuring apparatus. R_1 = 50 ohms, R_b = 10 kilohms and C_b = 0.01 μF.

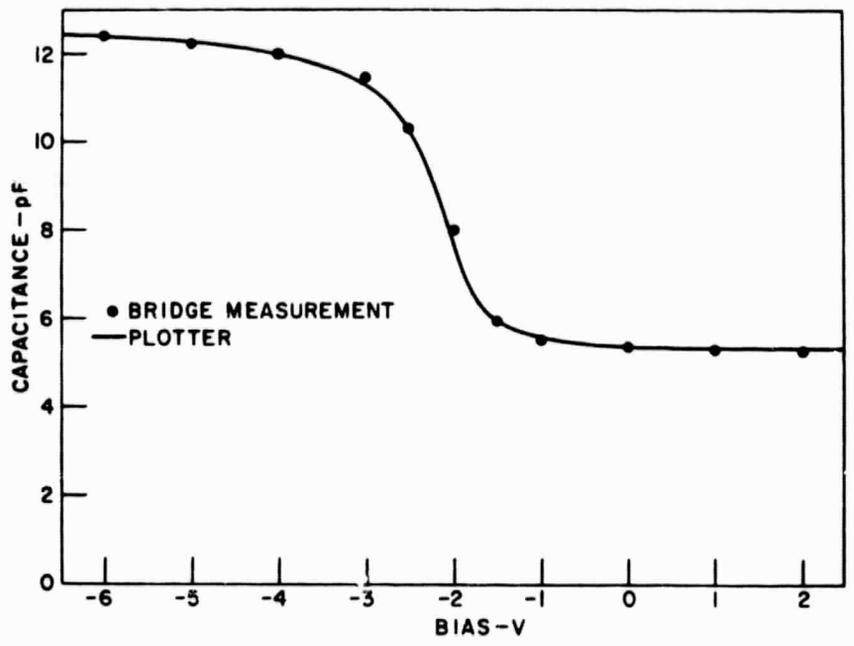


Figure 8. MIS capacitance vs. bias as obtained by measurement with the automatic plotting equipment and with a Boonton Electronics 75 A Capacitance Bridge.

2. Automatic I_d-V_g Characteristic Plotter

A schematic diagram of the basic circuit used for the measurement of the transfer characteristic is shown in Figure 9. The gate bias sweep circuit consists of the positive sweep from an oscilloscope being driven

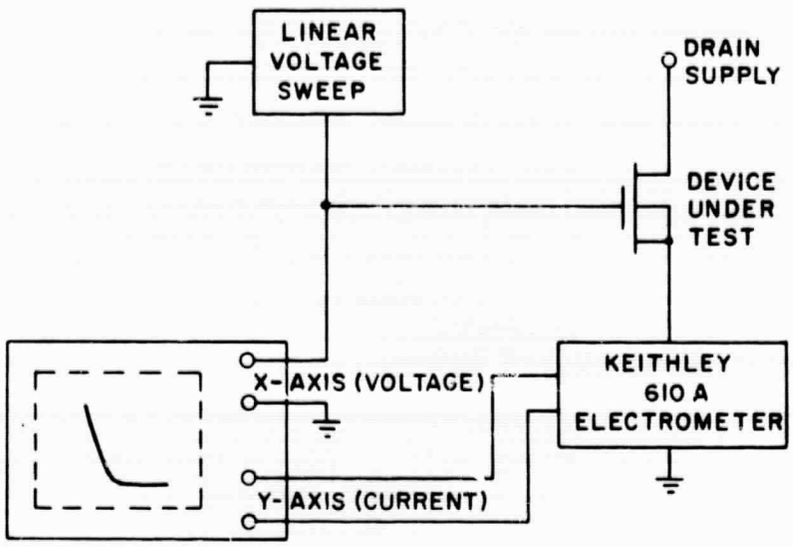


Figure 9. Simplified schematic of MOS transistor transfer characteristic measuring apparatus.

against a battery supply and associated potentiometer so that the voltage could be trimmed to the proper magnitude. The ammeter was a Keithley 610 A electrometer which has an output suitable for driving an x-y recorder. The electrometer was operated in a mode so that the voltage drop across the instrument never exceeded 0.1 V. The drain supply was fixed at 10 V.

V. EXPERIMENTAL RESULTS

A. CRITERIA OF RADIATION SENSITIVITY

It has been stated earlier (see Section II) that ΔN_{ss}, the change in number of "surface states" produced in the oxide by a given process is, as defined here, a quantity in which fixed bulk oxide charge and bias-dependent interface charge may both be included. This is so because it is derived simply from ΔV_{fb}, the change in flat-band voltage of the C-V characteristic. If a large number of interface states are present in the oxide, ΔV_{fb} is thus not a good measure of the fixed oxide charge produced by radiation, although it may still serve as a gross characterization of the sensitivity of an oxide to radiation.

In this report it can be assumed that, unless otherwise indicated, the shifts in flat-band voltage (ΔV_{fb}) were taken for samples which exhibited a near-parallel shift of the whole C-V or I-V characteristic. Hence, the ΔN_{ss} values consist largely of fixed oxide charge and not bias-dependent interface charge. The error in ΔN_{ss} introduced by this assumption will not be greater than 10% and frequently less, since the preparation of the oxides was carried out by methods which allowed only very small quantities of interface states to form; and samples for which the C-V characteristic indicated an appreciable concentration of bias-dependent interface states after fabrication and before irradiation were rejected for most analyses made here. V_{fb} was calculated from C-V plots as follows: The flat-band voltage (V_{fb}) of an MOS capacitor is that gate voltage for which

$$\frac{C}{C_o} = \frac{1}{1 + C_o\left(\frac{kTq}{\varepsilon_s q\ N}\right)^{1/2}} \tag{6}$$

where C = measured capacitance
C_o = oxide capacitance
ε_s = dielectric constant of semiconductor
q = elementary electronic charge
N = semiconductor doping density
k = Boltzmann constant
T = temperature in degrees Kelvin.

This fraction is sometimes called normalized flat-band capacitance value C_{fb}/C_o. If the experimenter is analyzing a C-V curve without the benefit of data on doping density, N, this can be calculated from the ratio of the minimum capacitance to the oxide capacitance, C_{min}/C_o. Curves for rapid

calculation of this quantity are presented in a series of graphs in reference 31. C_{fb}/C_o can then be read conveniently from another curve in this reference. For example, for a p-type semiconductor with a 1000 Å-thick oxide, if the measured $(C_{min}/C_o) = 0.25$, then the doping density can be found from the curves to be $N_a = 10^{15}$/cm (about 13 ohm-cm). Using this as input data for another curve the normalized flat-band capacitance can be found; in this example, $C_{fb}/C_o = 0.7$.

Irradiation conditions used were determined by several considerations. Firstly, although the importance of irradiation bias (bias during irradiation) on radiation effects in MOS devices was realized, it was decided to survey first a wide range of oxides without irradiation bias, since as wide a survey as possible in the time available was thought preferable to more information on bias effects over a narrower range of devices*. Bias effect studies were limited to a few series of oxides. Secondly, "saturation" of the radiation effect was not sought, as in some other studies[19,42], since the effects of radiation levels likely to be reached in operating satellites will not ever approach saturation (10^5 in space vs. 10^9 rads for good saturation). The radiation levels of most interest in space applications were considered to be 10^{11} to 10^{15} e/cm^2 (approximately equivalent to $3 \times 10^3 - 3 \times 10^6$ rads). Thirdly, other studies[10,18] indicated that any source of ionizing radiation could be used for the work and that bulk displacement damage in the silicon did not have to be considered when studying oxide effects. Thus, results obtained using 0.1- to 1-MeV electrons, x-rays, Cobalt-60 or reactor gamma-rays could be regarded as interchangeable, so long as the amount of ionization in the oxide (expressed as ergs/gm or rads absorbed) was used as the criterion of comparison.

* Note added after submission. Recent rapid 1-MeV electron irradiations by P. Newman (private communication) indicate that significant differences exist between ΔV_T shifts observed when gates are grounded to substrate as opposed to when gates are left floating. The probable reason is a buildup of negative charge on the gate and hence a buildup of oxide field during irradiation. The result is a difference in the ΔV_T vs. flux curves which do not saturate as early in the "floating" case as in the "grounded" case. Above fluences of about 10^{12} e/cm^2, the curves thus separate. At the reference fluence of 10^{13} e/cm^2, separation is of the order of 1 volt. Early in the experiments recorded in this report, MOS capacitors were irradiated without any form of contact to the metal islands which were thus floating. Later, spring-loaded tungsten probes were used to contact at least three islands per chip irradiated. In all experiments with MOS transistors the chips were mounted and wire-bonded and gates were routinely grounded. Throughout the tabulations given here, the electrical state of the gate is noted. It is not thought that the possible buildup of charge during the above survey experiments invalidates the comparison of different oxide processes since the irradiation rates and other conditions were the same in most cases.

B. DEPENDENCE OF RADIATION SENSITIVITY ON OXIDE GROWTH CONDITIONS

1. General

Since the silicon dioxide layer of MOS devices is usually formed by diffusion-limited inward growth, it is to be expected that the defect structure of the oxide (hence, its radiation sensitivity) will be strongly affected by variations in growth rate and the components of the oxidation atmosphere. Thus, it is not surprising that some significant differences in sensitivity appear to exist between films grown in dry oxygen and in steam, when irradiated either with or without an applied field during the bombardment. The results of these experiments on very pure laboratory-grown dry oxides and steam-grown oxides will now be discussed.

2. Oxides Grown in Dry Oxygen

a. Preparation - Insulator films of thicknesses ranging from 800 to 2000 Å were prepared by diffusion-limited oxidation or "growth" in an rf (radio-frequency-heated) furnace. The furnace consisted of a vertical vitreous silica tube which was cooled by a stream of forced air passing through an outer jacket. The silicon specimens to be treated were supported by a graphite pedestal on a silica holder coated with silicon carbide. The pedestal acted as a susceptor, or energy-absorber, for the rf energy that was provided by an inductively coupled generator wound around the outside of the tube. Very pure inert or reactive gases could be passed up the silica tube and over the pedestal. By this arrangement, evaporated impurities were carred away by the flowing gas or trapped on the cold tube wall.

Temperature was controlled automatically be means of the signal from an infrared detector which viewed the silicon sample through an optically flat silica plate in the top of the furnace. Most oxidations were carried out by passing pure dry oxygen over the samples at temperatures varying from 900 to 1200°C. Post-oxidation annealing was conducted in helium, nitrogen, or hydrogen.

After oxidation, the samples were provided with a large-area back nickel contact to the silicon and with nickel dots ("gates") on top of the oxide. The contacts were evaporated in a vacuum system operating in the 10^{-6} Torr range. The thickness of the evaporated nickel gates was 0.1 μ as estimated from a previous calibration of the evaporator. The gates were formed either by evaporation through a mask or by conventional photoresist etching from a continuous metal film. The size of the dots was usually 0.012 in. in diameter. No difference in the radiation-sensitivity was observed for the two methods of gate deposition.

The wafers were then divided into about ten chips, each of which contained about six gates, separated by about three gate diameters. The chips were normally mounted on a holder with silver paste and the holder bolted to a standard irradiation wheel used regularly on the RCA Laboratories' Van de Graaff generator. If bias was to be applied, spring-loaded tungsten probes could be lowered to contact the gates, and the desired bias could be applied during irradiation. Irradiations were usually carried out at a rate approaching 10^{15} electrons/cm^2/hr.

b. Effect of Radiation - A typical shift in the C-V characteristic caused by bombarding one of these "dry oxides" with a fluence of 10^{13} 1-MeV electrons/cm^2 is shown in Figure 10. As can be seen from the figure, the

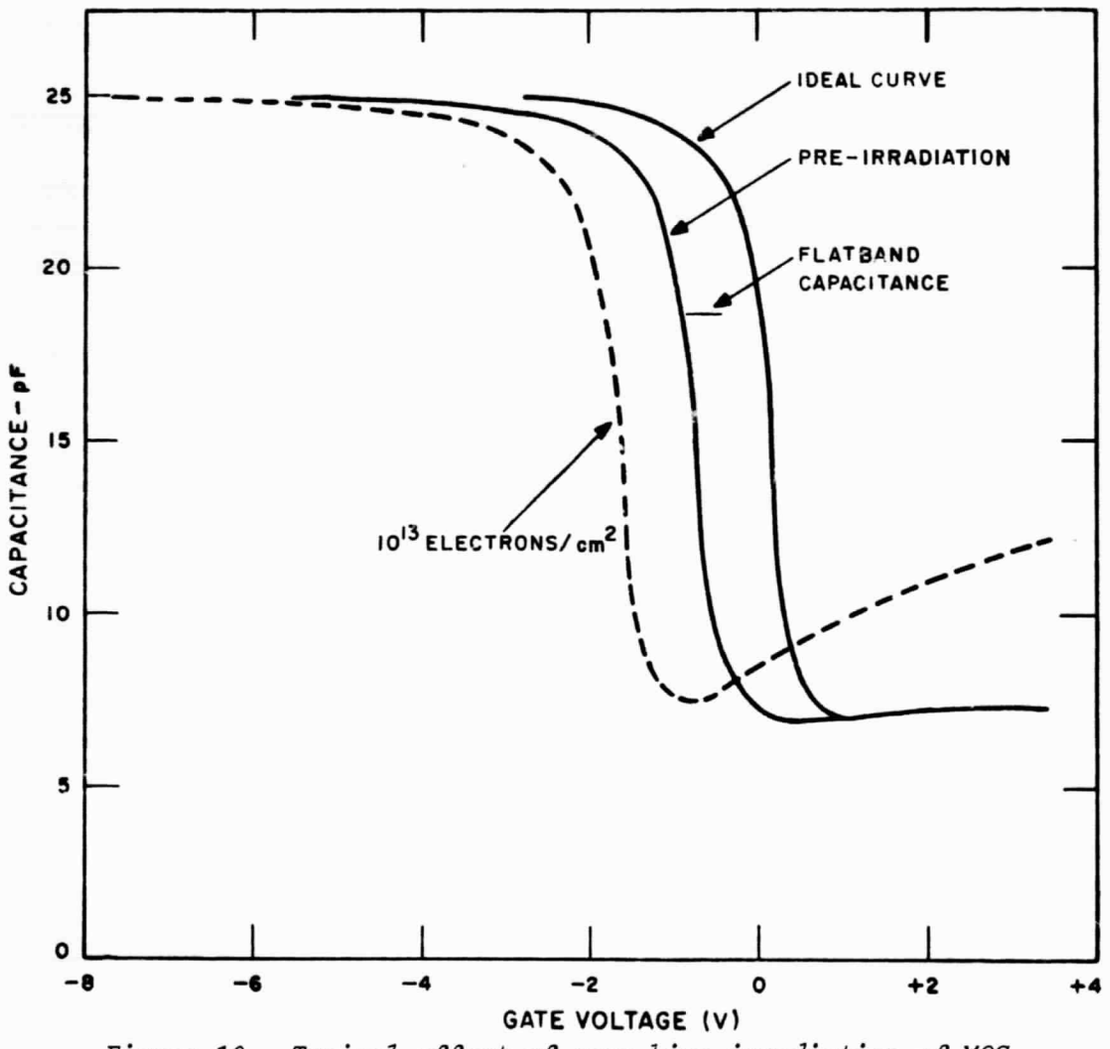


Figure 10. Typical effect of zero-bias irradiation of MOS capacitors with 10^{13} 1-MeV electrons/cm^2.

shift is parallel along the voltage axis, indicating that negligible interface states (i.e., less than 2 x 10^{10} states eV^{-1} cm^{-2}) are being introduced by the radiation. An analysis of the pre-irradiation C-V characteristic of the sample shown indicates that the initial interface state density was also near-ideal (density less than 2 x 10^{10} states) and tended to correlate with low amounts of radiation-induced interface state density.

Table I lists the oxidation conditions for the MOS capacitors studied during the present project. The table also indicates the initial surface-state density and the changes produced by an irradiation with 10^{13} 1-MeV electrons/cm^2.

c. Dependence of V_{fb} Shift on Fluence - Figure 11 summarizes the data obtained on the dependence on fluence of the radiation-induced shift in dry-grown MOS capacitors irradiated without bias on the gate. In all cases, the curves of the radiation-induced shift vs. fluence were similar in their general shape, having high values of slope in the early decades of fluence (10^{11} to 10^{13} electrons/cm^2), with slope value then, gradually falling off in later decades, although no true saturation could be said to occur in most of the samples observed. Over some part of the range (usually in the charge density range 10^{11} to 10^{12} states/cm^2), the fluence dependence approximates a power law similar to that observed for oxide effects in bipolar transistors[11]:

$$\Delta N_{ss} \simeq K \Phi^{0.4} \tag{7}$$

The very wide range of sensitivities possible under zero irradiation-bias extending over one and a half orders of magnitude is worthy of note.

d. Dependence of Sensitivity on Initial Characteristic - All available results on ΔV_{fb} at 3 x 10^5 rads at V_I = 0, for capacitors grown in this laboratory were collected in an attempt to establish whether there was a close correlation between pre- and post-irradiation charge density. They are plotted in Figure 12. Important preparative details are included where available.

The results shown in Figure 12 indicate a grouping which shows that the low initial oxide charge density leads to a low increase in oxide charge density under electron bombardment. The few examples which do not follow this trend can perhaps be explained when one considers the inaccuracies in the measurements made:

TABLE I

Process Data on MOS Capacitors Used in Process-Effects Study

Sample	Wafer Cleaning Procedure	Type of Furnace	Oxidation Atmosphere	Annealing Conditions	Oxide Thickness t(Å)	Flat-band Voltage Before Irradiation (V_{fbo})	Shift in Flat-band Voltage After 10^{13} 1-MeV e/cm^2 (ΔV_{fb})	Surface-State Density Before Irradiation (N_{ss})(cm^{-2})	Change in Surface-State Density after 10^{13} 1-MeV e/cm^{2*} ΔN_{ss}(cm^{-2})	Equivalent Voltage Shift for 0.15-μm-Thick Oxide ΔV_E
M13-RA	Standard Chemical Cleaning + H_2 fire @1250°C for 5 min	rf induction @1150°C	dry O_2	H_e@1150°C for 15 min + H_2@950°C for 15 min	1280	-1.05	-0.85	1.73×10^{11}	1.40×10^{11}	-1.4
M14-R	Standard Chemical Cleaning + H_2 fire @1250°C for 5 min	rf induction @1150°C	dry O_2	H_e@1150°C for 15 min + H_2@950°C for 15 min	1410	-1.05	-1.0	1.56×10^{11}	1.52×10^{11}	-1.52
CH 11**	Standard Chemical Cleaning	Resistance @1200°C for 6 min	dry O_2	--	850	--	--	2.05×10^{11}	4.05×10^{11}	-4.05
CH 12**	Standard Chemical Cleaning	Resistance @1200°C for 6 min	dry O_2	H_2@450°C for 15 min	850	--	--	4.0×10^{10}	3.9×10^{11}	-3.9
CH 8**	Standard Chemical Cleaning	Resistance @1200°C for 6 min	dry O_2	H_2@450°C for 60 min	920	--	--	4.0×10^{10}	3.7×10^{11}	-3.7
M16S	Standard Chemical Cleaning	Resistance @1100°C for 5 min	Steam	H_2@950°C for 15 min	1790	-2.05	-1.63	2.4×10^{11}	1.93×10^{11}	-1.93
C-23	Standard Chemical Cleaning	Resistance @1100°C for 3 min	Steam	H_2@500°C for 15 min	858	-2.0	-0.95	4.92×10^{11}	2.33×10^{11}	-2.33
CP-1	Standard Chemical Cleaning	Resistance @1100°C for 4 min	Steam	as above	1380	-1.25	-2.4	1.91×10^{11}	3.66×10^{11}	-3.66
M18 SA	Standard Chemical Cleaning	Resistance @1100°C for 4 min	Steam	H_2@500°C for 30 min	1340	-2.90	-1.73	4.53×10^{11}	2.72×10^{11}	-2.72

*Metal gate floating during bombardment.
**The capacitors had no metal gates, hence, were "floating" during bombardment.

TABLE I (Continued)

Process Data on MOS Capacitors Used in Process-Effects Study

Sample	Wafer Cleaning Procedure	Type of Furnace	Oxidation Atmosphere	Annealing Conditions	Oxide Thickness t(Å)	Flat-band Voltage Before Irradiation (V_{fbo})	Shift in Flat-band Voltage After 10^{13} 1-MeV e/cm^2 (ΔV_{fb})	Surface-State Density Before Irradiation (N_{ss})(cm^{-2})	Change in Surface-State Density after 10^{13} 1-MeV e/cm^2* ΔN_{ss}(cm^{-2})	Equivalent Voltage Shift for 0.15-μm-Thick Oxide ΔV_E
C3A*		rf Induction	dry O_2	?	1660	-3.5	-11.5	4.54×10^{11}	1.46×10^{12}	-14.6
C-31*	Standard Chemical Cleaning	rf induction @1080°C for 1 hr	dry O_2	N_2@1080°C for 1 hr	1130	-0.5	-2.5	0.94×10^{11}	4.7×10^{11}	-4.7
C-22	Standard Chemical Cleaning	rf induction @1090°C for 1 hr	dry O_2	N_2@1090°C for 1 hr	1230	-3.13	-4.35	5.37×10^{11}	7.45×10^{11}	-7.45
C-21*	Standard Chemical Cleaning	rf induction @1090°C for 1 hr	dry O_2	N_2@1090°C for 1 hr	1210	-2.9	-5.55	5.0×10^{11}	9.67×10^{11}	-9.67
C-24*	As above	As above	dry O_2	As above	1240	-3.38	-3.0	5.75×10^{11}	5.14×10^{11}	-5.14
C-20	Standard Chemical Cleaning	rf induction @1200°C for 66 min	dry O_2	N_2@1200°C for 30 min	2035	-4.5	-3.55	5.61×10^{11}	3.7×10^{11}	-3.7
M3R*	Standard Chemical Cleaning	rf induction @1080°C for 1 hr	dry O_2	N_2@1080°C for 30 min + H_2@800°C for 5 min	1085	-1.46	-1.1	2.85×10^{11}	2.14×10^{11}	-2.14
C-40	Standard Chemical Cleaning + in situ H_2 fire @ 1290°C for 5 min	rf induction @1090°C for 1 hr	dry O_2	N_2@1090°C for 30 min	1820	-1.96	-2.03	2.27×10^{11}	2.36×10^{11}	-2.36

*Metal gate floating during bombardment.

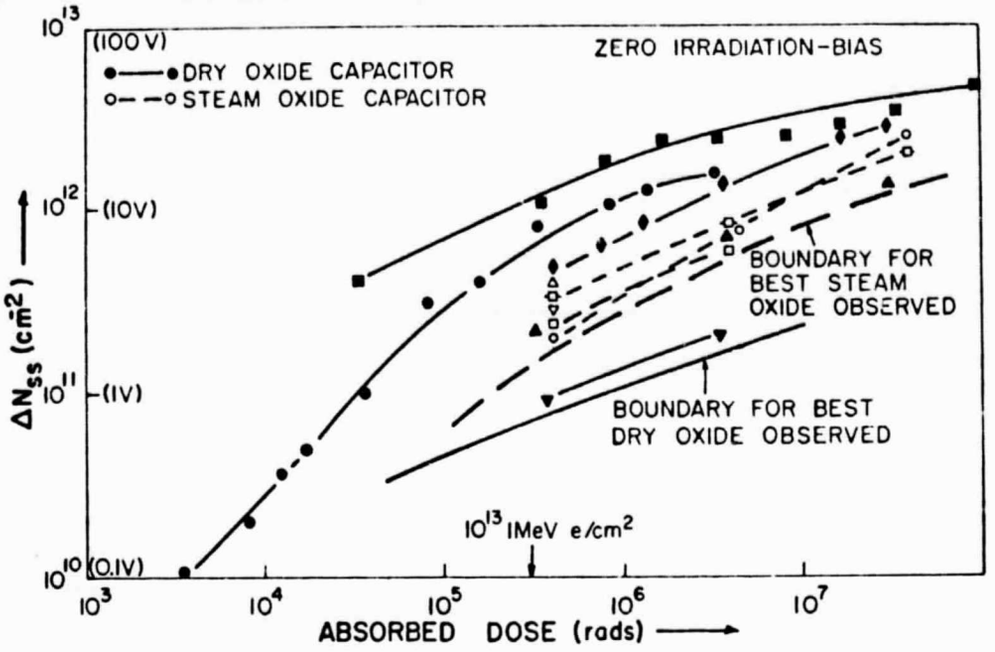
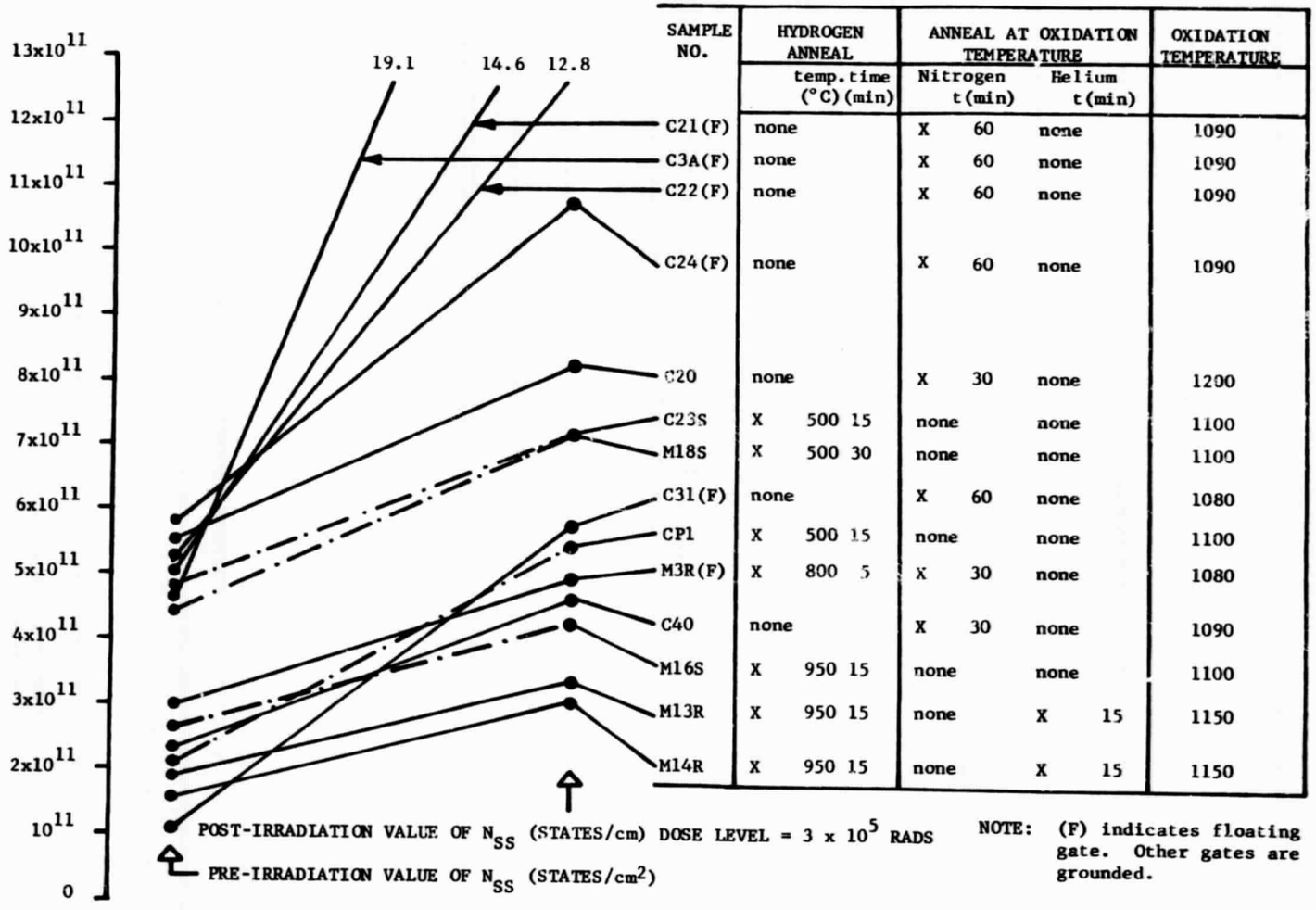


Figure 11. Collected data on 1-MeV electron irradiation of MOS capacitors made from steam-grown and dry-grown oxides. Measured voltage shifts are normalized for oxide thickness to charges per cm^2, and (in brackets) the corresponding voltage shift in a 0.211-μm oxide. Electron fluence is normalized to equivalent absorbed dose in rads. Gates in this experiment were floating during bombardment.

(1) The electron fluence measurement is accurate to only ± 10%.
(2) The thickness from sample to sample of the gate electrode is only accurate to approximately ± 30%. Thicker gates would produce more secondary electrons and hence an increased dose.
(3) When making our comparison of fluence levels, small differences in the trap distributions of different oxides could have a comparatively large effect, since the traps are not yet saturated.
(4) The grounding conditions for the gate differed among the experiments and this could conceivably have an effect on the results.

A controlled experiment, specifically designed to throw light on this connection between initial oxide charge density and radiation-induced oxide charge density, would be very profitable.



SAMPLE NO.	HYDROGEN ANNEAL temp. (°C)	HYDROGEN ANNEAL time (min)	ANNEAL AT OXIDATION TEMPERATURE Nitrogen	Nitrogen t(min)	Helium	Helium t(min)	OXIDATION TEMPERATURE
C21(F)	none		X	60	none		1090
C3A(F)	none		X	60	none		1090
C22(F)	none		X	60	none		1090
C24(F)	none		X	60	none		1090
C20	none		X	30	none		1200
C23S	X	500 15	none		none		1100
M18S	X	500 30	none		none		1100
C31(F)	none		X	60	none		1080
CP1	X	500 15	none		none		1100
M3R(F)	X	800 5	X	30	none		1080
C40	none		X	30	none		1090
M16S	X	950 15	none		none		1100
M13R	X	950 15	none		X	15	1150
M14R	X	950 15	none		X	15	1150

NOTE: (F) indicates floating gate. Other gates are grounded.

Figure 12. Comparison of pre-irradiation and post-irradiation characteristics of MOS capacitors at a 1-MeV electron fluence of 10^{13} e/cm^2. Some key processing data for the samples shown are also tabulated.

e. Dependence of Shift on Irradiation Bias - The effect of gate bias during irradiation is shown in Figure 4 as the density of induced oxide charge vs. the gate bias applied during irradiation. The electron fluence in this case was 10^{13} 1-MeV electrons/cm^2. Unfortunately, since the induced oxide charge density is not saturated, these data cannot be analyzed in terms of the models given by Grove et al.[19] and Stanley[42]. However, one important issue can be examined using these data, namely, the relation of shift under irradiation bias vs. shift without bias. In both conditions, sample C3A is considerably more sensitive to radiation than the other dry oxide, sample M-14. If this trend is found to be universal, it may be possible to predict the radiation sensitivity of an oxide at all irradiation bias conditions by irradiating a sample without bias at a few radiation levels. This would greatly simplify routine evaluations of MOS transistors for radiation sensitivity.

The data in Table II again show the gross relationship between the pre-irradiation oxide charge density and the radiation-induced oxide charge density which was illustrated in Figure 12. The table lists the dry oxides studied in the order of increasing initial oxide charge density. Also shown in this table is the radiation-induced oxide charge density for a fluence of 10^{13} 1-MeV electrons/cm^2. Although there are several exceptions, notably samples with high initial oxide charge densities, there is a definite tendency for an increase in the radiation-induced oxide charge density with increasing initial oxide charge.

f. Influence of Cleaning Method - In all cases, the silicon wafers were cleaned in a combination of organic and inorganic solvents and reagents prior to being placed in the oxidation furnace. In three cases (samples M-13RA and M-14R and 7a) the samples were given, in addition to the standard chemical cleaning, a pre-oxidation firing in hydrogen at 1250°C for 5 min in the rf-heated furnace. This firing removed several hundred angstroms of the silicon surface by the reaction,

$$Si + H_2 \rightarrow SiH_4$$

and rendered the surface very clean. After oxidation and annealing, the samples had low oxide charge densities (see Table I). When irradiated with 1-MeV electrons, these samples proved to be the least radiation-sensitive thermal oxides observed to date.

g. Variation of Shift Over Wafer - Both small-scale and large-scale variations of sensitivity across a wafer could be examined since, in most cases, several adjacent dots were irradiated uniformly in the Van de Graaff beam, while more than one chip from a wafer was irradiated to the same electron fluence. In general, the variation of radiation sensitivity over a wafer was low. Typical figures for variation over several adjacent

TABLE II

Pre-irradiation and Post-irradiation Surface State Density of MOS Capacitors in Order of Pre-irradiation Values

Sample	Initial N_{ss}	ΔN_{ss} for Φ 10^{13} e/cm^2
C-31(F)	9.4×10^{10}	4.7×10^{11}
M-14R	1.56×10^{11}	1.52×10^{11}
M-13RA	1.73×10^{11}	1.4×10^{11}
C-40	2.27×10^{11}	2.36×10^{11}
M3R(F)	2.85×10^{11}	2.14×10^{11}
C3A(F)	4.54×10^{11}	1.46×10^{12}
C-21(F)	5.0×10^{11}	9.67×10^{11}
C-22(F)	5.37×10^{11}	7.45×10^{11}
C-20	5.61×10^{11}	3.7×10^{11}
C-24(F)	5.75×10^{11}	5.14×10^{11}

NOTE: (F) indicates floating gate.

gates are 4.4 to 5.3 x 10^{11} states/cm^2 at a fluence of 10^{13} 1-MeV selections/cm^2 (V_B = 0). For a chip on the opposite side of the same wafer, the corresponding figures were 4.3 to 5.1 x 10^{11} states/cm^2. Similar variations were found for the "Pattern 7" developmental transistors from the same wafer. Here, four units are integrated on one chip. The most widely divergent values for the shift in threshold voltage after irradiation by a fluence of 10^{13} electrons/cm^2 are -2.25 V to -2.65 V on one chip and -2.5 V to -2.95 V for another transistor cut from the same wafer.

C. OXIDES GROWN IN STEAM

Oxides grown in steam have considerable practical interest because the growth rate is considerably higher than for dry oxygen growth. This is important in silicon device technology because diffusion profiles can change drastically if the sample has to be left at the higher temperatures and longer times required for oxidation to the same thickness. Consequently, several steam-grown oxides were prepared to test their sensitivity to radiation.

All wafers were chemically cleaned prior to being placed in the oxidation furnace. The oxidation furnace was a resistance-heated high-purity alumina tube. The wafer to be oxidized was passed into the furnace in a high-purity quartz boat. After oxidation, the wafers were usually annealed in hydrogen in a separate furnace. Nickel contacts were placed on the sample in the same manner as for the dry oxides (see Section V-B).

As in the case of the dry oxides, parallel shifts in the C-V characteristic were usually obtained when the steam oxide capacitors were bombarded with 1-MeV electrons, indicating that no new interface states were being introduced. Figure 11 shows the dependence of radiation-induced oxide charge density on fluence for several steam oxide capacitors which were bombarded with 1-MeV electrons. The gates were left floating during the irradiation. Again, a saturation of the radiation-induced oxide charge density was not observed, even at the highest fluence levels used. The pertinent data for these samples are listed in Table I. The dependence of the fixed oxide charge density on irradiation bias at a fluence of 10^{13} electrons/cm^2 is shown in Figure 4 for two samples.

Unlike the dry oxide capacitors, the radiation sensitivity of all the steam oxide capacitors was quite similar. Sample C-23 was least sensitive to radiation, both in the floating-gate fluence-dependence experiment and in the bias-dependence study. However, the differences between all steam samples was small. This would seem to indicate that the ability to reproduce trap distributions is much easier in the case of steam-grown oxides then in dry-grown oxides.

Figure 12 includes some steam-grown samples. It is seen that, as before, final oxide charge density bears some correlation with initial charge density.

D. POST-OXIDATION ANNEALING

1. Annealing in an Inert Atmosphere

Thermal oxidation of silicon results in a nonuniform distribution of defects in the oxide and in a Si-SiO_2 interface condition which is disordered. High-temperature post-oxidation annealing treatments, either in vacuum or in an inert atmosphere, appear to effect a redistribution of the oxide defects and a rearrangement of the interface to a state of higher order[43,44]. In isothermal annealing, it has been shown that the density of donor type surface states decreases logarithmically with time. Hence, it might be expected that the post-oxidation annealing time will have some effect on the radiation sensitivity of the oxide, and experiments to test this hypothesis were made.

Several pure dry-grown oxides were prepared in the rf furnace (see Section V-B), followed by an in-situ annealing in helium at the oxidation temperature for varying lengths of time. However, no clear-cut dependence of the radiation sensitivity on the duration of the post-oxidation annealing was observed. Rather, two trends were observed for the dry oxide: (1) The greater the initial density of interface states, the greater the number of new interface states introduced by the radiation. (2) The lower initial oxide charge densities usually lead to the lower radiation-induced oxide charge densities. Hence, we can conclude that post-oxidation annealing in an inert atmosphere is effective in reducing the radiation sensitivity of an oxide layer only insofar as it affects the pre-irradiation character of the oxide and interface.

2. Annealing in Hydrogen

A technique which is often employed to reduce the flat-band voltage and to provide a charge-free $Si-SiO_2$ interface is the post-oxidation annealing of the oxide film in hydrogen at temperatures in the 400 to 600°C range. This phenomenon has been discussed by Kooi[20], and he has suggested that it is due to a reaction of defect centers with hydrogen so that they are no longer able to capture holes or electrons. Thus, the effect of hydrogen baking on radiation sensitivity was specially studied.

The oxides used were grown under pilot production-line conditions. A silicon wafer was oxidized in dry oxygen in a resistance-heated furnace to approximately 900-Å thickness. The wafer was then divided, one half only being further treated in hydrogen at 450°C for 60 min. The C-V curves were recorded by use of the mercury-gold probe technique*. The initial oxide charge densities for the unannealed and annealed samples were 2×10^{11} states/cm^2 and 5×10^{10} states/cm^2, respectively. Samples from both halves were then bombarded with 1-MeV electrons to a fluence of 10^{15} electrons/cm^2 with no bias applied. The induced oxide charge density of the unannealed and annealed samples was 3.0×10^{12} states/cm^2 and 2.5×10^{12} states/cm^2, respectively. Thus, the sample which had received the hydrogen treatment was slightly less sensitive than the untreated sample, probably due to the reduced number of hole trapping sites. The results of this experiment support the observations which we have made on the pure laboratory-grown oxides (see Section V), namely, that the lower the initial oxide charge density, the less sensitive is the oxide to radiation. However, the observed reduction in sensitivity of the annealed sample is only about 16%, and the effect of hydrogen baking was thus not as strong as would be expected if hydrogen and radiation-induced holes indeed reacted at the same type of defect center.

* Since no metal gates were used, the free oxide surface can be regarded as "floating" during irradiation.

E. NONTHERMAL OXIDATION PROCEDURES

1. Anodic Oxides

Anodic oxidation of silicon offers the possibility of producing thin, dense, oxide layers free of pinholes and hence might become a valuable process in MOS device technology. The production of these layers has been described by Revesz[45] but is reproduced here for the sake of completeness.

Chemically polished 10 ohm-cm p-type silicon of (111) and (100) orientations was used. The silicon wafers were cut to a 1 by 1 cm square with a 1-cm long stem that was attached to a holder in the anodizing apparatus. The specimens were carefully cleaned, and just before anodization they were submerged in hydrofluoric acid and rinsed with distilled water.

Following the work of Schmidt and Michel[46] the electrolyte chosen was 0.04 M solution of KNO_3 in N-methylacetamide (NMA). Since it is known that this electrolyte is hygroscopic and the oxidation process is influenced by its water content[46,47] fresh electrolyte was used for each oxidation. Because the electrolyte has a strong tendency to creep, the upper part of the stem of the silicon specimen together with the holder was masked. The temperature during anodization was about 50°C. The cathode was a platinum sheet. The anodization was performed in the constant-voltage mode at 300 V in about 5 hr.

After oxidation the specimens were rinsed in water. Specimens were then treated in hydrogen at 500°C for 15 min in a vitreous silica tube furnace. For MOS capacitance measurements the specimens were provided with nickel back contacts, and aluminum electrodes on the oxide.

Constant-voltage anodization to low final current densities followed by annealing can result in a surface-state density with no states within the silicon forbidden band. The relatively high perfection of this interface is shown by the lack of interface instability effects at 300°C under high field.

The result of irradiating a typical anodic oxide, which exhibited good pre-irradiation interface characteristics, with 10^{13} 1-MeV electrons/cm^2 is shown in Figure 13. The gate was "floating" during irradiation. As can be seen from the figure, the C-V curve undergoes a parallel shift along the voltage axis. This indicates that few new interface states are being introduced by the radiation. From the shift along the voltage axis the density of oxide charge introduced into the oxide is found to be 1.4×10^{11} states/cm^2 for 10^{13} 1-MeV electrons/cm^2. This is one of the lower values obtained during the present project. The radiation-induced oxide charge could be annealed out by heating the sample in a nitrogen ambient at 300°C for 10 min.

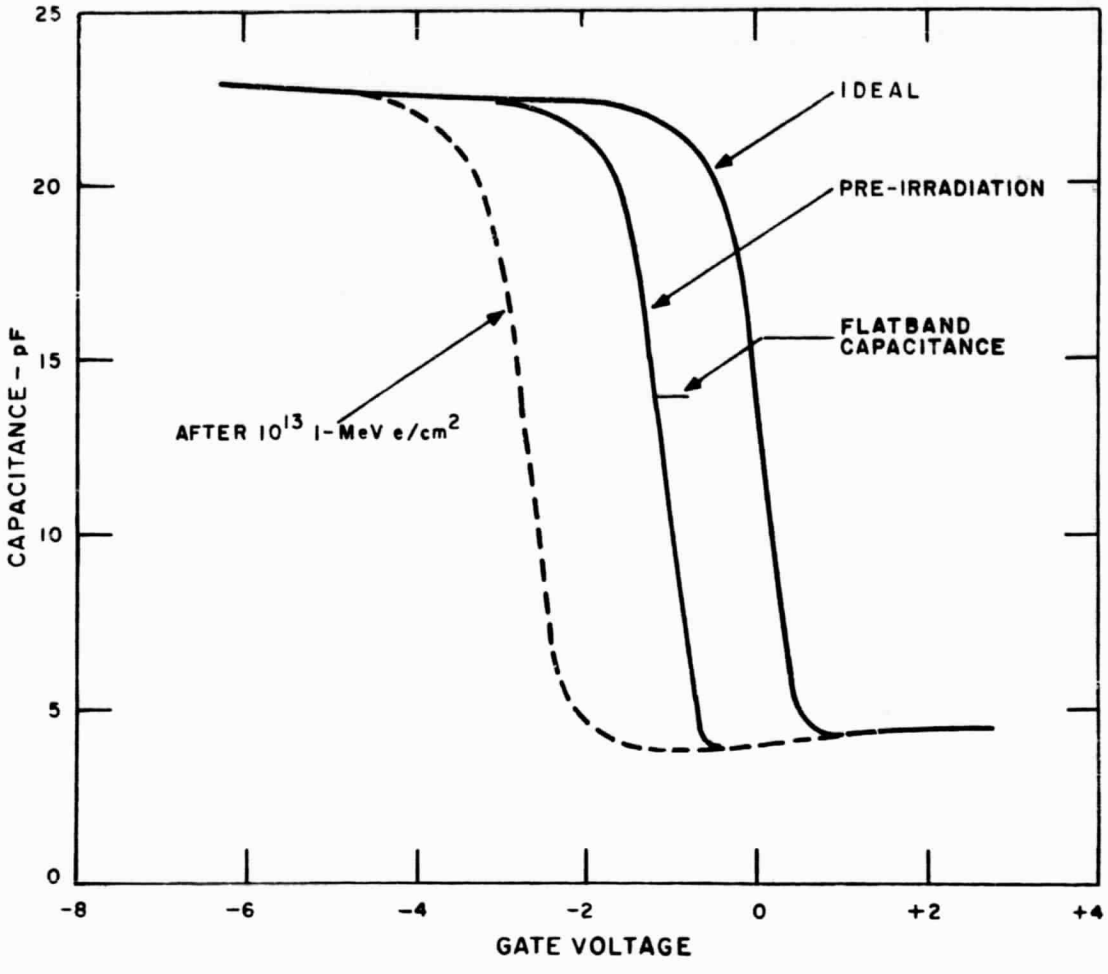


Figure 13. Effect of irradiation on anodic-oxide capacitor at a 1-MeV fluence of 10^{13} e/cm^2 and with gate floating.

2. Pyrolytically Deposited Oxides

Low-temperature (400 to 600°C) pyrolytic deposition of glasses is receiving increasing interest in many semiconductor research laboratories. The need for this technology is especially important in large-scale integrated-circuit development where good insulation is needed for cross-over connection. The low-temperature processes are needed because metallization can be destroyed at high temperatures. Several forms of these insulators are presently being developed by RCA Laboratories[48].

Since the radiation response of an MIS device is determined by the trap distribution in the insulator, it was reasoned that if one could produce an insulator which exhibited electron-trapping rather than hole-trapping under electron bombardment (i.e., a shift in the C-V characteristic in the unconventional, positive direction along the voltage axis) then, by compensation, a radiation-resistant MIS device could possibly be produced. Facilities for the low-temperature chemical vapor deposition of various insulators were available at RCA Laboratories, by courtesy of the Process Development Laboratory.

Chemically polished silicon wafers, of <111> orientation, and 10-ohm-cm resistivity were chemically cleaned using a combination of organic and inorganic reagents. Insulating films of silicon dioxide, borosilicate, phosphosilicate, and alumino borosilicate were then formed on the silicon by chemical vapor deposition. The pertinent chemical reactions are:

$$SiH_4 + 2\ O_2 \rightarrow SiO_2 + 2\ H_2O$$

$$B_2H_6 + 3\ O_2 \rightarrow B_2O_3 + 3\ H_2O$$

$$2\ PH_3 + 4\ O_2 \rightarrow P_2O_5 + 3\ H_2O$$

$$2\ Al(CH_3)_3 + 12\ O_2 \rightarrow Al_2O_3 + 6\ CO_2 + 9\ H_2O$$

By varying the amounts of the reactant gases, various compositions of glass could be obtained.*

The particular compositions studied were nominally 15% B_2O_3, 15% P_2O_5, and 15% Al_2O_3. The samples were irradiated without gates and capacitance-voltage measurements were performed using the mercury probe technique.

Several samples from each wafer were irradiated with 1-MeV electrons and the C-V curves were recorded both before and after irradiation. The samples, both before and after irradiation, exhibited large amounts of interface instability (e.g., 2 to 3 V shift in the C-V characteristic for application of 10-V bias at room temperature). In addition, there was some shape change in the C-V characteristic after irradiation to the higher fluence levels, indicating that new interface states are being introduced. However, as is shown in Figure 14, the C-V curve shifted in all cases toward more negative voltage with increasing fluence. Thus, although minor amounts of electron trapping could conceivably have been masked by the interface effects described, no indications of strong electron trapping were found in the deposited layers described above.

* The development of this technique was carried out on RCA Funds.

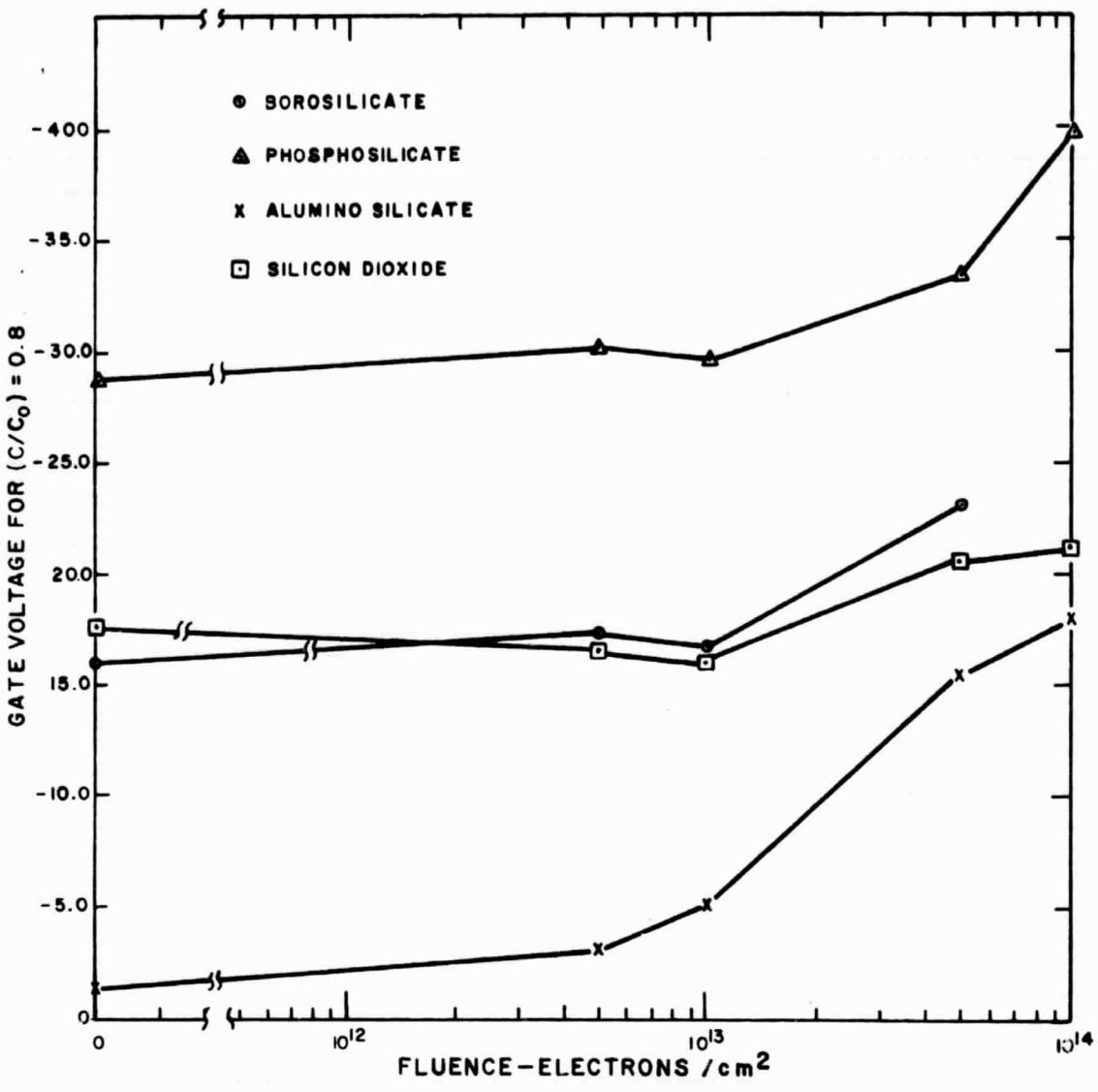


Figure 14. Radiation-induced shifts for pyrolytically deposited layers derived from mixtures of oxygen, silane, and hydrides of silicon, phosphorus, boron, and aluminum. "Silicon dioxide" indicates use of unmixed silane with oxygen. Other legends indicate the other hydrides which were added to silane in about 15% concentrations. The capacitors had no metal gate and hence, were irradiated in the floating condition.

3. Composite Insulator Layers

As is well known contamination of silicon dioxide layers with sodium ions leads to large-scale ion drift instabilities in MOS devices when subjected to temperatures bias stress. It is also well known that SiO_2 layers can be stabilized against this ion drift by incorporation of a P_2O_5 layer on top of the SiO_2 gate insulator[49]. Since many commercially available MOS devices employ this technique, it is important to study the influence of such layers on device sensitivity to radiation. The effect of such layers on device sensitivity to radiation is also of interest for several other reasons:

(1) It is to be expected that the presence of phosphorus in a silicon dioxide network should profoundly affect the defect structure and, hence, the effective charge-trap concentration.

(2) The presence of a new interface within the MIS insulator film presents new possibilities of trapping or transfer of charge. Several experiments by the authors have indeed indicated a possible influence of phosphorus on the radiation sensitivity of MIS devices[21,50]*. Figure 15 shows the shift in threshold voltage, ΔV_T (where V_T is the gate voltage at which the drain current I_d is 2×10^{-5} A), as a function of 1-MeV electron fluence, for semi-integrated "Pattern 7" (see Section IV-F-2) MOS transistors irradiated with the gates grounded. Series A-13 contains phosphorus while series A-41 transistors are entirely similar samples which do not contain phosphorus. Table III gives the fabrication procedure for both of these lots.

Figure 16 shows a typical pattern of change of transfer characteristic for a "Pattern 7" device. There is only a slight change in shape of the characteristic, indicating small generation of interface states. At low radiation doses, a small positive shift is seen, probably caused by interface states[50] but soon overcome by positive oxide charge buildup.

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* In a late news paper at the recent IEEE Nuclear and Space Radiation Effects Conference (Columbus, Ohio, July 10-14, 1967), D. Long reported the fortuitous discovery of six particularly radiation-resistant transistors among a batch of devices made by Sprague, Inc. The treatments which were thought to have caused this unexpected "hardening" included heat-treatment and phosphorus glass deposition followed by etch-back. No controlled experiments had yet been carried out.

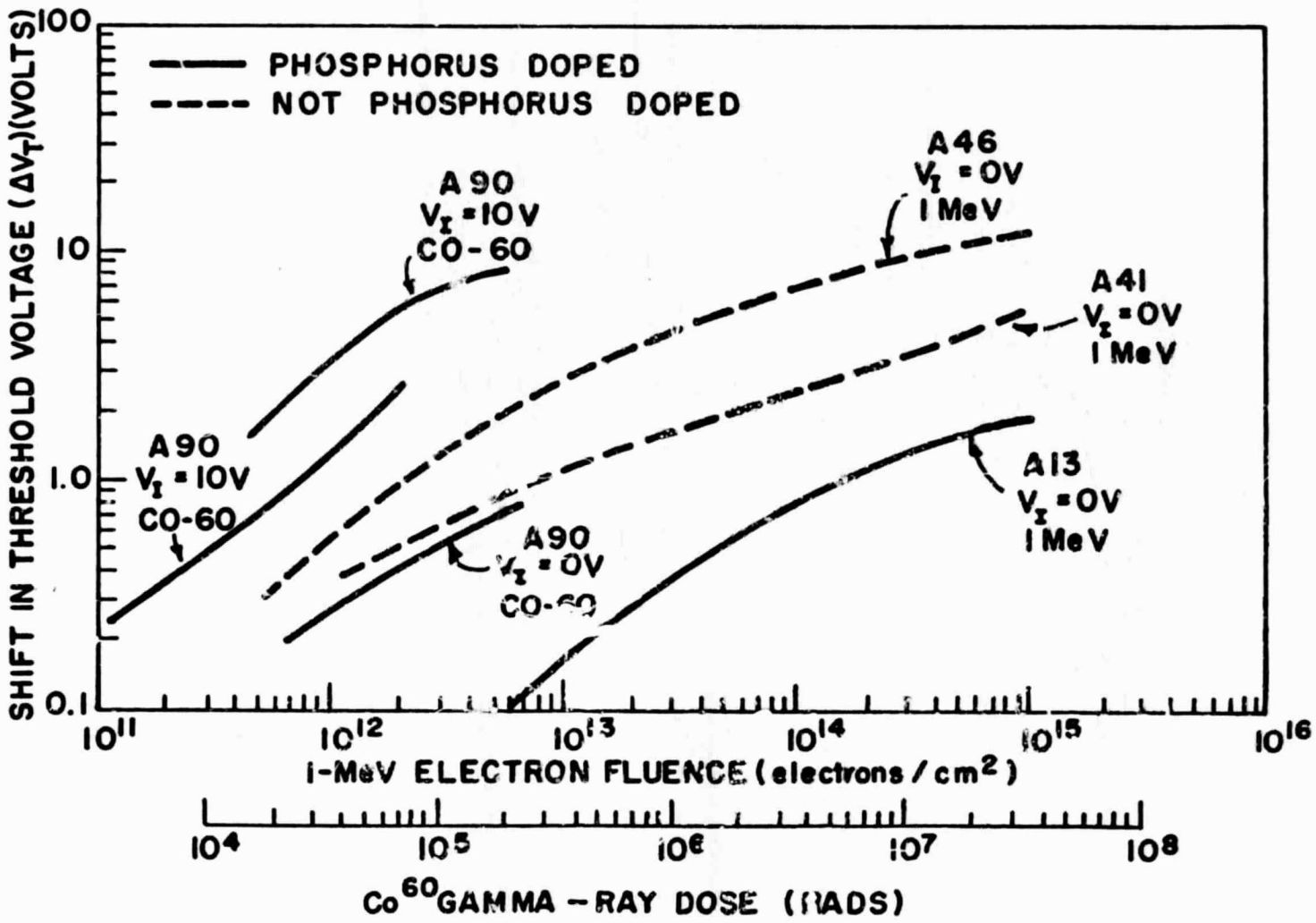

Figure 15. Collected results of irradiation with 1-MeV electrons and cobalt-60 gamma rays of RCA "Pattern 7" transistors. The abscissae are aligned to express equivalent absorbed dose. Irradiation bias values and wafer numbers are indicated on the curves. For cases labeled $V_I = 0$, gates were grounded during irradiation. A-13 and A-90 contain phosphorus, A-41 and A-46 do not.

TABLE III

Fabrication Conditions for Gate Insulator of "Pattern 7" Samples A-13 and A-41

A-13	A-41
(1) Grow thermal oxide in dry O_2 @ 1200°C.	(1) Same.
(2) Deposit pyrolytic layer containing phosphorus at 675°C substrate temperature.	(2) Deposit pyrolytic SiO_2 layer at 675°C substrate temperature (no phosphorus included).
(3) Deposit thin pyrolytic SiO_2 layer at 675°C (for metallization adhesion only).	(3) (Step not required).
(4) Heat treat in dry O_2 @ 1200°C for 15 min ("densification").	(4) Same.
(5) Anneal in H_2 @ 450°C for 15 min.	Same.
Details of deposition of phosphosilicate glass: Reacted gases are (1) mixed oxygen and nitrogen and (2) argon, bubbled through separate vessels containing liquid tetraethyl orthosilicate (TEOS) and trimethyl phosphate (TMP) at room temperature. Flow rates for phosphosilicate glass are normally $Rate_{TMP}/Rate_{TEOS} = 2$. Total argon flow rate is normally about 2 liters/min. [These details are similar to those reported by RCA Electronic Components to the U.S. Army Electronics Command, Fort Monmouth, New Jersey, on Contract No. DA-28-043-AMC-00314(E)].	

Figure 15 compares the phosphorus vs. nonphosphorus containing samples. An exact comparison between radiation-induced charge densities was not possible, using the "Pattern 7" transistors, since an accurate determination of the insulator thickness was not possible. Thus, model experiments were done using MIS capacitors made by a similar series of steps and in the same furnaces in which the above transistors were made.

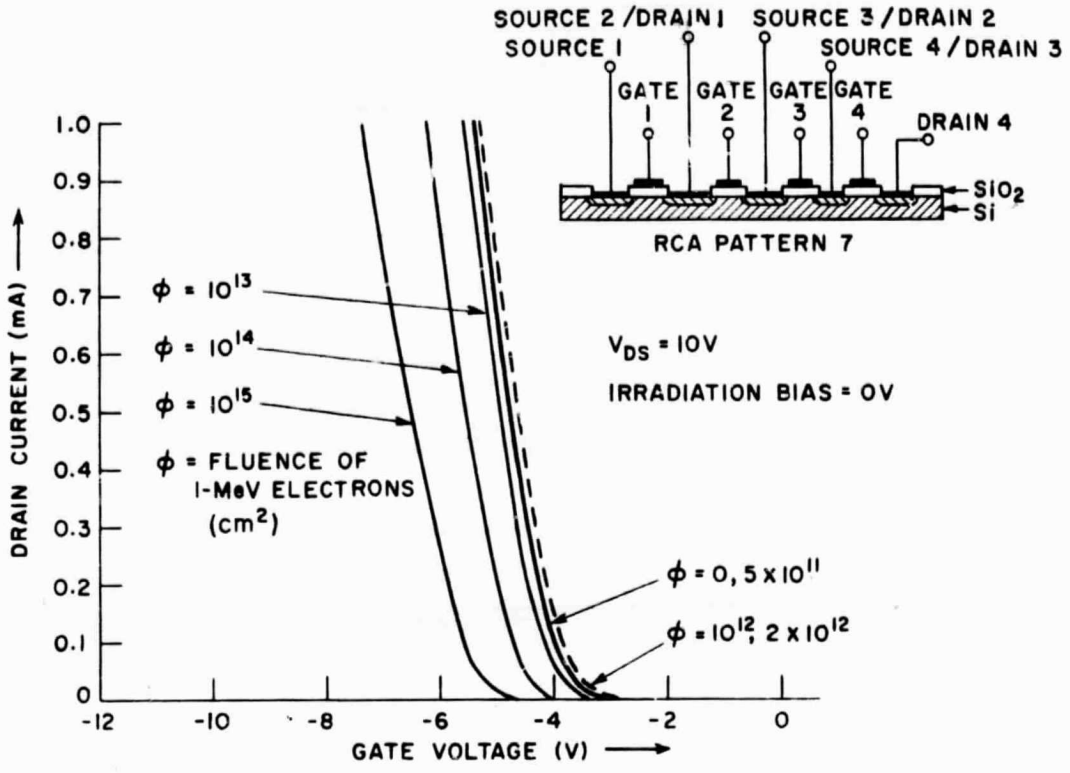

Figure 16. Typical changes in transfer characteristics of a "Pattern 7" transistor under zero irradiation bias (gate grounded during bombardment).

Insulator films were prepared by oxidizing several silicon wafers in dry oxygen in a resistance-heated furnace at 1200°C. This was followed by annealing in hydrogen at 450°C for 15 minutes. On one of the wafers only, prior to annealing, approximately 600 Å of phosphosilicate glass were deposited on top of the thermal oxide using the same techniques and experimental conditions as for the "Pattern 7" transistors above (see Table III). The overall thickness of the layers was then determined by ellipsometry. Metallic gates were not evaporated on the wafer and C-V measurements were made before irradiation and at several 1-MeV electron fluences, using the mercury-gold probe technique. While a detectable amount of interface states was introduced by the radiation, it was possible to extract reasonable data on the radiation-induced fixed oxide charge density. These results are shown plotted in Figure 17. The calculation normalizes the different thicknesses of the two films. Clearly, the oxide containing the additional phosphosilicate layer is considerably

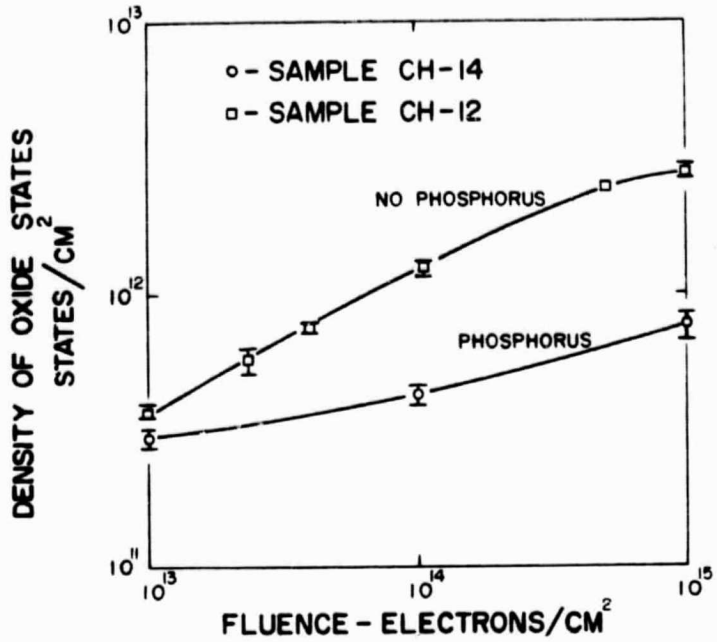

Figure 17. Comparison of radiation sensitivities of MOS capacitors containing composite insulator layers, using 1-MeV electron irradiation. Voltage shifts are normalized for thickness and expressed in charged states per cm². These samples had no gates and hence were floating during bombardment.

less sensitive than the simple thermal oxide, and the relative and absolute magnitude of the radiation effects agree with the results for the semi-integrated transistors shown in Figure 15.

The exact mechanism by which P_2O_5 layers reduce the radiation sensitivity or the optimum combination of variables by which the maximum in reduced radiation sensitivity can be obtained is still not known, and many more experiments will have to be done to answer these questions.

F. PRODUCTION-LINE TRANSISTORS

1. TA 2578 Transistors

The TA 2578 transistor is a commercially available developmental type MOS transistor used for chopper and low-frequency amplifier applications. The device is particularly suited to radiation effects work

because of its relatively large gate capacitance (2 to 3 pF), thus allowing C-V measurements to be made as well as transfer characteristic. The fabrication procedure for the device was as follows. The starting material was 20 ohm-cm p-type silicon. The n-type source and drain regions were doped to a surface concentration of approximately 10^{19} cm^{-3}. The channel width was approximately 10^3 microns and its length 10 microns. It was arranged in a closed rectangular type geometry to eliminate leakage effects. The thickness of the gate oxide was approximately 2000 Å and contained layers of thermally grown ("wet-grown") oxide and a layer of chemically deposited, phosphorus-doped oxide. Contacts to the device were made by evaporation of aluminum. After the contacts were evaporated, the device was treated in forming gas at an elevated temperature for several minutes.

Some preliminary measurements of this device under radiation were previously reported[21]. Two peculiar properties of the device were noted:

(1) Under bombardment by electrons or cobalt-60 gamma rays with the gate grounded, there is a shift in the transfer characteristic toward more positive gate voltage.

(2) The post-irradiation transfer characteristic is bias-unstable in a direction opposite to the ionic-drift instability. A slow interface trapping model was postulated to explain this effect.

In light of the positive shift in transfer characteristic under electron irradiation, further study of this device was carried out. Devices were bombarded with 1-MeV electrons, and the I_d-V_g and C-V characteristics were recorded (the C-V characteristic was measured with the drain shorted to the substrate and the source floating). Figure 18 shows the effect of electron irradiation on these characteristics. The solid curves are the pre-irradiation characteristics, and the dotted curve shows the characteristics after the devices have received a fluence of 2×10^{12} 1-MeV electrons/cm^2. Several interesting results are indicated in these curves. First, although the transfer characteristic shifts toward more positive gate voltage, the shift in flat-band voltage is negative. Hence, the positive shift in transfer characteristic can be assigned, in this case, to the generation of interface states and not to the trapping of fixed negative charge in traps deep in the oxide. Secondly, it can be deduced from the C-V curve that the states introduced by the radiation are distributed throughout the forbidden gap of the semiconductor. An estimate of the density of interface states that are being introduced by the radiation can be made by taking the difference between the shift in flat-band voltage and the shift in the threshold voltage (gate voltage for $I_d = 2 \times 10^{-5}$ A). Essentially we are looking at the broadening of the C-V characteristic. This has been done for several samples which were

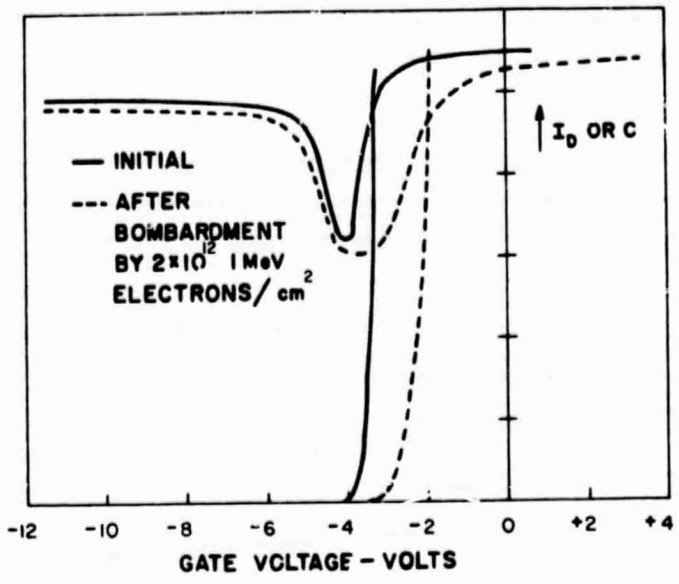

Figure 18. Correlated C-V and I_d-V_g characteristics of TA 2578 transistor before and after irradiation at zero irradiation-bias (gate grounded during bombardment).

irradiated with the gates grounded. The results are shown in Figure 19. As can be seen from the figure, the spread in the data was quite large. It was not possible, in this case, to make wafer identifications. The large spread in data indicates that this effect may be a very sensitive function of one of the processing steps. The large spread in the data also precludes, at the present time, a determination whether this effect depends on the gate bias during irradiation. In experiments on this device in which gate bias was applied during irradiation, it was not possible to discern any difference in the introduction rate of the interface states with or without irradiation bias. However, when the device is irradiated to medium dose levels with gate bias applied, the threshold voltage now shifts in the negative direction (i.e., the broadening of the C-V characteristic is the same for a given fluence but all the characteristics shift toward more negative voltage). Figure 20 shows the threshold voltage as a function of fluence for gate biases of 0 V* and $\pm$ 10 V applied during the irradiation. There are several points of interest in this curve. First, the application of gate bias during the irradiation caused the oxide-charge build-up with the net effect that the threshold voltage shifted in the negative direction. Secondly, under negative bias; the shift in threshold voltage with increasing fluence reversed direction at a fluence value of approximately 10^{13} e/cm^2. Under

* Gates were grounded during bombardment.

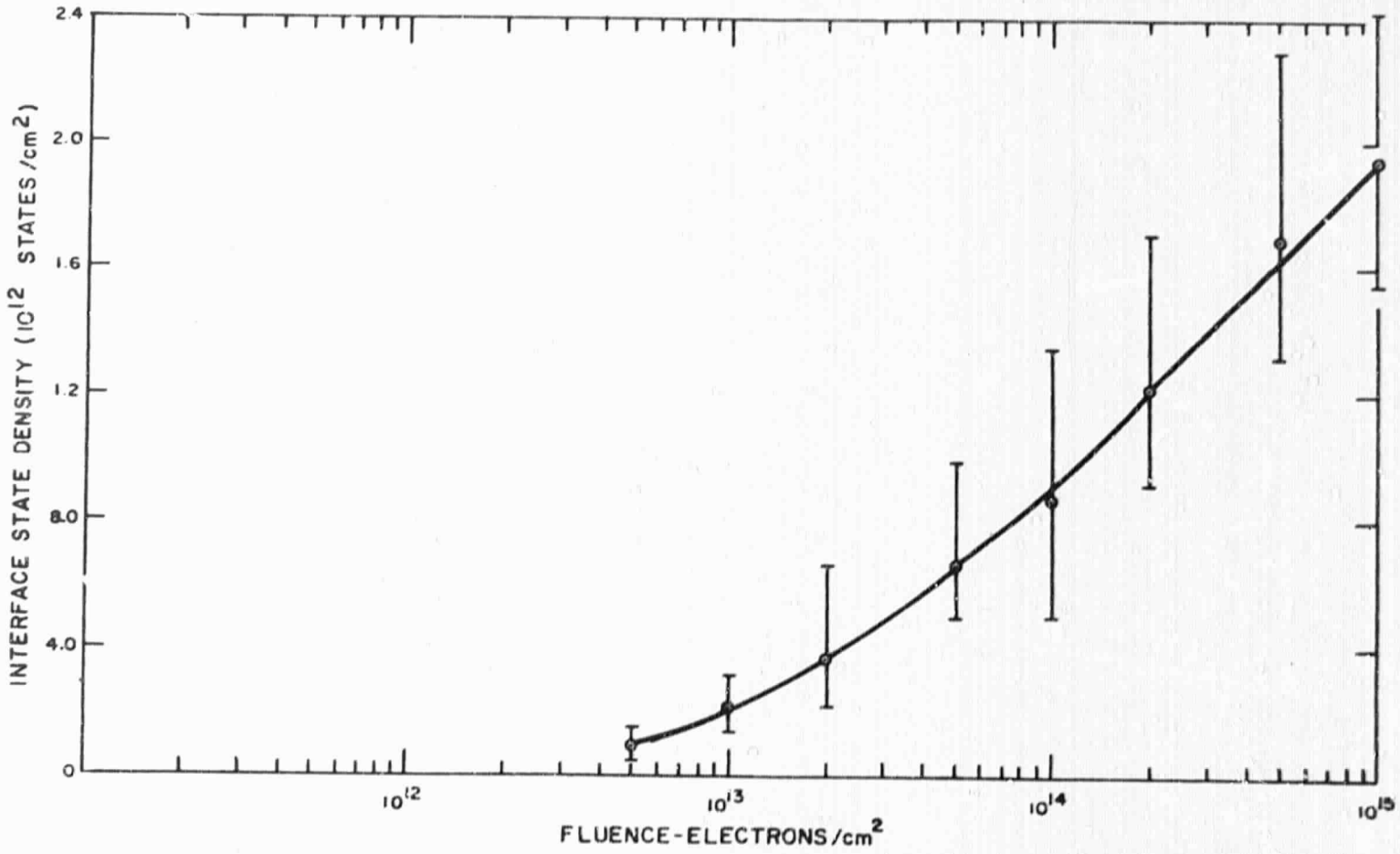

Figure 19. Generation of interface states in several samples of TA 2578 transistor during 1-MeV electron irradiation at zero irradiation bias. "Flags" indicated spread of results; points indicate average value. Gates were grounded during bombardment.

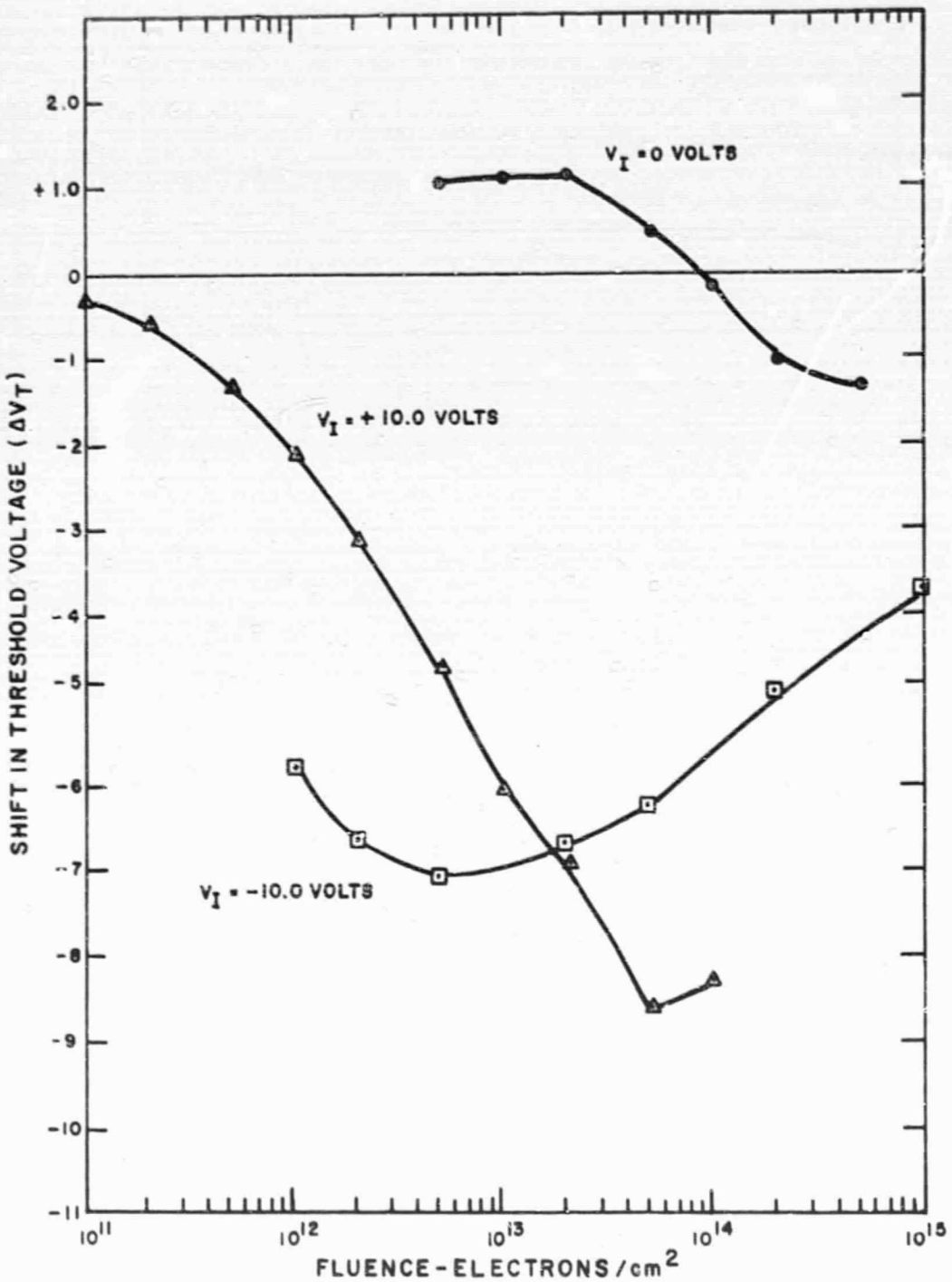

Figure 20. Radiation-induced shift in threshold voltage (gate voltage for I_d = 2 x 10^{-5} A) vs. 1-MeV electron fluence for three irradiation-bias conditions (TA 2578 transistor).

positive bias, some reversal of the ΔV_T also occurred, although irradiations have not yet been carried to a high enough fluence level to see if the threshold voltage decreases monotonically as for negative bias. A similar peaking effect has been observed by Newman and Wannemacher in certain p-channel transistors[59]. These authors have observed this peaking effect only in open-geometry transistors when irradiated with greater than -20 volts negative bias applied to the gate. Also, no broadening of the C-V curve was observed.* Since the particular device studied here has an almost completely closed geometry and since the peaking effect is observed at considerably lower voltages it is probable that the effect observed here is different from that observed by Newman and Wannemacher. One possible explanation of the effect described in this report might be that the introduction of new interface states, which we can infer from the broadening of the C-V characteristic, might tend to compensate the oxide charge and hence cause the reversal. This hypothesis, of course, requires more verification.

2. Semi-Integrated "Pattern 7" Transistors

The RCA "Pattern 7" transistor has been used as a test vehicle for the development of fabrication techniques for several logic circuits. Four MOS transistors are available, the source of one serving as the drain for the next, and so on.

Through the cc[illegible]f the Advanced Development Group, RCA Electronic Components and Devices, many samples from 5 different batches of these transistors have been made available, with wafer identifications and detailed processing data for each batch. Samples of whole silicon wafers oxidized in the ovens used for gate-oxide growth on these transistors were also supplied. It was thus possible to assess the variations in radiation sensitivity to be expected in transistors grown in pilot-line conditions and with several important but well-controlled variations in oxide process.

Figure 15 compares the data obtained for all batches of "Pattern 7" devices.

As indicated in Figure 16 (inset), the "Pattern 7" transistor is a "semi-integrated device, with bar geometry of source and drain diffusions. Channel length is about 0.010 in. and channel width is variable, but normally about 0.0003 in. In the samples employed in the present project, the gate insulator was composed of several layers, as indicated in Table III. Growth of thermal oxide was followed by one or two coatings of pyrolytically deposited oxides. These layers then require a high-temperature treatment to increase density and film integrity ("densification").

* P. Newman, private communication.

The performance data and irradiation results for the "Pattern 7" devices were given as a comparison with capacitors containing composite oxide layers in Section V-E.

3. Complementary Integrated Circuits

Some early-development samples of complementary inverter units, containing two p-channel and two n-channel transistors on the same chip, were also made available by the same group that supplied the "Pattern 7" devices. Each transistor could be tested individually or as a logic circuit. In this way, it was possible to investigate the effect of extra diffusion steps and impurities on the gate oxides grown on the same chip. Gate oxides are grown simultaneously for n- and p-channel units. The transistors employed geometry similar to that used in the "Pattern 7" transistor. The substrate was n-type silicon, into which was diffused a p-type "well" which acted as the substrate for the n-channel transistors.

On irradiation to 1-MeV electron fluences greater than 10^{13} e/cm^2 these devices tended to break down. Data up to this point, however, indicated that the shifts induced at zero irradiation bias were of the same order of magnitude for n- and p-channel devices on the same chip and of values similar to the better "Pattern 7" devices, namely about 1 volt shift at 10^{13} e/cm^2.

G. SPECIAL EXPERIMENTS

1. Crystallographic Orientation

Samples 7a and 7b were both oxidized in an rf-heated furnace in dry oxygen at 1100°C and then annealed in-situ in helium at the same temperature. Sample 7a was (111) orientation and 7b was (100) orientation. C-V characteristics of both samples had near zero values of V_{fb}. Irradiation to a fluence of 10^{13} 1-MeV electrons/cm^2 with no applied oxide field resulted in parallel shifts along the voltage axis. The fixed oxide charge induced by the radiation was the same in both samples, indicating that the crystallographic orientation of the substrate does not affect radiation sensitivity, provided that the interface is already low in interface state concentration, i.e., in a state of high order.

2. Oxide Thickness Effects

As a study of the effect of oxide thickness on radiation sensitivity, several samples of oxide were prepared in an identical manner except for the duration of the oxidation. The oxidations were carried out in steam at 1100°C followed by annealing in hydrogen at 500°C for 30 minutes. The resulting sample thicknesses were 1200 Å, 2430 Å, and 6190 Å. The pre-irradiation character of the interface was not as good as was observed in

other samples, and when the samples were bombarded under negative bias to a fluence of 10^{13} electrons/cm^2 some interface states were introduced. However, it appeared that, as in previous experiments, the thickness of the oxide had no major effect on the charge density produced in the oxide by radiation when no electrical field was applied across the oxide. However, when the field exceeded approximately 2 $\times$ 10^5 volts/cm, the thicker oxides were more strongly affected. One interpretation of this effect might be the increased number of secondary electrons produced in the thicker oxides. The interpretation of the data was somewhat obscured by the radiation-induced generation of interface states as well as by the slightly different initial oxide charge densities for the three samples studied.

3. Stepwise Etch Dissolution Experiments

For an experimental verification of the proposed general model for the radiation-induced positive oxide charge in MOS structures, and particularly for a quantitative description of the oxide space charge build-up, it is important to know the profile of this radiation-induced fixed oxide charge density over the depth of the oxide. Von Hippel's theory predicts that, for any irradiation-bias value, a steady-state thickness of space charge will be achieved when all the hole traps within this thickness have been saturated with holes, and that the density of the space charge in the oxide would decrease with distance from the oxide-silicon interface, if the irradiation were carried out with positive voltage on the gate electrode. For different spatial distributions of hole traps, the extent of the space charge and the saturation value for volume density of charge in the oxide (Q_{sat}) will have a different functional dependence on the irradiation bias. Von Hippel's theory assumed a uniform spatial distribution. This results in a dependence of the form $\Delta Q_{sat} \propto V^{1/2}$.

The assumption of hole traps at a single energy level and uniformly distributed throughout the insulator is somewhat over-simplified and can only serve as a first approximation in gaining understanding of the radiation process. Actually, there is ample evidence that insulators have a wide distribution of defect states throughout the forbidden gap, even though the density of certain levels may be large as compared with that of the quasi-continuum of states.

Furthermore, it is reasonable to assume that, depending on the method of formation of the insulator film, gradients exist in the spatial distribution of the traps. A thorough treatment of the bias dependence of the radiation damage has to take into account all the levels, and their spatial distribution. It is quite possible, however, that there will always be a discrepancy in different authors' experimental results because of the different defect structure of insulator films prepared in various ways.

The general features of this oxide charge distribution, for zero-bias irradiation, have been confirmed in earlier experiments by one of the authors[3] and by Grove and Snow[4]. This was achieved by stepwise removal of layers of silicon dioxide with a buffered etch, thickness determination by ellipsometry and measurements of the oxide charge by the mercury-gold probe technique. The results of this study are shown in Figure 21. The fluence level used was 10^{15} 1-MeV electrons/cm^2. Because

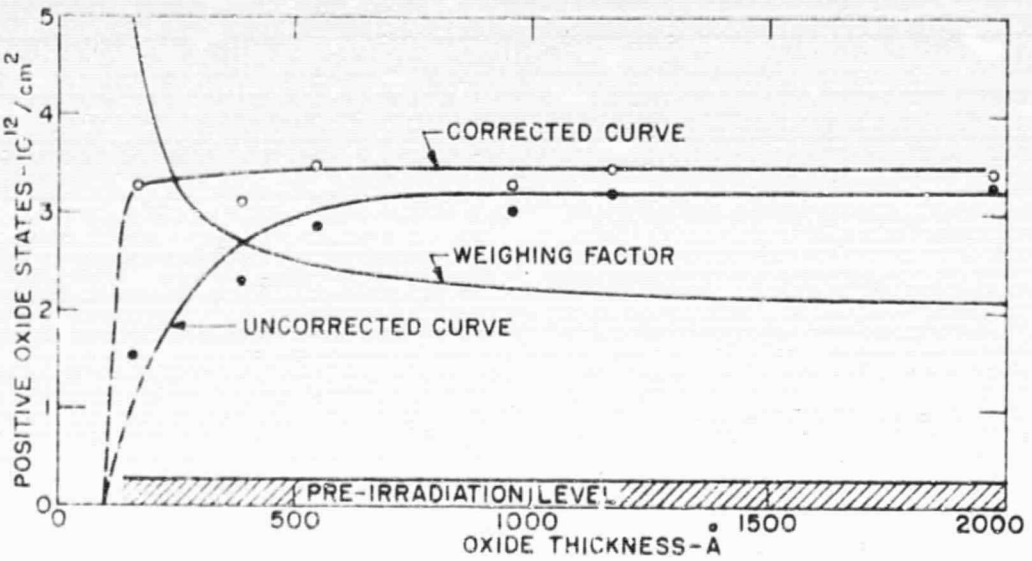

Figure 21. Spatial location of fixed oxide charge within dry-oxygen grown oxide irradiated with 10^{13} 1-MeV electrons/cm^2 under zero irradiation bias. Successive oxide layers were removed by etching. Weighing factor is a correction for the imaging of some of the charges in the metal at oxide thicknesses below 1000Å (as explained in the text). Gates were grounded during bombardment.

the "gate electrode" moves closer and closer to the oxide charge with each removal of an oxide layer, some of this charge is imaged in the metal, and to find the actual oxide charge, a simple electrostatic correction has to be applied, i.e., a weighing factor. If we assume that the positive oxide charge builds up from the silicon-silicon dioxide interface, then this correction has the form

$$(N_{ss})_{actual} = \frac{(N_{ss})_{measured}}{1 - \frac{x_o}{2\ t_{ox}}} \qquad (8)$$

where t_{ox} is the oxide thickness and x_o is the distance, from the Si-SiO_2 interface, to which the traps are filled. Clearly, since x_o is the parameter we wish to determine, we must use some form of self-consistent analysis of the data whereby we choose some value for x_o and then see if it gives a reasonable result. This was done for the data shown in Figure 21 with a value of x_o = 100 Å. For this corrected curve we can see that almost all the positive charge is indeed within 100 Å of the Si-SiO_2 interface. This is presumably the region from which radiation-excited electrons can escape from the oxide in the absence of an applied bias. However, in the presence of applied bias, the charge profiles are likely to extend to greater depths in the oxide.

In the present project it was of interest to determine the form of these deeper charge profiles induced by bias. Such tests would lay the ground work for analyzing the effect to be expected from cyclic or continuous bias such as might be expected during the operation of MOS devices in satellite circuits.

Accordingly, several capacitors were bombarded while positive or negative bias was applied to the gate. Large-area gates were used so that the area which was subjected to bias-irradiation could easily be indexed and found again after removal of the gate electrode and etching of the oxide. Successive oxide layers were then etched off and C-V measurements were made between etches.

The results of such an experiment, in which +5.0 V bias and a fluence of 1×10^{13} e/cm^2 were used, are shown in Figure 22. It can be seen that, if it is assumed that most of the radiation-induced charge is within 200 Å of the Si surface, and if the proper electrostatic correction for this condition is then applied, the results are reasonably self-consistent. The rounded shape of the corrected curve, however, indicates that some charge has also been trapped still deeper in the oxide.

The results of a second experiment, in which a -10.0 V bias and a fluence of 1×10^{15} e/cm^2 were used, are shown in Figure 23. Here the analysis becomes more difficult since one now has to be concerned with space-charge buildup from both interfaces. The electrostatic correction factor for space-charge buildup from the metal-silicon dioxide interface is:

$$(N_{ss})_{actual} = (N_{ss})_{measured} \frac{2t_{ox}}{(t_{ox} - x_2)^2} \qquad (9)$$

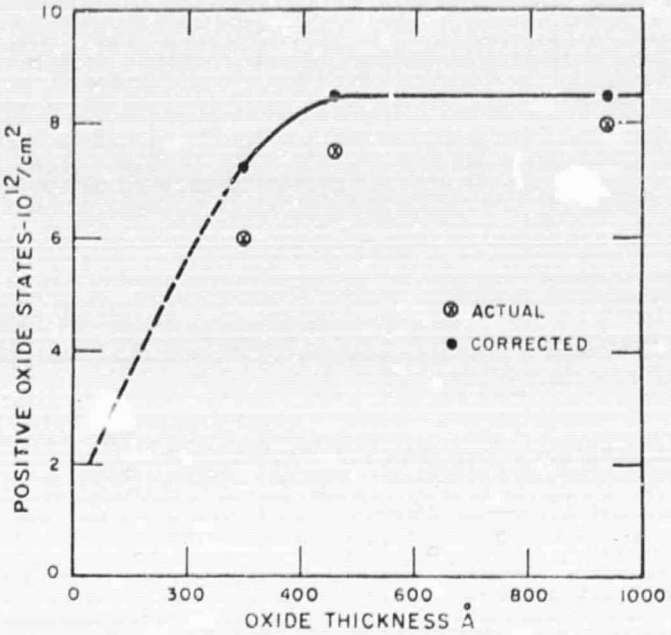

Figure 22. Spatial location of fixed oxide charge within steam-grown oxide irradiated with 10^{13} 1-MeV electrons/cm^2 at an irradiation bias of +5 volts. Correction factors as for Figure 21.

where x_2 is the distance from the silicon-silicon dioxide interface at which the boundary of the space-charge occurs. At present, we can make no reasonable assumption about x_2, and hence the data shown in Figure 23 have been left in raw form. However, it is of considerable interest to find that a large amount of charge remains in the oxide, even when etched to a thickness of 200 Å (probably over 5 x 10^{12} states/cm^2 after electrostatic correction). Thus, not all of the radiation-induced positive charge in the sample resides near the metal-oxide interface, as would be expected in the simplest model[1]. A reasonable picture would be that of two space-charge regions, one near the silicon-oxide interface and one near the metal-oxide interface. Actually, for all bias conditions, a certain amount of charge build-up occurs at both the semiconductor-oxide interface and the metal-oxide interface. However, the charge build-up from the metal-oxide interface would be expected to be the strongest in the negative-bias case and weakest in the positive-bias case. This situation is evident in the data shown in Figures 21, 22, and 23, if these data are considered in the light of the following analysis.

Suppose that two space-charge regions are formed in the oxide as a result of irradiation, one in the region of the semiconductor-oxide

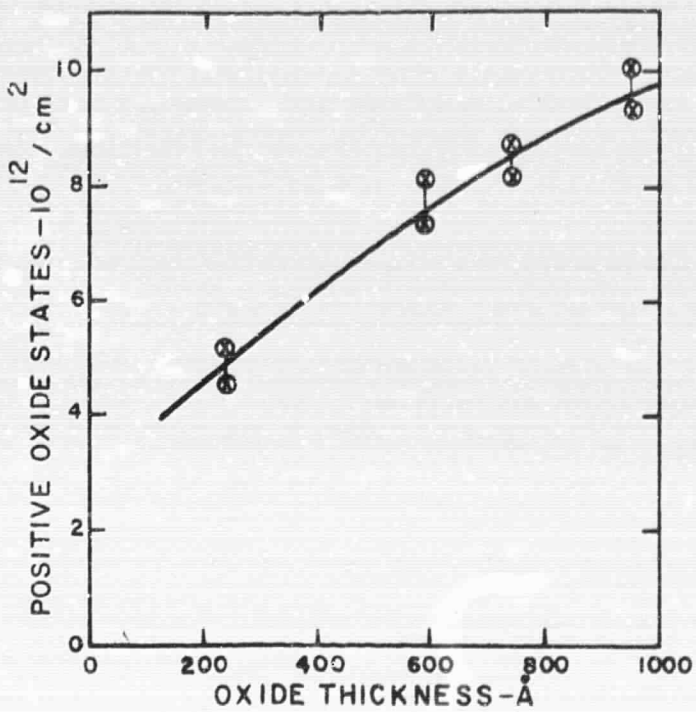

Figure 23. Spatial location of fixed oxide charge within steam-grown oxide irradiated to a fluence of 10^{14} 1-MeV electrons/cm^2 at an irradiation bias of -10 volts.

interface, the other in the region of the metal-oxide interface. In our model, the semiconductor-oxide interface is located at position x = 0 and the metal-oxide interface at position x = t_o so that the thickness of the oxide is t_o. We also assume that the density of trapped charge near the semiconductor face is qN_1 coulombs/cm^2, this region extending a distance x_o into the oxide; the density of trapped charge near the metal-oxide face is qN_2 coulombs/cm^2, this region extending from the metal-oxide interface out to x = x_2. The image of these charges in the silicon, Q_{Si}, is then given by

$$Q_{Si} = \int_0^{t_o} \left(1 - \frac{x}{t_o}\right) \rho(x)\, dx \qquad (10)$$

where, $\rho(x)$ is the oxide charge distribution described above. Hence, this becomes

$$Q_{Si} = qN_1 x_1 \left[1 - \frac{x_o}{2t_o}\right] + qN_2 \left[\frac{(t_o - x_2)^2}{2t_o}\right] . \qquad (11)$$

What we measure in a step dissolution experiment is the change in Q_{Si} as the oxide thickness, t_o is decreased. With this measurement, however, the fact that etching removes part of the space charge must not be neglected. Therefore, the above expression must be rewritten:

$$Q_{Si} = \begin{cases} qN_1 x_1 \left[1 - \frac{x_1}{2t_o}\right] + qN_2 \left[\frac{(t_o - x_2)^2}{2t_o}\right] & t_o \geq x_2 \\ qN_1 x_1 \left[1 - \frac{x}{2t_o}\right] & x_1 \leq t_o \leq x_2 \\ \frac{q N_1 t_o}{2} & t_o \leq x_1 \end{cases} \qquad (12)$$

From this expression, then, the rate of change of the silicon image charge as the oxide is etched away can be obtained:

$$\frac{dQ_{Si}}{dt_o} = \begin{cases} \frac{qN_1}{2}\left(\frac{x_1}{t_o}\right)^2 + \frac{qN_2}{2}\left[1 - \frac{x_2}{t_o}\right]^2 & t_o \geq x_2 \\ \frac{qN_1}{2}\left(\frac{x_1}{t_o}\right)^2 & x_1 \leq t_o \leq x_2 \\ \frac{qN_1}{2} & t_o \leq x_1 \end{cases} \qquad (13)$$

It can be seen that the initial rate of change of Q_{Si} will be larger as the extent of the space charge region at the metal-oxide interface is made larger (i.e., as x_2 is made smaller).

Figure 24 shows the "states imaged in the silicon, (Q_s/q)", normalized to the initial number of imaged states, (i.e., the number of imaged states before any oxide is etched away) as a function of the oxide thickness. The three curves are for positive, zero, and negative irradiation bias. As can be seen, the initial rate of change of the charge imaged in the silicon is greatest in the negative-bias case, indicating that charge build-up from the metal-oxide interface is more important in negative-bias irradiations.

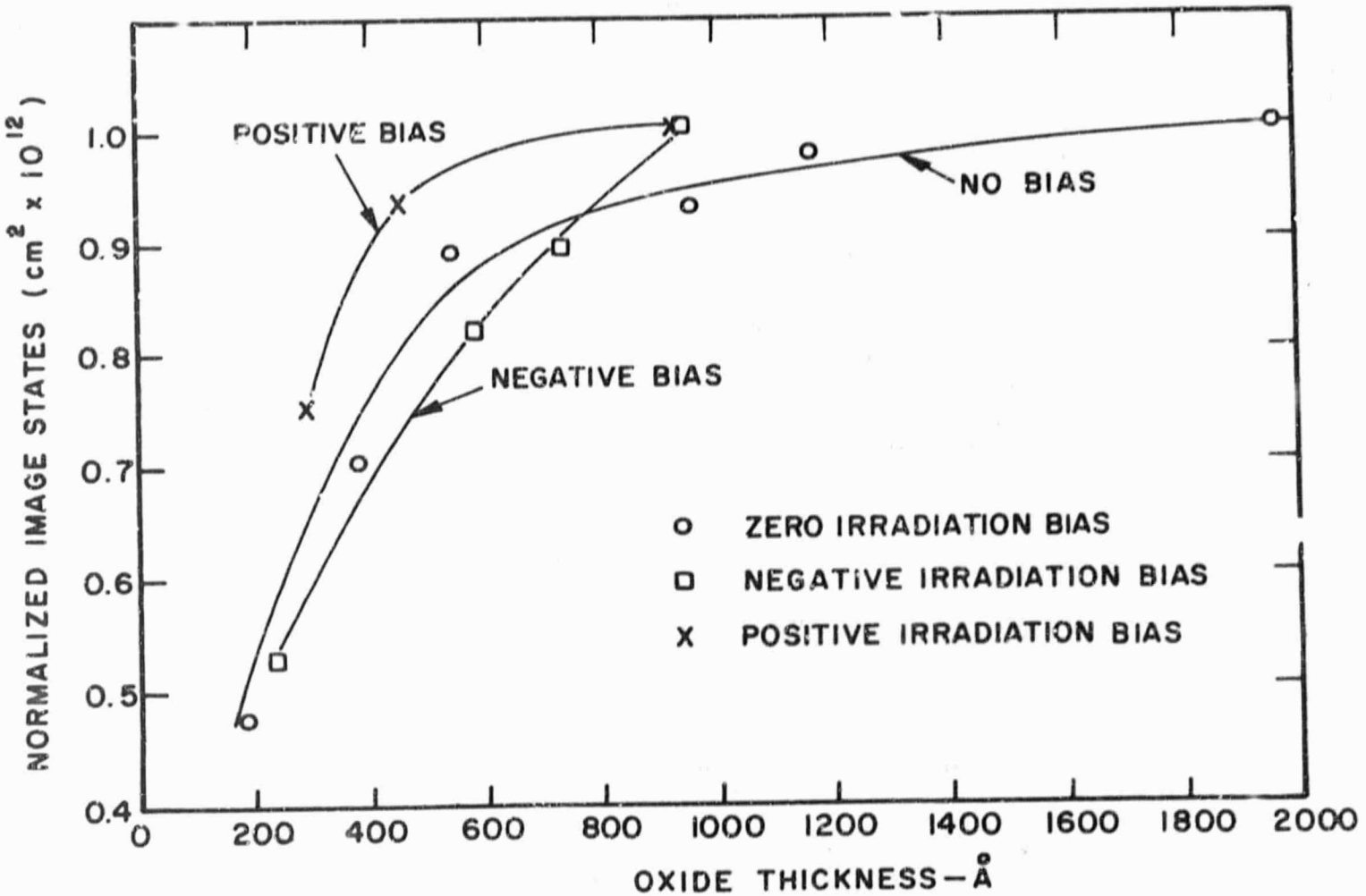

Figure 24. Comparison of the uncorrected curves shown in Figures 21 through 23 on a normalized scale of image charge vs. oxide thickness. These curves show the "greatly" increased slope near the original metal-oxide interface exhibited in the negative-bias case.

VI. DISCUSSION

A. VARIATION IN SENSITIVITY

In this section we will discuss further he factors which affect sensitivity of oxides to radiation. The reference radiation level chosen will be 3×10^5 rads (equivalent to about 10^{13} 1-MeV electrons/cm^2), both because this is well match i to the typical space mission dose and because the most data exist tor this dose range, both in the present project and in other workers' reports. In this respect, the study made here will differ from that made by Snow et al.[25], in which the authors irradiated until the radiation-induced C-V shifts no longer changed. This requires doses well in excess of 10^7 rads. Such doses are too high to be of direct interest in determining the behavior of MOS systems in typical space environments. It appears from the present work that the shape of the rise of ΔV with fluence (see, e.g., Figure 25) varies significantly from oxide to oxide. Moreover, as again notable in Figure 25 the curve shape of ΔV vs. dose is also radically different for different bias conditions.

Thus, it will probably not be possible tc derive simple general model fluence-dependence curves for MOS transistors (as was possible, for example, with solar-cell radiation degradation) and to extrapolate, from ΔV data at one dose level, to ΔV values at higher or lower dose levels.

For this reason it is necessary to study the relative radiation sensitivities of MOS devices at dose levels quite close to those of ultimate interest.

The objective of the present discussion is to compare the radiation-sensitivity of the various MOS systems tested. As has been seen earlier, the most valid criterion of sensitivity is probably the charge density induced in the oxide layer by a given radiation dose.

However, this quantity cannot be calculated from ΔV_T in transistors if the oxide thickness is not known. Thus, to compare commercial transistors we will cite ΔV_T as measured. We will compare the relative merits of capacitors and intercompare the capacitor and transistor group by following arbitrary conversion. Given an observed ΔV_{fb} shift in a capacitor of oxide thickness d (micrometer) at an absorbed dose of 3×10^5 rads, we will multiply ΔV_{fb} by $0.211/d$. The result is the ΔV_{fb} value which would have been obtained from the same radiation-induced charge density in any MOS device with an oxide layer of thickness 0.211 μm. We can, thus, at once validly compare various capacitors and also conveniently intercompare capacitors and transistors on the practical

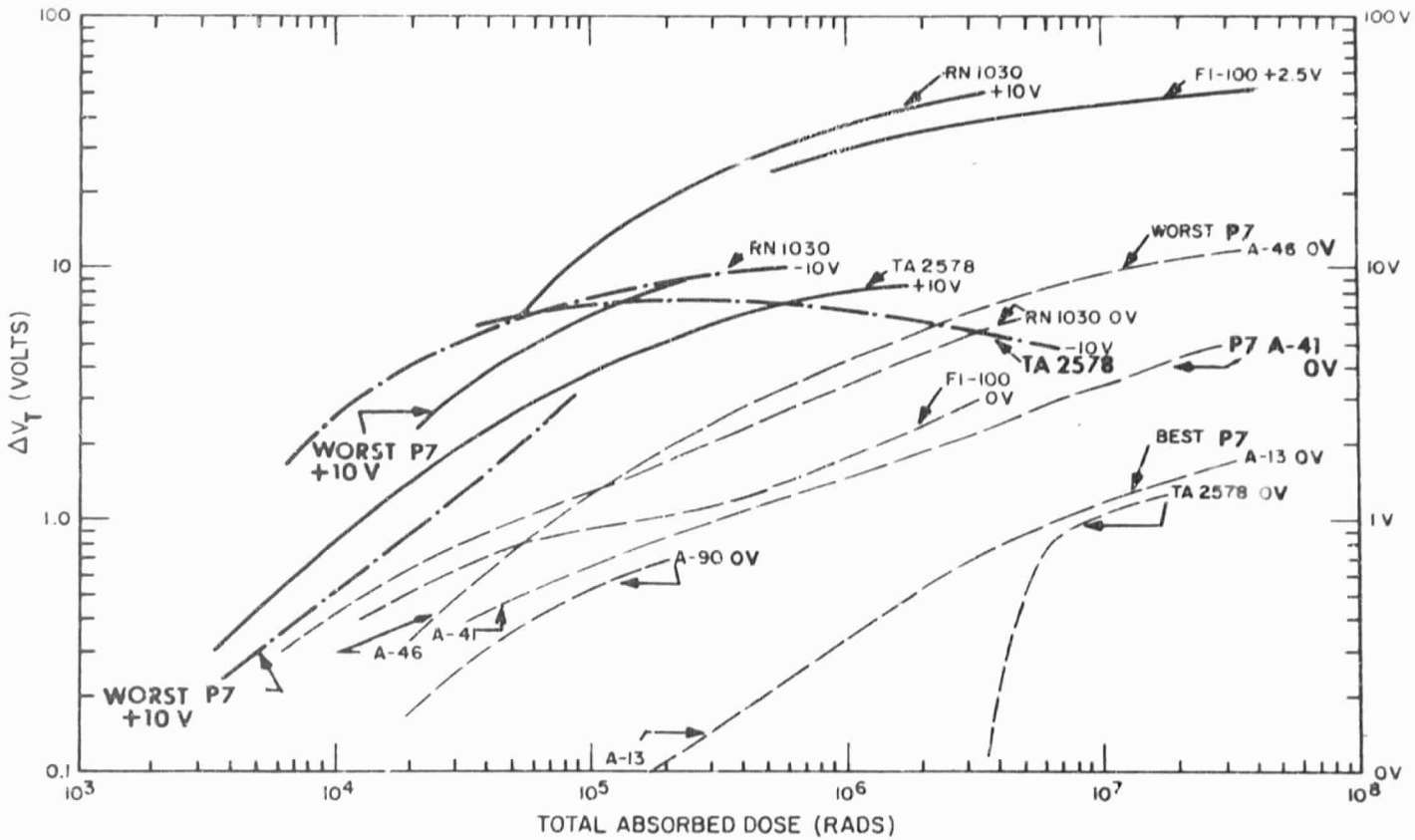

Figure 25. Collection of data on radiation-induced threshold voltage shifts in commercially available, mass-produced MOS devices. Irradiation bias and manufacturer's type are indicated on the curve. The equivalent absorbed dose was calculated from the original data on the 1-MeV or 1.5-MeV electron fluences or Cobalt-60 gamma ray fluences used. P7 = RCA "Pattern 7" semi-integrated transistor (designations A-13, -41, -46, and -90 indicate various batches of P7 transistor; TA 2578 is the RCA type number of a discrete commercially available unit; RN-1030 is a Raytheon series number; FI-100 is a Fairchild series number.

and intuitively sensible scale of volts. The thickness of 0.211 μm is chosen for convenience, being that thickness of silicon dioxide at which a positive charge density of 10^{11} positive charges/cm^2 leads to negative shift in pinchoff voltage of 1 volt, and 10^{12} charges/cm^2 leads to 10 volts and so on. The sensitivity data emanating from the present project can be summarized as follows: Zero bias sensitivities of MOS capacitors at an absorbed dose of 3×10^5 rads have been distributed: two with shifts of less than 1 volt in the negative direction, nine with shifts between 1 and 3 volts, twelve with shifts between 3 and 10 volts, and three between 10 and 20 volts. The corresponding results for transistors are (for RCA units batch-tested) four batches with shifts below 1 volt, one with shift between 1 and 3 volts; (these data no not include the special case of the TA 2578, in which all five batches exhibited a *positive* shift of 1 to 2 volts). Combining data on commercial types of MOS transistor from several authors[22,52,53] and the present project, the distribution is as follows: none below 1 volt, five makes with shifts between 1 and 3 volts (FI-100, RN-1030, SC-1129, MEM 511, and MEM 2009), and one above 3 volts (MM-2103). The apparent first conclusion, that commercial processes appear to be able to achieve a level of shift lower than the average for laboratory capacitors, may simply be due to the choice of a normalization factor for the capacitors based on oxide thickness of 0.211 μm. In a commercial transistor with an oxide thickness of 0.16 μm (a common oxide thickness), the same density of charge near the interface would produce 25% less voltage shift in the electrical characteristics* (the 0.211-μm thickness is chosen for reasons of convenience in conversion). Thus, the capacitor and transistor curves should not be compared on a competitive basis.

A trend of some interest seen in these charts is that, within the accuracy of this type of plot, there appears to be a constant relation, extending through laboratory capacitors and commercial devices, between the voltage shifts obtained under zero, negative and positive irradiation bias, the factor in each case being about three. This could be of some practical importance in developing testing techniques if, from a measurement of an unstressed device, one could make a statement concerning the behavior of that device when irradiated under bias stress.

This is a possibility which should be tested carefully in future work. There is a reasonable probability of success since, on the simplest model of the mechanisms of radiation effect in MOS systems, it is assumed that there is effectively a constant relationship between the hole-trap density near the interface (the region which is filled with charge during zero-bias irradiation) and the hole-trap density at points further into the oxide, which would only be filled with charge when under bias stress. In other words, this rule would follow if the *shape* of the hole-trap concentration profile were constant from sample to sample, even if the

*I.e., reduce the voltage shift scale for capacitors in Figure 23 by a factor of 0.75.

absolute densities changed. On the other hand, it is also quite possible that, in fact, considerable deviations in shape of the hole-trap profile occur from sample to sample. Only detailed bias dependence data over a carefully selected set of oxides could establish whether the bias-dependency of ΔV_{fb} can be kept constant over a group of oxides. From such data, it will then be possible to determine whether zero-bias irradiation will ever be valid as an indicator of radiation-sensitivity for all bias stress conditions.

Figure 26 shows a histogram of the distribution of voltage shifts for capacitors under zero-bias irradiation on a finer scale. The spread in data when it was attempted to repeat preparation in exactly the same way was considerably less than that seen in the lower peak. The concentration of data in the 2 to 4 volt region is, in fact, partly due to the establishment of routine methods of oxidation in an rf-induction furnace and steam oven, including routine annealing procedures. However, it is not yet perfectly clear what factors led to the improvements observed in certain samples. Further statistical data should contribute to the solution of this problem. The most likely process causing improvement is a cleaning procedure. In samples M13R, M14R, and 7a, a special cleaning procedure was used, involving vapor-etching of a layer of silicon by heating in hydrogen above the temperature at which silicon and hydrogen react; oxygen was then admitted without any further opportunity for surface contamination; the result would have been an unusually uncontaminated, and hence particularly reactive, surface.

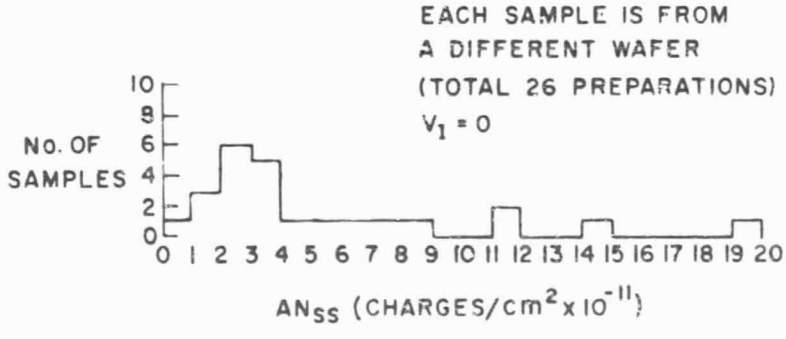

Figure 26. Histogram of voltage shifts observed in MOS capacitor samples irradiated to 1-MeV electron fluence of 10^{13} electrons/cm^2 at zero irradiation bias.

Two possible models would fit the effect of silicon surface purity on radiation sensitivity.

(1) Lack of contamination could have allowed the growth of oxide configurations which are normally blocked by impurity atoms. An example

of such impurity-sensitive growth process is described by Revesz[54]. The growth of certain configurations of Si-O-Si-O chain termed "microheterogeneities" can be blocked by several types of impurity and defect. The existence of long, straight Si-O-Si-O chains can produce higher levels of electronic conduction than otherwise possible. It has been indicated by Snow and others[25] that the conductivity level in nitrides correlate well with their lower radiation-sensitivity (i.e., that higher conductivity allows the trapped charge to leak away).

(2) Certain impurities actually act as hole-trapping sites (an example known to act in this way is the lower valency state of cerium[56]); it is possible for such impurities to travel with the interface. On the other hand, there is no reason to think that samples exhibiting fairly high sensitivity were subject to any extra gross metallic contamination.

The extra-sensitive group seen in Figure 26 may constitute a group in which insufficient annealing was performed. Although, after oxidation, most of this group was heated at the oxidation temperature in an inert gas for over 15 minutes, subsequent hydrogen baking was short and at low temperature or not performed. While, according to Revesz, the action of hydrogen should be to reduce electronic conduction, the beneficial action of hydrogen in improving interface-state density in thermal oxides appears to be connected with the reaction of the hydrogen with undesirable impurities, and with unsatisfied or strained chemical bonds at the interface. Since the species thought to produce the hole-trap in silicon dioxide is a nonbridging oxygen atom, it would not be surprising that reaction with hydrogen would change the properties of this center. Arguing against the role of hydrogen are several experiments in which hydrogen treatment was varied on samples of the same wafer, and little sample-to-sample difference was noted. The conclusion seems to be that hydrogen annealing is one factor, but not the only factor in controlling radiation sensitivity, and that, if other factors are to be determined, all samples should be very thoroughly hydrogen-annealed first.

A comment which should be made concerning data on commercial transistors is that, when data from several different workers have been compared, the same transistor type has always behaved in fairly similar fashion. This indicates that the radiation sensitivity produced by a given production-line process remained fairly constant from batch to batch in the few cases tested. This is not to say that a minor change in a production process could not have radically affected sensitivity in either direction.

B. DOSE DEPENDENCE OF RADIATION SENSITIVITY

For all the MOS systems surveyed, there has been a striking similarity in the shape of the plots of radiation-induced shift (or charge buildup) versus dose. In Figure 25, data on RCA transistors examined in this project are compared with data on commercial transistors made by other manufacturers. Shown are data on the Raytheon RN-1030 and Fairchild FI-100, irradiated by Mitchell[52] using cobalt-60 radiation and measured by the C-V technique. It will be noted that the zero-bias dependence is most nearly monotonic, certain sections approximating a power-law curve ($\Delta V_T \propto \phi^{0.4}$). The negative-bias curve rises steeply and saturates early, while the positive-bias curve rises more slowly to saturation, exhibiting a curve resembling Mitchell's model.* In some production transistors, both positively and negatively biased samples have shown saturation followed by a reversal.

In the 12 examples of data on fluence dependence of shift in capacitors, under zero-bias conditions, produced during the present project, it is notable that the slopes of log ΔV_T vs. log D do not vary greatly from high-sensitivity samples to low-sensitivity ones, indicating that the same processes are probably taking place in both cases.

The phenomenon of saturation of shift followed by reversal observed in several batches of the RCA TA 2578 and also by Long[57] is, of course, of great practical interest since it provides a limit to the tolerance which a designer may have to provide, in his circuit, for the shift. It is not clear what process is causing the reversal. Some permanent increase in conductivity of the oxide may be produced by the radiation. On the other hand, the effect may be a product of interface changes which are manifested in the channel conductivity characteristics as reversals of the threshold voltages and are not true measures of fixed oxide charge.

C. METHODS OF REDUCING RADIATION SENSITIVITY

The main outcome of the present project is the indication that thermal oxides which have considerably lower radiation sensitivity than those found commonly in commercial use can be fabricated. Such thermal oxide films have been found while surveying a fairly wide range of laboratory-grown oxides available from several different furnaces. Experiments aimed at pin-pointing the exact process step which affects sensitivity most strongly in these simple oxides have not given clearcut solutions to the problem. One of the more likely candidates, post-oxidation

*Mitchell, Ref. 52: $\Delta V_T = - \alpha V_I (1 - e^{-\beta D})$ where α and β are constants, V_I is irradiation bias, and D is dose.

annealing procedures, has been tested in a controlled manner but the effect of varying the annealing procedures (hydrogen and inert gas) has been so small that it is tempting to eliminate annealing as an important variable. However, the groupings observed on analyzing differences between oxides with randomly different fabrication procedures suggest that post-oxidation hydrogen annealing may indeed be a key factor.

While the picture in simple thermal oxide films is still unclear, one oxide treatment used widely in mass production has been found to be beneficial. In controlled experiments, the addition of a phosphorus-containing coating to a thermal oxide was found to decrease its sensitivity by a factor of 2 to 3. With study to determine the ideal concentration and distribution of dopant, this effect, which can be termed the first clearly demonstrated "radiation-hardening" of an MIS insulator film, may produce a higher factor of improvement. Developmental transistors incorporating phosphorus-containing layers of the type described show the lowest radiation sensitivity observed in any known transistor structure (less than 10-V shift at 3×10^5 rads at +10-V irradiation bias); thus, it is clear that the process is well adapted to mass-production use.

It is thought likely that other extraneous treatments, such as intentional doping of the insulator film during growth, should also produce improvements in sensitivity. These improvements could come about either by modification of the conductivity of the oxide or modification of the charge-trap concentration (the minor increases in conductivity needed should not degrade transistor properties). Charge-trap modification could occur by two separate modes: (1) decrease of the hole-trap density by reaction of the dopant with a trapping site, and (2) increase in electron-trap density using atomic species with an affinity for electrons (e.g., higher valences of cerium ion).

D. RECOMMENDATIONS FOR HARDENING OF MOS DEVICES

It is not yet possible to give a recipe for producing high-performance MOS transistors which are insensitive to radiation. However, several ground-rules for improving radiation sensitivity are made clear by the present work:

(1) Reject oxidation processes which yield high interface-state and fixed charge densities after oxidation and annealing.

(2) Incorporate pyrolytically deposited, phosphorus-doped layers in the gate oxide structure.

(3) If the greatest possible insersitivity is required, pre-irradiate all samples to be used to the expected integrated dose and at the bias stress levels expected. Select the least affected

sample for use. The radiation effect may then be annealed out without any residual damage, and the devices, when re-irradiated, can be expected to follow closely the course which they followed on the first irradiation.

VII. CONCLUSIONS

The work described here has uncovered several important features in the relationship of MOS device fabrication procedures to the final radiation sensitivity of the device. It is possible to vary radiation sensitivity in oxides (as manifested in their electrical characteristics) over more than an order of magnitude, the best samples being much less sensitive than those now available on the commercial market, sensitivity being measured in terms of charge concentration buildup in the oxide. While some clues are emerging as to the ideal techniques for repeatably producing low-sensitivity oxides, no recipe is yet possible. However, it is concluded that only a moderate amount of further statistical study of a few candidate processes should reveal the correct set of oxide growth and annealing conditions for low radiation sensitivity. To produce the ultimate in insensitivity to radiation, extra processes can be added to the above conventional steps. One is phosphorus-glass coating, already widely adapted to commercial use. Another is stringent vapor-etch cleaning of samples *in situ* in the oxidation furnace.

It is estimated that, using these measures, supported by selection, the shifts obtained in a typical space mission (e.g., 3×10^5 rads in 1 year from all particles) could be made as low as 0.5 V if the device is at zero gate bias throughout the mission, 2.5 V if under positive gate bias, and 2 V if under negative bias.

Preparative factors for MOS transistors which can be ruled out with fair certainty as to their effect on radiation sensitivity are:

(1) source-drain spacing or length,
(2) gate metallization,
(3) crystal orientation of original silicon (experiments by the authors[50] and Snow et al.[25] have established this),
(4) oxide thickness, and
(5) mobile metal ion (indicated by several experiments by K. Zaininger[58] not reported here).

Preparative factors which cannot be ruled out are:

(1) oxidation temperature,
(2) uncontrolled impurities other than mobile metal (indicated by the hydrogen-etch experiment, Section V-B.)
(3) phosphorus content of oxide (indicated by phosphorus-coating experiment, Section V-E.),
(4) hydrogen annealing (indicated by the distribution of sensitivities vs. processing procedures shown in Section V-B.),
(5) inert-gas annealing procedure, and
(6) oxidation atmosphere and temperature.

The question of relative superiority of oxide growth in steam or dry oxygen has not been settled. Figure 27 indicates the situation. While steam-growth leads to greater reproducibility of radiation sensitivity, dry-oxygen growth has produced a few samples with the lowest sensitivity ever observed.

An important effect as yet little characterized in radiation effects on MOS transistors is the formation of a new interface state under ionizing radiation. Production of new states must imply bond rearrangements. These are not easy to identify. However, the serious effect that these states have on transistor characteristics makes it important to study them further.

Future work should thus consist of:

(1) Statistical studies of the sensitivity of very clean steam-grown oxides, varying annealing times and temperatures in helium, followed by variable times of hydrogen bake, to be carried out on simple MOS capacitor structures.
(2) Statistical studies of the effect on radiation sensitivity of pre-oxidation gaseous etching procedures on samples oxidized in an rf-heated pedestal furnace, again using capacitor structures.
(3) Studies of the influence of hole-trap profiles by studying the variation of dependence of radiation sensitivity on irradiation bias for several different oxide growth-rate schedules.
(4) Studies of the effect of radiation on the production of bias-dependent interface states in MOS capacitors with guard-rings, and in transistors located on the same wafer.
(5) Studies to determine the effect on radiation sensitivity of different phosphorus distributions in MIS insulators and also the related effect of an insulator-insulator interface near the center of the insulator film, as in two-layer MOS gate oxides (again using integrated capacitors and transistors).
(6) Studies on other insulators which are suitable for MIS devices and now show promise of low radiation sensitivity, such as aluminum oxide and hafnium dioxide.

Techniques which will be of particular use in determining factors affecting radiation sensitivity, over and above those used at present are (a) study of the electrical and optical phenomena observed during thermal annealing of the oxide charge (including thermoluminescence) (b) study of photo-excited changes in oxide charge distribution (see Section III-F.), (c) fast sweeping and sampling of C-V characteristics, accompanied by time-lapse photography (to display, e.g., the shift of flat-band voltage of a device during irradiation, biasing or heating on the millisecond scale). Such circuits have recently been developed under RCA funds.

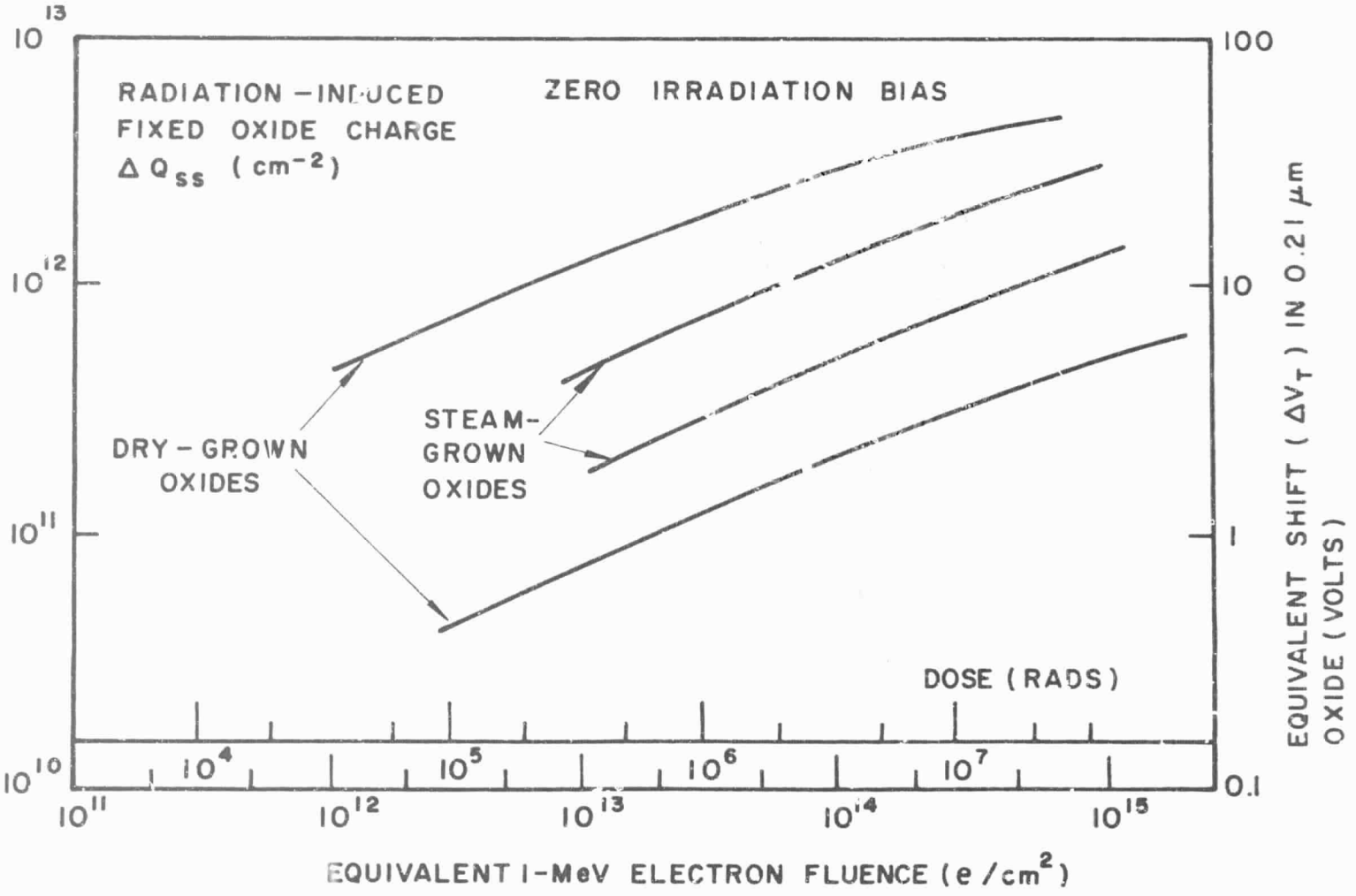

Figure 27. Upper and lower boundaries of radiation-sensitivity of MOS capacitors.

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