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NASA CR-66636

Issued: August 9, 1968
AED R-3325

CONTRACT NO. NAS1-7084

# Laminated Ferrite Memory System

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Prepared for

LANGLEY RESEARCH CENTER
NATIONAL AERONAUTICS AND
SPACE ADMINISTRATION
HAMPTON, VIRGINIA

RCA

RCA | Defense Electronic Products
Astro Electronics Division | Princeton, N J

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# ABSTRACT

A design study was conducted to determine the feasibility of developing a 131,072-bit random-access laminated ferrite memory system suitable for use in space flight. Based on the results of this study, a preliminary design for an engineering model was performed. The design indicated that all program goals, except power consumption, were feasible using the specified state-of-the-art laminated ferrite materials and peripheral driver, logic, and sensing devices. Total estimated power consumption was 25 watts at a 2-microsecond memory cycle time. Possible reductions in power to meet or exceed the design goal of 12 watts were shown to hinge principally on additional research and development to obtain more uniform, low-drive laminated ferrite materials, and on the development of improved sense amplifiers.

The design study and preliminary model design determined optimal memory wafer size, measured laminated ferrite material characteristics, and determined optimal methods of driving, terminating, and switching memory plane, word, and digit lines. The effort also included completion of logic and timing diagrams, design of hybrid word-line and digit-line drivers circuitry, selection of an integrated circuit family for required memory system logic, and the design of a sense amplifier. Using the parts and interconnections indicated by the preliminary design, a failure rate analysis was made which yielded an estimated probability of survival for one year in the space environment of 83.3%. The planned completion of the engineering model design and fabrication was discontinued and the program terminated by mutual agreement at the end of the preliminary design effort, due primarily to the unavailability of a production source for laminated ferrite wafers.

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# SECTION I

# INTRODUCTION

## A. OBJECTIVES

Contract NAS 1-7084 provided for the study, design, fabrication, and testing of a random access laminated ferrite memory system. The contract was to be conducted in two phases: Phase I to cover study and preliminary design and development; and Phase II to include final design, fabrication, and test of a 131,072-bit engineering model.

The objective of the Phase I study effort (stated in Langley Research Center's Statement of Work L-6645, dated May 5, 1967) was to develop a basis for design by performing the following study tasks:

- Memory plane process development,
- MOSFET logic development,
- MOSFET word and bit driver investigation,
- Hybrid integrated circuit word and bit driver investigation,
- Sense amplifier investigation,
- Peripheral circuits tradeoff study,
- Preliminary logic design,
- Preliminary packaging design,
- Preliminary reliability evaluation, and
- Phase I engineering report.

The Phase II objective was to design, fabricate, test, and deliver to LRC an engineering model of the memory system, together with a memory tester. The detailed requirements for the engineering model were to be developed during the study phase and presented to LRC for review and approval in the Phase I engineering report.

## B. PROGRAM SUMMARY AND KEY RESULTS

All Phase I study tasks were completed. Each task developed adequate data for the design of a feasible engineering model which would meet all program goals except power consumption. Also developed was an alternate design which could meet the power goal with an increase in memory cycle time.

The memory element selected consists of a laminated ferrite wafer containing 128 embedded conductors arranged into an orthogonal matrix of 64 conductors in each direction. The type 3515 composition (containing 12.5% ZnO, 22% MnO, 25.5% MgO, and 40% $Fe_2O_3$, and fabricated with a standard RCA Memory Products Division process) was selected over other compositions with slightly better temperature characteristics because all other compositions were excessively affected by digit line disturb currents.

Complementary MOSFET (metal oxide semiconductor field effect transistor) logic elements (single or dual circuits in 14-lead inline packages) were selected as the most advantageous MOSFET logic technique. Complementary MOSFET arrays were found to have advantages over the discrete logic elements, but are not available as production units. Discrete element designs can, with little change, however, be implemented with arrays when arrays become available.

MOSFET bit and word driver circuits were investigated, and it was concluded that these devices, at the drive current levels required for the memory system, are still in the development stage and will not soon be available as production units.

Designs for hybrid bit and word driver circuits were completed, breadboarded, and tested. Hybrid circuit suppliers affirmed that the circuits are feasible in hybrid integrated circuit form.

A sense amplifier was designed capable of detecting memory sense output signals as low as 1.0 millivolt lasting for 100 nanoseconds or more. This amplifier consists of two commercially available integrated linear amplifiers coupled by an RC network. Extensive breadboard testing verified the performance of this circuit.

In the peripheral circuits tradeoff study, an analysis was made of the relationships between cost, maximum operating speed, and power dissipation using a number of different logic element types. A graph was prepared showing the total estimated system power versus memory cycle time for several logic configurations, with and without sense amplifier power switching. The optimum lowest cost logic system configuration was found to require 7.4 watts of logic power to maintain a 2-microsecond

cycle time. Alternate systems were configured to consume less power, with longer cycle times and at higher unit cost.

A preliminary logic design was developed based on the configuration selected for 2-microsecond cycle time and lowest unit cost. This design, fully synchronous with a multiphase clock at 8 MHz, was shown to meet all of the system functional requirements.

Packaging considerations of the memory stack and electronic circuitry were investigated to develop a preliminary packaging concept. The design concept which evolved was based on the use of printed wiring boards to mount the memory planes and driver circuits. Other electronic circuits, mounted on commercial plug-in boards containing receptacles for inline modules, were connected with the memory planes through a printed wiring harness board.

The preliminary reliability evaluation resulted in the assignment of tentative parts failure rates to most of the memory system components, and a preliminary failure mode analysis. The results of these analyses show that the parts which were evaluated are satisfactory for ultimate flight use, and that the overall memory system has an estimated probability of successful operation in a flight environment of 91% for six months and of 83.3% for one year.

Although it appeared likely that an engineering model satisfying most of the explicit design goals of the contract could be produced from previous pilot-production samples of the type 3515 material selected, a future production source could not be guaranteed at this time. Perhaps of greater weight were the limitations of the type 3515 material in satisfying the implicit obectives for a material which could provide the growth potential for ultimate, extremely low-powered, high-capacity, highly miniaturized memories needed for many aerospace requirements.

As indicated previously, other initially promising laminated ferrite material compositions with very low-drive properties were found to be insufficiently characterized to permit reliable production at this time. Of equal importance was the determination of the unavailability in reliable production quantities of batch-fabricated driving and sensing components which are essential to properly exploit the properties of a low-drive material.

For these reasons, it became evident that the design and production of an engineering model would not demonstrate a major improvement in the state of the art, although valuable contributions had been achieved in individual preliminary circuit, logic design, and tradeoff analyses. In view of this conclusion, RCA proposed, and Langley Research Center agreed and directed, the termination of the effort at the conclusion of Phase I.

# SECTION II

# STUDY TASK REPORTS

## A. MEMORY PLANE PROCESS DEVELOPMENT

### 1. Initial Program Plans

The plan for this task, presented in the proposal and at the first review at Langley Research Center, assumed that three different ferrite materials might be used for this program. Type 47 material (produced in limited quantities at RCA Laboratories for research under Contract NASw-979 (I) for low-drive wide-temperature use) was selected for the first tests. The plan was to obtain samples of types 47, 3515, and 3750, and run tests to provide engineering data for the memory system design.

Type 47 material was selected for the initial investigations on the basis of the results of the prior contract. These results indicated that this composition, in addition to having a wider temperature range than types 3515 or 3750, was capable of operation with substantially lower drive currents, in a slower-speed, domain wall motion mode. Since these lower drive currents permitted a longer rise time of the read current, preliminary results also indicated that capacitive noise coupling into the sense amplifier would be sufficiently small that one-crossover-per-bit operation might be feasible. Tests of the samples of the two higher coercive force materials would provide a backup in case the type 47 samples were not useful.

The plan was based on making the Phase I samples and wafers for the engineering model at RCA Laboratories. Wafers could be made in sizes larger than the conventional 64-conductor size. For this reason, a study was planned, concurrent with the material tests, to find the best size and shape for wafers for the engineering model.

After choosing the best material type and the best wafer size and shape, the plan was to have new fabrication masks made and a set of completed wafers prepared and tested. It was also planned, as part of the study effort, to develop the detailed processes to produce wafers for the engineering model.

### 2. Type 47 Material Investigations

The material investigation started with type 47 material (5% ZnO, 19% MnO, 38% MgO, and 38% $Fe_2O_3$), based on results reported in previous work (Laminated Ferrite Memory — Phase II, Final Technical Report, Contract NASw-979, RCA

Laboratories, Princeton, N.J.). These results reported a minimum fully disturbed "1" signal of 1.6 mV peak at a read current of 100 mA, a write current of 70 mA, and bipolar digit currents of ±18 mA. Preliminary design analysis of the probable sensitivity of the sense amplifier indicated that a peak signal of at least 3.6 mV was needed for reliable operation of the memory system. A reported rate of increase of output with read current of 0.5 mV per 10 mA led to the selection of a minimum read current of 150 mA and write current of 100 mA as the initial levels.

A special test setup was designed for wafer testing, shown in Figure 1, using a Computer Test Corporation model 1551 program generator. Since this unit has four programmable ouputs, an additional digit driver unit was designed and built, which accepts "1" and "0" signals from two of the generator outputs and produces the necessary dual bipolar digit drive currents. The sense amplifier used was a differential integrated amplifier with a calibrated gain of 100. All connections were made with 50-ohm coaxial cable, with loops provided at the test wafer to measure the word and digit drive currents. A printed wiring board was designed and fabricated for mounting the test wafers so that the conductors were fanned out for more convenient connection.

The first sample wafers of type 47 composition were received in July 1967. These wafers (one of which is shown in the photograph in Figure 2) were expected to be identical to the wafers prepared during the previous program except that the firing schedule was changed from 24 hours at 2200°F to 2 hours at 2450°F. Previous experience at RCA Laboratories had indicated that these firing schedules resulted in equivalent wafer performance. These wafers were mounted on the test boards and the first tests completed on Sept. 1, 1967 on wafer 47-4;10-2.

The tests which were made on this wafer were under both undisturbed and fully disturbed conditions. Figure 3 shows the full disturbed pattern which was used. Two full patterns are shown. Sixteen pre-disturb read-write cycles storing the opposite polarity as the desired storage bit (the illustration shows pre-disturb storage in the "0" direction) were followed by the desired storage bit (shown as a "1") which was then followed by a post-disturb pattern of 16 digit pulses, without read or write, of the opposite polarity (shown as a "0"). The stored output was then examined during the first read pulse of the next pattern. For the undisturbed measurements, the pre-disturb and post-disturb digit pulses were removed.

The data taken in this manner on the first wafer is shown in Figure 4. In order to obtain measurable output signals, the read current was increased to 200 mA, and the write current was adjusted for maximum output signals, resulting in an 85-mA write current. The maximum fully disturbed output signal, measured as indicated in the previous paragraph, was about 2.5 mV at 25°C. This output was judged to be too low.

The second wafer (47-40;59-2) was then tested. For this wafer the optimum write current at a read current of 200 mA was found to be 100 mA. This wafer showed about the same undisturbed outputs as 47-4;10-2, but had substantially better fully

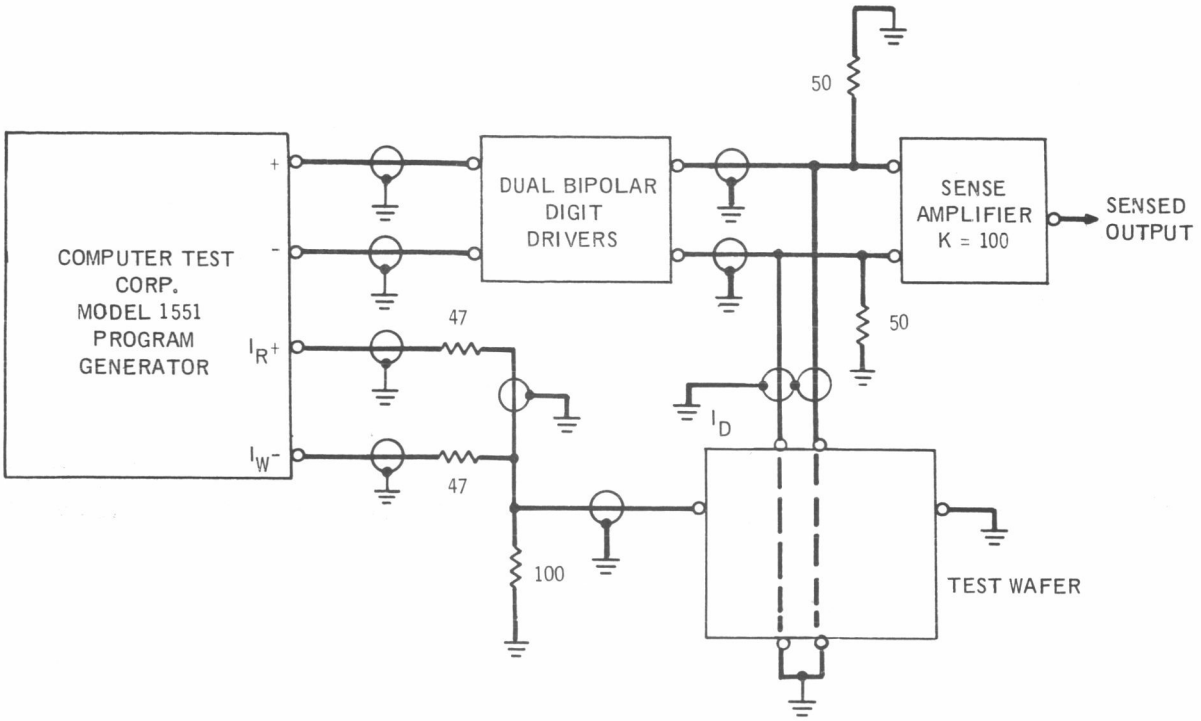



Figure 1. Wafer Test Setup

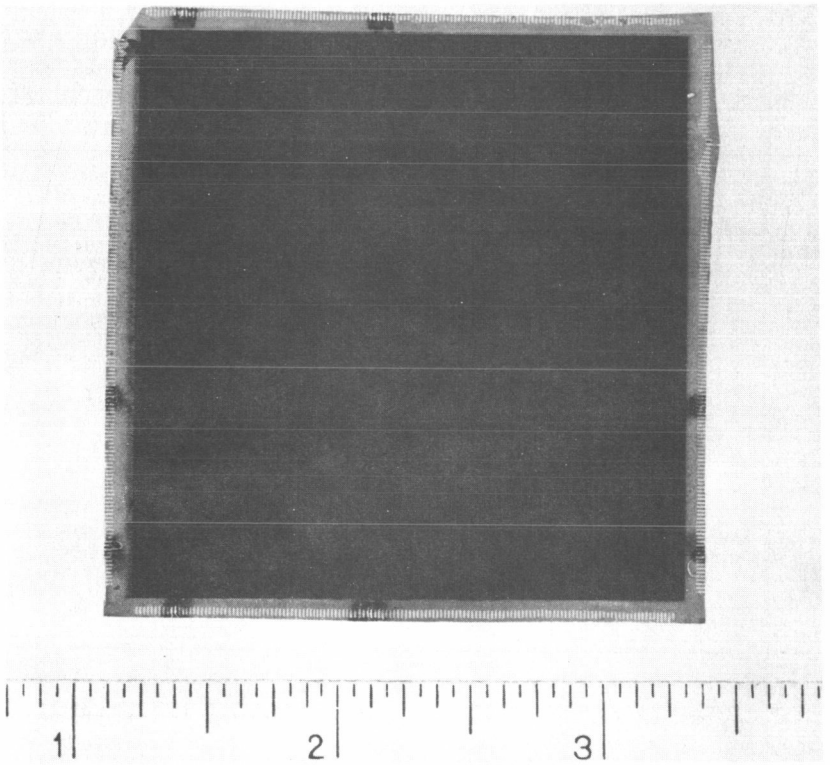



Figure 2. Type 47 Wafer, 140 x 140 Size

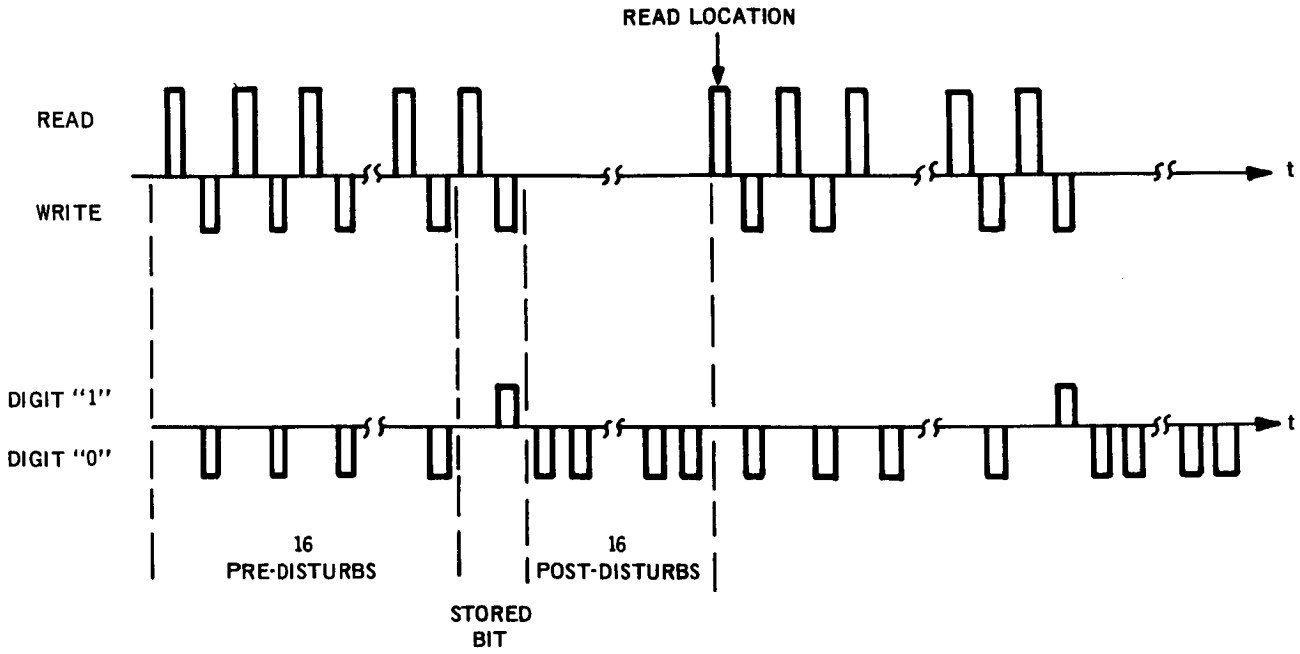



Figure 3. Full Disturb Pattern

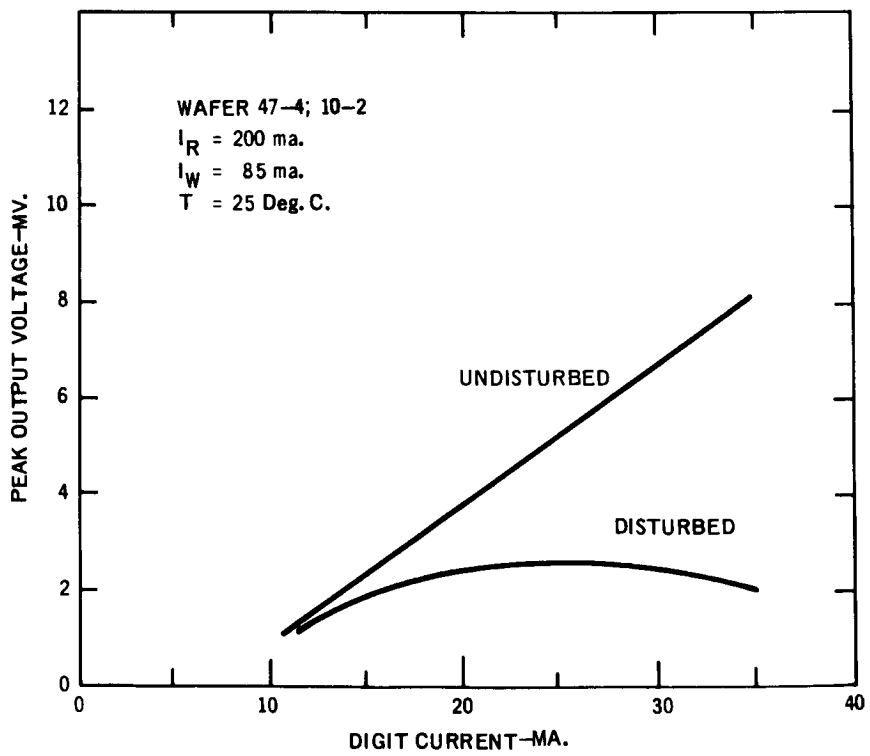



Figure 4. Test Data, Type 47 Wafer 47-4;10-2

disturbed outputs. However, this wafer was also judged inadequate, producing only 4.5 mV at 25°C at ±20 mA of digit current and at the increased read and write currents. The results of this test are shown in Figure 5.

The third wafer in this series which was tested was 47-21;63-2. The results of this test, shown in Figure 6, are poorer than for either of the previous two type 47 wafers.

A review was then held, on Sept. 19, 1967, with RCA Laboratories personnel. Since the results of the three wafer tests indicated that increases in firing temperature (47-21;63-2 at 2250°F), (47-40;59-2 at 2400°F), (47-4;10-2 at 2450°F) improved the performance, a request was made for more sample wafers fired at higher temperatures. Two wafers fired at 2400°F were received at this time and one of these (47-13;59-1) was tested and found to produce high outputs. The data for this wafer is shown in Figure 7.

Subsequent tests run on wafers fired at 2550° and 2600°F showed lower output signals than the type 47 wafer fired at 2400°F. Wafer 47-21;1-47 was then prepared, fired at 2500°F, and tested. This showed the best results of all of the wafers tested, and on October 16, 1967, RCA Laboratories was directed to start the preparation of the final Phase I encapsulated sample wafers using the process which had been used for wafer 47-21;1-47.

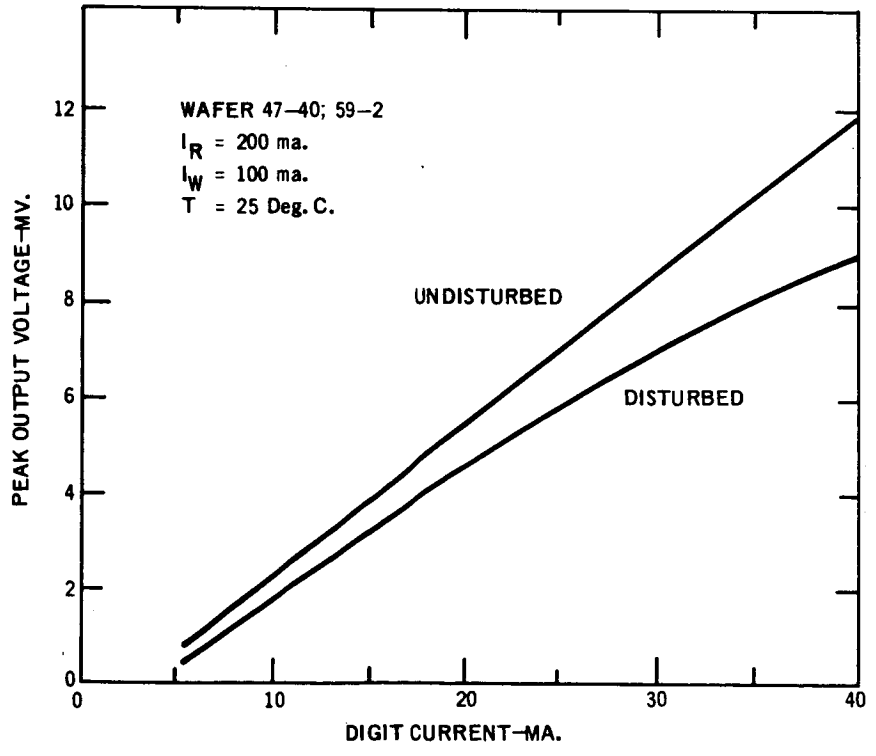



Figure 5. Test Data, Type 47 Wafer 47-40;59-2

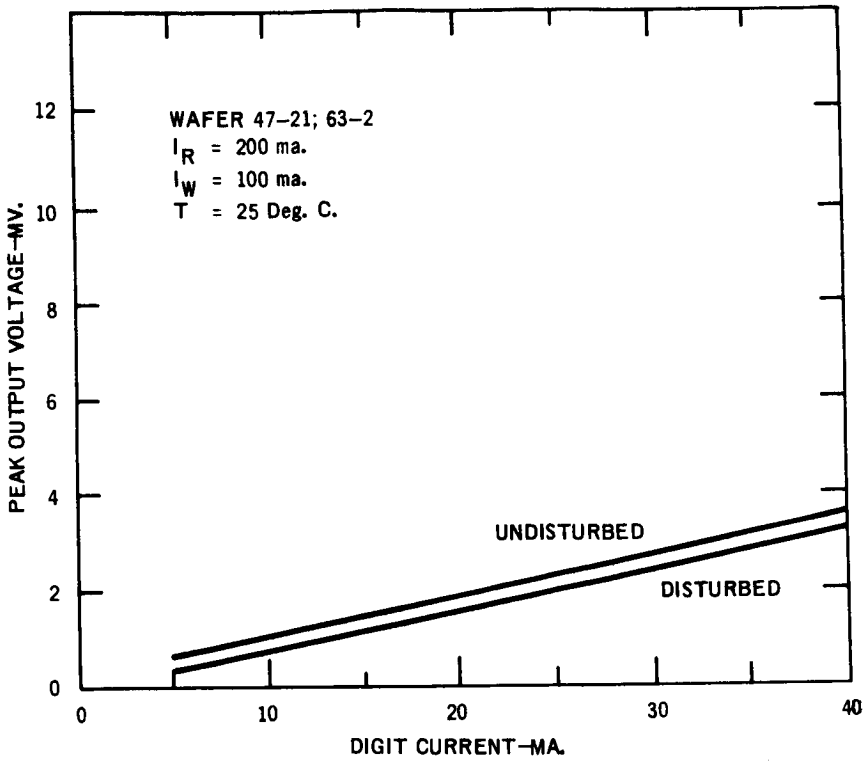



Figure 6. Test Data, Type 47 Wafer 47-21;73-2

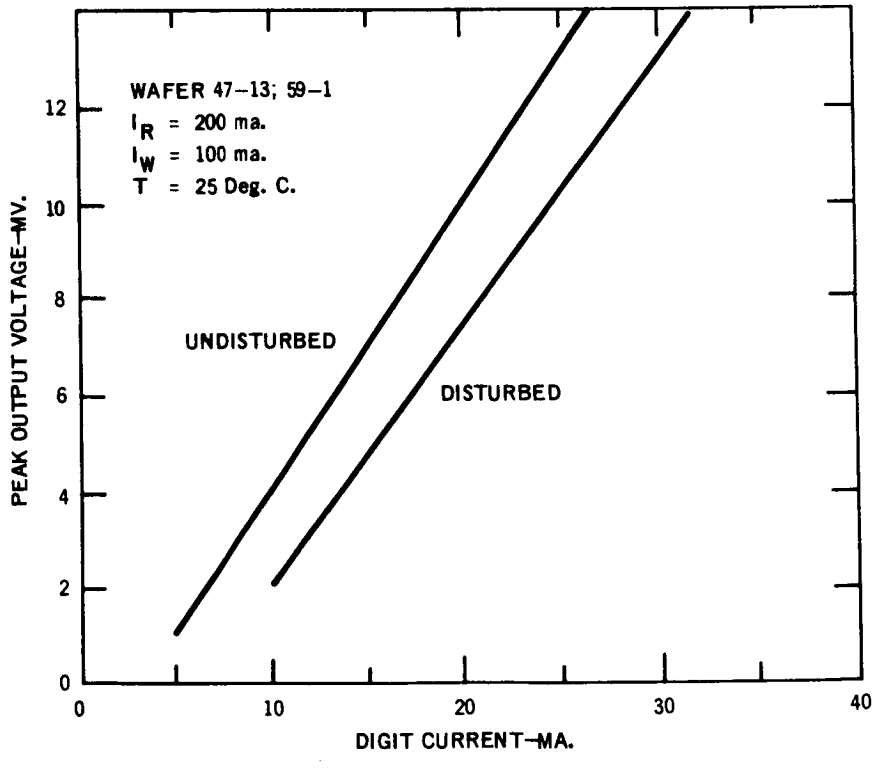



Figure 7. Test Data, Type 47 Wafer 47-13;59-1

During the last two weeks of November 1967, a series of tests was started using a breadboarded sense amplifier and wafer 47-21;1-47. These tests indicated that the wafer was not producing sufficient output signal to exceed the amplifier threshold, which was known to be approximately 1.0 mV. The wafer was again put through the same characterization tests which had been run previously, and it was found that the "1" storage output signal was not exceeding the amplifier threshold for fully disturbed operation.

This effect was due to previously undetected excessive disturb sensitivity of the type 47 samples prepared at RCA Laboratories. Figure 8a shows the type of output signals which would normally be expected from a monolithic ferrite wafer with a stored "1", a stored "0", and with no digit current during the write interval. As the drawing shows, because of the clearing action of a read/write cycle without digit current, the output after such a cycle was expected to consist of noise alone. The output "1" signal would then be the difference between the "no data" output and the output with a stored "1" as shown by the line marked "1". The output "0" signal would similarly be the line marked "0". Figure 8b shows the type of output signals that were actually obtained from the type 47 wafers. The "no data" output for a fully disturbed "1" pattern was in the "0" direction, and the "1" signal output was, at best, only slightly in the "1" direction. The results for stored "0" signals were similar, but inverted. The readings which were taken (shown in Figures 4 through 7) were the differences shown by the line marked "reading" in Figure 8b. The appreciable output obtained with no digit current during the storage interval was attributed to reducible system noise, whereas in fact it was due to remanence of the pre-disturb bit pattern which was not cleared by the read/write currents during the storage interval. With respect to potential use of the type 47 wafers in a memory, it was concluded that, with worst-case disturb patterns applied to a storage location, it would not be possible to distinguish between a stored "1" and a stored "0".

The existence of this severe disturb sensitivity in all wafers made at RCA Laboratories was then confirmed, by measurement on wafers of other compositions and by discussion with RCA Laboratories personnel. Further tests on the type 47 composition were then discontinued at AED.

At RCA Laboratories, as a step toward determining the cause of the severe disturb sensitivity of the wafers prepared for this program, a sample of type 47 composition (prepared during the prior contract and stored in "green" condition) was fired according to the schedule used in the earlier program. The resulting wafer was tested, and showed results similar to those reported from contract NASw-979. A further set of samples were then prepared from the same raw materials used to prepare the samples described earlier in this section, but the preparation of the wafers and the firing schedules followed those from the earlier contract. The results on these wafers also substantially duplicated the results of the earlier contract.

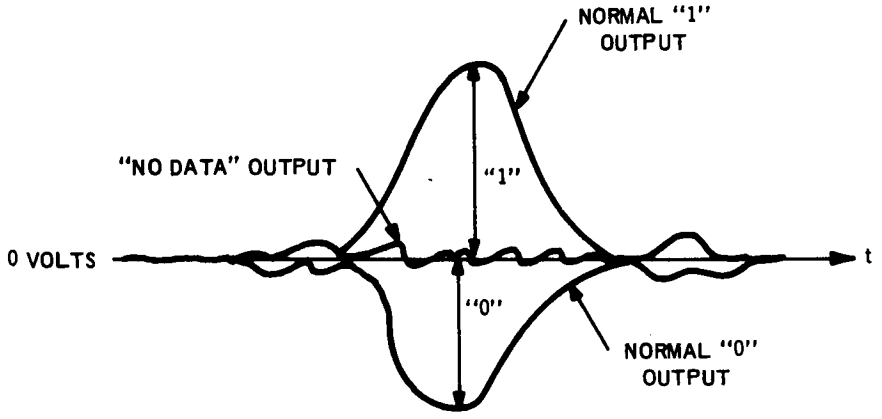



Figure 8a. Normal Monolithic Ferrite Outputs

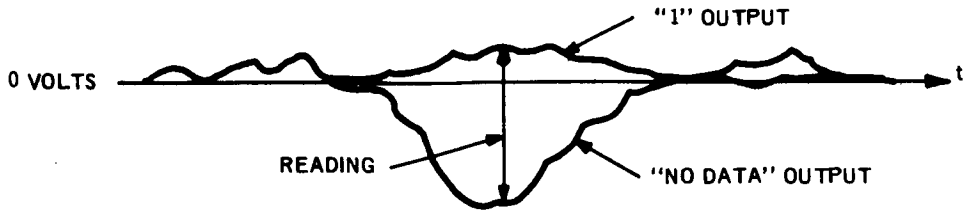



Figure 8b. Typical Type 47 Outputs

Differences in results were thus obtained, with type 47 composition, from the 140 x 140 crossover wafers fabricated for this program, and from the 256 x 100 wafers fabricated for the prior program and duplicated during this study task. While no complete understanding of this problem exists at this time, two factors, which are known to be important in determining the magnetic properties of laminated ferrite wafers, are suspected to have contributed to the poorer performance of the 140 x 140 crossover wafers.

The 256 x 100 crossover wafers were made by embossing the green ferrite layers with the conductor pattern and filling the grooves with conductor paste. The 140 x 140 wafers could not be made this way because embossing tools were not available for 140 conductors. A screen process was used instead, with a screening mask which was not geometrically perfect. It is believed that embossing produces conductor patterns which are geometrically and electrically better than conductors made by screening.

In an effort to develop a fabrication process which would lend itself better to volume production, the 140 x 140 crossover wafers were sintered for two hours at temperatures around 2500°F, in an air atmosphere. The 256 x 100 crossover wafers were sintered for 24 hours at about 2200°F, in inert atmospheres. It is now believed that these two firing processes, initially thought to be equivalent, produce very different magnetic properties in the ferrite.

The disturb sensitivity found in the 140 x 140 crossover wafers is now thought to be due to the sintering schedule used. The effect of the screening process in place of the embossing process is thought to have had its major effect on the uniformity and amplitude of the output sense signals.

Although the samples of type 47 composition tested during this program did not meet the requirements for this memory system, some of the samples tested did show desirable properties. Foremost among these was a relatively wide temperature range. Results of the prior contract, partially duplicated during this program, also showed that type 47 can be operated using domain wall switching, at much lower current and with longer rise times than were used during this program. These properties, if available in production wafers, would substantially improve the operating properties of the memory system with respect to temperature range and operating power. Further research is necessary to determine the optimum processes to be used in fabricating wafers from the type 47 to obtain satisfactory production yields.

### 3. Type 3515 Material Investigations

Among the samples of compositions other than type 47 that were prepared and tested was a sample of type 3515 (12.5% ZnO, 22% MnO, 25.5% MgO, 40% $Fe_2O_3$) fabricated in the 140 conductor size at RCA Laboratories. This sample was tested

during the type 47 test program, and was found to produce about the same output signals, at the same drive currents, as type 47 wafer 47-4;10-2, shown in Figure 4. Since there was not an evident gain in output signals, and since the type 3515 composition was known to have a less desirable temperature characteristic than the type 47 composition, further investigation of these samples was dropped in favor of the type 47 wafers.

When the difficulties described in section II-A-2 were encountered in November 1967, a test was initiated using a type 3515 wafer previously fabricated by RCA Memory Products Division in the 64 crossover size, to determine whether or not the disturb sensitivity noted in the type 47 wafers was caused in some way by the test conditions or whether it was an inherent property of the material. The wafer tested was no. MF2102.

These tests showed very little disturb sensitivity for the type 3515 wafer, and, in addition, showed that this wafer was capable of producing larger signals than the best type 47 wafer, at the same drive currents. Figure 9 shows the fully disturbed output signals for this wafer as a function of digit current, for a read current of 200 mA and a write current of 100 mA. In all cases there was good signal-to-noise ratio for both "1" and "0" storage, so that accurate detection of a stored "1" by a threshold amplifier is possible.

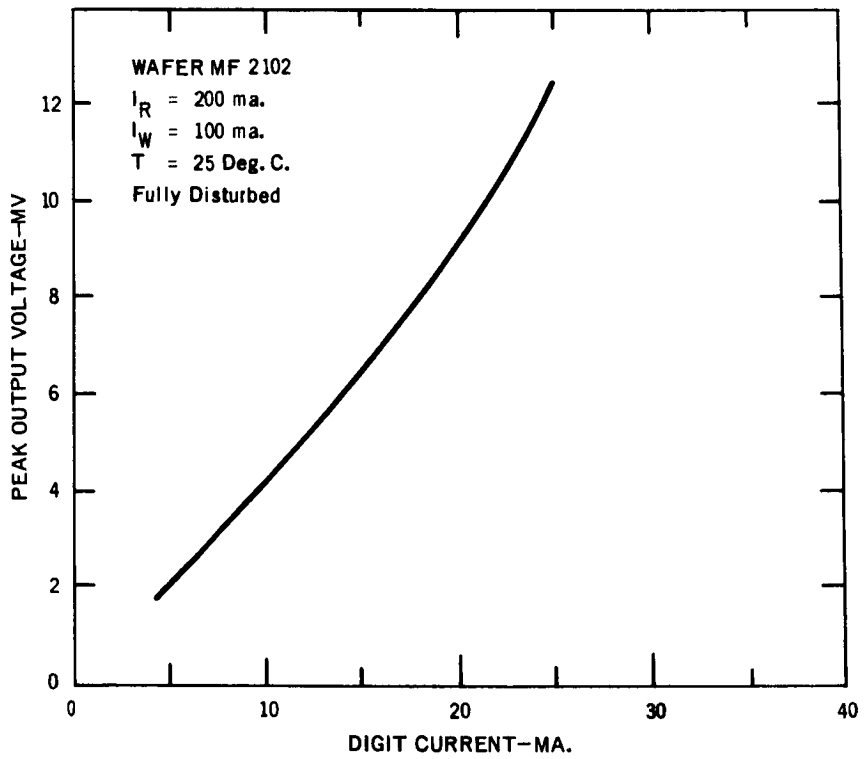



Figure 9. Type 3515 Characteristic

Having determined that the basic performance of the type 3515 wafer was adequate for this program, a temperature test was performd. The results of this test, shown in Figure 10, indicates that while there is a large variation in output signal over the temperature range, the use of a moderate amount of temperature compensation for the read and write currents will improve the low-temperature output signal sufficiently. Two points are shown at -20°C on Figure 10: one at 240 mA of read current and 150 mA of write current, producing 5 mV of fully disturbed output signal; and the second at 250 mA of read current and 140 mA of write current, producing 6.5 mV of fully disturbed output signal.

A complete set of characteristic data was taken both at +25°C and at -20°C to assist in selecting the best operating points for subsequent tests of type 3515 wafers. For room temperature operation, the ranges were 150 to 250 mA for read current, 80 to 140 mA for write current, and 10 to 40 mA for digit current. Based on the results of these measurements, the ranges at -20°C were 250 to 350 mA for read current, 80 to 200 mA for write current, and 10 to 25 mA for digit current. The results of these measurements of typical type 3515 characteristics are shown in Figures 11 and 12. Figure 11, at a digit current of ±20 mA, shows that an output of around 10 mV can be obtained at +25°C with a read current of 200 mA and a write current of 100 mA. At -20°C, it is necessary to increase the read current to 290 mA and the write current to 140 mA to maintain the 10-mV output signal. Figure 12 shows that at a digit current of ± 15 mA, the output at room temperature can be maintained at 10 mV only by increasing the read current to 245 mA, and that at -20°C a 10-mV output cannot be maintained (the maximum

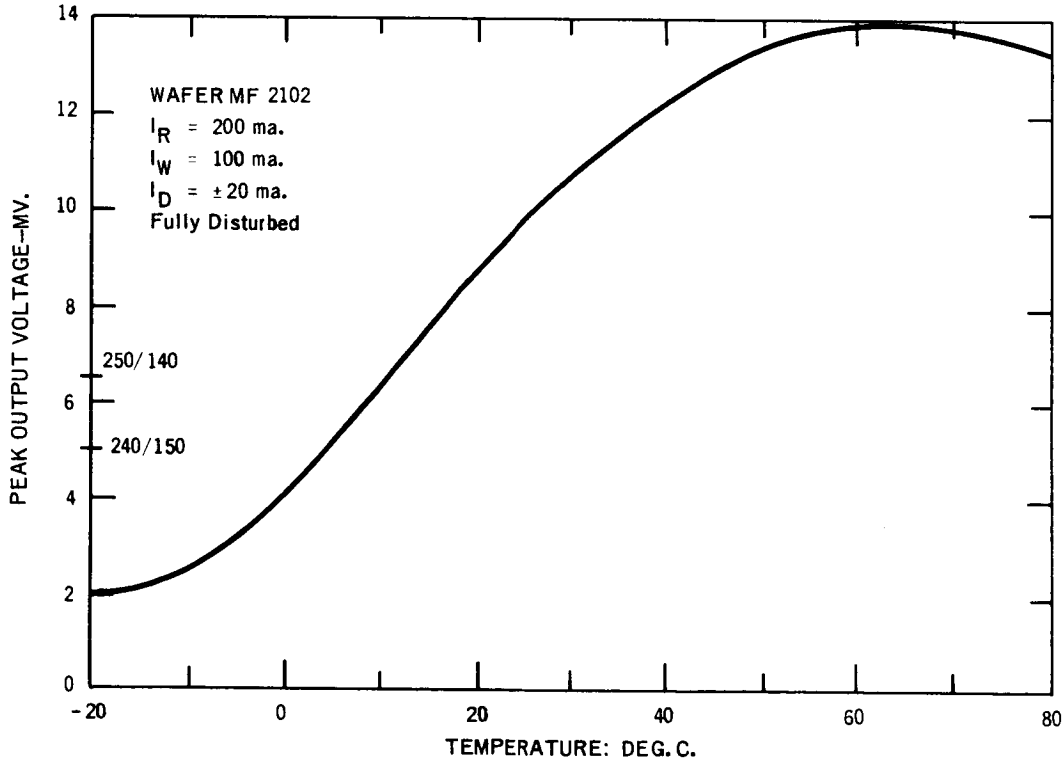



Figure 10. Type 3515 Temperature Characteristic

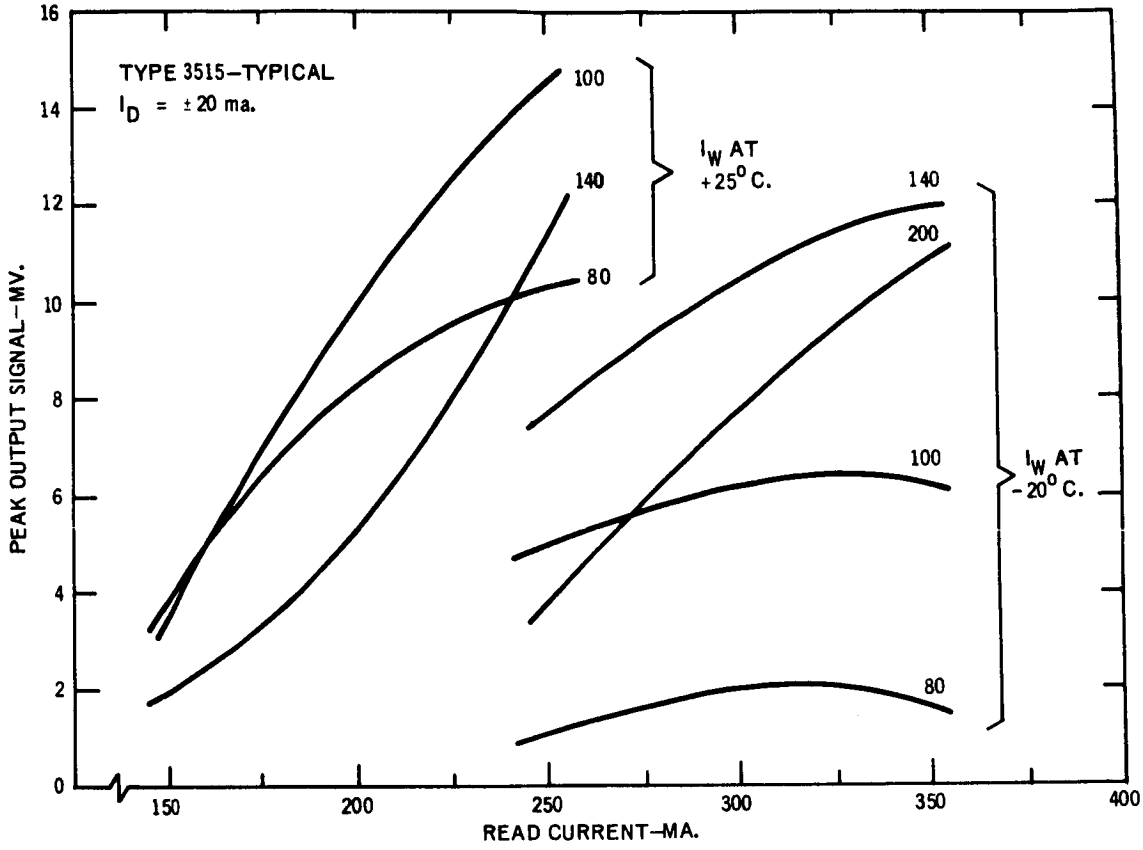



Figure 11. Type 3515 Typical Operating Characteristics

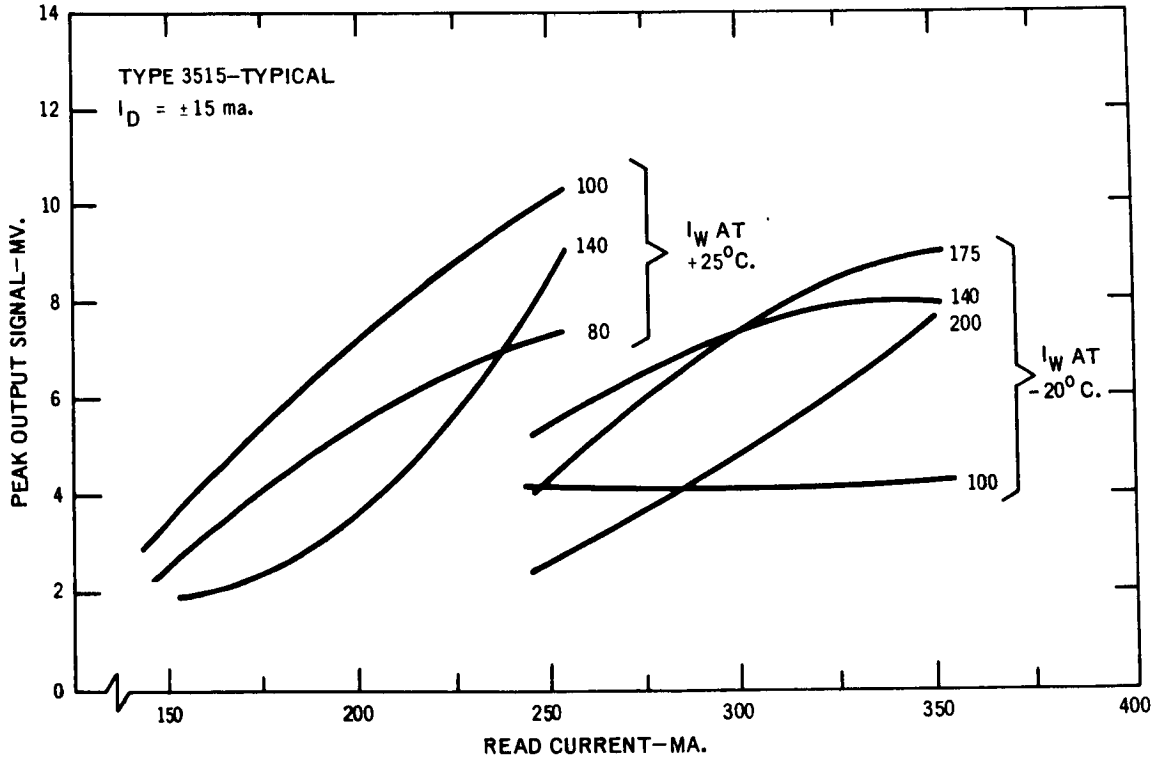
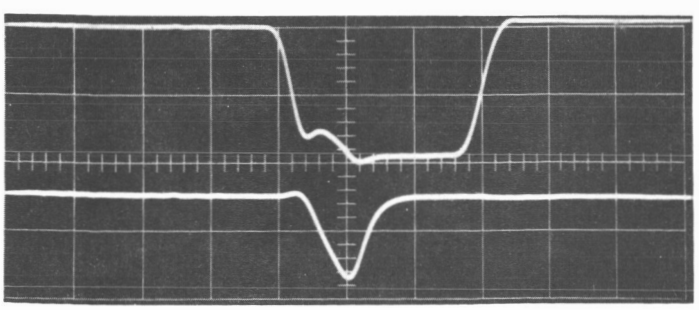



Figure 12. Type 3515 Typical Operating Characteristics

output at this temperature being about 9 mV). Based on these measurements, test conditions of 200 mA of read current, 100 mA of write current, 20 mA of digit current at +25°C were selected.

To ensure that these results were not unique to the individual wafers tested, a number of additional samples were obtained from the stock of 87 wafers made by RCA Memory Products Division and available within RCA. A total of ten different wafers were tested. All but one of these was partially tested, and one was fully tested. Results were consistently good. Of 194 locations tested on seven wafers, there were 191 locations with output signals above 5 millivolts, and the three below 5 millivolts were usable. The one wafer which was fully tested showed all outputs above 13 millivolts (Figure 13 shows the output signal from a typical location on this wafer).

These tests indicated that type 3515 wafers, made under production conditions at the RCA Memory Products Division, could operate successfully in the memory system.



TOP: READ CURRENT 100 mA/cm

BOTTOM: SENSE OUTPUT 10 mV/cm

$I_W$: 100 mA

$I_D$: 20 mA

HORIZONTAL: 100 ns/cm

Figure 13. Typical Type 3515 Wafer Output Signal

4. Optimum Size Analysis

a. Selection Criteria

Selection of the best size for the memory wafers for a flight memory must be made by trading off three basic factors which are directly influenced by the wafer size and shape. These factors are reliability, volume and weight (assuming a direct proportion), and cost; and the factors should be evaluated for the ultimate flight-type memory system. The procedure for this analysis will be to postulate a set of possible sizes and shapes and evaluate the above factors for the 4096 x 32 memory in the two-crossover mode.

b. Postulated Possible Sizes and Shapes

Three sizes of monolithic ferrite wafers have been fabricated to date. These are 64 x 64 conductors having 15-mil spacing, 140 x 140 crossovers having 15-mil spacings, and 256 x 100 crossovers having 10-mil spacing. These can be fabricated with equal ease in any of the postulated materials. Since square wafers up to 140 crossovers, and oblong wafers up to about 2.5 inches on the longest side, have been made, it is permissible for this analysis to assume any size and shape which does not exceed 140 crossovers in a square configuration or 2.5 inches in an oblong configuration.

Since a 256-conductor wafer using 15-mil spacing would exceed the maximum demonstrated length limit of 2.5 inches, this configuration with any width will not be considered. Since the memory is operated at 32 bits per word, using two crossovers per bit, at least 64 conductors along the word lines are required. Because of end effects which make it advisable not to use the two endmost conductors in either direction, the number of conductors for the larger wafers has been increased so that end conductors need not be used.

Based on these considerations, the following sizes have been selected for analysis:

64 x 64, 15-mil spacing

140 x 70, 15-mil spacing

140 x 140, 15-mil spacing

256 x 100, 10-mil spacing

c. Reliability Characteristics

Of major importance in the reliability evaluation are the interconnections, the monolithic integrated circuits, and the hybrid integrated circuits. It has been assumed that for the ultimate flight configuration all interconnections to the memory

wafers will be made by deposition or by reflow soldering, and all interconnections to the integrated circuits will be made by reflow soldering. The following failure rates, obtained from AED Reliability Engineering, are typical for this application.

a) All interconnections: $10^{-11}$ failures per hour

b) Monolithic integrated circuits: $10^{-8}$ failures per hour (average)

c) Hybrid integrated circuits: $3 \times 10^{-8}$ failures per hour (average).

The net failure rate will be determined for each wafer size using the optimum circuit configuration.

d. Volume and Weight

The expected volume and weight for each postulated configuration will be calculated for the ultimate flight configuration of the memory, using the ceramic carrier approach to memory packaging outlined in the original proposal and using AED standard multilayer printed wiring for the electronic components, which will be assumed to be entirely contained in flat-packs. The weight will be calculated based on the physical hardware contained within the memory package.

e. Cost

The cost of an ultimate flight package will be estimated for each of the postulated configurations. The yields, manufacturing and assembly times, parts costs, and other data will be taken from historical records wherever possible or the data will be estimated by qualified personnel.

f. Reliability Considerations

A reliability analysis has been performed on the recommended memory system. In order to incorporate reliability considerations into the size analysis, the failure rate for the recommended configuration has been taken as a starting point and modified for other configurations in order to determine the relative reliability of the four postulated configurations.

The recommended 64 x 64 crossover configuration has been assigned a net failure rate of 5.76% per 1,000 hours, resulting in an MTBF of 17,300 hours. The 140 x 70 configuration has about 8,000 fewer memory stack connections, because of the larger size wafer, and, with a failure rate per connection of $10^{-11}$, will show a slight increase in MTBF, compared to the 64 x 64 size, of 17,330 hours. The 256 x 70 configuration

has 12,000 fewer connections than the 64 x 64 size, and the MTBF is then 17,340 hours. The 140 x 140 configuration, with fewer connections but much more electronics than the other sizes, shows an MTBF of about 16,700 hours.

g. Volume and Weight Analysis

The volume for each configuration will be calculated on the basis of the following assumptions:

a) The ferrite wafers will be packaged in ceramic carriers, each 0.1 in. thick, 0.5 in. longer than the wafer in one dimension and 1.0 in. longer than the wafer in the other dimension. The density of the ceramic has been taken as 0.1 pounds per cubic inch.

b) The electronic circuits will be packaged in flat packs, and the flat packs will be assembled on conventional printed wiring boards. Experience with this type of mounting demonstrates a total weight for a package to be about 0.01 pound per module, and a packing density of about 0.5 cubic inch per module.

A. 64 x 64 crossovers.

Wafer size - 1.0 x 1.0 inch

Ceramic carrier size - 0.1 x 1.5 x 2.0 = 0.3 cubic inch

Total size of 64-wafer stack - 64 x 0.3 = 19.2 cubic inches

Electronics: 160 cubic inches

Total volume - 160 + 19 = 179 cubic inches

Weight of stack - 19.2 x 0.1 = 1.9 pounds

Weight of electronics - 3.2 pounds

Weight of memory - 3.2 + 1.9 = 5.1 pounds

B. 140 x 70 crossovers

Wafer size = 1.0 x 2.0 inches

Ceramic carrier size = 0.1 x 2.6 x 2.0 = 0.52 cubic inch

Total size of 32-wafer stack = 32 x 0.52 = 16.6 cubic inches

Electronics volume same as 64 x 64 = 160 cubic inches

Total volume = 160 + 17 = 177 cubic inches

Weight of stack = 16.6 x 0.1 = 1.7 pounds

Weight of electronics = 3.2 pounds

Weight of memory = 3.2 + 1.7 = 4.9 pounds

C. 140 x 140 crossovers

Wafer size = 2.0 x 2.0 inches

Ceramic carrier size = 0.1 x 2.6 x 3.0 = 0.8 cubic inch

Total size of 16 wafer stack = 16 x 0.8 = 12.8 cubic inches

Electronics: 224 cubic inches

Total volume = 224 + 13 = 237 cubic inches

Weight of stack = 12.8 x 0.1 = 1.3 pounds

Weight of electronics = 4.48 pounds

Weight of memory = 4.48 + 1.3 = 5.78 pounds

D. 256 x 70 crossovers

Wafer size = 2.56 x 0.70 inches

Ceramic carrier size = 0.1 x 3.2 x 1.3 = 0.416 cubic inch

Total size of 8 wafer stack = 8 x 0.416 = 3.3 cubic inches

Electronics volume same as 64 x 64 = 160 cubic inches

Total volume = 160 + 3.3 = 163 cubic inches

Weight of stack = 3.3 x 0.1 = 0.33 pound

Weight of electronics same as 64 x 64 = 3.2 pounds

Weight of memory = 3.2 + 0.3 = 3.5 pounds

h. Cost Analysis

The cost analysis is based on the following assumptions:

a) The cost of wafer fabrication is negligible compared to the assembly, wiring and test costs for the wafers.

b) The cost of assembly is equal to $50 per wafer and is independent of the wafer size.

c) The cost of wafer wiring is $0.25 per wire.

d) The selection diodes cost $0.50 each.

e) The cost of testing wafers containing 131072 bits is independent of the wafer size and is equal to $5000.

f) The cost of stack assembly using ceramic carriers is equal to $10 per wafer.

g) The cost of hybrid modules is $100 each and the cost of monolithic integrated circuits is $25 each.

h) The cost of module board fabrication and assembly is $2000 for a 50-module board.

A. 64 x 64 crossovers

1) 64 wafers are required. The wafer assembly cost is 64 x $50 = $3200.

2) Each wafer has 256 wires for a total of 16,384 wires. Wiring cost will be 16,384 x $0.25 = $4100 approximately.

3) 8200 diodes will cost $4100.

4) Wafer testing costs $5000.

5) Stack assembly costs will be 64 x $10 = $640.

6) 192 hybrid modules will cost 192 x $100 = $19,200.

7) 128 monolithic circuits will cost $3200.

8) 7 module boards will be required and will cost 7 x $2000 = $14,000.

The total cost using 64 x 64 crossover wafers will be $56,640.

B. 140 x 70 crossovers

1) Wafer assembly: 32 x $50 = $1600.

2) Wafer wiring: 12,400 x $0.25 = $3100.

3) 8200 diodes: $4100.

4) Wafer testing: $5000.

5) Stack assembly: 32 x $10 = $320.

6) 192 Hybrid modules: $19,200.

7) 128 Monolithic circuits: $3200.

8) 7 boards: $14,000.

The total cost using 140 x 70 crossover wafers is $50,520.

C. 140 x 140 crossovers

1) Wafer assembly: 16 x $50 = $800.

2) Wafer wiring: 9850 x $0.25 = $2460.

3) 4100 diodes: 4100 x $0.50 = $2050.

4) Wafer testing: $5000.

5) Stack assembly: 16 x $10 = $160.

6) 288 Hybrid modules: 288 x $100 = $28,800.

7) 160 Monolithic circuits: 160 x $25 = $4000.

8) 9 Boards: 9 x $2000 = $18,000.

The total cost using 140 x 140 wafers is $61,270.

D. 260 x 70 crossover at 10-mil spacing. (It is assumed that because of the 10-mil spacing the wiring costs will increase by a factor of 2.)

1) Wafer assembly: 8 x $50 = $400.

2) Wafer wiring: 5100 x $0.25 x 2 = $2550.

3) 8200 diodes: $4100.

4) Wafer testing: $5000.

5) Stack assembly: 8 x $10 x 2 = $160.

6) 192 Hybrid modules: $19,200.

7) 128 Monolithic circuits: $3200.

8) 7 boards: $14,000.

The total cost using 260 x 70 crossover wafers is $48,210.

i. Tradeoff Chart

The memory size tradeoff chart (Table 1) lists the results of the preceding paragraphs for each contributing factor and for each of the postulated sizes. Under each factor is listed the actual value and the value normalized to the smallest entry. The right-hand column shows the unweighted total of all of the contributing factors for each postulated size.

It is evident from the chart that the 260 x 70 crossover size is optimum, since it is minimum for all factors. The nearest competitor is the 140 x 70 size.

TABLE 1

MEMORY SIZE TRADEOFF CHART

| Size | Reliability | | Memory Wt. (8.3) | | Cost (8.4) | | Unweighted Rating |
|---|---|---|---|---|---|---|---|
| | Actual | Norm | Actual | Norm | Actual | Norm | |
| 64 x 64 | 17.3 | 1.003 | 5.1 lb | 1.46 | $56.6K | 1.17 | 3.63 |
| 140 x 70 | 17.33 | 1.001 | 4.9 | 1.40 | 50.5 | 1.05 | 3.45 |
| 140 x 140 | 16.7 | 1.09 | 5.8 | 1.65 | 61.3 | 1.27 | 4.01 |
| 260 x 70 | 17.34 | 1.00 | 3.5 | 1.0 | 48.2 | 1.0 | 3.00 |

Since the reliability and weight ratios are strongly controlled by the characteristics of the various wafer sizes, and since the 260 x 70 size is best in all categories, it is not necessary to ask if changes in the assumptions will affect the results, with the possible exception of the cost factor. This was calculated on the basis of an assumed complexity constant of 2 for the 260 x 70 size, based on the requirement for 10-mil spacing. If it is possible to build this size using 15-mil spacing, this will result in an even greater difference in favor of the larger size. It is reasonable to ask, if the complexity constants were greater than 2 for the 10-mil spacing, would it be possible that the 140 x 70 size might turn out best.

In order to assess this, it should be observed that the relative cost of the 260 x 70 size would have to become larger than the cost of the 140 x 70 size to make up for the differences in the weight columns. The cost of the memory using the larger size wafers would have to go to about $80K to make the 140 x 70 memory competitive. In order for this to result, the complexity factor would have to increase to 17.8. Even with the increased difficulties of wiring and assembly for the 10-mil spacing, it is not reasonable to expect that the wiring costs would be 17 times higher than for the smaller wafer. If, on the other hand, cost were the only important factor, the cost of the memory using the larger wafer would only have to increase to $50.5K, requiring a complexity factor of 3.4, for the smaller wafers to become competitive.

### j. Conclusions

Based on the calculations given above, and the tradeoff chart, the 260 x 70 crossover wafer, with either 10-mil or 15-mil spacing, is best for a laminated ferrite memory in flight configuration.

If it turns out that the 10-mil spacing causes a wiring complexity factor, compared to 15-mil spacing, and only 10-mil spacing can be used for the larger capacity wafer, it will be necessary to investigate very closely the effect of increased cost on the size selection. If the complexity factor approaches 4, and cost is a major factor, it is likely that the 140 x 70 crossover wafer, which can be easily made with 15-mil spacing, will be better than the larger capacity wafer.

The present recommendation is to attempt 260 x 70 wafers using 15-mil spacing. If difficulty is encountered in this, an investigation should be made of the wiring difficulty using 10-mil spacing. If the difficulty is not too great by a factor of no more than 3 compared to 15-mil spacing, the 260 x 70 wafer with 10-mil spacing should be used. If not, the 140 x 70 wafer using 15-mil spacing should be used.

5. Digit/Sense Line Investigation

At the start of the program, it was necessary to make engineering judgements about the probable memory stack organization, in order to provide a uniform basis for the various study tasks. A review of the expected characteristics of the peripheral circuitry (such as sense amplifiers, word and digit drivers, and logic and timing circuits) indicated that the stack could be operated as a 4096-word, 32-bit-per-word arrangement. This configuration was preferred because it leads to the greatest simplicity and minimizes the peripheral circuitry.

In order to determine the parameters of such a system organization, particularly with respect to sense signal attenuation and delay, a series of tests were run on a simulated 4096-word digit/sense line. This line was obtained by wiring in series a set of 16 lines each threading 4 wafers of 64 crossovers each. Delays and attenuation were measured for a variety of line lengths and terminations. The results of these tests, described in detail below, indicate that because of both delay and signal attenuation, the use of 4096-word digit/sense lines is not feasible and a practical upper limit is 2048 words.

An analysis was then made of means for using 2048-word digit/sense lines in a 4096-word, 32-bit system. The only approach which does not incur a penalty in sense signal is one which uses digit/sense line switches to switch each digit driver/sense amplifier set to the proper half of a split 4096-word line. An experimental investigation (Section II-A-6) has been made into the characteristics of a two-transistor switch which has been used previously for similar purposes and the results of this investigation show that such a switch is a feasible solution to the digit/sense line problem.

a. Attenuation and Delay Tests

To measure the effects of digit/sense line length and termination on the digit drive current and sense signal, a series of tests were conducted. Table 2 shows the results of these tests.

Signals were first measured on a 2048-word test line fabricated by wiring four wafers as illustrated in Figure 14. Signals were then measured on a 4096-word line fabricated by extending the wiring scheme of Figure 14.

The word lines of these 64 x 64 RCA Memory Products Division wafers were grounded and the digit lines between the wired digit lines were left unterminated.

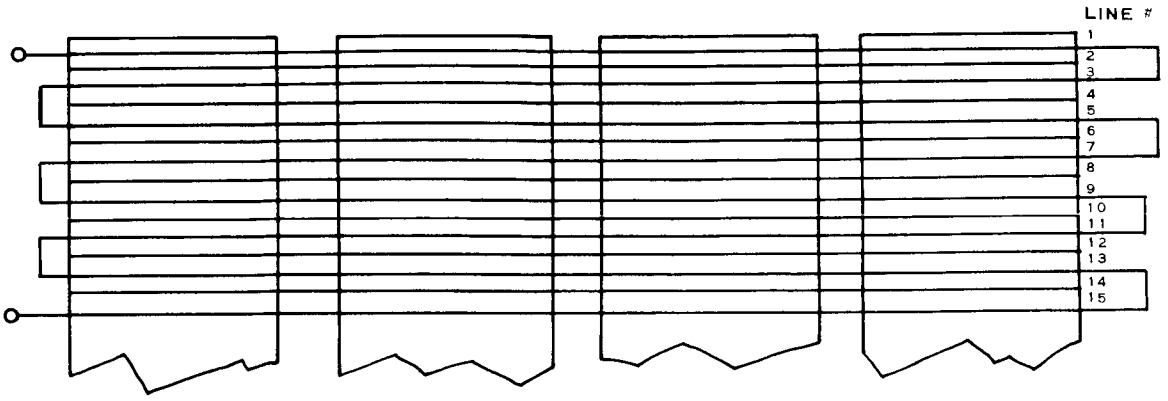



Figure 14. 2048-Word Test Line Wiring Scheme

The test photos shown were all taken with the material at ambient temperature. No temperature tests were conducted in this test series.

The test setup is shown in Figure 15.

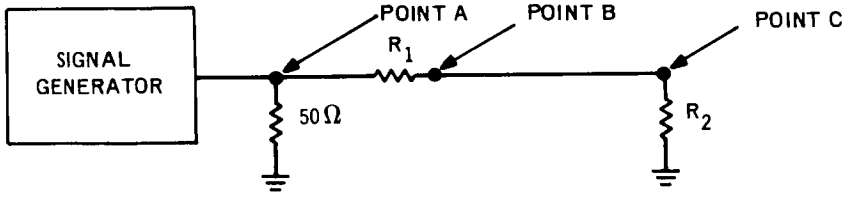



Figure 15. Digit Line Test Setup

Input pulses were modified for the different tests by having their pulse widths and rise times varied.

TABLE 2

PULSE TEST DATA ON LAMINATED FERRITE DIGIT LINES

| Test No. | Length (words) | Input Pulse Width (ns) | Input Rise Time (ns) | $R_1$ | $R_2$ | Reflection | | Termination Voltage | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Amp | Delay (ns) | Amp | Delay (ns) |
| 1 | 2048 | 40 | 15 | 220 | 0 | -0.17 | 150 | - | - |
| 2 | | | | 220 | 220 | +0.07 | 100 | 0.4 | 75 |
| 3 | | | | 220 | ∞ | +0.2 | 160 | 0.67 | 75 |
| 4 | | 80 | 35 | 220 | 220 | +0.1 | 100 | 0.5 | 75 |
| 5 | | 80 | 35 | 220 | 0 | -0.3 | 150 | - | - |
| 6 | | 120 | 50 | 220 | 220 | +0.16 | 120 | 0.67 | 75 |
| 7 | | 120 | 50 | 220 | 0 | -0.35 | 150 | - | - |
| 8 | | 120 | 50 | 220 | ∞ | +0.5 | 180 | 1.2 | 75 |
| 9 | | 50 | 20 | 220 | 220 | +0.04 | 100 | 0.5 | 75 |
| 10 | | 50 | 20 | 220 | ∞ | +0.4 | 180 | 0.95 | 80 |
| | 4096 | 50 | 20 | 220 | 200 | +0.02 | 120 | 0.25 | 160 |
| | 4096 | 50 | 20 | 200 | 0 | -0.05 | 300 | - | - |
| | 4096 | 80 | 35 | 200 | 200 | +0.04 | 110 | 0.35 | 160 |
| | 4096 | 80 | 35 | 200 | 0 | -0.10 | 320 | - | - |
| | 4096 | 80 | 35 | 200 | ∞ | +0.10 | 320 | 0.67 | 160 |

The photographs in Figures 16 through 19 show the pulse response of the 2048-word and 4096-word lines, with terminations at both ends. Figure 16 was taken on a 2048-word line with an 80-nanosecond pulse, and shows the output at 512-word taps. Figure 17 shows the same conditions for a 50-nanosecond input. Figure 18 shows the voltages at 1024-word taps along a 4096-word line with an 80-nanosecond input, and Figure 19 shows the same conditions for a 50-nanosecond input.

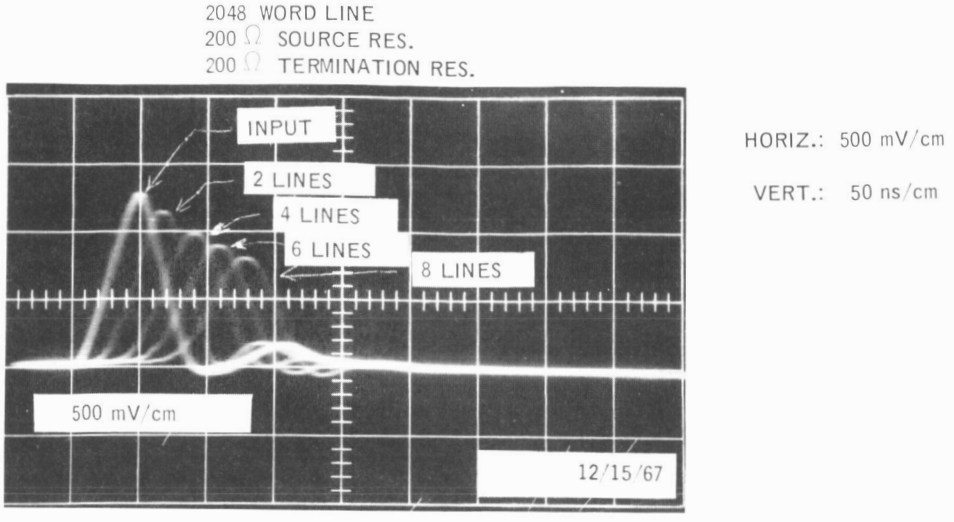



Figure 16. Digit Line Waveforms, 2048 Words, 80-Nanosecond Input

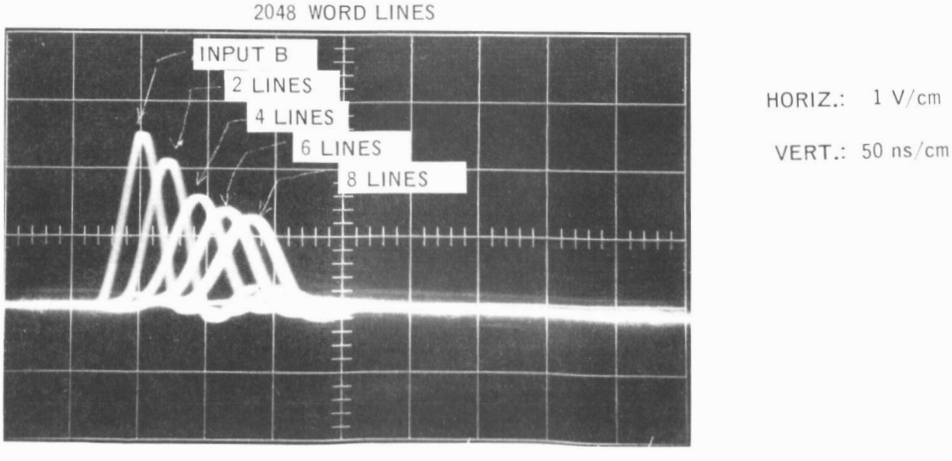



Figure 17. Digit Line Waveforms, 2048 Words, 50-Nanosecond Input

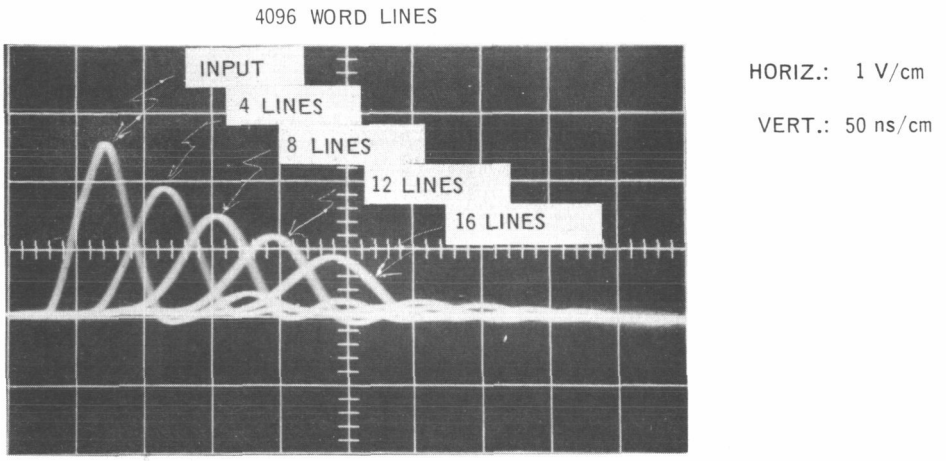



Figure 18. Digit Line Waveforms, 4096 Words, 80-Nanosecond Input

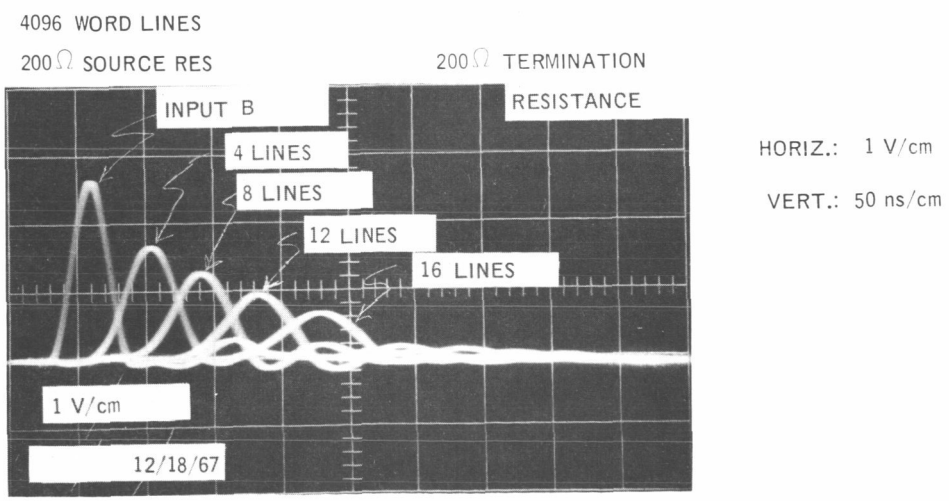



Figure 19. Digit Line Waveforms, 4096 Words, 50-Nanosecond Input

b. Other Data and Conclusions

1. The DC resistance of the 4096-word line is 200 ohms.
2. The characteristic impedance of the line measured between 200 and 220 ohms.
3. The conductance losses of the 4096-word line (see Figure 20) appeared to be approximately 4% of the Input Signal and are independent to a first order of the voltage across the line.
4. The line attenuation is a function of pulse width (see Figure 21) and was measured as 6.7 db for a 50-nanosecond pulse on a 2048-word line.
5. The delay down a 4096-word line was measured to be 165 nsecs.

c. Analysis of Potential Digit-Line Connections

Since the results of the digit/sense line investigation show that a 4096-word digit/sense line is not feasible, a study was made of possible interconnections of 2048-word digit/sense lines which would be compatible with a 4096-word, 32-bit system.

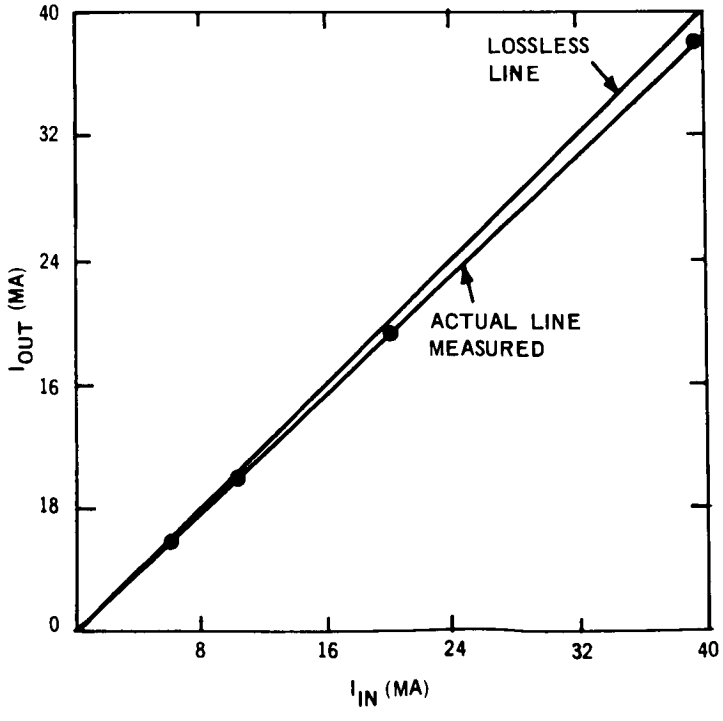



Figure 20. Conductance Losses for 4096 Words

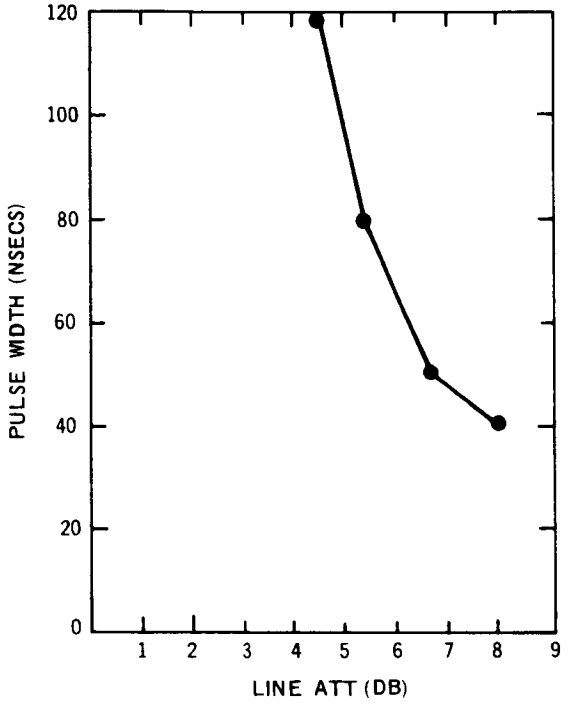



Figure 21. Line Attenuation for 2048 Words

A. Center-tapped 4096-word lines (Figure 22)

Advantages:

1. With each half of the line unterminated, the maximum signal attenuation will be about 6 dB.
2. With each half of the line terminated, the digit current split between the two halves will be approximately one-half.
3. With the lines grounded at the ends distant from the drivers, the differential line voltage presented to the sense amplifier will be within the 6-volt breakdown rating of the amplifier.
4. Sense signal delays are within acceptable limits.

Disadvantages:

1. With the lines terminated, the differential line voltage presented to the sense amplifier will exceed the 6-volt breakdown rating of the amplifier.
2. With the lines terminated, the signal attenuation will be about 12 dB, which is too large.

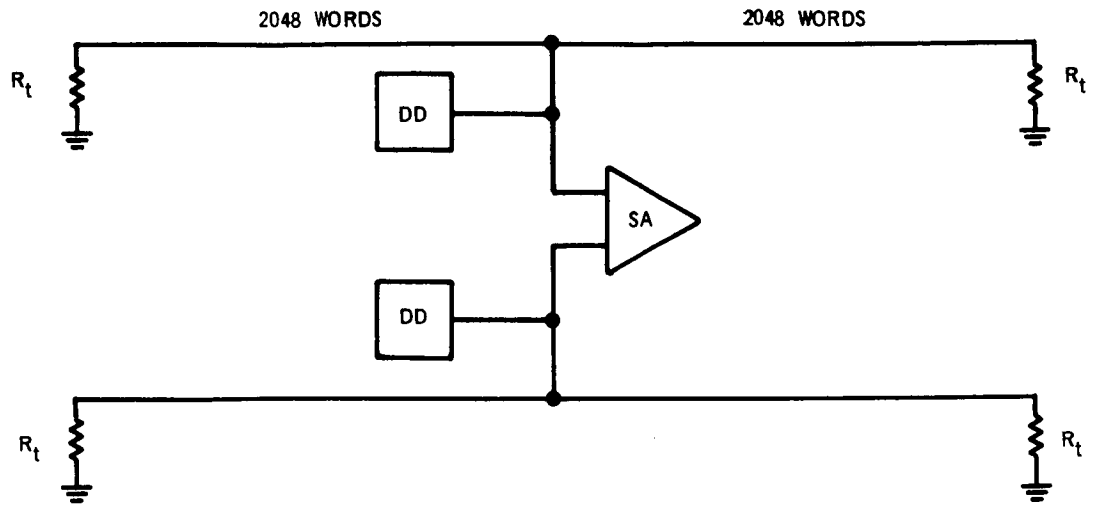



Figure 22. Center-Tapped Digit Line Configuration

3. With the lines grounded, the digit current split between the two lines will be dependent on the line resistance match.
4. With the lines grounded, improper reflections will appear at the sense amplifier during the sense strobing interval.
5. The digit drivers will be required to produce double the current of the single-line configuration, doubling digit power dissipation.

B. Bridge Connection (Figure 23)

Advantages:

1. No sense amplifier breakdown problem.
2. Sense signal delays are within acceptable limits.

Disadvantages:

1. The number of digit drivers, and the digit power is doubled relative to the 4096-word digit/sense line configuration.
2. A reflection problem exists due to the line mismatch when the digit drivers are off during read.
3. Signal attenuation is about 12 dB.

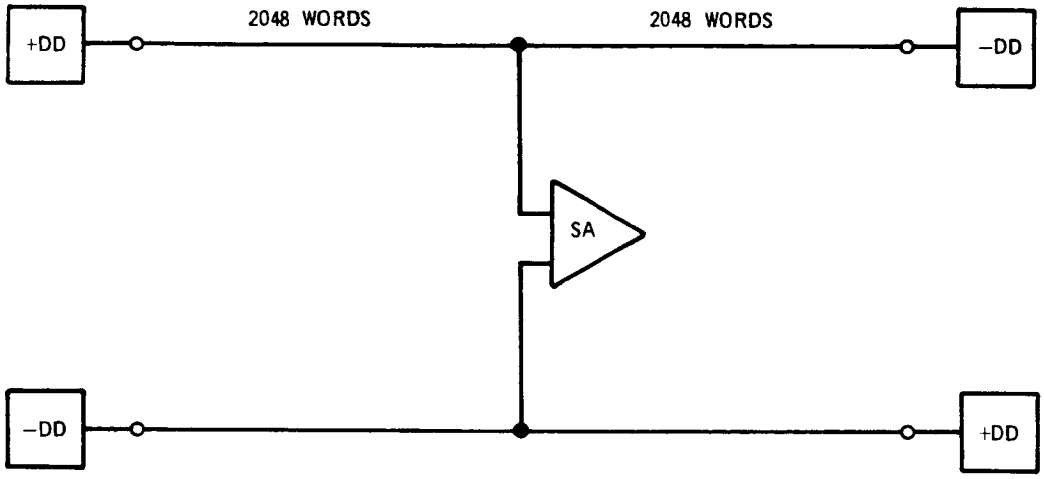



Figure 23. Digit Line Bridge Connection

C. Bridge Connection with Single-Ended Digit Drivers (Figure 24)

Advantages:

1. No sense amplifier breakdown problem.
2. Sense signal delays are within acceptable limits.

Disadvantages:

1. A reflection problem exists due to the line mismatch at the digit drivers.
2. Signal attenuation is about 12 dB.

D. Bridge Connection with Parallel Digit Drive (Figure 25)

Advantages:

1. No sense amplifier breakdown problems.
2. Sense signal delays within acceptable limits.
3. No reflection problems.

Disadvantages:

1. Digit current split is dependent on line resistance match.
2. Digit power is doubled.
3. Signal attenuation is about 12 dB.

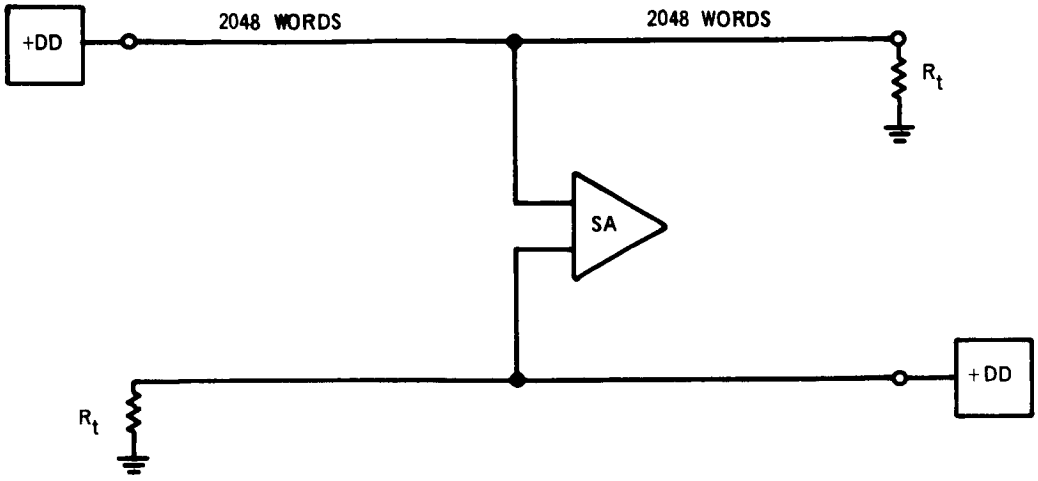



Figure 24. Digit Line Bridge Connection with Single-Ended Digit Drivers

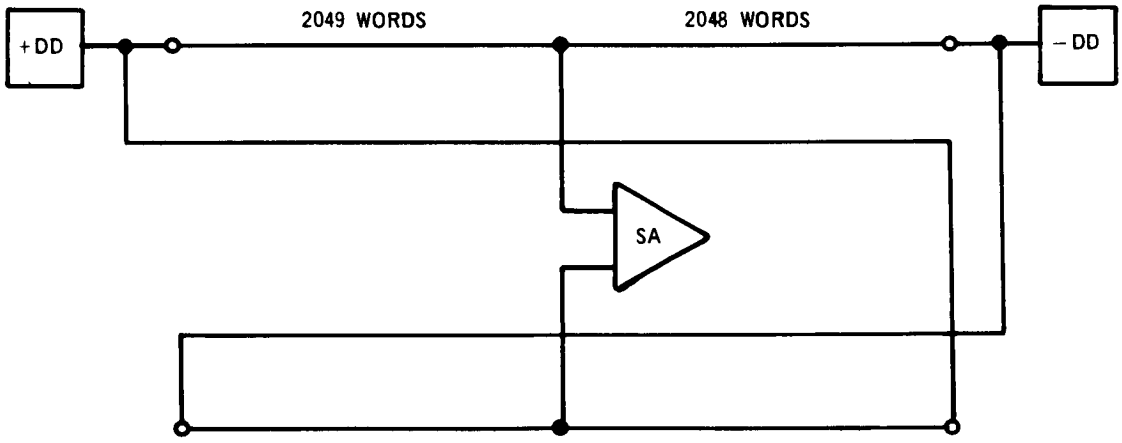



Figure 25. Digit Line Bridge Connection with Paralleled Digit Drivers

E. Split Lines with Digit/Sense Switches (Figure 26)

Advantages:

1. No sense amplifier breakdown problem for grounded lines.
2. Sense signal delays within acceptable limits.
3. Maximum signal attenuation 6 dB.
4. Reflections from grounded lines are in phase with desired signal.

Disadvantages:

1. Additional circuit elements are required for digit/sense switches.

6. Digit/Sense Switch Investigation

Results of the digit/sense line study, reported in the previous section, demonstrate that the timing requirements and sense amplifier sensitivity preclude the use of digit lines longer than 2048 words. One solution to this condition is the use of twice the number of digit drivers and sense amplifiers as are required for 4096-word digit/sense lines, so that each 4096-word line is split in half, each half having separate electronics. The disadvantage of this approach is that, although only the active circuits (as determined by the word address) need be powered, an additional 32 sense amplifiers and 64 digit drivers must be provided.

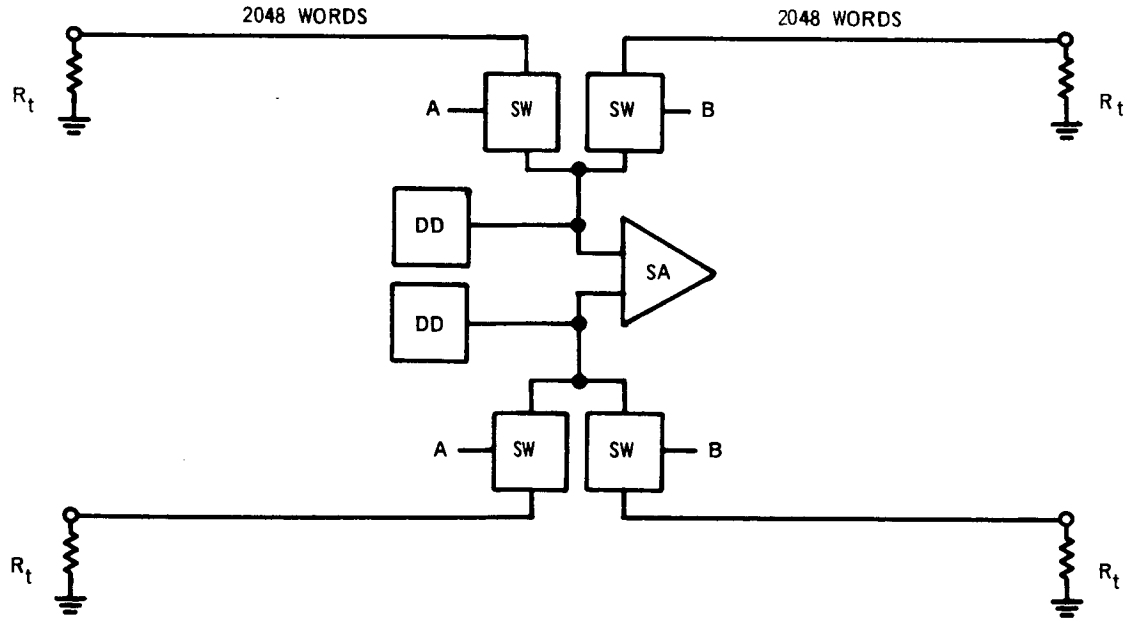



Figure 26. Split Digit Lines with Digit-Sense Switches

An alternate approach is to connect the two halves of each digit/sense line to the sense amplifier and digit driver through bidirectional transistor switches. Figure 27a shows the equivalent circuit of such an arrangement, for the two digit/sense lines associated with one bit. The switches will connect the proper half of each digit/sense line to the digit drivers and the sense amplifier in response to switching signals derived from the most significant bit of the word address.

The transistor switch must be capable of conducting the digit current in either direction with a low offset voltage and with minimum base drive. During the read time, the switch must conduct a millivolt level sense signal with little degradation and attenuation. There is a wide choice of transistors available for this application. Figure 27b, which shows the schematic diagram of the switch, shows the 2N2222A NPN and 2N2907A PNP transistors used. Each of these devices has low $V_{CE}$ at 20 mA (the design digit current), high current gain, and low offset voltage when used in an inverted connection to carry the sense signal.

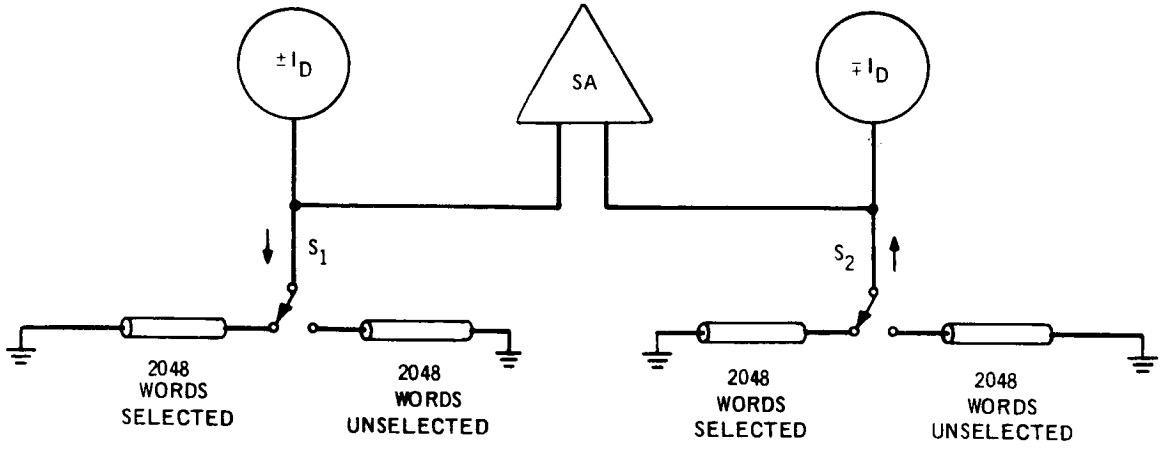
A pair of discrete circuits is required to provide the ±3-V control signals needed to operate the digit line switches. The same two transistor types can be used to switch the control signals.

A series of preliminary tests were made using a 2N2222A and a 2N2907A for the switch transistors. At 20 mA current in each direction, with 1.0 mA of base current, the saturation voltage was 80 mV. The differential offset voltage, when used as a low level switch for the sense signal, was measured for five different pairs of transistors, with fixed drive signals. The largest offset voltage measured was 7.27 mV. Since the sense amplifier's MC1510 preamplifier has a linear input range of over 80 mV, this offset voltage will not affect sense amplifier performance.

## 7. Recommended Stack Configuration

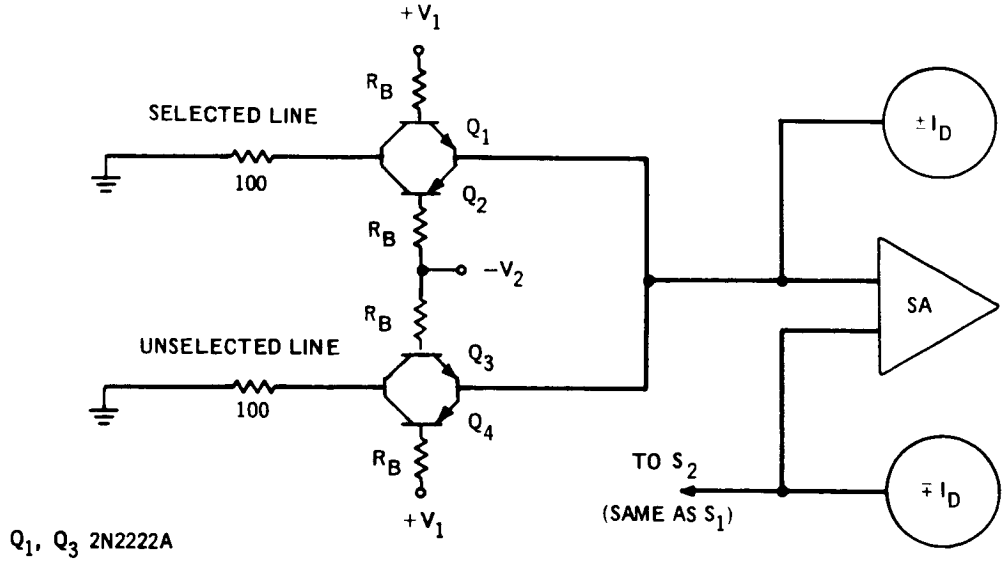
The 4096-word, 32-bit-per-word memory stack must be designed and assembled as two 2048-word, 32-bit-per-word units, with the corresponding digit pairs of each unit connected to a common set of digit drivers and sense amplifiers through a set of digit line switches.

Figure 28 shows the word selection matrix. Each of the write drivers WD 1 through WD 64 is connected to 64 word lines, and each of the write switches WS 1 through WS 64 is connected to 64 word lines, so that each combination of write driver and write switch is connected to a single word line. The write drivers are connected through isolation diodes, so that the write current will pass only through the selected word line and not through the path formed by all of the other lines. Each of the read drivers RD 1 through RD 64 is also connected, through isolation diodes, to 64 word lines, and each of the read switches RS 1 through RS 64 is connected to 64 word lines, so that each combination of read driver and read switch is connected to a single word line.




a) IDEAL EQUIVALENT CIRCUIT

Figure 27a. Digit Line Equivalent Circuit




$Q_1$, $Q_3$ 2N2222A
$Q_2$, $Q_4$ 2N2907A
$V_1$, $V_2$ ±3V

b) SWITCH CIRCUIT DETAILS

Figure 27b. Digit Line Switch Circuit Details

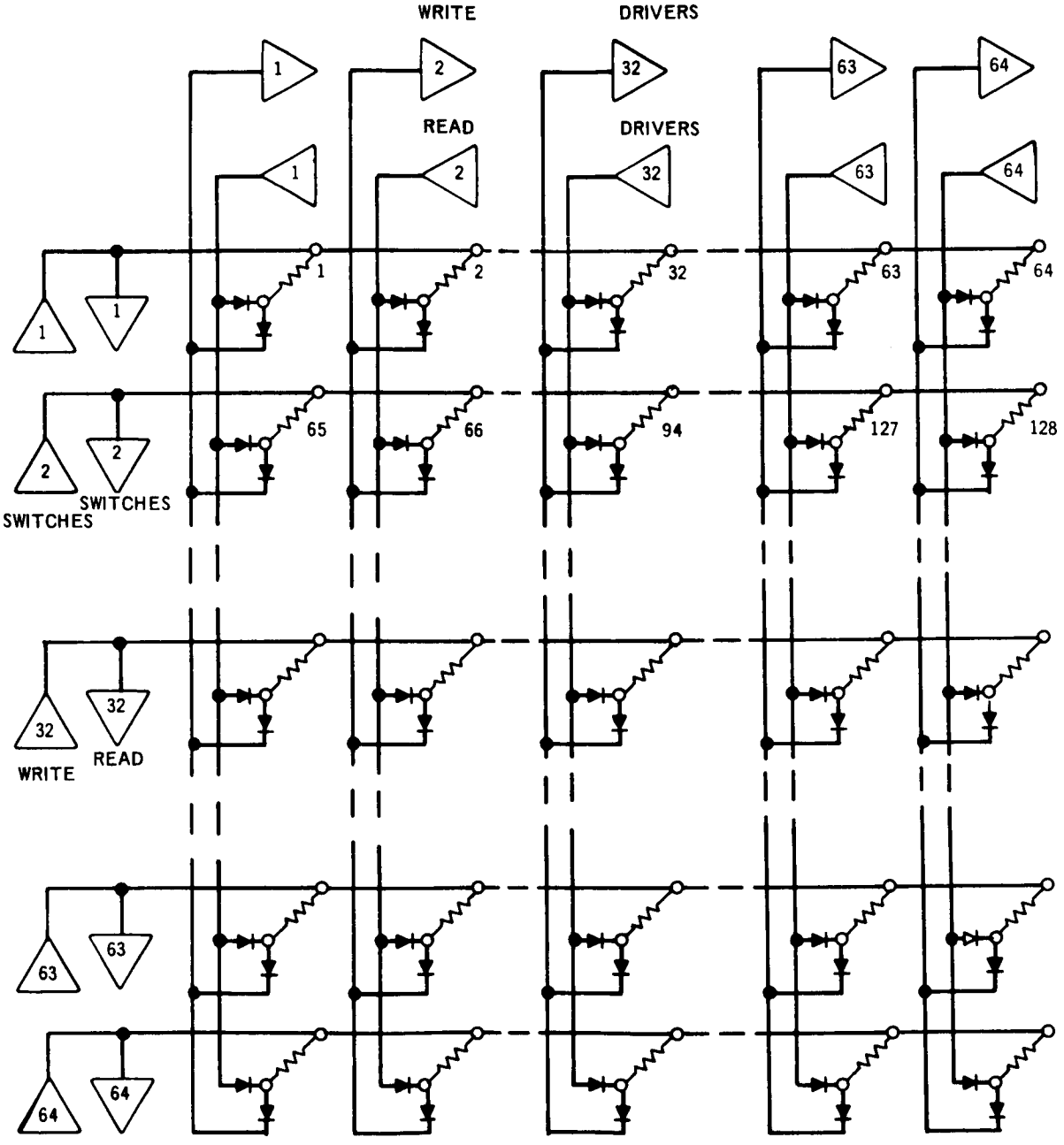



Figure 28. Word Selection Matrix

Figure 29 shows the method of digit line selection. The two halves of each digit pair are connected to a bidirectional digit driver and to a sense amplifier through a set of digit line switches. The switches used for one half of the stack are energized by the most significant bit ($X_0$) of the address register. The other switches, for the second half of the stack, are energized by the complement ($\overline{X}_0$) of the most significant bit of the address. In this way one half of each digit line will be used if the address is from word "0" to word "2047", and the other half of each digit line will be used if the address is from "2048" to "4095".

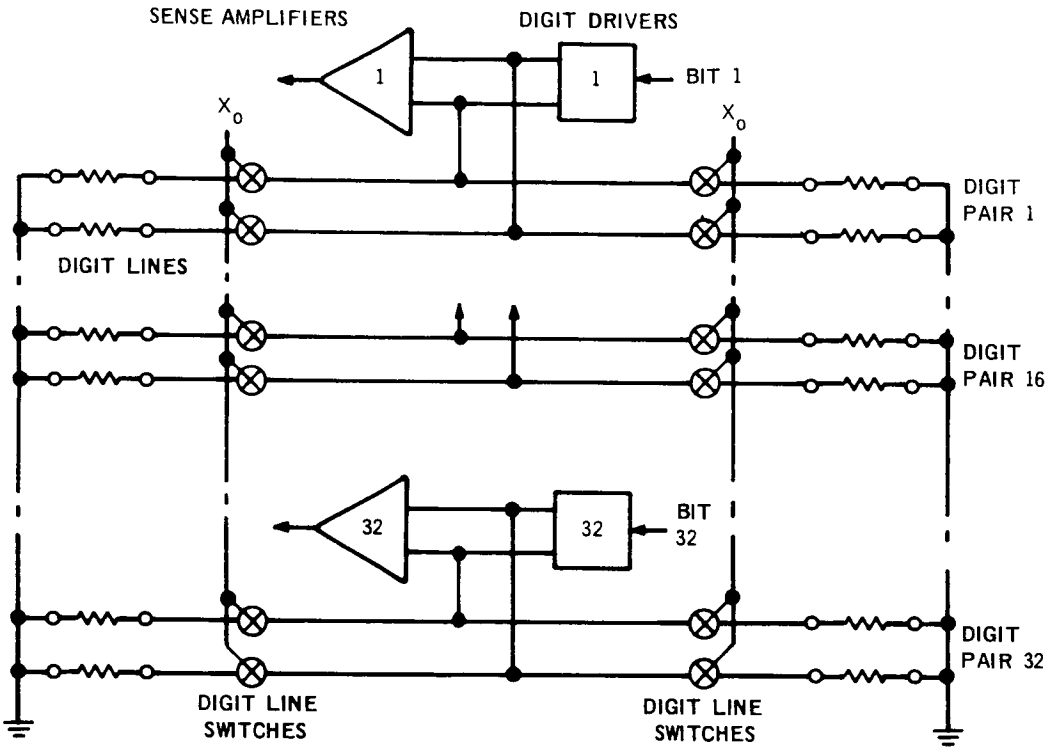



Figure 29. Digit Line Selection

## B. MOSFET LOGIC INVESTIGATION

Selection of the best method for MOS implementation of the memory logic is based on five basic factors: availability, speed, power, size, and cost. Four possible methods are analyzed below with respect to these factors.

### 1. P-MOS Circuits

The memory system logic was examined for possible implementation using P-MOS digital logic arrays. These arrays consist of large numbers of P-MOS transistors fabricated on a monolithic silicon chip. A study of available arrays from RCA and other suppliers showed that the only arrays available from other suppliers were shift registers, not usable for general logic. Two types of RCA universal arrays were considered. The first of these is known as the Gate Universal Array, and consists of 52 two-input gates which can be interconnected on the chip to form almost any desired static digital logic network. The second of these is known as the Register Universal Array, and it consists of 96 dynamic shift register stages which can be interconnected on the chip to form dynamic registers of various lengths.

#### a. P-MOS Gate Universal Array (GUA)

GUA is a P-MOS array of 52 cells. Each cell contains four P-MOS devices of various geometries. The cells and devices are physically arranged for easy construction and interconnection of NOR gates of various fan-in.

Using specified design constraints, the array is capable of operation at speeds up to 1 MHz. The high speed is attained using dynamic logic, precharge buffers and critical clock phase timing. Several circuit designs have been analyzed to determine the feasibility of using the GUA for memory decode logic. It was found that the fastest decode circuit would have a stage delay of about 800 ns, with an optimum metalization layout. These decode circuits also require the generation of a two-phase strobe signal to drive transmission devices and precharge buffer circuitry.

A typical decode circuit is shown in Figure 30. The circuit consists of a six-input NOR gate followed by a precharge buffer circuit. The precharge buffer is required to speed up the output transition edge (0 to -12 volts). The delay through the precharge buffer is 400 ns driving a load of 30 pF. The delay through the NOR gate (0 to -9 volts) is about 400 ns.

The decode circuit is first clocked to -12 volts by $\phi 1$. The decoded output level of the NOR gate is then clocked to node N by $\phi 2$. If the decoded level at N is 0 volt, the output remains at -12 volts. If the level at N is -12 volts, the output level goes to 0 volts. Note that the circuit output is valid only during the presence of $\phi 2$.

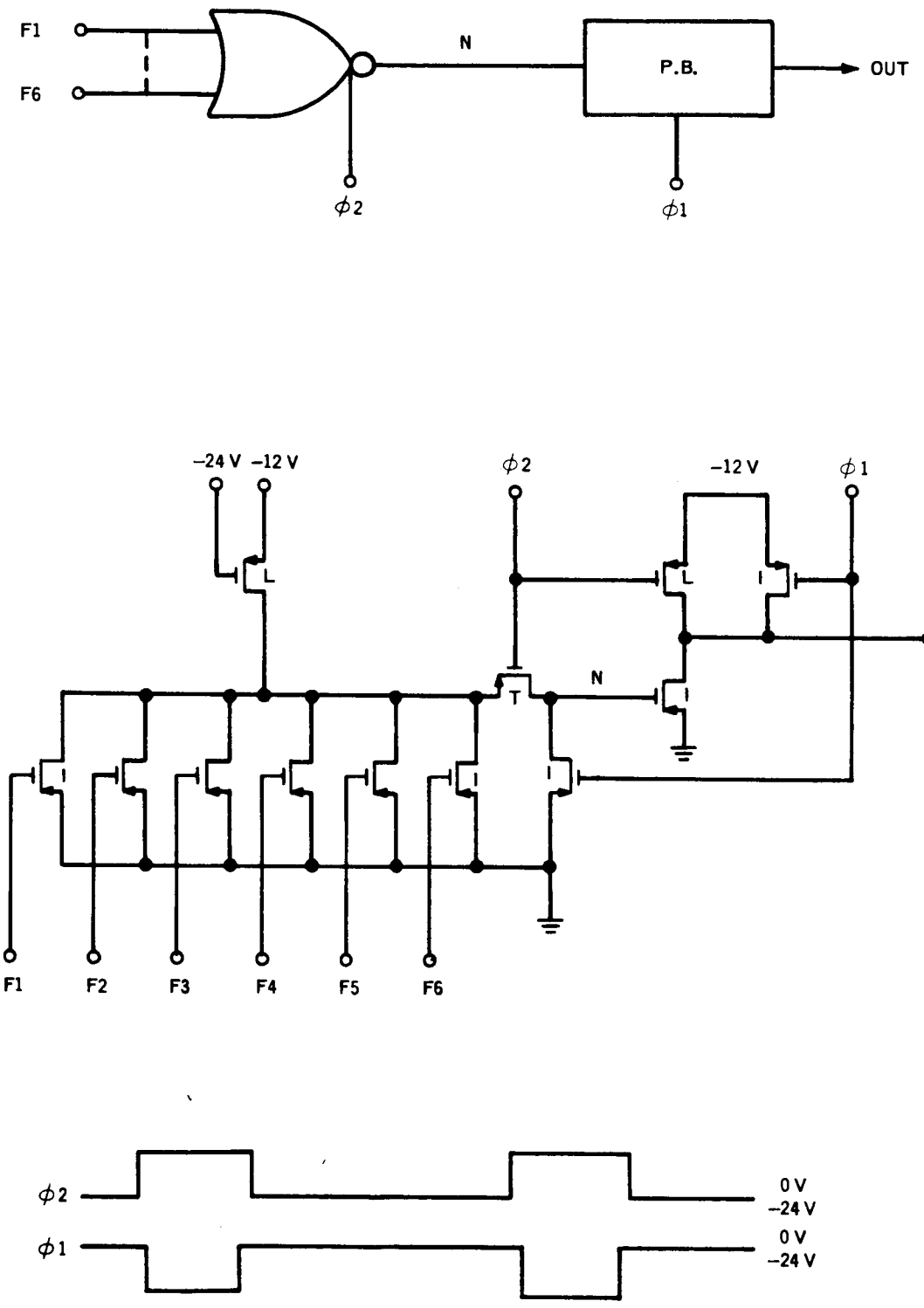



Figure 30. Decode Stage Using GUA

The total delay is:

for a -12 volt level: 400 + 400 = 800 ns

for a 0 volt level: 400 ns.

These time estimates are based on an optimum layout and would have to be verified experimentally.

Using the above scheme, a total of 8 decode circuits can be placed on a single chip. This number is limited by the number of bonding pads on the array. Sixteen packages would be required to implement the entire decode matrix.

Use of the GUA requires both input and output buffers. Assuming the address is to be decoded from IC logic levels, an input buffer is needed to translate logic levels. Due to the high output impedance of the P-MOS circuits, an output buffer with a high input impedance, probably the gate of an MOS, is required.

b. P-MOS Register Universal Array (RUA)

RUA consists of 192 inverter components which can be custom interconnected to produce 96 dynamic shift register stages. The 96 stages can be connected to form registers of various lengths. Seventeen signal bonding pads are available on the array, limiting the number of discrete registers.

Dynamic registers constructed on this array have a low-frequency limit of about 10 KHz. Quasi-static shift registers can be constructed with requirements imposed on the phasing and duty cycles of the two-phase register clocks.

Parallel IN/OUT operation of the register stages is not possible because of the nature of the circuitry and the 17 signal pad limit.

RUA is a new development. At the time of this investigation, only one test metalization had been fabricated. Testing of this circuit was then being performed by the designers. No test results were available.

After consulting with RCA Defense Micro-electronics personnel, it was concluded that RUA can not be used for implementation of the memory register logic. This decision was based on the following reasons:

a) Lack of parallel operation.

b) Dynamic nature of the registers.

c) Developmental nature of the array (Performance specifications have not been generated).

2. Complementary MOS Circuits

a. Complementary MOS Arrays (CMOS Arrays)

Because of the high speed and low power of CMOS logic, CMOS arrays are the ideal method of logic implementation. During the study, custom or universal arrays directly applicable to the study were not available. A seven-stage binary counter array capable of operation to 14 MHz has since become available. Samples of this array should be evaluated for possible use in the control logic of a memory.

b. Complementary MOS Discrete Logic Elements

Discrete CMOS logic elements are currently available. Packages containing dual three-input NOR gates and one inverter are available from RCA at $17.50 each. These gates dissipate low power (1 nanowatt quiescent) and operate with a typical pair delay of 50 ns. The gates can be operated from a 6 volt supply, compatible with IC logic level outputs of 0 and +6 volts. The fan-out capability of 50 unit loads enables a matrix decode scheme to be used.

3. Tradeoff Analysis

a. Availability

a) The Register Universal Array is available on an experimental basis.

b) The Gate Universal Array is available to a specification.

c) Complementary MOS arrays are not available.

d) Complementary MOS logic elements meeting military specifications are available from RCA. Logic implementation using these devices will be directly applicable to arrays when they become available.

b. Analysis

During the study, it was determined that the RUA and CMOS arrays were not feasible. The P-MOS GUA and the CMOS logic elements were compared to determine the best method for implementing the memory logic. The decode logic was used as the vehicle for this comparison. The results are tabulated in paragraph c.

(1) Decode Delay Driving 30 pF

GUA has a total decode delay of 800 ns not including the delay in the input and output buffer circuits. CMOS decode logic has a total delay of about 180 ns.

(2) Power at 500 KHz

GUA will dissipate a total of 5.2 mW per decode not including the power dissipated in the buffer circuits. The total power dissipated by the decode matrix is 665 mW, at any frequency. CMOS logic dissipates power only when switching. At 500 KHz, the power dissipated is (10 gates) x ($8 \times 10^{-4}$ watts/gate) = 8 mW. This is the worst-case power dissipation. At 100 KHz, the dissipation is about 1 mW.

(3) Relative Size

Implementation of the decode logic using the GUA requires 16 packages. Using an 8 x 8 matrix, implementation of the decode logic using CMOS logic elements requires a total of 80 packages. From these 80 packages, a total of 48 inverter circuits will be unused.

(4) Relative Cost

Using an estimated cost of $3000 per metalization design, the decode logic using the GUA would cost $3000. This figure does not include manpower used to generate specifications, speed calculations, an optimum mask design or buffer circuit design. Decode logic implementation using CMOS logic elements would require a total of 80 units at $17.50 per unit for a total cost of $1400. Since the units are compatible with IC logic there is not a requirement for input or output buffers.

c. Comparison of Decode Implementations

| | P-MOS | CMOS |
|---|---|---|
| Number of packages | 16 | 80 |
| DC power per decode | 5.2 mW | 5 mW |
| Total decode power | | |
| at 500 KHz | 665 mW | 8 mW |
| at 100 KHz | 665 mW | 1 mW |
| Stage delay, $C_L$ = 30 pF | 800 ns | 180 ns |
| Buffer circuits required | Input<br>Output | None |
| Cost for decode hardware | $3000 | $1400 |
| Engineering manpower required | 2.0 MM | 0.25 MM |

d. Conclusions

P-MOS arrays are not usable for implementation of the memory logic for the following reasons:

- Speed,
- Power dissipation,
- Input and output buffers, and
- High engineering cost.

Discrete complementary MOS logic elements provide the most feasible method of MOS implementation. Complementary MOS logic is not currently available in arrays. However, logic designs using discrete elements will be directly applicable to CMOS arrays when available. Discrete CMOS logic elements offer the following advantages:

- Low power,
- High speed,
- Logic levels compatible with bi-polar integrated circuits,
- High fan-out, and
- Low output impedance in either state.

Complementary MOS discrete logic elements are recommended for the memory logic.

## C. MOSFET DRIVER INVESTIGATION

MOSFET devices designed to drive ferrite word lines have been fabricated by RCA Laboratories under Contract NAS 1-5794 on an experimental basis. The drivers were fabricated in strips, each strip containing 64 units. The following results were obtained:

1. The yield, based on 20 strips from the last two wafers, was 5%. By cutting good 32-element segments from the strips, a yield of 30% could have been achieved.
2. Electrical non-uniformity of the device characteristics will result in word current variations of about ±20%, based on a nominal word current of 105 milliamperes.
3. The devices as fabricated have shown a tendency to fail within months. A major cause of these failures is the special metal alloy needed for compatible driver-laminate interconnections.

The laminated ferrite memory system requires drive currents as high as 200 milliamperes. Based on low reliability and inadequate current output of the experimental drivers, it was concluded that these devices are not ready for practical use. The task was terminated with no selection, since further development of MOS drivers was not included in the scope of the contract.

## D. HYBRID DRIVER INVESTIGATION

An investigation was conducted to determine the feasibility of hybrid integrated circuit drivers for the word and digit lines, and to design a suitable set of hybrid circuits. The need for hybrid construction for these driver circuits is a result of the unavailability of monolithic circuits with sufficiently high current capability. As a result it is necessary to fabricate the drivers using discrete transistor chips mounted in the smallest sealed container, with chip resistors mounted on the same substrate and with wired interconnections.

As is indicated below, the requirements for these circuits were first established, and then a number of alternate approaches were considered to determine the best approach. The circuits selected in this way were then designed, breadboarded and tested.

### 1. Driver Requirements

Each digit driver will deliver a bilateral current to a single digit line in the memory. The direction of current will be controlled by a single DATA input coincident with a memory timing signal. The current levels required of the digit driver circuits are +22 ma and -22 ma. The tolerance on these levels is ±10%.

The Read and Write drivers will each deliver single polarity current. The load on each driver will be one of 64 selected laminated ferrite word lines and 63 reverse biased diodes, all in parallel. A Read/Write driver pair will be selected by a single address input (ADD). The durations of the Read and Write currents will be controlled by two memory timing signals called Read Driver Gate (RDG) and Write Driver Gate (WDG). The current levels required of the Read and Write drivers are 200 ± 10% ma and 110 ± 9% ma respectively.

Two word switch circuits are required. Each Read/Write switch pair will be connected to 64 word lines and a parallel 220 Ω termination resistor. The Read Switch must pull this load to -6 volts potential and sink the Read current on one selected line. The Write Switch must pull the load to +6 volts and sink the write current on one selected line. Both switch circuits must maintain the respective potentials within 0.2 volts during the active current period. A Read/Write switch pair will be selected by a single address input (ADD). Active switch times will be determined by two memory timing signals called Read Switch Gate (RSG) and Write Switch Gate (WSG).

2. Approaches Considered

a. Single Current Source

One approach to the word driver design is to develop two separate constant current sources, Read and Write. The driver circuitry consists of current switches enabled by the address signal ADD. Active current time would be controlled by a single signal (RDG or WDG) to each current source.

The advantages of this approach are:

- A single current source enables a high degree of accuracy and temperature compensation.
- Low power dissipation since this current source is turned off during standby.

The disadvantage of this approach is the transmission of high current pulses throughout the memory circuitry. This will lead to excessively high noise levels, particularly in the low-level sense circuitry.

b. Constant Current Drivers

The constant current driver family is built around the stage shown in Figure 31.

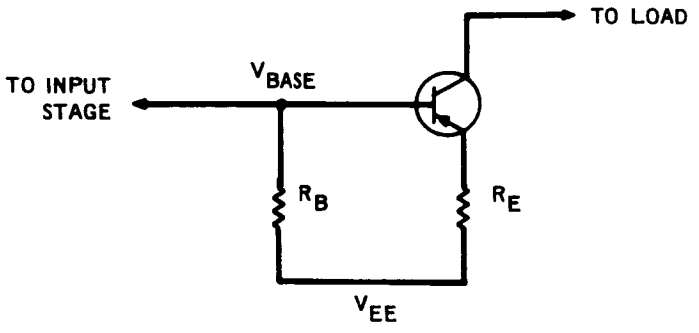



Figure 31. Constant-Current Stage

The constant current is controlled by the voltage across $R_E$ ($V_{EE}$ - $V_{Base}$ - $V_{BE}$). When the driver is ON, the base is pulled to ($V_{EE}$ - 6) volts by the input stage. When OFF, the base is switched to $V_{EE}$. For minimum delays and transition times, the output stage is designed to be nonsaturating when driving the memory line.

Two alternate input stages were considered. The first version uses an FET to produce the AND function of DATA (or ADD) and GATE. The voltage reference for the constant current is determined by $V_G$ and the drain to source voltage of the FET. The second version has a transistor input stage with a low-voltage zener diode producing the reference voltage.

Because of the input current required of the transistor stage and the superior performance of the FET switch, the FET version was selected.

3. Selected Approach

The second approach, with constant-current sources in each driver, was selected. This will minimize noise pickup.

This approach has the following advantages:

a. Minimum Power - Each circuit requires no power in standby. Power is dissipated only during the active current time.

b. High Speed - Non-saturated operation of the circuits yields minimum stage delays.

c. Constant Current - Each driver circuit is designed to provide its own constant current source.

d. Symmetry of Design - Each circuit in the family is designed with the same basic configuration for ease of fabrication.

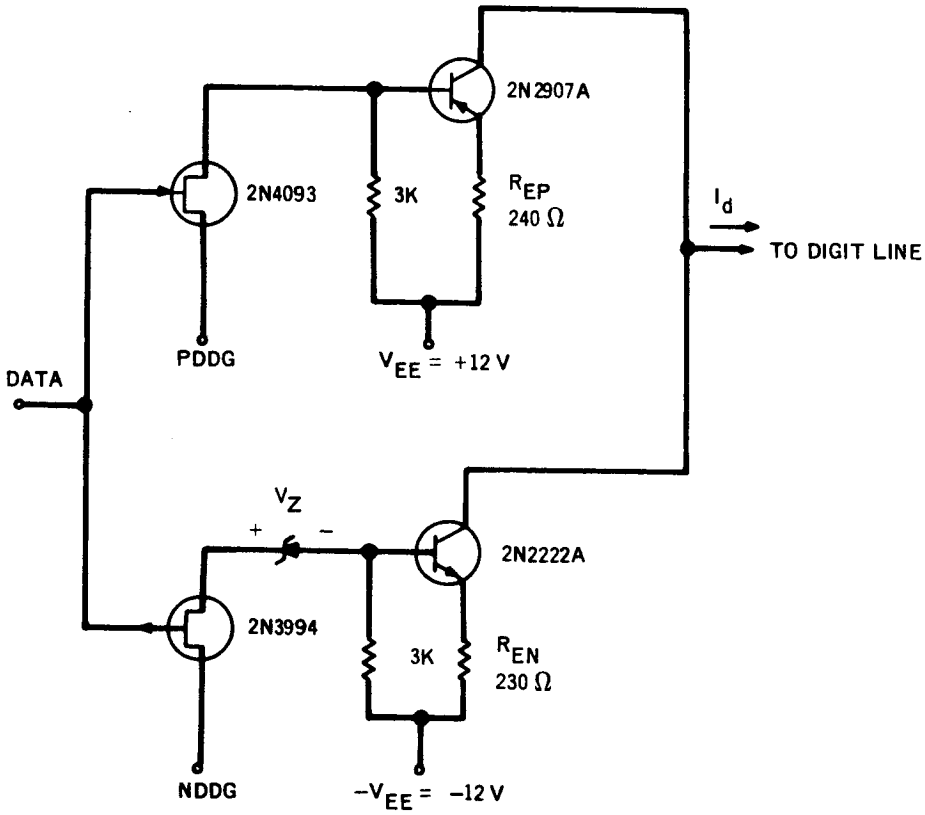
e. Controllable Transition - The output current follows the input gate transition. This feature enables close control of the word line transients due to reactive components of the load.

4. Detail Circuit Design

The digit driver schematic and truth table are shown in Figure 32. Digit current polarity is determined by the data input. When the data is high, (+6 volts), positive current is enabled. When the data is low, (0 volts) negative current is enabled. During active digit time, PDDG goes to +6 volts, NDDG goes to GND, and the enabled digit driver will turn ON.

The current in each case is determined by the voltage at the emitter of the output transistor. For positive digit current:

$$I_d = \alpha_B \cdot \frac{V_{EE} - (V_{BE} + V_{DS} + V_{PDDG})}{R_{EP}}$$




| DATA | PDDG | NDDG | $I_d$ |
|---|---|---|---|
| 0 V | X | −12 V | 0 |
| 0 V | X | 0 V | −22 ma |
| +6 V | +12 V | X | 0 |
| +6 V | + 6 V | X | +22 ma |

Figure 32. Bi-Directional Digit Driver

For negative digit current:

$$I_d = \alpha_B \cdot \frac{-V_{EE} + (V_{BE} + V_{DS} + V_{NDDG} + V_Z)}{R_{EN}}$$

The tolerance on each current will consist of the initial tolerance which the supplier must guarantee for nominal conditions plus the variation over temperature of parameters in the current equations.

The positive digit current tolerance is tabulated as follows:

| Parameter | Variation of $I_d$ @ T = +80°C | Variation of $I_d$ @ T = -20°C |
|---|---|---|
| Initial Tolerance | ±5% | ±5% |
| $\alpha_B$ | ±1% | -1% |
| $V_{BE}$ | +2.2% | -1.8% |
| $V_{DS}$ | -1.3% | +1.1% |
| $V_{EE} - V_{PDDG}$ | ±1.5% | ±1.5% |
| $R_{EP}$ | +1.7% | -1.4% |
| Total Tolerance from Nominal Digit Current | +9.8%<br>-2.9% | +3.4%<br>-9.6% |

The negative digit current tolerance is tabulated as follows:

| Parameter | Variation of $I_d$ @ T = +80°C | Variation of $I_d$ @ T = -20°C |
|---|---|---|
| Initial Tolerance | ±5% | ±5% |
| $\alpha_B$ | +1% | -1% |
| $V_{BE}$ | +2.2% | -1.8% |
| $V_{DS}$ | -1.3% | +1.1% |
| $(V_{NDDG} + V_Z)$ | -2.2% | +1.8% |
| $V_{EE}$ | ±3% | ±3% |
| Total Tolerance from Nominal Digit Current | +7.7%<br>-8.2% | +8.1%<br>-7.9% |

Each circuit dissipates no power in standby. The total power dissipated during digit time is 264 mw/driver. Of this total power, about 73 mw is dissipated in the memory line and termination, and 191 mw is dissipated in the driver. The average power per digit driver at a 500 KHz data rate is:

$$(191 \text{ mw}) \frac{(750 \text{ ns})}{2\ \mu\text{s}} = 71.6 \text{ mw}$$

The Word Driver schematic and truth table are shown in Figure 33. The address input (ADD) enables a selected pair of word drivers with a GND level signal. The READ/WRITE cycle is generated by first strobing RDG to +6 volts for the duration of the read current, then strobing WDG to GND for the duration of the write current. The inverter input stage in the Read circuit is required to enable the read driver with a level compatible with the write driver ADD input.

The word current is determined by the voltage on the emitter of the first output stage transistor. Consider the Middlebrook configuration in Figure 34.

For DC conditions, the read current is:

$$I_R = I_E - (I_B + I_A) = 220 \pm 22 \text{ ma.}$$

Since the selected word line is first switched to -6 volts, the DC current ($I_A$) through the bias resistor $R_A$ is:

$$I_A = \frac{V_{BE} + V_D + V_{CE(SAT)} + I_R R_L}{R_A}$$

or:

$$I_A = 3.5 \text{ ma Nominal.}$$

The base current $I_B$ is:

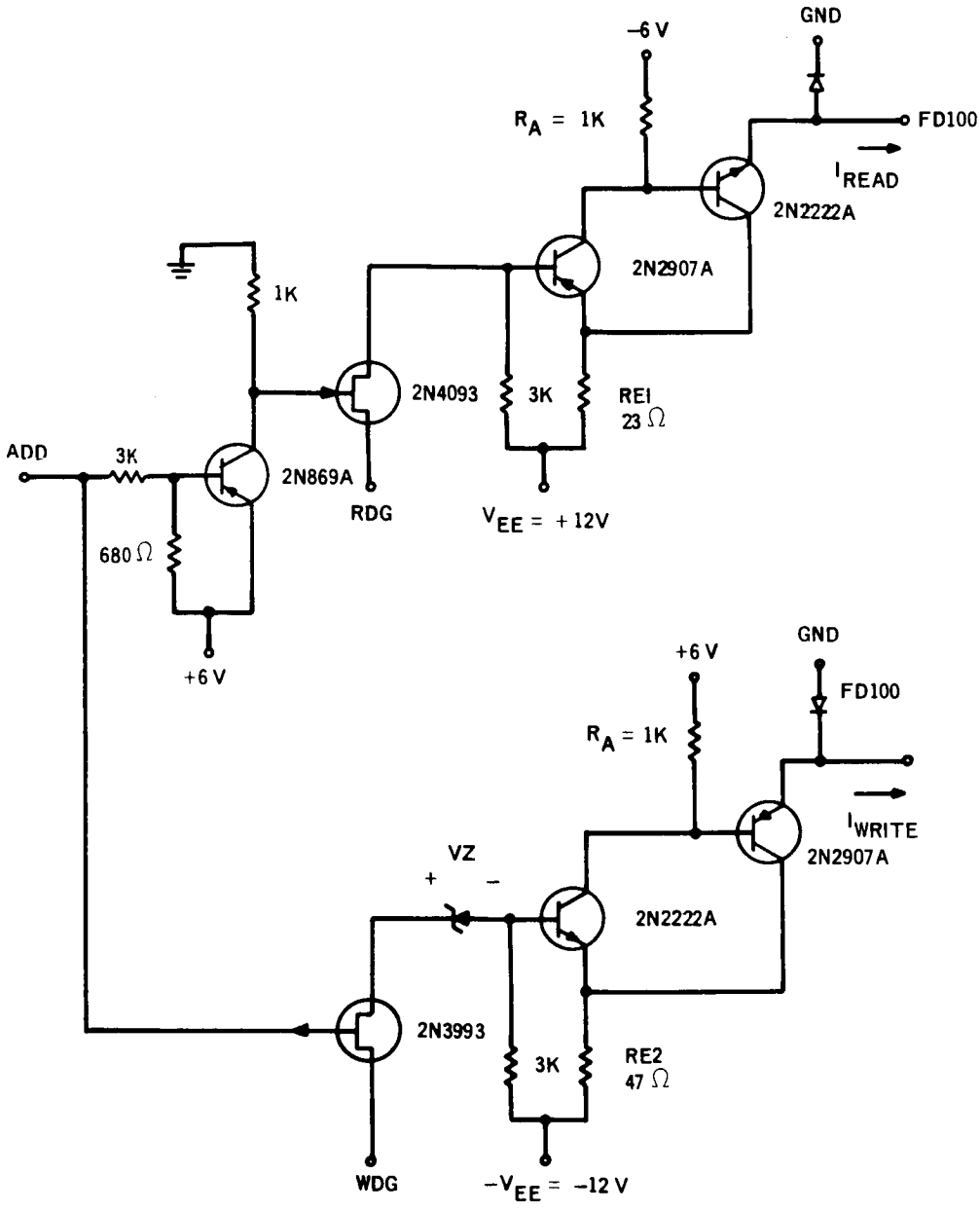
$$I_B = \left[ \frac{I_R}{\beta_1 (\beta_2 + 1)} + \frac{I_A}{\beta_1} \right]$$

$$= \left[ 0.524 + 0.175 \right] = 0.699 \text{ ma for } \beta_1, \beta_2 = 20.$$

The constant current required through $R_E$ is then

$$I_E = I_R + (I_A + I_B)$$

$$= 220 \pm 22 + (3.5 + 0.7) = 224.2 \pm 22 \text{ ma Nominal.}$$




| WORD STATE | ADD | RDG | WDG | $I_{READ}$ | $I_{WRITE}$ |
|---|---|---|---|---|---|
| Addressed | 0 V | +12 | -12 | 0 | 0 |
| Write | 0 | +12 | 0 V | 0 | -110 ma |
| Read | 0 V | + 6 | -12 | +220 ma | 0 |
| Not Addressed | +6 | X | X | 0 | 0 |
| Not Allowed | 0 | + 6 | 0 | X | X |

Figure 33. Read-Write Driver

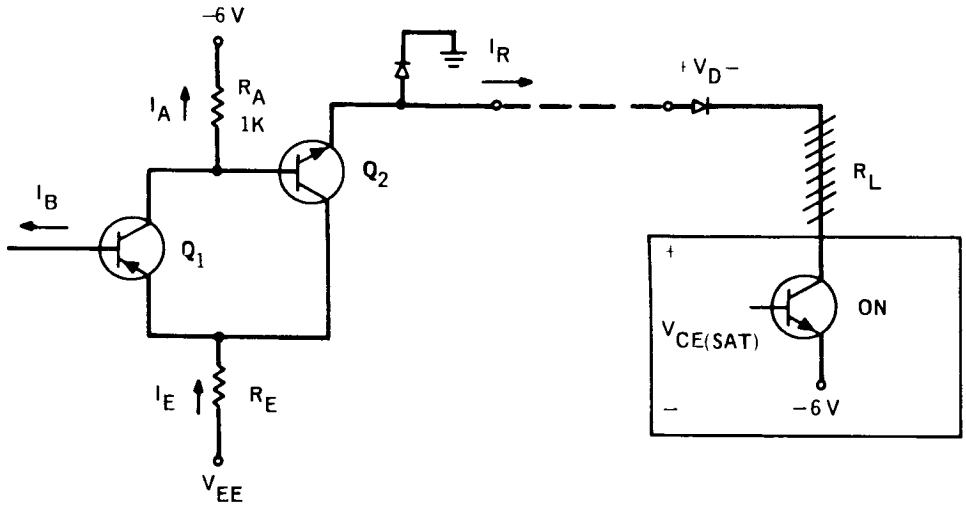



Figure 34. Middlebrook Circuit

The current lost, $(I_A + I_B)$, is 1.9% of the nominal read current. The currents $I_A$ and $I_B$ are the only portions of the read current which are dependent upon the circuit load and transistor characteristics ($R_L$, $\beta$, $V_{BE}$, $V_{CE}$).

A 50% variation in $(I_A + I_B)$ over temperature would result in a 0.95% variation in the Read Current.

The constant emitter current is:

$$(1) \quad I_E = \frac{V_{EE} - (V_{BE} + V_{DS} + V_{RDG})}{R_{E1}}$$

for the Read current and:

$$(2) \quad I_E = \frac{-V_{EE} + (V_{BE} + V_{DS} + V_Z + V_{WDG})}{R_{E2}}$$

for the write current.

Since both the Read and Write currents are less than 1% dependent upon load and transistor gain, the variations of the respective currents are mainly due to the worst-case variations of the parameters in equations (1) and (2). To eliminate the initial tolerances on $R_E$, $V_{BE}$, $V_{DS}$ and $V_Z$, the supplier will be required to guarantee an initial tolerance for nominal conditions. This initial tolerance will absorb all manufacturing variations of $R_E$, $V_{BE}$, $V_{DS}$, $V_Z$ and $(I_A + I_B)$. The variation of these parameters over temperature will then determine the final tolerance of the output currents.

The total tolerance on the read current is tabulated as follows:

| Parameter | % Variation of $I_R$ | |
|---|---|---|
| | at +80°C | at -20°C |
| Initial | ±5 | ±5 |
| $V_{BE}$ | +2.2 | -1.8 |
| $V_{DS}$ | -1.3 | 1.1 |
| $(I_A + I_B)$ | ±0.95 | ±0.95 |
| $(V_{EE} - V_{RDG})$ | ±1.5 | ±1.5 |
| $R_E$ | +1.7 | -1.4 |
| Total tolerance from nominal specified read current | +10.05%<br>-4.85% | +6.25%<br>-9.55% |

The write driver circuit utilizes the same output stage as the read driver with all transistor and voltage polarities reversed. The input stage includes a 6.2 volt zener diode to produce the voltage differential. The 6.2 volt value was chosen to give the supplier the option to use a base-emitter junction reverse breakdown.

The total tolerance on the Write current is tabulated as follows:

| Parameter | % Variation of $I_W$ | |
|---|---|---|
| | at +80°C | at -20°C |
| Initial | ±4 | ±4 |
| $V_{BE}$ | +2.2 | -1.8 |
| $V_{DS}$ | -1.3 | +1.1 |
| $(I_A + I_B)$ | ±0.95 | ±0.95 |
| $V_Z$ | -2.2 | +1.8 |
| $R_E$ | +1.7 | -1.4 |
| $V_{EE}$ | ±3.0 | ±3.0 |
| Total tolerance from nominal write current | +8.35%<br>-7.15% | +7.65%<br>-7.85% |

The diodes returned to ground at the output stages of both drivers serve to prevent the output transistors from approaching saturation during turn-on. The highly underdamped ringing on the RLC memory line load is clamped at ground maintaining a minimum $V_{CE}$ of about 5 volts.

Each Driver dissipates no power in standby. When the line is switched to -6 volts, the DC power dissipated in the read driver is:

$$P_R = (223 \text{ ma})(12 + 5) + (7 \text{ ma})(6 \text{ V})$$

$$= 3.83 \text{ watts}$$

When the line is switched to +6 volts, the DC power dissipated in the write driver is:

$$P_W = (112 \text{ ma})(12 + 5)$$

$$= 1.90 \text{ watts}$$

For a 500 KHz word rate, the average power is:

$$P_R = (3.8)\ \frac{375}{2} \text{ mw}$$

$$P_R = 718 \text{ mw}$$

and

$$P_W = (1.90)\ \frac{375}{2} \text{ mw}$$

$$P_W = 356 \text{ mw}$$

The word switch schematic and truth table are shown in Figure 35. The circuits are enabled and turned on in a similar fashion to the driver circuits. The read switch contains an inverter input stage to make the ADD enable level compatible with the write driver. The constant current stage is non-saturating and is the same configuration as the digit drivers described in section 4.1. Each circuit has a saturating transistor output stage designed to sink 400 ma with a minimum B of 20. The output transistor will be chosen to provide a minimum turn-off delay and minimum offset voltage when sinking the Read or Write current.

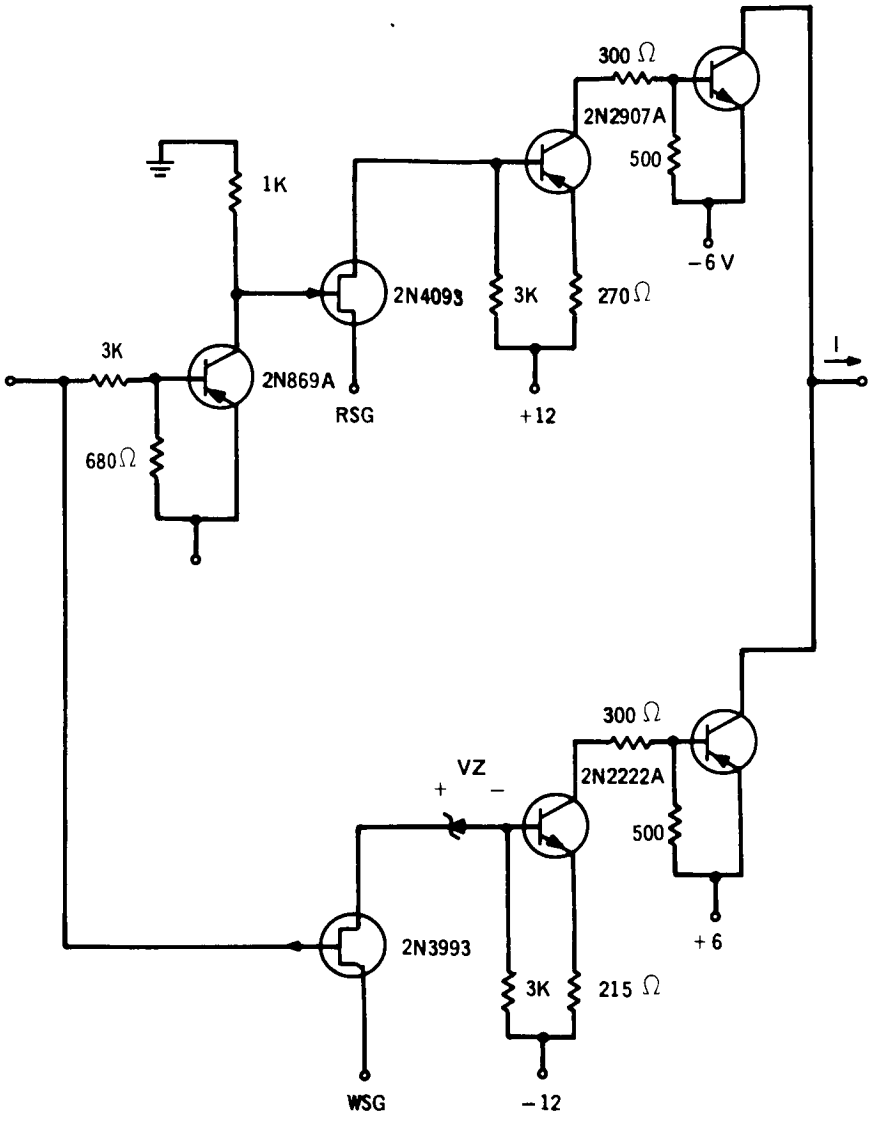
Excluding the load current, the Read and Write switch DC power dissipation is:

$$P_R = (22 \text{ ma})(18 \text{ volts}) + (7 \text{ ma})(6 \text{ volts})$$

$$= 438 \text{ mw}$$

and

$$P_W = (22)(18) = 396 \text{ mw}$$




| WORD STATE | ADD | RSG | WSG | I |
|---|---|---|---|---|
| Addressed | 0 V | +12 | -12 | 0 |
| Write | 0 V | +12 | 0 | I write |
| Read | 0 V | + 6 | -12 | I read |
| Not Addressed | +6 | X | X | 0 |
| Not Allowed | 0 | + 6 | 0 | X |

Figure 35. Read-Write Switch

The average power dissipation for a 500 KHz word rate is:

$$P_R = (438)\left(\frac{500}{2}\right) = 110 \text{ mw}$$

and

$$P_W = (396)\left(\frac{500}{2}\right) = 99 \text{ mw}$$

5. Hybrid Procurement

During the design effort, a number of hybrid circuit suppliers were contacted to ensure that the designs would be feasible in hybrid form. Most of the contacts were with Sprague Electric and with Amelco, during the design activity, and with Fairchild Semiconductor when the design was finished. A specification was prepared containing the requirements given above for each circuit, with options left for the supplier with respect to certain of the component types. Based on delivering to a performance-type specification, each of the suppliers contacted stated a willingness to produce the circuits, and budgetary quotations were received from Sprague and Amelco.

6. Hybrid Driver Breadboard Testing

All of the hybrid circuit designs were breadboarded using standard discrete elements. The breadboard models were used to prove the functional properties of the paper design and are not intended to exhibit the final hybrid characteristics. The vendor will be required to provide the final selected circuit elements for a more complete breadboard and paper analysis of the circuits.

a. Digit Driver Test Results

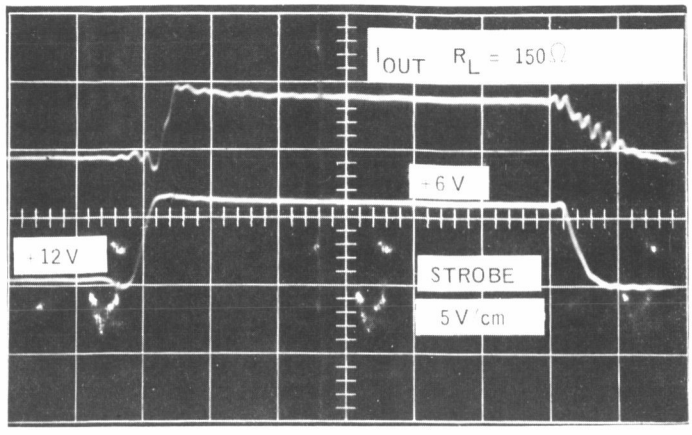
Figure 36 shows the results of the digit driver tests at room temperature.

b. Read Driver/Read Switch Test Results

The read driver/switch pair was breadboarded using the loading configuration shown in Figure 37.

The Read Driver was first tested with a fast transition on the leading edge of the input strobe signal, RDG. The resulting current from the Read Driver was approximately a step function ($t_r \approx 20$ ns). When driving the reactive load shown in Figure 37, the transients caused an initial current overshoot of about 75% on the word line. This

n-DIGIT DRIVER ROOM TEMP.




+6V

+12V

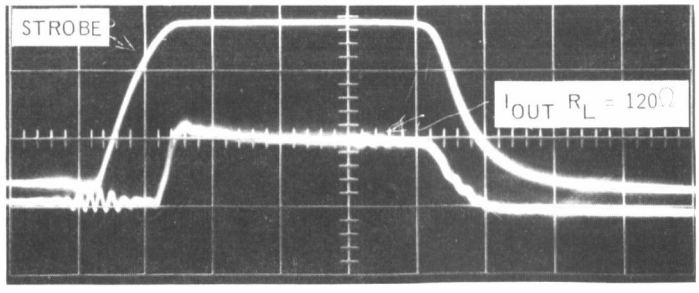
50 ns/cm

150Ω RESISTIVE LOAD
SWEEP = 50 ns/div.
I OUT = 20 ma/div.

1a

POSITIVE DIGIT DRIVER
UPPER TRACE: DIGIT CURRENT
LOWER TRACE: PDDG

+25°C




0V

VT

-12V

5 V/cm

50 ns/cm

P–TYPE DIGIT DRIVER

120Ω RESISTIVE LOAD
SWEEP = 50 ns/div.
I OUT = 20 ma/div.
$V_T$ = FET THRESHOLD

1b

NEGATIVE DIGIT DRIVER
UPPER TRACE: NDDG
LOWER TRACE: DIGIT CURRENT

Figure 36. Digit Driver Test Waveforms

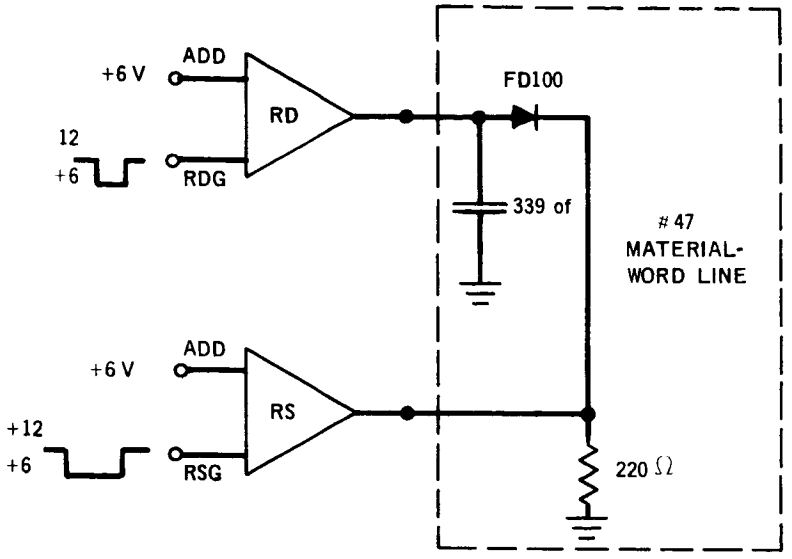



Figure 37. Read Driver-Switch Test Setup

ringing lasted for about 50 ns before reaching a DC current level. To minimize the overshoot, a controlled strobe circuit was designed. The function of this circuit is to develop a ramp input at RDG and thus present a ramp current drive to the reactive load. The RDG and its effect upon the read current is discussed in a later section on peripheral circuits.

Figure 38a shows the RDG and read current waveforms taken at room temperature.

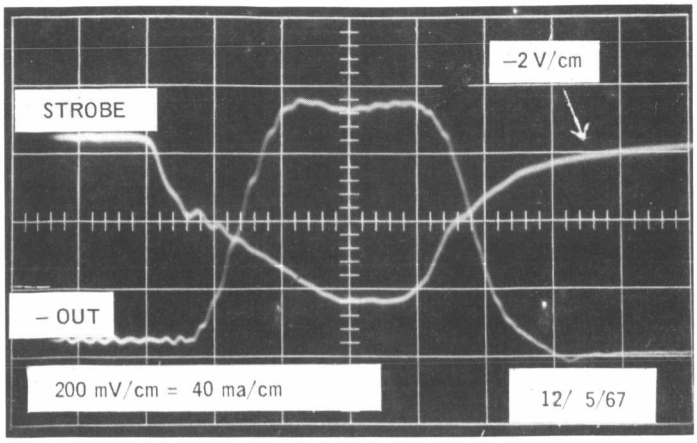
Figure 38b shows the turn-off delay of the read switch with respect to the RSG signal. The saturating output transistor used in this test was a 2N2222A.

c. Write Driver/Write Switch Test Results

The Write Driver/Switch pair was breadboarded using the loading configuration of Figure 37 with the FD100 diode polarity reversed. The current waveform is shown in Figure 39.

The major problem encountered in this group of tests was the write switch turn-off delay. For the test shown in Figure 39, a 2N869A PNP transistor was used as the output stage transistor.

PRIOR TO TEMP TEST @ RM. TEMP.

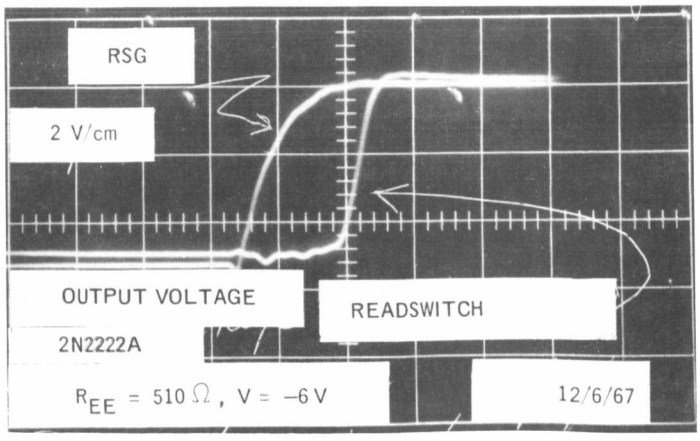



MEMORY LOAD OF
FIGURE 37

SWEEP = 50 ns/div.
I OUT ◘ 200 ma

READ DRIVER
a) UPPER TRACE: RDG
LOWER TRACE: READ CURRENT

READ SW TURN OFF DELAY




MEMORY LOAD OF
FIGURE 37

SWEEP = 50 ns/div.

READ SWITCH DELAY
b) UPPER TRACE: SWITCH OUTPUT VOLTAGE
LOWER TRACE: RSG

Figure 38. Read Driver-Switch Test Setup

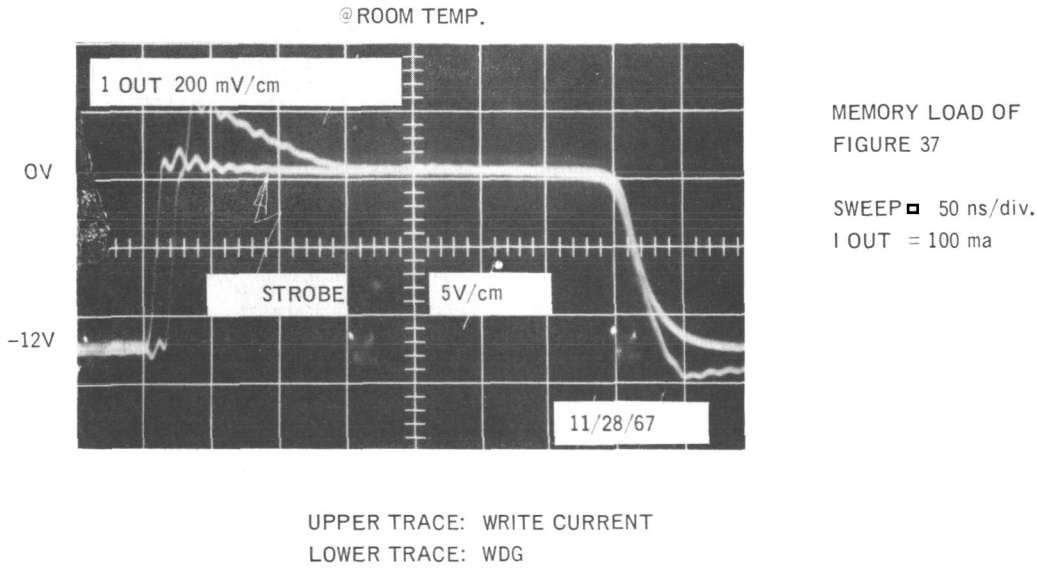



Figure 39. Write Driver Waveform

d. Temperature Tests

Each of the breadboarded circuits were tested at the +85°C and -25°C temperature extremes. The functional and transient characteristics were essentially unchanged at these temperatures. Extensive temperature testing of the circuits implemented with the final hybrid components will be necessary to verify the tolerance limits of the design.

7. Discrete Circuits Study

a. Required Circuits

Several discrete circuits are required to interface the IC logic modules and the memory drive and sense circuitry. The required circuitry and the loads they drive are tabulated in Table 3.

A preliminary design has been completed on the RDG and will be discussed in the following section. The remaining gate requirements are not as critical and will be presented functionally in the remaining sections.

TABLE 3.

LF MEMORY DISCRETE CIRCUITS

| Circuit Type | Number Required | Number of Loads |
|---|---|---|
| Read Driver Gate (RDG) | 1 | 64 Read Drivers |
| Write Driver Gate (WDG) | 1 | 64 Write Drivers |
| Read Switch Gate (RSG) | 1 | 64 Read Switches |
| Write Switch Gate (WSG) | 1 | 64 Write Switches |
| POS DD Gate (PDDG) | 2 | 64 Pos Digit Drivers |
| NEG DD Gate (NDDG) | 2 | 64 Neg Digit Drivers |

b. Read Driver Gate (RDG)

The RDG is designed to strobe a bank of FET switches internal to the hybrid Read Drivers. The output of the RDG is wired to the FET source input of each Read Driver.

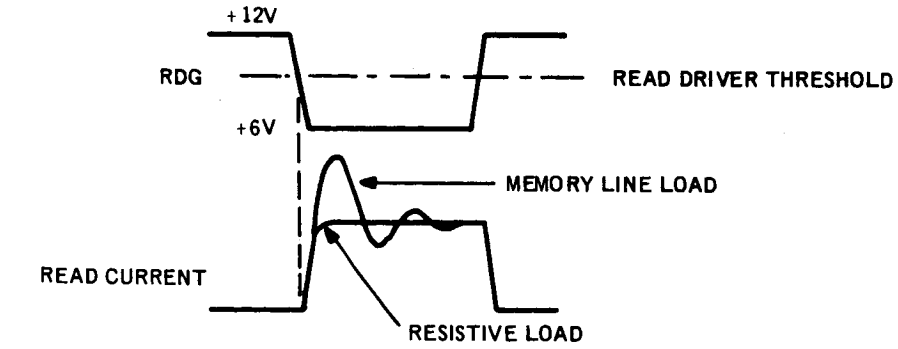
(1) RDG Transfer Characteristics

The RDG is required to translate the 0 to +5 volt IC logic level to the +6 to +12 volt levels required of the selected Read Driver.

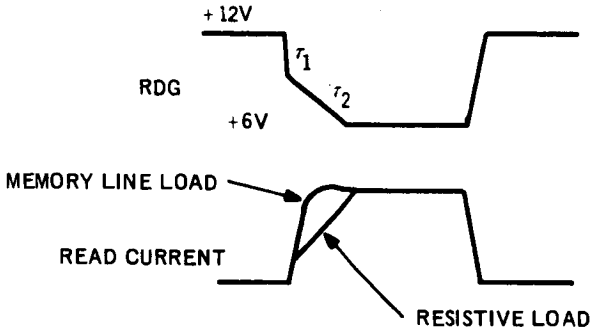
Because of the reactance of the memory word lines, it is necessary to drive the lines with a controlled transition. When a word line is driven with a step input, the resulting word current has a large overshoot on the leading edge. To minimize this overshoot the leading edge of the read current must be slowed down to approximate a ramp input. As noted in the hybrid driver section, the transition of the read current closely follows the transition of the RDG. As the RDG signal falls towards +6 volts, the enabled FET load is turned on at about +9 volts. At this point, the Read Current is determined by the RDG voltage. It is thus possible to control the current rise time by controlling the slope of the RDG signal as it sweeps through the active circuit region of +9 to +6 volts. Figure 40 illustrates the read current waveform for a step and a controlled transition at RDG.

(2) RDG Circuit Design

A preliminary design of the RDG is shown in Figure 41. With the input to the circuit at +5 volts, $Q_1$ is turned on, thereby holding $Q_3$ and $Q_4$ in an off state. The




a. UNCONTROLLED INPUT AT RDG




b. CONTROLLED INPUT AT RDG

Figure 40. Word Line Switching Transients

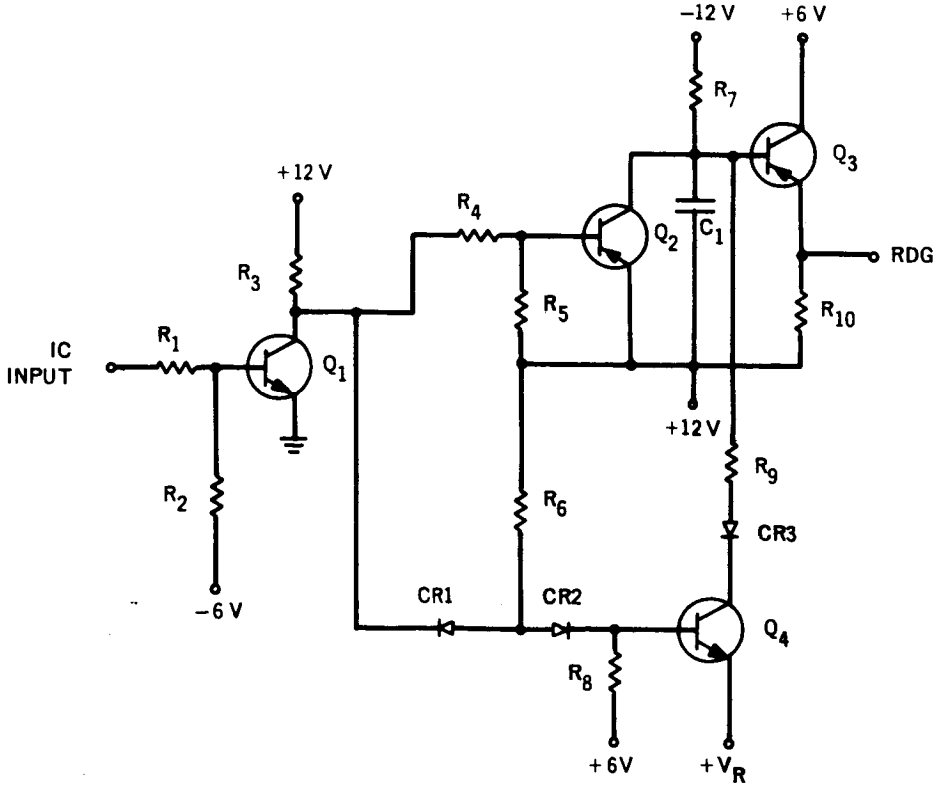



Figure 41. Controlled-Time Strobe Circuit-RDG

output of the RDG is maintained at +12 volts, the off condition for the Read Drivers. The turn-on state is entered by switching the input level from +5 volts to 0 volts. $Q_1$ turns off and the excess base charge is removed via $R_2$. With the turn-off of $Q_1$, $Q_2$ turns off and $Q_4$ turns on via base current injection from $R_6$ and CR2 in series. C1 which was initially uncharged now charges towards $(V_R + V_D + V_{CE})$, with a time constant determined by $R_7$ in parallel with $(R_9 + R_{diode} + R_{sat})$. With $R_7 >> R_9$, the time constant is $\tau_1 \approx C1R_9$. $\tau_1$ is made short to minimize the turn-on delay of the Read Driver.

A second charge path is through $R_7$ and is dominant after C1 has charged to $V_R$. This time constant, $\tau_2 = C1R_7$, is the controlled one which determines the rise time at the output. Charging towards -12 volts, the output circuit, $Q_3$, clamps the final signal at $(+6V + V_{CE(sat)})$. Due to the -12 volt charge goal the resultant signal is more linear than had the +6 volt supply been used as the charge source voltage.

In the circuit shown, $R_7$ was set at 10K, while the fast charge resistance was approximately 500 Ω. Hence, a 20/1 ratio of time constants, $\tau_1/\tau_2$, was achieved.

c. Read Switch Gate (RSG)
POS DD Gate (PDDG)

Both the RSG and the PDDG are required to interface IC logic modules and memory driver circuitry. Both circuits are required to produce a +12 to +6 volt output swing. The function of each circuit is similar to that of the RDG circuit driving a bank of P-type FET switches and producing a voltage reference for the respective hybrid drivers.

The reactive loading on the driver circuitry is not critical during the write cycle, (PDDG), and is not present during word switch turn-on (RSG). The circuits must therefor switch with minimum delay and transition time.

## E. SENSE AMPLIFIER INVESTIGATION

### 1. Requirements

The sense amplifier design requirements were based on several system design criteria and material constraints. System design criteria include: memory organization, available power supply voltages, power budget, memory capacity, speed of operation, system noise, and packaging configuration. Material constraints include: line impedance, temperature variation of output signals, drive requirements, worst-case minimum and maximum signal levels, signal attenuation, properties, line propagation delays, line series losses, and output waveform frequency components.

Detailed system design criteria are given in Statement of Work L-6645, dated May 5, 1967. The material constraints are to be found in section IIA of this report. The resultant input signal used as the basis of the amplifier design is shown in Figure 42. This signal is based on the use of Type 47 material. The amplifier to be described in this report will also be capable of operating with a shorter and larger amplitude signal input (±2 mv for 50ns) which approximates the worst-case output of type 3515 material. Amplification of the short input signal puts a wide bandwidth requirement on the sense amplifier. For example, a cosine-squared pulse of 50 nanoseconds duration has a useable harmonic content out to 40 MHz.

An additional major design requirement of the amplifier is common-mode rejection (CMR). The sense amplifier with a two-crossovers-per-bit input signal has to have

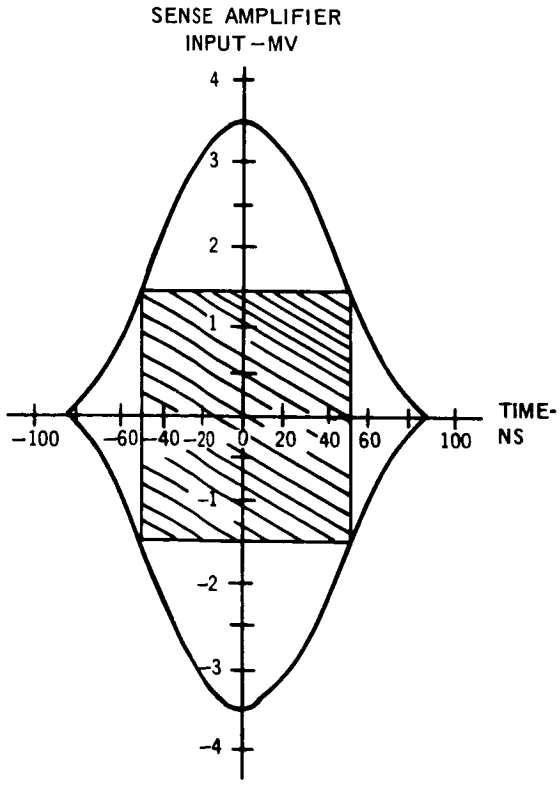



Figure 42. Minimum Sense Amplifier Input Signal

an excellent CMR versus frequency characteristic to output noise generation. This requirement is important due to the low threshold of the amplifiers, required by the low valid signal levels.

The maximum input differential voltage characteristic of the amplifier is an important design consideration as it strongly affects the maximum bit line length due to the IR drop during digiting.

The amplifier input impedance is also a significant design parameter. If the input impedance is high during the read operation, and the sense line is not loaded, in-phase reflections of the signal will result. If the input impedance is loaded to eliminate reflections, significant energy losses will accrue during digiting. For the purposes of this program the high input impedance state was chosen. The reflection problem was minimized through careful strobing of the data output signal.

## 2. Approaches Considered and Final Unit Design

The ideal solution to the sense amplifier circuit problem is to implement the circuit with a single low powered monolithic amplifier unit. After a careful search of the literature of both commercial and developmental units, it was found that no single unit capable of meeting the device requirements was available. With this finding, several generalized design approaches had to be evaluated. These approaches include:

(1) The design of a special unit for this program, in either discrete or hybrid form.

(2) The design of a special pre-amplifier to be used in conjunction with a commercial sense amplifier, in either discrete or hybrid form.

(3) The use of a monolithic pre-amplifier to be combined with a monolithic sense amplifier, to be used as two separate packages, or combined together in a hybrid package.

The first approach was considered impractical because of both time and cost. The second approach was considered to be advantageous if the pre-amplifier requirements were simple. As the circuit evolved, the pre-amplifier requirements became more stringent and therefore the third approach was adopted.

The amplifier unit selected was the Fairchild $\mu$A710. This unit was chosen because of its low input offset voltage (.6 mv typ), high voltage gain (1700 typ), fast response time (40 ns typ), and moderate power consumption (90 mw). Several other factors led to this choice, among them good reliability, multiple sources, and moderate cost.

An evaluation of applicable pre-amplifier units led to the possible selection of the RCA type CA3001 and the Motorola type MC1510 video amplifier. The latter device is also manufactured by Texas Instruments as their type SN5510 video amplifier.

The first sense amplifier design employed the CA3001 as the pre-amplifier. The CA3001 contains a Darlington-arranged differential input stage. This makes possible the application of a ±9V differential input voltage. For long terminated word lines, where the voltage drop in the line and termination is large during the digiting operation, a large voltage appears directly across the amplifier inputs. As an example, a 4096 word line of Type 47 material with a 100Ω termination will have a voltage drop of 4.2 volts across it when driven with a 20 mil digit current. When organized in a two crossover per bit mode, the resultant voltage across the amplifier will be 8.4 volts.

The CA3001 has a minimum double ended voltage gain of 22 db at 1.75 MHz and a common mode rejection (CMR) of 46 db at 2.0 MHz. The amplifier bandwidth is 16 MHz. The amplifier has an AGC input terminal which permits strobing of the output signal.

The first sense amplifier, designed around the CA3001 and μA710, is shown in Figure 43. Capacity coupling is employed at the output to eliminate effects of the pre-amplifier DC offset. A negative AGC gate pulse is employed to gate the pre-amplifier off during the digit signal as illustrated by the timing waveforms in Figure 44. This prevents a large transient from occurring on the output due to the digit pulse saturating the pre-amplifier. A small transient due to the difference in the quiescent DC voltage level of the two output terminals still results from the gating of the output with the AGC pulse. An RC time constant of 300 ns is, therefore, used in the coupling network so that it can recover from the transient in time to begin the next timing cycle. This sets the low frequency cutoff of the amplifier at 530 KHz which is still adequate to pass the sense signal.

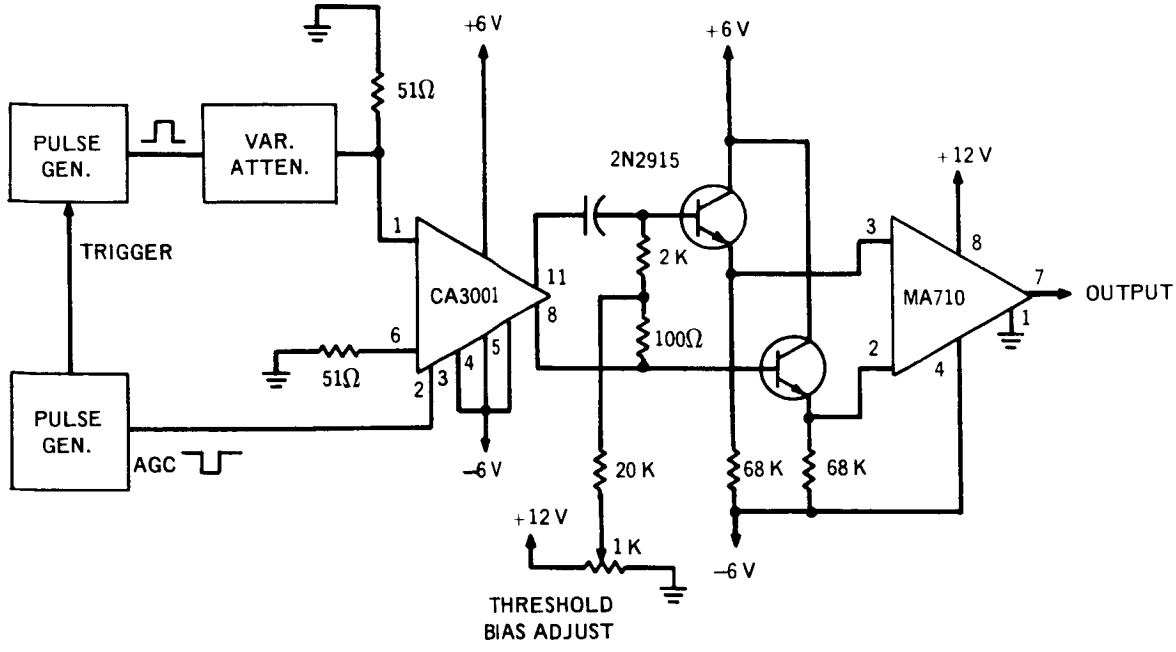



Figure 43. Sense Amplifier Using CA3001, and Test Setup

The output impedance at each of the CA3001 outputs is typically 75 ohms. In order to maintain the sense signal amplitude as high as possible, the AC load on the CA3001 should be at least ten times the total output impedance, or greater than 1500 ohms. The μA710 input offset current, over the required temperature range, changes enough that the manufacturer will not guarantee meeting the offset voltage specification if the source DC resistance at either input exceeds 200 ohms. The bias circuit shown in Figure 43 coupling a bias current into the μA710 must satisfy both the CA3001 maximum loading requirement and the μA710 maximum source resistance requirement, and this cannot be accomplished without an impedance buffer. A matched pair of emitter followers is used to provide this impedance buffering with no loss in signal.

The type 2N2915 transistor is well suited for this purpose because the VBE drop of the pair is matched to within 3mv at a collector current of 100 na and because the transistors both have high matched betas at that same current. Due to the tolerance buildup of the DC offset voltage in the μA710 and the 2N2915, and due to the limited input signal and gain of the CA3001 amplifier, a threshold bias adjustment is required to compensate for these variations from unit to unit. In production units, the bias potentiometer shown in the test circuit would be replaced by a trim resistor. All or part of the circuit can then be packaged in a hybrid circuit so that the trim resistor is integral with the μA710 and 2N2915.

Although the circuit outlined above will meet the overall design requirements, the selection of a trim resistor, the use of a matched pair of transistors and the necessity of incorporating all these elements in a hybrid circuit can be avoided if sufficient

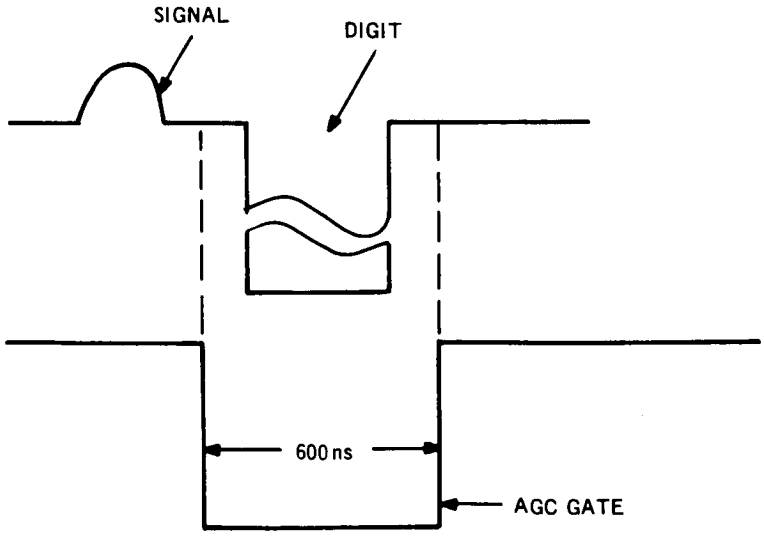



Figure 44. Timing of Signal, Digit and AGC Pulses

gain is available from the preamplifier to overcome the offset voltage tolerance buildup. The Motorola type MC1510 had, therefore, been investigated. It has a minimum gain of 37db and a bandwidth of 40 MHz, but it does not contain a Darlington input stage. Consequently, the maximum allowable differential input signal for the digit pulse is 6 volts, which was initially below the sense amplifier requirements.

During the study program, the maximum usable digit line length was shown to be 2048 words, and the use of terminations on the digit line was shown to be unnecessary.

This resulted in a reduction of the maximum differential input voltage requirement from 9 volts to 5 volts, permitting the use of the MC1510 amplifier as a preamplifier with the μA710 comparator.

The Motorola type MC1510 was evaluated using the test circuit illustrated in Figure 45. The coupling network impedance is smaller than in the CA3001 test circuit in Figure 43 so that the emitter followers are eliminated. Due to the higher gain of the MC1510 a fixed offset bias can be used on all units by setting the threshold level high enough to overcome the tolerance buildup of offset voltage from unit to unit. This is verified in the analysis that follows.

The factors which determine the threshold bias level under varying conditions can be explained with the aid of Figure 46, "Signal Threshold Bias Conditions for a μA710 Comparator". This figure shows the effective offset voltage tolerance spread of the

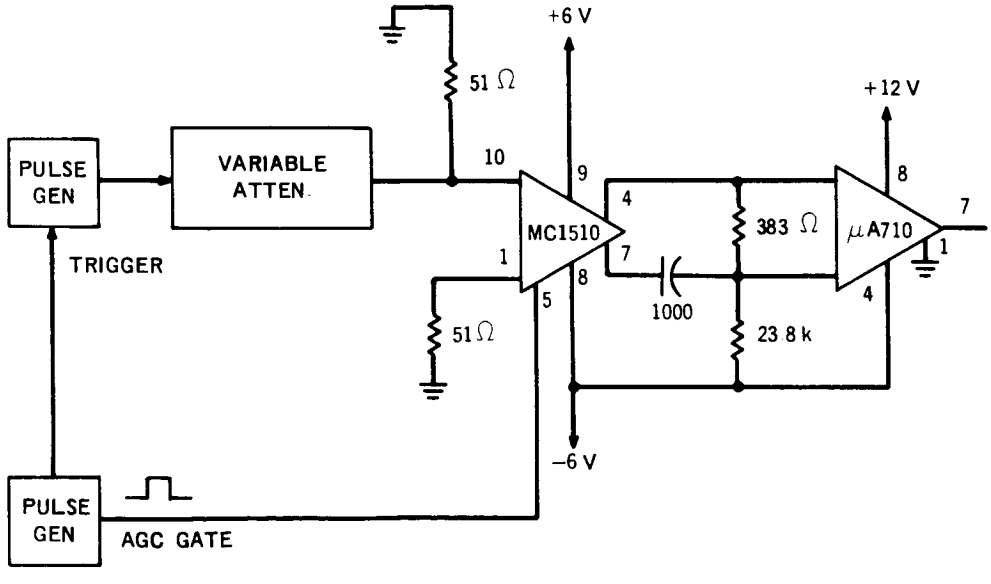



Figure 45. Test Circuit for MC1510 Preamplifier

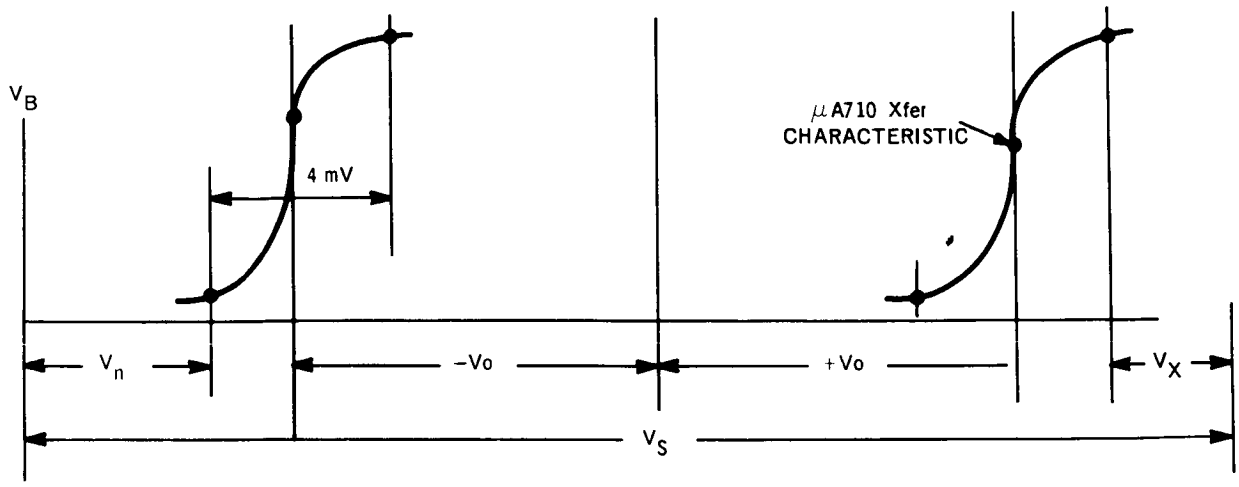



Figure 46. Signal Threshold Bias Condition for μA710 Comparator

transfer characteristic for the Fairchild type μA710 comparator. Two inequalities relating the threshold bias voltage ($V_B$), the signal voltage ($V_S$), and the noise voltage ($V_N$) to the effective amplifier gain (K), the offset voltage (VO), and the μA710 sensitivity and over-drive voltage $V_X$ can be written as follows:

$$V_B + V_S \text{ K min.} \geq Vo + V_X + 2 \qquad \text{(All voltages are in mv.)}$$

$$V_B + V_n \text{ K max.} \leq -Vo - 2$$

These two inequalities specify all the conditions that must be met simultaneously under all operating extremes to obtain satisfactory performance. With the exception of $V_B$, all the variables in these two equations can be determined independently.

The value of K max. and K min. can be found by referring to the specification control data sheet of the MC1510.

The effective gain is the product of the initial gain (Ko) of the unit, its variation with temperature $K_T$ and the loading factor $K_L$. The min-max values of $K_O$ and $K_T$ are as follows:

$$146 < K_O < 220$$

$$0.85 < K_T < 1.70 \text{ for temperature extremes of } -25°C \text{ to } +85°C$$

The value of $K_L$ is determined by the load impedance ($R_L$) and the output impedance ($R_O$) of the amplifier. The defining equation is:

$$K_L = \frac{R_L}{2 R_O + R_L}$$

$$R_O \text{ max} \cong 53\,\Omega$$

The load impedance ($R_L$) is assumed to have a 1% initial tolerance and a 1% change at end of life so that the minimum load impedance is:

$$R_L \text{ min.} = 0.98 \times 383 = 375 \text{ ohms}$$

Therefore,

$$K_L \text{ min.} = \frac{R_{L \text{ min.}}}{2 R_O \text{ max.} + R_L \text{ min.}}$$

$$= \frac{375}{2 \times 53 + 375} = 0.78 \text{ and}$$

$$K \text{ min.} = Ko_{min} K_{Tmin} K_{Lmin} = 146 \times 0.85 \times 0.78 = 96.5$$

The maximum value of $K_L$ approaches one when $R_O$ is at its minimum value.

$$K \text{ max.} \approx Ko \text{ max. } K_T \text{ max.} = 220 \times 1.07 = 236$$

The offset voltage tolerance buildup ($V_O$) includes the following factors:

Offset voltage tolerance of the uA710 = ±3mv

Coupling network impedance variation effect = ±2.9mv

Power supply variation effect = ±1.5mv

Variation due to DC shift of preamplifier output = ± 7.2mv

Offset due to incomplete AGC transient recovery = ±22mv

The offset voltage tolerance of the uA710 is ±3mv as specified in the data sheet. Assuming a 2% variation in coupling network impedance, a 1% variation in the power supply and on initial threshold bias $V_B$ = 145mv, the tolerance for each is:

$$\pm 0.02 \times 145 = \pm 2.9\text{mv coupling network}$$

$$\pm 0.01 \times 145 = \pm 1.5\text{mv power supply}$$

The maximum variation of the DC level of the MC1510 output is + 2.6 to + 3.5VDC from the data sheet and the bias resistor is tied to -6VDC so that the max. shift is

$$\frac{(3.5 - 2.6)}{(3 + 6)} \times \frac{V_B}{2} = \frac{0.9}{9} \times \frac{145}{2} = \pm 7.2\text{mv}$$

An AGC gate pulse is applied to terminal #5 of the MC1510 to turn off the output emitter followers during the digit pulse to minimize the transient in the output and the subsequent recovery time. A small transient, however, is still present due to the difference in the DC operating point of the two output terminals. This is manifested in a voltage ($V_D$) which is the difference in the positive swing of one output with respect to the other during the AGC gate pulse period. As noted earlier, this voltage varies from 3.5 to 2.6V so that

$$V_D = 3.5 - 2.6 = 0.9 \text{ volts}$$

Due to the RC coupling, two transients result as illustrated in Figure 48, one beginning at t = 0 and the other at t = 600ns. During the AGC gate pulse period the output emitter followers of the MC1510 are cut off, as can be seen in the schematic of the MC1510 output stage and the coupling network as illustrated in Figure 47.

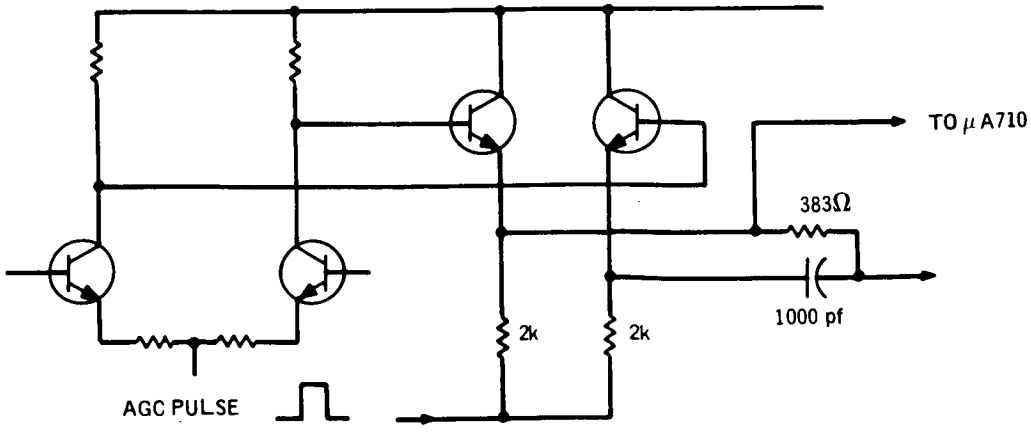



Figure 47. MC1510 Output State and Coupling Network

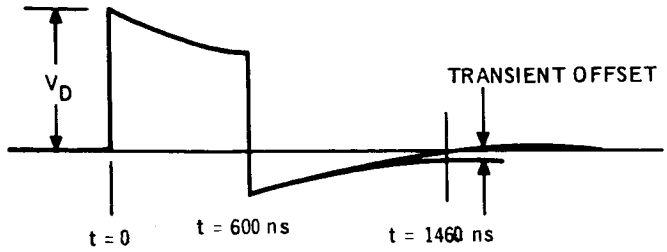



Figure 48. AGC Transient Recovery

The two 2K resistors in the emitters of the output stage therefore form a part of the total resistance in the RC time constant during the first transient. Thus,

$$RC = (2K + 2K = 383) \times 10^{-9} = 4.383 \times 10^{-6} \text{ sec.}$$

The maximum drop in the output is then

$$V_D (1 - e - \frac{t}{RC}) = 0.9 (1 - e - \frac{600}{4.383}) = 0.115 \text{ volt}$$

At t = 600ns, the AGC gate goes negative and the emitter followers are turned back on so that the maximum effective RC time constant is now

$$(2 \text{ Ro} + R_L) \text{ C} = (2 \times 53 + 383) \times 10^{-9} = 483 \times 10^{-9} \text{ ns}$$

where Ro is the maximum output impedance of the emitter followers. The offset of the output from the steady state value at t = 1.4 useconds is then

$$.115 \text{ e } \frac{-t}{RC} = .115 \text{ x e } \frac{-800}{483} = 22\text{mv}$$

The total offset voltage tolerance buildup (Vo) can now be calculated as the RMS value of all the contributing factors.

$$\text{Vo} = \pm \sqrt{3^2 + 2.9^2 + 1.5^2 + 7.2^2 + 2.2^2} = \pm \sqrt{555} = \pm 23.5\text{mv}$$

Since Vo is now known and the noise voltage (Vn) is specified as 1/2 mv, the offset bias ($V_B$) can be determined using the equation

$$V_B + Vn\ K\ max. \leq -Vo - 2$$

$$V_B \leq -0.5 \times 236 - 23.5 - 2$$

$$V_B \leq -143.5mv$$

It should be noted that the value of 145mv used for $V_B$ to calculate Vo is very near to the required value of 143.5mv so that the approximation is valid.

The value of the bias resistor to obtain this offset bias voltage is computed as follows:

$$I = \frac{V_B}{R_L} = \frac{143.5}{383} = .374ma,\ R = \frac{E}{I} = \frac{9}{.374} = 24K$$

The nearest standard 1% value of 23.8K is therfore used.

The minimum input signal ($V_S$) required can now be determined from the equation

$$V_B + V_S\ K\ min \geq Vo + V_X + 2$$

$$-143.5 + 96.5\ V_S \geq 23.5 + 5 + 2$$

$$V_S \geq \frac{23.5 + 5 + 2 + 143.5}{96.5} = 1.74mv$$

In this calculation, a signal overdrive ($V_X$) of 5mv is used to ensure adequate rise time of the output pulse from the uA710 comparator.

From the foregoing analysis of the MC1510 preamplifier, it may be concluded that this design offers a simpler and more cost effective design than that of the CA3001 preamplifier. The sense amplifier circuit of Figure 45 is recommended.

Temperature tests were performed on this circuit to check for gain variation in the preamp and for offset voltage drift in the uA710 comparator. No appreciable change was noted in either gain or offset from +25° to -25°C. At a temperature of +85°C, the gain of the preamplifier dropped approximately 10%, but no offset bias variation was noted.

3. Power Switching

The recommended sense amplifier consists of an MC1510 preamp stage AC coupled to a uA710 amplifier. The amplifier uses three different power supply voltages. A study was made to determine:

(i) the most feasible supply(s) to switch,

(ii) the response time of the sense amplifier to power turn on, and

(iii) the transient problem of delivering full power to the sense amplifier terminals.

a. +6 Volt Power Switch

The +6 volt supply powers only the MC1510. An analysis of this circuit shows that a reduction of this supply level below digit line voltage levels (+4V) will cause digit current to flow into the MC1510 input terminals. An open circuit on the +6 volt line will produce the same results, i.e., a loss of digit current.

b. +12 Volt Power Switch

The +12 volt supply powers only the μA710. This supply could be reduced without any adverse effects at the input terminals.

c. -6 Volt Power Switch

The -6 volt supply powers both the MC1510 and the μA710. Switching this supply level will provide the greatest power reduction with a minimum of disturbance at the input/output terminals. It was found that by reducing the -6 volt level either to zero or to an open circuit, the current drawn from the +12 volt supply was reduced by 65%. The following data was taken to determine the DC power savings with the -6 volt supply in various states:

| | Power Line Current | | | |
|---|---|---|---|---|
| State | +12V | +6V | -6V | Output Level |
| D.C. | 8 ma | 13.5 ma | 16 ma | |
| -6V open | 2.8 ma | 4.1 ma | | +8V |
| -6V to GND | 2.8 ma | 10.0 ma | | +6V |

d. Response to Power Turn On

The following sense amplifier power turn on delays were recorded. Each recorded time indicates the total elapsed time from 90% power to usable output signal. The test setup and waveform definition is shown in Figure 49.

| PWR Line Switches | Delay (Figure 2) |
|---|---|
| +12 Volt line | 1 μs to μA710 Output |
| +6 Volt line | 1 μs to MC1510 Output |
| -6 Volt line | 300 ns to μA710 Output |

e. Power Line Transient

The greatest turn on delay will be due to the filter capacitors local to each sense amplifier. These capacitors are estimated to be 0.01 μf each and must be located at each sense amplifier power terminal to prevent oscillations.

Calculations were made to obtain approximate turn on time for a power line. Assuming one 10 Ω switch and neglecting wiring inductance, the time required to bring power to 98% is about 13 μs. This transient time is reduced to about 10 μs by the inclusion of series wiring inductance (0.8 μh was assumed). The power system is highly overdamped indicating that a switch distribution scheme will reduce the transient time.

f. Power Switching Conclusions

Switching the -6 volt power line reduces the total sense amplifier DC power dissipation by 79%. The amplifier output goes to +8 volts in this mode. Returning the -6 volt line to GND reduces the output level to +6 volts and the DC power dissipation by 66%.

Switching the -6 volt line minimizes the sense amplifier response time and reduces the +12 volt DC current drain by 65%. In view of this, it is not necessary to switch the +12 volt level.

To control transients on the power lines, a scheme will have to be developed to distribute power through several switches. By reducing the capacitive loading in this manner, power can be switched for memory cycle times of 10 μs or more. This time is based on the following assumptions:

1. Large filter capacitors local to each amplifier; (0.01 μf).
2. Switch impedance = 10 Ω.
3. Total amplifier impedance large compared to the switch impedance. (Separate switches for MC1510 and μA710.)

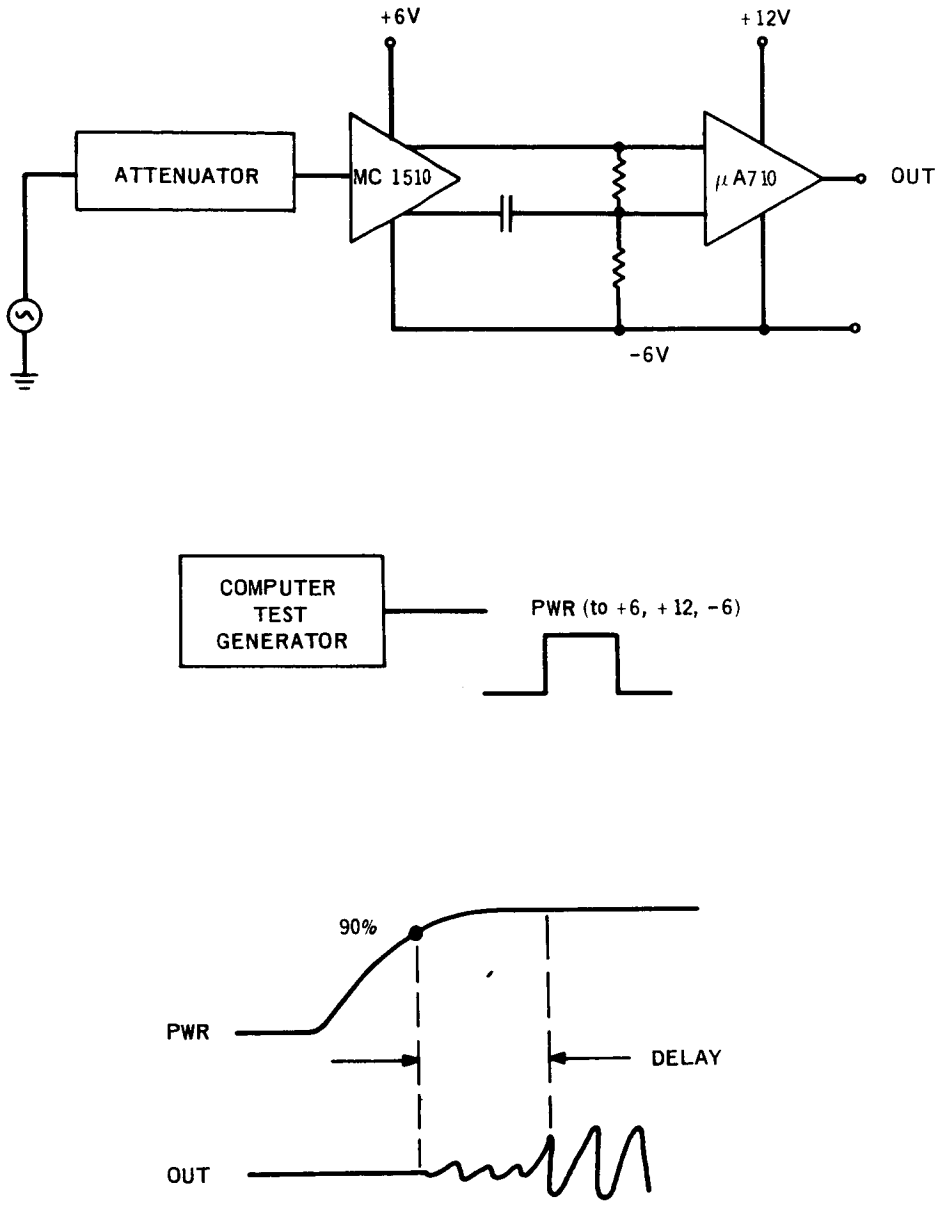



Figure 49. Power Turn-on Test Setup

Reduction of the minimum cycle time to below 10 $\mu$s is probable but cannot be demonstrated at this time. The following tasks would be involved:

1. The design of a low impedance switch ( $\approx 4\ \Omega$ ).
2. Changing the location of the filter capacitors to the power source side of the switch.
3. Reducing the magnitude of the filter capacitors.
4. Proper distribution of switches.

Tasks (1) and (4) are related in the area of minimizing DC power dissipated in the switches. Tasks (2) and (3) are dependent upon the amplifier characteristics.

### 4. Procurement

As previously stated, the sense amplifier unit can be fabricated in either hybrid or discrete form. For the purposes of the subject program with its basic cost and schedule limitations, it was decided to fabricate the unit in a discrete form. Essentially this requires about three times the space that would be used by the hybrid version.

Both amplifiers required for the composite unit have multiple sources, and established production history.

## F. PERIPHERAL CIRCUITS TRADEOFF STUDY

The Laminated Ferrite Memory must operate at the maximum data input/output rate of 500,000 words per second, each memory cycle consisting of a reset and store of externally supplied address and data, a read (or clear) operation and a write (or restore) operation. To meet this goal, experimental data taken on the ferrite wafers indicated that timing increments of 125 nanoseconds would be best for generating the various control signals for memory drivers and switches. An internal 8 MHz oscillator and a logic family capable of operation at this speed are needed. Two logic families considered to be adequate for this task are ECL (emitter coupled logic) and TTL (Transistor-Transistor Logic). ECL was eliminated as a choice due to very high power dissipation and the need for special interface circuits because of negative logic levels. Experimental data also revealed that when a memory bit is read, the sense amplifier output pulse may last only 50 nanoseconds. This information must be stored in a flip-flop stage of a shift register. The use of a high speed TTL device is indicated for this reason also. A pulse stretcher such as a one shot might be considered, but since 32 of these are required for the 32-bit word, the added power requirements for these devices and the inherent susceptibility to noise make the TTL flip-flop a more favorable choice.

An address decode time of 375 nanoseconds has been allotted in the memory cycle time. The use of back to back gates as the storage medium in the address register and two 8x8 matrices to decode 64 switch lines and 64 driver lines requires the address logic that 3 $t_{PD-}$ + 2 $t_{PD+} \leq 325$ nanoseconds (where 50 nanoseconds has been allowed for the final stage located in the hybrid switch/driver circuits). $T_{PD-}$ is a gate propagation delay for a negative going output and $T_{PD+}$ is the delay for positive output transitions. This requirement precludes the use of LPDTL devices under worst-case conditions but DTL devices similar to Fairchild FA 930 series might be used. A low power TTL line, (the Texas Instrument 54L series) which has typical average gate power of 1 milliwatt and a maximum propagation delay of 60 nanoseconds, can meet these requirements.

Complementary MOS Devices having very low quiescent power dissipation were also considered for use in the address logic. However, propagation delays are excessive when these devices are powered at a logic level of 6 volts. For example, a typical nominal gate pair delay at 6 volts was measured to be 300 nanoseconds whereas with a 10 volt supply the pair delay was 120 nanoseconds. This is borne out by MOS theoretical equations which predict that Pair Delay $= \frac{K C_L}{\left(1-\frac{V_T}{V}\right)^2}$

where $C_L$ = Load Capacitance, $V_T$ = Threshold Voltage, and V = Supply Voltage.

If used in the memory address logic, these devices would have to be powered by the +12V supply to obtain fast enough operation. This necessitates buffer circuits (and extra power) between these devices, the low level input signals and the remaining logic. When system capacitances are added as loads, propagation delays will be increased. No worst-case data was available to predict maximum delays. A further disadvantage of the only available C-Mos gate package, the RCA TA5361, is that it is a developmental type. Since only one packaging configuration is offered, the number of modules required is 119 for address decoding alone as compared to 60 modules with TTL or DTL configurations. The most promising outlook for C-MOS devices at high speeds lies in large arrays rather than individual gate or flip-flop modules. In the array, capacitances can be kept to a minimum. The channel impedance of the device is in the area of 2 to 4 K ohms, and it is the external capacitances which limit useful operating speed. In terms of interconnections and interface wiring, the address logic presents the most difficult packaging problem in the logic. An excellent approach to this problem makes use of a 1 of 8 decoder device currently available in the Fairchild TTL family. Using these decoders reduces the number of interface wires from logic to memory stack from 128 to 22 and reduces the number of hard wire interconnections from 384 to 70. The number of modules for decoding is 27 as compared with 60 modules for conventional schemes. The price paid for this packing density is in power; about 2.9 watts compared to the lowest possible power of about 200 milliwatts. A possible means of reducing all logic power by 19% is to reduce to the logic supply voltage from 5 volts to 4.5 volts. A further reduction to 4.0 volts will reduce power by 36%.

Having set the requirements for the major sections of the logic, it remains to select a specific integrated circuit family of logic elements. Most of the TTL logic currently available from various manufacturers uses the same basic circuit. The product lines of two manufacturers, Fairchild and Signetics, were evaluated for possible use in the memory system. The Fairchild TTL series is quite versatile and offers many types of logic modules. Among these are multi-function devices such as dual flip-flops, a 1 of 8 decoder and a 4 stage shift register which has all outputs available as well as serial and parallel entry provisions. These help to reduce total module count and number of external connections for assembly. The Signetics series also offers a good selection of module types including dual flip-flop packages. In addition, a lower power TTL series is also available so that in many areas, where an increase in propagation delay can be tolerated, gate power can be reduced from a typical 15 mW to 8 mW. A dual flip-flop package contains 2 AC-coupled flip-flops which combine high-speed operation (counting rates to 25 MHz) with power dissipation of 45 mW, typical, compared to the 75 mW power of the Fairchild master-slave flip-flop. Texas Instruments has a TTL line which offers 3 series differing in their speed/power characteristics. The high and medium power versions are similar to the devices already discussed. Their unique feature is a low power series, 54L, which no others are manufacturing. The power is very low at 1 mW per gate and 4 mW per flip-flop, typically, for propagation delay of 60 nanoseconds, maximum, and counting rate to 2.5 MHz. The packaging concept for the logic uses dual-in-line packages and the 54L is only available in flat packs. This, coupled with the fact that speed limitation restricts use to only the address logic, made this series an undesirable choice in a memory system designed for a 2 microsecond cycle time. From a cost standpoint, a single low power flip-flop is $25 compared to $7.70 for a dual flip-flop package in the medium power range and a low power gate is $15 compared to $3.30 for a standard Signetics gate.

Several systems were tabulated to compare power, module count and cost. All systems except one are capable of the required 2 microsecond memory cycle time. Cost figures are based only on the actual module costs and an estimated assembly cost to assemble an engineering breadboard exclusive of engineering or debugging time. Included in the tabulation is a system composed entirely of the low power T154L series for comparison. This system, however, would be feasible only if the memory cycle time could be increased to 4 microseconds. Not included in this estimate, but necessary for operation, is a means for stretching the sense amplifier output pulse from 50 nanoseconds to at least 100 nanoseconds so that the low power flip-flop may respond. The 32 pulse stretchers will add some additional power and circuit requirements to that shown.

| | TTL Logic Type | Modules | Logic Power | Cost | Cycle |
|---|---|---|---|---|---|
| A. | FA9000, 9300 | 93 | 7.4 W | $1800 | 2 |
| B. | SIG 8400, 8800 | 128 | 5.9 W | 1800 | 2 |
| C. | SIG 8800, T154L | 128 | 4.0 W | 3000 | 2 |
| D. | TI 54L | 143 | 1.0 W | 4700 | 4 $\mu$s |

Systems "A" and "B" consist entirely of dual-in-line packages (DIP), System "C" is a mixture of DIP and flat packs, and system "D" contains only flat packs. The optimum system from a packaging and cost standpoint is system "A" which contains at least 350 less interconnection wires than the other systems. The optimum system with respect to power is system "D" if one is willing to slow the maximum operating speed to 250,000 words per second. System "C" represents a compromise which features a power reduction while maintaining the maximum operating speed of 500,000 words per second.

The logic power represents only a portion of total memory system power. A breakdown of the estimated power requirements for the various memory driver circuits is as follows:

| | | |
|---|---|---|
| A. | Digit Drivers | (64 DR) x (20 ma/DR) x (12V) x (Duty Cycle) = (15.36 W) x DC |
| B. | Write Driver | (120 mA) x (18 V) x DC = (2.16 W) x DC |
| C. | Read Driver | (210 mA) x (18 V) x DC = (3.78 W) x DC |
| D. | Sense Amplifiers | (32 Ampl) x (280 mW/Ampl) x DC = (8.96 W) x DC |
| E. | Miscellaneous | 1 W |
| F. | Logic | 1 - 7.5 W (Depending on final speed/packaging-considerations) |

The duty cycles of the digit, read, and write drivers bring their average power dissipation down to reasonable levels, but the sense amplifier power represents a steady state loss of almost 9 watts while the useful time of the amplifier represents less than 20% of the memory cycle time. Therefore, switching of the power to the sense amplifiers is a possible approach to power reduction. The switching and amplifier transient recovery time make this technique unuseable with a 2 microsecond cycle time. A separate study was made of sense amplifier switching and preliminary results indicate that a cycle time of approximately 10 microseconds is necessary for this technique to be feasible.

Figure 50 depicts the total estimated average memory system power (not including conversion efficiency) versus memory cycle time for the several logic configurations and for the case of switched sense amplifiers.

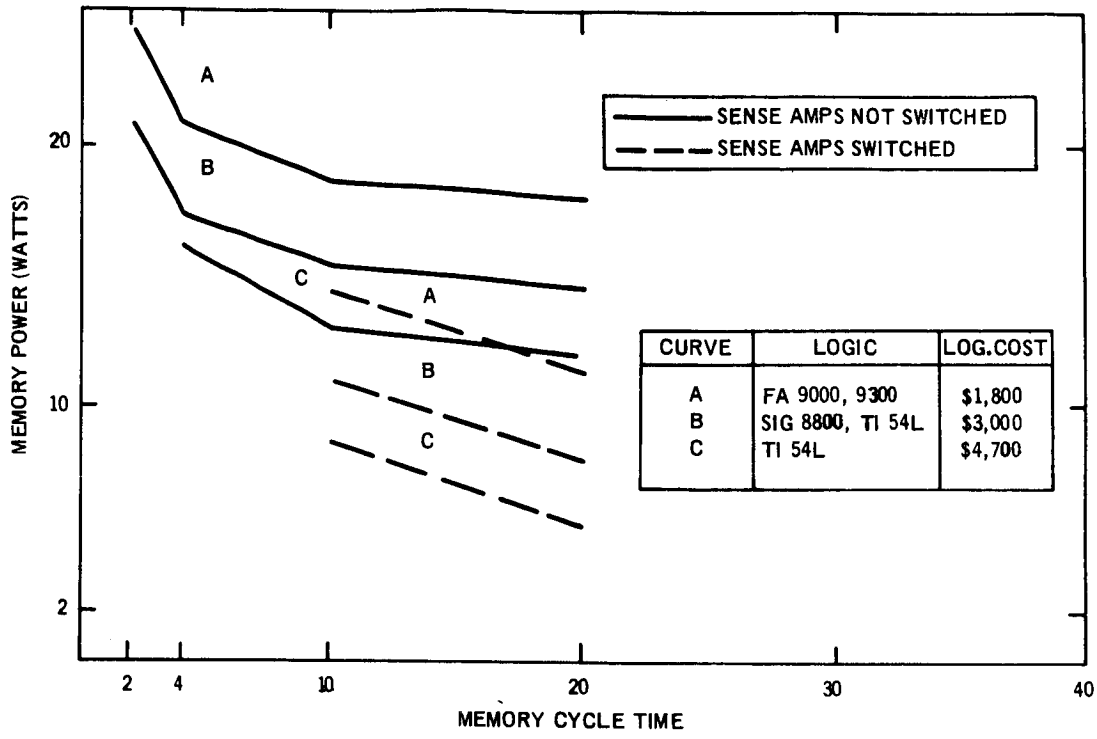



Figure 50. Memory Logic Power-Speed Tradeoff Diagram

## G. PRELIMINARY LOGIC DESIGN

A preliminary logic design for the memory system has been completed. This design is capable of meeting the design goals given in Statement of Work L 6645 dated May 5, 1967, with the exception of total power dissipation. Operating speed and power dissipation are both determined by the choice of logic element, and, as was reported in Section F, Peripheral Circuits Tradeoff Study, an alternate design is feasible using slower, but lower power circuits. The general logic design concept presented in this section is also applicable to the lower power design.

Figure 51 is a block diagram of the complete logic system.

### 1. Input-Output Requirements

All signal inputs and outputs will be binary in nature. A high level of +4.5±1 volts corresponds to a logical "1" and a low level of 0 to 0.3 volts corresponds to a logical "0".

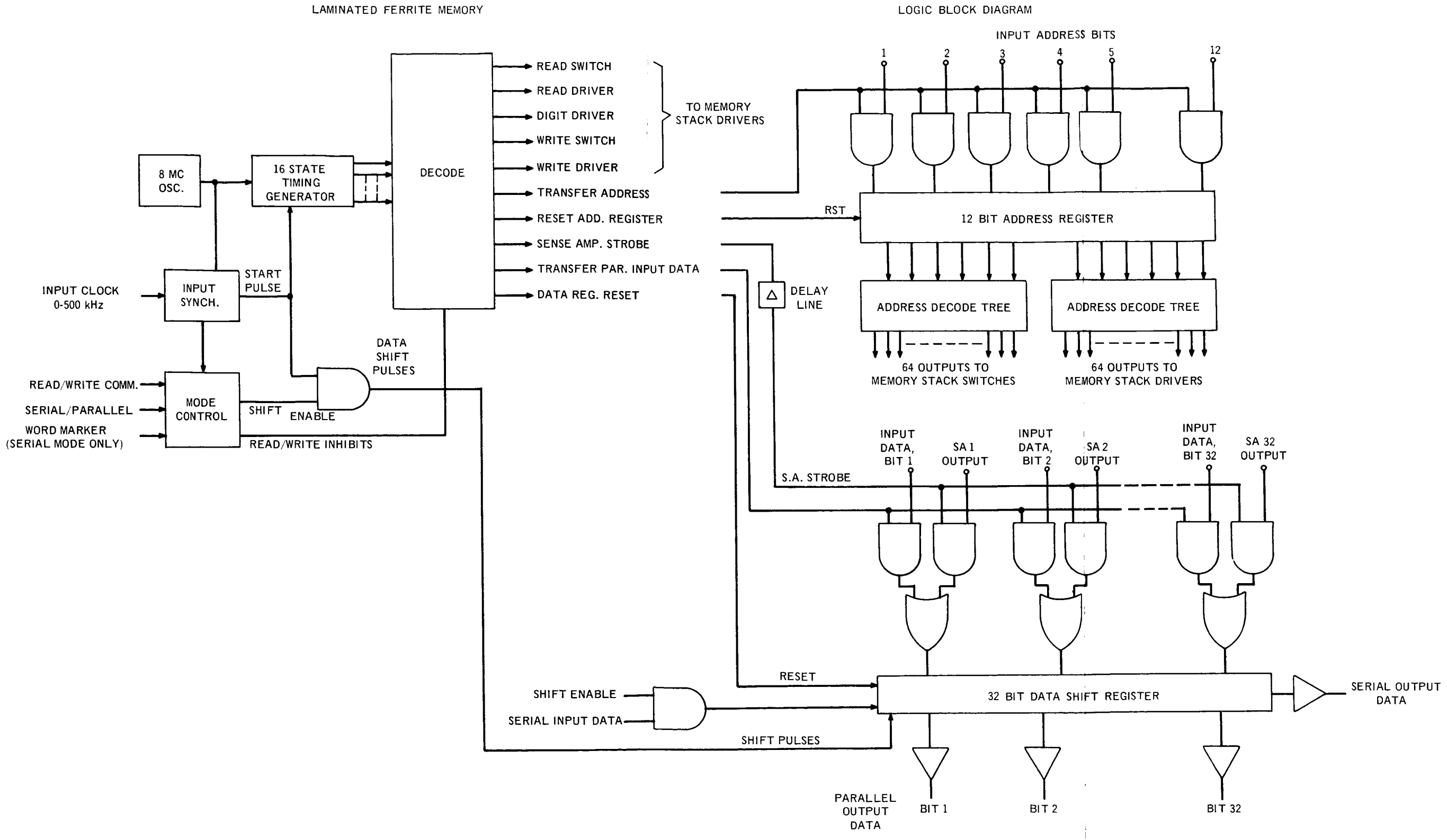



Figure 51. Memory System Logic Block Diagram

a. Inputs

(1) Serial/Parallel Format Command

A logical "1" on this input will indicate serial operation and a logical "0" will indicate parallel operation.

(2) Read/Write Mode

A logical "1" on this input will indicate a read-restore operation and a logical "0" will indicate a clear-write operation.

(3) Word Address

The address input will consist of 12 binary coded parallel input lines which will be used to select one of 4096 word locations in the memory.

(4) Parallel Data

The parallel data will consist of 32 parallel input lines each of which will correspond to a single bit of the 32 bit word. A logical "1" on any input will cause a data 1 to be stored in the selected address for that bit. The parallel data input word rate will be determined by the input clock.

(5) Serial Data

The serial data will consist of a single input line which will provide a serial bit stream in NRZ format with the least-significant-bit (LSB) occurring first. The LSB of each input word is identified as the bit which occurs at the same time that a serial Word Marker bit is present. A logical "1" on this input will cause a data 1 to be stored in the selected address in the appropriate bit position. The serial input bit rate will be determined by the input clock.

(6) Clock

The input clock will be a square wave having frequency from 1 to 500 KHz. This frequency will determine the parallel input/output data word rate when parallel format is commanded and will determine the serial input/output data bit rate when serial format is commanded. The leading edge of this signal (positive transition) will be in synchronism with all other changing input signals. These signals must be settled within 100 nanoseconds of the positive clock transition and must remain stable for a minimum of 1.6 microseconds thereafter.

(7) Word Marker

This signal will be present when serial format is commanded by the Serial/ Parallel Format command input. This marker will indicate the start of a serial word and will be present for one bit period which will correspond to the LSB of the word.

b. Outputs

(1) Parallel Data Output

The parallel data output will consist of 32 parallel output lines each of which will correspond to a single bit of a 32 bit word. A logical "1" on any output will indicate that a data 1 has been read from that bit position of the word stored in the selected address.

(2) Serial Data Output

This is a single output line which will provide the selected word data in serial NRZ format with the LSB occurring first whenever serial operation has been commanded. The location of the LSB will be indicated by the simultaneous occurrence of the Word Marker input and the Access signal output.

(3) Access Time

The presence of a logical "1" on this output line will indicate that valid information is present on either the parallel or serial data output lines depending on the format commanded by the format command. During parallel operation the access time will be 625 nanoseconds.

(4) Address Markers

This output will consist of 4 lines which correspond to memory locations 0, 1024, 2048, and 3072 respectively. The presence of a logical "1" on any of these lines will indicate that the corresponding address is currently being decoded by the address logic.

2. Timing System

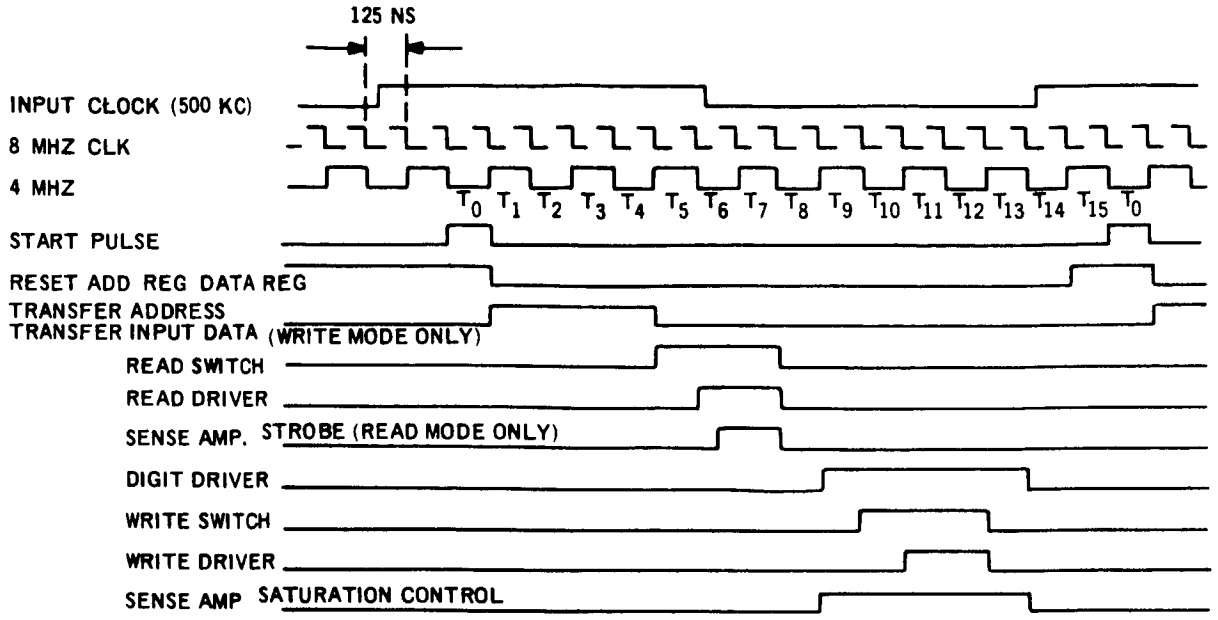
Experimental data taken during the ferrite material investigations and during the development of memory drivers and switches led to the conclusion that a timing system

having a resolution of 125 nanoseconds will be required to step the memory thru a complete cycle. The minimum acceptable pulse width for read and write drivers is 350 nanoseconds, to accomplish memory switching and to allow for ferrite switching delays and propagation delays expected in a 4096 word system. Transients due to switch turn-on require that the associated driver be delayed by at least 100 nanoseconds. Thus, seeking this 125 nanosecond resolution, a basic internal clock frequency of 8 MHz has been chosen. The clock will be a standard crystal oscillator and will be a purchased item. The requirements of the oscillator are: (1) Square wave output compatible for driving a current-sinking logic type such as TTL logic; (2) Power consumption less than 200 milliwatts; and (3) Stability over the temperature range -20°C to +80°C of ±0.005%. Oscillators meeting these requirements are available from a number of suppliers.

At the maximum memory operation speed of 500 K words per second (parallel operation) the memory cycle time is 2 microseconds. The 8 MHz clock will drive a ÷ 16 synchronous counter to provide sixteen 125-nanosecond increments each memory cycle. The logic circuitry to be used must be fast enough to operate with this clock and the decoded outputs of the counter must have minimal propogation delays as well as no spurious output race conditions. To achieve this, a single change synchronous counter scheme will be used, as shown in Figure 51. Logic elements of the TTL family have been chosen for this section of the logic since this offers the best speed/power compromise. A 4-stage Grey code counter was considered for this function but, due to the propagation delays thru the gating logic required, was found to be inadequate at 8 MHz when worst-case propagation delays are considered. An 8-stage Johnson counter (a specific type of shift-register-with-feedback counter) meets the requirements easily. Although inefficient, this circuit offers a unique decoding advantage. A pulse of any desired pulse width from 125 ns to 2000 ns, in 125-ns increments, located at any desired location in the cycle, can be decoded with a simple 2-input gate. Multi-level decoding is eliminated and all outputs have approximately the same delay.

The input clock will be sampled and synchronized to the internal logic clock. The synchronizer will produce a single pulse called a "start" pulse after each input clock leading edge. This logic will also provide some noise rejection on the input clock line by rejecting any spurious inputs on that line lasting less than 250 nanoseconds. The start pulse will be used to initiate the ÷ 16 counter. When the counter has advanced to its final state, a standby condition is reached until a new start pulse is received to initiate another cycle. In this manner the memory cycle repetition rate will be controlled by the input clock while the actual control signals generated for the memory will always be of fixed duration.

The timing signals which must be decoded from the timing generator are as follows (see Figure 52).




NOTES: 1. ABOVE TIMING REPRESENTS REQUIREMENTS FOR MEMORY USING TYPE 3515 MATERIAL AND SWITCHING DIGIT LINES TO REDUCE LINE LENGTH FROM 4096 TO 2048 WORDS
2. TIMING SHOWN FOR PARALLEL OPERATION WITH MAXIMUM FREQUENCY INPUT CLOCK

Figure 52. Memory Timing Diagram

a. Address Register Reset.

b. Data Register Reset.

c. Address Transfer Pulse

Transfer the 12 bit parallel address from the inputs to the address register.

d. Parallel Data Transfer Pulse

Transfer the 32 bit parallel data word from the inputs to the data register when parallel operation is commanded.

e. Read Switch Gate

Turn on one (out of 64 possible) address selected read switch.

f. Read Driver Gate

Turn on one (out of 64 possible) address selected read driver.

g. Digit Driver Gate

Turn on 64 digit drivers.

h. Write Switch Gate

Turn on one (out of 64 possible) address selected write switch.

i. Write Driver Gate

Turn on one (out of 64 possible) address selected write driver.

j. Sense Amplifier Strobe

Transfer the outputs of 32 sense amplifiers into the data register. This signal may be delayed via one or more delay lines in order to compensate for switching and line delays and will sample the amplifier outputs at the maximum sensed signal output.

3. Address Logic (Figure 53)

The memory contains 4096 addresses each of which will store a 32 bit word. Word selection is accomplished by means of a 64 x 64 matrix. There are 64 drivers in the memory and each one drives 64 word lines in the stack. The lines are terminated by electronic switches so that a coincidence of a driver selection and a switch selection results in a unique word address selection in the memory stack. The logic requirement is to provide two 1-out-of-64 decodes from two 6-bit halves of the 12-bit address register.

A 500-nanosecond time slot has been allotted in the memory cycle time for address decoding. An additional constraint imposed is that the external address be stored and completely decoded within this time. Since the interface circuit between the logic and the switch/driver circuits has a possible delay time of 200 nanoseconds, the logic delay must be less than 300 nanoseconds.

The address register only drives a parallel transfer of information from the memory input lines. The best method for this storage, from a standpoint of minimum power dissipation and minimum propagation delays, is use of two gates tied back-to-back to form a simple R-S flip-flop. An additional gate on each stage will perform an "and" function so that the external address may be gated into the register only at a time when the address inputs are in a stable state. A reset bus provides an initial reset of all stages. By doing this only logical 1's need be transferred into the register, saving some hardware.

The fastest propagation time for decoding may be accomplished by using a 6-input NAND Gate since the total delay time will be the register flip-flop delay plus a single gate delay. However, there are several drawbacks to this method. The number of modules required for decoding is 128 while the number of interconnections needed is 768, not including the 128 wires that interface with the memory drivers and switches.

In addition, the fan-out requirement imposed upon each register flip-flop output is 32. An additional quantity of at least 24 drivers would be required and the delay time increased. A scheme which could meet the fan-out requirements is the use of FA930 DTL gates for the register and FA9042 LPDTL series gates for decoding since a FA930 gate

NOTES:

1. ONLY 1/2 OF DECODING IS SHOWN ADDRESS BITS 7–12 ARE DECODED IN THE SAME MANNER.
2. THE LOWER ROW OF 8 MODULES WILL BE MOUNTED AT THE MEMORY STACK THEREBY NECESSITATING ONLY 11 INTERCONNECTIONS BETWEEN THE LOGIC AND THE STACK (TOTAL CONNECTIONS = 22)

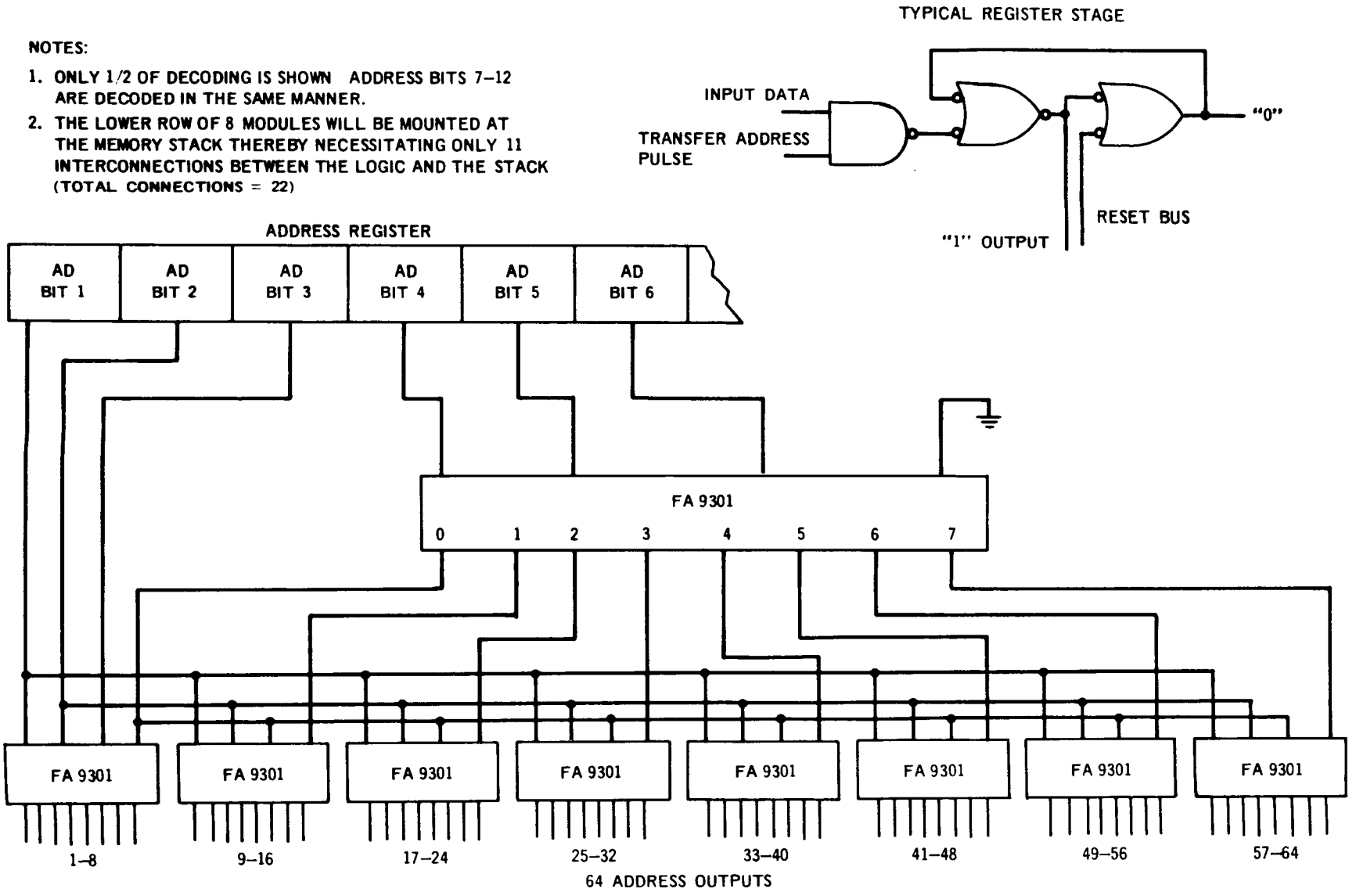



Figure 53. Address Logic

can drive 75 FA9042 gates. Since no 6 input gate exists in that series, it is necessary to use an expandable 4 input gate with diode expanders. This results in an additional 128 interconnections. An alternate solution is the use of T154 series TTL gates for the register and TI54L series low power TTL gates for decoding since a TI54 series gate can drive 40 TI54L series gates and an 8 input gate is available. In general, however, this technique is poor from a packaging and cost viewpoint.

A more efficient decoding scheme for a 1 of 64 decode is the use of an 8 x 8 matrix. (Figure 54) Since the decoding requires 3 levels of logic (including inverters) an additional gate pair delay is added to the total decoding propagation delay. The number of modules required is 51 and the number of interconnections required is 384 exclusive of the 128 interface connections to the memory. The fan-out requirement on each flip-flop output is reduced to 4. This represents a considerable savings in hardware and packaging problems over the previous scheme. The total propagation delay from input address bit to decoded address signal presented to memory driver hybrid circuit input is given by:

$$t_{\text{add delay}} = 3\ t_{PD-} + 3\ t_{PD+}$$

and this address delay must be ≤ 300 nanoseconds. LPDTL and MOS devices were found to be too slow for this application. The lowest power scheme possible uses the TI54L TTL logic elements. The maximum address decode delay is 360 nsec. (typical delay = 200 nsec.) at ambient temperature. An increase of less than 10% can be expected over the temperature range -25°C to +100°C so that these circuits can meet the requirements under typical conditions but not under worst-case conditions. Typical power dissipation is about 180 mw. Delay time can be slightly decreased from 360 to 285 nsec., maximum by using TI54 series gates for the register flip-flops at the cost of an additional 215 mw of power. A moderate power TTL line, the Signetics 8480 series, used in this application will have a maximum decode delay of 175 nsec, with a maximum increase over the temperature range of -25°C to +100°C of 5%. Power dissipation is typically 1.36 watts.

The most efficient decoding scheme from a packaging viewpoint involves the use of a new line of Medium Scale Integration (MSI) devices offered by Fairchild. One of these, the FA9301, is a 1 of 8 decoder and 9 of these modules may be interconnected to form a 1 of 64 decoder. The entire memory decoding can be accomplished with only 18 modules. Using this device a packaging scheme was conceived wherein one decoder module is packaged at the memory stack with each group of 8 drivers or switches. The number of interface wires between the logic and the stack is reduced from 128 to 22 and the number of interconnections required at the logic level is reduced from 384 to 70. The maximum decode delay is 100 nsec. and the power dissipation is 2.96 watts.

1 OF 64 DECODER (2 LEVEL 8x8 MATRIX)
2 REQUIRED FOR 4096 WORD MEMORY

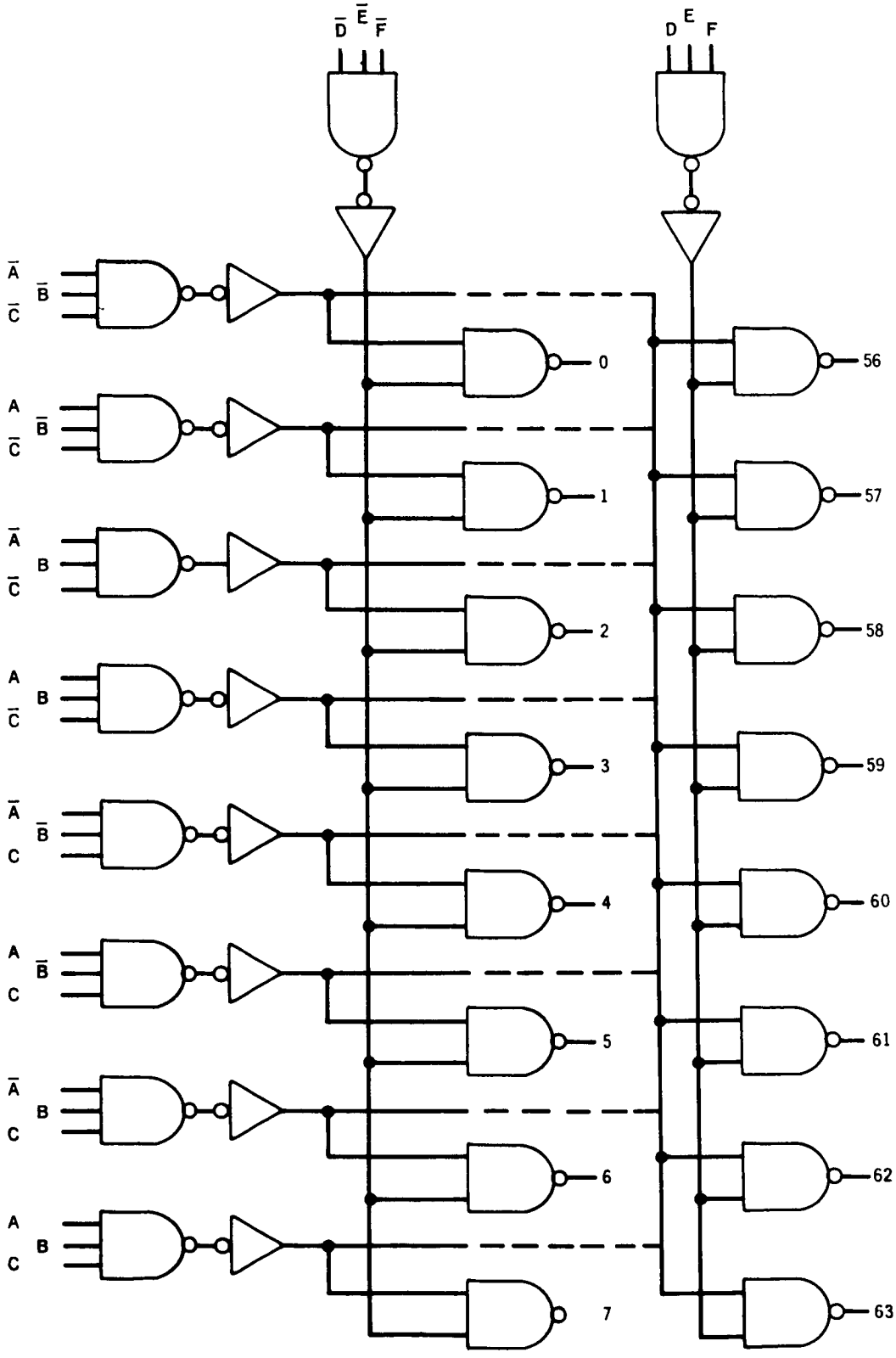



Figure 54. 8 x 8 Decode Matrix

4. Data Path Logic (Figure 55)

Incoming and outgoing memory data will be stored in a 32 stage data register which will accept both parallel and serial input data. The parallel inputs will come from the 32 sense amplifier outputs when the Read Mode is commanded and from the 32 parallel data input lines when the Write Mode and Parallel Format are commanded. The register must shift at 500 KHz so that serial input and output data may be processed. The data register flip-flop must be fast enough to accept a 50 nanosecond pulse on the direct set input of the device, since experimental data on the type 3515 material ferrite wafers has indicated that the sense amplifier outputs for a sensed data bit will have an effective pulse width of only 50 nanoseconds. Medium power TTL devices such as the FA 9022 and the SIG 8827 have this capability. The TI54L series low power flip-flop requires at least a 100-ns pulse to set which then necessitates a pulse stretcher. One such device is the FA 951, a DTL monostable multivibrator available in integrated circuit form. The typical power dissipation is 38 mW which, when added to the typical flip-flop power of 3.8 mW, gives a total power dissipation of approximately 42 mW per stage. The SIG 8827 power dissipation is typically 45 mW. The medium power devices come in packages containing dual flip-flops whereas the low power device is a single flip-flop package and the one-shot is an additional package. Thus, the lower power scheme would save about 100 mW, at the expense of requiring 64 modules as opposed to only 16 modules for the data register.

The two parallel entry paths to each register stage will be implemented by using dual exclusive OR circuit modules. The inputs will be strobed by control signals developed in the timing generator. Input data will be gated in at the same time that address decoding occurs and the sense amplifier outputs are gated in during the read interval.

5. Control Logic

The function of the control logic is to sense the states of the Serial/Parallel Format and Read/Write Mode inputs and to generate control signals which will insure the proper sequence of operations for the operational mode commanded.

When parallel format is commanded a new memory cycle is initiated after receipt of each input clock pulse and during that cycle time a 32-bit parallel word is processed.

In the parallel read mode, the parallel data transfer pulse must be inhibited. Normal read and write signals are transmitted to memory drivers so that the read word is restored to the same memory location.

In the parallel write mode, the sense amplifier strobe pulse must be inhibited. Normal read and write signals are transmitted to memory drivers so that the read operation functions as a clear which precedes the writing of external data into the selected memory location.

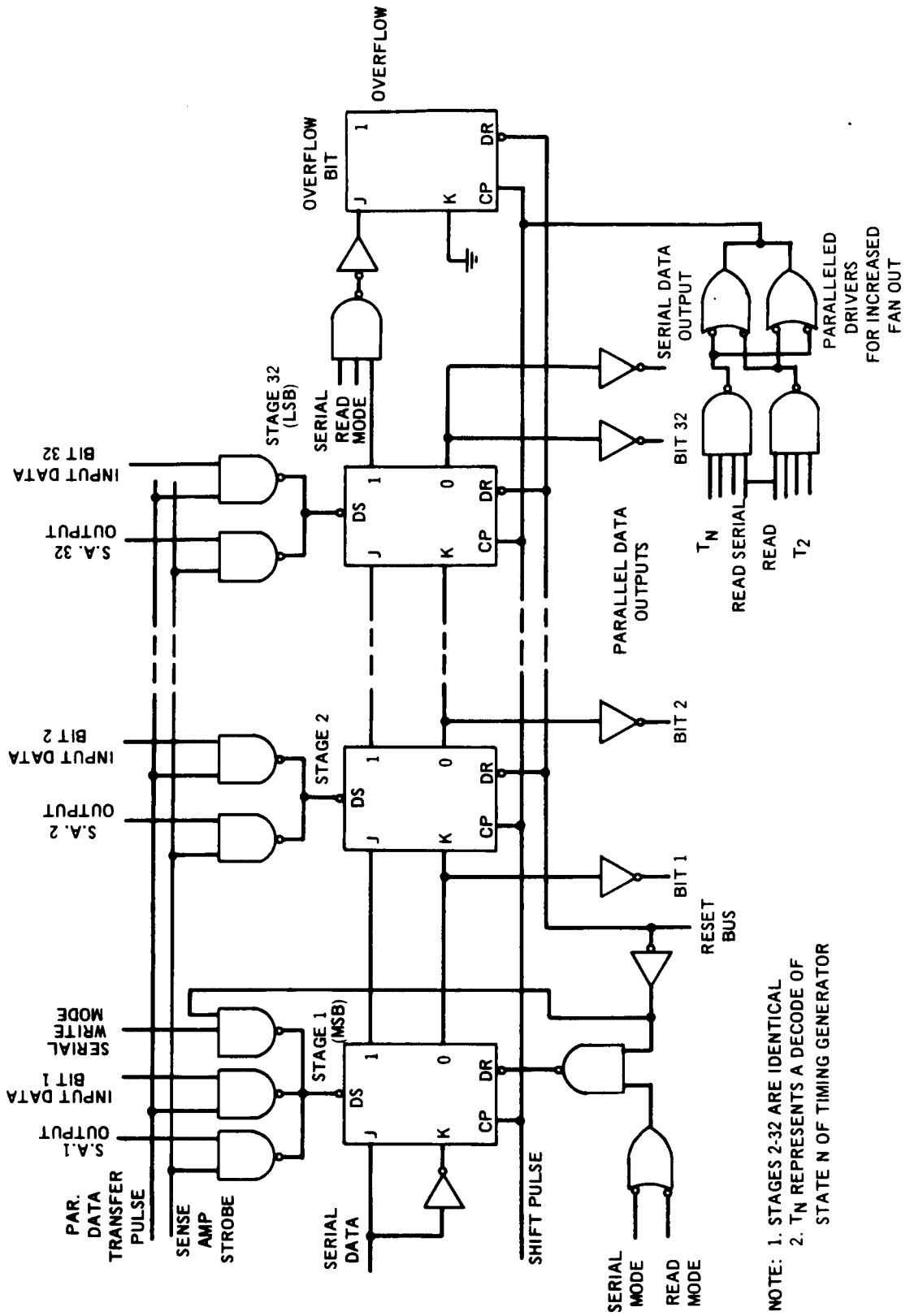



Figure 55. Data Register

When serial format is commanded each memory cycle requires 32 input clock pulses and a word marker pulse.

The control logic will generate shift pulses for the data register and an access time signal at the appropriate times by means of timing signals from the timing generator and the input mode control signal.

When serial read mode is commanded, read and write signals are transmitted to the memory drivers only when the word marker pulse is present. Data register reset is activated only when the word marker is present. After the read period a Shift Enable state is reached and shift pulses are generated during the write period. Since the word marker is present for only one clock pulse, no further writing into the memory occurs after the first restoring write interval. Data access time is indicated during the Shift Enable time. A new word marker bit occurring in conjunction with the input clock causes the next cycle to begin.

When serial write mode is commanded and the word marker pulse is present, registers are reset and the Shift Enable signal is generated. The data register has a "1" preset into the first stage to act as a marker bit for overflow detection. During the read interval, a read signal is transmitted to the memory drivers to clear the selected memory location. In addition, during the read interval shift pulses are generated for the data register. Write signals are inhibited from the memory during the Shift Enable period. When the data register overflow is detected, the write signal is transmitted to the memory drivers and the contents of the data register will be written into the selected memory location. Shifting is then terminated until the next word marker is received when the above sequence is repeated.

## SUMMARY OF INTEGRATED CIRCUIT PARAMETERS

### A. FLIP FLOPS

| NO. | TYPE | POWER (MW.) | | f, MIN. (MHz) | MAX. PROPAGATION DELAYS IN NANOSECONDS | |
|---|---|---|---|---|---|---|
| | | TYPICAL | MAX | | ON DELAY | OFF DELAY |
| FA948 | DTL, J-K | 50 | - | <7 | 50 (TYP) | 75 (TYP) |
| FA9001 | TTL, J-K | 75 | 120 | 30 | 30 | 12 |
| SIG8827 | TTL, Dual J-K (AC) | 45 | 60 | 25 | 35 | 20 |
| SIG8424 | DTL, Dual R-S | - | 22 | 8 | 60 | 60 |
| TI5474 | TTL, Dual D | 45 | - | 15 | 35 | 50 |
| TI5472 | TTL, J-K | 40 | - | 10 | 50 | 50 |
| TI54L72 | TTL, J-K | 3.8 | 6.5 | 3 | 75 | 150 |

### B. GATES

| NO. | TYPE | POWER (MW.) TYP | MAX | AV. PROP. DELAY TYP | MAX | FANOUT |
|---|---|---|---|---|---|---|
| FA9046 | LP-DTL | 1 | 1.3 | 60 | 150 | 10 |
| FA930 | DTL | - | 8.1 | - | 50 | 10 DTL/75 LP-DTL |
| FA9002 | TTL | 11 | 18 | 6 | 12 | 10 |
| FA9009 | TTL | 30 | 52 | 10 | 17 | 30 |
| SIG8480 | TTL | 8 | 10 | 35 | 48 | 10 |
| SIG8880 | TTL | 15 | 17 | 13 | 20 | 10 |
| SIG8855 | TTL | 29 | 34 | 13 | 22 | 30 8800 Series<br>60 8400 Series |
| TI54L00 | LP-TTL | 1 | 1.6 | 33 | 60 | 10 |
| TI5400 | TTL | 10 | - | 13 | 22 | 10 54 Series<br>40 54L Series |
| TI54H00 | TTL | 22 | - | 6 | - | 12.5 54 Series |
| TI54H40 | TTL | 43 | - | 6 | - | 37.5 54 Series |

## CONTROL LOGIC BOOLEAN EQUATIONS

The following abbreviations will be used:

P = Parallel Format

S = Serial Format

R = Read Mode

W = Write Mode

M = Serial Word Marker

$T_{n-m}$ = Decoded pulse from timing generator where n is the state of the generator that the pulse begins and m is the state after which the pulse ends. The pulse width is (m-n + 1) x 125 nanoseconds. Thus $T_{5-7}$ is a pulse starting at state 5 and lasting thru state 7 and is 3 x 125 = 375 ns in width. A single digit subscript is a pulse lasting for only one state.

OF = Data Register Overflow

1. Data Register/Address Register Reset = $(T_o)\ (P + S \cdot M)$
   since $P = \overline{S}$, this simplifies to: Reset = $(T_o) \cdot (P + M)$
2. Parallel Data Transfer Pulse = $(T_{1-4}) \cdot (P) \cdot (W)$
3. Address Transfer Pulse = $(T_{1-4}) \cdot (P + M)$
4. Read Switch = $(T_{5-7}) \cdot (P + M)$
5. Read Driver = $(T_{6-7}) \cdot (P + M)$
6. Sense Amp Strobe = $(T_{6-7}) \cdot (R) \cdot (P + M)$
7. Digit Driver = $(T_{9-13}) \cdot \left[P + (R) \cdot (M) + (W) \cdot (OF)\right]$
8. Write Switch = $(T_{10-12}) \cdot \left[P + (R) \cdot (M) + (W) \cdot (OF)\right]$
9. Write Driver = $(T_{11-12}) \cdot \left[P + (R) \cdot (M) + (W) \cdot (OF)\right]$
10. Data Shift Pulses = $(S) \cdot \left[(T_{11}) \cdot (R) + (T_6) \cdot (W)\right]$

## H. PRELIMINARY PACKAGING DESIGN

Some broad packaging concepts have been evolved to allow for a final package design meeting the work statement package requirements. These design concepts are presented below.

### 1. Plane Packaging

Packaging design of the Phase II engineering model was based on the use of an encapsulated package for the laminated ferrite wafers. This technique, developed at the RCA Memory Products Division, use a pair of plastic rectangular rings between which the wafer, with attached leads, is placed. The package is then sealed with epoxy between the rings and with top and bottom metal plates. Figure 56 shows a typical encapsulated 64 x 64 wafer. To prevent contamination by moisture, a desiccant is sealed into the package with the wafer. The result is a rugged device, approximately two inches on a side and one tenth inch thick containing 2048 bit locations, with wires brought out from the four sides of the rectangular assembly. This assembly can then be cemented to a printed wiring board, and the wires soldered to runs on the board.

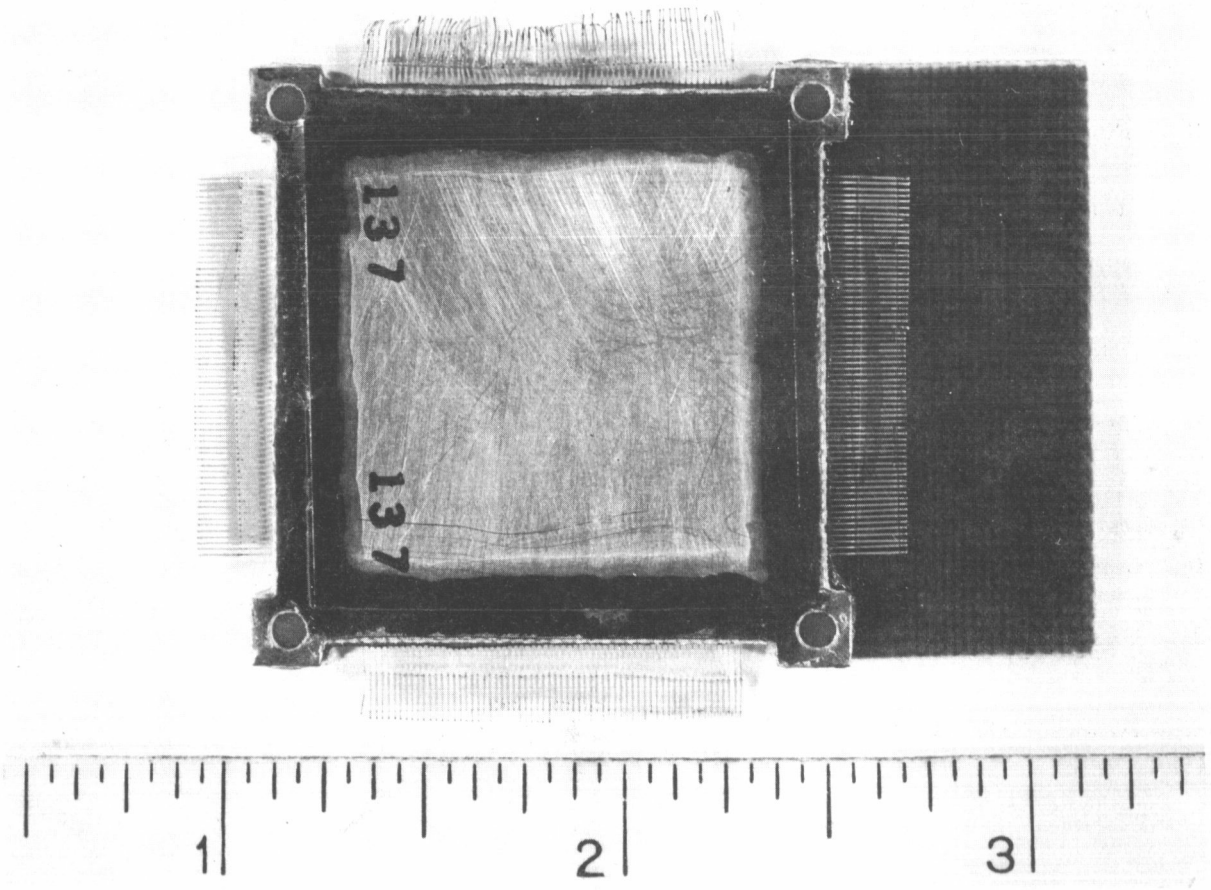



Figure 56. Encapsulated 64 x 64 Wafer

The encapsulated ferrite wafers will be mounted in a planar fashion on eight circuit boards by precision impulse soldering, a technique developed by RCA. Eight planes will be mounted on each circuit board with digit lines wired in series. Each circuit board will also contain the necessary decode circuits, diodes and drivers* to perform word addressing functions for read and write operations. The boards will be two sided with a printed circuit interconnection pattern on the surface to which the wafers are mounted and a ground plane on the unmounted surface. Driver addressing will be completed on the circuit board, so that decoded driver addresses will not be carried off a board unit. The word switch addresses will not be completed on a board and they will be carried through the connectors and harnessing from board to board.

2. Digit and Sense Circuitry Packaging

A board identical in size to the eight boards used for plane mounting will be used to mount the Hybrid Digit Drivers, the Integrated Sense Amplifiers, the Discrete Circuits, and the Hybrid Digit Line Switches. These circuits will be mounted on the same board due to the critical nature and interrelations of their functions. It should be pointed out that despite the large number of these circuits (32 digit drivers, 32 dual switch units, 14 discrete circuits, and 32 sense amplifiers) the board will have sufficient mounting area (in excess of 180 sq. inches) to permit relatively straight forward planar circuit board interconnection.

3. Logic Circuit Packaging

Great care must be taken in packaging the logic modules* to insure minimum crosstalk and noise generation. The package must also be designed for ease of repair, modification, and trouble shooting. To achieve these conditions at minimum cost, a commercially available packaging panel of the AUGAT 8136 series will be used. This board is designed to work with dual-in-line packages and comes with either solder pot or wire wrap terminals. The board has both a ground and a power plane and can accommodate sixty modules. The wire wrap terminal scheme will be used. This scheme is preferred due to its reliability, ease of interconnections, and ease of repair. The board and pin design also allow for module replacement, through the simple procedure of replacing a faulty unit by plugging a proper unit into the terminals. Based on the logic studies presented in this report, two 60 module boards will have sufficient capacity to perform the required functions with enough spare positions to meet good design practice.

* Shown in the logic diagrams in Section II-G.

By employing this high density packaging technique and by performing a careful board layout to minimize the length of point-to-point wiring runs, this packaging scheme will permit the use of any of the dual-in-line circuits proposed including high speed MSI units. It will be necessary to include power line filters on each board to minimize system effects of TTL switching transients.

4. DC/DC Converter Packaging

The DC/DC Converter which supplies +6V, -6V, +12V and -12V will be mounted on a tenth board equal in size to those boards discussed in sections I & II. In this fashion the converter unit can be developed, built, and tested as a separate entity. For system modification, the unit can be tested with this board removed through the use of a paralleled power input connector on the harness board. The +5V filter unit will also be located on this board.

5. Harness Board

The circuit boards described above will be connected via a harness board that will also serve as a mounting medium for the individual boards. This harness board will connect with the long dimension of the individual boards and will be a four layer printed wiring board. The outer two layers will be used for signal lines, and the center two layers for ground and power planes. In this manner, minor modifications in the wiring can be performed without need for redesign and rebuilding of the harness board.

6. The Composite Unit

The assembled unit is shown in sketch form in Figure 57. Ten large boards, and two logic boards are plugged into the harness board which affords both a mounting medium and an interconnection matrix. Additional interboard interconnections are supplied by connectors attached to the vertical edges of the circuit boards shown in Figure 57. This connector scheme is conceptually demonstrated in Figure 57. These connectors are employed on both vertical edges of each large memory plane board, and are mainly used to connect the digit lines and the switch lines which must be distributed to all of the memory plane boards. External connectors will be mounted on a bracket on the periphery of the harness board.

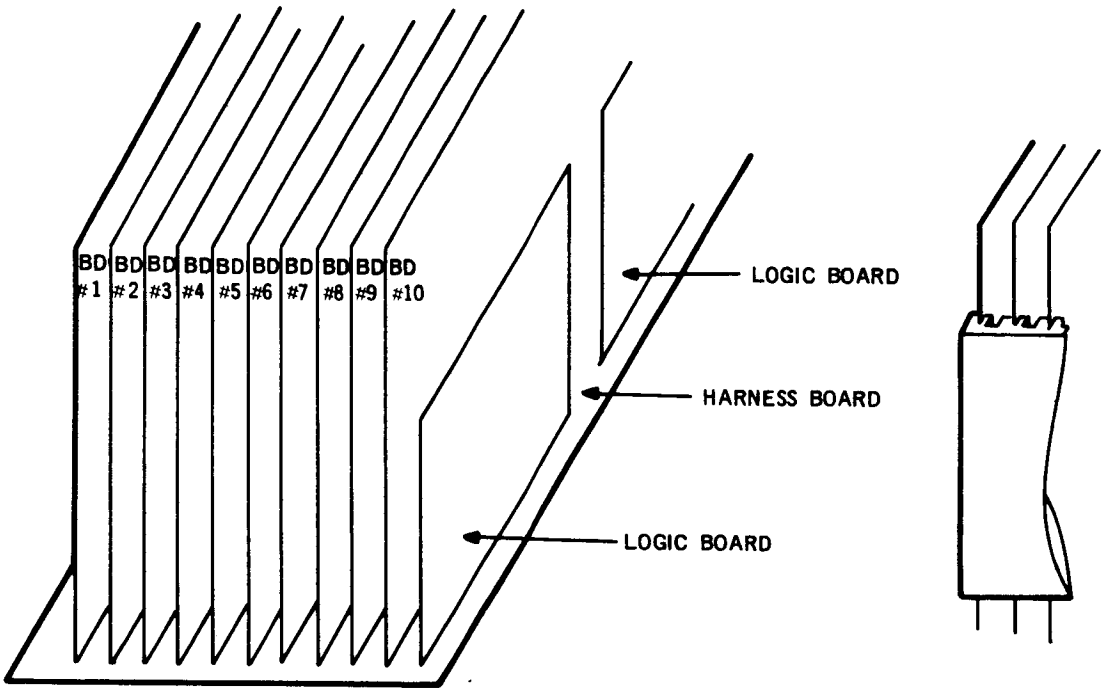



Figure 57. Memory System Packaging Concept

This composite arrangement will permit complete and basic package disassembly, to simplify trouble shooting and replacement of the components in the system.

## I. PRELIMINARY RELIABILITY EVALUATION

The preliminary reliability evaluation consisted of three subtasks. The first of these was a preliminary parts evaluation, conducted on those parts which were identified during the design phases of the study tasks. Tentative failure rates were determined for these parts, and the second subtask was to obtain a preliminary probability of survival for the memory system based on these failure rates. The third subtask was to analyze the system for failure modes and determine the effects of these failures on system performance.

The system for which this evaluation was performed was essentially that given in the preliminary logic design, hybrid driver, and sense amplifier task reports.

1. Parts Evaluation

The parts evaluation was conducted in accordance with standard AED procedures, by reliability engineers. These procedures have been established in accordance with NPC 250-1: Reliability Program Provisions for Space System Contractors, and are followed at AED on all NASA programs. The reliability program is based on the application of NPC 200-2: Quality System Provisions for Space System Contractors, NPC 200-3: Inspection System Provisions for Suppliers, and NPC 200-4: Quality Requirements for Hand Soldering of Electrical Connections, as well as other NASA requirements. The environmental levels for which the failure rates were established were taken from typical NASA spacecraft programs.

Laminated Ferrite Wafers

The manufacturing processes and physical packaging of the laminated ferrite wafers were reviewed. Wafers fabricated at the Memory Products Division and packaged in sealed, encapsulated enclosures have been tested for extended periods in a 95% humidity environment, with no indication of degradation. A vibration survey (2 g's to 2000 cps) was conducted on individual wafers and on a 16-wafer memory stack. No serious resonances were detected. These tests demonstrate that wafers which are initially acceptable electrically will not degrade with time.

Logic Circuits

The Fairchild FA9000 Series of Diode-transistor logic, FA9300 four-bit shift register and FA9301 Decoder which were selected for the logic circuits have been used on high-reliability programs. There are established failure rates for each type.

Sense Amplifiers

Both the MC1510 preamplifier and the $\mu$A710 comparator have been used on high reliability programs. The failure rate for the sense amplifier was estimated on the basis of this prior usage and experience with similar devices.

Hybrid Circuits

High-reliability hybrid circuits have been produced by a number of manufacturers for use in space programs. Reliability is achieved by a combination of conservative design, use of high reliability components, and tight manufacturing process control. The circuits used in the memory system have been designed to provide adequate safety margins in electrical performance. The specifications used for procurement of these circuits should include provisions to insure that only reliable components are used.

The estimated failure rates used in this study for hybrid circuits are based on experience gained on similar programs. AED has had such circuits supplied by four suppliers: Sprague, Amelco, Halex and RCA. In all cases it was possible to obtain satisfactory parts by imposing controls on device selection, incoming inspection, assembly of the devices in the package, including bonding to the substrate and wire bonding, and use of high-quality packages. The failure rates were estimated by considering the circuit and package complexity and assuming that similar controls would be imposed on the supplier.

8 MHz Oscillator

A Greenray oscillator was selected for this part. Approval was based on, and the failure rate estimated by a review of the individual components used in the unit, the ability of the supplier to comply with spacecraft program requirements, the provision for qualification testing of the units, and the use of similar units on high-reliability programs.

Interconnections

Two types of interconnections are required for the system: removable connections using plugs and receptacles, and permanent connections. The removable connections will be made using space-qualified parts. The permanent connections will be made using reflow solder techniques, with adequate controls and using trained personnel and qualified equipment. The failure rate per connection has been established on prior programs, and the number of connections was obtained by analysis of the system.

Other Parts

Because of the preliminary status of the design, it was not possible to evaluate the DC-DC converter, power line filters, or the diode selection matrix. In order to include these in the failure mode analysis and system reliability estimate, average failure rates were used for these parts, based on rates for similar parts.

Table 4 is a listing of those parts which have been identified with respect to manufacturer or part number.

2. Survival Probability

To determine the aggregate failure rate of the system, a simple summation of failure rates was made. On a summary basis, a tabulation of failure rates for the Laminated Ferrite Memory System is as follows.

TABLE 4

PARTS IDENTIFICATION

| Item | Manufacturer | Parts Data | |
|---|---|---|---|
| | | Part No. | Description |
| Laminated Ferrite Wafers | RCA | --- | Similar to MF 2102 |
| 8 MHz Oscillator | Greenray | Y-283-3 | Crystal Oscillator |
| Integrated Circuit | Fairchild | FA 9300 | 4-Bit Shift Register |
| Integrated Circuit | Fairchild | FA 9301 | 1 out of 8 Decoder |
| Integrated Circuit | Fairchild | 9000 Series | Diode-Transistor Low Power Logic Elements |
| Sense Amplifier | Fairchild | μA 710 | Comparator |
| Sense Pre-amplifier | Motorola | MC 1510 | Linear Amplifier |
| Connectors | Cannon | RCA 1960830-4 | 37 Pin Connector |

Reliability Estimate (% per 1000 hrs)

| | | | | |
|---|---|---|---|---|
| Switches | 128 x 0.0016 | = | 0.2048 | |
| Digit Driver | 64 x 0.002 | = | 0.128 | |
| R/W Driver | 64 x 0.004 | = | 0.256 | |
| R/W Switches | 64 x 0.004 | = | 0.256 | |
| Diode Matrix | 8192 x 0.0001 | = | 0.8192 | |
| Sense Amplifier | 32 x 0.002 | = | 0.064 | |
| SUB TOTAL | | | 1.7280 | 1.728 |
| ADDRESS | | | | |
| Register | 12 FF 3 gates each 36 gates | = | 0.036 | |
| Decoding | 18 CCSL 9301 (18 x 0.01) | = | 0.180 | |
| SUB TOTAL | | 0.216 | 0.216 | |
| Input/Output Reg. | 32 FF x 0.01 | = | 0.3200 | |
| | 98 Gates x 0.001 | = | 0.0980 | |
| | 34 Diodes x 0.0001 | = | 0.0034 | |
| SUB TOTAL | | | 0.4214 | 0.4214 |

| | | | | |
|---|---|---|---|---|
| Command Circuits | | | | |
| 1) | 8MHz Osc | = | 0.002 | |
| 2) | CCSL 9300 (2) 2 x 0.01 | = | 0.020 | |
| 3) | Decoder 30 Gates x 0.001 | = | 0.030 | |
| 4) | Input Sync 3 Gates x 0.001 | = | 0.003 | |
| 5) | Mode Control 9 Gates x 0.001 | = | 0.009 | |
| SUB TOTAL | | | 0.064 | 0.064 |
| Power System | | = | 0.625 | 0.625 |
| Memory Plane Interconnections = | | | | |
| | $65,536 \times 1 \times 10^{-6}$ | = | 0.065 | |
| Other Interconnections | | | | |
| Reflow Solder: | $1800 \times 10^{-6}$ | | 0.002 | |
| 37 pin Connection: | 52 x 0.005 | | 0.260 | |
| | | | 0.262 | 3.380%/1000 hrs |

The probability of success for a one year operation for a 60% duty cycle is calculated as follows:

$P_s = e^{-\lambda t}$

$\lambda$ = TOTAL Failure Rate %/1000 hours = 3.38

t = Total time (operating) hours

= 0.6 x 8760 = 5256 hours per year

0.6 x 4380 = 2628 hours per 6 months

$P_s$ = 83.3% for one year, 60% duty cycle

$P_s$ = 91.0% for one half year, 60% duty cycle

a. Performance Requirements

Mission durations of 6 months and a year were used in this analysis to obtain the probability of survival. A duty factor of 60% was also selected as a realistic figure for use in this analysis.

b. Level of Severity

In accordance with standard reliability practices, three levels of severity were used defined as follows:

Level 1. The failure mode will have no significant effect on the internal system performance.

Level 2. This failure mode will produce a partial loss of data or degradation of performance but the memory system still retains a measure of usefulness.

Level 3. The failure mode will completely destroy the usefulness of the memory system.

3. Failure Modes and Effects (FM&E)

The memory system was examined with respect to the impact of various modes of failure on the Laminated Ferrite Memory system operational capability. The major components were next examined for the impacts of the various failure modes on system performance.

In general, the lowest level of assembly reached under this task was the functional circuit; and this is the level for which data is presented. Inherent in the analysis, however, is an examination of the parts employed and their respective failure mode.

Failure rates used were for generalized average parts where specific part data was not available. In cases where specific part data was available, specific failure rates were used based on average stress levels.

Failure Mode and Effect Summary — Ten failure modes were identified which could cause complete failure of the memory system (level 3). The net failure rate for these modes was estimated to be 0.65% per 1000 hours. Based on one year operation at 60% duty cycle, the probability of complete failure is 3.3%.

Thirty-one level 2 failure modes were identified, which will cause degraded, but useful, performance from the system. The total failure rate for these modes is 2.73% per 1000 hours, leading to a probability of degraded performance for one year at 60% duty cycle of 13.3%.

The remaining failure modes identified are at level 1, and are not considered to have a degrading effect on memory system performance.

Table 5 lists the failure modes by level of severity.

TABLE 5

FAILURE MODES AND EFFECTS

| LEVEL 3: Complete loss of function | | | | |
|---|---|---|---|---|
| Part or Function | Failure Mode | Possible Cause | Failure Effect | Failure Probability |
| DC-DC Converter | Loss of supply voltage | Transistor, transformer or capacitor failure | No memory operation | 0.625%/1000 hours |
| Timing Generator | Loss of timing signal | Failure of FA 9300 or decoding gate | No memory operation | 0.01 |
| 8 MHz Oscillator | No output | Failure of crystal or amplifier | No memory operation | 0.002 |
| Input Synchronizer | No output | Failure of gate or flip-flop | No memory operation | 0.001 |
| Input/output register | No sense ampl strobe signal | Failure of a strobe gate | No read function | 0.001 |
| Address register | No transfer pulse | Failure of transfer gate | Wrong address selected | 0.001 |
| Input clock | No signal | Bad connection | No memory operation | Very low |
| Input read command | No signal | Bad connection | No memory operation | Very low |
| Input write command | No signal | Bad connection | No memory operation | Very low |
| Input Read/write mode command | No signal | Bad connection | No read/write mode | Very low |

TABLE 5

FAILURE MODES AND EFFECTS (Continued)

| LEVEL 2: Partial loss of function: | | | | |
|---|---|---|---|---|
| Part or Function | Failure Mode | Possible Cause | Failure Effect | Failure Probability |
| Decoding network | No read switch signal | Gate failure | Unable to read 64 words | 0.001 |
| | No read driver signal | Gate failure | Unable to read 64 words | 0.001 |
| Decoding network | No write driver signal | Gate failure | Unable to write 64 words | 0.001 |
| | No write switch signal | Gate failure | Unable to write 64 words | 0.001 |
| | No digit driver signal | Gate failure | Unable to write 1 bit | 0.001 |
| Mode control | No output | Gate failure | Loss of write or parallel function | 0.001 |
| Input/output | No shift pulses | Gate failure | Loss of serial operation | 0.001 |
| | No serial data in | Gate failure | Loss of serial operation | 0.001 |
| | No shift enable signal | Gate failure | Loss of serial operation | 0.001 |
| | No data reset signal | Gate failure | Loss of parallel operation | 0.001 |
| | No parallel transfer sig. | Gate failure | Loss of parallel operation | 0.001 |

TABLE 5

FAILURE MODES AND EFFECTS (Continued)

| Part or Function | Failure Mode | Possible Cause | Failure Effect | Failure Probability |
|---|---|---|---|---|
| Decode Matrix | Wrong address | FA9301 failure | Some addresses will be incorrect | 0.01 |
| Address register | No reset pulse | Gate failure | Wrong address may be selected | 0.001 |
| | One output incorrect | Gate failure | Wrong address may be selected | 0.002 |
| Sense Amplifier | No output | Sense amplifier failure | Loss of one bit | 0.002 |
| Read switch | No output | Transistor failure | Not able to read 64 words | 0.002 |
| Read driver | No output | Transistor failure | Unable to read 64 words | 0.002 |
| Write switch | No output | Failed transistor | Unable to write 64 words | 0.002 |
| Write driver | No output | Failed transistor | Unable to write 64 words | 0.002 |
| Digit Line switch | No switching | Failed transistor | Unable to read or write one bit | 0.02 |
| Digit driver | No data 1 | Failed transistor | Unable to write one bit | 0.02 |
| | No data 0 | Failed transistor | Unable to write one bit | 0.02 |

TABLE 5

FAILURE MODES AND EFFECTS (Continued)

| Part or Function | Failure Mode | Possible Cause | Failure Effect | Failure Probability |
|---|---|---|---|---|
| Memory stack | Single bit not stored | Open bit line | Unable to read or write one bit | 0.032 total |
| Memory stack | Single word not stored | Open word line | Unable to read or write one word | 0.032 total |
| | Single word not stored | Open write diode | Unable to write one word | 0.41 total |
| | Single word not read | Open read diode | Unable to read one word | 0.41 total |
| Parallel output | One bit wrong | Bad connection | Unable to read one bit during parallel mode | Very low |
| Serial output | No data | Output stage | Unable to shift out data in serial mode | Very low |
| | Wrong data | Bad input/output register flip-flop | Unable to read or write correct data in serial mode | Very low |
| Address register | One bit wrong | Bad address register flip-flop | Some addresses will be incorrect | Very low |
| | One bit wrong | Bad connection | Some addresses will be incorrect | Very low |
| Input serial/ parallel mode command | No signal | Bad connection | No parallel mode | Very low |

TABLE 5

FAILURE RATES AND EFFECTS (Continued)

| Part or Function | Failure Mode | Possible Cause | Failure Effect | Failure Probability |
|---|---|---|---|---|
| LEVEL 1: No effect on operation | | | | |
| Word position marker | No output | Failed transistor | No word marker data | Very low |
| Access signal | No output | Failed transistor | No access timing data | Very low |

Reliability improvement for the memory system can be obtained by either complete or partial redundancy. Complete redundancy, in the form of a second standby unit, will reduce the probability of complete failure from 3.3% to 0.11% for one year. The probability of full operation for one year will be improved from 83.3% to 97.2%, and for six months from 91.% to 99.2%.

The failure modes for the memory system are well distributed. The only failure mode for which partial redundancy will offer a major improvement is the power supply system. If a standby DC-DC converter and filters were provided, the probability of complete failure within one year will be reduced from 3.3% to 0.18%. The probability of complete operation for either six months or one year will be changed from 83.3% to 86.5% by dual power supply systems.

# SECTION III

# CONCLUSIONS AND RECOMMENDATIONS

The work performed under this contract establishes in adequate detail the feasibility of designing spacecraft memory systems using laminated ferrites. The system elements critical with regard to present day performance as well as future potential have been identified and characterized in sufficient detail to serve as guides for such future material, device and circuit development or research which may be undertaken.

With regard to materials, the ferrite wafers produced under laboratory conditions for use on this contract contained several nonuniformities which precluded their use for this application.

The nonuniformities found during this study are in three main areas. The first of these is output signal under constant drive conditions. Output signals have been shown to vary appreciably from location to location on the same wafer, and between locations on different wafers made by the same process. The second area of nonuniformity is in the variations in noise capacitively coupled from the word lines into the sense line. This is a function of the spacing of the embedded conductors, and is evidence that the mechanical fabrication of the wafers has not been adequately controlled. The third source of inconsistent output signals was found to be due to an excessive disturb effect. The cause of this effect has not been fully identified, although it is believed to be associated with non-square hysteresis loops.

To improve the uniformity of laminated ferrite wafers, further effort must be devoted to identifying the causes of the effects listed above, and to evolution of production processes which provide sufficient control over these effects. Work presently being done at RCA in the fabrication of wafers using solid metal conductors rather than deposited sintered conductors is expected to result in substantial improvement in uniformity. With more uniformity in output signals, and a substantial reduction in capacitive noise which should also result from better mechanical control of the conductors, the use of lower coercive force materials at lower drive currents becomes more practical. The type 47 composition, despite the poor results obtained with it during this study, holds the greatest promise for a low-power, high-capacity spacecraft memory system.

A second factor found during this study to impose limitations on laminated ferrite memory systems is the attenuation and delay in the digit/sense lines. The use of solid conductors will also improve this characteristic, by reducing both the attenuation constant and characteristic impedance of the digit/sense lines.

As a result of the appreciable digit line attenuation and delay, it was found necessary to limit the length of the sense line to 2048 words and to drive a pair of sense lines with the same digit drivers by using a digit line switch. Even with improvements in attenuation and delay which will be obtained with better embedded conductors, increases in memory system capacity beyond the present requirement of 4096 words will necessitate the use of either paralleled digit drivers and sense amplifiers, or digit line switches. A preliminary circuit which was designed during this program shows promise as such a switch. Further effort is needed to refine the design, and to obtain multiple switches in hybrid packages or on monolithic chips.

The storage element which was selected, during the study, for use in the Phase 2 engineering model, was the standard Type 3515 wafer produced in some quantities at the RCA Memory Products Division. This wafer contains 4096 storage locations in a 64 x 64 matrix, and was produced in a sealed, encapsulated package.

Study of the state of the art in MOS logic devices and arrays showed that P-MOS arrays are not capable of operating at a 2 microsecond cycle time. Complementary MOS logic elements can meet the cycle time requirement, and save a substantial amount of power. At the present time there are few C-MOS types available. Availability of more complex C-MOS devices, and, ultimately, large arrays, will permit the use of such devices competitively with bi-polar logic arrays.

Driver circuits capable of producing 200 milliampere word currents and 20 milliampere digit currents, at the required speeds for 2 microsecond operation, were designed. These circuits presently require hybrid packaging. Future monolithic memory drivers employing either bi-polar transistors or Metal-Oxide-Semiconductor transistors will permit substantial improvements in system cost, power and reliability. Further development of the type 47 composition resulting in operation at lower drive currents will facilitate the future design of such monolithic driver circuits.

The sense amplifier designed during the study is adequate for sensing outputs which exceed 1.0 millivolt for at least 100 nanoseconds. It consists of two monolithic circuits and a passive coupling network, and can be packaged in a hybrid form. Since the sense amplifiers dissipate about one-fourth of the total system power, it would be useful to be able to switch this power off except during the read operation. It is not possible to switch sense amplifier power when operating at a 2 microsecond cycle time. The cycle time must be reduced to 10 microseconds in order to achieve a useful power saving in this way.

Further research in this area should be devoted to reducing sense amplifier power dissipation in one or more of three ways. The first is the development of a much lower power amplifier capable of sensing the millivolt level signals which would be obtained from Type 47 material operated at low drive currents. The second is to design an amplifier which will remain stable with a relatively high source impedance at the power supply terminals, eliminating the need for large filter capacitors at the power supply terminals, and thus speeding up the power turn-on and turn-off time. The third is improving the internal settling time of the amplifier after power turn-on. It is expected that the elimination of filter capacitors will permit appreciable power savings at cycle times as short as 4 to 5 microseconds, and improving the internal settling time in addition would permit operation at a 50% duty cycle with a 2 microsecond memory cycle time.

For the planned Phase 2 engineering model, the logic design was based on a family of medium power bi-polar logic devices. This selection was made after consideration of both operating speed and packing density. The use of a Medium-scale Integration line of Transistor-transistor logic (Fairchild FA9300 series) permitted a 2 microsecond cycle time, a reduction in the number of logic modules from 143 to 93, and a reduction of 350 in logic module interconnections. With this logic design, it was estimated that the power dissipation of the memory system, at a 2 microsecond cycle time, would be 25 watts. Using lower-power, but slower, circuits, and switching sense amplifier power, at a cycle time of 10 microseconds, it was estimated that the power consumption could be reduced to under 10 watts.

While earlier studies had indicated a laminated ferrite spaceborne memory system meeting these requirements could be production packaged within a volume of 400 cubic inches or less, the allotted volume specified under this contract was 18 x 12 x 12 inches maximum. The principal reason for this relatively large volume was to facilitate evaluation and test of the memory and its component parts, rather than to demonstrate ultimate packaging density. Accordingly the choice of packaging technique was predicated on ease of fabrication and test.

Packaging of the memory stack depends to a large extent on the size and shape of the laminated ferrite wafers. Four configurations for the wafers were studied, and it was concluded that a wafer with 260 conductors in one direction and 70 conductors in the other direction, using a 15 mil spacing for the conductors, would result in the optimum combination of reliability, weight and cost. Because other sizes were not available for the Phase 2 engineering model, it was decided to use the 64 by 64 square wafer, contained in encapsulated plastic holders. These wafer assemblies were to be mounted on printed circuit boards together with the word selection diode matrices, driver circuits and address decode circuits. Eight boards, with eight wafers on each, are required.

The packaging concept for the logic circuitry was predicated on the use of 14 lead in-line packages for the logic modules, plugged into an Augat 60 module board with ground and power planes.

As indicated previously in this report, RCA recommended, and Langley Research Center directed, termination of the effort at the conclusion of Phase 1. Underlying this action were two predominant reasons:

1. The lack of a current production source of laminated ferrite wafers. While sufficient type 3515 64 x 64 crossover wafers were on hand to probably satisfy the needs of this contract, no future source could be guaranteed. These type 3515 wafers (which limited measurements indicated possessed uniform properties) had been fabricated previously by the RCA Memory Products Division at Needham, Mass., during earlier pilot production operations. Subsequently, however, all laminated ferrite operations were terminated there. No other production source is known at the present time.

2. While the type 3515 wafer material could be used for this application, it is apparent that a lower drive material such as type 47 would offer greater advantages for advanced spacecraft memory applications.

Among these advantages are the prospect of single crossover operation and the promise of a completely batch fabricated memory--both of which would permit significant eventual cost, power and package size reductions. The conclusions of this study indicated the necessity for additional research on the process development of the type 47 material, as well as the necessity for additional development of the related integrated drivers and sensing batch fabricated circuits which are essential to permit full exploitation of the type 47 potential. It is essential that such component research and development be undertaken, of course, prior to system or circuit development for a spaceborne memory system.

Interconnections between the logic modules and to the board connector were to be made using wire wrap techniques. Interconnections between the memory boards and the logic boards were to be made by means of a harness board, for logic signals, and either coaxial or flexible shielded flat cable for the low level sense signals. This preliminary packaging concept demonstrated that the engineering model could be contained within the 18 x 12 x 12 inch allowable volume.

The preliminary reliability evaluation indicated that the memory system could be made sufficiently reliable for flight use by following standard RCA high reliability procedures. Included in these procedures are controlled processing for the laminated ferrite wafers, adequate 100% testing to insure proper wafer operation, pre-conditioning by burn-in and screening of all electronic components, and the use of proven high-reliability interconnections. An estimated probability of survival for one year of 83.3% was derived from the assigned parts failure rates.