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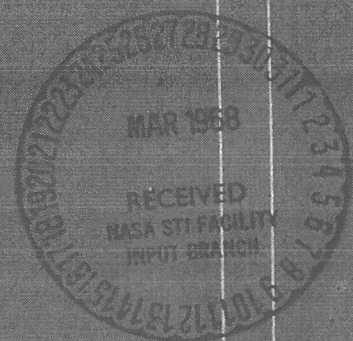
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AROD TEST MODEL HARDWARE
 FINAL REPORT
 CONTRACT NO. NAS8-11835

MOTOROLA Military Electronics Division

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FINAL REPORT

VOLUME II

Prepared for

INSTRUMENTATIONS AND COMMUNICATIONS DIVISION

ASTRIONICS LABORATORY

GEORGE C. MARSHALL SPACE FLIGHT CENTER

Huntsville, Alabama

Approved by

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Telecommunications Laboratory

AROD TEST MODEL HARDWARE

FINAL REPORT

CONTRACT NO. NAS8-11835

AROD SYSTEM
FINAL REPORT
AC-F-3065-3

ABBREVIATED TABLE OF CONTENTS

VOLUME I

- Section I. Introduction
- Section II. AROD Concept
- Section III. Program History
- Section IV. Program Results

REFERENCES

APPENDICES

- A. Developmental Vibration Test
- B. Pressure Test of AROD Base Plate
- C. Results of Thermal Mock-up Test for the Vehicle-Borne AROD Unit
- D. Thermal Test of a Typical AROD Cordwood Module
- E. AROD Vehicle Borne Equipment, Reliability Analysis
- F. AROD Ground Station Equipment, Reliability Analysis

VOLUME II

- Section V. Vehicle-Borne Equipment

VOLUME III

- Section VI. Transponder Station
- Section VII. AROD Vehicle Checkout Equipment
- Section VIII. Transponder Checkout Equipment

VOLUME II

TABLE OF CONTENTS

Section	Title	Page
SECTION I	INTRODUCTION	VOL. I
SECTION II	AROD CONCEPT	VOL. I
SECTION III	PROGRAM HISTORY	VOL. I
SECTION IV	PROGRAM RESULTS	VOL. I
REFERENCES		VOL. I
APPENDICES A Through F		VOL. I
V	VEHICLE-BORNE EQUIPMENT.	5-1
5.1	Type Construction.	5-2
5.2	Station Control Transmitter.	5-22
5.2.1	Technical Approach	5-25
5.2.2	Circuit Descriptions	5-27
5.2.3	Test Results	5-32
5.3	Control Data Modulator	5-32
5.3.1	Technical Approach	5-32
5.3.2	Logic Description.	5-37
5.3.3	Output Filter Description.	5-37
5.3.4	Test Results	5-40
5.4	Tracking Transmitter	5-40
5.4.1	Technical Approach	5-42
5.4.2	Functional Description	5-42
5.4.3	Test Results	5-48
5.5	Test Results	5-48
5.5.1	AROD Frequency Converters.	5-48
5.5.2	Tracking Subsection.	5-62
5.5.3	Vehicle Receiver Code Control.	5-129
5.6	Frequency Synthesizer.	5-154
5.6.1	Technical Approach	5-156
5.6.2	Circuit Descriptions	5-164
5.6.3	Physical Description	5-174
5.6.4	Performance Deviations	5-178
5.6.5	Conclusion and Results	5-179

VOLUME II

TABLE OF CONTENTS (Cont)

Section	Title	Page
V	VEHICLE-BORNE EQUIPMENT (cont)	
5.7	Data Measurements Subgroup	5-180
5.7.1	Vehicle Timing Unit	5-181
5.7.2	Data Readout System	5-195
5.7.3	Velocity Extraction Unit.	5-217
5.7.4	Range Extraction Unit	5-224
5.8	System Control Logic.	5-240
5.8.1	System Philosophy and Requirements.	5-242
5.8.2	Detailed Functional Description	5-242
5.8.3	Implementation.	5-255
5.8.4	Memory.	5-268
5.8.5	Test Results.	5-272
5.9	Power Converter	5-273
5.9.1	Requirements.	5-273
5.9.2	Technical Approach.	5-274
5.9.3	Theory of Operation	5-274
5.9.4	Breadboard Test Results	5-281
5.9.5	Test Results.	5-283
5.9.6	Design Changes.	5-288
5.9.7	Conclusions	5-288
5.10	Vehicle Transmitter Code Control.	5-289
5.10.1	Subsystem Requirements	5-289
5.10.2	Functional Logic Description.	5-290
5.10.3	Discrete Component Circuits	5-296
5.10.4	Test Results.	5-297
SECTION VI	TRANSPONDER STATION	VOL. III
SECTION VII	AROD VEHICLE CHECKOUT EQUIPMENT	VOL. III
SECTION VIII	TRANSPONDER CHECKOUT EQUIPMENT	VOL. III

VOLUME II

LIST OF ILLUSTRATIONS

Figure	Title	Page
5-1	Vehicle-Borne Equipment Functional Block Diagram . . .	5-3
5-2	Case 1 Top View.	5-4
5-3	Case 2 Top View.	5-5
5-4	AROD Vehicle-Borne Equipment	5-7
5-5	Station Control Transmitter.	5-8
5-6	Vehicle Tracking Transmitter	5-9
5-7	Bi-Phase Mod/Mult. X2.	5-11
5-8	R-F Converter.	5-13
5-9	Vehicle Tracking Receiver	5-14
5-10	Typical R-F Cordwood Module.	5-15
5-11	Micro Matrix Technique	5-16
5-12	Digital Integrated Circuit Module	5-17
5-13	Vehicle Frequency Synthesizer	5-19
5-14	Distribution Amplifier	5-20
5-15	Data Measurement Subsystem	5-21
5-16	System Control Logic	5-23
5-17	Vehicle Power Converter	5-24
5-18	Station Control Transmitter, Block Diagram	5-26
5-19	Station Control Transmitter, Schematic Diagram	5-28
5-20	Modulation Frequency Response Station Control Transmitter.	5-34
5-21	Modulation Linearity Station Control Transmitter	5-35
5-22	AROD Station Control Transmitter S/N 1 Modulation Linearity (without Modulation Amplifiers).	5-36
5-23	Station Control Transmitter, Motherboard Schematic Diagram.	5-38
5-24	Station Control Transmitter, I/C Module Logic Diagram	5-39
5-25	Phase Modulation and Power Amplifier of Vehicle Tracking Transmitter	5-41
5-26	Vehicle Tracking Transmitter, Block Diagram	5-43
5-27	TWTA Waveforms	5-49
5-28	Vehicle Tracking Transmitter, Schematic Diagram.	5-50

VOLUME II

LIST OF ILLUSTRATIONS (Cont)

Figure	Title	Page
5-29	Relative Sideband Power vs Modulation Frequency for Square Wave Modulation	5-51
5-30	Effective Modulation Bandwidth of Phase Modulator and Multiplier Composite of Above Curves	5-51
5-31	Power Output vs Power Input.	5-52
5-32	Phase Modulator and X4 Multiplier Modulated Output vs Power Input	5-52
5-33	Modulation Index vs Temperature.	5-53
5-34	Total Power Output of Phase Modulator and Multiplier	5-53
5-35	Vehicle TWTA Assembly	5-54
5-36	X8 UHF Multiplier and Filter Output Levels Relative to 8 Harmonic Level at -10 dbm	5-55
5-37	AROD Frequency Converters.	5-60
5-38	AROD Vehicle Tracking Receiver Subsection.	5-66
5-39	Vehicle Tracking Receiver Subsection, Block Diagram.	5-69
5-40	Frame Filter, Type T Output Voltage vs Frequency Input at 500 mv, S/N 1, 2, 5	5-77
5-41	Balanced Phase Demodulator Circuit	5-78
5-42	Phase Demodulator Spectral Component Output Relative to +J1	5-79
5-43	First Mixer Output Level vs Ref. Level	5-81
5-44	Second IF. Amplifier Test Data	5-83
5-45	Second Mixer Gain vs Ref. Input Level.	5-85
5-46	Predetection Channel Filter	5-84
5-47	Limiter Gain	5-87
5-48	AGC Amplifier Gain Linearity	5-89
5-49	8 MHz Balanced Detector 20 kHz Gain and Linearity Curves	5-91
5-50	Amplifier and A_L Demodulator	5-92
5-51	A_L Demodulator Gain	5-93
5-52	Carrier Loop Filter Input Signal	5-94
5-53	G_C Gate and Carrier Loop Filter.	5-96
5-54	G_C Gate and Carrier Loop Filter Test Date	5-98
5-55	6.0 MHz VCO Gain	5-100

VOLUME II

LIST OF ILLUSTRATIONS (Cont)

Figure	Title	Page
5-56	6 MHz VCO Test Data.	5-101
5-57	Frame Filter, Type M Output Voltage vs Frequency . .	5-103
5-58	A _H and Data Demodulator and A _H , A _L and Data Matched Filter Modules Detector Characteristics.	5-104
5-59	Integrate and Dump Matched Filter.	5-106
5-60	Range Loop Filter Response	5-108
5-61	12.757447 MHz VCO Gain	5-110
5-62	12-757447 MHz VCO Temperature Stability	5-111
5-63	12.8 MHz VCO Gain.	5-114
5-64	12.8 MHz VCO Temperature Stability	5-115
5-65	Rate AID Loop Filter Response.	5-116
5-66	Carrier Loop Frequency Preset.	5-118
5-67	Frequency Comparison - Preset Discriminator.	5-120
5-68	Frequency Comparison - Preset Discriminator.	5-121
5-69	Shift Register Mixing Action	5-123
5-70	Preset Discriminator Waveforms	5-123
5-71	H-Code Search Sweep Waveform	5-124
5-72	Doppler Mixer Test Data.	5-126
5-73	Doppler Multiplier Test Data	5-128
5-74	AROD Receiver Coder Control	5-130
5-75	Vehicle Code Control States (Program Sequence)	5-133
5-76	Code Clock Generator, Timing Diagram	5-136
5-77	Timing Pulses.	5-139
5-78	Frequency Synthesizer, Block Diagram	5-157
5-79	Phase Locked Loop Synthesis Technique	5-161
5-80	8 MHz X5 Multiplier Filter	5-162
5-81	7.2 MHz Doppler.	5-164
5-82	44.8 MHz Converter	5-165
5-83	8 MHz X5 Multiplier.	5-166
5-84	Digital Divider Module Packaging	5-169
5-85	Loop Filter.	5-171

VOLUME II

LIST OF ILLUSTRATIONS (cont)

Figure	Title	Page
5-86	VCO	5-172
5-87	AROD Distribution Amplifier.	5-175
5-88	Data Measurements Subgroup	5-182
5-89	Vehicle Timing Unit.	5-184
5-90	Timing Diagram for Data Readout Cycle.	5-186
5-91	Synchronous Monostable Multivibrator	5-188
5-92	Timing Diagram for the Synchronous Monostable Multivibrator	5-188
5-93	Timing Diagram of the Velocity Preset Signals. . .	5-191
5-94	Interface Circuit for Telemetry to AROD Interfacing	5-192
5-95	Data Readout Unit - Block Diagram.	5-196
5-96	Timing Diagram for Data Readout Cycle.	5-203
5-97	Word Order and Format.	5-204
5-98	Timing Diagram for the Generation of the Gated Clock Signals.	5-208
5-99	+5.6 VDC Power Source	5-214
5-100	Velocity Extraction Unit, Block Diagram.	5-220
5-101	Vehicle Velocity Extraction Module 1, Logic Diagram	5-221
5-102	Vehicle Velocity Extraction, Module 2.	5-222
5-103	Timing Signals	5-223
5-104	Functional Block Diagram of the Range Extraction Unit	5-226
5-105	VT-2F _H Signal Timing	5-228
5-106	Range Extraction Unit, Block Diagram	5-233
5-107	Oscillator Frequency Variation vs Temperature. . .	5-238
5-108	AROD System Control Logic Block Diagram.	5-241
5-109	Vehicle System Control, Logic Output Signal Timing Diagram.	5-243
5-110	VHF Data Format.	5-244
5-110A	AROD Station Acquisition Data Flow Diagram	5-251
5-111	Load Memory Address	5-267
5-112	Variable Duty Cycle Power Converter With Post Regulators	5-275

VOLUME II

LIST OF ILLUSTRATIONS (cont)

Figure	Title	Page
5-113	Variable Duty Cycle Pre-Regulator with Series Regulator and DC-DC Converter.	5-276
5-114	AROD Vehicle-Borne Power Converter	5-277
5-115	Power Converter, Schematic Diagram	5-279
5-116	Regulation of Breadboard Series Regulator.	5-282
5-117	Output Impedance of Power Amplifier Used for Audio Susceptibility When Loaded With 2 Ohms	5-286
5-118	Conducted Interference Using LSN (CW).	5-287

VOLUME II
LIST OF TABLES

Table	Title	Page
5-1	Performance of S/N 1 Station Control Transmitter . .	5-33
5-2	AROD Vehicle Receiver Code and Gate Equations. . . .	5-131
5-3A	Frequency Synthesizer Output Signals	5-154
5-3B	Temperature Compensated Master Oscillator Specifica- tion Summary	5-160
5-4	Phase Locked Loop Parameters	5-168
5-5	Package Configurations	5-176
5-6	Frequency Synthesizer Power and Weight Requirements.	5-177
5-7	Deviations From Specified Performance.	5-178
5-8	Performance Deviations of Master Oscillator.	5-179
5-9	Summarization of the Data Measurements Subgroup Documentation.	5-180
5-10	Fine Range Counter Output.	5-229
5-11	Q1 Output.	5-229
5-12	Control and Information Messages	5-245
5-13	Channel-Frequency Assignments.	5-245
5-14	Transponder Responses at the End of 4 Seconds. . . .	5-247
5-15	Station Sequence Registers	5-261

SECTION V

5. VEHICLE-BORNE EQUIPMENT

Since the AROD system is primarily a vehicle-based system, the functions of timing, control, station selection, and data extraction are all performed in the vehicle equipment.

The vehicle equipment will operate with up to four stations simultaneously. Two radio frequency links are used to accomplish the functions of station control, acquisition aid, and the determination of the relative range and velocity to each station. The relative range is derived from the two-way time delay of a ranging modulation on the S-band transmission, and the relative velocity is derived from the two-way Doppler shift of the S-band carrier from the vehicle to the station and back.

The system is fully coherent in the tracking mode, for all radio frequency carriers as well as the ranging modulation are derived from a common source.

The vehicle-borne equipment performs all of the functions normally assigned to a ground tracking station in a "turnaround" manner. The vehicle-borne equipment originates the control and tracking signals and acts as the measurement and data collection point.

The vehicle range relative to a ground station is derived from the time delay between originating the ranging signal and correlating the returned signal at the vehicle. The range measurement is instrumented with a resolution of 0.183 meter over an unambiguous range of 3042 kilometers.

The vehicle velocity relative to a ground station is derived from the Doppler frequency shift on the returned signal and is measured with a resolution of 0.026 meter/second over a span from 0 to +13,500 meters/second.

A time label is made with an accuracy of ± 0.1 milliseconds of real time referenced to the vehicle oscillator with a resolution

of 10 microseconds over a 5-minute period. The time label references the time all measurements commenced for every 250-millisecond period.

At an approximate rate of four times per second (to telemetry or external source) the vehicle equipment is capable of reading out simultaneously four range measurements, four velocity measurements, and the time label.

The data readout is compatible with either an on-board computer or a telemetry system, or both, simultaneously.

The terminal equipment which eventually receives the data determines the actual position and velocity vector of the vehicle by processing the measured data and the known location of the ground stations.

General information regarding the requirements and characteristics for the vehicle equipment subsystems can be found in references 1 and 12. The following sections provide further detail of the subsystem design characteristics.

The AROD vehicle borne equipment is packaged in two cases. Within the cases, the subsystems are roughly divided into frames. The circuitry within the frames is then packaged, mainly, in modules with some exceptions where the components are mounted directly to open boards.

Figure 5-1 is a functional block diagram of the major subsystems of the vehicle borne equipment. Reference designations for the sub-assemblies and the physical location within the cases is shown in Figures 5-2 and 5-3.

The AROD vehicle-borne system is divided into two cases to provide improved r-f isolation and to provide greater ease in handling. The angled case, see Figure 4-4, is used to permit easy removal of modules or frames, while still retaining a rigid connector mounting panel. The two cases are designed for mounting upon a thermal conditioning panel within the space vehicle or to the "cold plate" in the laboratory (see Figure 1-1) to maintain the base plate at approximately room temperature.

5.1 TYPE CONSTRUCTION

The lower half of the angle case consists of a thick aluminum base plate to which sheet aluminum sides have been dip-brazed.

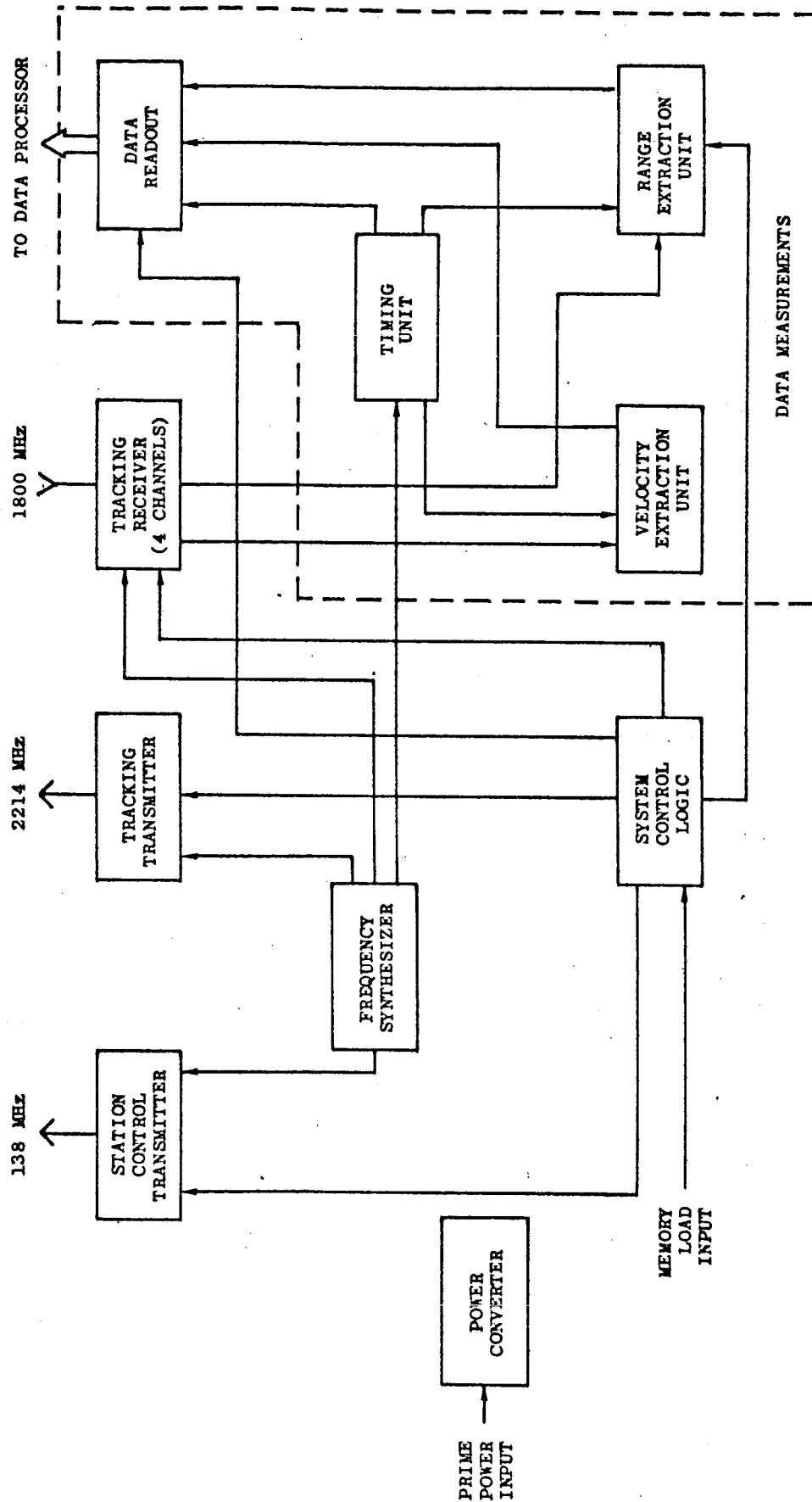


Figure 5-1. Vehicle-Borne Equipment Functional Block Diagram

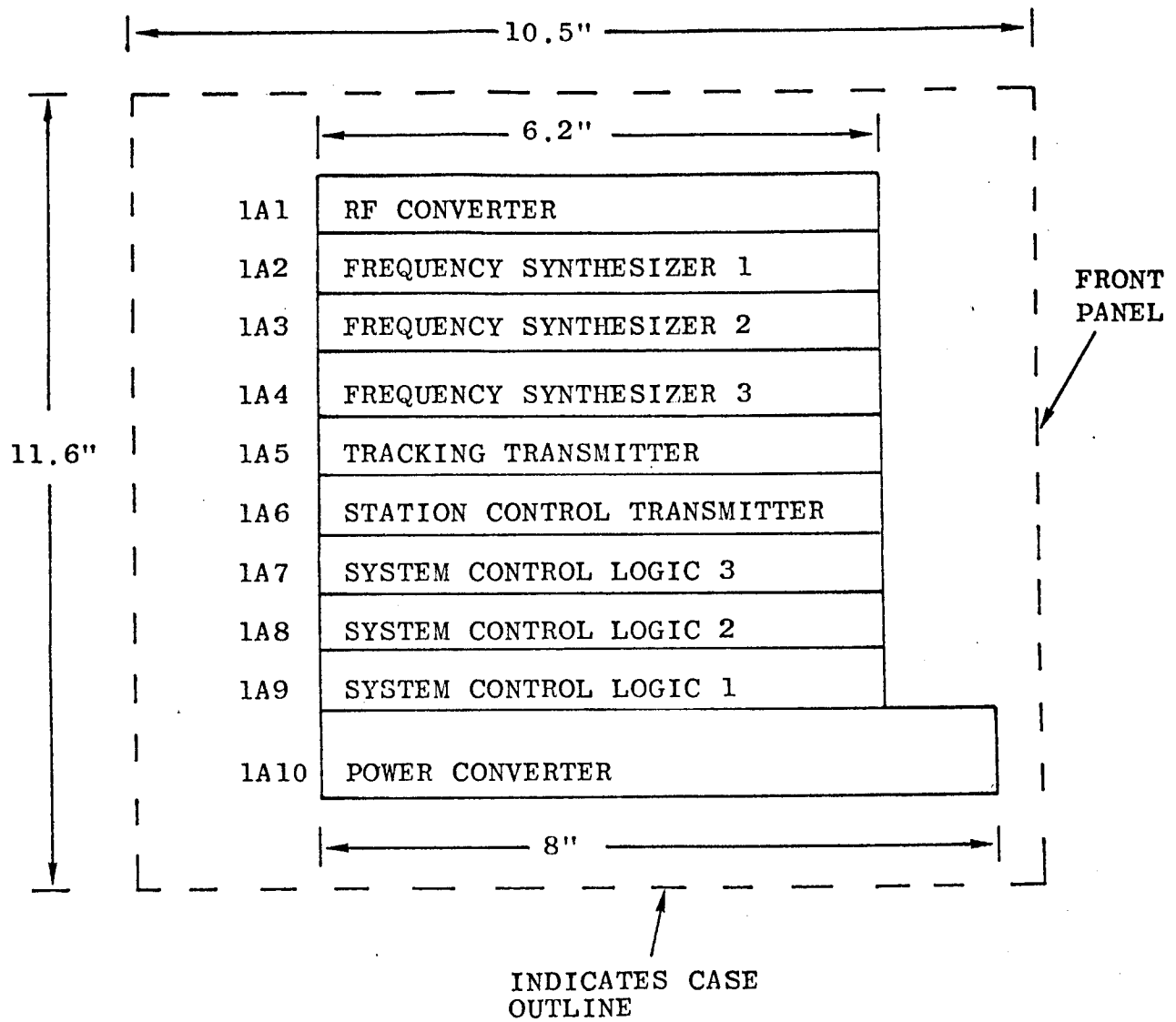


Figure 5-2. Case 1 Top View

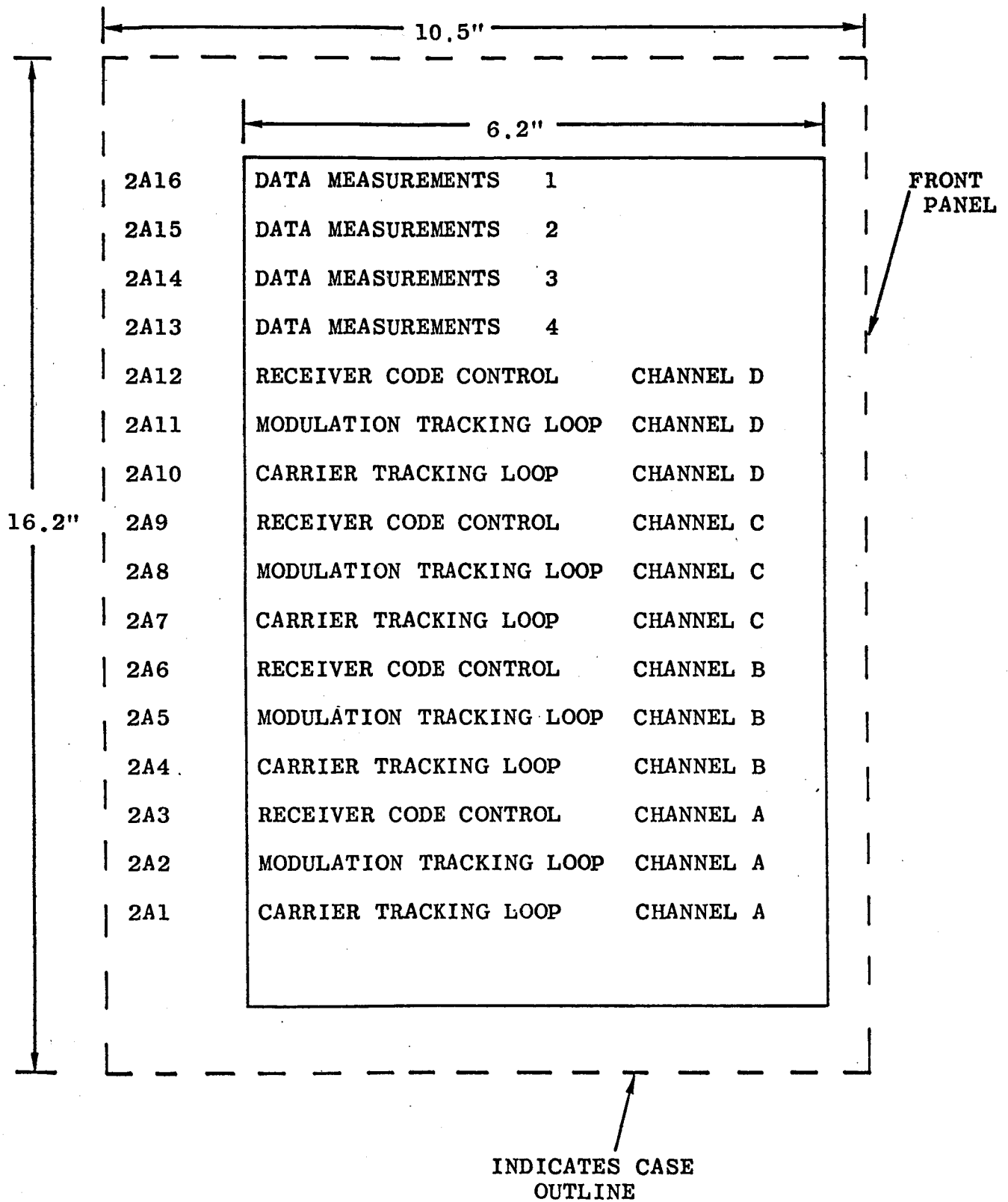


Figure 5-3. Case 2 Top View

Stiffening members have been brazed to the side panels. The high side serves as the case front panel and is used, therefore, as the connector mounting panel. The upper half of the case is fashioned in a similar manner -- of sheet aluminum with stiffening ribs added by dip-brazing.

Mechanical Features

Each case is provided with an inlet and a purging valve so that the case, when sealed, may be filled and pressurized with an inert gas. The cases and the internal module frame structures are designed to withstand the environmental conditions.

The interframe wiring harness is designed around prewired, pre-potted, miniature multipin connectors. The angled case as shown in Figure 5-4 provides good accessibility to the modules, to the wiring harness, and to the connectors.

Dimensions and Weight

The total volume of Case 1 and Case 2 is approximately 1700 cubic inches and the total weight is approximately 51 pounds, including interconnecting cables.

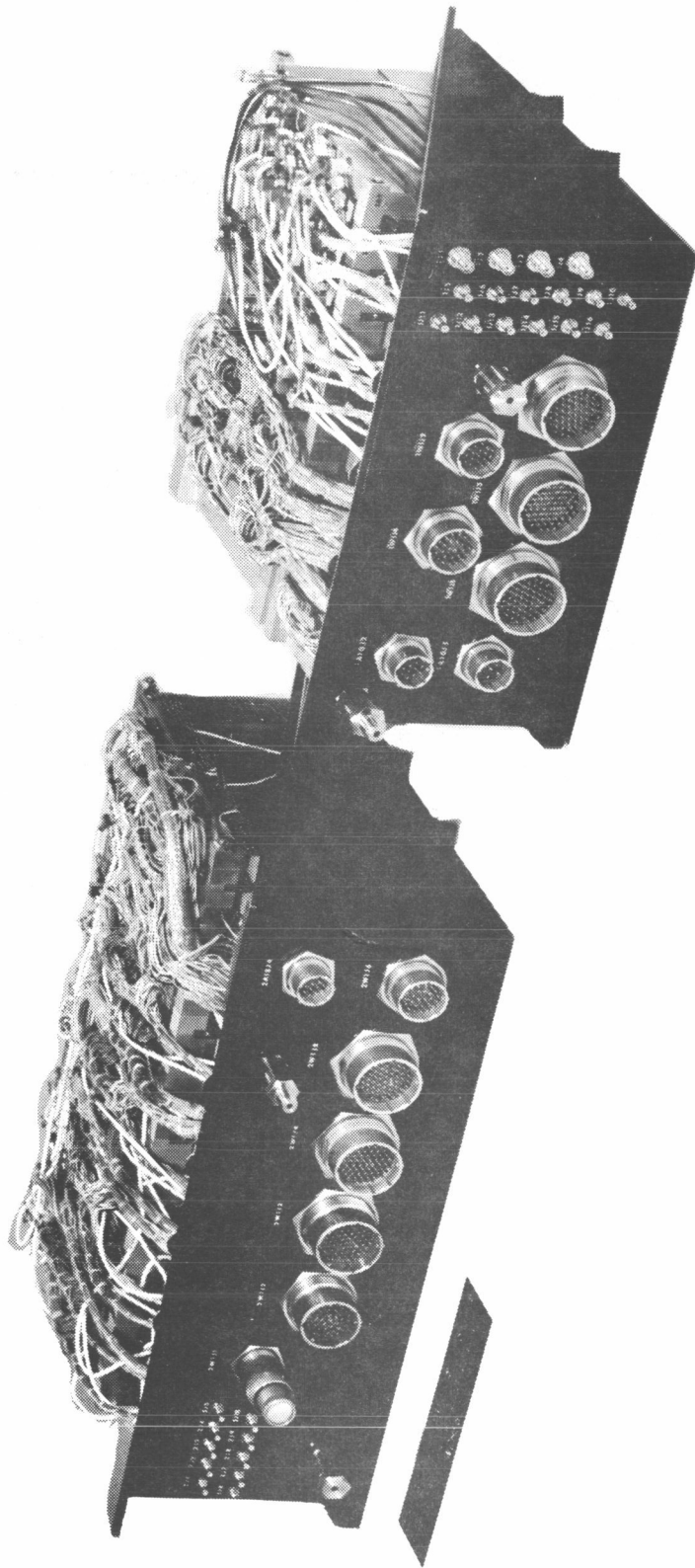
Frame Assemblies

All frame assemblies, 10 in Case 1 and 16 in Case 2, except for the d-c power converter, have common dimensions -- 0.9 x 4 x 6.2 inches. The method of securing the frames to the base plate is also identical from frame to frame and consists of a cap screw in each end. There are three basic types of module construction utilized -- integrated circuit "microharness" modules, cordwood style, and point-to-point style.

Station Control Transmitter

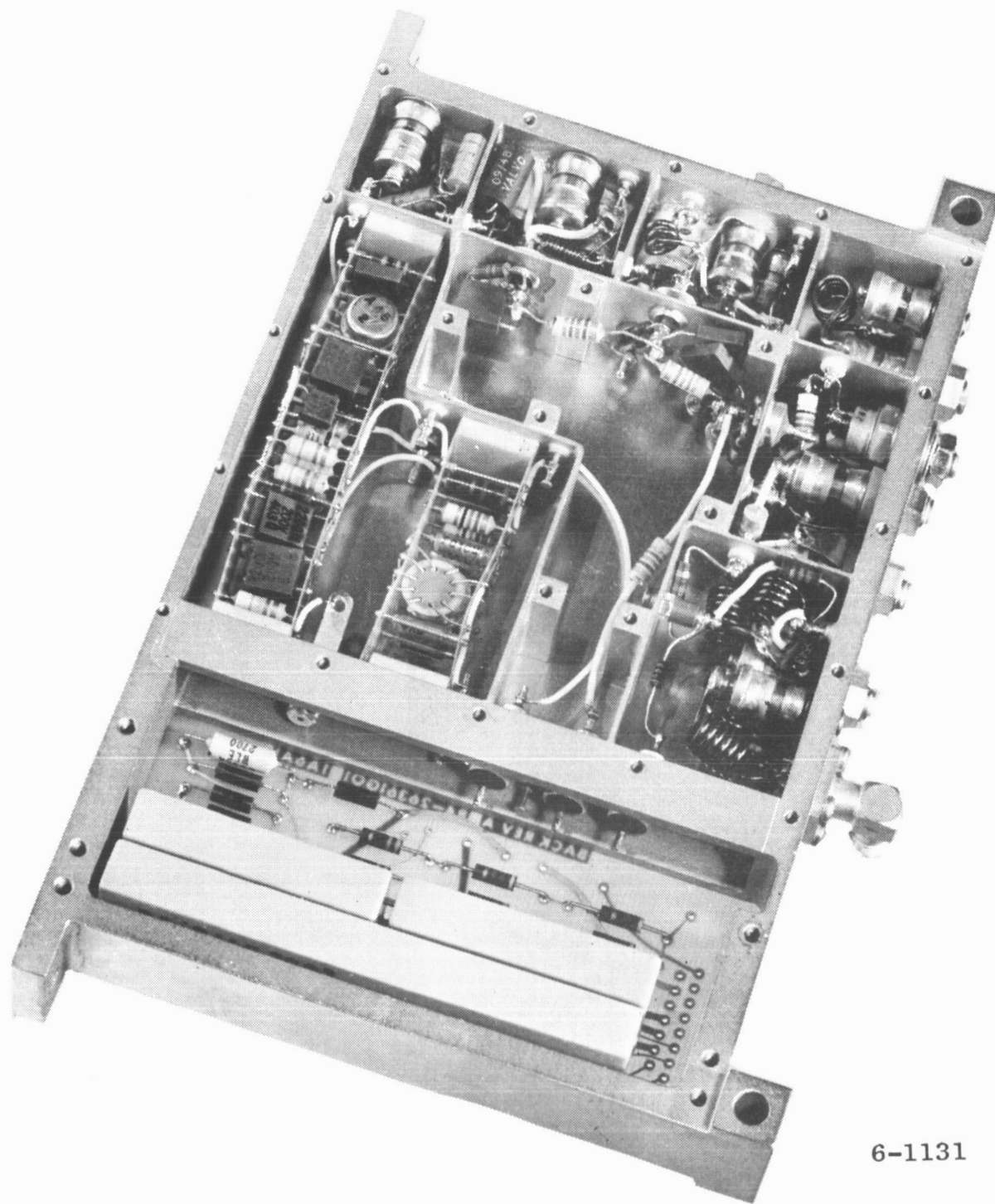
The station control transmitter is of standard dimensions and weighs 434 grams. The assembly is a combination of point-to-point wiring, r-f cordwood, and integrated circuit digital modules. A photograph of the transmitter is shown in Figure 5-5.

The Control Data Modulator, located at one end in Figure 5-6 uses digital integrated circuit modules attached to a printed motherboard along with a few discrete components. The modulator and first r-f stages utilize cordwood type construction while the later r-f stages, being more critical as to lead length and component placement utilize point-to-point wiring. The entire assembly is potted with epoxy-glass foam for shock and vibration considerations.



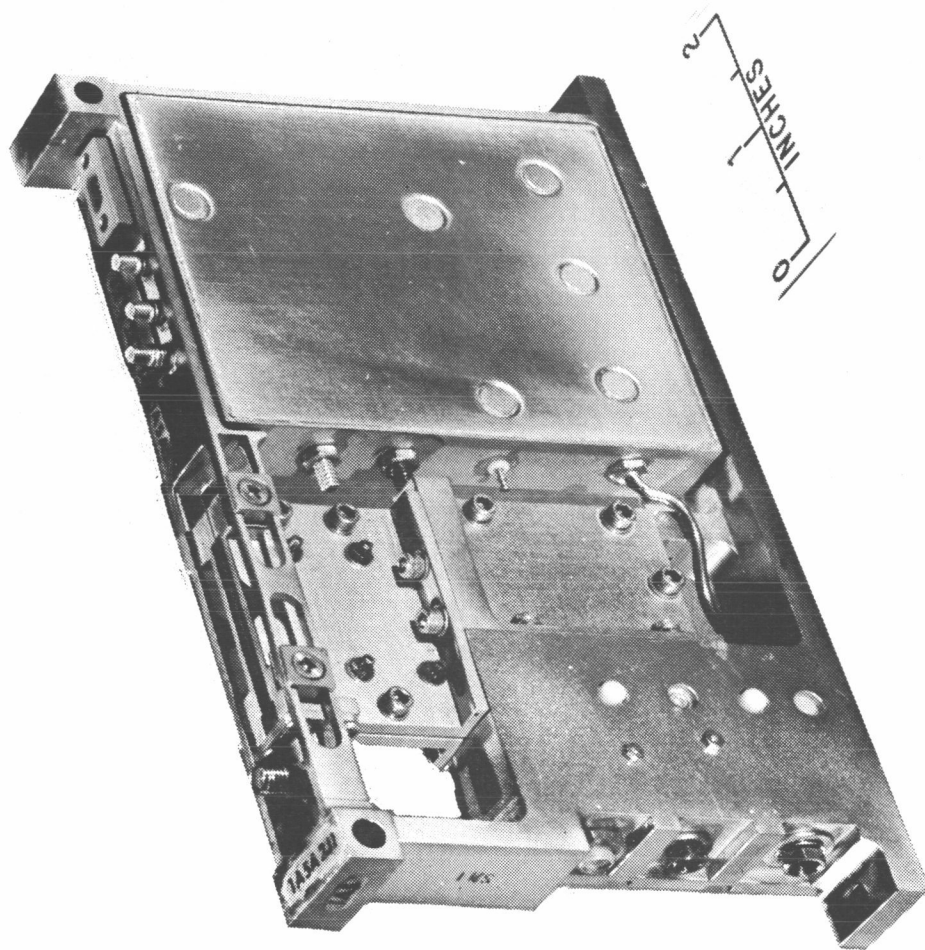
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Figure 5-4. AROD Vehicle-Borne Equipment



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Figure 5-5. Station Control Transmitter



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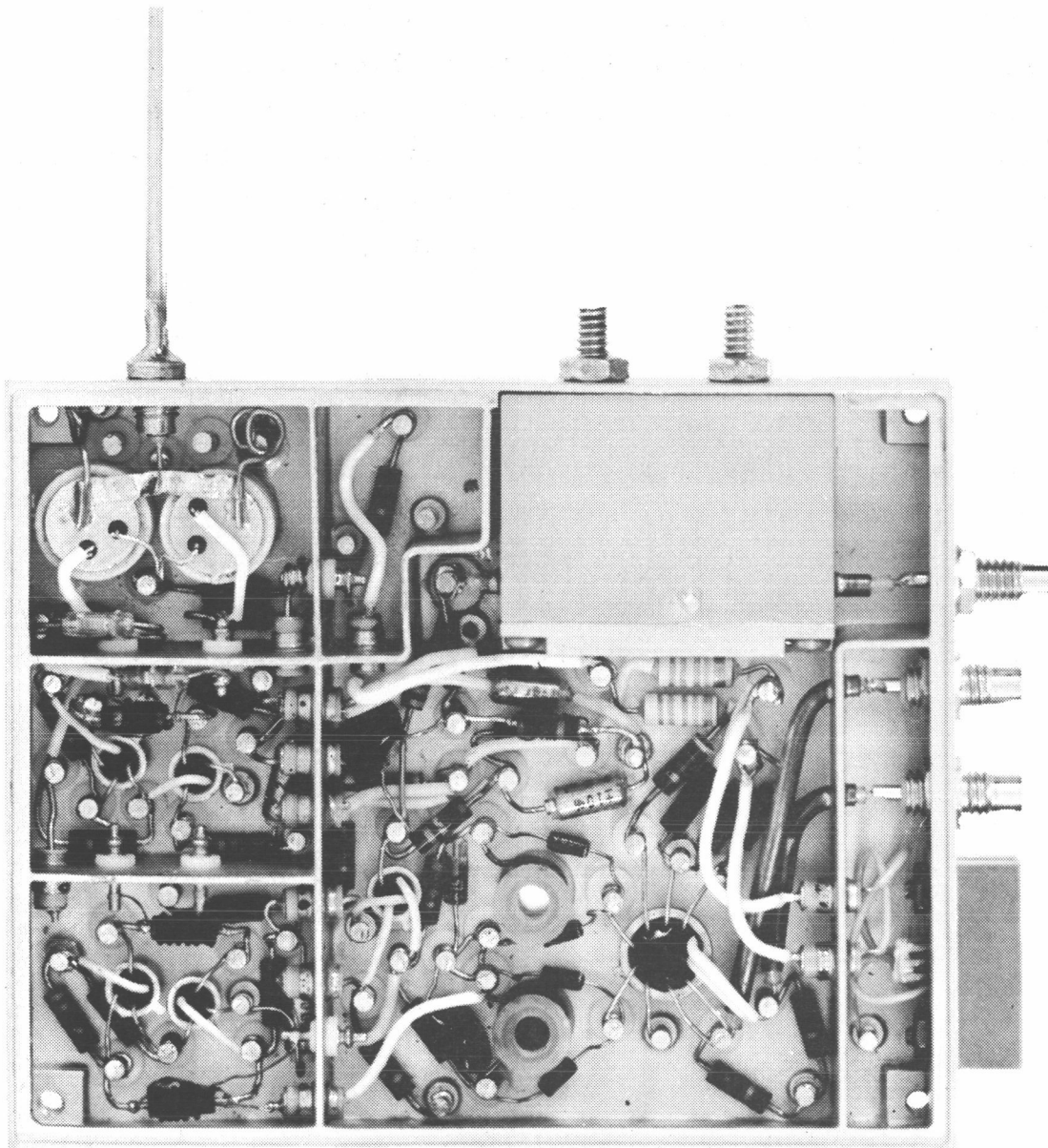
Figure 5-6. Vehicle Tracking Transmitter

Vehicle Tracking Transmitter

The vehicle tracking transmitter is built around the S-band X4 multiplier (see Figure 5-6), which occupies the left half of the frame. The entire housing is milled from a solid block of aluminum, with the X4 multiplier input circuitry located in a cavity at the lower left corner. Provision is made to accommodate the sliding adjustment on the output filter, upper left.

The bi-phase modulator/multiplier X4 subassembly is installed in the right half of the frame. For r-f shielding and ease of assembly, the d-c power connector and the coaxial input fittings are integral to the subassembly. A slot is provided in the frame through which they are inserted during assembly. This subassembly is completely hand-wired, point-to-point wiring, see Figure 5-7. The semi-rigid coaxial output is cut to fit at assembly with the S-band X4 multiplier.

After assembly and alignment, both the S-band X4 multiplier and the bi-phase mod/mult X2 are filled with an epoxy-glass form, Scotchcast #XR5068, to secure all components in position. The assembled unit is of standard dimensions and weighs 399 grams.



6-1110

Figure 5-7. Bi-Phase Mod/Mult. X2

R-F Converter

The r-f converter assembly is shown in Figure 5-8 (with the covers removed). The S-band diplexer is located in the upper side (under the nameplate). The mixer is located in the left center portion with the low-noise i-f stage and local oscillator multiplier just below. This assembly utilizes the point-to-point wiring style. This subassembly weighs 411 grams.

Vehicle Tracking Receivers

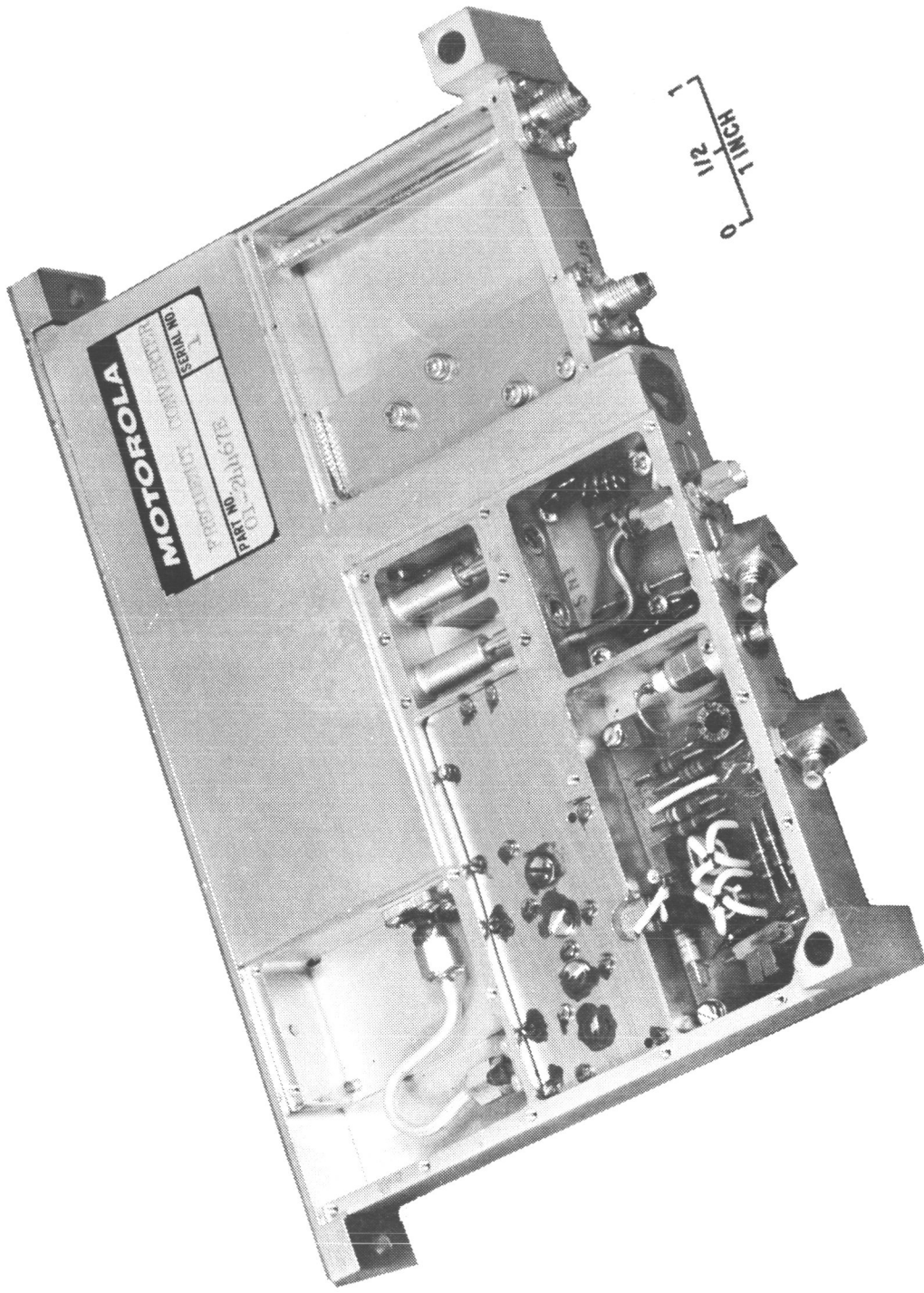
Each of the four vehicle tracking receivers utilizes three frames of Case 2. One frame, the carrier tracking loop, utilizes all r-f cordwood modules, the receiver code control frame is a double motherboard using all digital integrated circuit modules, while the third frame, the modulation tracking loop, uses a mixture of r-f cordwood and digital modules. A photograph of the three frames, which weigh approximately 1440 grams, is given as Figure 5-9.

RF Cordwood Modules

A typical r-f cordwood module is shown in Figure 5-10. The dimensions are 3.15 in. long x 0.55 in. wide x 0.7 in. high. After component assembly, the module is tested and aligned, if necessary, and the metal cover is sealed to the header. The assembly is then potted using epoxy-glass foam.

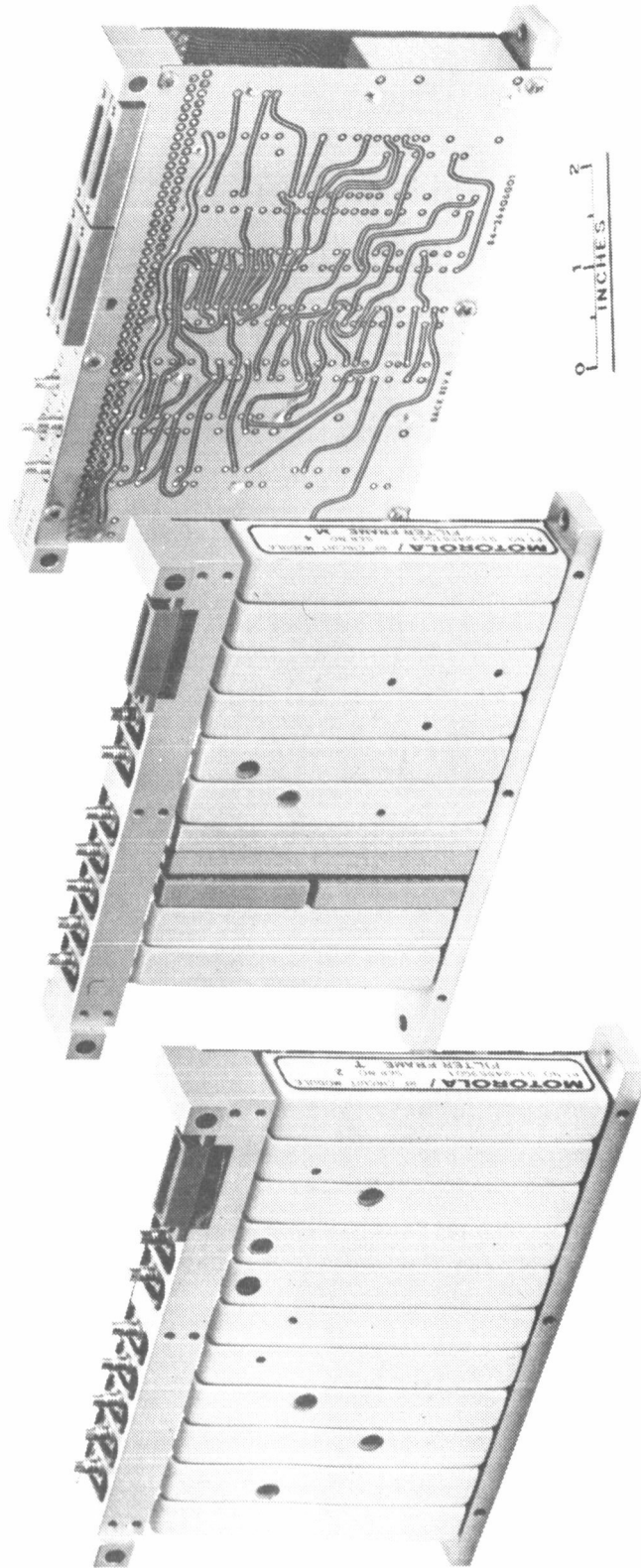
Digital Integrated Modules

Figure 5-11 shows the technique used in AROD for packaging "flat-pack" integrated circuit elements. Up to 20 flat packs are mounted in a module, 10 in each "U-Channel". Electrical interconnections are made by the circuit layers, which consist of thin (0.004 in.) "Kovar" clad mylar sheets, separated by 0.002 in. thick plain mylar sheets. Connections between flat-packs and header pins are made by resistance welding. The resulting package, after test, is then encapsulated with stycast to form the completed module which is 3.15 in. long x 0.35 in. wide x 0.7 in. high. Figure 5-12 is a photograph of a typical module.



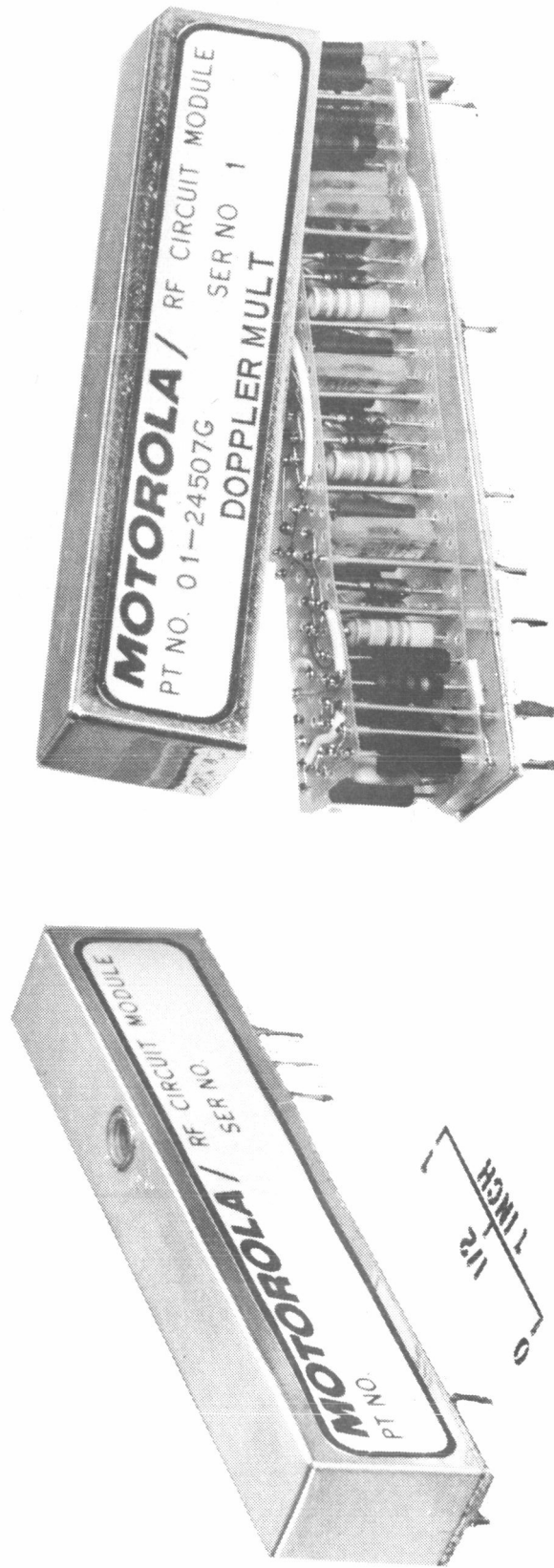
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Figure 5-8. R-F Converter



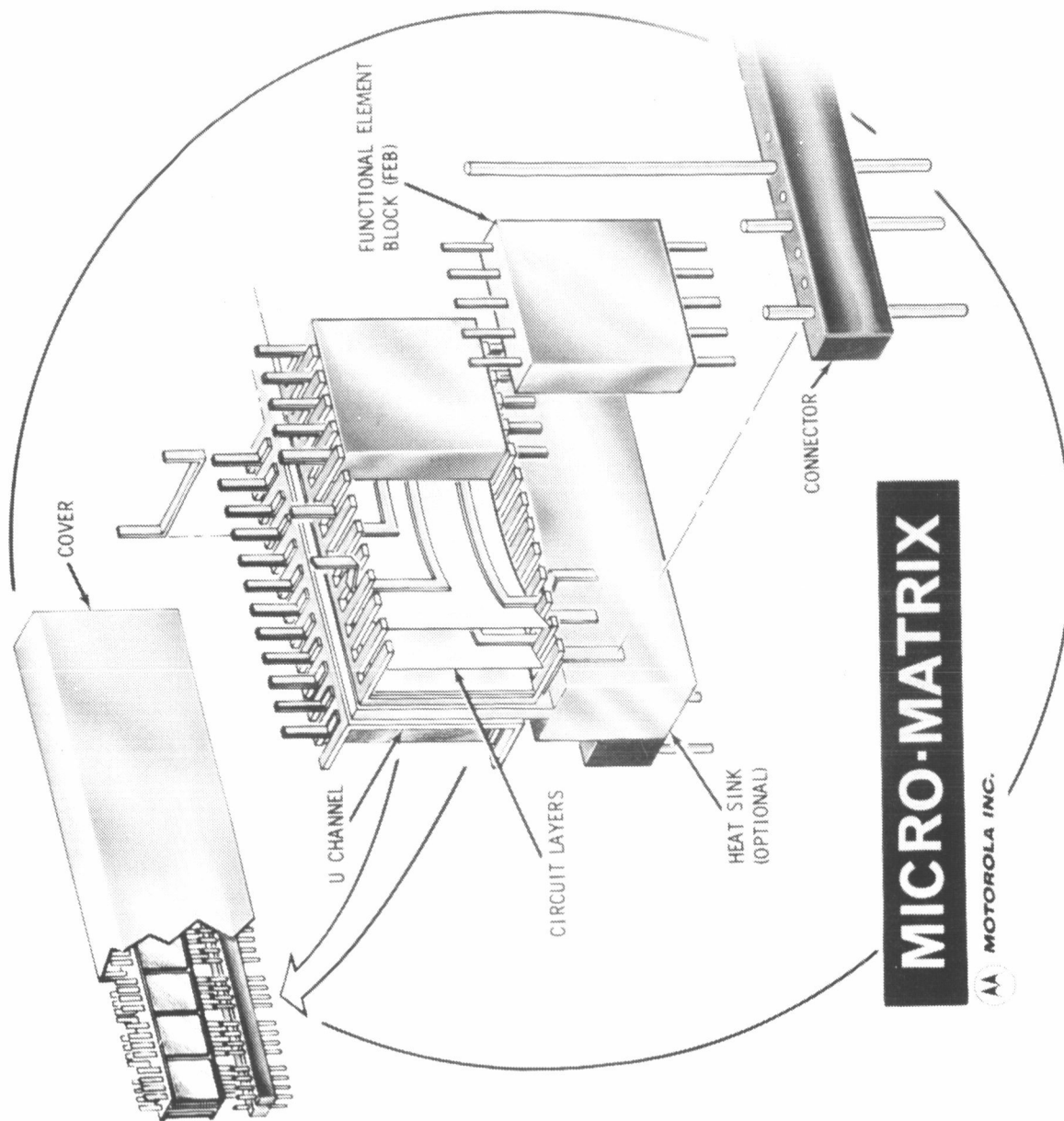
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Figure 5-9. Vehicle Tracking Receiver



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Figure 5-10. Typical R-F Cordwood Module



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Figure 5-11. Micro Matrix Technique

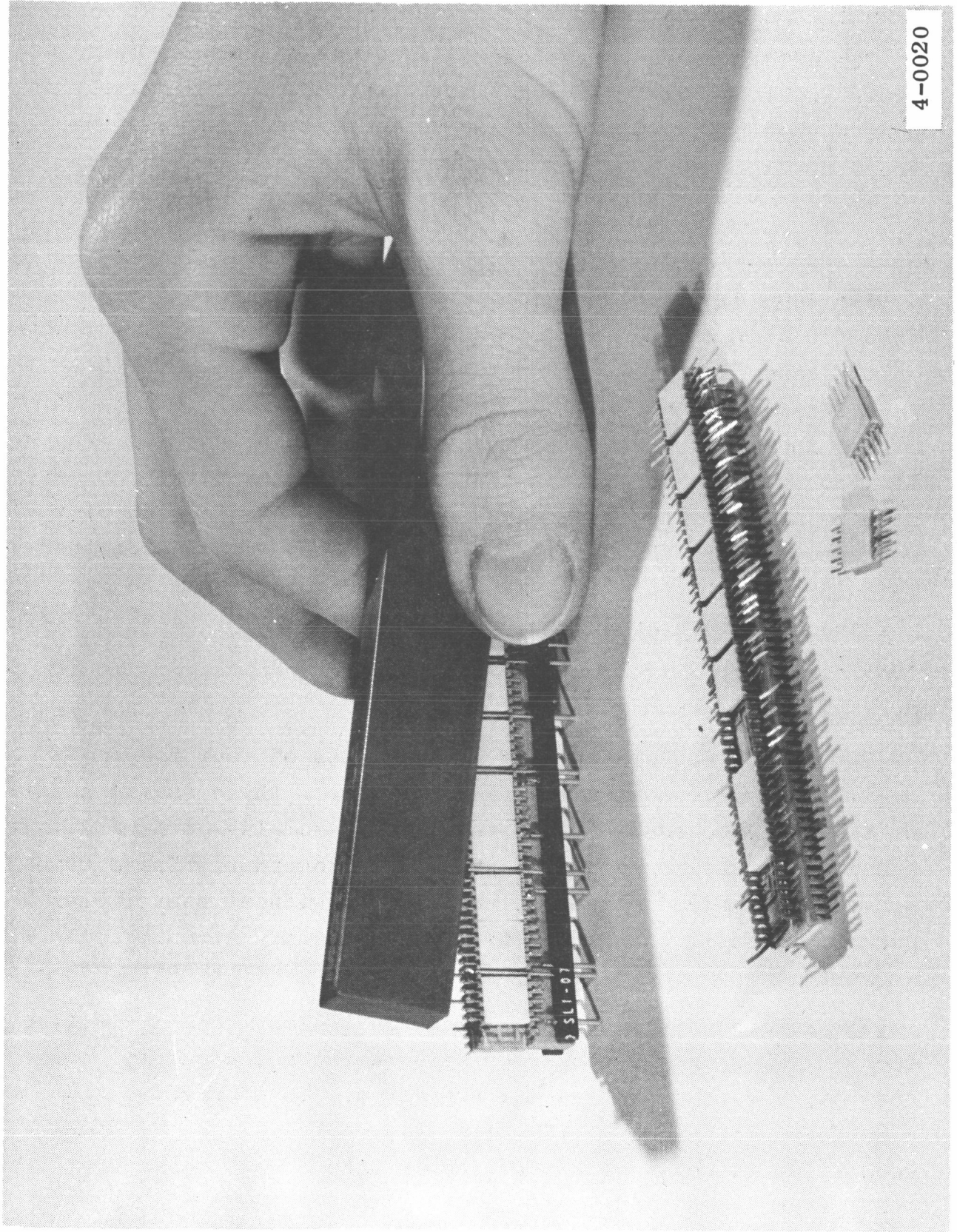


Figure 5-12. Digital Integrated Circuit Module

Frequency Synthesizer

The AROD frequency synthesizer consists of three frames, as shown in Figure 5-13, having a total weight of 1445 grams. It uses a combination of RF and cordwood modules. In addition, the 3.2 MHz frequency standard is installed on the center frame.

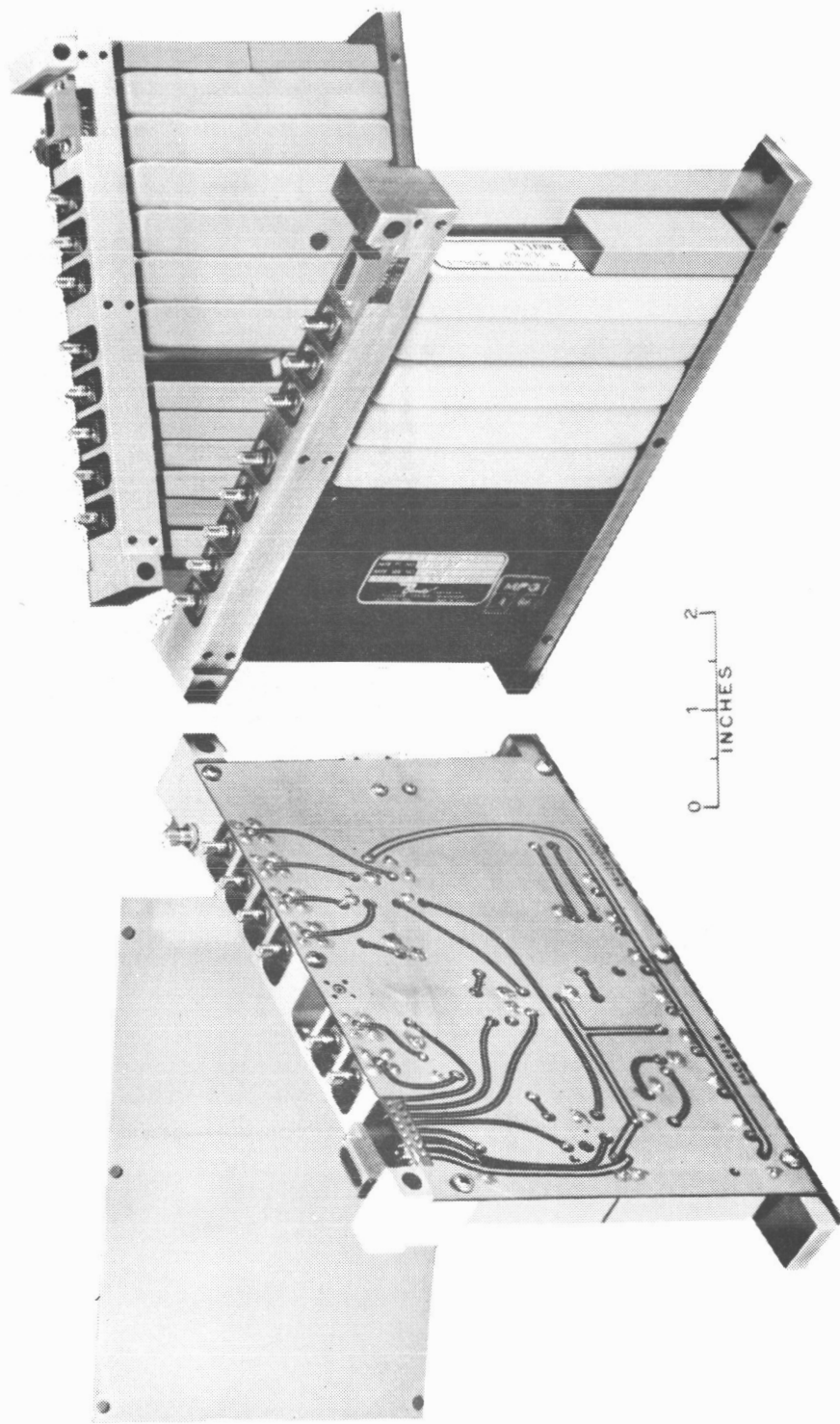
Distribution Amplifier

The AROD distribution amplifier, shown in Figure 5-14, is constructed differently from other portions of AROD. It is mounted on the base of Case 2 just below the coaxial connectors 2J1-2J10. The distribution amplifier accepts three r-f signal inputs from Case 1 and distributes them to their proper location in Case 2. Within the distribution amplifier, the three signals are buffered providing isolated outputs to each of the four receivers. The small (0.9 x 1 x 6 inch) case is divided into three isolated compartments with the components mounted on printed circuit boards within the compartments. The total weight is 131 grams.

Data Measurements

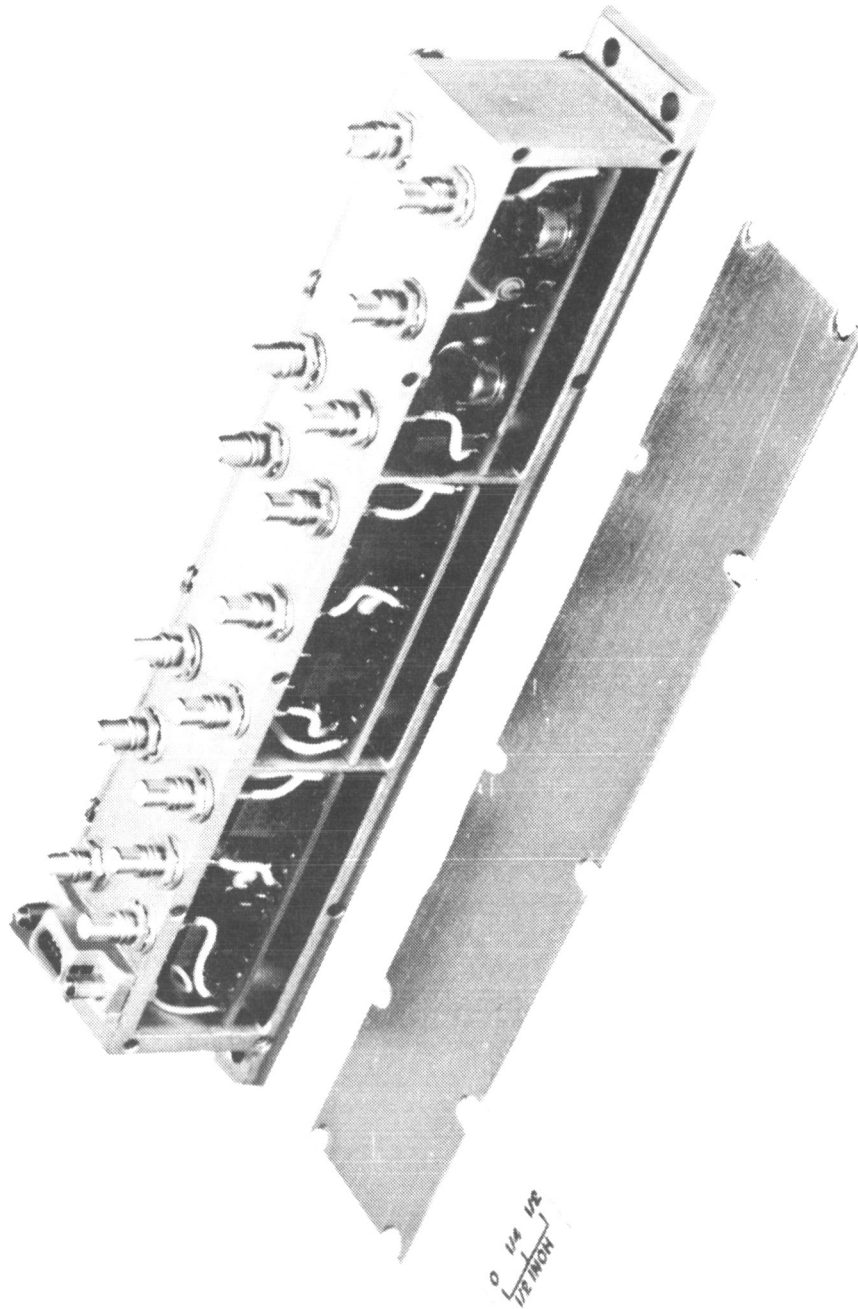
The data measurements subgroup consists of four frames of digital integrated circuits (Figure 5-15). These frames consist of two motherboards, with up to nine I/C modules per board. The I/C modules are spaced so they sandwich together. The method provides the added printed circuit paths without sacrificing packaging density, and results in an extremely strong, rigid assembly.

The subgroup includes the timing unit, four velocity extraction units, four range extraction units, the transmitter code control, and the data readout subsystem. This consolidation into a subgroup was made to alleviate the requirements of the interconnection harness. The four frames have a combined weight of 1635 grams.



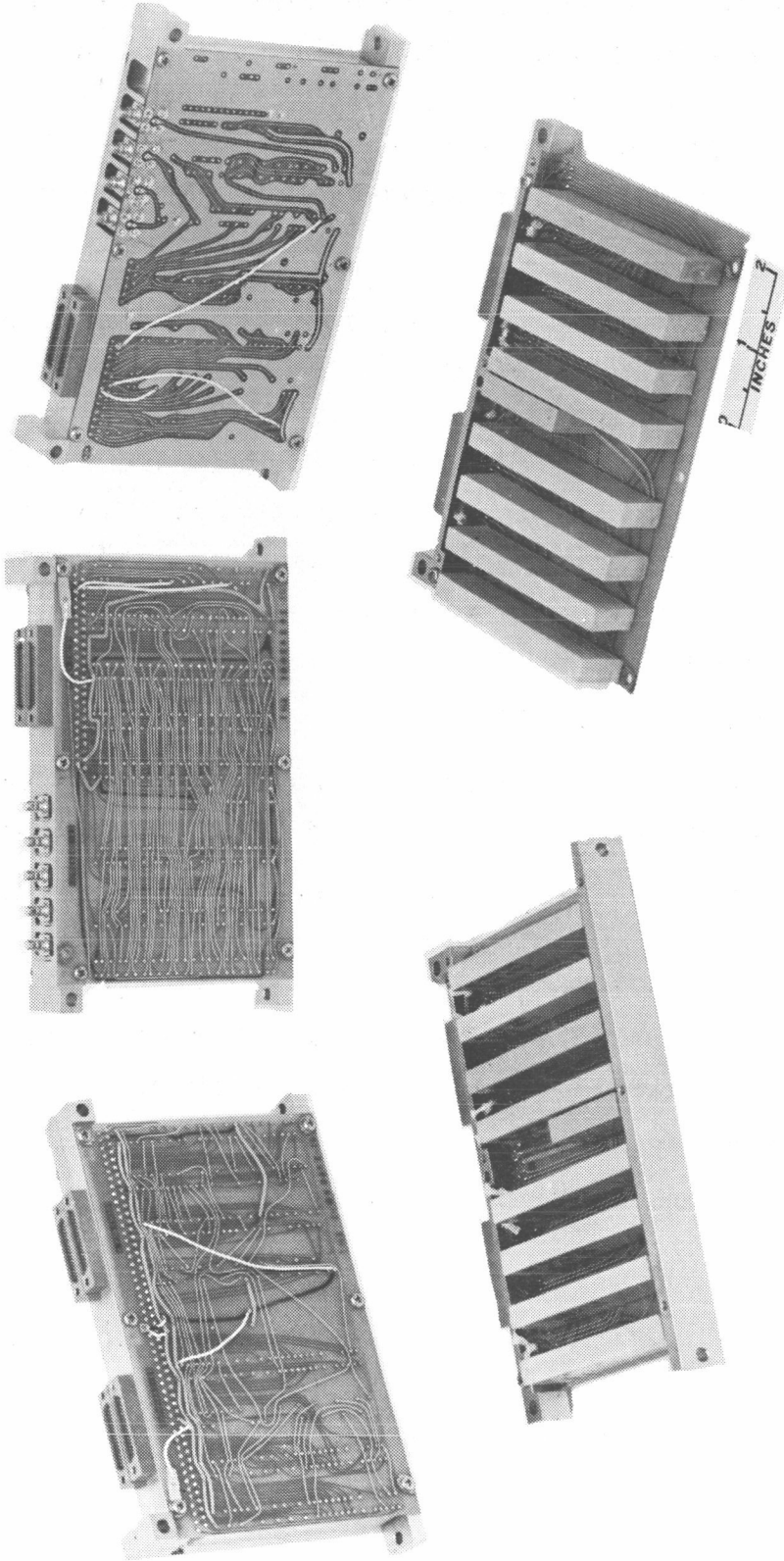
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Figure 5-13. Vehicle Frequency Synthesizer



6-2291

Figure 5-14. Distribution Amplifier



6-2895

Figure 5-15. Data Measurement Subsystem

System Control Logic

The AROD System Control Logic (Figure 5-16) consists of three frames of digital integrated circuits packaged with the double motherboard concept described above. One frame of the system control logic contains the magnetic memory. The three frames of the system control logic weigh 1152 grams.

D-C Power Converter

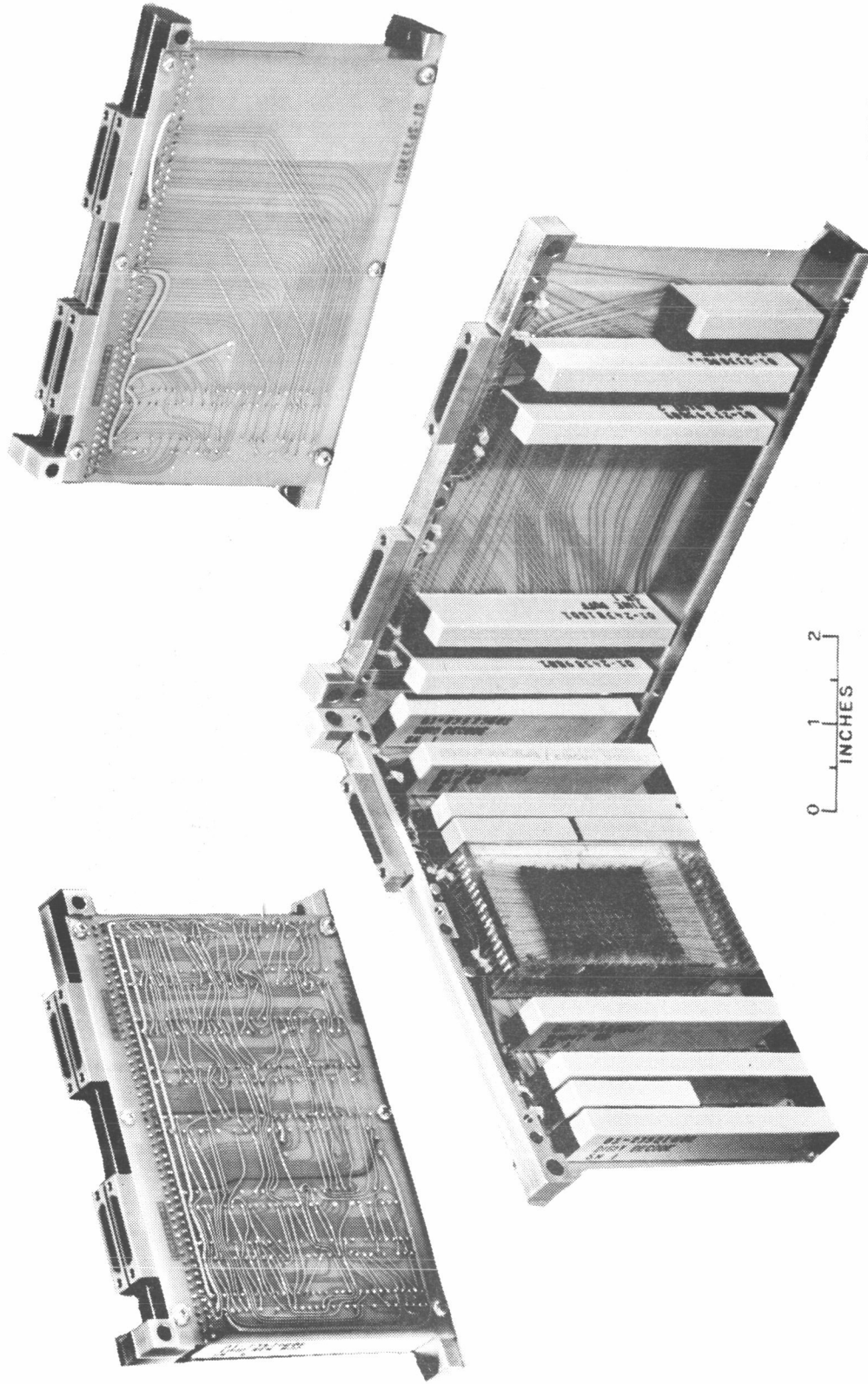
The d-c power converter is the largest (1.75 x 4 x 8 in.) and the heaviest (1545 grams) of all the subsystem frames. It is constructed in two halves (see Figure 5-17) which then sandwich together to form a closed frame. The enclosures are milled from solid aluminum stock with the base left quite heavy to serve as a heat sink for the power diodes and transistors. Power input leads and Case 2 power leads are shielded within metallic bellows to allow for dimensional tolerances.

5.2 STATION CONTROL TRANSMITTER

This section is the final Engineering Report on the Station Control Transmitter designed and developed for the AROD System.

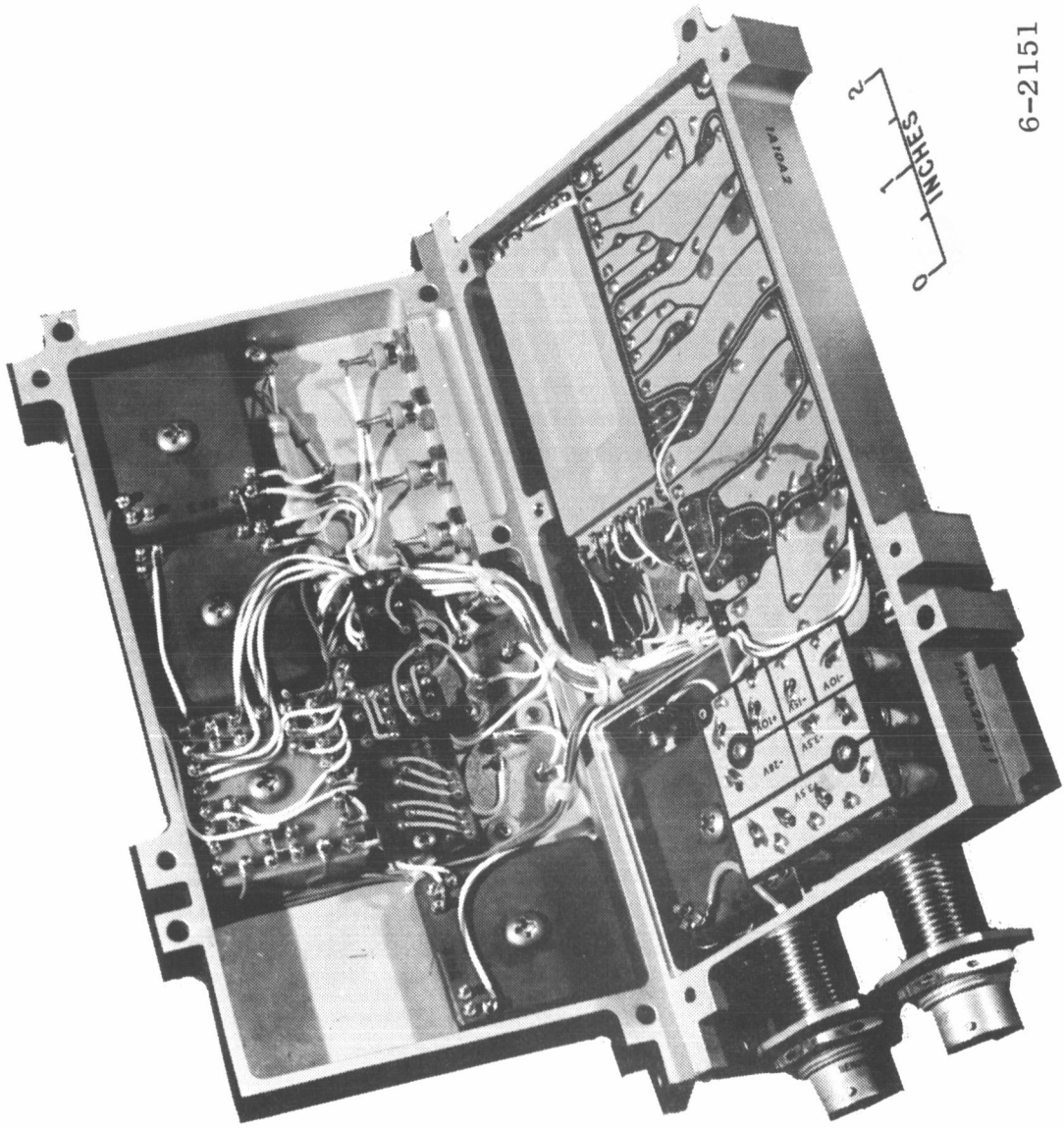
The transmitter (Figure 5-5) is the space vehicle portion of the VHF link between the vehicle and the ground station. Information is transmitted on this link to control the state of the ground stations. The link also provides a coherent carrier which is used for coarse acquisition and antenna tracking prior to lock-on to the S-band link.

The output frequency of the transmitter is 138 MHz at a power level of 6 watts. The carrier is phase modulated to a nominal index of 1.2 radians. Modulation linearity is $\pm 5\%$ of the best straight line for modulation indexes up to 1.5 radians. Complete specifications on the transmitter can be found in Document No. 12-25562J, Electrical Performance Requirements for the Station Control Transmitter.



6-2536

Figure 5-16. System Control Logic



6-2151

Figure 5-17. Vehicle Power Converter

5.2.1 Technical Approach

Figure 5-18 is a block diagram of the Station Control Transmitter. This section presents very briefly some of the technical considerations which resulted in the configuration shown in Figure 5-18.

The VCO carrier frequency reference for the Station Control Transmitter is at a frequency of 34.5 MHz. This requires that the transmitter provide a multiplication of 4 to obtain the proper output frequency of 138 MHz. This presents many implementation possibilities such as a varactor X4, a transistor X4, two varactor doublers, two transistor doublers, or a varactor doubler and a transistor doubler combination. Since present day transistors can multiply by two or four and still provide gain at these frequencies, active multipliers were selected as being more economical in both size and cost. The reduced number of components also results in better reliability.

Because of the stringent specifications on antenna conducted spurious emissions, two doublers were selected rather than a single X4 so that filtering could be provided between the multipliers. This greatly facilitates reducing the spurs occurring 34.5 MHz above and below the carrier to the specified 88 db down from the carrier level.

The phase modulation is applied prior to the multiplication so the index of modulation is multiplied also. This makes it easier to obtain large modulation indexes linearly. The phase modulator is followed by a limiter to strip off any unwanted amplitude modulation.

The modulation amplifiers, the buffer amplifier and the limiter all utilize hybrid integrated circuit differential amplifiers which had already been designed and developed for other uses on the project. This was done to minimize design time and conserve space.

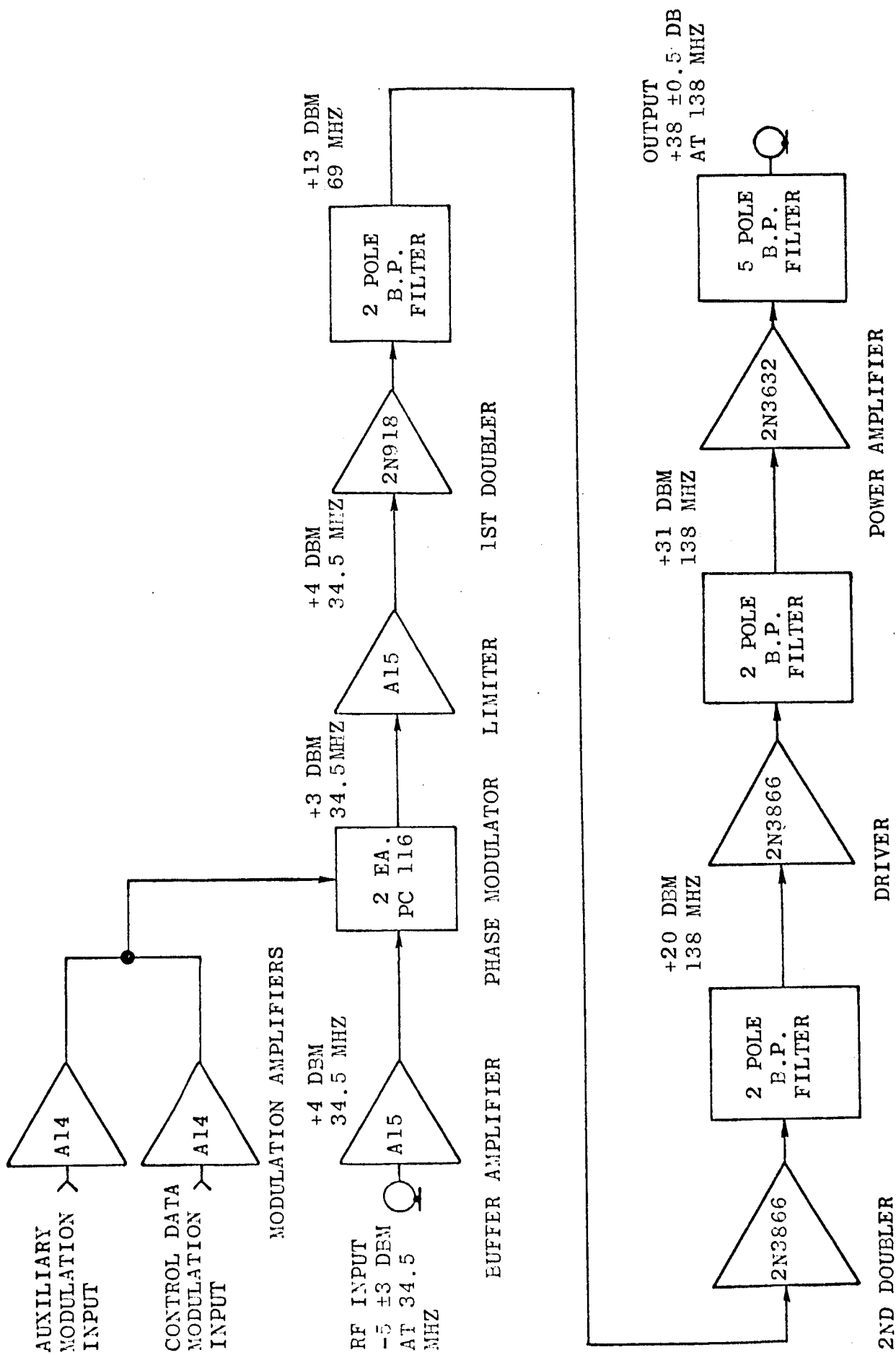


Figure 5-18. Station Control Transmitter, Block Diagram

5.2.2 Circuit Descriptions

A schematic diagram of the Station Control Transmitter is shown in Figure 5-19. A discussion of each of the stages shown in the schematic follows.

5.2.2.1 Phase Modulator Assembly

The Phase Modulator Assembly is a cordwood assembly containing the Buffer Amplifier, Phase Modulator and Limiter plus the base return, emitter by-pass and emitter resistor for the First Doubler. Cordwood construction techniques were used to conserve space.

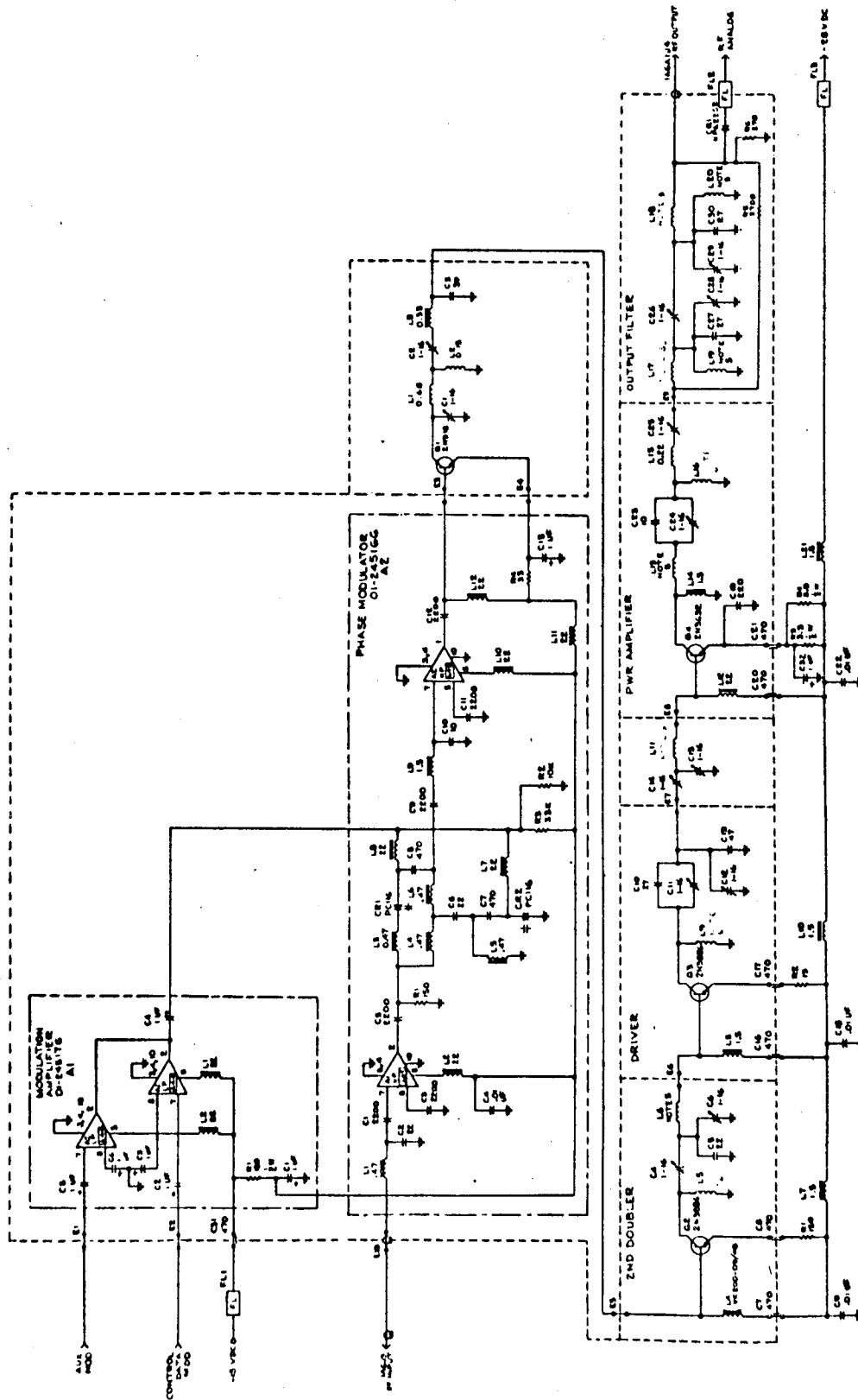
Buffer Amplifier

The Buffer Amplifier is a hybrid differential amplifier. It has a saturated output power level of approximately +4 dbm with a gain of 23 db. The input signal to the Buffer Amplifier is nominally -5 dbm at 34.5 MHz. Matching to the 50 ohm line is accomplished by L1 and C2 while DC decoupling is provided by C1, C3, and C5. This stage draws approximately 19 ma at -9 vdc.

Phase Modulator

The Phase Modulator is a bridged-T network in which CR1 is a voltage variable capacitor and CR2 is made to look like a voltage variable inductor through a quarter wave transmission line. Phase shift through the network then becomes a function of the bias voltage on CR1 and CR2. In the transmitter, the diodes are DC biased at -2 volts and the modulating voltage is AC coupled to them. The DC bias is to prevent the diodes from becoming forward biased when modulation voltage is applied.

A bridged-T network was selected as the phase shifter because of its ability to provide large phase shifts linearly while introducing a minimum of amplitude modulation. This circuit is capable of modulating the transmitter output to an index of greater than 4 radians linearly when driven directly. (See Figure 5-20) However, when used with the Modulation Amplifiers the capability for linear modulation drops to approximately 1.5 radians because



63-24515G

Figure 5-19. Station Control Transmitter, Schematic Diagram

of the limiting action of the amplifiers. A modulation index of 1.5 radians is more than adequate for this application.

Complete details on the design and operation of this type of phase modulator can be found in NASA Technical Report, Constant Amplitude, Variable Phase Filters, by L. J. Rogers and D. S. Helper.

Limiter

A hybrid integrated circuit differential amplifier was selected for the limiter stage because of its excellent limiting characteristic as well as for its ability to save space and design effort. The amplifier is operated deep into saturation to strip off any residual amplitude modulation and to provide a temperature stable signal source for the first doubler.

The saturated output of the limiter is approximately +4 dbm with a gain of about 23 db. The input level from the Phase Modulator is approximately +3 dbm putting the stage well into limiting.

Current drain of the limiter is about 19 ma at -9 vdc. The impedance match from the Phase Modulator to the Limiter is made by L4 and C10. DC isolation is provided by C9, C11, and C12. L12, R4, and C13 although packaged in the Phase Modulator Assembly are respectively the base return, emitter resistor and emitter by-pass for the first doubler stage.

5.2.2.2 Modulation Amplifier Assembly

The Modulation Amplifier Assembly consists of two identical amplifier stages. The two amplifiers provide the transmitter with two isolated modulation inputs. Low power hybrid integrated circuits are used in the two stages. Each amplifier has an output to input isolation of 40 db resulting in an isolation of greater than 80 db between modulation inputs.

Modulation voltage sensitivity of the transmitter is set by selecting resistors in voltage divider networks at the inputs of the amplifiers. The divider networks are located on the Printed

Circuit Board Assembly (01-26360G01). The two amplifiers operate on -15 vdc and draw approximately 7 ma each.

Resistor R1 in the Modulation Amplifier Assembly is simply a dropping resistor to reduce the -15 vdc to -9 vdc for use in the Phase Modulator Assembly. C1 provides filtering between the Modulation Amplifier Assembly and the Phase Modulator Assembly on the power supply line.

The hybrid integrated circuit differential amplifiers were selected for use as the modulation amplifiers because of their high output to input isolation, broad frequency response, and small size. However, because of their limiting action, the voltage swing into the Phase Modulator is limited which limits the modulation index at the transmitter output to about 1.5 radians if good linearity is to be maintained.

5.2.2.3 Multipliers and Power Amplifier

The First and Second Doublers, the Driver and the Power Amplifier utilize point-to-point wiring techniques because of the frequencies and power levels involved. All of the active elements are mounted directly to the chassis providing a heat sink to minimize the junction temperature rise. High Q components such as air core inductors are used to reduce losses in the high power stages.

First Doubler

The First Doubler is a 2N918 transistor driven in class C operation to produce harmonics. The two pole filter following the doubler selects the desired harmonic and makes the necessary impedance transformation into the following stage.

Input to the doubler is about +4 dbm at 34.5 MHz from the Limiter. The output of the doubler is +14 dbm at 69 MHz for a conversion gain of 10 db. Collector efficiency of the stage is approximately 16%, thus requiring a current of 15 ma at -9 vdc.

Second Doubler

This stage uses a 2N3866 transistor operated as a class C doubler having an output frequency of 138 MHz at a power level of +21 dbm. As originally designed, this stage had a conversion gain of 13 db, however, the output level of +27 dbm placed the driver stage too far into a power saturated condition resulting in inefficient operation and a high junction temperature. The emitter resistor of the doubler was, therefore, increased to 150 ohms to decrease the doubler output power to +21 dbm. The stage now draws approximately 11 ma at -28 vdc for a collector efficiency of 42%. A two-pole bandpass filter follows the doubler and provides the necessary impedance transformation to the driver stage.

A ferrite choke was used as the base return in the Second Doubler to improve the stability of the stage.

Driver

The Driver is a class C RF amplifier which provides slightly over 10 db of gain at 138 MHz. The output level is about +31 dbm (1.25 watts) and the stage draws 70 ma at -28 vdc. The active device is a 2N3866 transistor.

To ease design and test problems, the impedance transformation from the Driver to the Power Amplifier is made in two discrete steps. The first step is down to 50 ohms and the second step is down to the input impedance of the Power Amplifier (about 6 ohms). The two transformation steps also provide two poles of bandpass filtering between the stages.

Power Amplifier

The Power Amplifier is a class C amplifier using a 2N3632 transistor. This stage develops approximately 8 watts of power at a collector efficiency of 66% through the two pole filter and matching network formed by L13, L15, and L16 and C23, C24, and C25 into a 50 ohm load. However, the spurious outputs at this point were too high to meet the EMI specification, so an additional three poles of filtering had to be added to the output.

The three pole filter has an insertion loss of approximately 1 db at center frequency which reduces the transmitter output power to the required +38 dbm (6.3 watts).

Multiple emitter by-passing is used on the Power Amplifier to insure its stability and to improve the gain. The stage draws about 445 ma at -28 vdc which requires the use of two $\frac{1}{2}$ watt resistors in parallel in the emitter.

A monitor of the transmitter output power is provided by the detector circuit formed by R5, R6, CR1 and FL2. The detector circuit was placed at the front end of the output filter rather than at the output connector so the harmonics generated by the detector diode must pass through the output filter. With a transmitter output of 6 watts the detector circuit develops an RF analog voltage of approximately +3 vdc into a 1 K load.

5.2.3 Test Results

Table 5-1 and Figures 5-20 to 5-22 compare the performance of SN-1 Station Control Transmitter with the design specifications and with the Breadboard Transmitter performance.

5.3 CONTROL DATA MODULATOR

The Control Data Modulator uses the Control Data input and the sub-bit input to phase modulate a subcarrier of 18.75 kHz. The subcarrier is modulated in a manner such that an output data "1" level is represented by 18.75 kHz at -90 degrees for the first-half bit and 18.75 kHz at 0 degrees for the second-half bit. A data "0" level is represented by 18.75 kHz at +90 degrees for the first-half bit and 18.75 kHz at 0 degrees for the second-half bit.

5.3.1 Technical Approach

The digital portion of the Control Data Modulator is packaged in a standard AROD I/C module and an output filter section is mounted on the motherboard assembly. The motherboard assembly

TABLE 5-1. Performance of S/N 1 Station Control Transmitter

Parameter	Specification	0°C				+25°C		+52°C	
		B/B	S/N 1	B/B	S/N 1	B/B	S/N 1	B/B	S/N 1
Power Output	+38 ±0.5 dbm	+38.2 dbm	+38.26 dbm	+38.2 dbm	+37.6 dbm	+37.6 dbm	+37.6 dbm	+37.25 dbm	
Dynamic 3 db Bandwidth	2 MHz min	5 MHz	6 MHz	5 MHz	6 MHz	5 MHz	6 MHz	6 MHz	
-28v Current	550 ma min	485 ma	520 ma	495 ma	525 ma	470 ma	505 ma	505 ma	
-15v Current	80 ma max	56 ma	64 ma	58 ma	64 ma	58 ma	63.5 ma	63.5 ma	
Spurious Outputs									
103.5 MHz	-88 db min	>-96 db	-96 db	-94 db	-96 db	-96 db	-81 db	-81 db	
172.5 MHz	-88 db min	-88 db	>-96 db	-88 db	>-96 db	-90 db	-88 db	-88 db	
276.0 MHz	-60 db min	>-96 db	-76 db	>-96 db	-76 db	>-96 db	-76 db	-76 db	
414.0 MHz	-60 db min	>-96 db	-72 db	>-96 db	-72 db	>-96 db	-72 db	-72 db	
552 MHz	-88 db min	>-96 db	-92 db	>-96 db	-90 db	>-96 db	-90 db	-90 db	
690 MHz	-88 db min	>-96 db	-95 db	>-96 db	-95 db	>-96 db	-95 db	-95 db	
828 MHz	-88 db min	>-96 db	-92 db	>-96 db	-91 db	>-96 db	-92 db	-92 db	
966 MHz	-88 db min	>-96 db	-93 db	>-96 db	-93 db	>-96 db	-93 db	-93 db	
All Others	-88 db min	>-96 db	>-96 db	>-96 db	>-96 db	>-96 db	>-96 db	>-96 db	

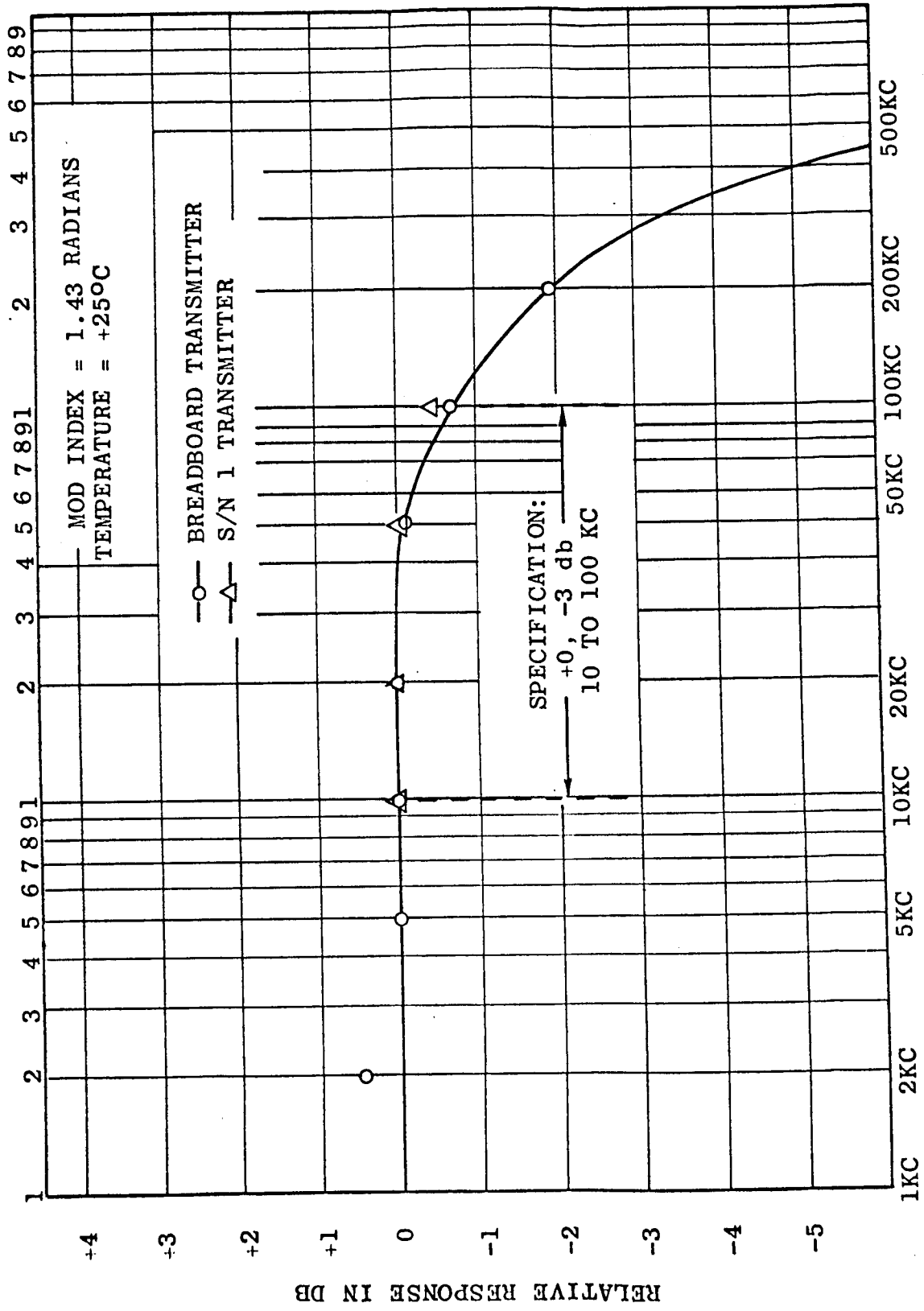


Figure 5-20. Modulation Frequency Response Station Control Transmitter

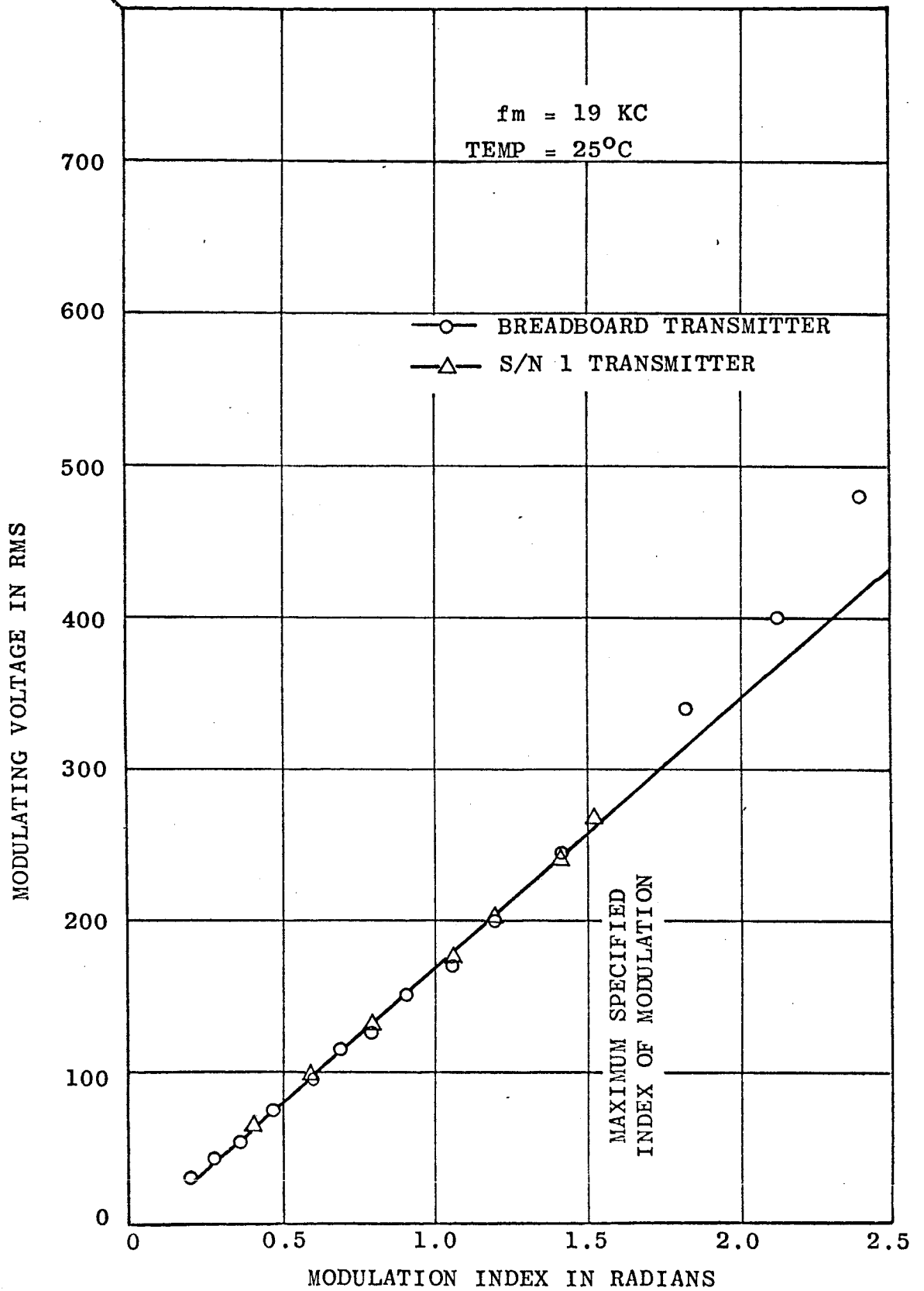


Figure 5-21. Modulation Linearity Station Control Transmitter

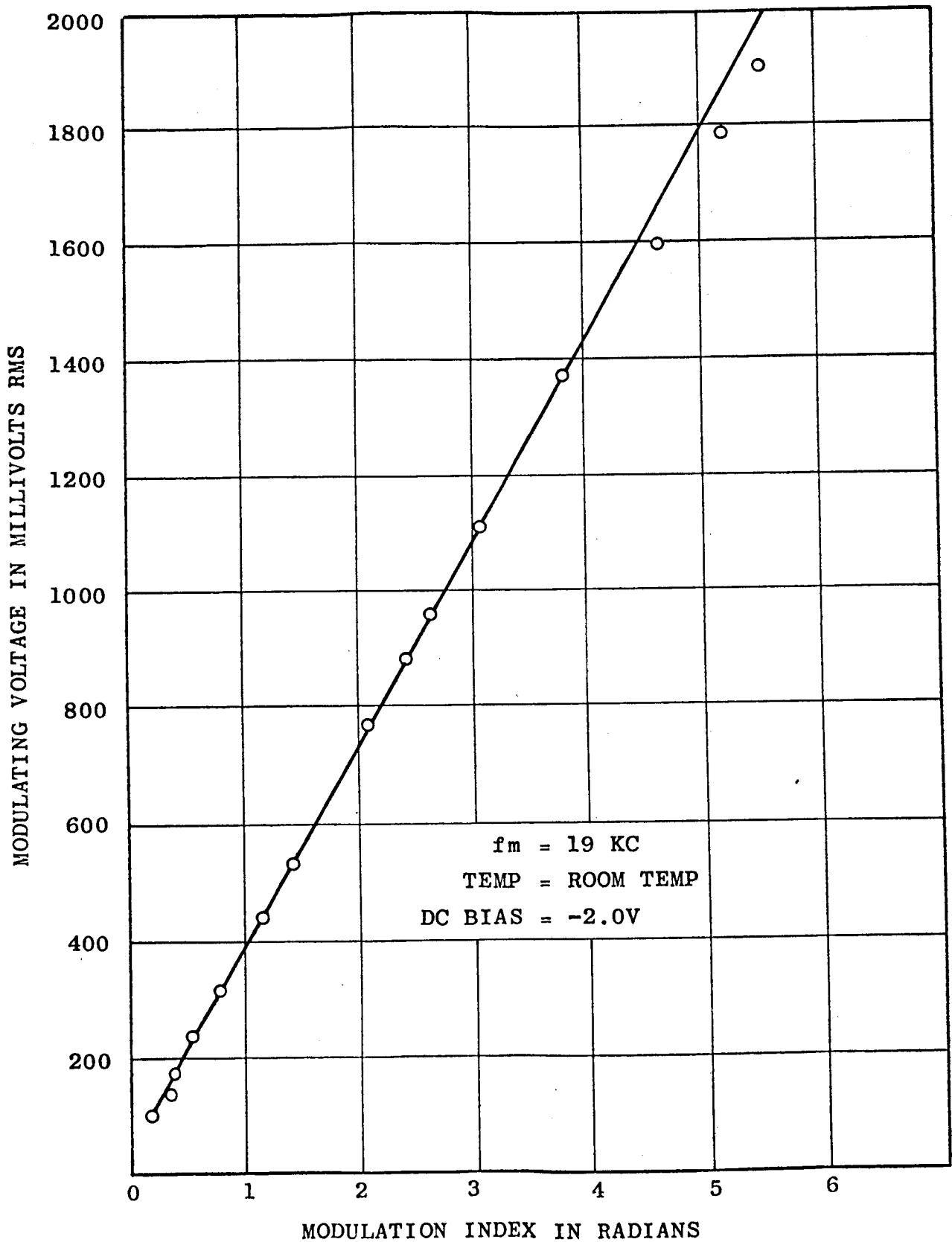


Figure 5-22. AROD Station Control Transmitter S/N 1 Modulation Linearity (without Modulation Amplifiers)

schematic diagram is shown in Figure 5-23 and the logic diagram for the I/C module is shown in Figure 5-24.

The digital logic portion of the Control Data Modulator was well defined and presented no design problems. The output filter section specifications were a delay time of $11 \mu\text{s} \pm 2 \mu\text{s}$ at 18.75 kHz and given attenuations at each of the first five harmonics of 18.75 kHz.

In the design effort both active and passive symmetrical bandpass filters were evaluated. These proved unsatisfactory because of the large variation in time delay with respect to small changes in component values. An inductor-input, π -section, low pass filter was chosen because of its relatively insensitive time delay at all frequencies less than the cutoff frequency and its non-critical component values.

5.3.2 Logic Description

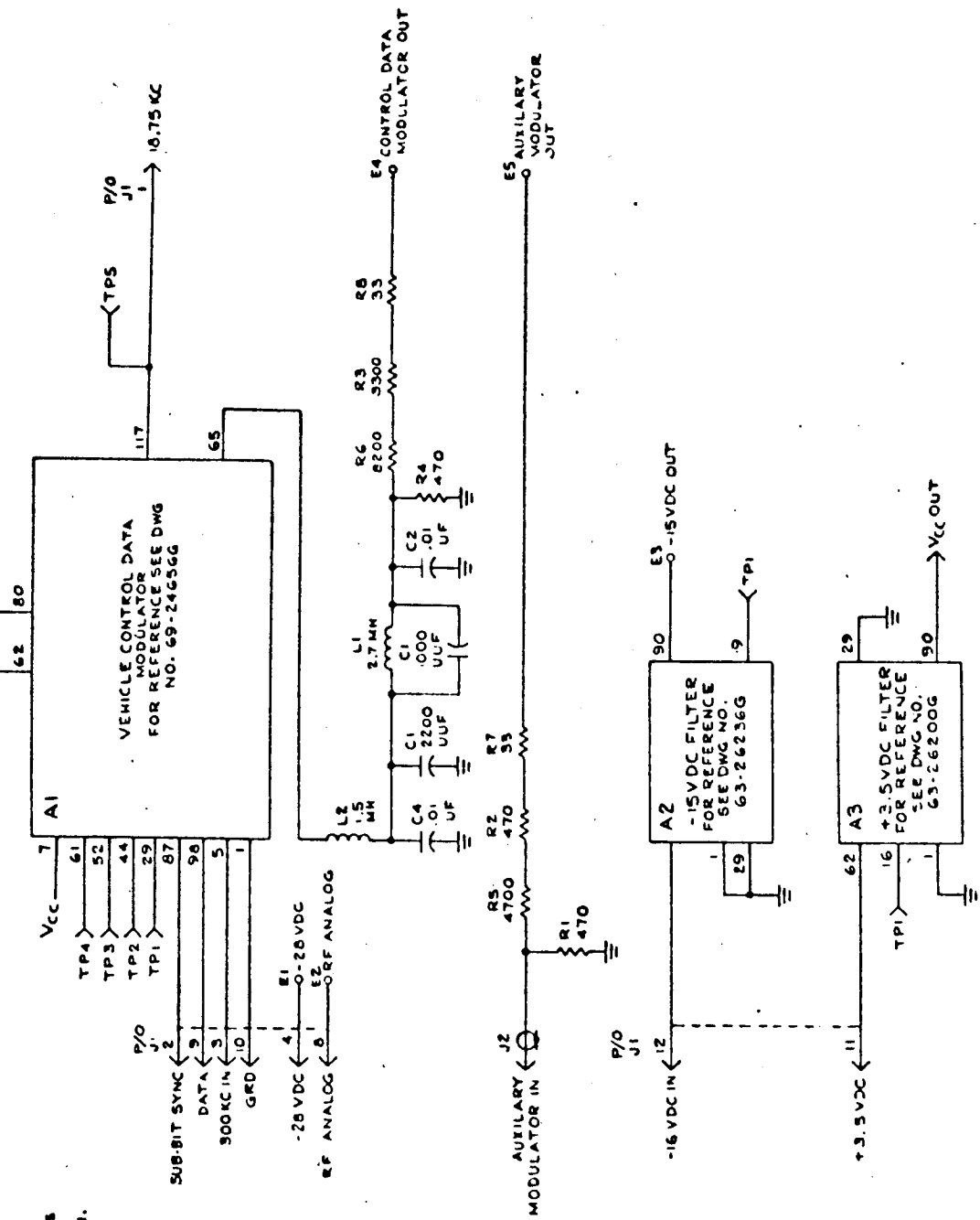
The 300 kc signal from the Frequency Synthesizer is shaped by a hybrid interface circuit and is divided by 16 to form 18.75 kHz at 0 degrees (B) and shifted to form 18.75 kHz at +90 degrees (A) and 18.75 kHz at -90 degrees (C). These signals are then gated by the data input (D) and the sub-bit clock (SB) to form the sub-carrier output modulation.

$$\text{Output} = A \cdot \overline{\text{SB}} \cdot D + B \cdot \text{SB} + C \cdot \overline{\text{SB}} \cdot \overline{D}$$

This output is capacitively coupled through a 510 ohm resistor to the output filter. The 510 ohm resistor provides the proper source resistance for the output filter.

5.3.3 Output Filter Description

The output filter section is made up of L2, C4, C1, L1, C3, C2, and R4. The input section to the filter, L2, C1, and C4, provide the first roll off frequency at 42 kHz while L1 and C3 provide a notch at 94 kHz and L1 and C2 maintain the attenuation above the notch frequency. Resistor R4 is the filter termination while resistors R6, R3, and R8 are selected to provide the proper modulation voltage sensitivity of the transmitter.



- NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH TAGAL.
 2. ALL RESISTORS ARE IN OHMS 2% PCT, 1/4 WATT.

Figure 5-23. Station Control Transmitter, Motherboard Schematic Diagram

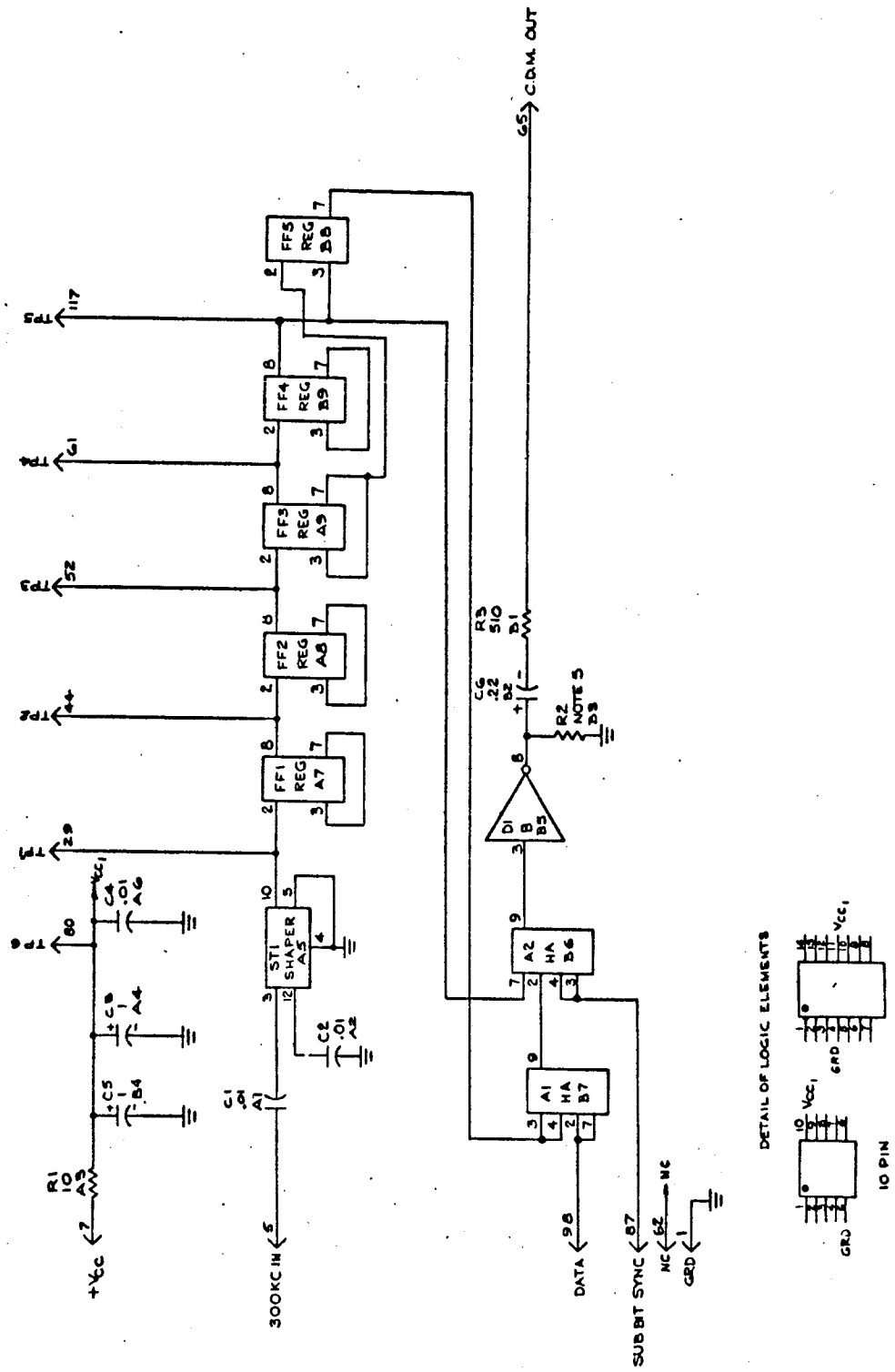


Figure 5-24. Station Control Transmitter, I/C Module Logic Diagram

5.3.4 Test Results

The digital portion of the Control Data Modulator imposes no speed or loading problems for the logic family and is easily implemented as shown in Figure 5-24.

Original calculations on the output filter did not show that the third harmonic of 56 kHz required additional attenuation above its attenuated component in the square wave itself. Subsequent calculations have shown that the 56 kHz component requires 21 db of attenuation. This is approximately 10 db greater than the present filter provides.

Evaluation by the System Analyst resulted in the decision that this particular discrepancy did not warrant redesign at this time.

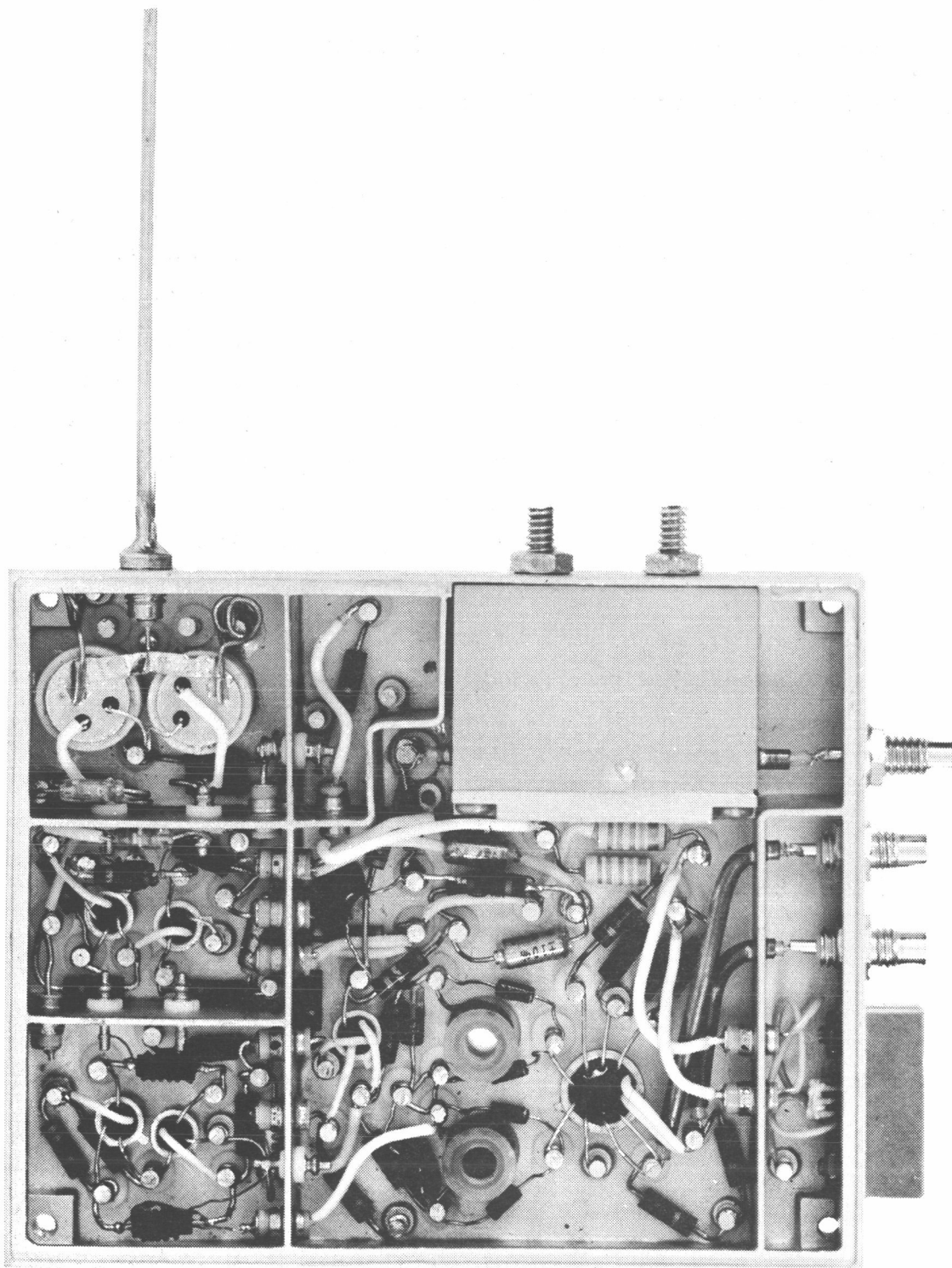
The Control Data Modulator requires 155 mw of power out of the 3.5 vdc supply.

5.4 TRACKING TRANSMITTER

The transmitter is the space vehicle portion of the S-band link between the vehicle and ground stations. The modulation on this link is the range modulation signal to be demodulated by all ground stations which have been acquired during that orbital pass.

The transmitter is capable of operating over the entire output frequency range of 2200 MHz to 2450 MHz. The output frequency is varied by changing the input carrier frequency reference and by retuning where necessary. The input frequency can be varied in steps of 6.25 kHz and the output frequency which is the 64th harmonic of the input frequency is varied in steps of 400 kHz. This provides approximately 625 separate channels.

The output frequency designated for the transmitter is 2214 MHz at a power level of 10 watts. The carrier is biphase modulated ($\pm 11.25^\circ$) with the PN range code at 277 MHz and multiplied times eight to 2214 MHz with $\pm 90^\circ$ phase modulation. Figures 5-6 and 5-25 are photographs of the AROD Vehicle Tracking Transmitter.



6-1110

Figure 5-25. Phase Modulation and Power Amplifier of Vehicle Tracking Transmitter

The transmitter was developed as three separate entities:

1. Phase Modulator and Power Amplifier
2. X8 S-Band Frequency Multiplier
3. TWTA.

The transmitter (with the exception of the TWTA) is packaged in a frame assembly physically located in Case 1 of the vehicle-borne equipment. The outside dimensions of the frame are 0.9" x 4" x 6.2" and the weight is 399 grams. The 2214 MHz signal is amplified to +10 dbm in the frame assembly and then delivered to the TWTA assembly which is a separate package where the signal is amplified to +40 dbm. The frame assembly operates from the system supply voltages (-10 v at 90 ma and +10 v at 40 ma) consuming a total power of 1.3 watts. The Hughes TWTA has its own separate power supply which operates from 60 cps AC at 110 volts.

Complete specifications of the transmitter can be found in Document No. 12-25564F, Electrical Performance Requirements for the Vehicle Tracking Transmitter.

The Hughes TWTA is an interim device for the present AROD configuration and was a subcontracted item.

5.4.1 Technical Approach

The Vehicle Tracking Transmitter performs the following functions:

1. Multiplies the output frequency of a VHF VCO up to S-band
2. Provides biphase modulation of the carrier, and
3. Amplifies the modulated signal up to a level of approximately 10 watts.

Figure 5-26 is the basic block diagram of the transmitter.

5.4.2 Functional Description

The following are brief functional descriptions of each of the major divisions of the Vehicle Tracking Transmitter in order of the serial signal flow. The divisions consist of the X8 UHF

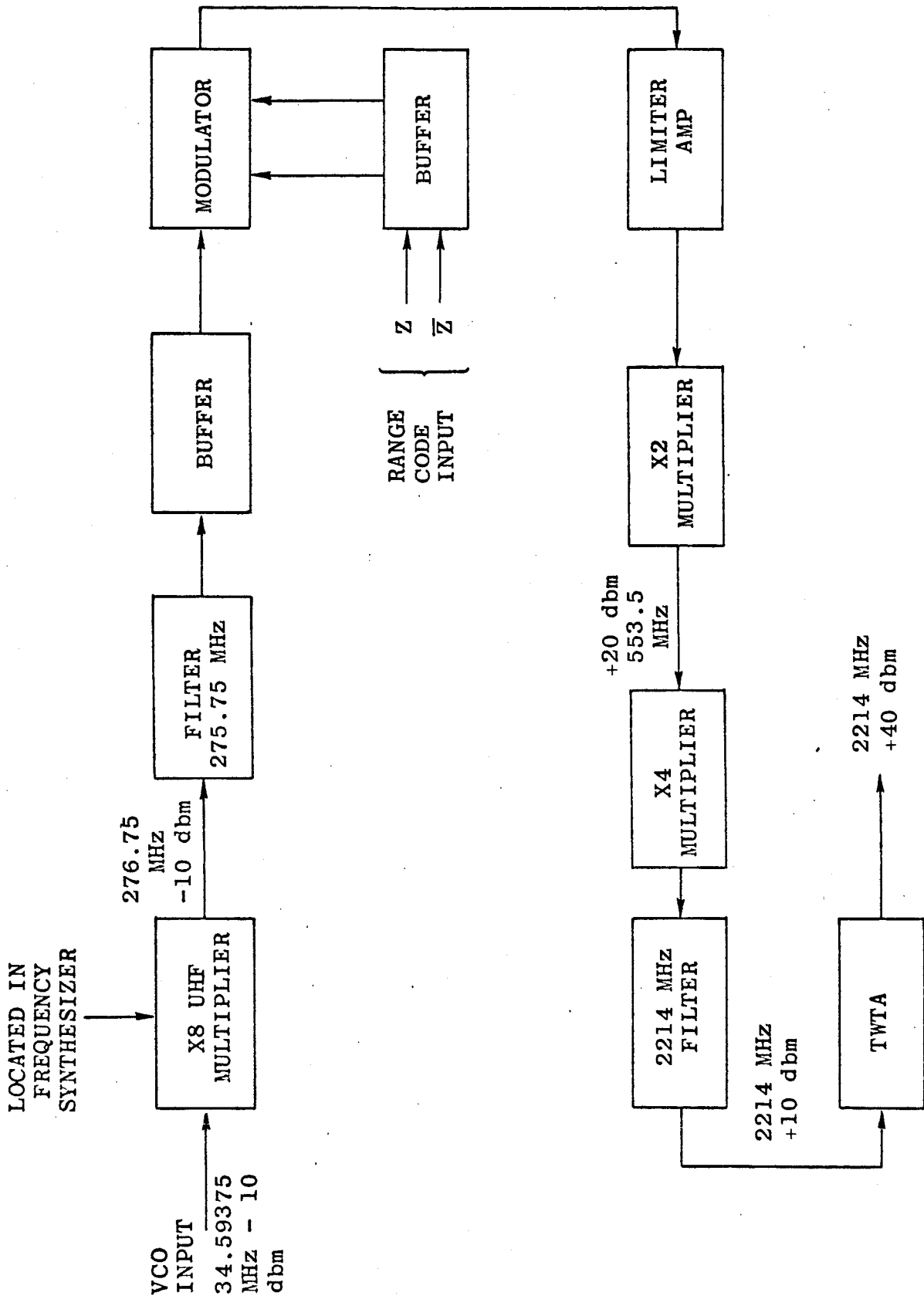
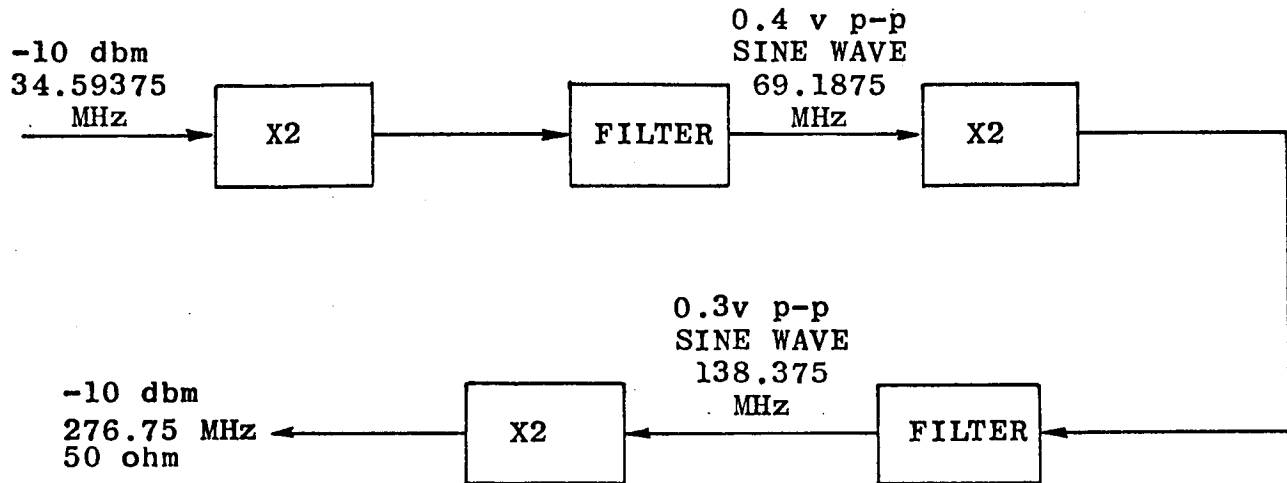


Figure 5-26. Vehicle Tracking Transmitter, Block Diagram

Multiplier, Phase Modulator, Limiter Amplifier, X2 Multiplier, X4 Multiplier, and Traveling Wave Tube Amplifier.

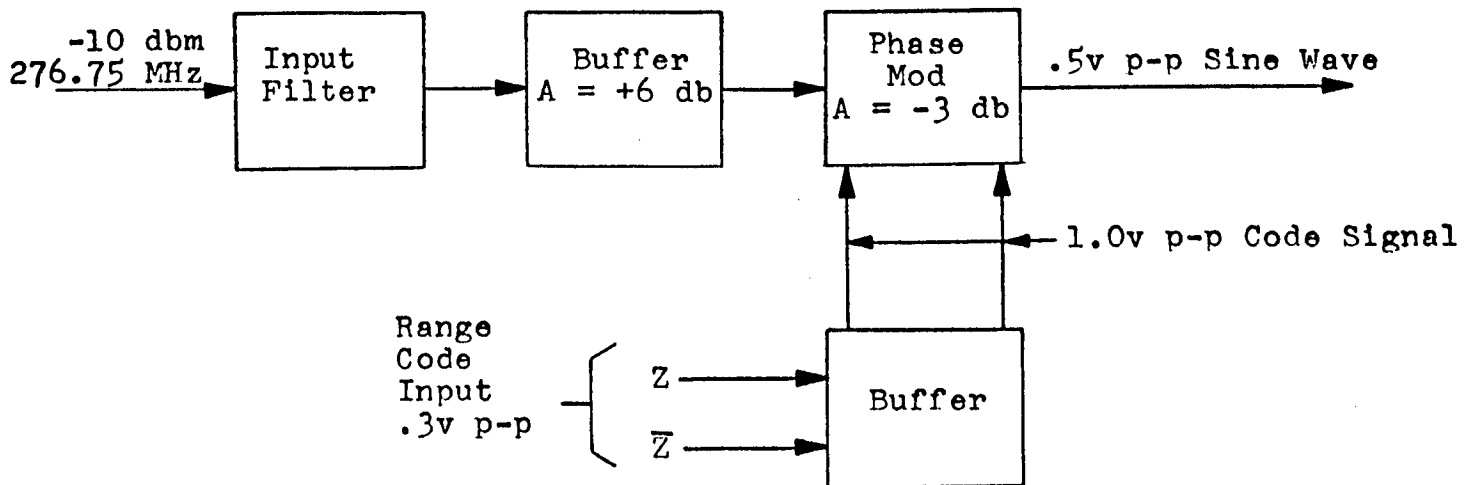
5.4.2.1 X8 UHF Multiplier (Located in the Frequency Synthesizer)

The functional breakdown of the multiplier is given below.



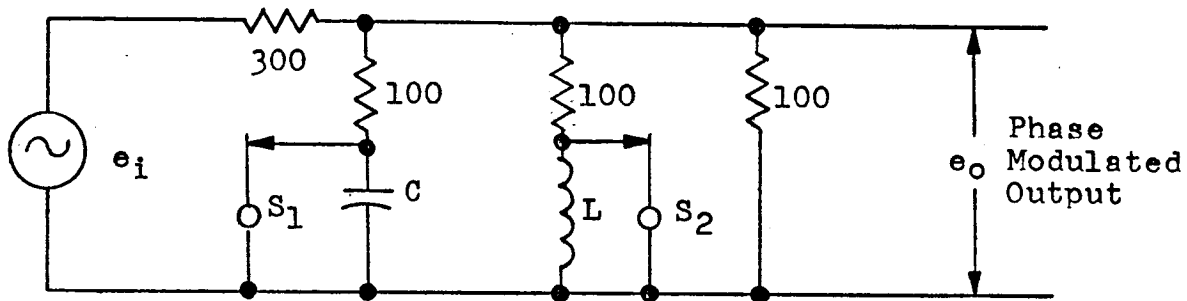
This multiplier is a broad band multiplier utilizing the Differential Amplifiers (A-44) and a pair of diodes to function as a full wave rectifier. This technique provides for a broad band frequency multiplication requiring a minimum of filtering. Additional filtering of the output signal is provided in the phase modulator section with a two pole helical resonator.

5.4.2.2 Phase Modulator



The phase modulator input circuit includes a two pole helical resonator filter and a buffer stage before the phase modulation. The input filter is required to improve the spectral purity of the incoming signal from the X8 UHF Multiplier. The required phase modulation at this point is $\pm 11.25^\circ$. This modulation index gives the desired $\pm 90^\circ$ after a multiplication factor of eight as required to increase the frequency to S-band.

The basic technique employed for the biphas modulation is given below. The impedances are approximate values that appear in the actual circuit.



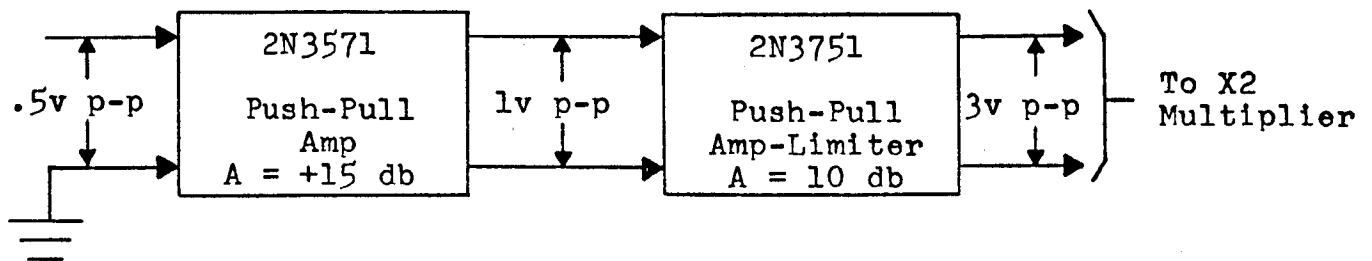
S_1 and S_2 are hot carrier diode switches operated such that one switch is open while the other switch is closed. S_1 and S_2 are operated such that the switching transient resulting in the abrupt change in current in the diodes is essentially cancelled out minimizing the distortion caused by the switching transient. The values of L and C are chosen to give the required phase modulation index with a minimum of amplitude components.

This technique of modulating at a low frequency and at a low power level is fairly easy to implement and the required stability and speed are easily achieved. As of mid-1965, no technique existed for modulation at a higher power level and at a higher frequency so that the required switching speed could be accomplished.

If it has been possible to perform the modulation at this higher power and frequency, the signal handling after modulation

would have been only a minor problem. With the technique employed the modulation was relatively simple but the signal handling after modulation became difficult. The problems arise from the fact that a modulation bandwidth of greater than 40 MHz must be preserved through a two-stage amplifier, a X2 transistor multiplier and a X4 diode multiplier. The bandwidth of this signal processing chain must be such that the spectral distortion is very low over the required information bandwidth.

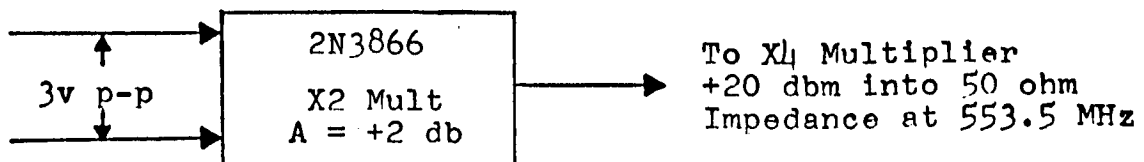
5.4.2.3 Limiter Amplifier



This section consists of a two-stage push-pull amplifier. The push-pull arrangement is used to give a very broad band amplifier with low distortion limiting characteristics. The actual gain of the two stages when operated in the linear mode is approximately 35 db.

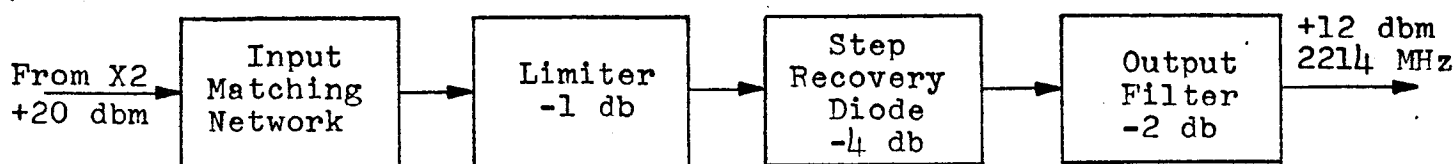
The limiter is required to insure that no amplitude distortion is present on the input to the step recovery diode. The amplitude distortion occurs during the time the phase is changing from the one state to the zero state (or zero to one) due to the finite bandwidth of the input matching network.

5.4.2.4 X2 Multiplier



This multiplier is a broad band push-push doubler. The push-push arrangement provides an output with the major component of power at the second harmonic of the input frequency. The fundamental component appearing on the output is approximately 30 db below the desired harmonic.

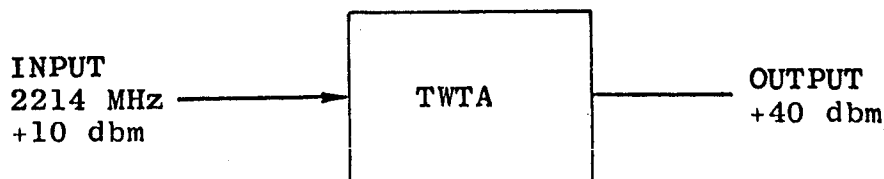
5.4.2.5 X4 Multiplier



The input matching network consists of a two-pole, low pass filter with a cut off frequency of approximately 700 MHz followed by a π -section matching network. The overall bandwidth of the matching network and input filter is approximately 20% of the center frequency.

The frequency multiplication is accomplished with a HPA 0241 step recovery diode with self bias. The desired harmonic (4th) is selected with a 4-pole, strip-line filter with approximately 4% bandwidth. The strip line filter elements are capacitive loaded on the high impedance end to suppress odd order modes and to provide for tuning of the filter to the desired center frequency.

5.4.2.6 Traveling Wave Tube Amplifier



This amplifier is a broad band traveling-wave tube amplifier having a linear gain of over 30 db and a bandwidth of greater than

100 MHz. The +10 dbm input signal to the TWTA from the X4 Multiplier is sufficient to drive the amplifier into limiting; the small amount of residual AM occurring during the phase modulation switching is removed by the limiting action of the TWTA. The amplitude wave form is shown in Figure 5-27.

Figure 5-28 is an electrical schematic diagram of the Vehicle Tracking Transmitter.

5.4.3 Test Results

Figures 5-29 through 5-36 give a comparison of the Vehicle Tracking Transmitter performance versus the design specifications and with the breadboard transmitter performance. The Electrical Test Procedure for the Vehicle Tracking Transmitter is contained in Document No. 12-24602G.

5.5 VEHICLE TRACKING RECEIVER

The Vehicle Tracking Receiver is composed of four subdivisions described in the following sections. These are:

1. Frequency Converter, common to all channels
2. Carrier Tracking Loop
3. Modulation Tracking Loop
4. Receiver Code Control.

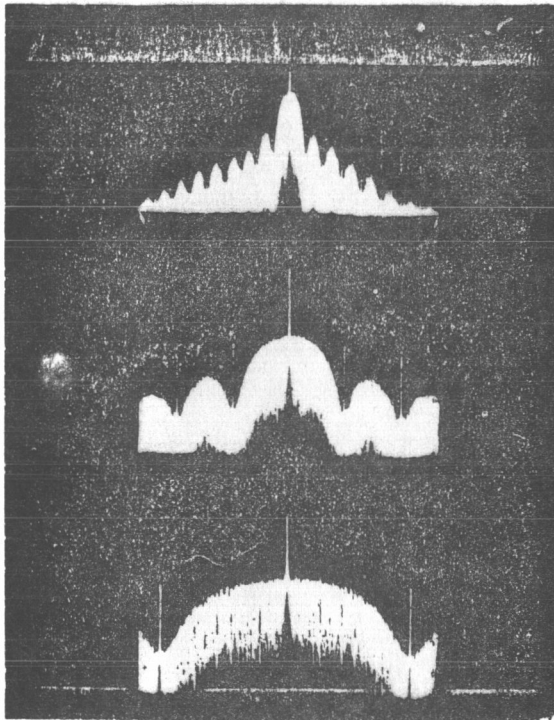
Items 2 and 3 are described under the common heading of Tracking Subsection.

Reference 6 provides a comprehensive report on the design and evaluation of the prototype Vehicle Tracking Receiver. The reader should refer to that report for the overall receiver design information.

5.5.1 AROD Frequency Converters

This section is a final summary of design, fabrication and testing of both the vehicle and transponder frequency converters. It contains the initial project objectives, what was accomplished,

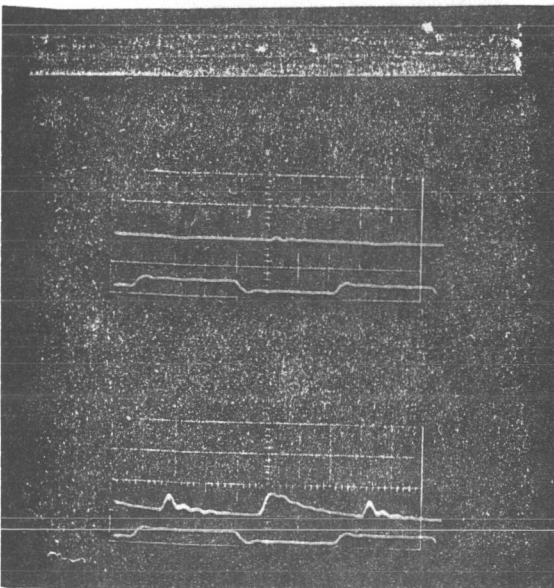
FINAL OUTPUT OF PHASE MODULATOR AND
TWTA WITH PN RANGE CODE MODULATION



Horizontal = 100 MHz Full Scale
Vertical = 70 db Full Scale

Horizontal = 30 MHz Full Scale
Vertical = 70 db Full Scale

Horizontal = 16 MHz Full Scale
Vertical = 70 db Full Scale



AMPLITUDE MODULATION - TOP TRACE
MODULATION INPUT - BOTTOM TRACE

Amplitude modulation on output
of TWTA (1 db/division vertical,
50 nanoseconds/division horizontal)

Amplitude modulation on output of
phase modulator and X8 multiplier
(Same scale as above)

Figure 5-27. TWTA Waveforms

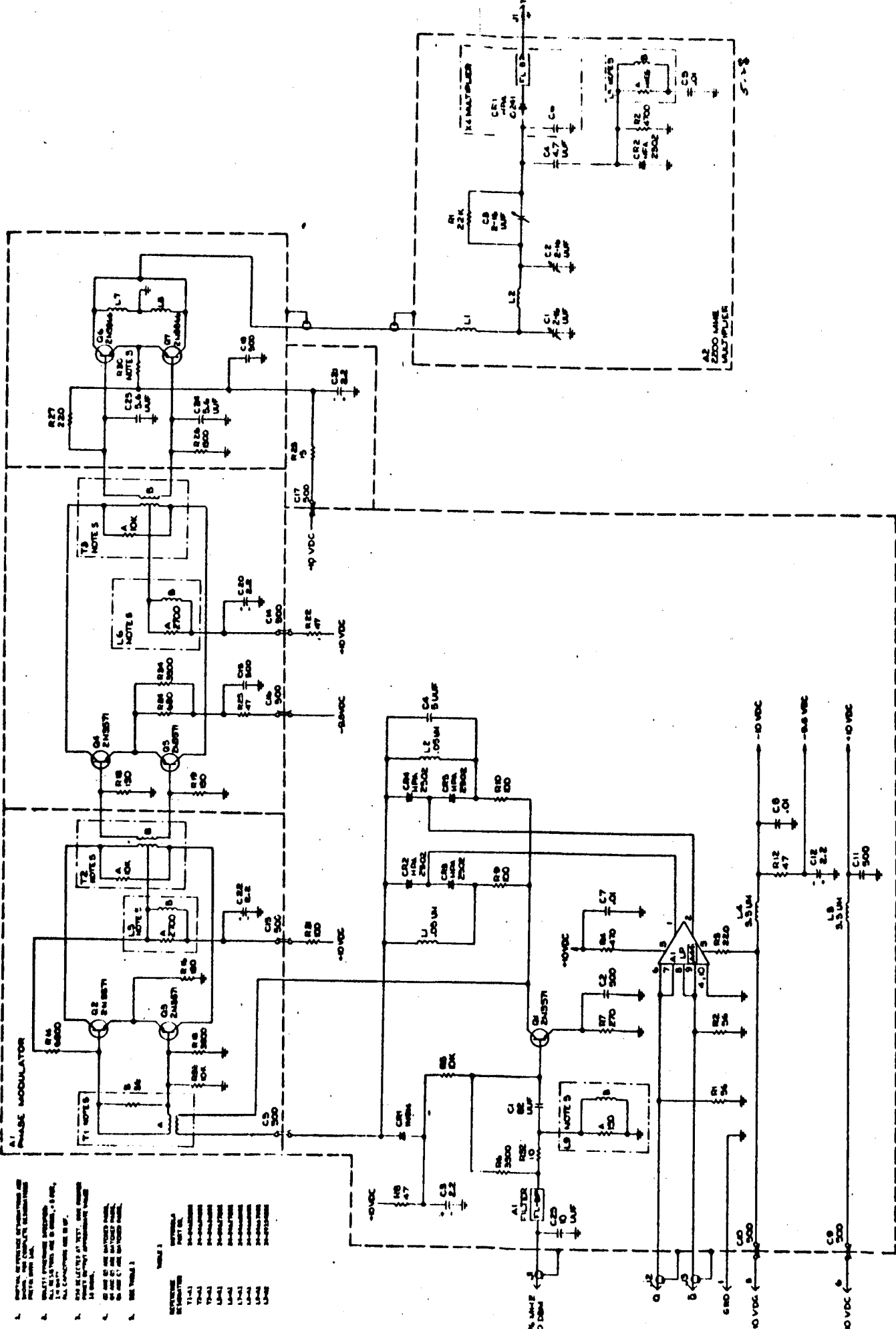


Figure 5-28. Vehicle Tracking Transmitter, Schematic Diagram

Figure 5-29.

Relative Side band
Power Vs Modulation
Frequency for square
wave modulation.

$$f_0 = 2216 \text{ MHz}$$

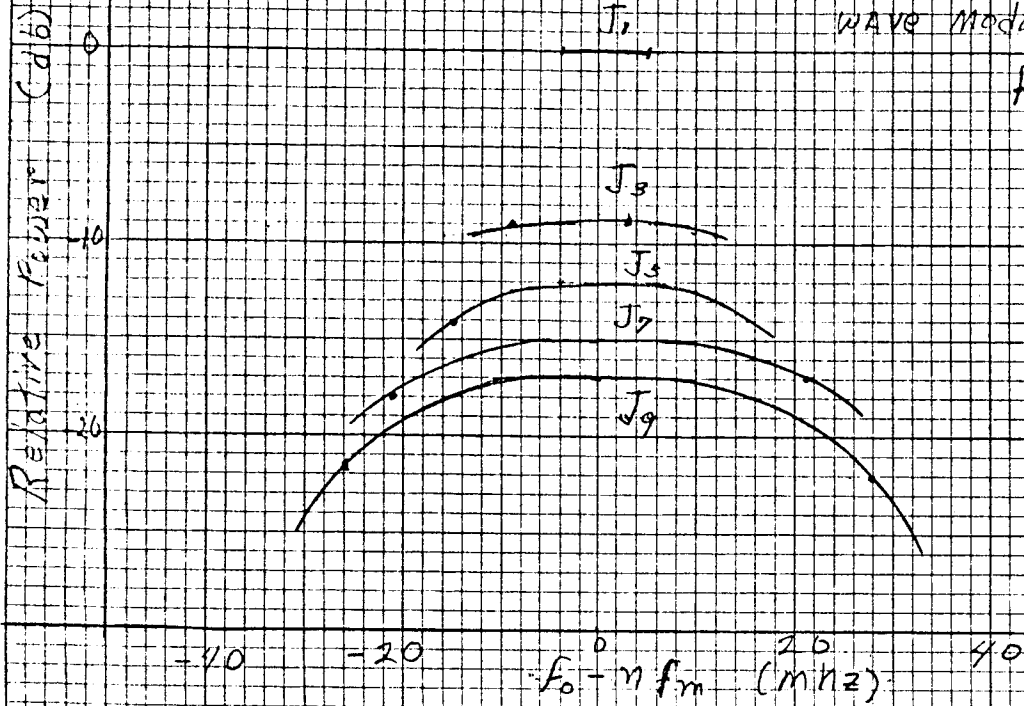


Figure 5-30.

Effective
Modulation bandwidth
of ϕ modulator
and multiplier
Composite of above
Curves.

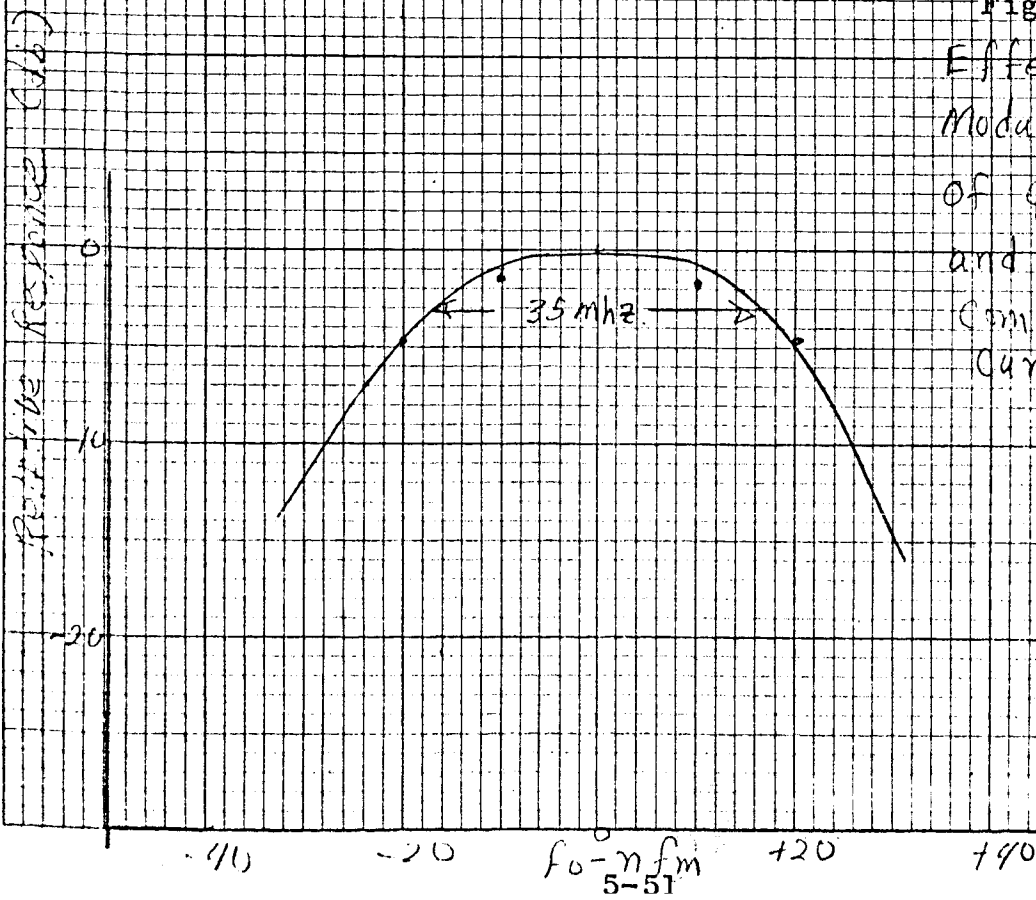


Figure 5-31.

Power output
vs power input

$f_{in} = 277 \text{ MHz}$
 $f_{out} = 2216 \text{ MHz}$

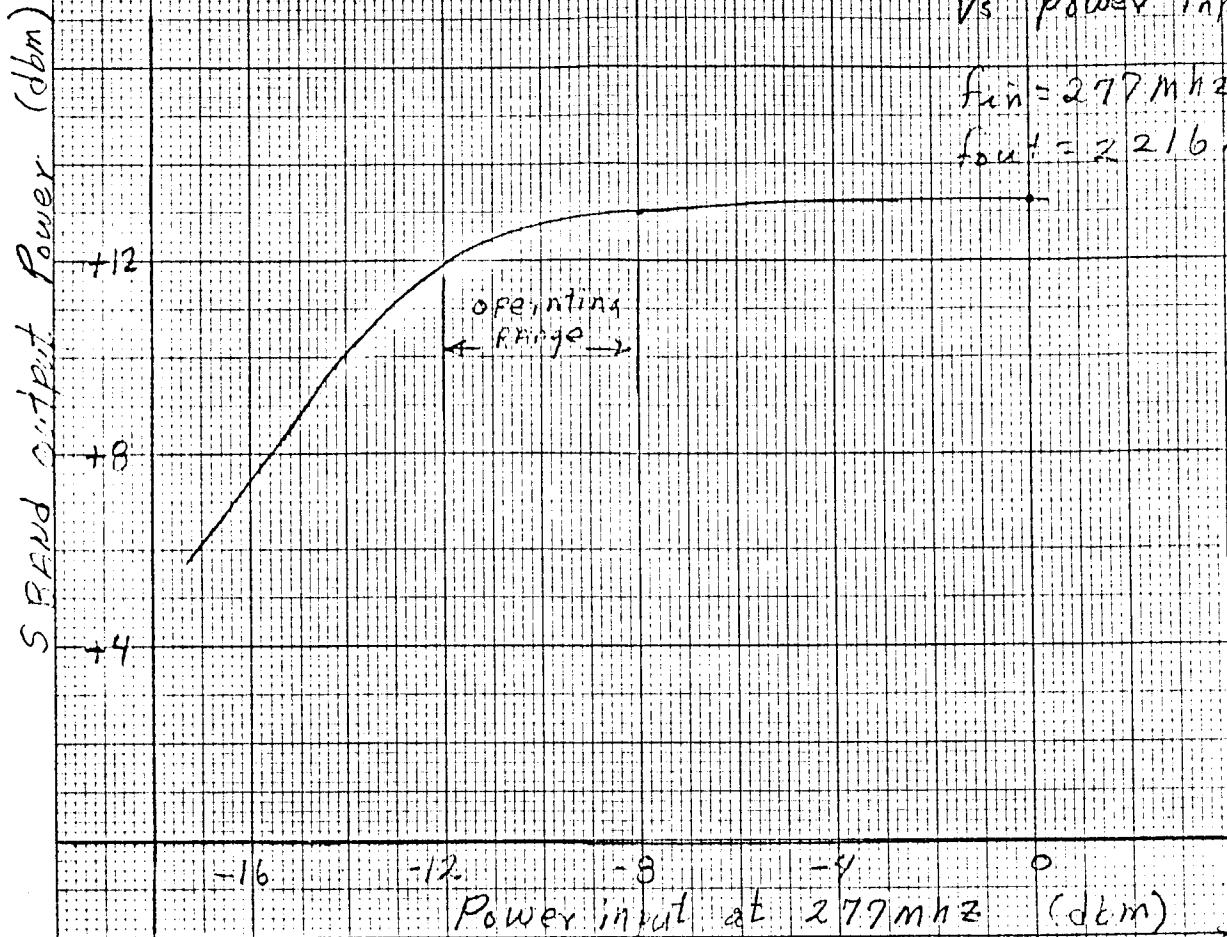
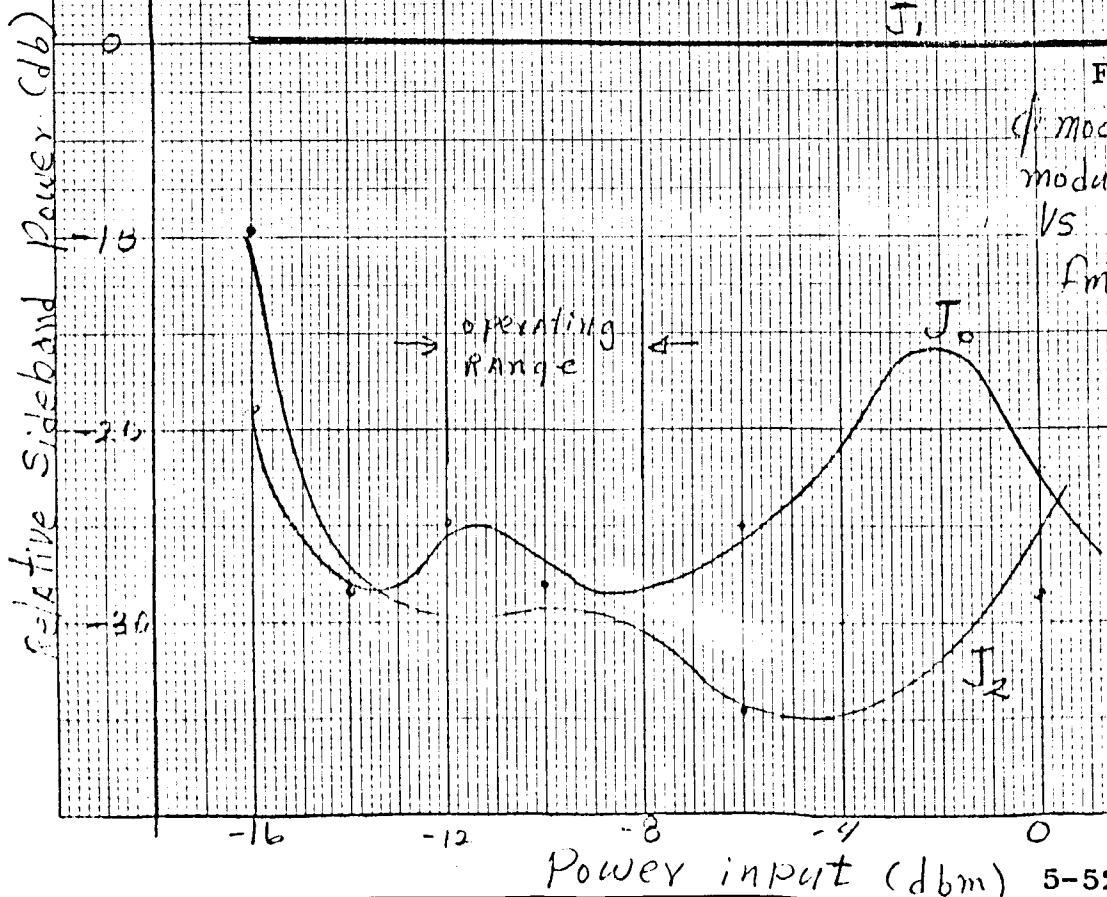


Figure 5-32.

(f_{in} mod 4 X 4 Mult
modulated output
vs Power input

$f_m = 2.0 \text{ MHz}$ square
wave.



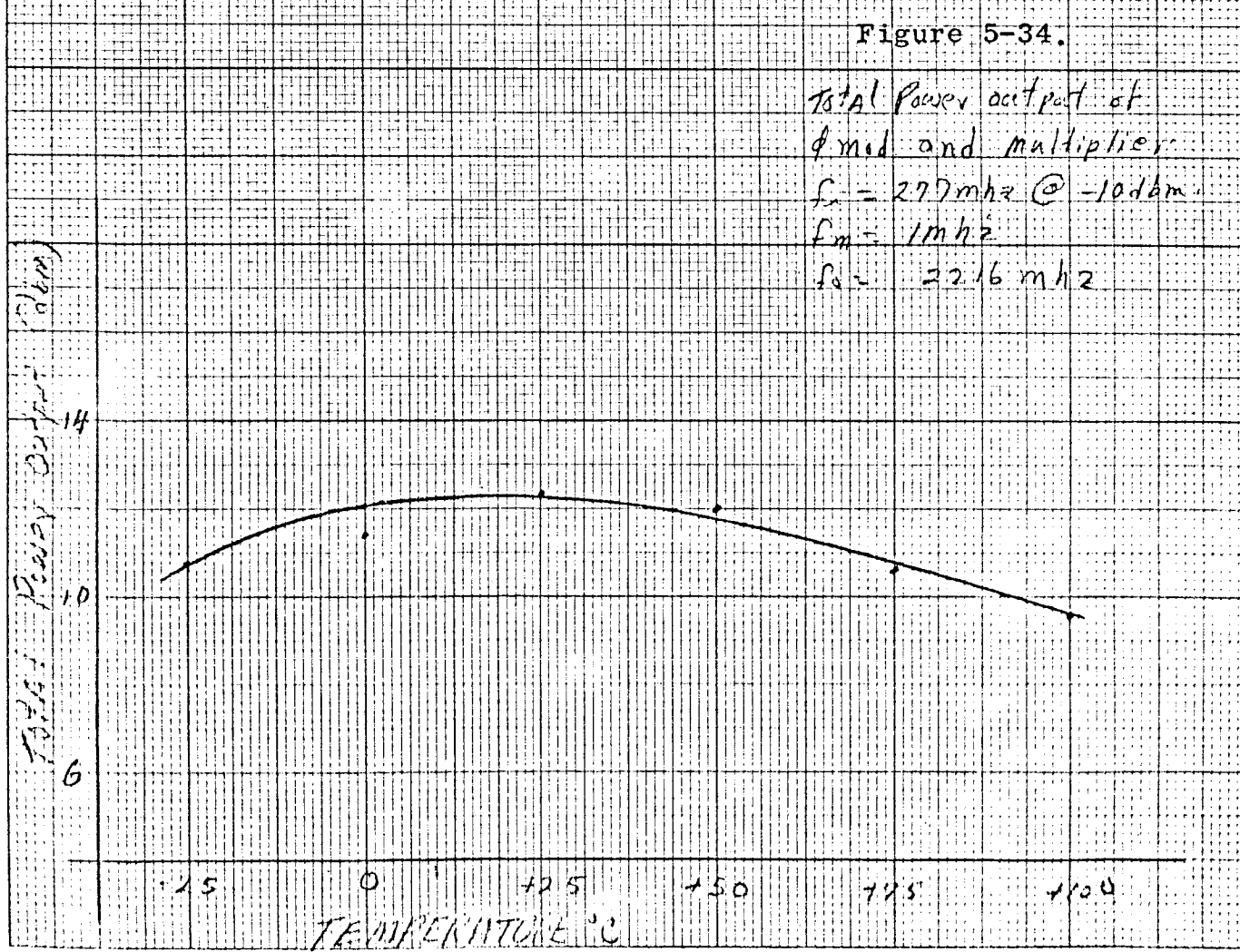
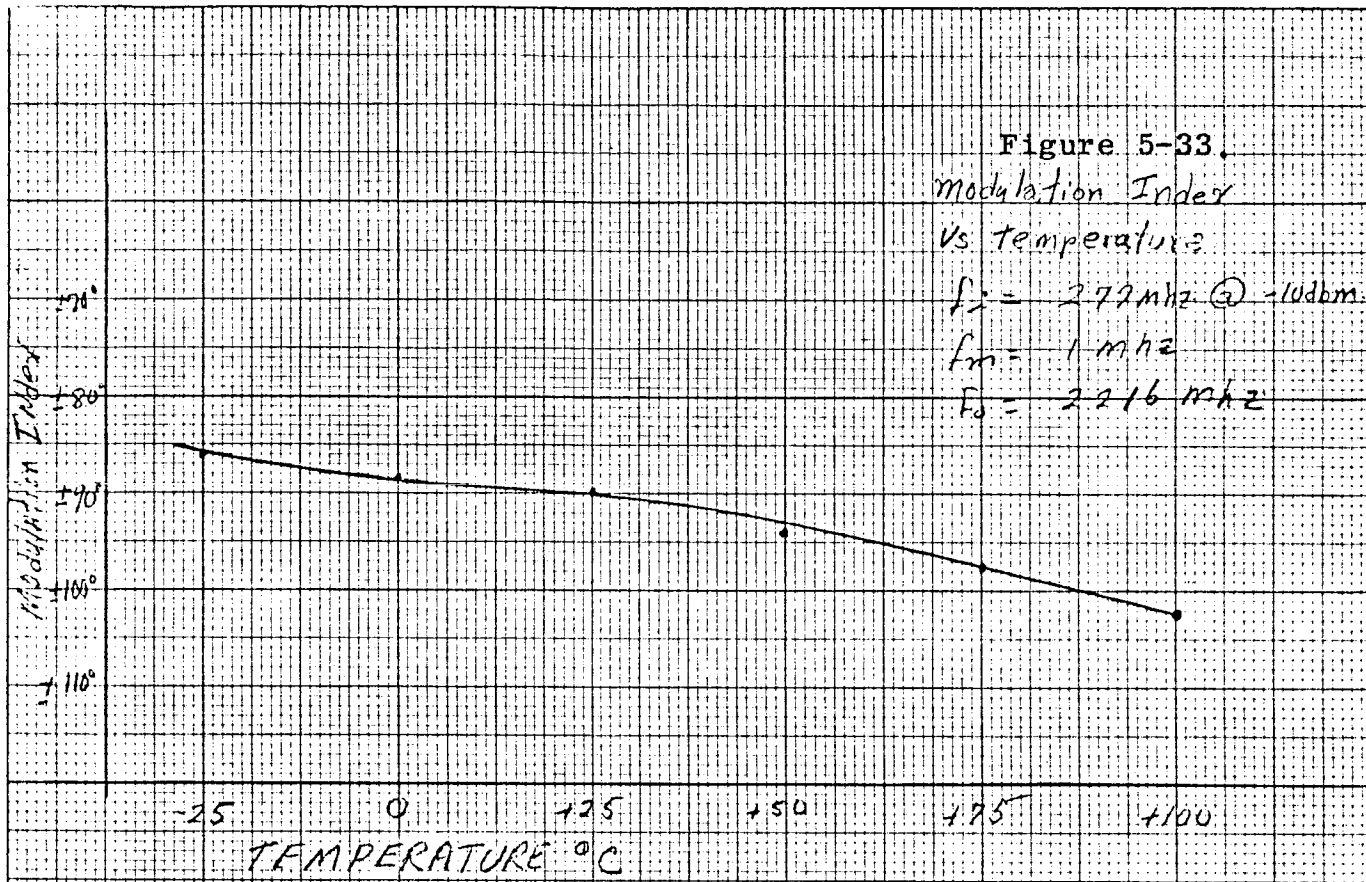
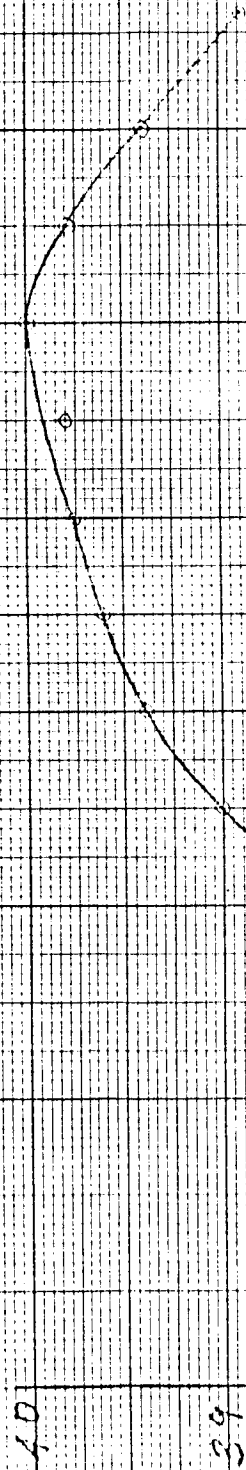


Figure 5-35
VENUE TIME AERIAL
Phase Plot 6-20-54 MHz

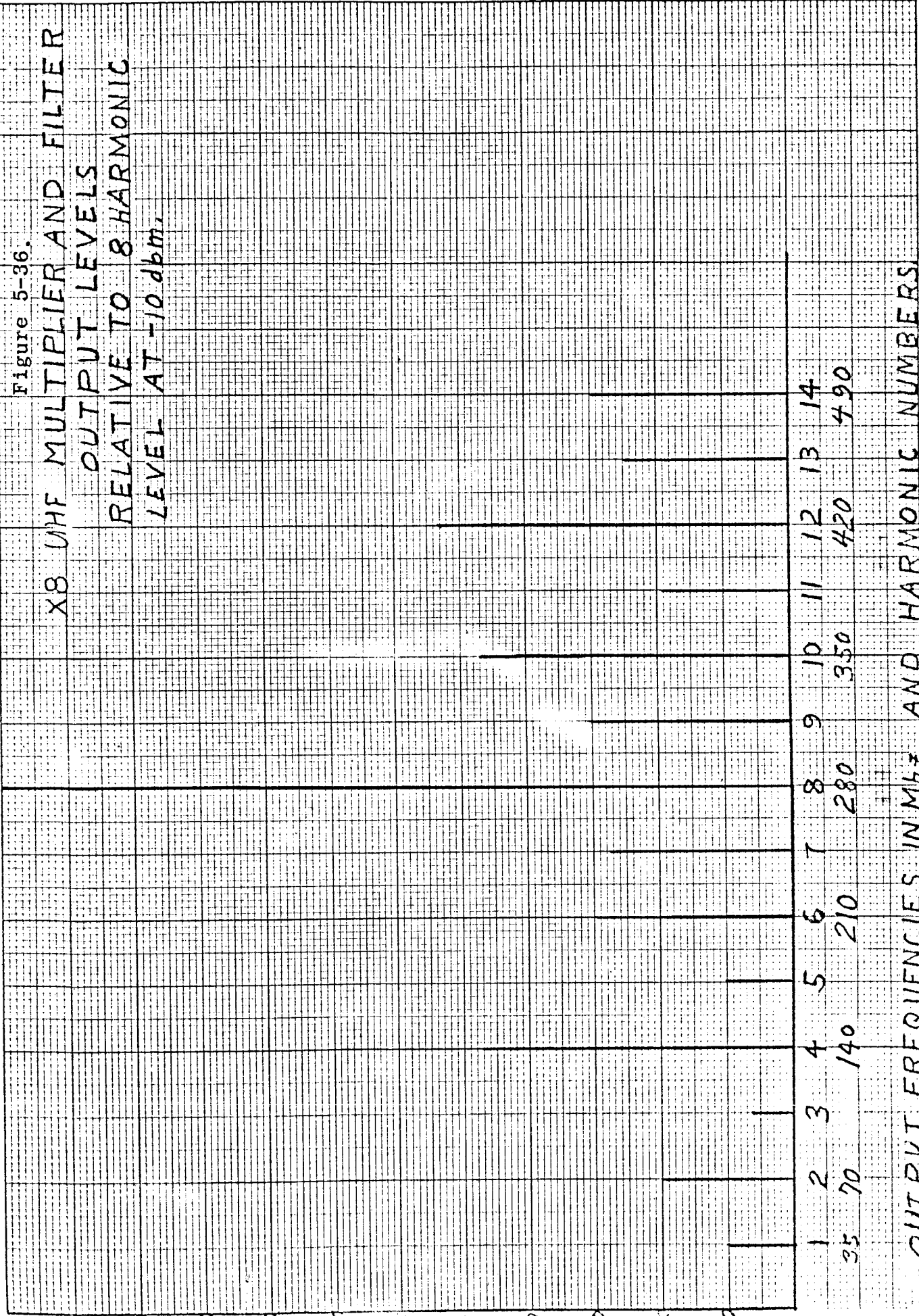


POWER Output (dBm)
5-54

6-3-55

Figure 5-36.

X8 UHF MULTIPLIER AND FILTER
OUTPUT LEVELS
RELATIVE TO 8 HARMONIC
LEVEL AT -10 dbm.



the conclusions to be drawn, and finally recommendations directed toward possible future work in this area.

5.5.1.1 Objectives

The objective was to design, develop, fabricate, test, and deliver, complete with documentation and drawings, one vehicle (L-band) and three station (S-band) engineering model RF converters for the AROD system. The main objectives were low noise figures, wide bandwidth, good linearity, and minimum size and weight. Some of the more important initial objectives were:

1. Frequency:

Vehicle	1800 MHz
Station	2214 MHz

2. Local Oscillator

Vehicle	217.7 MHz
---------	-----------

 Input Frequency:

Station	268.8 MHz
---------	-----------

3. Intermediate

Vehicle	58 MHz
---------	--------

 Frequency:

Station	63.6 MHz
---------	----------

4. IF Bandwidth

30 MHz minimum, 50 MHz maximum (3 db):

5. Conversion Gain: +22 db \pm 2 db (includes preselector loss in vehicle converter)

6. Dynamic Range: -130 dbm to -60 dbm

7. Intermodulation: $2f_1 - f_2$ and $2f_2 - f_1 > 70$ db below f_1 or f_2 where f_1 and f_2 are in the passband and have a power level of ≤ -60 dbm

8. Noise Figure: 8.5 db with 0.5 db preselector insertion loss included (objective 6.5 db)

9. Signal Input VSWR: 1.2:1 maximum

10. Local Oscillator

-20 dbm maximum Leakage:

11. Local Oscillator +16 dbm \pm 3 db
Input Power:
12. Local Oscillator 1.5:1 maximum
Input VSWR:
13. IF Output Impedance: 50 \pm 10 \pm j10 ohms
14. IF Output Linearity: Linear \pm 1 db up to -15 dbm power
output

5.5.1.2 Design and Development

Individual circuits for both the vehicle and station converters were independently designed, breadboarded, and tested. Following completion of these design phases the individual circuits were assembled into breadboard converters. The breadboard converters were also tested and delivered to the project. The deliverable converters were built as integrated units using these breadboards as models. No intermediate prototypes were constructed in the interest of both time and cost.

Single Stage Step Recovery Diode Multiplier

The frequency multiplier was designed to use a Microwave Associates MA4752 step recovery diode. A number of different HPA and Microwave Associates' step recovery diodes were tested and the MA4752 chosen as the most efficient. Conventional varactor diodes were not considered because of the multiplier size limitation and their poor high order multiplication efficiency. The design of the output bandpass filter and input low pass filter both emphasized small size. The multipliers were designed to deliver a nominal 4 to 5 mw as recommended by the mixer diode manufacturer. A small lumped constant circuit on the input was determined to be necessary to assure satisfactory operation when operated with a bandpass filter connected to the multiplier input rather than a 50 ohm generator.

Balanced Hot Carrier Diode Mixer

Both a rat race and a directional coupler hybrid were considered in the mixer design. A 3 db directional coupler was selected

since this hybrid is approximately 6 times smaller than a rat race hybrid.

The directional coupler hybrid assures a good impedance match to the diode but requires tuning screws to improve the isolation. A rat race hybrid would assure good isolation but require tuning screws for a good impedance match. Since both a good impedance match and high isolation was required, the directional coupler hybrid was chosen.

Hot carrier diodes were selected as the mixer diode because of their extremely low noise properties and low conversion loss. Optimum noise figure is obtained with about 2 to 3 mw LO drive per diode. At the time the design was done, only one hot carrier diode was available (the HPA 2350). This diode proved satisfactory and is therefore used in the AROD converters. Texas Instruments has since come out with a hot carrier diode designated the A1024 which should be interchangeable with the HPA 2350. Data was taken on several 2350 diodes at various LO drive levels over a frequency range of 1600-2400 MHz. The mixer hybrid and diode mounts were designed to give broadband operation from 1600-2400 MHz.

Low Noise Transistor IF Preamp

Both cascade and cascode circuits were studied for the IF preamp. The cascode configuration was chosen mainly because of its superior stability as a function of the operating temperature range. The initial design used Motorola 2N3783 transistors with a rated noise figure of 2.2 db maximum. However a problem developed with delivery of these units and the design was modified to use the KMC 2021 with a rated noise figure of 1.5 db maximum. Considerable effort was necessary to achieve gain stability in the small package size required. The wide bandwidth was finally achieved by use of a ferrite core transformer on the IF input to match the mixer impedance (approx. 50 Ω) to the required impedance for best IF noise figure (approx. 400 Ω). A powdered iron

core was used in the IF output to match approximately 3K ohms to 50 ohms. The design uses a KMC 2021 in the first half of the cascode circuit and a 2N918 in the second half.

5.5.1.3 Final Results

Three station converters and one vehicle converter were fabricated. The performance data on the three station converters is very similar and the vehicle converter data is quite similar to the station converter data. However, during the development of these converters it became apparent that certain of the initial converter specifications should be changed for one reason or another. A revised converter specification was written and released. The delivered converters meet these specifications with the exception of two areas. First, the converter conversion gain is typically a little low (1 dB), and the vehicle converter LO leakage is as much as 8 dB higher than the revised specification although it is still 7 dB better than the initial specification. In other words, the present specifications represent realistic values for the existing converters except for the conversion gain specification which should be reduced to 21 dB \pm 2 dB and the vehicle converter LO leakage specification which should be changed to specify a level of less than -25 dbm. With the exceptions noted above, the delivered converters meet all the present specifications. However certain discrepancies do exist in the diplexer performance. Primarily, the receive channel VSWR on the vehicle converter diplexer is high. This could be improved by a slight redesign of the diplexer printed circuit board. However the cost to modify this unit was not considered to be worth the performance improvement.

5.5.1.4 Theory of Operation

Figure 5-37 shows a general block diagram for both the station and vehicle converters. The two converters are basically very similar except the vehicle converter has a diplexer as part of the unit while the station converter does not. The VHF LO input signal frequency is multiplied eight times by a single stage step recovery

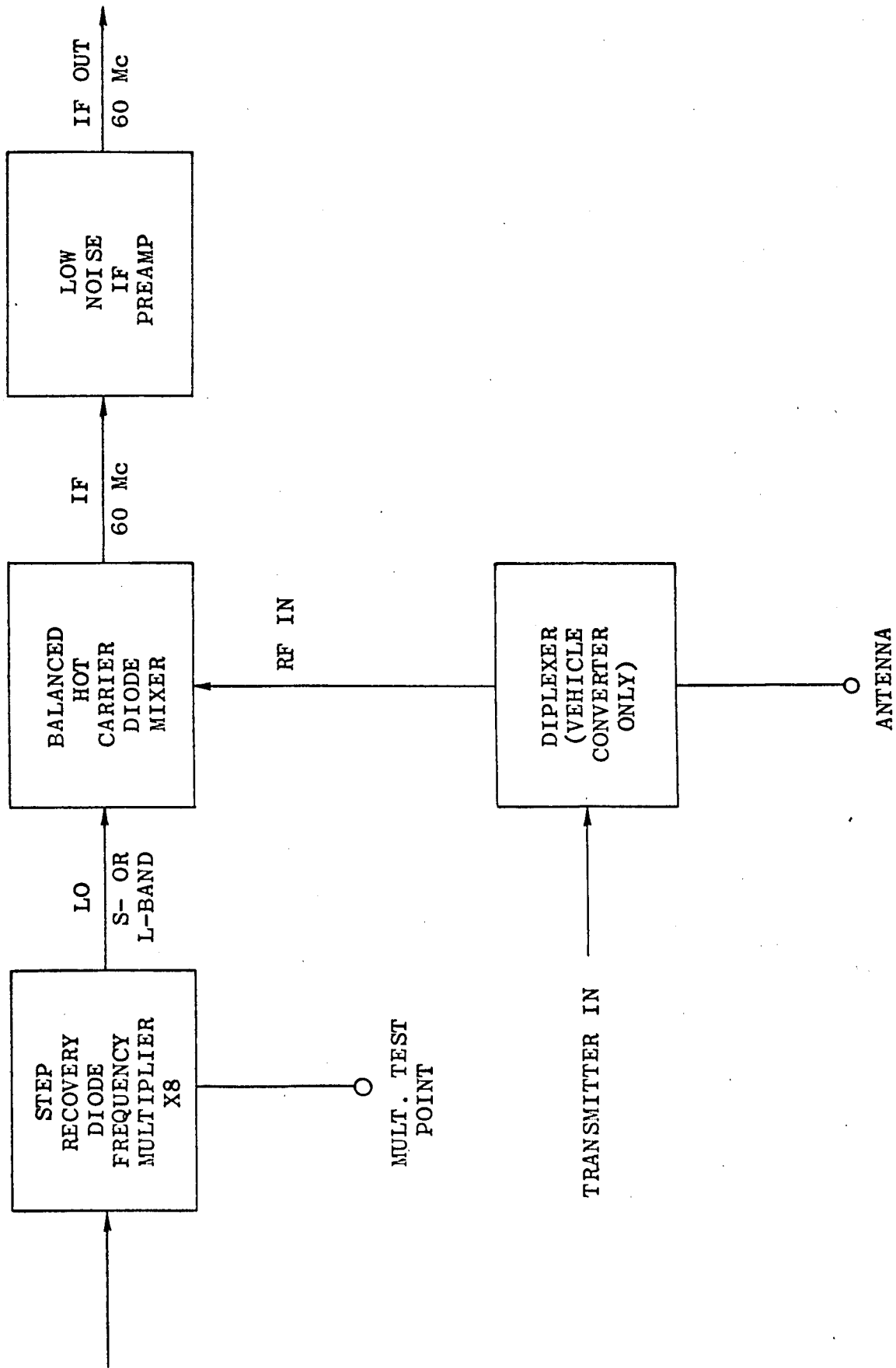


Figure 5-37. AROD Frequency Converters

diode multiplier, whereupon it is then used as the LO drive signal to a balanced hot carrier diode mixer. Multiplier power output is a nominal 4 mw and the mixer output is connected to a low noise (1.5 dB NF) wideband (30 Mc min.) IF preamplifier. The IF center frequency is approximately 60 Mc. This mixer-IF preamp combination provides a nominal 7 dB noise figure excluding the diplexer insertion loss. Overall conversion gain from the RF signal input to the IF output is approximately 20 dB. The vehicle converter diplexer allows the antenna to be used by both receiver and transmitter simultaneously. It provides the receive channel with more than 100 dB isolation from the transmitter channel and the transmitter channel with more than 50 dB isolation from the receiver channel.

The converters can be checked for proper operation by a number of different measurements, however, they are all rather complicated and somewhat inconclusive individually. Probably the two most meaningful measurements are converter noise figure, which should be 6.5 to 8.5 dB, and overall conversion gain, which should be 21 dB \pm 2 dB. The step recovery diode frequency multiplier can be checked independently by sampling the multiplier output on a spectrum analyzer through the multiplier test point connector. No spurious responses should be visible, however care should be taken to insure that what appears to be spurious frequencies of the multiplier are in fact spurious frequencies of the multiplier and not spurious responses of the spectrum analyzer or frequency related harmonics of the multiplier output. If for any reason a converter should ever perform improperly no attempt should be made to either realign or repair the unit. The unit should be returned to its source for proper repair and alignment.

5.5.1.5 Conclusions

Three station and one vehicle frequency converter have been designed, developed, and fabricated for delivery to NASA. They are smaller and lighter weight than any previously known units.

The vehicle converter weighs approximately 15 oz. and the station converters approximately $9\frac{1}{2}$ oz. The converters make use of state of the art semiconductors such as the step recovery diode, hot carrier diode, and low noise transistors along with advanced miniaturization techniques. However, these units are difficult to assemble. A few minor design changes and modifications would greatly improve their ease of reproducibility and assembly time. The design has been well documented and with some design improvements would enable production of an advanced miniaturized, low noise converter assembly.

5.5.2 Tracking Subsection

This section describes the implementation of the Vehicle Tracking Subsection which is part of the Vehicle Tracking Receiver in the Airborne Range and Orbit Determination (AROD) system. The purpose of this report is to complement reference 6 AROD Vehicle Tracking Receiver Design. This is a final engineering report which delineates system constraints imposed on the receiver design and presents the functional implementation, salient design features, and module test results.

The Vehicle Tracking Receiver is the on-board terminal of the S-band up-link. Its function is to communicate simultaneously with up to four transponder ground stations.

The receiver has a common RF converter and distribution amplifier followed by four Vehicle Tracking Subsections operating in parallel. Each Tracking Subsection is identical in implementation with the exception of the predetection filter center frequency. Channel offsetting is done with four different coherent reference frequencies.

Each Tracking Subsection interfaces with a receiver code control subsection that provides the demodulation signals and programmed operational commands. All four Tracking Subsections, or receiver channels as also referred to, interface with a common vehicle frequency synthesizer subsystem that provides coherent reference signals.

A Vehicle Tracking Subsection consists of two module frame subassemblies located in Case 2 of the airborne equipment. The two frame subassemblies have been named Carrier Tracking Loop (CTL) and Modulation Tracking Loop (MTL) for the respective subsystem functions performed.

In this report, a functional block diagram is discussed in Section 5.5.2.3 to assist in determining the location and usage of circuits which are packaged in modules on a subsection frame assembly. Sections 5.5.2.5 and 5.5.2.6 contain the theory of operation, on a module basis, defining circuit operation and design goals with references to the circuit schematic diagrams. Following each module description, test data is presented in graphical form with data superimposed from several modules of the same type to show normal production tolerances. This data was obtained following the test procedures outlined in the referenced documents test specifications.

5.5.2.1 Tracking Subsection Function and Requirements

The Tracking Subsection provides amplification, demodulation and coherent tracking of the receiver input signal. The receiver signal is a balanced-modulated, pseudo-noise coded, suppressed carrier spectrum. This spectrum is centered at approximately 58 MHz at the Tracking Subsection input and the signal level varies between -100 dbm to -40 dbm. Both acquisition and tracking are performed over this dynamic range.

The pseudo-noise (PN) sequence is a combination of a high and a low speed code. The high speed code is called H-code and the low speed code is called L-code. There are two main phase-locked loops used to acquire coherent tracking in minimum time. These loops are called the Carrier Tracking Loop and the Modulation Tracking Loop or Range Loop. When locked to the transmitted signal, the Tracking Subsection provides the following outputs for use by other subsections of the AROD system.

<u>Output Signal</u>	<u>Function Provided</u>
3.2 MHz \pm 8D	Doppler Signal for Velocity Measurement
12.8 MHz	Clock for PN Code Generator
A _L Amplified	Low Speed Code Lock Indication
A _H Amplified	High Speed Code Lock Indication
Data	Binary Data Output

To provide the tracking and demodulation function, the subsection requires the following input signals.

<u>Input Signal</u>	<u>Source</u>	<u>Usage</u>
Signal Input	58 MHz Distribution Amplifier	Carrier and Range tracking
G _I	Vehicle Receiver Code Control	Inhibit carrier loop
G _C	Vehicle Receiver Code Control	Carrier loop demodulator gating
V-0 + V-1	Vehicle Receiver Code Control	Carrier preset inhibit
G _R	Vehicle Receiver Code Control	Range loop demodulator gating
G _H	Vehicle Receiver Code Control	High speed code gate
V-3 + V-4	Vehicle Receiver Code Control	Carrier loop bandwidth switch
V-4	Vehicle Receiver Code Control	Range loop bandwidth switch
DR-A _L	Vehicle Receiver Code Control	A _L detector dump signal
f _R	Frequency Synthesizer	Phase detector reference
44.8 MHz	Frequency Synthesizer	Second LO reference
6.4 MHz	Frequency Synthesizer	Carrier preset reference

Within the Tracking Subsection are the following loops:

<u>Loop</u>	<u>Function</u>
AGC	Dynamic tracking of signal strength
Carrier	Coherent tracking of carrier frequency
Range	Coherent tracking of modulation code
Preset	Preset carrier VCO for fast acquisition
Rate Aid	Preset range VCO for dynamic tracking

Implementation of the loops is discussed in Section 5.2.3.

Power is required for the Tracking Subsection as follows:

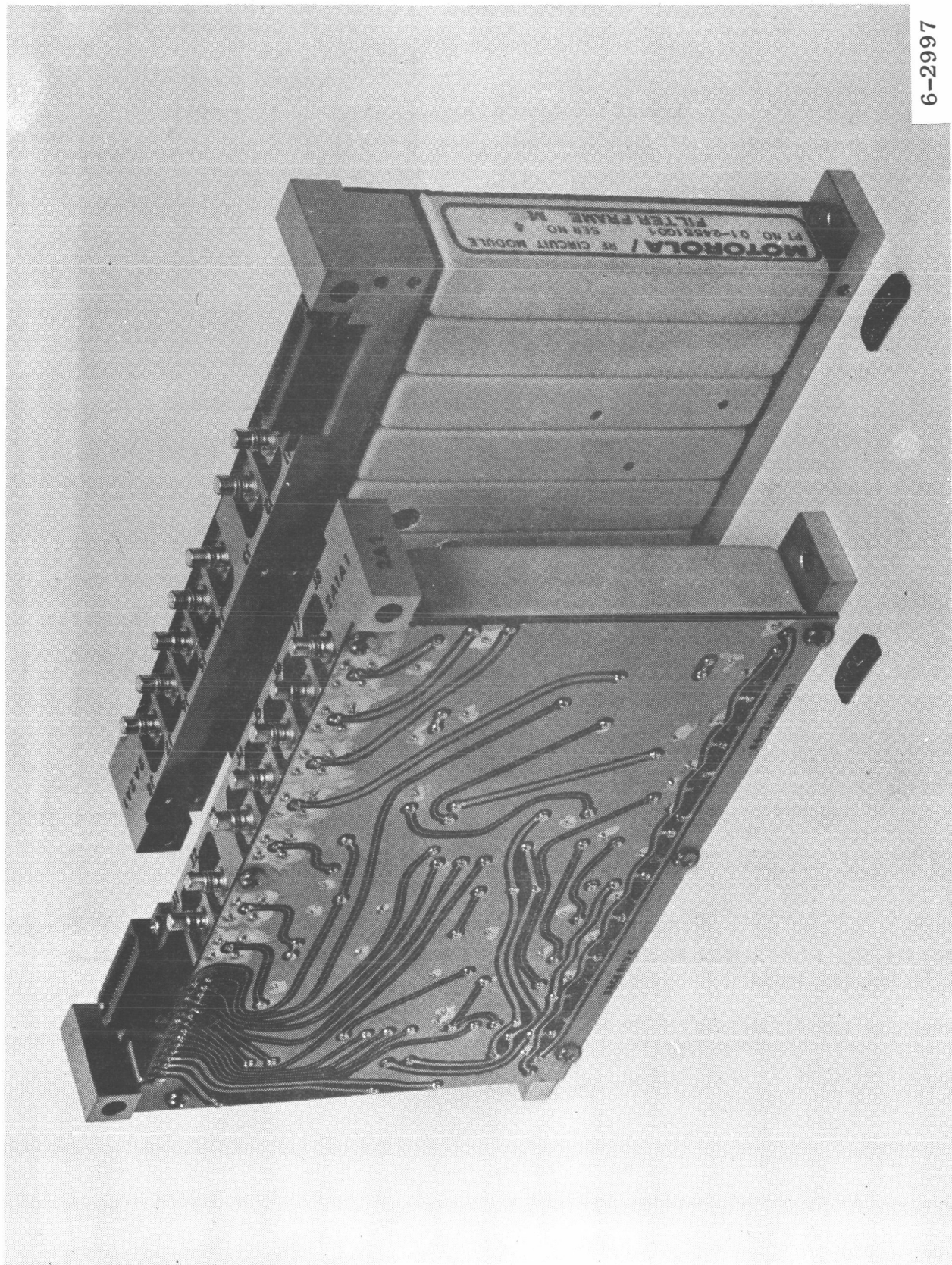
Voltage	CTL FRAME		MTL FRAME	
	Current	Power	Current	Power
+10 VDC	160 ma	1.60 watts	126 ma	1.26 watts
-10 VDC	115 ma	1.15 watts	150 ma	1.50 watts
-16 VDC	23 ma	0.37 watts	64 ma	1.02 watts
+3.5 VDC	N/A	0.00 watts	155 ma	0.54 watts
TOTAL POWER PER FRAME		3.12 watts	3.82 watts	
TOTAL POWER PER TRACKING SUBSECTION				
CTL + MTL = 6.94 watts				

5.5.2.2 Subsection Physical Description

Figure 5-38 is a photograph of the Vehicle Tracking Subsection which consists of two frame assemblies. The frames consist of RF and digital type modules mounted to a printed circuit motherboard.

The CTL frame has 11 RF type cordwood modules. The titles of these modules are:

1. Filter Regulator T
2. Balanced Demodulator
3. First Mixer



6-2997

Figure 5-38. AROD Vehicle Tracking Receiver Subsection

4. Second IF Amplifier
5. Second Mixer
6. Limiter and AGC Amplifier
7. Balanced Detector (2 each)
8. Amplifier and A_L Demodulator
9. G_C Gate and Carrier Loop Filter
10. 6.0 MHz VCO

The dimensions of an RF module are 0.7" h x 3.15" l x 0.55" w while a digital module measures 0.7" h x 3.15" l x 0.35" w. A typical RF module contains 35 components, weighs 28 grams, and is enclosed in a metal can. Digital modules incorporate a welded microharness system of interconnects used mainly for integrated circuit flatpacks. The typical digital module contains 18 components, weighs 13.5 grams and is encapsulated in a stycast potting compound.

The RF cordwood module scheme used on the Tracking Subsection was developed to provide flexibility for a variety of high frequency circuits with minimum intercircuit coupling.

Components are assembled in a fixture using two thin support boards for accurate location of components. Interconnect wires are soldered to the components in the fixture which then forms a semi-rigid module. The module is then soldered to a header support and sealed with an aluminum top can. A glass-bead type encapsulant is injected through a small fill hole and cured by heating the assembly for a specified time. This module has three distinct advantages over other types of packaging.

1. Hand wiring allows quick re-routing of signal lines to minimize intercircuit coupling during the prototype module phase. For larger quantity production, the hand wiring operation can be eliminated by the substitution of printed circuit support boards.

2. Modules can be opened easily for repair during the engineering evaluation phase by removing the encapsulant with a solvent.
3. The metal container, which is soldered to the motherboard ground plane via the module grounding pins, provides complete electrical isolation.

The MTL has 8 RF cordwood modules plus 2 full length and 2 half length digital modules. The titles of these modules are:

<u>Module Title</u>	<u>Module Type</u>
Filter Regulator M	RF Cordwood
Doppler Multiplier	RF Cordwood
Doppler Mixer	RF Cordwood
H-Code Search	1/2 Digital I/C
+3.5 Volt Filter	1/2 Digital I/C
Preset	Digital I/C
±141	Digital I/C
12.8 MHz VCO	RF Cordwood
12.757 MHz VCO	RF Cordwood
Range Loop Filter	RF Cordwood
Demodulator	RF Cordwood
Matched Filter	RF Cordwood

All modules are soldered to printed circuit motherboards which are bolted to top and bottom frame supports. The top support has been milled to accommodate RF and multipin connectors. Back and front cover plates are then bolted to the supports providing rigidity and RF shielding. Each subsection frame is approximately 6" l x 4.5" h x 1" t. This does not include the bolt down bosses. The CTL weighs approximately 1.18 pounds and the MTL weighs 1.06 pounds.

5.5.2.3 Subsection Implementation and Operation

Figure 5-39 is a block diagram of the Vehicle Tracking Receiver Subsection. Dotted lines on the block diagram outline modules located on a particular motherboard frame assembly. The

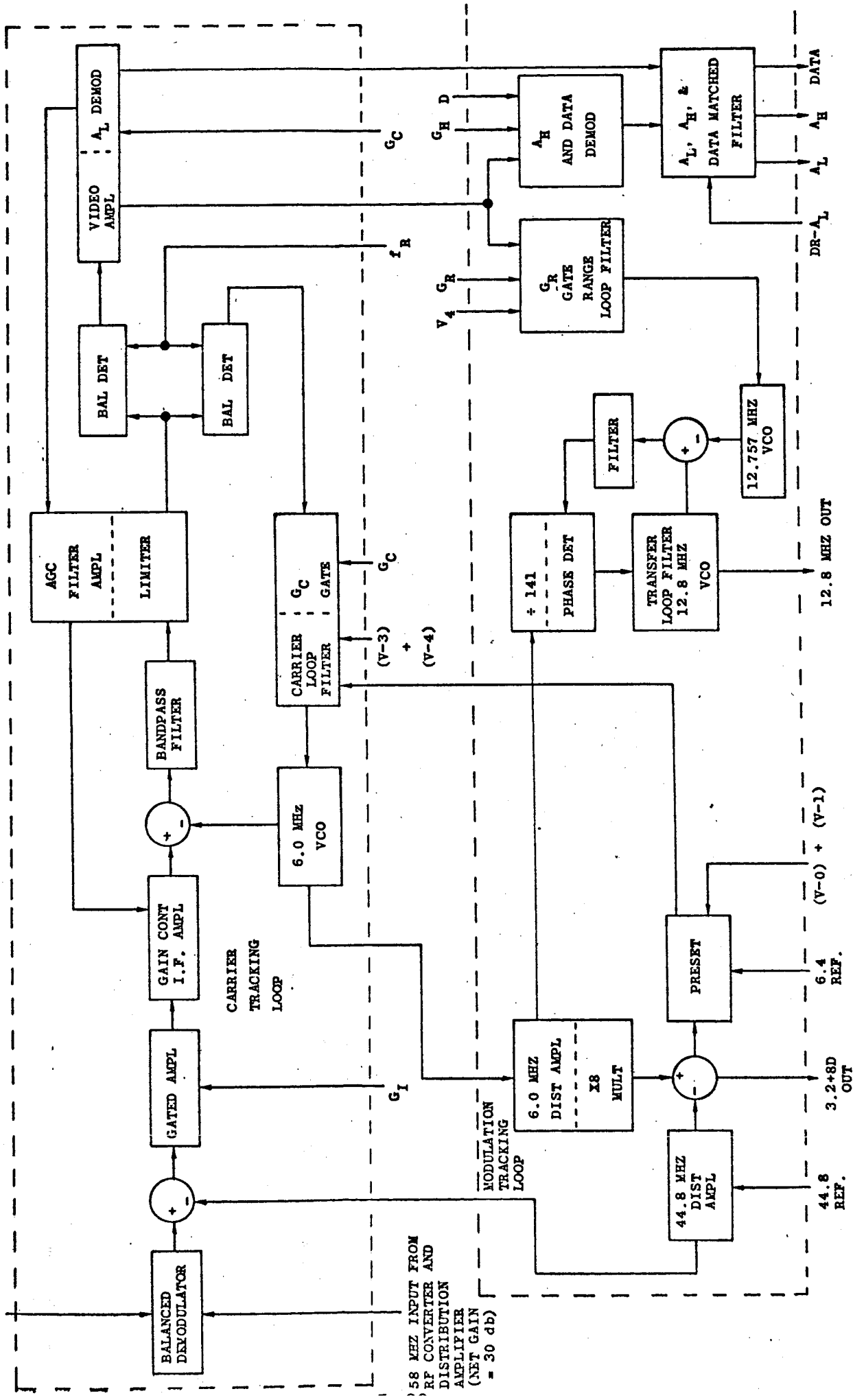


Figure 5-39. Vehicle Tracking Receiver Subsection, Block Diagram

input signal comes directly from the 58 MHz distribution amplifier and is connected to the balanced demodulator for correlation with the pseudo-noise Z-code. Other inputs and outputs to the Tracking Subsection, as well as frame interconnects, are shown on the block diagram. These other interfaces are with the frequency synthesizer, receiver code control, and system control logic subsections.

The Tracking Subsection input signal is centered at approximately 58 MHz with a power level, P_s , where $-100 \text{ dbm} < P_s < -40 \text{ dbm}$. Signal bandwidth at the input is 40 MHz with a noise power level of -71 dbm . The function of the balanced demodulator is to correlate the PN power spectrum with the tracking receiver generated Z-code. The circuit provides a 40 db carrier null and 20 db of signal gain. After correlation, the signal is heterodyned down to the second intermediate frequency (13.2 to 14.4 MHz) in the first mixer module. This circuit uses a 44.8 MHz reference signal from the frequency synthesizer subsection, and has as part of its function, a signal path inhibit capability. A gated output amplifier connected to the G_I vehicle code control command inhibits the carrier tracking loop during a range measurement. The mixer module has a -3 db conversion gain in a 2 MHz output bandwidth.

The heterodyned signal is amplified in a 3 stage, gain controlled amplifier that is part of the automatic gain control loop. This amplifier, with a maximum gain capability of 60 db, is controlled by AGC to provide a gain between $+26 \text{ db}$ and -31 db . The bandwidth is controlled to approximately 1.6 MHz by a single pole filter in the second gain stage. Amplifier noise figure is less than 20 db.

The correlated, amplified signal is heterodyned again in the second mixer module to minimize undesirable coherent signals in the IF passband. An important part of the second mixer module is the predetection filter following the mixer. It has a 120 kHz bandwidth to determine the channel predetection bandwidth. All tracking subsections are identical with the exception of the center frequency of the predetection filter. The reference to this mixer

circuit is the 6 MHz carrier loop voltage controlled oscillator, which produces a difference frequency in the second IF band (7.2 to 8.4 MHz). The second mixer module provides 5 db of conversion gain.

After predetection filtering, the signal level is normalized in the limiter and AGC amplifier module. The limiter transfer function provides an additional +36 db of gain and hard limits at 0 dbm on both outputs. At the limiter output, the signal splits for use by the modulation and carrier track phase-locked loops. A second circuit function physically contained in this module, the AGC amplifier, directly controls the gain of the IF amplifier. The AGC amplifier has a voltage gain of 4.3 and a low pass characteristic with a 0.5 Hz cutoff frequency. Also included in the circuitry is a non-coherent AGC function which operates on rectified peak code noise. This function suppresses the IF gain during code search, thus reducing the required linear dynamic range of detector operation.

The limiter outputs are connected to two balanced detectors. They operate from a common reference frequency at a 90 degree phase difference. Phase shifting occurs partly in each detector module. The detector in the range loop operates as a coherent amplitude detector while the one in the carrier track loop detects phase difference. Both detector outputs are normalized to 0.5 volts peak by the AGC loop. Detector balance is greater than 55 db over input signal levels from -20 dbm to 0 dbm.

The carrier error signal is sampled by the G_C Gate-Carrier Loop Filter module. This circuit uses a full wave detector implemented with MOS field effect transistors and an active lead-lag loop filter having DC gain. The overall gain is a function of the G_C sample rate and varies from 12 to 48 with the lowest gain in the range tracking state V-4. A bandwidth control changes the filter lead and is operated by the V-3 + V-4 command. During the low speed code search mode, a preset loop holds the carrier VCO at near center frequency by injecting an error signal in front of the loop filter as shown. The amplified loop error

signal drives the carrier VCO which is an LC oscillator with variable capacitance diodes as the control elements. The gain is 120 kHz/volt with an absolute stability of 5 parts in 10^4 . There are two buffered limited VCO outputs for the second mixer reference and for the modulation tracking loop frame functions.

Range loop modulation from the coherent amplitude balanced detector is demodulated in the amplifier and A_L demodulator module. An amplification of 2 is performed in the video amplifier portion prior to demodulation. Demodulation is obtained with a full wave MOS field effect transistor detector similar to the G_C gate circuit. Coherent demodulation supplies an AGC voltage and further signal processing provides a low speed code lock indication. An additional amplification of 3.5 is obtained in the A_L demodulator circuit. The range modulation is further distributed by the video amplifier to the range loop gate and A_H and data demodulator. Detection of high speed code lock and extraction of data is performed by the A_H and data demodulator. This circuitry consists of MOS field effect transistor gates operated by the receiver code control. Properly sequenced switch closures allow the incoming signals to be integrated in the matched filter module and then later provide a discharge path during the dump portion of the cycle. The A_L , A_H , and data matched filter module is directly interconnected with the data demodulator module. The circuitry consists of integrating capacitors and amplifiers required to produce a response at detector threshold. The A_L , A_H , and data responses are stored in flip-flops and direct the operations in the receiver code control.

The modulation loop error signal is detected in the G_R Gate-Range Loop filter module. Detection is done with a single series MOS field effect gate transistor. The detected error signal is directly applied to the active loop filter. In states

V-1, V-2, or V-3 the amplifier feedback loop remains open giving wideband DC gain, resulting in a Type I first order loop with a 4 Hz bandwidth. During the track mode, V-4, the feedback loop switch is closed, producing a Type I second order loop with a 5 Hz noise bandwidth. The detector gain is constant in this loop and the filter amplifier has a fixed gain of 33.

The amplified range error drives a 12.757 MHz VCO which, when summed to an aiding signal in the rate aid loop, provides the receiver code clock frequency. This oscillator has an absolute stability of ± 5 parts in 10^6 and a controlled gain of 500 Hz/volt.

Range loop tracking is assisted by summing the signal from the 12.757 MHz oscillator with a Doppler shifted signal from the carrier loop. The carrier loop VCO frequency is divided by 141 to provide this rate aid signal on a 43 kHz offset. A 12.8 MHz oscillator is phase-locked to the sum frequency. The transfer loop error is smoothed in an active lead-lag filter having a DC gain of 23.

The output signal for extraction of the S-band Doppler shift (3.2 MHz +8D) is obtained by multiplying the 6 MHz VCO frequency by 8 to increase the resolution and then heterodyning against the 44.8 MHz reference in the Doppler mixer module. Since this signal is indicative of the open loop carrier oscillator frequency in the states V-0 and V-1, the preset loop uses it as an error source. The frequency preset circuitry digitally compares the 3.2 MHz +8D signal against a stable 6.4 MHz reference and produces an error signal that keeps the carrier VCO bounded with respect to the reference during carrier loop acquisition.

5.5.2.4 Subsection Testing

Frame Level Tests

Frame level and subsection tests are made prior to releasing a receiver channel to system integration in the vehicle package, Case 2. The purpose of the tests are to verify subsystem operation

and performance, build a history of nominal production tolerances, verify module temperature performance, and to align the channel.

The first frame level testing is done on the carrier tracking loop assembly. This frame contains the complete carrier gain channel, phase-lock loop, and AGC loop. In this phase of test, the frame is exercised on the bench with a 58 MHz modulator test fixture. Non-coherent generators are used for reference signals and the modulation source is a square wave generator. Channel alignment is completed, and the phase-lock loop acquired using the same square wave source for the G_C gate demodulator drive. After lock up, several additional tests are made as required by the test procedure.

Following CTL bench tests, the frame is mated with the modulation tracking loop assembly and vehicle receiver code control subsection. Mating and testing of these pieces is done in a double layered screen room with the transponder signal source located outside. The frames are mounted on a test chassis that provides power and frame interconnect wiring and several toggle switch commands which, in the AROD system, are supplied by the vehicle system control logic subsection.

The test of the combined CTL-MTL and code control is begun with carrier loop locked on the low speed code modulation. If necessary, the demodulation signals G_{C1} and G_{C2} are re-phased on the CTL motherboard by a wiring change provided for this purpose. Next, the modulation tracking loop is acquired and static offsets nulled out. At this point, the receiver channel is operational and performance tests can be made. Performance tests include:

1. Verifying the open loop gain, K_V .
2. Measuring loop responses in all modes of operation.
3. Recordings of the carrier acquisition characteristics.
4. Recordings of the cross correlation error signals.
5. Receiver threshold and dropout measurements.
6. Performance characteristics over the environmental temperature range.

Module Level Tests

RF cordwood module under tests are performed to verify operational performance and to build a history of nominal production tolerances.

These tests occur at three phases of module construction. The first electrical test is after assembly. In this state, the module is fully wired, but not yet attached to the rigid header assembly. A preliminary operational test is made and key performance data like gain, output power, and frequency response are recorded. Wiring errors or faulty components are detected and corrected. Next, the module is soldered to the header; the module cover is slipped on and all required tests including RFI are made and recorded. At this stage the module is complete less the encapsulant.

A glass bead type encapsulant is inserted through a small fill hole in the module cover and cured by heating. After encapsulation, complete final tests are made. Results are compared against data obtained before potting for performance degradation and against nominal tolerances. All data are recorded on reproducible master copies and approved before acceptance for frame assembly.

5.5.2.5 Carrier Tracking Loop, Module Operation and Test Results

Frame Filter T

Each frame has a filter module located close to the input connector. The function of this filter is to distribute power along the frame and to suppress conducted power line interference into and from the frame. Additional voltage supplies are generated in the module by shunt regulating (zener diode) from the prime inputs.

The frame filter module has filtered outputs of plus and minus 9 vdc, minus 15 vdc and zener diode regulated outputs of plus and minus 6.2 vdc. Inputs are plus 10 vdc, minus 10 vdc, and minus 16 vdc from the vehicle power converter. Zener regulated supplies are derived internally from the plus and minus 9 vdc outputs.

An active filter circuit design provides -15 db minimum attenuation for frequencies from 10 kHz to 1 MHz within the tight packaging constraints. These line filters have series pass transistors whose base connections are capacitively coupled to signal ground. Capacity applied to the transistor base is effectively multiplied by the common emitter gain thus providing low frequency filtering without using large capacitors. Additional shunt ceramic capacitors filter at frequencies where the larger tantalum units are not effective. The pass transistors are biased at approximately 1 volt collector to emitter and provide regulation for small ($\pm 5\%$) line variations from the power converter.

A shunt zener diode regulator provides plus and minus 6.2 volt outputs. The series resistor is chosen for 5 to 9 ma of diode current under worst case operating conditions. Additional filtering precedes these outputs by virtue of the plus and minus 9 vdc filtering. Figure 5-40 is the test data for Frame Filter T.

Balanced Demodulator

The balanced demodulator is the first module in the signal path of the Tracking Subsection. Correlation of the received code with the local reference is done at this point to avoid the introduction

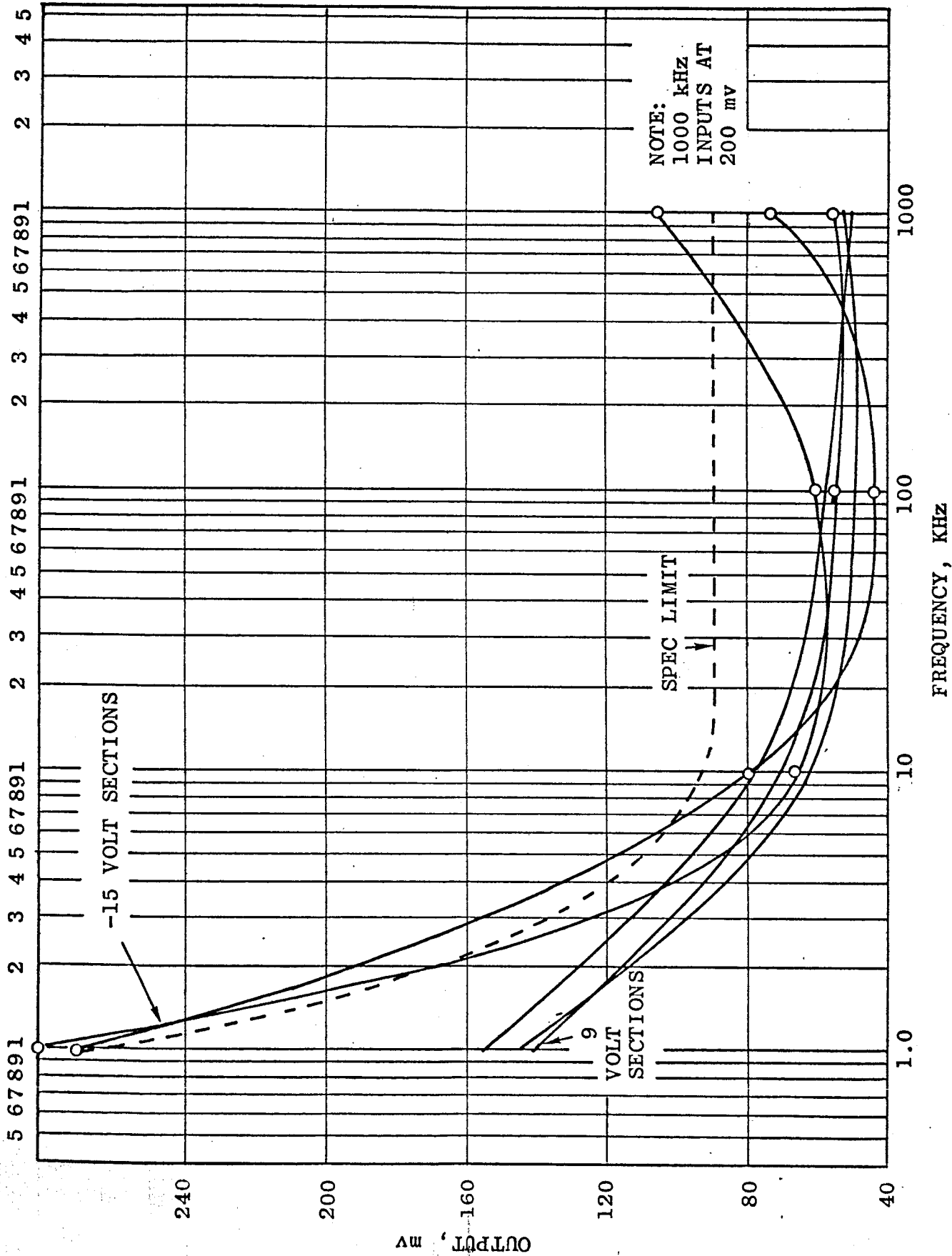


Figure 5-40. Frame Filter, Type T Output Voltage vs Frequency
Input at 500 mv, S/N 1, 2, 5

of range delays due to narrowing of the bandwidth through the channel. This circuit was a particularly critical design because of the very fast switching required to maintain carrier suppression. The input signal is at approximately 58 MHz.

The balanced phase demodulator is basically a diode ring modulator operating at the first IF amplifier frequency. Figure 5-41 is a functional configuration of the module.

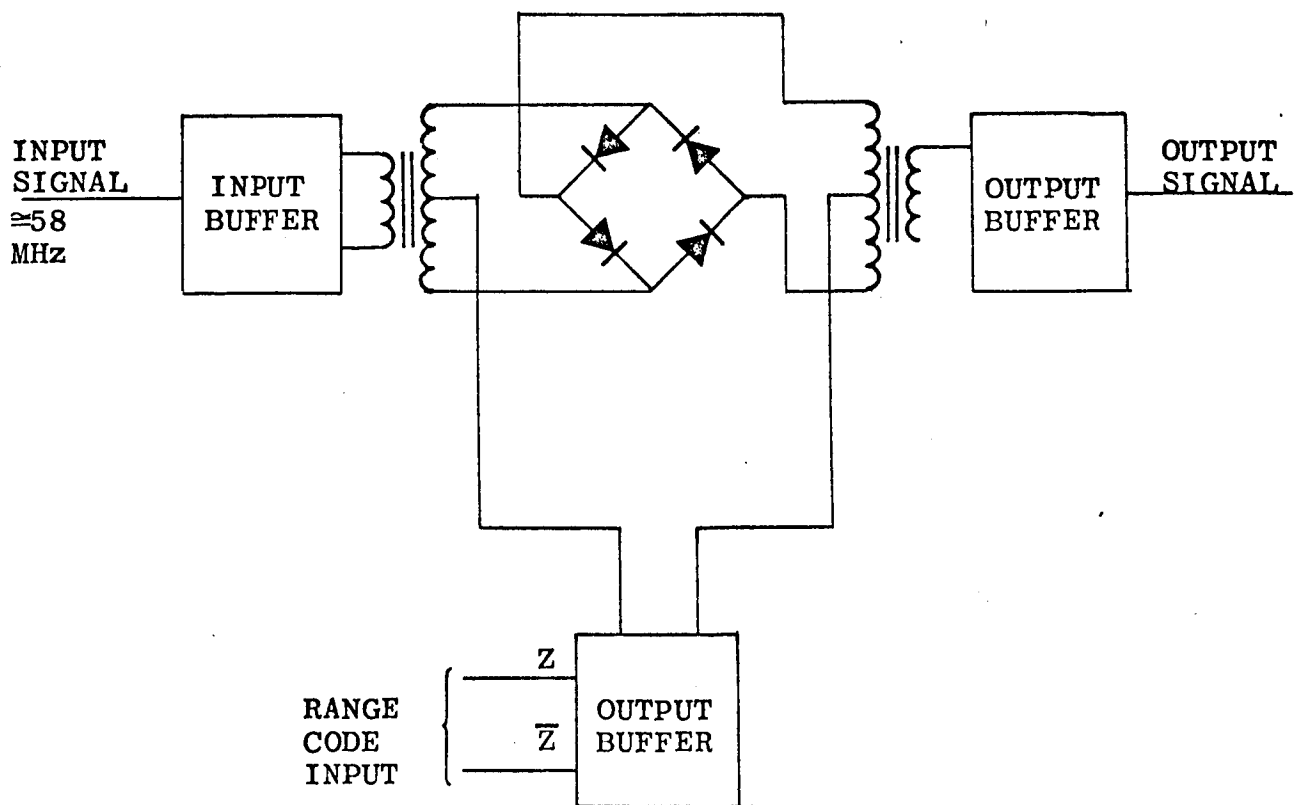


Figure 5-41. Balanced Phase Demodulator Circuit

Switching speed of less than one nanosecond with amplitude and phase balance of 40 db is achieved by the use of four matched hot carrier diodes as the switching elements as shown in test data, Figure 5-42. The amplitude and phase balance are achieved with

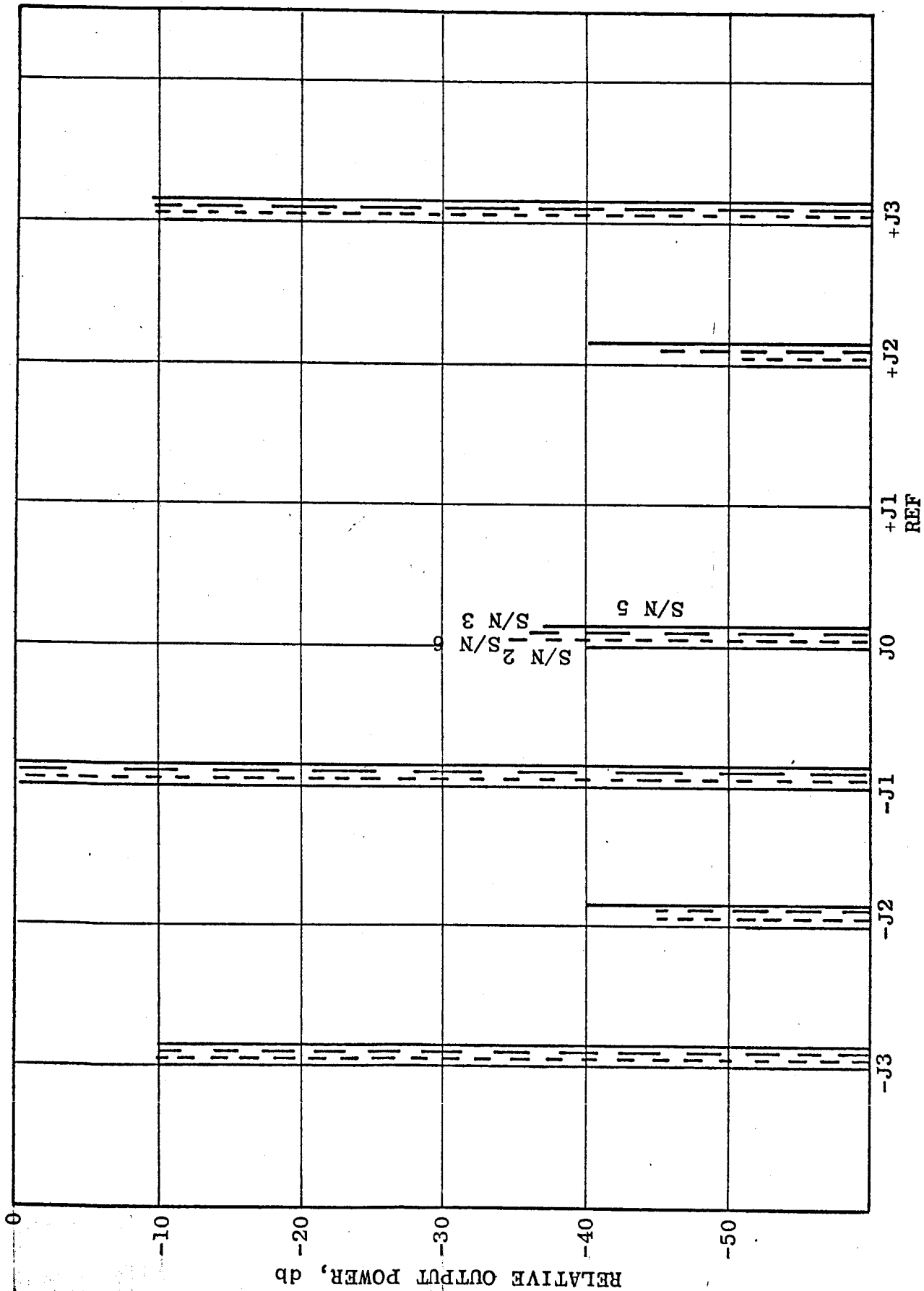


Figure 5-42. Phase Demodulator Spectral Component Output Relative to +J1

ballun wound transformers on the input and output of the diode quad. Further balance precautions include the use of double ended input, output, and switch signal buffers. The double ended stages give a higher degree of common mode rejection than could be obtained from a balanced transformer.

The input signal buffer stage has a 3 db bandwidth of approximately 60 MHz to reduce group delay in the spectrum before the correlation process.

Due to very short propagation delays in the buffer stages and in the phase switch, it is impossible to make an accurate measure of the signal propagation delay before the correlation point. A worst case calculation for total propagation delay, and delay variation, shows a total delay variation of 0.51 nanoseconds at the correlation point. This module uses 15 ma at +9 vdc.

First Mixer

The first mixer follows the balanced demodulator and heterodynes the output signal to the first intermediate frequency in the range 13.2 to 14.4 MHz. A gated amplifier in the signal path is controlled by the GI code control signal for inhibiting the carrier tracking loop. The mixer reference signal is 44.8 MHz provided by the frequency synthesizer subsection.

Mixing is done in a basic diode mixer driven from a hybrid integrated circuit differential amplifier. The medium power amplifier, A43, was chosen for this application. Optimum mixing is obtained by setting the reference signal level with the power divider network R1 and R2. (See Figure 5-43.) Diode operating points are optimized by setting the quiescent diode current with resistor R4.

The desired mixer product frequency is selected with a parallel resonant, transformer coupled filter. It is tunable for all four channel frequencies in the range 13.2 to 14.4 MHz. Signal inhibiting is done with the GI gate transistor Q1 which drives

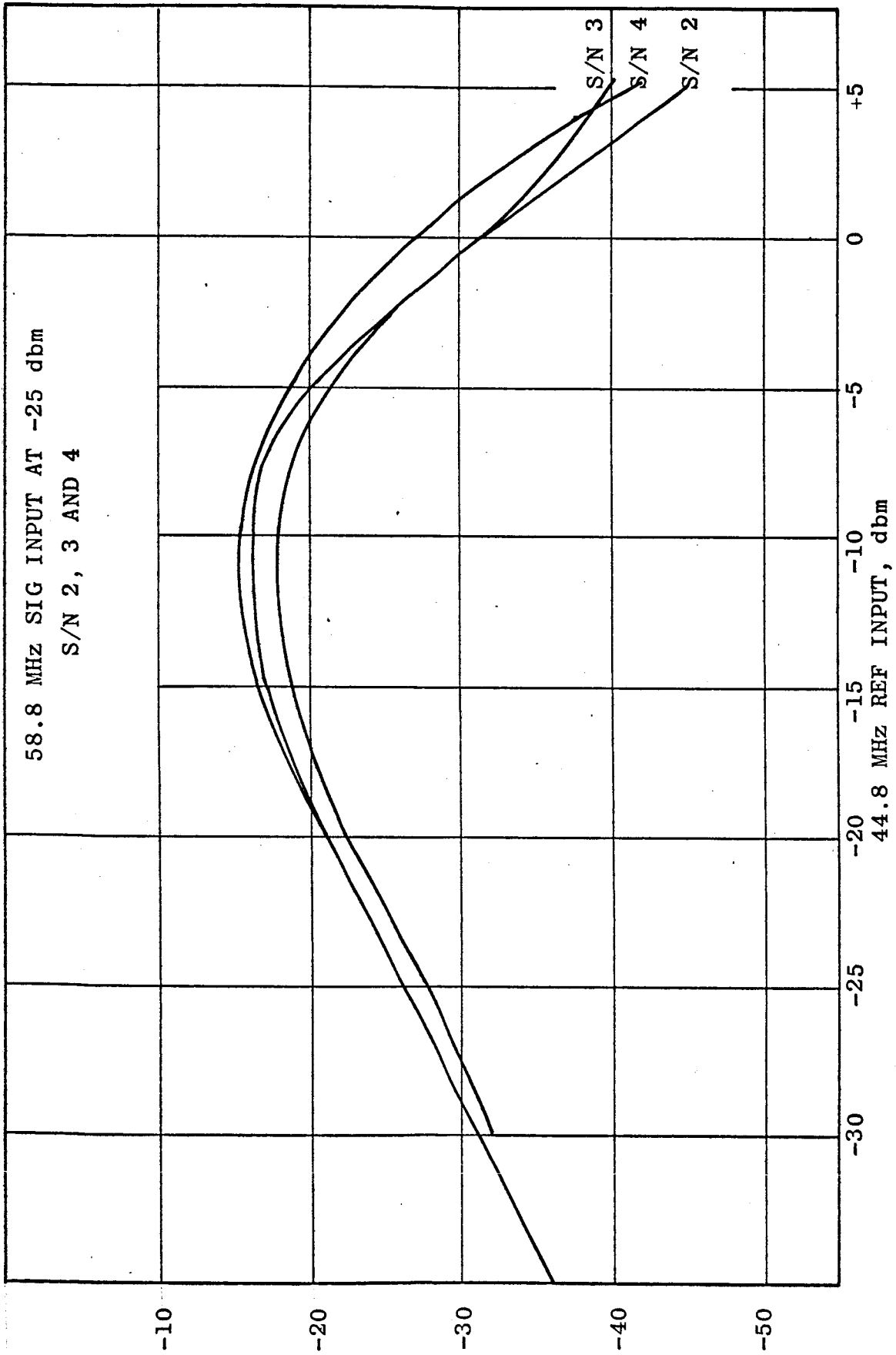


Figure 5-43. First Mixer Output Level vs Ref. Level

amplifier A-2 into cutoff when enabled. Switch ON time (10 to 90%) is 40 nanoseconds and the release time is 150 nanoseconds.

The output of amplifier A-2 is power matched to 50 ohms with a bandwidth of approximately 4 MHz. Inductor-capacitor power line filtering reduces conducted interference below 30 microvolts rms. The module uses 8 ma of current from the 9 vdc supply.

Second IF Amplifier (Reference Schematic)

The second IF amplifier module is common to both the vehicle and ground station tracking receivers. In the vehicle it operates at frequencies of 13.2, 13.6, 14.0, and 14.4 MHz. The automatic gain control capability is provided for a gain range from -12 db to +60 db. (See Figure 5-44.) With a module input power level ranging from -88 dbm to -38 dbm, the nominal output power is -50 dbm.

The amplifier consists of three transformer-coupled stages. Input and output terminals provide a power match into 50 ohms. The second stage has a single pole filter that is tunable over all four channels and provides a 3 db bandwidth of 1 MHz. Each stage operates with a +9 vdc supply and an AGC voltage range of 0 to -5 vdc. Maximum gain is achieved at the -5.0 volt AGC level.

Each stage of the amplifier utilizes a Motorola MC 1110 hybrid integrated circuit RF amplifier as the gain-controlled active device. The AROD receiver requirements for such a device include low noise figure, large AGC range, high gain per stage, and low power dissipation. The MC 1110 meets these requirements with additional performance features of good gain temperature stability, and low internal feedback.

The amplifier was designed with the aid of y-parameter analysis and two-port network equations. A design check with a Linville chart confirmed excellent phase stability margin at the required frequencies. Amplifier noise figure for several production units was typically 17 db. Maximum current for this module is 13 ma from the +9 vdc supply.

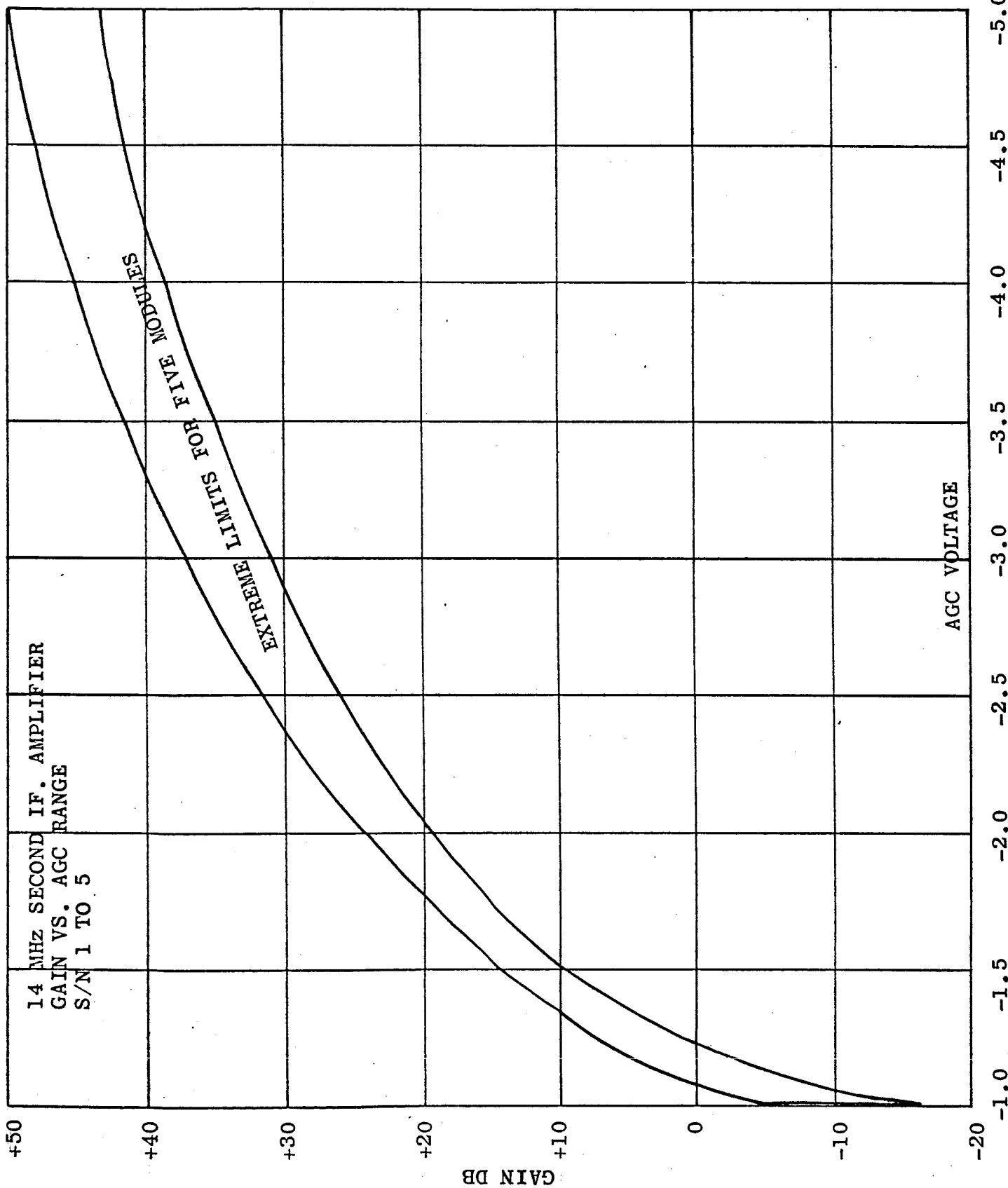


Figure 5-44. Second IF. Amplifier Test Data

Second Mixer

The second mixer module precedes the limiter and provides the second intermediate frequency whose range is 7.2 to 8.4 MHz over the four channels. Its input comes from the first IF amplifier and the carrier VCO provides the signal reference. The circuit employs a basic diode mixer driven from a medium power hybrid integrated circuit differential amplifier, A43. See test data Figure 5-45.

A high Q parallel resonant filter follows the mixer and sets the predetection bandwidth. This circuit has a center frequency of approximately 8 MHz and a 3 db bandwidth of 120 kHz.

The narrow bandwidth requires the use of a high Q toroid inductor in series with a small variable inductor for fine tuning. Figure 5-46 shows the basic filter arrangement with input and output impedances indicated as approximate values.

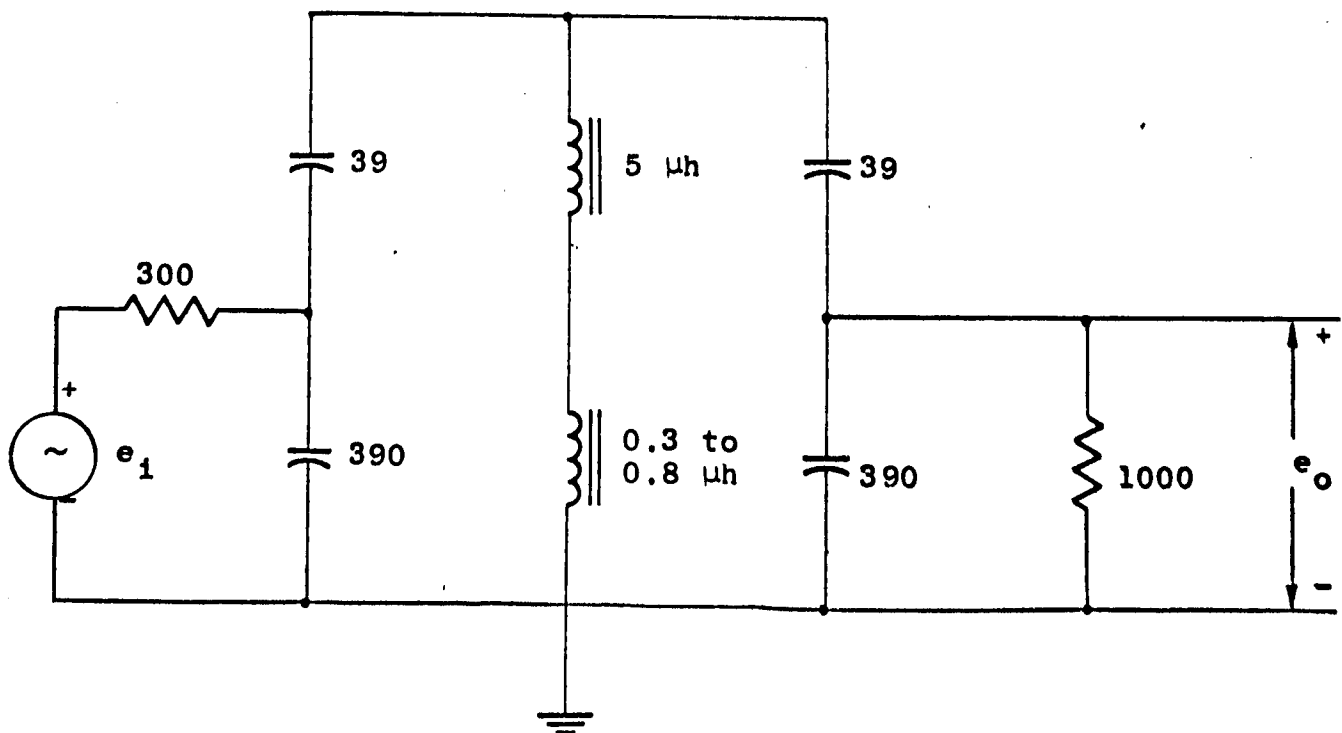


Figure 5-46. Predetection Channel Filter

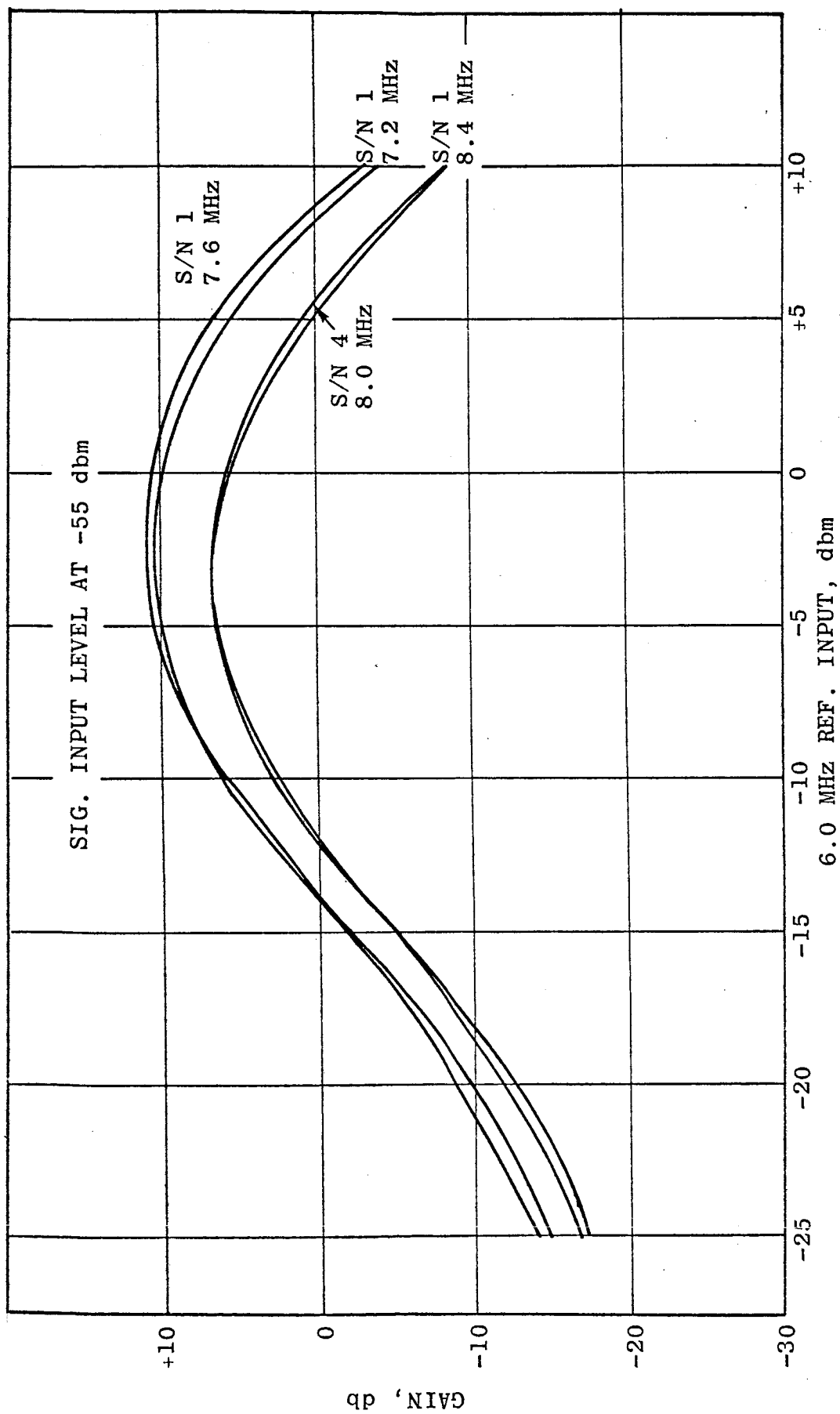


Figure 5-45. Second Mixer Gain vs. Ref. Input Level

The unloaded Q of the tuned circuit is approximately 150. Loading on the input and output of the filter results in an effective circuit Q of approximately 70. The required temperature stability is achieved by careful processing of the larger (5.0 uhy) toroid coil. The overall bandwidth is specified at 120 KC \pm 20 KC which includes variations over the temperature range. An output buffer amplifier prevents bandwidth degradation due to loading. This module uses 11 ma at -9 vdc.

Limiter and AGC Amplifier

Two separate circuit functions are provided within this module as the title implies -- limiting and AGC.

The limiter circuit determines the maximum amplitude signal into the balanced detectors. This is desirable to fix the maximum phase detector gain and consequently the maximum loop bandwidth as a function of signal strength. This circuit normally operates as a linear amplifier and provides limiting only during acquisition and near the receiver threshold.

The limiter circuit consists of two cascaded low power hybrid differential amplifiers (A44). The IF input signal is received single ended into a 50 ohm termination, and the first amplifier output provides a double ended connection to drive the second amplifier. Two separate outputs are provided, each with a 50 ohm matching section. A gain of 36 db through the cascaded circuit is realized and the last stage is in hard limiting at zero dbm output level. Figure 5-47 shows the test data results.

The other half of the module comprises the AGC amplifier. Its function is to set the IF amplifier gain proportional to signal strength as sampled by the A_L demodulator. Under strong signal conditions the AGC amplifier input ranges between -2.5 to -3.5 volts. A zener bias supply (CR1) is used in front of the AGC amplifier to offset the input to a nearly zero level. The AGC amplifier also has a non-coherent AGC action to prevent perturbations caused by uncorrelated code noise. Positive peak noise

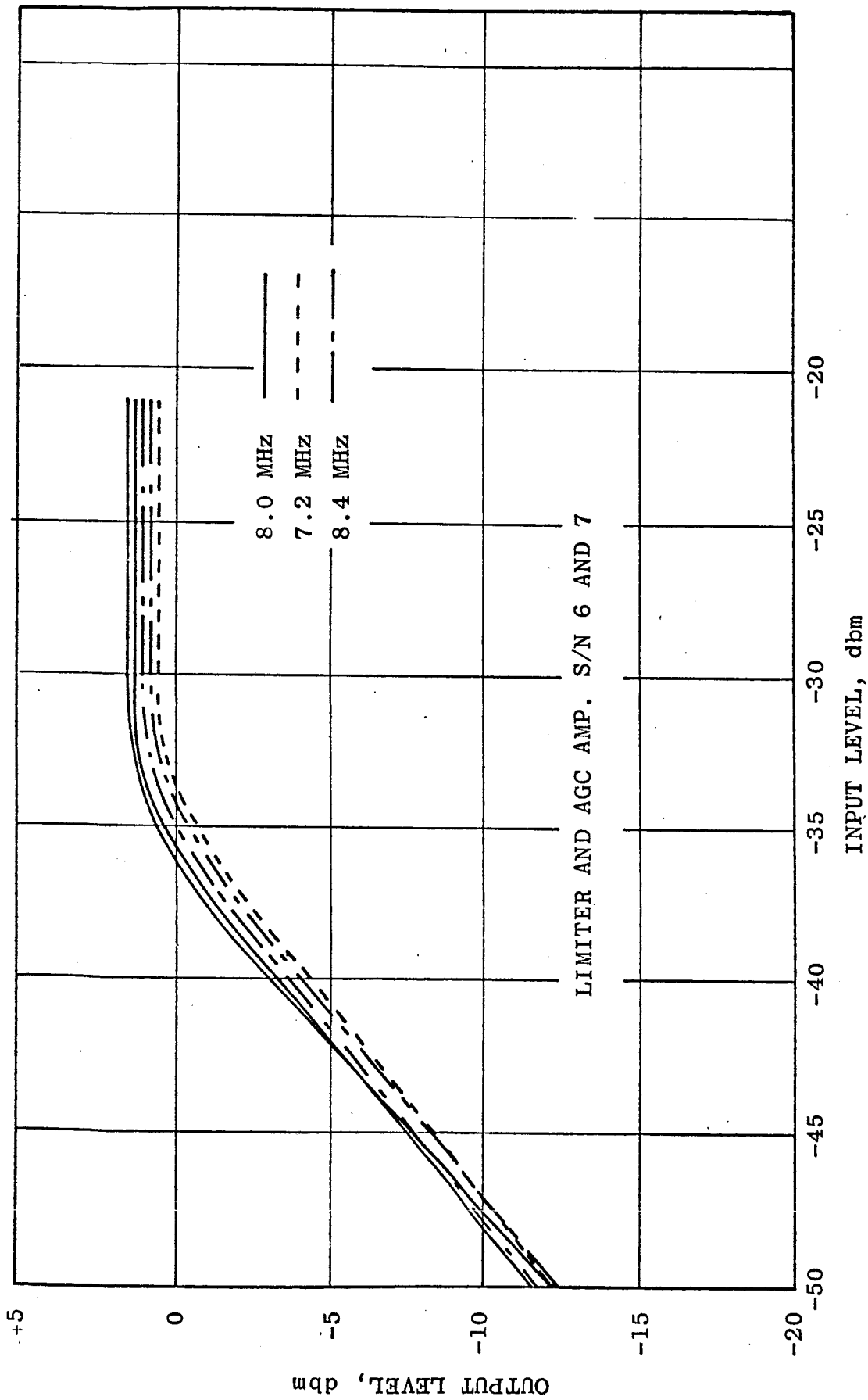


Figure 5-47. Limiter Gain

voltage from the A_L demodulator is rectified by CR2, then integrated on C22, and shifts the AGC amplifier output in a sense to reduce the IF gain. The operational amplifier A1 also acts as an active filter to smooth the demodulation. An emitter follower driver is required at the output for current driving the IF amplifier. This module uses 1.5 ma at +9 vdc, 11 ma at -9 vdc, 10 ma at +6.2 vdc, and 28 ma at -6.2 vdc when loaded by the IF amplifier. See Figure 5-48.

Balanced Detector

The balanced detector module is used in the carrier tracking loop as a phase detector and in the modulation loop as a coherent amplitude detector. To provide both detection functions, the reference frequencies must be 90 degrees out of phase. Adjustable lead or lag phase shifting of 45 degrees is provided in each module. The input network L4-R16 tunes 45 degrees over all four reference frequencies. Phase lead or lag is determined by the input network grounding connection.

The detector circuit uses a balanced ring demodulator with special precautions to assure carrier null and reproducibility. Carrier nulls of -55 to -65 db are achieved by judicious transformer construction and matching the legs of the bridge network. The bridge circuit uses a quad of diodes that are specially matched by the manufacturer for this application. Precision resistors are used in series with the diodes to minimize forward diode resistance effects. Constant loading of the detector circuit is provided by the shunt resistor R15. High frequency filtering is provided by C8 and C9.

Both the signal and reference frequency inputs are buffered by push-pull, transformer coupled amplifiers designed for good balance and low distortion. The reference amplifier is preceded by a hybrid integrated circuit (A43) differential amplifier that operates in limiting to give a non-variant switching source. Input impedances are 50 ohms for the signal and 100 ohms for the

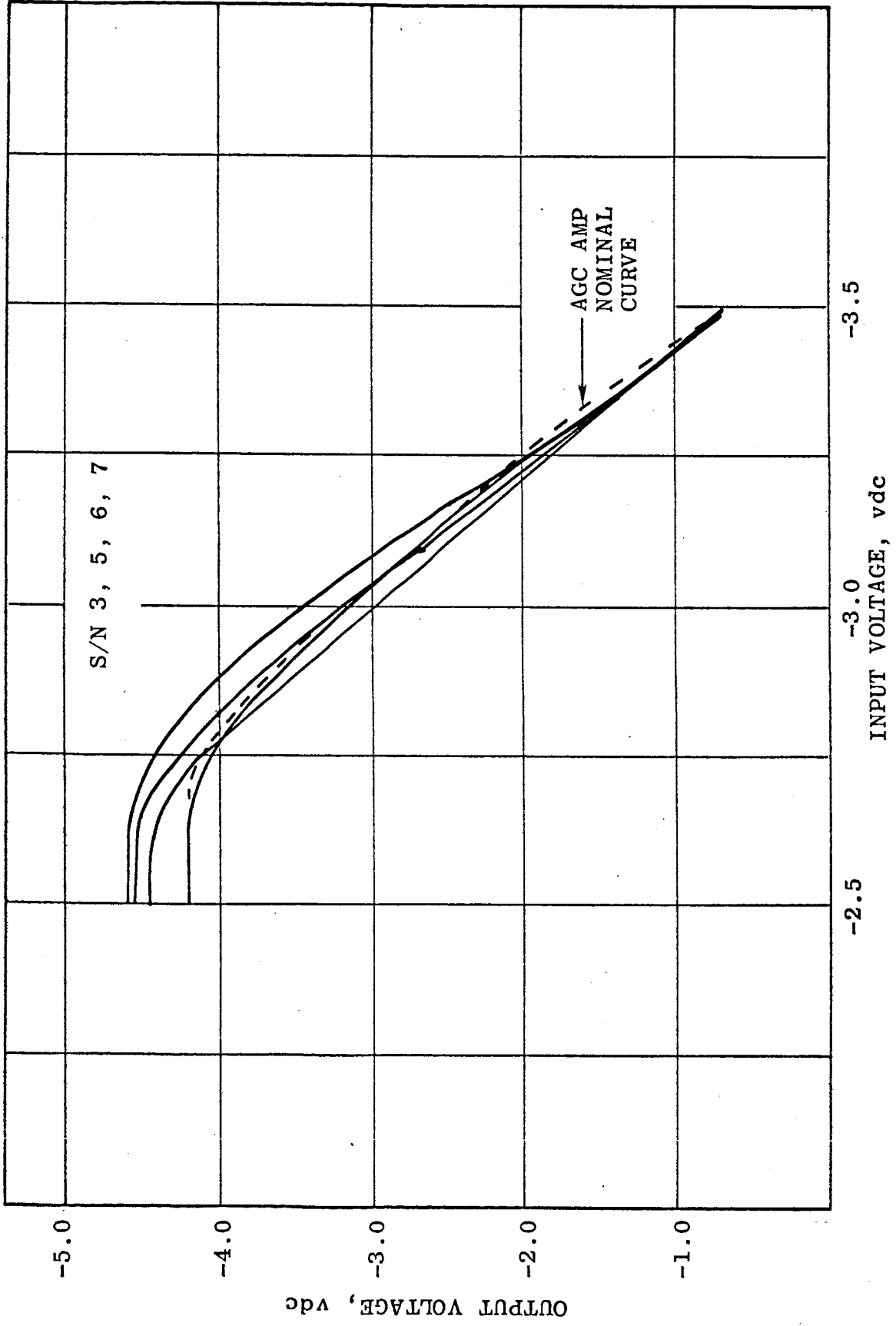


Figure 5-48. AGC Amplifier Gain Linearity

reference. Since both detectors are operated from a common reference, it is terminated in a parallel load of 50 ohms.

In normal system operation, the reference power is -3 dbm and the detector outputs are set by AGC for 1 volt peak-to-peak. This corresponds to an input power level of -14 dbm on the gain characteristic. Output limiting occurs when input power level is 0 dbm to 5 dbm. Each detector module uses 26 ma from the 9 vdc supply. Refer to Figure 5-49 for test data results.

Amplifier and A_L Demodulator

The A_L demodulator operates upon the output from the coherent amplitude detector. It rectifies the chopped carrier signal to provide coherent AGC voltage and a carrier loop lock indicator voltage. Gating is used similar to the G_C gates in the carrier loop and the demodulated signal is peak detected and amplified. Preceding the A_L demodulator is a video amplifier with a gain of 2.15 which is also used to distribute the modulation to other detectors.

The output level of the A_L demodulator varies with signal strength and is nominally -2.5 to -3.5 volts with the carrier loop locked. Figure 5-50 is a model of the circuit, and Figure 5-51 is test data of the demodulator gain.

S1 and S2 are MOS field effect transistor switches which provide no signal path offset voltage, high off impedance and fast switching (500 ns maximum including the driver circuit). They are switched by a hybrid integrated circuit driver that translates the digital logic levels to the required higher level control voltages (-15 vdc and +9 vdc). The G_C code control logic signal is the correlation reference signal which operates the choppers S1 and S2.

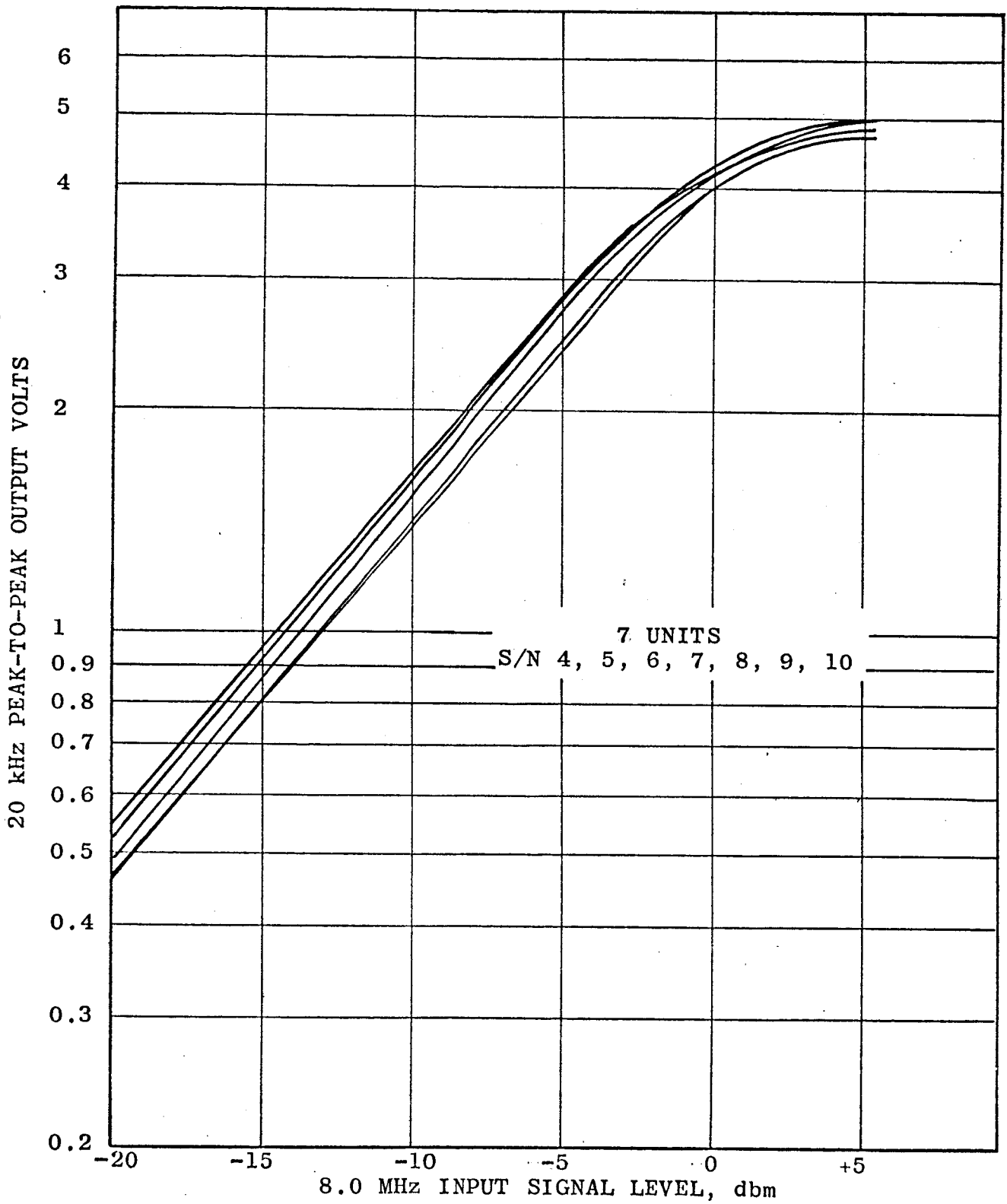


Figure 5-49. 8 MHz Balanced Detector 20 kHz Gain and Linearity Curves

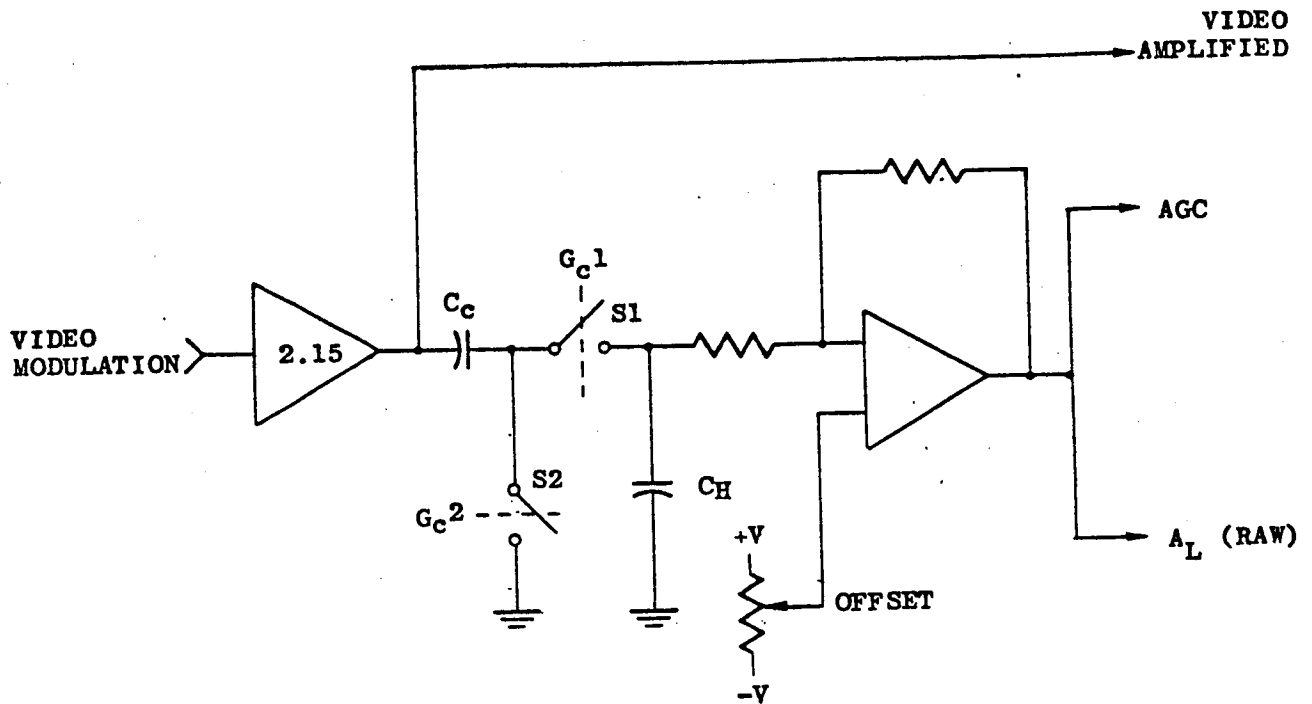


Figure 5-50. Amplifier and A_L Demodulator

In operation, a bi-polar modulation is received and doubled by the fullwave switching action. The detected signal is stored on holding capacitor C_H which maintains the AGC voltage between code pulse sequences. The output amplifier raises the signal by a factor of approximately 2. Overall signal gain through the module is approximately 7.

The output amplifier has an offset adjustment for nulling static signal path voltages which includes the balanced detector offset. The module uses 24 ma at 6.2 vdc, 26 ma at -6.2 vdc, and 3 ma at -15 vdc.

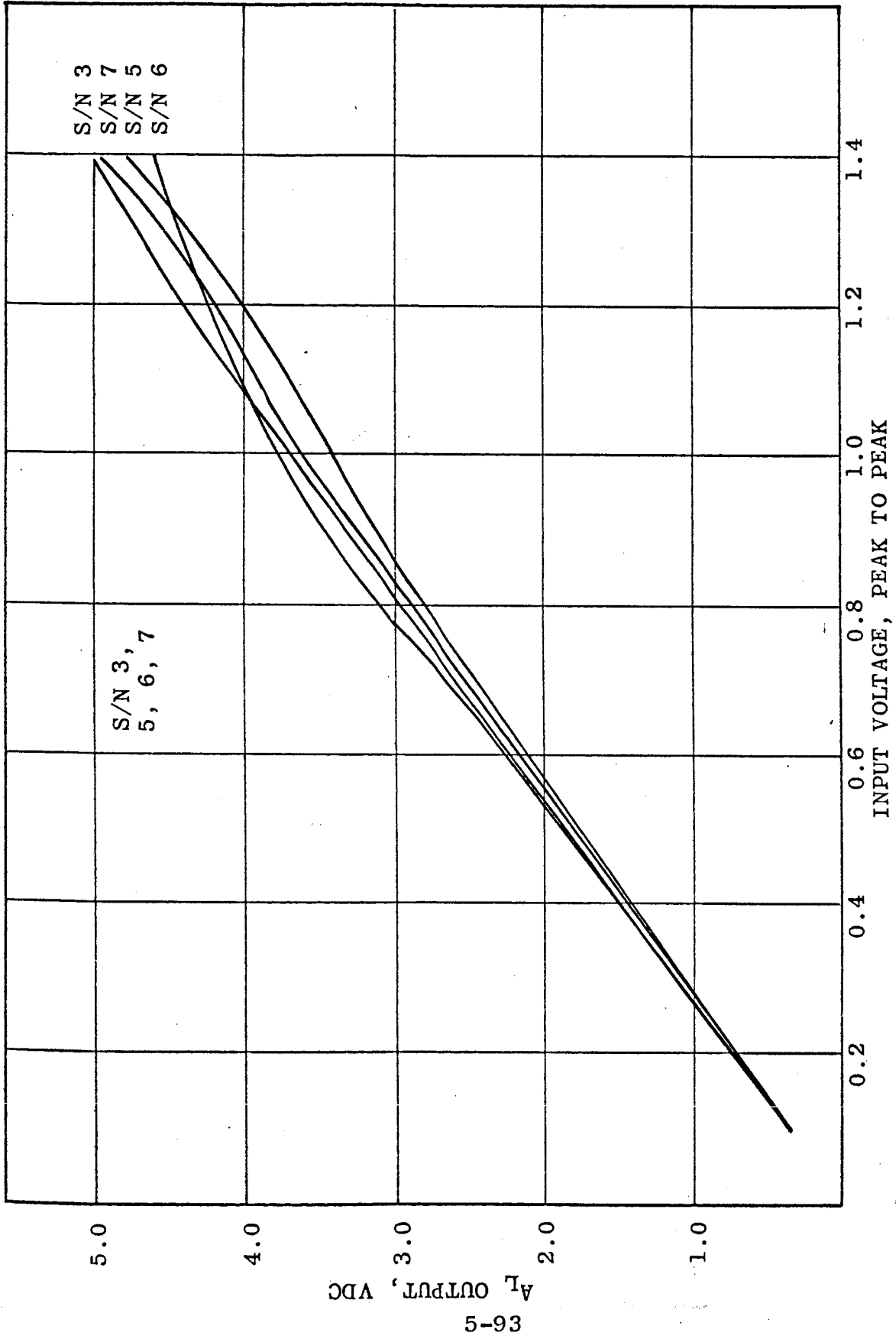


Figure 5-51. AL Demodulator Gain

G_C Gate and Carrier Loop Filter

The input to this module is a video signal derived from a balanced detector in the received signal path. This signal contains both the amplitude and the sense of the receiver carrier tracking error. The form of this signal is shown in Figure 5-52.

The peak amplitude is proportional to the magnitude of the tracking error, and the phase determines the sign of the error. The G_C gate performs full-wave demodulation which is then filtered and amplified in the carrier loop filter.

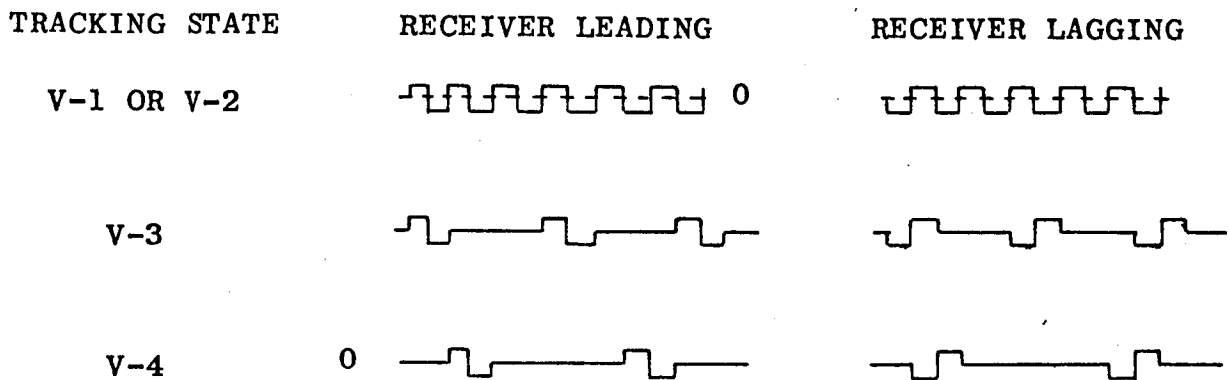


Figure 5-52. Carrier Loop Filter Input Signal

The carrier loop filter parameters are dictated by the desired overall carrier loop response. As derived in Reference 6 the desired transfer function of this module takes one of three forms, depending on the particular tracking state of the receiver. These transfer functions are:

V-1 or V-2	$H = 48 \frac{1 + .00125S}{1 + 15.75S}$
V-3	$H = 24 \frac{1 + .00375S}{1 + 15.75S}$
V-4	$H = 12 \frac{1 + .00375S}{1 + 15.75S}$

In addition to providing the correct transfer function, the module includes an adjustment for cancellation of static offset voltages, and an additive input for application of the carrier preset signal.

The change of the desired gain factor between states is accomplished by simply averaging the demodulated signal. Referring to Figure 5-52, the error signal is present full time in states V-1 and V-2, one-half time in V-3, and one-fourth time in V-4 which provides the correct gain ratios.

A simplified model for the circuit is shown in Figure 5-53.

The G_C gate section is a voltage doubling detector which delivers a sample of the input peak-to-peak voltage to the average resistor R_{av} during the time when G_{C2} is closed. The values of R_{av} and $C1$ have been chosen to provide a net gain through the gate of $3/2 T/T_1$ when operating from a 1000 ohm source impedance where T/T_1 is the duty cycle of G_{C2} . T/T_1 provides the variable gain between the acquisition states.

G_{C1} and G_{C2} are implemented with metal oxide semiconductor field-effect transistors (MOS FET) having high off impedance, relatively fast switching speed (500 ns maximum including its driver circuit), with no temperature dependent signal path parameters. Level shifting transistors are required as interface elements between the logic elements which generate the gating signals and the MOS FET. This interface consists of a specially designed hybrid integrated circuit (A32) shown in the schematic as A-1 and A-2. The high logic state (one) is translated to +9 volts for an open switch position and the low logic state (zero) translates to -15 volt and closes the switch.

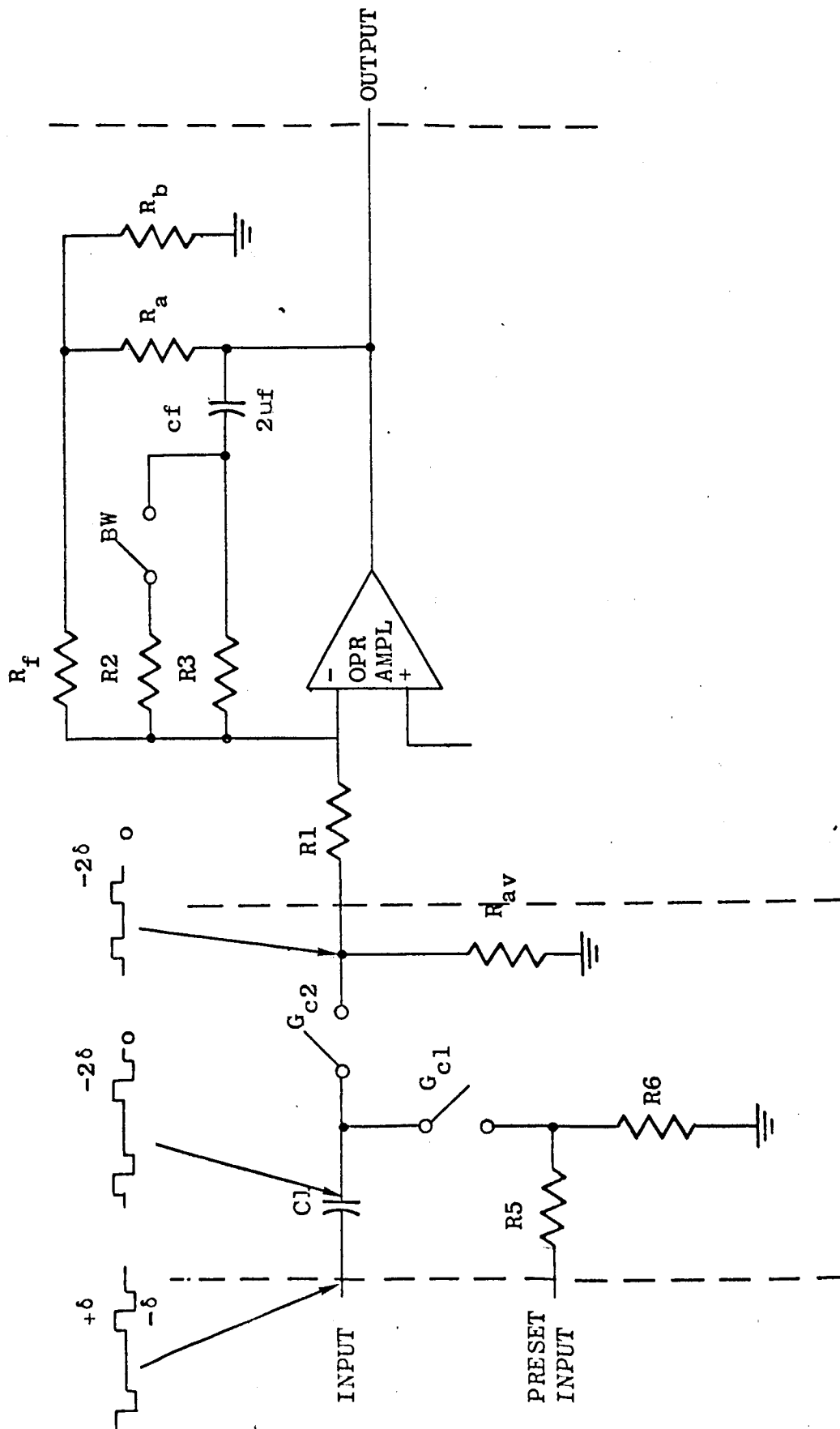


Figure 5-53. G_c Gate and Carrier Loop Filter

The loop filter amplifier is mechanized with a monolithic integrated circuit operational amplifier MC 1531. The transfer function of the filter amplifier is

$$H_{fA} = \frac{R_a + R_b}{R_b} \cdot \frac{R_f}{R_i} \cdot \frac{1 + R_2 C_f S}{1 + \frac{R_a + R_b}{R_b} R_f C_f S} = A \frac{1 + \tau_2 S}{1 + \tau_1 S}$$

where $R_i = R_1 + G_C$ gate output impedance. R_2 is changed in value by switching between states.

The input signal is a square wave with half amplitude about ground and having no DC component. After demodulation, this waveform is summed on R_7 and is further amplified by the operational amplifier A-3 whose gain is set by R_9 , R_{11} , R_{12} , and R_{13} . The amplifier is an active low pass filter which determines the loop bandwidth. (Refer to Figure 5-54 for test data results.)

Bandwidth is changed by switching the lead parameter, τ_2 , by shunting the resistance component of the lead network with a MOS FET switch and thus not changing the voltage on the series capacitor. This implementation prevents switching transients that could unlock the loop.

The carrier loop preset sweep voltage is scaled with R_5 and R_6 and summed with the input modulation. In V-0 and V-1 this error signal keeps the carrier VCO bounded within lock range by comparing it to a reference frequency from the frequency synthesizer subsection. The potentiometer R_{22} nulls static offset voltages up to plus and minus 60 millivolts. All power lines are heavily filtered. A theoretical presentation of this circuit is given in reference 6.

This module uses 4 ma at 9 vdc, 14 ma at -6.2 vdc, 14 ma at 6.2 vdc and 3 ma at -15 vdc.

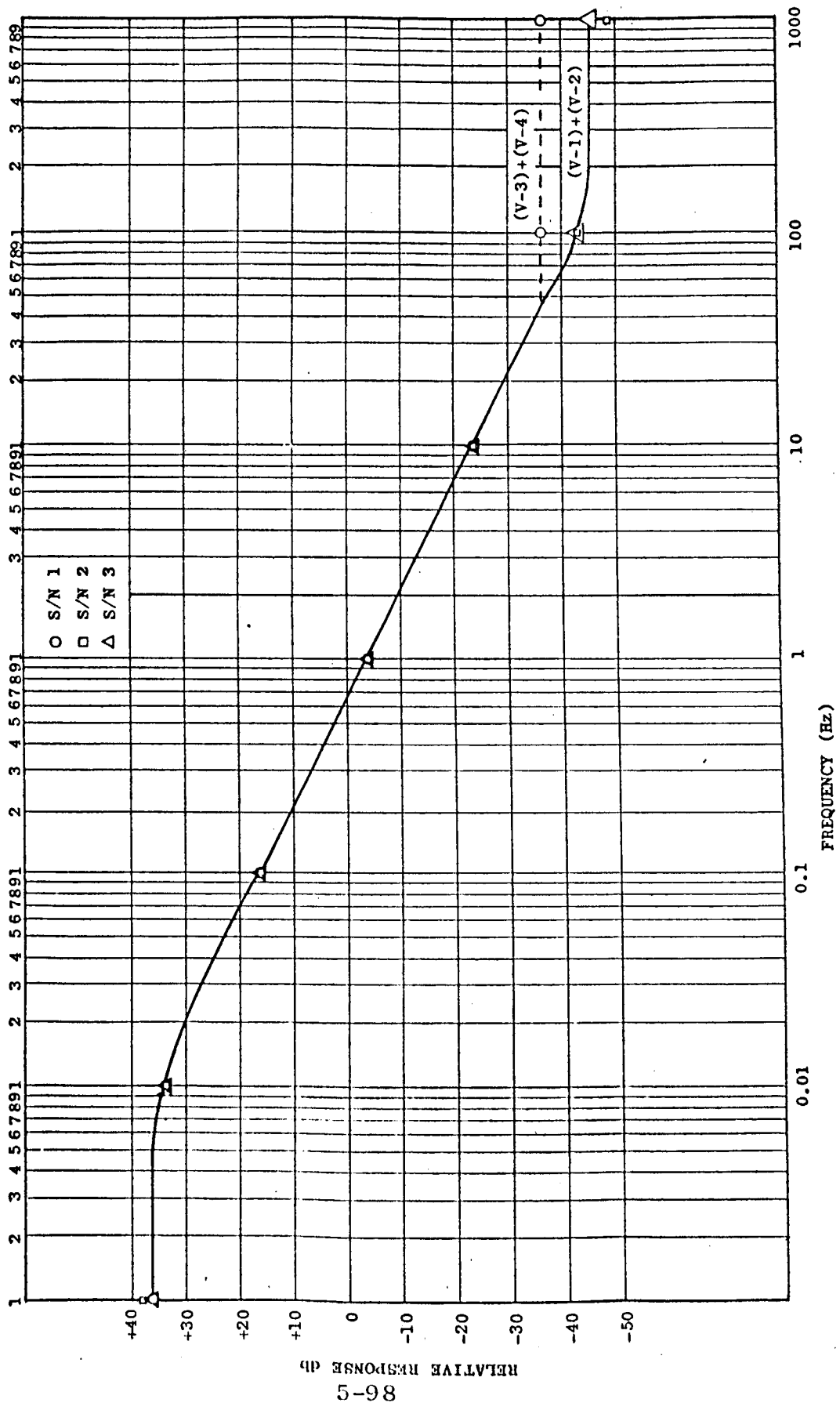


Figure 5-54. Gc Gate and Carrier Loop Filter Test Data

6 MHz Voltage Controlled Oscillator

The 6 MHz VCO is used in the carrier tracking phase lock loop and provides a gain of 120 kHz/volt. Absolute frequency stability is ± 0.05 percent over the vehicle temperature environment. The oscillator circuit configuration uses LC series resonant feedback. Frequency control is obtained with varicaps which are a part of the feedback circuitry. Employing two diodes in series increases the gain by producing a large L to C ratio. (See Figure 5-55).

The oscillator circuit is configured around the A43 medium power, hybrid integrated circuit amplifier. Additional power gain in the feedback loop is provided by the emitter follower Q2 which has low output impedance. A 4 db power gain margin under worst case operation has been calculated for the oscillator. Internal voltage regulation is used for the amplifier and diode bias and the frequency temperature compensation is obtained by controlling the regulator voltage over temperature variation. (See Figure 5-56). This is done primarily with diodes CR1 and CR3. An effect of the compensation is to change the L/C ratio and thus oscillator gain. Gain variation is ± 10 Hz/ volt over the temperature environment.

R₉ and C2 provide filtering of the reference diode whose noise tends to modulate the oscillator through the load resistor R₃. A buffer output amplifier is provided which operates in limiting and makes the oscillator insensitive to loading. There are two outputs and each is loaded differently. The output with matching section gives 0 dbm into 50 ohms. The second output interfaces with a hybrid differential amplifier on the MTL frame. The circuit occupies one-half of a RF module and uses 19 ma at -15 volts under nominal operation.

5.5.2.6 Modulation Tracking Loop, Module Operation and Test Results

Frame Filter M

The circuit configuration and operation of Frame Filter M is identical to that of Frame Filter T discussed in paragraph 5.4.2.5.

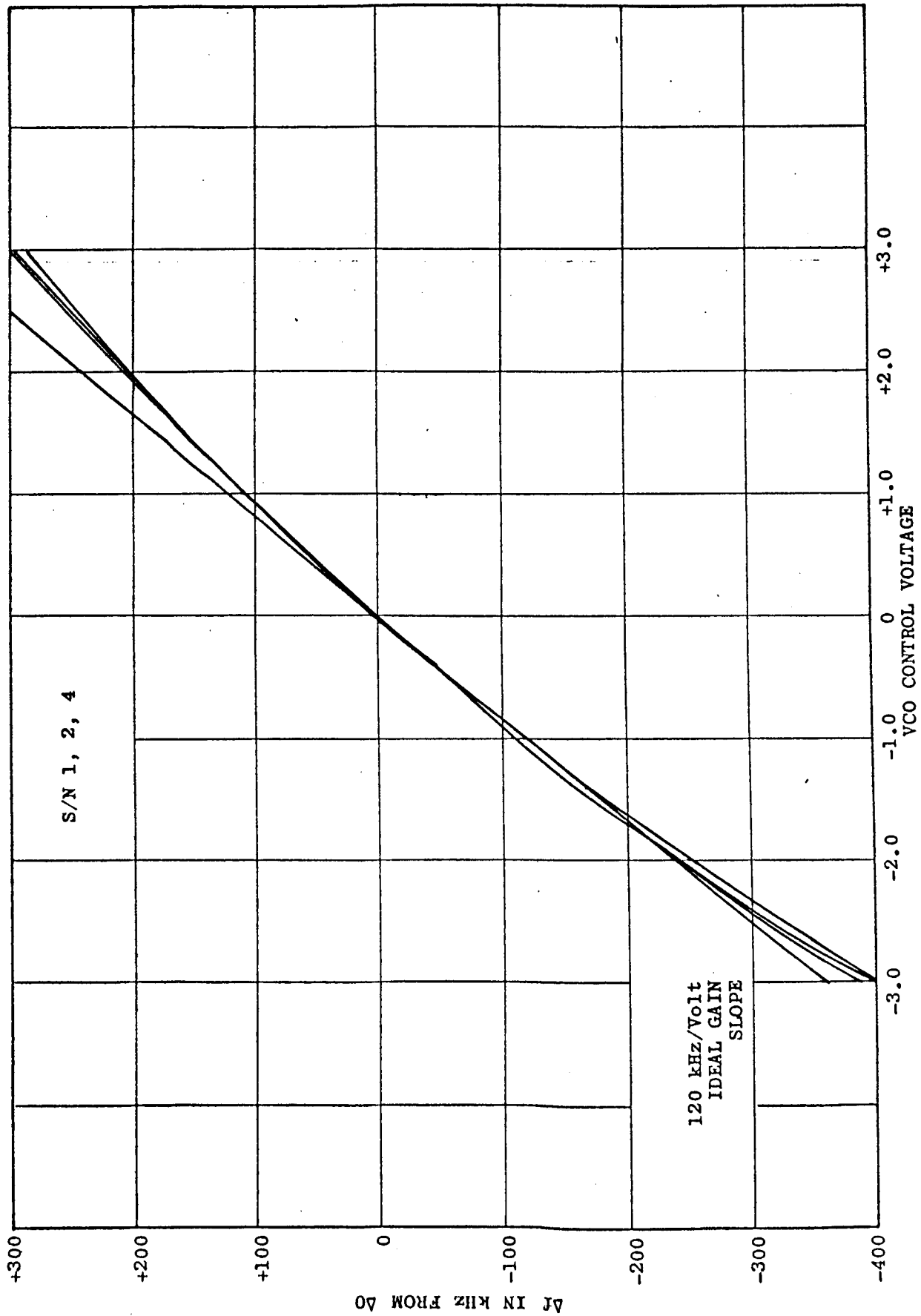


Figure 5-55. 6.0 MHz VCO Gain

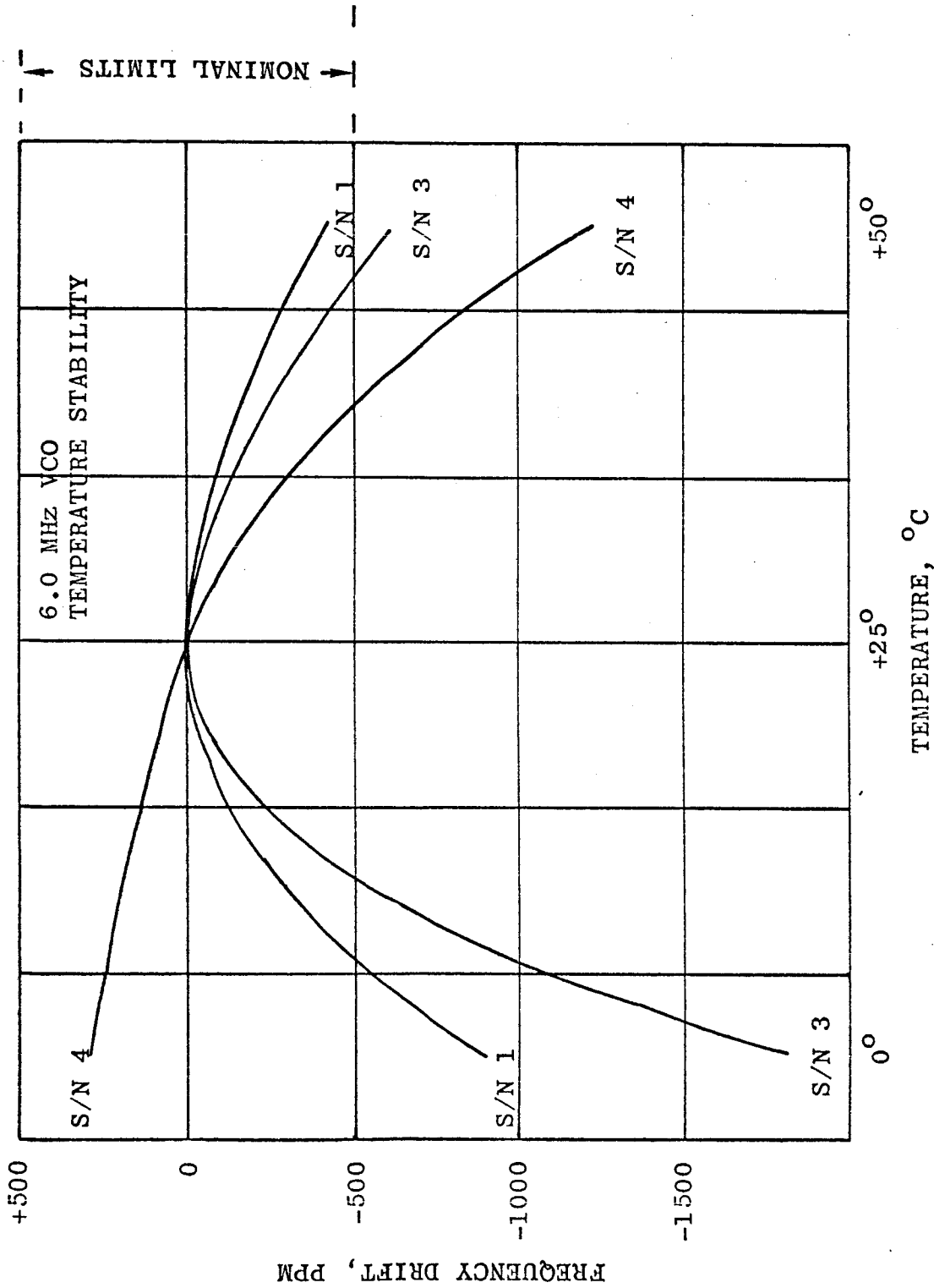


Figure 5-56. 6 MHz VCO Test Data

A difference between the two modules exists in the value of the series dropping resistors for the plus and minus 6.2 vdc outputs and thus the load current capability. See Figure 5-57.

A_H Data Demodulator

The A_H, data demodulator operates in conjunction with two other modules -- the A_L, A_H, data matched filter module and the A_L, A_H and data digital module. This latter module is contained in the receiver code control subsystem. The three modules perform the function of extracting the proper signals from the noisy input waveforms and converting them to a binary level. The circuitry is contained in three modules simply because of packaging considerations, not because of electrical functions. The A_H, data demodulator module contains the switches from the integrate and dump matched filters. The A_L, A_H, data matched filter module contains the matched filters. The A_L, A_H and data digital module generates the switching signals and converts the analog filter output to a binary level.

Two identical separate demodulators, and the A_L integrate and dump switch are located in this module. Each demodulator uses two MOS field effect transistor switches for full wave demodulation. A differential output is thus provided for better common mode noise rejection. Each demodulator has a current bias adjustment for setting the matched filter threshold. The demodulator switches also provide the match filter dump function. When commanded from the code control, both switches are closed simultaneously, thus dumping the stored charge on the integrator capacitors.

Test data for this group of modules is presented in Figure 5-58. The input voltage is integrated for variable amounts of time until the dumped signal is sufficient to change the binary output. The input voltage is set at three different levels for each demodulator section; A_H, A_L and data. A model of this circuit including the matched filter module is presented in Figure 5-59.

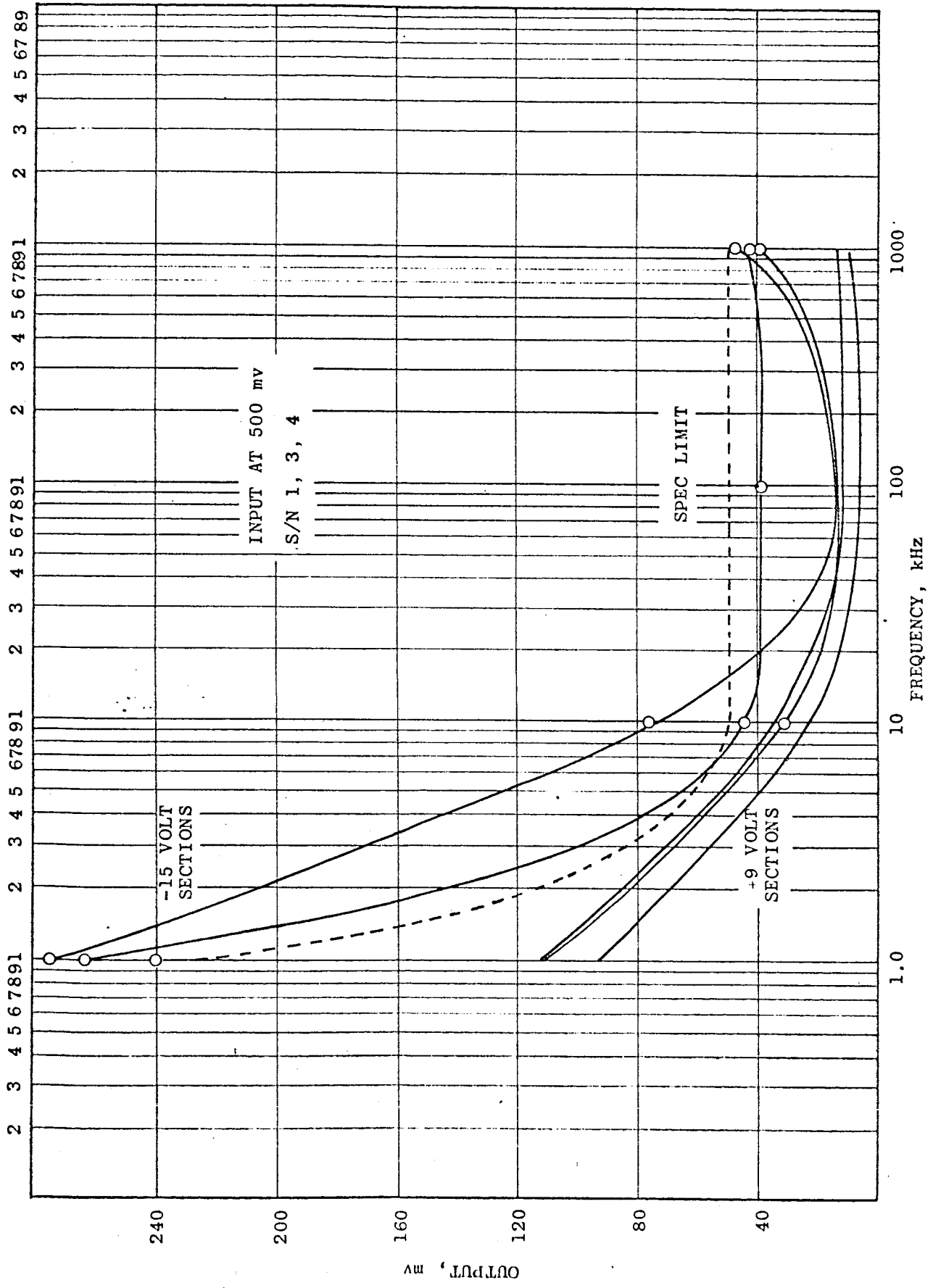


Figure 5-57. Frame Filter, Type M Output Voltage vs Frequency

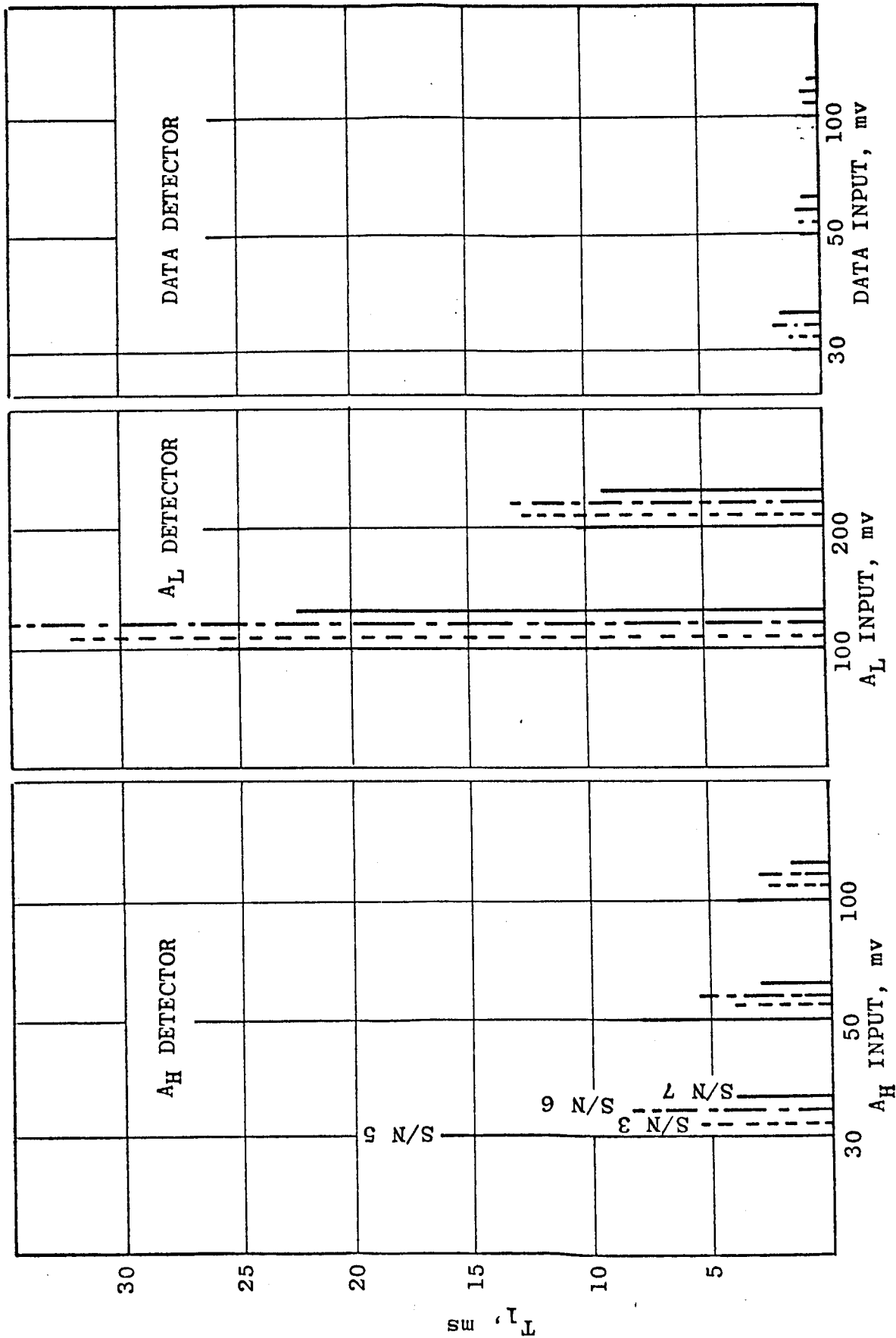


Figure 5-58. AH and Data Demodulator and AH, AL and Data Matched Filter Modules Detector Characteristics

A_L, A_H, Data Matched Filter

The A_L, A_H, data matched filter works in conjunction with the A_H, data demodulator module described above. A model for one demodulating section is shown in Figure 5-59.

The Data and A_H Demodulators accept the data output of the tracking receiver balanced detector. The A_L matched filter accepts the output of the A_L demodulator. When signals are present and time correlation occurs, dumping the integrator causes a pulse to set the data storage flip-flop. The data channel coded transmission is sampled each half L-code period, while the A_L and A_H states are sampled each full L-code period.

In the case of "Data" demodulation particularly, a means was needed to integrate and hold small intervals of data input for a relatively long period of time. The data modulation has a worst case integrate to hold ratio of 1/16 in time. The worst case for the A_H input is a ratio of 1/4.

To mechanize this integrate-and-hold, a high quality switch and a high input impedance amplifier is required. At the end of the integrate-and-hold period, the contents of the integrator are sampled. When the stored charge on the integrating capacitors is dumped to ground, the resulting voltage transition passes through the small coupling capacitor into the amplifier. AC coupling provides a high input impedance to low frequencies of the integrate and hold thus improving circuit operation.

The differential integrator circuit doubles the effective gain as well as providing common mode noise rejection.

The dump signal transient is shaped, amplified, and coupled to the storage flip-flop. The polarity of the dump signal transient determines the state of the storage flip-flop and this information is stored until the next sample period.

The high quality switches are implemented with MOS field effect transistors. They provide a very high off-to-on impedance ratio, good isolation of the signal from the gate drive circuits, and fast switching speed.

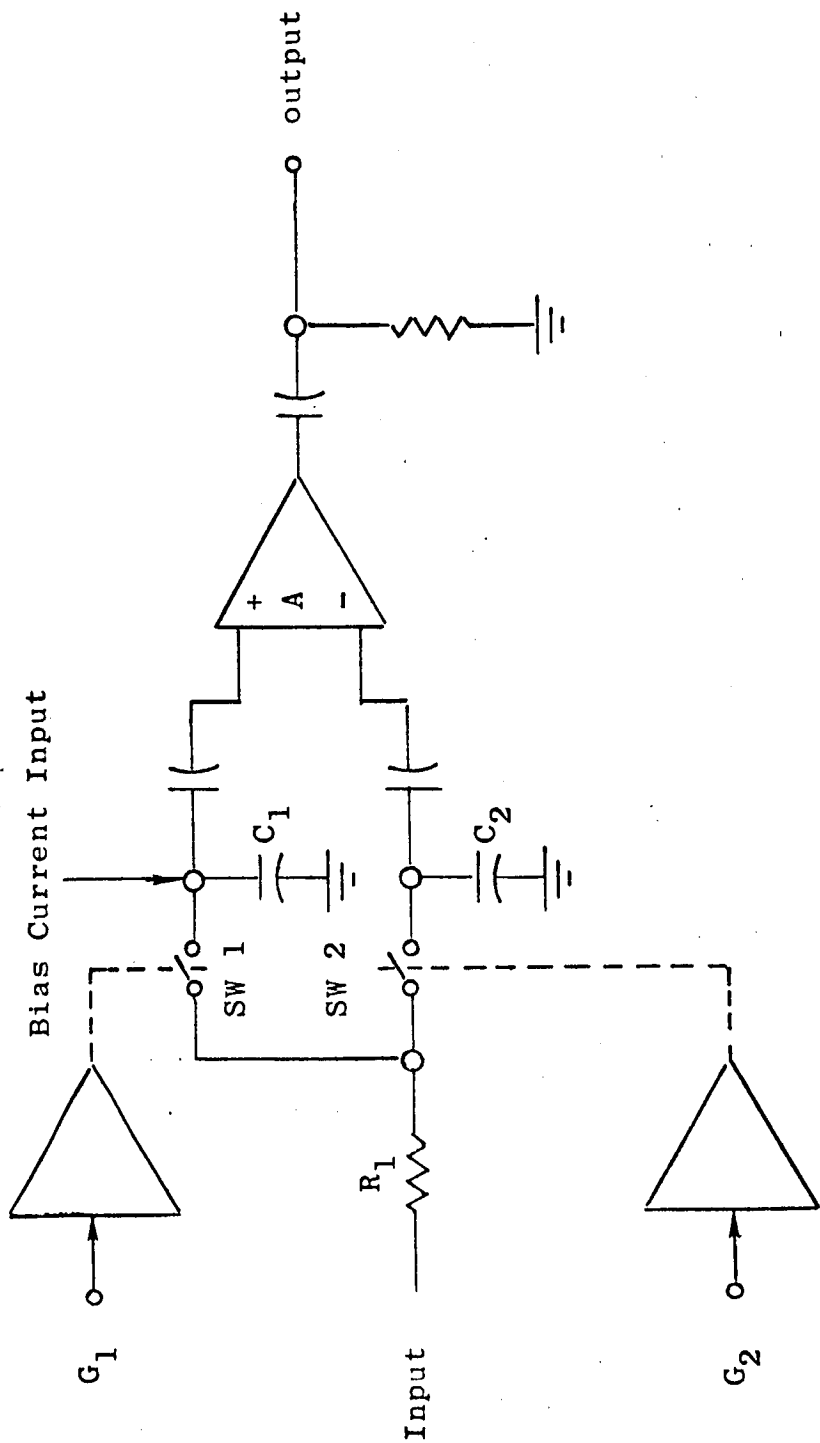


Figure 5-59. Integrate and Dump Matched Filter

A bias current is applied to one of the integrating capacitors to:

1. Overcome the inherent offset in the A_H and data circuits thus removing any circuit bias.
2. Provide a variable threshold setting in the A_H circuit so that in the no signal (noise only) condition the "0" state can be set properly.

The A_L demodulation is performed in the amplifier and A_L demodulator module producing a DC level output. A simple single ended integrator circuit is used. A variable potentiometer threshold capability is also provided in the A_L circuit.

Range Loop Filter

The range loop filter module has a series pass switch (Q1) that demodulates range tracking modulation and provides an error signal for the phase locked range loop. The error signal is then amplified and smoothed by an active low pass filter comprised of two fixed gain operational amplifiers. Loop filter bandwidth is switchable by the code control subsection. In states V-0, V-1, V-2, and V-3 (Figure 5-60) the filter bandwidth is limited primarily by the amplifier compensation networks and the range loop is a type I, first order loop.

In the track mode V-4, the MOS field effect transistor Q2 is enabled and negative feedback is applied through C6 to the amplifier A-2 without switching transients. This changes the loop to a type I second order tracking filter with a low pass noise bandwidth of 5 Hz. The forward gain, which is that of gate Q1 and amplifier A-2, is 32. Amplifier A-4 has a fixed gain of 10 that effectively multiplies the capacitor C6 in the feedback loop and provides the required low frequency response with realizable components. The potentiometer R13 nulls static signal path offsets and system time delays which appear in the loop as offset voltage. It can deviate plus and minus 100 millivolts referred to the amplifier input.

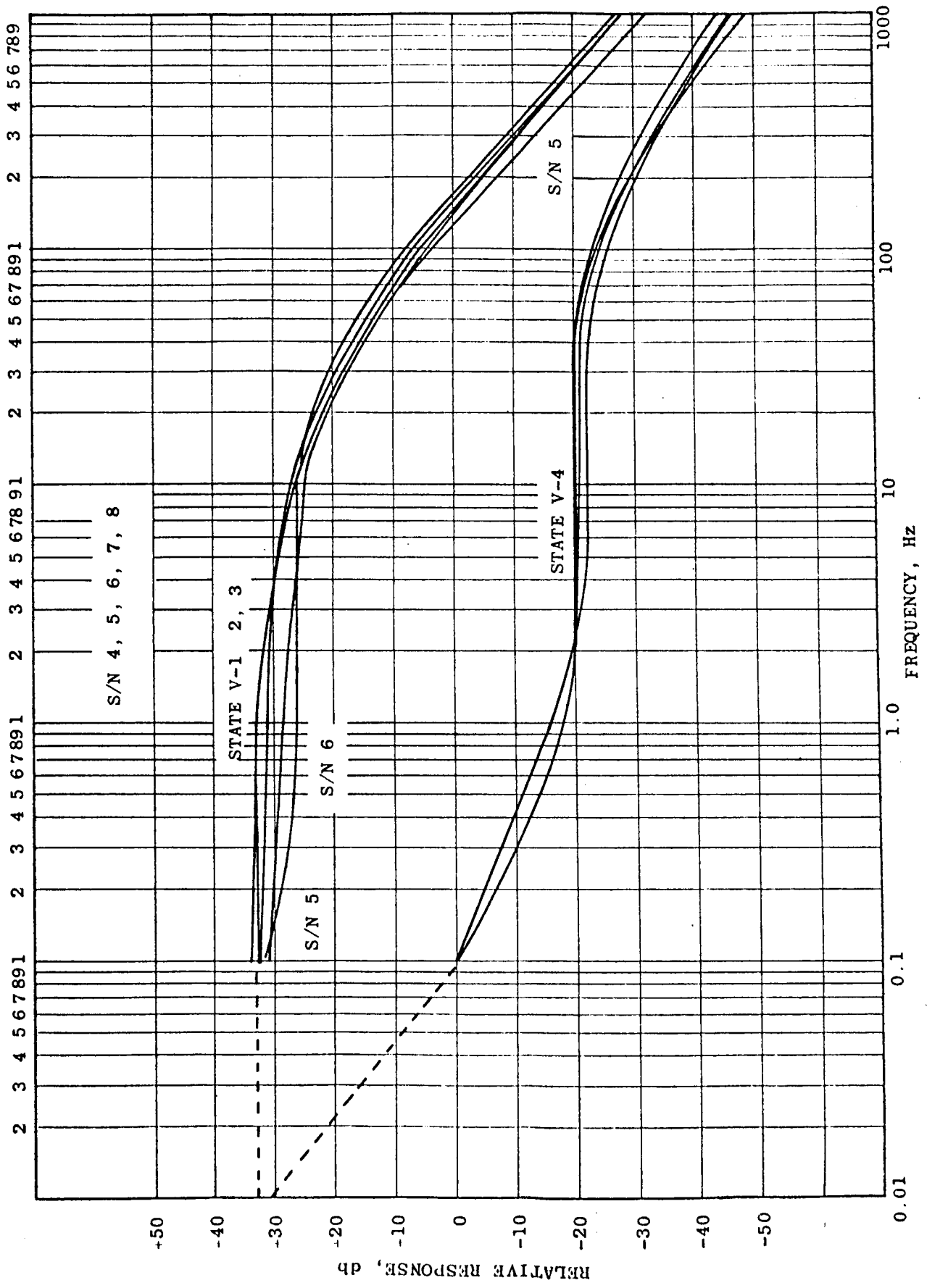


Figure 5-60. Range Loop Filter Response

The H-code search sweep input voltage is scaled down by the resistor network R7-R8 and applied to the offset error point. The sweep voltage causes the range loop to be modulated approximately plus and minus 6 H-code bit periods to capture exact correlation. A theoretical model and description of this circuit is given in reference 6, page 51. This module uses 25 ma at +6.2 volts, 23 ma at -6.2 vdc, 5 ma at -15 vdc, and 3 ma at +9 vdc.

12.7 MHz VCO and Mixer

The 12.7 MHz VCO and mixer module is used in the ranging phase lock loop to derive the clock signal for the PN code generator. The absolute frequency stability of the oscillator is ± 5 ppm over the vehicle temperature range (see Figure 5-61 and 5-62).

The oscillator circuit uses a crystal control configuration with a gain, K_{VCO} , of 500 ± 50 Hz/volt. An A43 medium power hybrid integrated circuit differential amplifier is used for the active device. The tuned transformer T1 is used for power matching and to adjust the center frequency. C5 and the primary inductance of T1 are tuned to prevent spurious or non-crystal controlled operating modes. Secondary transformer inductance plus L2 tune to the resonant frequency with the effective capacitive reactance of the parallel network L3, L4, CR4, and CR5. CR4 and CR5 are variable capacitance diodes used for frequency control. The voltage controlled series resonant equivalent circuit operates against the series resonant impedance of the crystal. As the controlled impedance is varied the crystal impedance changes accompanied by a compensating frequency deviation thereby providing a $\Delta F/\Delta C$. Since the control diode capacity is voltage sensitive it may be expressed as a $\Delta C/\Delta V_B$ control function. K_{VCO} then is

$$\frac{\Delta C}{\Delta V_B} \cdot \frac{\Delta F}{\Delta C} = \frac{\Delta F}{\Delta V_B} \cdot \frac{\text{Hz}}{\text{Volt}}$$

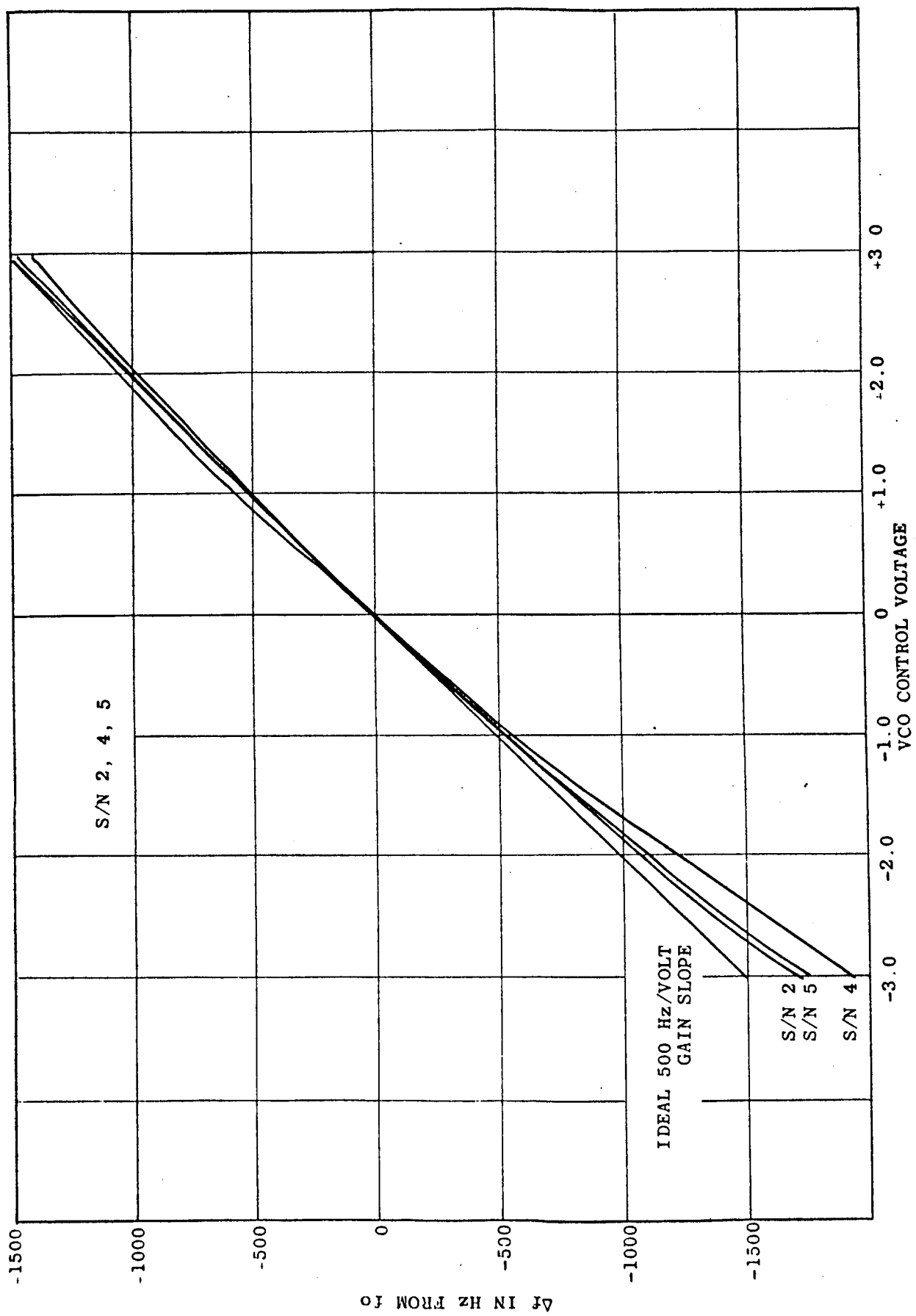


Figure 5-61. 12.757447 MHz VCO Gain

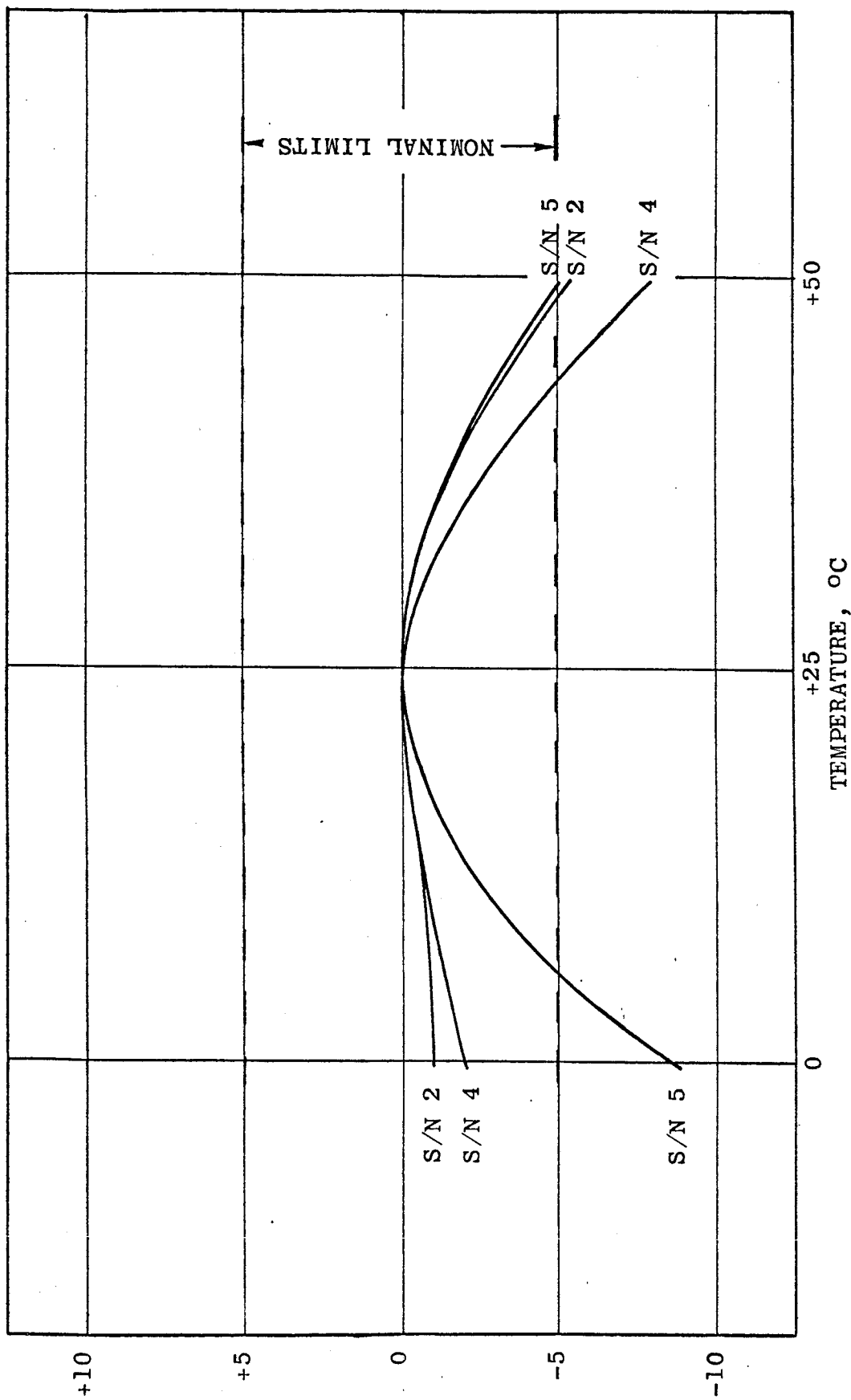


Figure 5-62. 12.757447 MHz VCO Temperature Stability

The change in capacity per unit voltage is small (about 1.2 pf/volt) which does not lead to high K_{VCO} gains. L3 and L4 are used in the circuit for Q multiplication by resonating with a large portion of the control capacity. The small equivalent capacitive reactance is series resonant with L2 and T1. Because of the Q multiplication the circuit is sensitive to parameter tolerance and L3 and L4 are selected at test to adjust the required gain and compensate for diode tolerances.

The oscillator module has an internal voltage regulator which makes it insensitive to supply variation. It changes the control diode bias voltage with temperature variation to compensate the oscillator. The oscillator output signal drives a mixer-shaper circuit in the same module.

The mixer circuit is a basic diode mixer driven by an A43 differential amplifier. This type of mixer is used commonly throughout the AROD vehicle equipment. Input resistors R7, R8 and load resistor R10 are selected to optimize mixing at the input power levels supplied. Q3 and Q4 are cascade amplifiers which raise the signal to a limiting level in amplifier Q4 and trigger the ST1 shaper acting as a monostable multivibrator operating at the difference frequency. The multivibrator provides a 260 nanosecond wide pulse for the flip-flop phase detector in the transfer or rate-aid loop.

Power required for the module is 21 ma at -15 vdc and 2.5 ma at +3.5 vdc.

12.8 MHz VCO and Loop Filter

The 12.8 MHz VCO and loop filter is part of the rate-aid loop which positions the PN code generator in the modulation tracking loop as a function of Doppler in the carrier tracking loop. The loop filter shapes and smooths the phase detector output and provides an error signal for the VCO. The VCO output drives the PN generator.

The 12.8 MHz basic oscillator is identical to the 12.7 MHz oscillator since oscillator tuning is broad enough for both

frequencies. K_{VCO} is 500 ± 50 Hz/volt and absolute stability is ± 10 ppm over the temperature environment. An A43 hybrid integrated circuit differential buffer output amplifier supplies two isolated outputs. Both circuit functions are contained in the module and are connected together externally to allow testing each circuit separately.

The loop filter input waveform is a varying pulse width digital signal operating between 0.2 to 2.8 volts. At zero phase error, the DC value is half the peak voltage. The DC component varies as a function of phase error. This signal is applied to the loop filter which is implemented with an operational amplifier. A voltage bias equal to half the peak voltage is applied to the positive amplifier terminal causing a zero output when no phase error exists. The potentiometer R2 adjusts the offset voltage for nulling phase error under static operating conditions. The offset bias voltage is derived in the digital module containing the phase detector and exhibits the same DC temperature drifts as the input signal, thus nearly cancelling each other. (Refer to Figures 5-63, 5-64, and 5-65).

The feedback amplifier circuit provides voltage gain in addition to being a lead-lag active filter. Its transfer function is as follows:

$$H(S) = \frac{(-22.8) (1 + 0.0015 S)}{(1 + 0.0345 S)}$$

Capacitors C1, C2, C5, C6, C8, C9, and C17 supply filtering to minimize spurious signals and noise at the VCO control point. This module uses 22 ma at -15 vdc, 8 ma at 6.2 vdc, and 9 ma at -6.2 vdc.

Vehicle Receiver Rate Aid Loop Divider ($\div 141$)

The function of this circuit is to divide the frequency output of the 6 MHz VCO by a factor of 141 and compare the phase of the resulting signal to the phase of a 43 kHz input signal. The phase detector output is used to drive the transfer loop filter thus providing rate aid to the 12.8 MHz VCO derived from the Doppler in the carrier tracking loop.

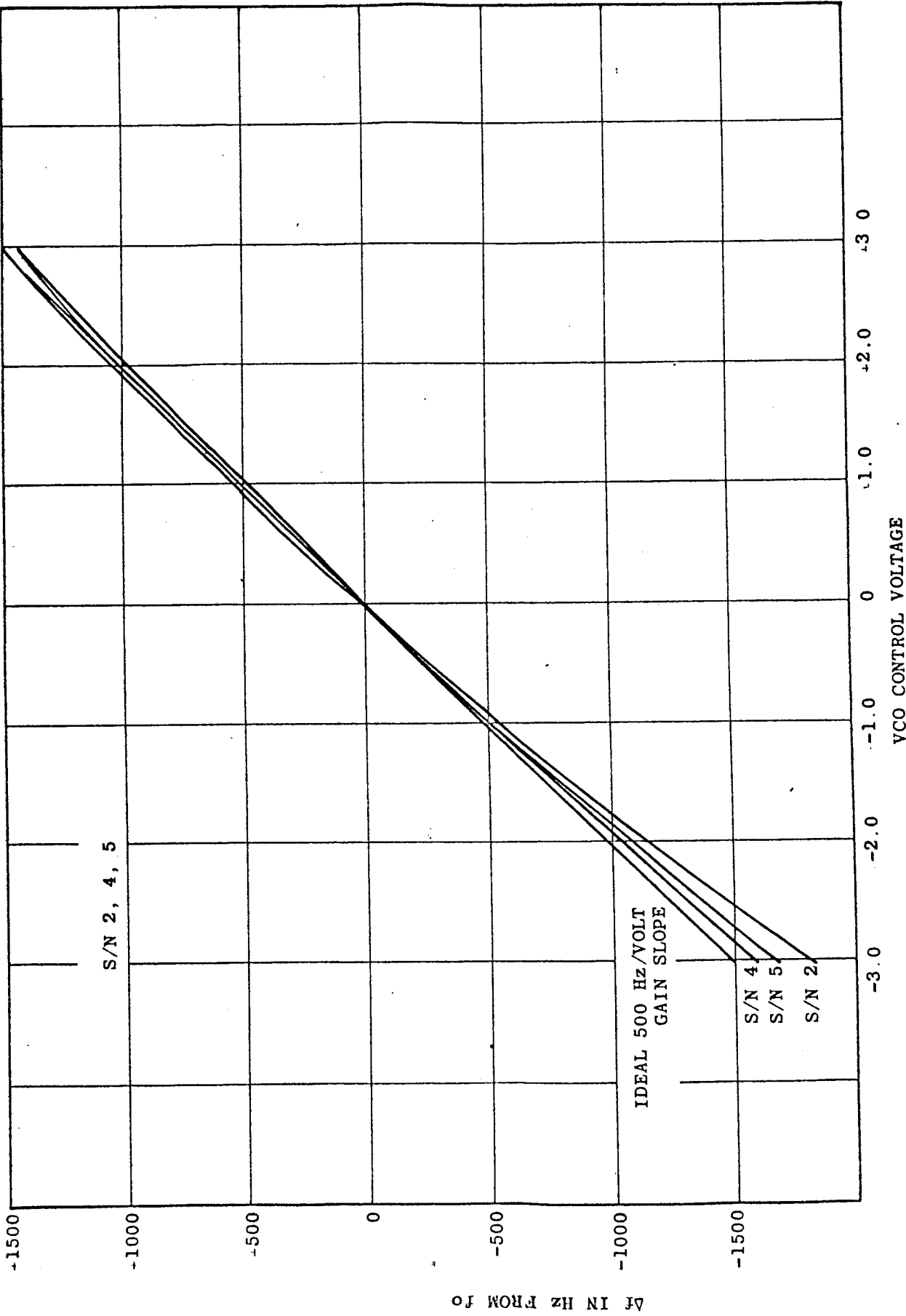


Figure 5-63. 12.8 MHz VCO Gain

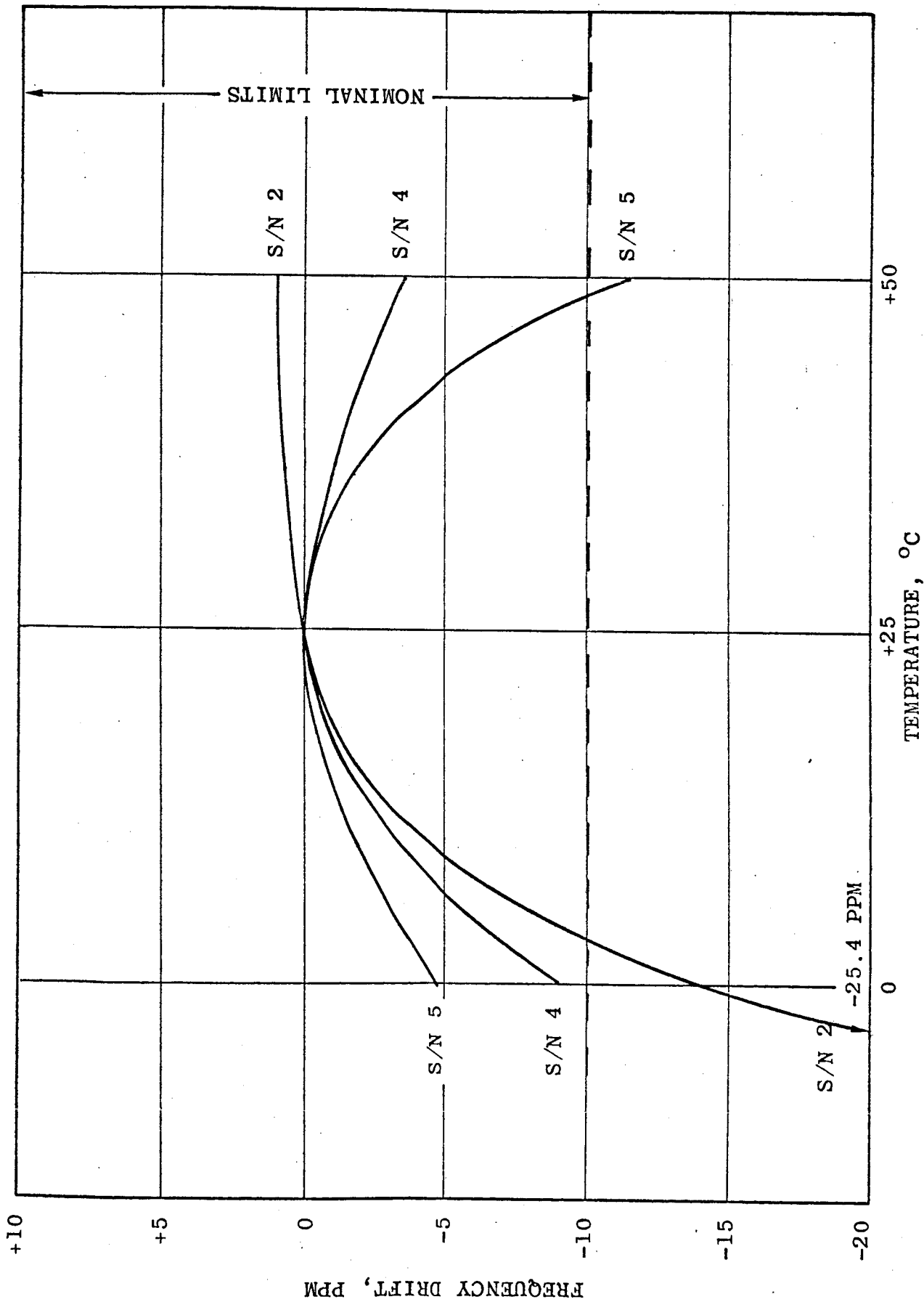


Figure 5-64. 12.8 MHz VCO Temperature Stability

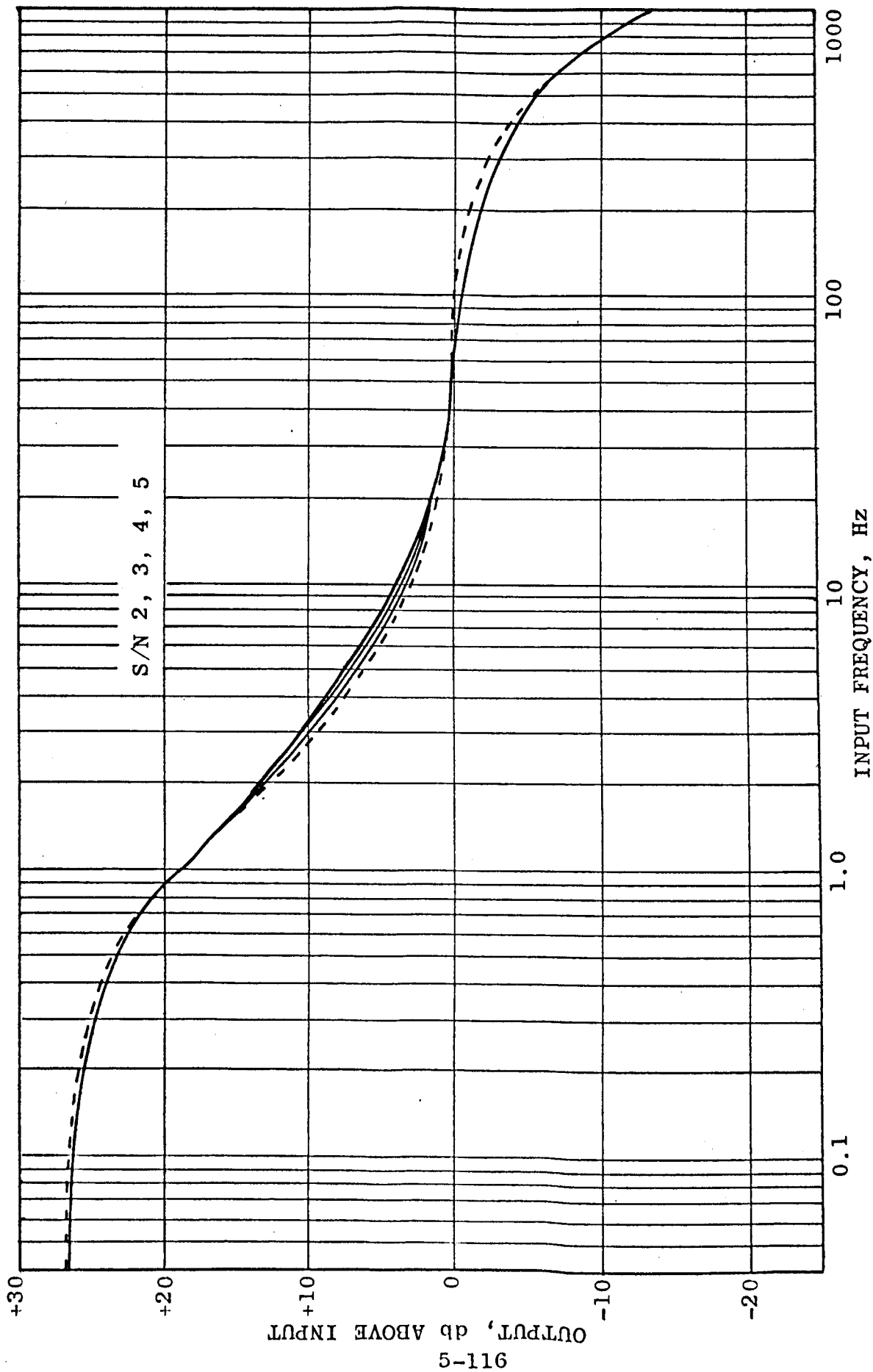


Figure 5-65. Rate AID Loop Filter Response

All circuits used are of the AROD selected digital family (Philco MW-3) except the square wave generator (A16 hybrid integrated circuit) used to buffer and shape the divider input.

The ÷141 module is implemented as a ÷3 circuit followed by a ÷47 circuit. The ÷3 circuit consists of two binary divider reset every three cycles of the input frequency.

The ÷47 circuit is driven by the output of the ÷3 circuit and is implemented as a six stage ripple counter which counts up to 63 (all "ones" state) and is reset to 17 (a "one" in the first and fifth stages) by the next drive pulse.

The all "ones" condition is detected by G6, G9, and G10. When this condition exists, clock pulses to FF3 and FF7 are inhibited by input 10 to G7 and input 2 to G21. However, the next clock pulse (after the pulse which set the all "ones" condition) is allowed to toggle FF4, which in turn toggles FF5 and FF6, and FF8 via gates G11 and G18, respectively. The all "ones" condition is the output of the ÷47 circuit with a frequency of $\frac{\text{DIVIDER INPUT FREQUENCY}}{141}$ and a pulse width of

$\frac{3}{\text{DIVIDER INPUT FREQUENCY}}$. The output of the ÷3 and ÷47 circuits are combined in a NOR gate giving the final divider output signal with a frequency of $\frac{\text{DIVIDER INPUT FREQUENCY}}{141}$ and a pulse width of $\frac{1}{\text{DIVIDER INPUT FREQUENCY}}$.

This module also contains two other circuits, a digital phase detector and a temperature compensating diode.

The digital phase detector consists of a single register element connected so that when the ÷141 output signal goes to a logic "one", the register output also goes to a logic "one". The register elements output will go to a logic "zero" when the phase detector input signal goes to a logic "one". The register element's output pulse width is proportional to the phase difference between the signals from the ÷141 circuit and the phase detector input.

The temperature compensating diode contained in this module is used in conjunction with the active loop filter in the rate aid loop to offset variations in the phase detector output signal due to temperature changes.

Frequency Preset (Reference Schematic: 69-23403G)

The Frequency Preset is a digital frequency discriminator used to preset a VCO to a reference frequency. This presetting technique is necessary in the transponder to program the S-band carrier VCO to the correct Doppler shift as measured by the VHF receiver. In the vehicle tracking receiver, the preset is used to program the S-band carrier VCO to the zero Doppler frequency. In both cases, presetting is required because the loop bandwidths are narrow with respect to the frequency uncertainty.

A discussion of the presetting technique is given in the AROD System Description Report, reference 1, Section 3.4.1. A simplified block diagram showing the relationship between the Frequency Preset and the carrier loop is shown in Figure 5-66.

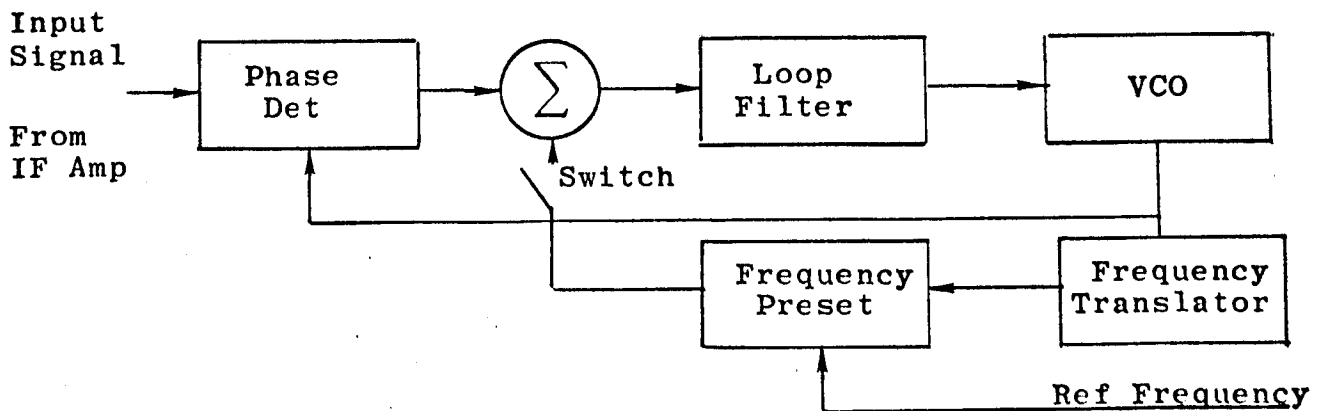


Figure 5-66. Carrier Loop Frequency Preset

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A sample of the VCO frequency is compared with a reference frequency by the Frequency Preset, and an error voltage is produced when the two frequencies differ. The polarity of the error voltage is determined by whether the VCO frequency is higher or lower in frequency than the reference frequency.

This error voltage is linearly summed with the phase detector output to program the VCO to the desired frequency. In the AROD application, the Frequency Preset is a two state device whose output is +V when the VCO frequency is high and -V when the VCO frequency is low. This will cause the VCO frequency to limit cycle about the correct frequency. When the input signal from the IF amplifier appears, the VCO will phase lock to this input signal through the Frequency Preset error voltage. After acquisition, the preset error voltage is removed.

It is not an easy task to construct a conventional discriminator for these loops as the accuracy of the preset requires very good discrimination at frequencies very close to the center frequency. For example, the vehicle requirements call for a discriminator with a center frequency stability on the order of 20 ppm. In a conventional discriminator the accuracy of the preset would be only as good as the stability of the discriminator itself. Replacement of the conventional discriminator with a digital frequency comparator using a very stable reference frequency would eliminate stability problems in the discriminator and allow discrimination to an accuracy of that of the reference frequency.

Figure 5-67 shows the method of the frequency comparison used in the Frequency Preset.

The unknown frequency f_w is mixed with the reference f_r at 0 degrees to form f_a , and with f_r at 90 degrees to form f_b in two difference mixers. The output of the two mixers, f_a and f_b , are the same frequency but are shifted in phase by 90 degrees. The phase compare circuit looks at the phase of f_b when $\alpha = \theta - \phi = 0$ degrees. In the case of Figure 5-67 where $f_w < f_r$, the frequency f_b will lead f_a by 90 degrees which will cause the output of the

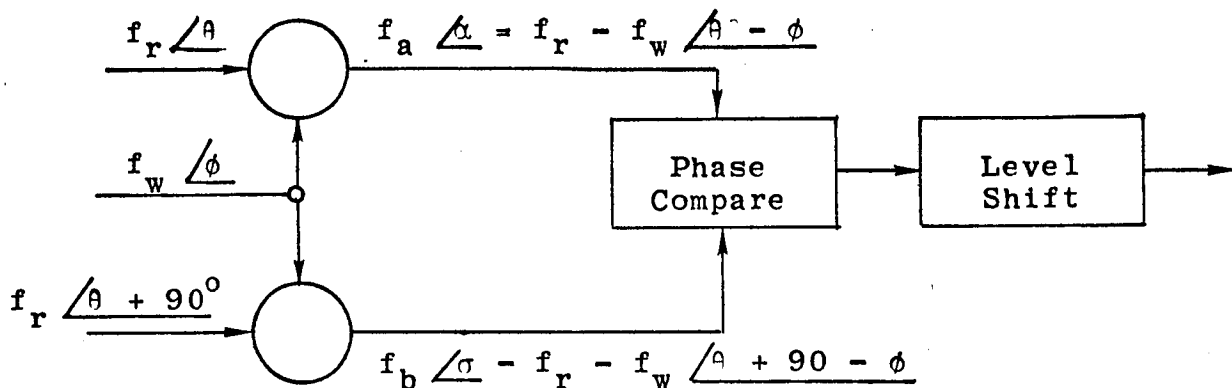
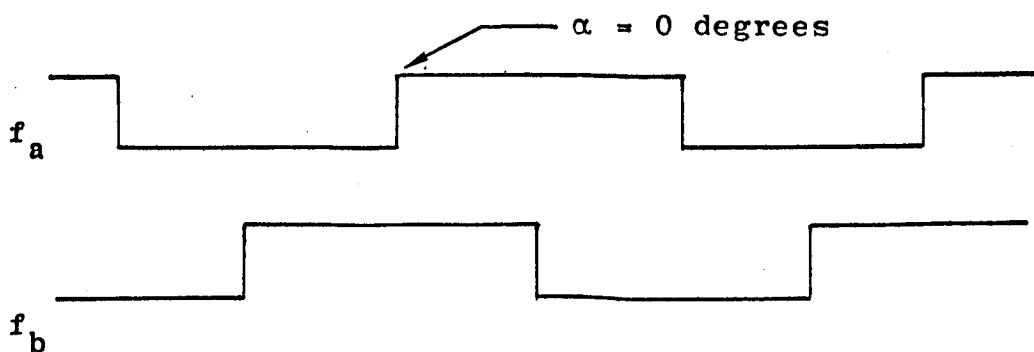


Figure 5-67. Frequency Comparison - Preset Discriminator phase compare circuit to go to a "1" level. The timing of f_a and f_b for $f_w < f_r$ is shown below:



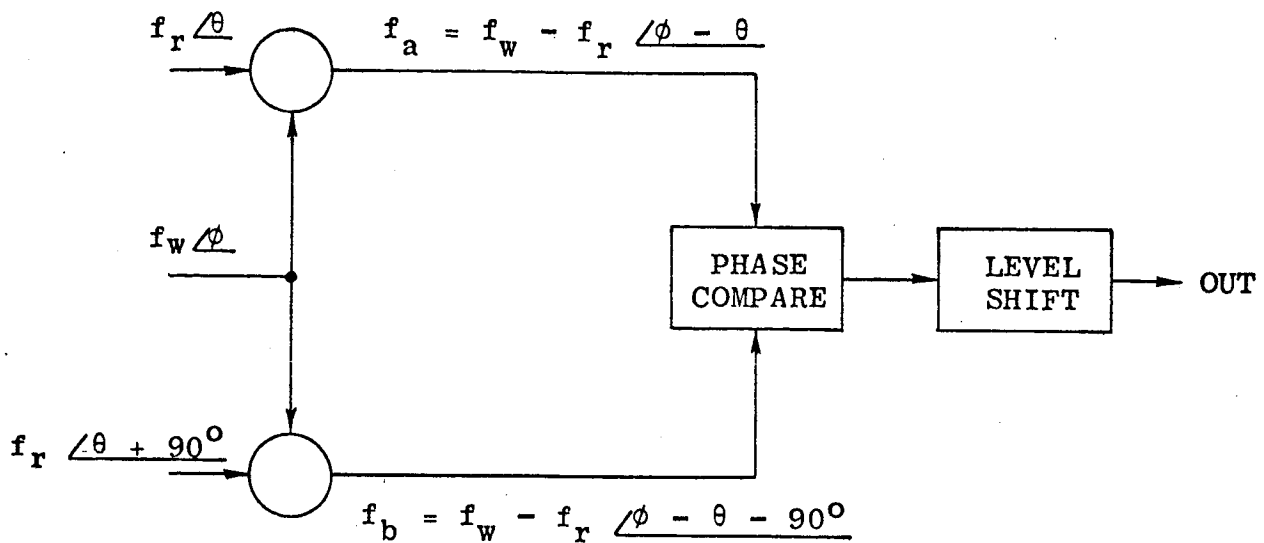
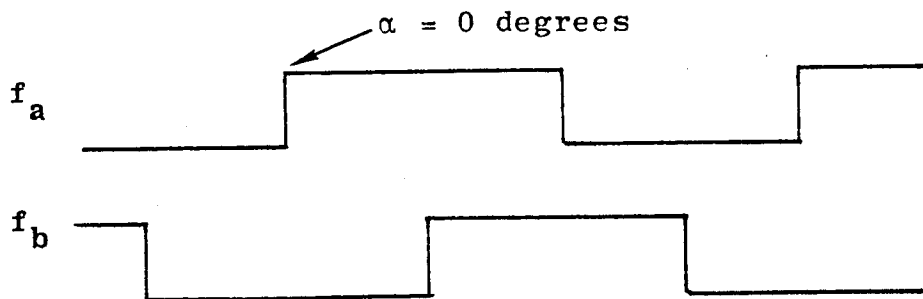


Figure 5-68. Frequency Comparison - Preset Discriminator

In Figure 5-68 where $f_w > f_r$ the mixer output frequencies, f_a and f_b , are again the same and are again different in phase by 90 degrees. The phase compare circuit will compare the phase of f_b when $\alpha = \phi - \theta = 0$ degrees but in this case f_b lags f_a by 90 degrees so the output of the phase compare circuit will be a "0" level. The timing of f_a and f_b for $f_w > f_r$ is shown below



The level shift circuit changes the logic "1" and "0" output levels of the phase compare circuit to a -3.3 vdc "1" level and a +3.3 vdc "0" level.

Implementation of a digital frequency comparator with an operation such as shown in Figure 5-67 requires a difference mixer capable of mixing two signals that the difference frequency varies from 0 to 1.2 MHz.

Using a shift register element as a mixer with one signal on the shift input and the other signal on the steering line, the maximum difference frequency is $1/2$ of the clock frequency, or, in this case, 1.6 MHz if the reference frequency of 3.2 MHz is used as the clock. The shift register element transfers whatever logic condition exists on steering line to the output whenever the clock makes a negative transition. Waveforms showing the mixing action of the shift register are shown in Figure 5-69 for the steering frequency less than the clock frequency. Figure 5-70 shows the waveforms for the steering frequency greater than the clock frequency.

An advantage of the carrier oscillator presetting method lies in its inherent stability and simple implementation. Virtually no DC circuit parameter variations are present because of the digital circuit mixing. Stability of the preset VCO is primarily determined by the reference frequency (which is the master oscillator) because of the high loop gain.

The digital logic diagram for the vehicle frequency preset is shown in the above reference schematic. All circuitry is packaged in one digital integrated circuit module. A 6.4 MHz input reference signal is first shaped by a hybrid amplifier circuit ST1. ST1 is used to drive FF1 and FF4 which are connected to a divide by 2 and a 90 degree phase shifter. The reference 3.2 MHz is obtained from FF4 and is used as the clock for the mixing register FF3. A 3.2 MHz signal at 90 degrees is obtained from FF1 and used as the clock on the other mixing register FF2. The unknown frequency is shaped in ST2 and is used as the steering for mixing registers FF2 and FF3. The output of FF2 and FF3 is used by register FF5 to provide the comparator output levels.

The output levels are inverted by gate G2 and drive the inverting amplifier Q1A. The output of Q1A operates between $+V_{cc}$ and a minus voltage set by reference diode VR1 and CR3. Signals from Q1A and Q1B are coupled to the output through an emitter follower for improved drive capability. In normal operation,

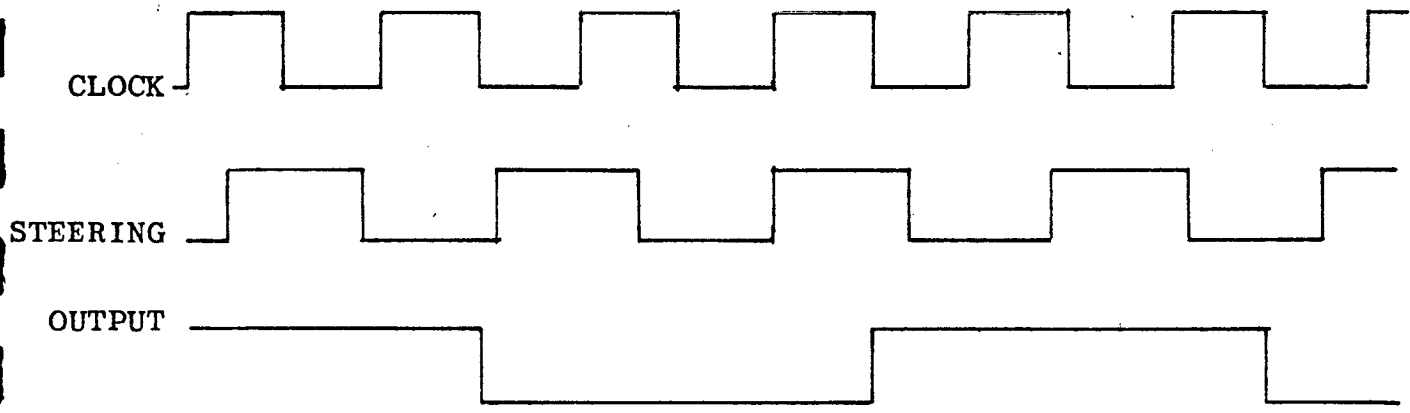


Figure 5-69. Shift Register Mixing Action

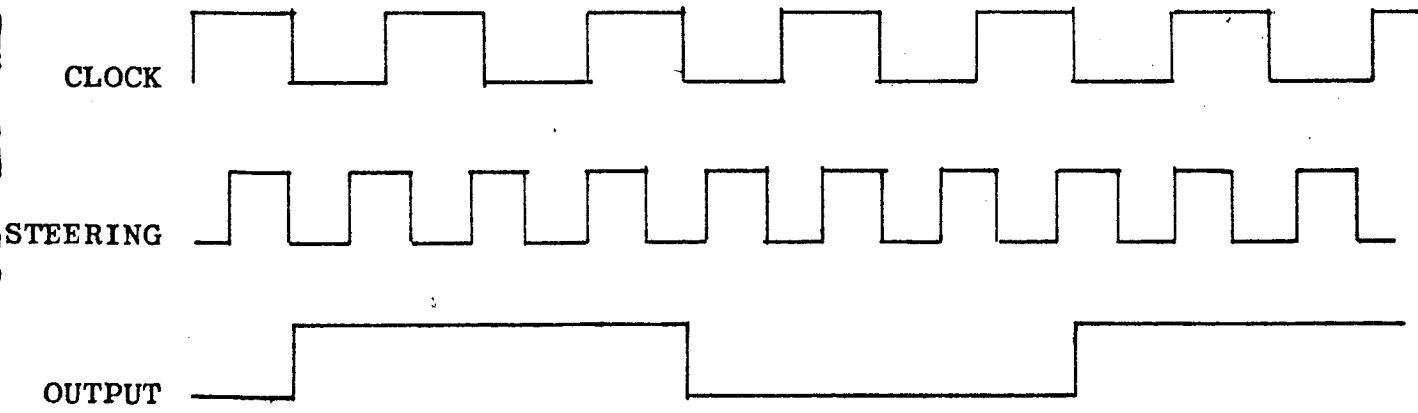


Figure 5-70. Preset Discriminator Waveforms

the output swings between +3.3 vdc and -3.3 vdc. The preset output is inhibited by a zero voltage level of the control input, $V-0 + V-1$. When $V-0 + V-1$ is a binary one, the signal is inverted by D1, has no effect on gate G2 and holds the output clamp transistor Q2 off. When $V-0 + V-1$ is a binary zero, D1 inhibits gate G2, and enables Q2 thus clamping the output to ground through the transistor, Q2.

+3.5 Volt Filter

The +3.5 volt filter is used on the MTL to suppress conducted electrical noise on the digital circuit power line. It is an LC, M-derived, four-pole, low pass configuration with a 3 db cutoff frequency at 3.5 KC. The filter is packaged in a digital half size module. An LC filter was chosen for this application to minimize power loss on the relatively high-current, low-voltage supply. The modules supplied by this filter are the divide by 141 and the frequency preset in the MTL frame.

H-Code Search

The H-code search module is a free running oscillator whose output is a sweep voltage balanced about ground. Figure 5-71 shows a typical output waveform when the circuit is loaded with 490 ohms.

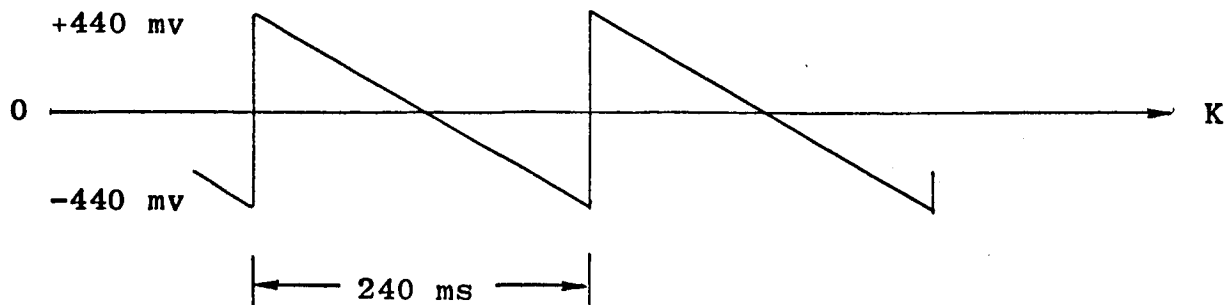


Figure 5-71. H-Code Search Sweep Waveform

The sweep voltage is injected in the modulation tracking loop as an induced error signal to sweep the receiver code for faster acquisition.

The circuit is a relaxation oscillator (RC charge type) and has a blocking oscillator sense-discharge circuit. During the ramp portion of the cycle, current flows through C1 and R2 and causes a voltage potential across R2 tending to turn on Q2. When Q2 is enabled, current flows in the transformer primary and inductive regeneration causes blocking oscillator action of Q1. Q1, in the on state, discharges the charge stored on C1, thus turning Q2 off and starting the cycle over. Zener diode CR1 and CR2 are selected to provide balance about ground. The peak-to-peak output voltage is scaled down by R6 and the 490 ohm external load. The circuit is packaged in a half size digital module utilizing welded cordwood construction.

Doppler Mixer

The function of the Doppler mixer module is to combine the Doppler multiplier output (48 MHz \pm 8 Doppler) with a reference frequency (44.8 MHz) from the frequency synthesizer to produce the required signal for Doppler extraction, 3.2 MHz \pm 8 Doppler (refer to Figure 5-72).

The mixing circuit is a basic diode mixer used throughout the vehicle modules. It is implemented with a differential amplifier and switching diodes. R6 sets the quiescent diode current and operating point. The reference input is buffered to obtain an additional reference signal for the receiver. Amplification and filtering are obtained with amplifiers A3 and A4. Unwanted mixing products are far removed from the desired output and simple RC filtering (C7 and the amplifier output impedance) is employed. R22 sets the reference power level for optimum mixing. LC filter sections are used for power line filtering and RC decoupling is employed at A3 to further reduce conducted interference. This module uses 21 ma at -9 vdc.

Doppler Multiplier

The function of the Doppler multiplier is to multiply the Doppler frequency contained on the 6 MHz VCO in the carrier tracking loop by a factor of eight in frequency. This is done

DOPPLER MIXER CHARACTERISTICS

S/N 1, 2, 3, 4

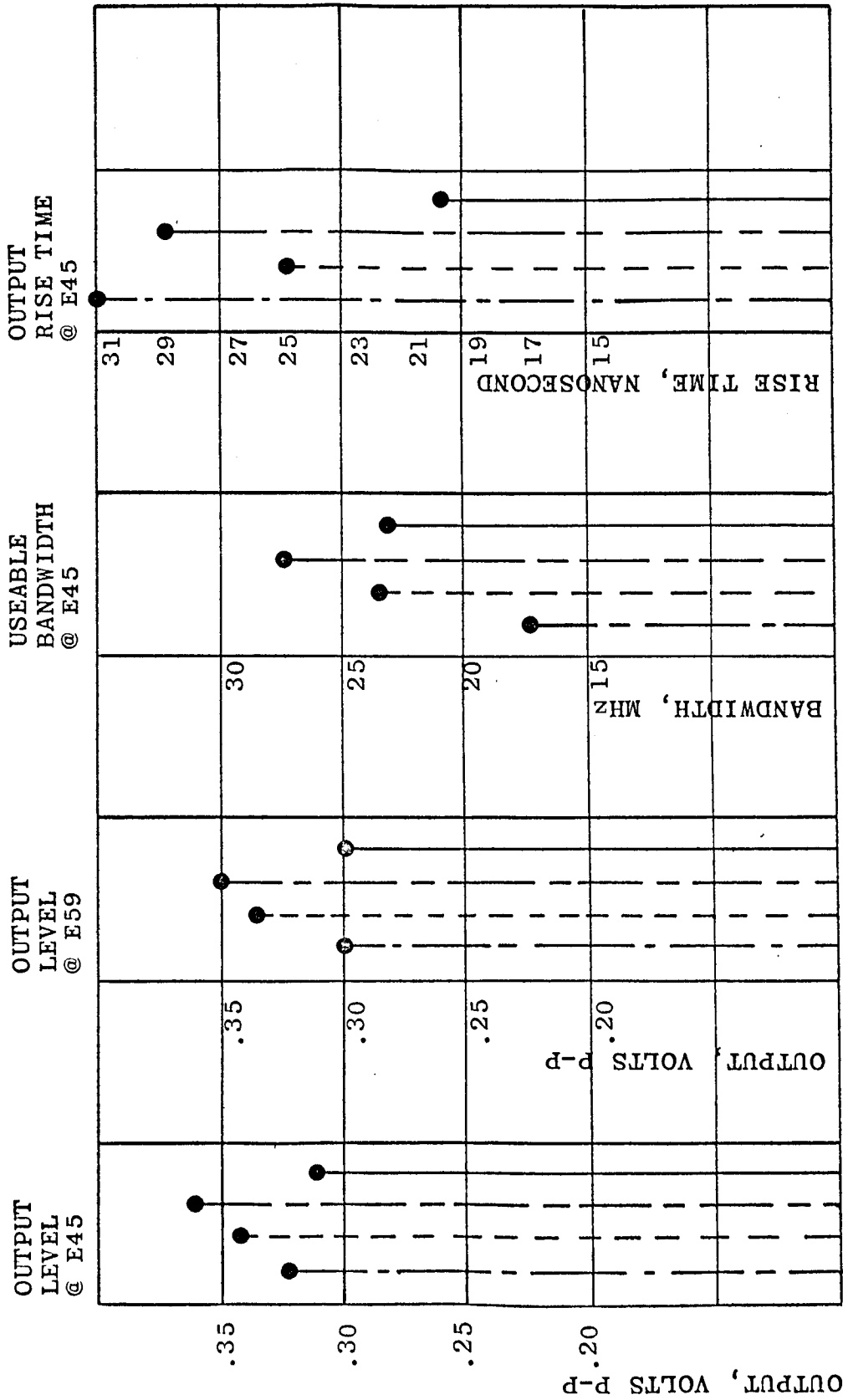


Figure 5-72. Doppler Mixer Test Data

to increase the resolution capability of the Doppler velocity extraction unit when the Doppler measurement is obtained. The multiplier contains three cascaded doubler circuits. Each doubler uses the mixer circuit common to vehicle modules consisting of a hybrid differential amplifier and switching diodes. Each doubler also has a single pole LC filter to discriminate against unwanted mixing products. The output signal is buffered by the amplifier A5 which operates in limiting and has a 50 ohm matching section (refer to Figure 5-73).

The 6 MHz \pm D input is buffered by a distribution amplifier which connects the signal to other modules on the MTL frame. These outputs do not have matching sections because they are used to drive digital circuits and have sufficient power to switch the pulse shaping circuits. This module uses 32 ma at -9 vdc.

DOPPLER MULTIPLIER CHARACTERISTICS

S/N 1,2,3,4

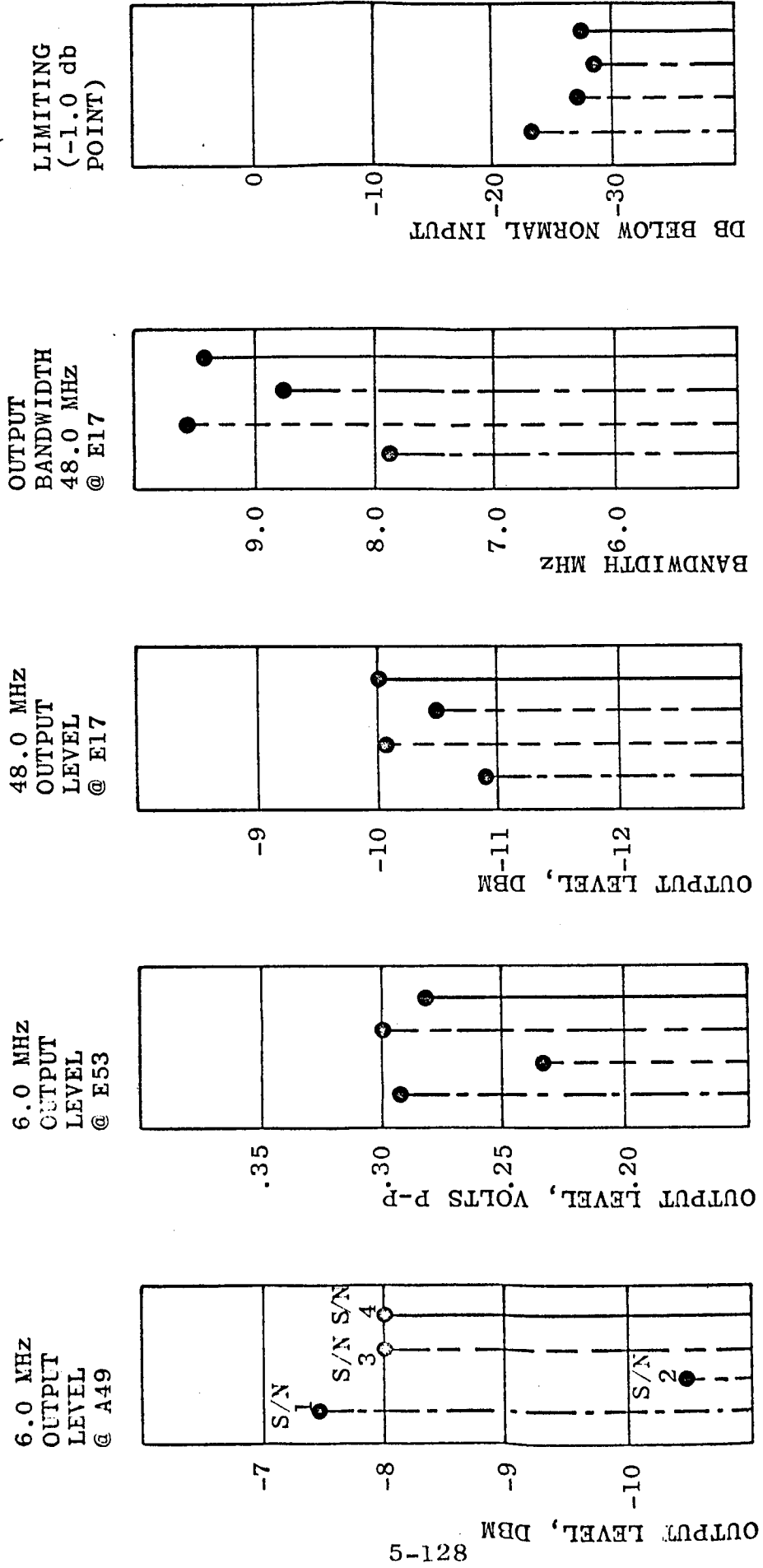


Figure 5-73. Doppler Multiplier Test Data

5.5.3 Vehicle Receiver Code Control

The Vehicle Receiver Code Control is part of the flight hardware of AROD. It generates the code used to demodulate the ranging code received from the ground station. It also supplies accurate timing and state signals to other subsystems.

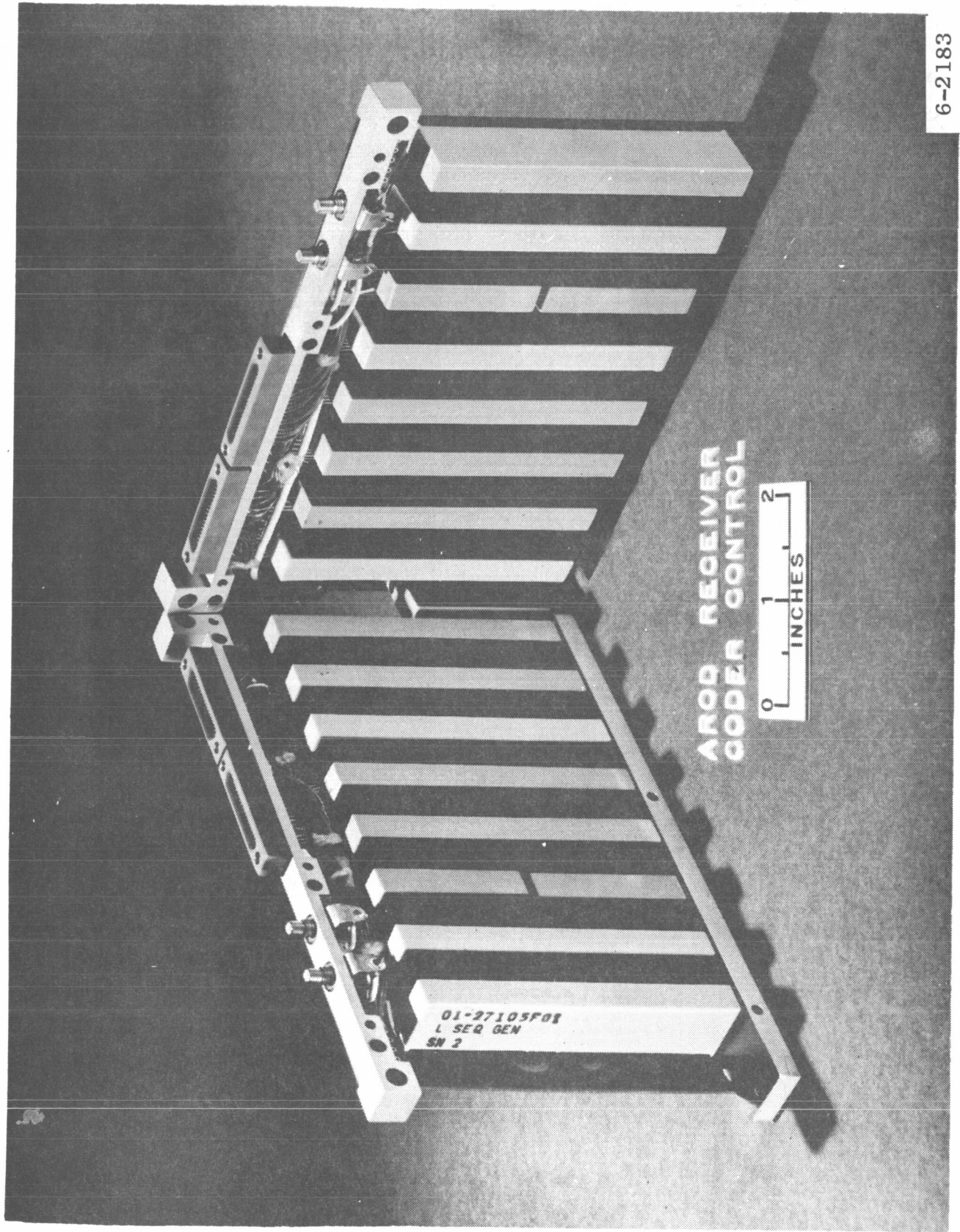
In order to achieve the high phase stability required for the code and timing signals, it was necessary to use a maximum clock frequency of 12.8 MHz. Special hybrid high speed flip-flop output circuits were used to minimize phase shift and insure fast rise and fall times for the code.

The fourteen digital modules and two filter modules making up this subsystem plus one module of the A_L , and A_H , and Data Demodulator subsystem are contained on two 4 x 6 inch printed circuit motherboards. The two motherboards mesh together to form a single logic frame (see Figure 5-74).

The Receiver Code Control weighs 0.96 pounds and the power consumption is approximately 1.0 amp at +3.5 vdc and 57 ma at -3.5 vdc (total of 3.7 watts).

5.5.3.1 Subsystem Requirements

The primary requirement for this subsystem is to generate the digital signals necessary to demodulate the received ranging code. These signals include a stable code for correlating with the received signal and various gate signals which are synchronized with the receiver code control. Both the code and the gating signals are required to have different forms depending on how the phase of the received code compares to the phase of the received code. In addition, this subsystem is to supply certain timing signals to other subsystems and highly accurate information concerning the phase of the received ranging code to the Range Extraction Subsystem.



6-2183

Figure 5-74. AROD Receiver Coder Control

The code generated by this subsystem, denoted by VR-Z, is to be a combination of two psuedo-noise sequences. The high speed component, called the H sequence, has a bit rate of 6.4 MHz and a period of 511. The low speed component, called the L sequence has a bit rate of 6.4/1022 MHz and a period of 127. The combination of these two sequences, which makes up the demodulating signal VR-Z, is dictated by the phase of the acquisition or tracking procedure at that time. For the vehicle receiver, this procedure has five unique steps denoted by V-0, V-1, V-2, V-3, and V-4. This program sequence is shown in Figure 5-75 while the forms of the code and gating signals are given in Table 5-2.

TABLE 5-2. AROD Vehicle Receiver Code and Gate Equations

VR-Z	$(V-0 + V-1 + V-2) (L \oplus F_L \bar{L}_{8K+2})$ $+ [V-3 + V-4 (L_{2N+1} + L_{8K+2})] [L \oplus F_L \bar{L}_{8K+2} \oplus H(F_L \oplus F_{L/2})]$ $+ V-4 L_{2N} \bar{L}_{8K+2} [L \oplus F_L F_{L/2} \oplus (H \oplus F_H) (F_L \oplus F_{L/2})]$
VR-GC1	$(V-0 + V-1 + V-2) \bar{F}_L + V-3 \bar{F}_L \bar{F}_{L/2} + V-4 \bar{F}_L F_{L/2} L_{2N+1}$
VR-GC2	$(V-0 + V-1 + V-2) F_L + V-3 F_L F_{L/2} + V-4 F_L \bar{F}_{L/2} L_{2N+1}$
VR-GH1	$V-3 \bar{F}_L F_{L/2} + V-4 \bar{F}_L F_{L/2} L_{2N+1}$
VR-GH2	$V-3 F_L \bar{F}_{L/2} + V-4 F_L \bar{F}_{L/2} L_{2N+1}$
VR-GI	$V-0 + V-1 + V-2 + V-3 + V-4 (F_L \oplus F_{L/2})$
VR-GR	$(V-0 + V-1 + V-2 + V-3) (F_L \oplus F_{L/2}) (H_{385} \rightarrow H_{151})$ $+ V-4 (F_L \oplus F_{L/2}) L_{2N}$
VR-D1	L_{16J+2}
VR-D2	L_{16J+10}

NOTES:

1. J = 0, 1, 2,, 7
2. K = 0, 1, 2,, 15

TABLE 5-2. AROD Vehicle Receiver Code and Gate Equations (cont)

NOTES (cont)

3. $N = 0, 1, 2, \dots, 63$
4. $H_{385} \rightarrow H_{151}$ is a "1" between the leading edge of H_{385} and the trailing edge of H_{151} and a "0" elsewhere.
5. F_L is a "1" between trailing edges of H_{256} and H_{511} and a "0" elsewhere.
6. $F_{L/2}$ is a square wave whose frequency is $(2f_h) \div (2044)$ and whose transitions occur at negative transitions of F_L .

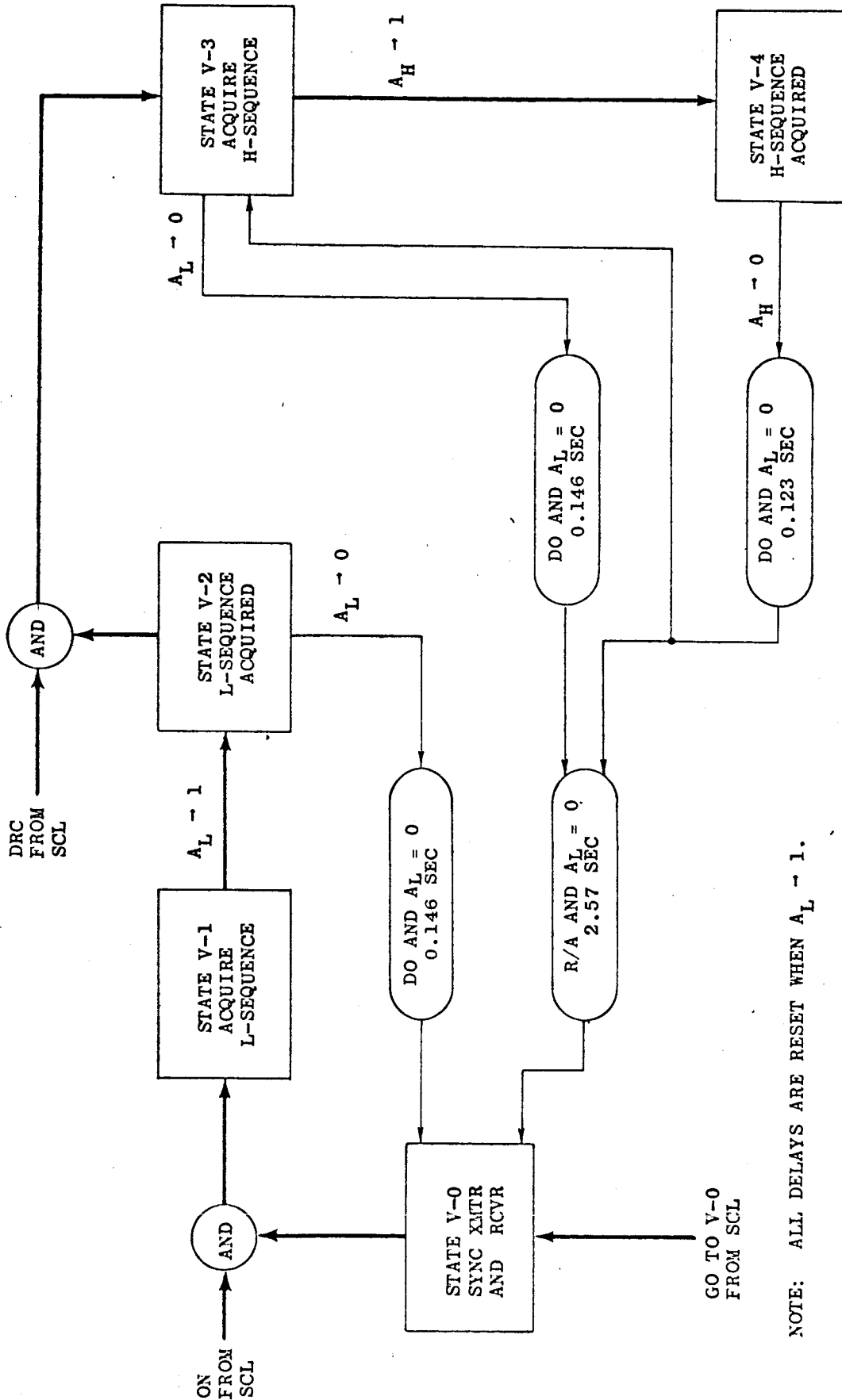
All timing signals are derived from the 12.8 MHz input frequency, whose analog form is denoted by $VR-2f_H$, and whose digital form is denoted by $VR-2F_H$.

All circuits used are of the standard digital family except the input signal shaper (A16) and the circuits (A56 and A33) used to retime the output code, VR-Z, and the 6.4 MHz square wave, F_{HS} .

5.5.3.2 Functional Logic Description

This subsystem is composed of 14 modules as listed below:

<u>Module</u>	<u>Logic Diagram</u>
Code Clock Generator	69-27140F
GR Gates	69-26252G
H Sequence Generator	69-27141F
L Sequence Generator	69-27142F
S-Band Data Encoder	69-27143F
Retimer	69-23364G
Buffer	69-23360G
Input Control	69-27120F
Program Counter and DO Timer	69-27116F
R/A Timer	69-27124F
Gate Generator	69-27136F
Code Combiner No. 1	69-27128F



NOTE: ALL DELAYS ARE RESET WHEN $A_L = 1$.

Figure 5-75. Vehicle Code Control States (Program Sequence)

<u>Module</u>	<u>Logic Diagram</u>
Code Combiner No. 2	69-27132F
Range Extraction Interface	69-26164G
2A-A1 Motherboard	69-26401G
2A-A2 Motherboard	69-26404G

In the discussions that follow, signals are called out without the prefix, VR, given on the logic diagrams.

Before discussing the logic design in detail, some definitions and conventions will be stated.

1. Buffer elements perform NOR logic so that an enable signal input to a buffer element is considered to enable the element when the signal is at the "zero" level.
2. H_{N-i} and L_{N-j} are the outputs of the i -th stage of the H sequence generator and the j -th stage of the L sequence generator, respectively.
3. The bits of the H and L sequences are defined by the following recursion formula and initial conditions.

$$a. \quad H_k = H_{k-9} \oplus H_{k-4} \quad k = 10, 11, 12, \dots, 511$$

$$H_1 = H_2 = H_3 = H_4 = H_5 = H_6 = H_7 = H_9 = 0$$

$$H_8 = 1$$

$$b. \quad L_m = L_{m-7} \oplus L_{m-6} \quad m = 8, 9, 10, \dots, 127$$

$$L_1 = L_2 = L_3 = L_4 = L_5 = L_7 = 0$$

$$L_6 = 1$$

Note that when H_k appears as the output of H_{N-9} , H_{k+1} through H_{k+8} are the outputs of H_{N-8} through H_{N-1} , respectively; and similarly, when L_m appears as the output of L_{N-7} , L_{m+1} through L_{m+6} are the outputs of L_{N-6} through L_{N-1} respectively. The notation, H_k and L_m , will be used interchangeably to denote the k -th or m -th bit of the H or L sequence, respectively, or to denote signals which are "one" when H_k or L_m appear as outputs of H_{N-9} or L_{N-7} and

"zero" at all other times. Thus, L_{127} might refer to the 127th bit of the L sequence, or to a signal which is a "one" only when L_{127} is the output of the last stage of the L sequence generator. This usage should cause no confusion since the context in which the notation is used will clearly indicate whether the bit or the signal is referred to.

Clock Signal Generation

All fundamental clock and timing signals are generated by using three modules consisting of the Code Clock Generator, the GR Gates, and the H Sequence Generator. The input signal $2f_H$ is shaped and buffered by an A16 shaper circuit and two buffer elements to form the signal $\overline{2F}_H$. This signal is further divided by two and buffered to form HCL Enable. $\overline{2F}_H$ is inverted by a buffer element to form $2F_H$ and is combined with HCL Enable to form the 6.4 MHz clock signal denoted by HCL. $\overline{2F}_H$ is also combined with LCL Enable to form the 6.4/1022 MHz clock signal denoted by LCL. By forming clock signals in this manner, the only timing variations (or clock skew) will be the differential propagation delay through different buffer elements. A 6.4 MHz square wave is reclocked by $2F_H$ to form the F_H signal. These signals are shown in the timing diagram, Figure 5-76.

The following list identifies the signals of interest on this drawing.

<u>Signal Number</u>	<u>Signal Name</u>
2	$\overline{2F}_H$
4	HCL ENABLE
5	HCL
6	$2F_H$
7	F_H
9	\overline{H}_{511}
10	LCL ENABLE

It should be remembered that only every other H_{511} pulse will generate an LCL Enable interval.

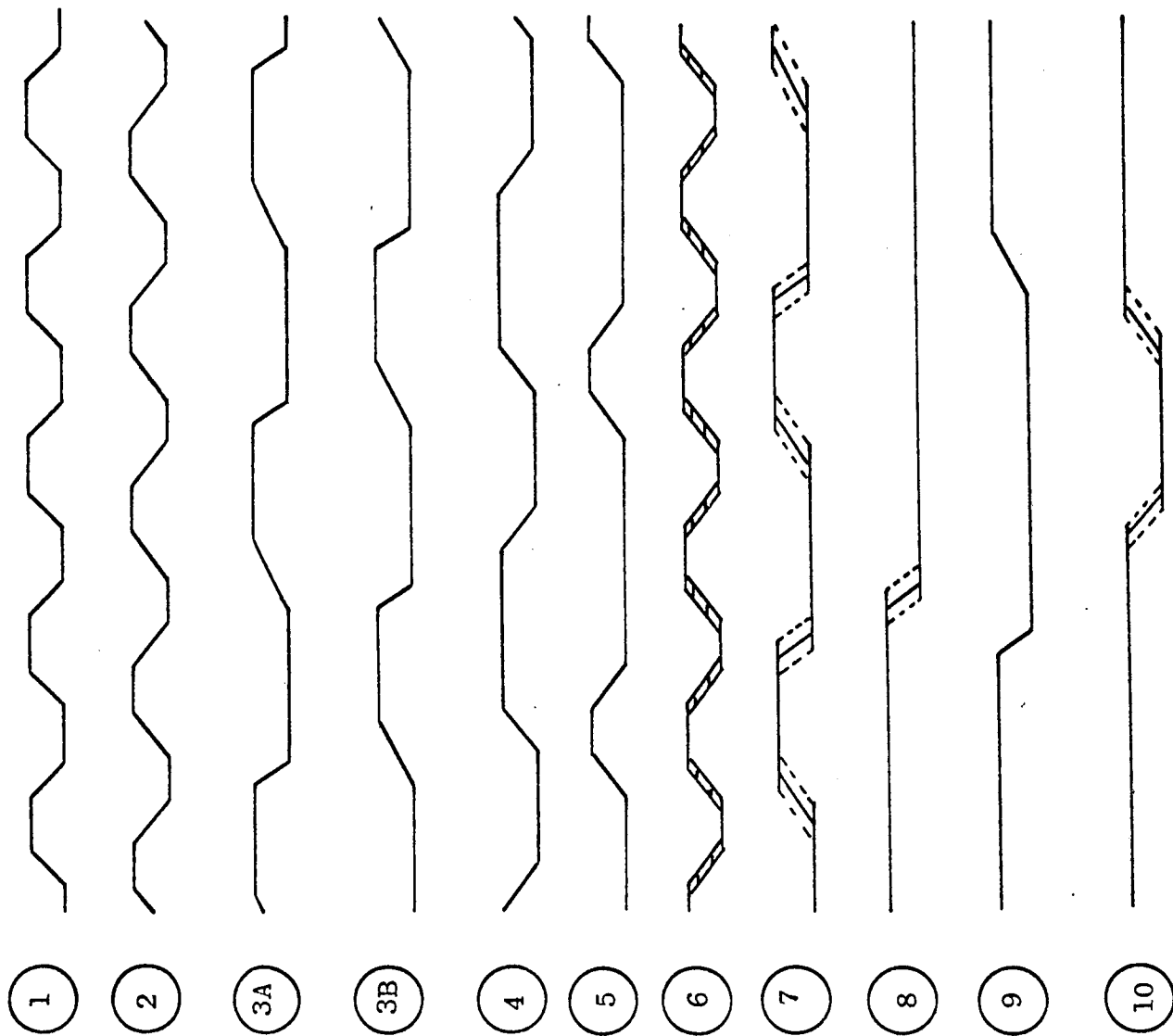


Figure 5-76. Code Clock Generator, Timing Diagram

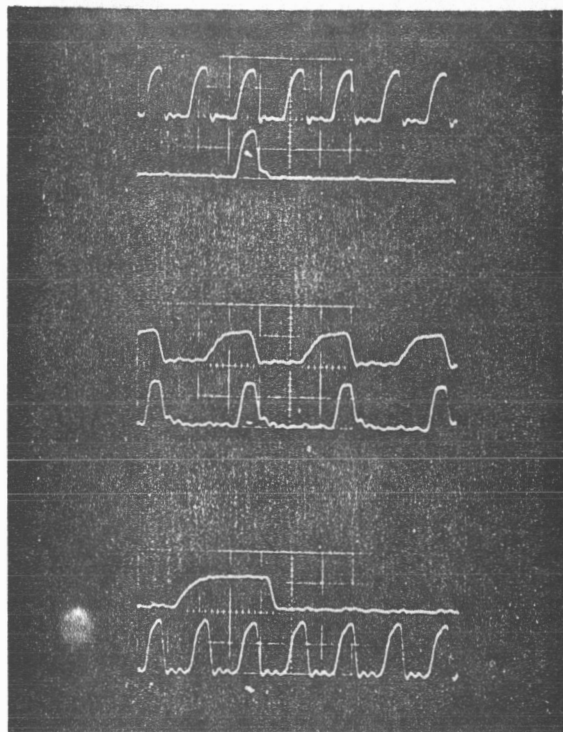
The H Sequence Generator module contains a standard linear shift register generator of nine stages and three word detectors. The three word detectors are connected so that one has a "one" output during code bit H_{255} , one has a "one" output during code bit H_{510} , and one has a "one" output any time the first eight stages contain "zero." This latter word detector is used to insure that the generator will not lock up in the "all-zero" condition. H_{510} and H_{255} are used by the code clock generator to generate F_L , $F_L/2$, $F_L \oplus F_L/2$, and LCL Enable as described below. This sequence generator includes provision for changing the phase of the sequence. This provision is the H Shift input. This signal line is normally held at a "zero" level, and when the signal is raised to a "one," a "zero" will be shifted into the second stage. If this signal is made a "one" for one cycle of HCL following H_{510} , the sequence generator will contain the following sequence:

H Shift	H_{N-1}	H_{N-2}	H_{N-3}	H_{N-4}	H_{N-5}	H_{N-6}	H_{N-7}	H_{N-8}	H_{N-9}	
0	0	0	0	0	0	0	0	0	1	H_{510}
1	1	0	0	0	0	0	0	0	0	H_{511}
0	0	0	0	0	0	0	0	0	0	H_0
0	1	0	0	0	0	0	0	0	0	H_{511}
0	0	1	0	0	0	0	0	0	0	H_1

It is seen that two additional states have been added to the sequence in that H_0 has been forced into the register and H_{511} has been repeated. Hence H_1 appears 2 bit times later and the sequence has been delayed by 2 bits. Since the sequence length is odd, any delay from 1 to 510 bits, inclusive, may be accomplished.

H_{510} and H_{255}^* are retimed by HCL in the code clock generator to become H_{511} and H_{256} respectively. The "one" to "zero" transition of F_L will coincide with the "one" to "zero" transition of H_{511} , and the "zero" to "one" transition of F_L will coincide with the "one" to "zero" transition of H_{256} . Transitions of $F_{L/2}$ will coincide with the "one" to "zero" transitions of H_{511} , while transitions of $F_L \oplus F_{L/2}$ will coincide with the "one" to "zero" transitions of H_{256} . Note that H_{256} , H_{511} , F_L , $F_{L/2}$, and $F_L \oplus F_{L/2}$ appear at the output terminals of register elements which are all clocked by the same HCL. H_{511} , $F_{L/2}$, and F_H are combined to form LCL Enable in a manner which will allow LCL to be coincident with the HCL pulse which caused $F_{L/2}$ to make a "one" to "zero" transition. Photographs of the actual timing pulses are shown in Figure 5-77.

* Note that these signals are defined to be a "one" when H_{510} and H_{255} , respectively, appear as outputs of stage H_{N-9} , and "zero" otherwise.

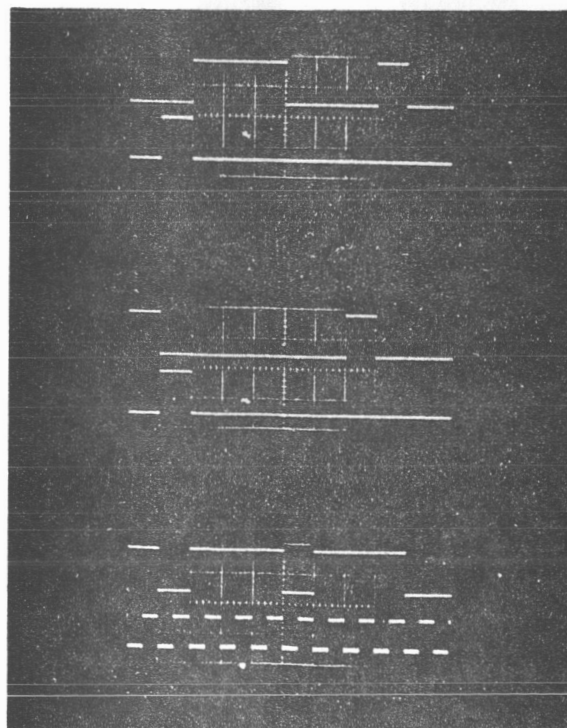


2 FH
ICL

FH
HCL

H₅₁₁
H_{N-9}
H₅₁₁
2 FH

50 nsec/cm

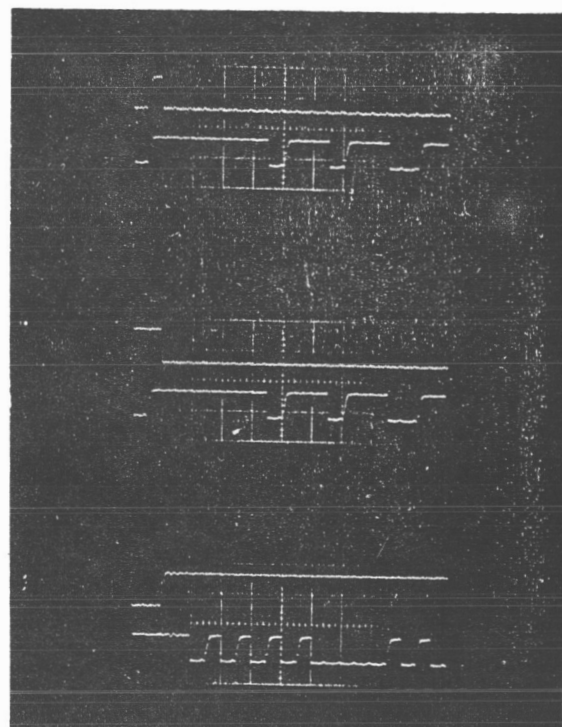


L_{N-9} F_L
L₅₉ H_{N-9}

L_{N-7}
L₁₂₇

L_{N-7}
F_{L/2}

one L Sequence bit/cm



two H sequence bits/cm

Figure 5-77. Timing Pulses

L Sequence Generator

The module consists of a 7 stage shift register generator with synchronous preset capability, three word detectors, and a retiming circuit. One word detector is to prevent lock up in the "all-zero" state and detects "zeroes" in the first six stages of the register. Another word detector is connected to detect "zeroes" in the first six stages and "one" in the last stage. This state of the generator occurs during bit time L_{126} . The signal from this detector is retimed and becomes the L_{127} signal, shown in Figure 5-77. The remaining word detector is set to detect "ones" in the first six stages and "zero" in the last stage which occurs at bit time L_{119} . When the L Search signal is "zero," this L_{119} signal will force the next state of the register to be L_{121} instead of L_{120} by causing a "zero" to be set in the first stage instead of a "one." Thus, the phase of the L sequence will change at a rate of one L sequence bit per L sequence period when the L Search signal is at a "zero" level. When this signal is at a "one" level, the L sequence phase shifting circuits are inhibited.

The synchronous preset capabilities are utilized when the EM + L SYNC signal goes to "one" or when both this signal and the L SYNC signal goes to "one." When both signals are held at a "one" level, the 7 bit word 1000000 is continuously set into the first through the seventh stages by LCL until

both signals go to a "zero" level. This condition sets the L Sequence Generator, such that the first full L sequence bit after the EM + L SYNC and L SYNC signals go to a "zero," is 0100000 which is the L_1 bit time. In a similar manner, making only the EM + L SYNC signal a "one" will cause the state 1010110 to be set into the register. The first full L sequence bit after the EM + L SYNC signal goes to "zero" will then be 1101011 which is the L_{75} bit time.

S-Band Data Encoder

This module contains an L Sequence Generator word detector for detecting L_{58} , three retiming circuits, and a four stage presettable counter with logic for generating the bit sequence L_{16N+1} , L_{16N+9} , and L_{8k+1} (for $N = 0, 1, \dots, 7$ and $k = 0, 1, \dots, 15$) and the bit stream, D^v .

The word detector is connected to the L Sequence Generator module to detect the bit pattern 0011100 which occurs during bit time L_{58} . This detector output is retimed by LCL to yield the signal called L_{59} .

The four stage counter is preset by L_{127} and synchronously divides the LCL rate by 16 so that the L Sequence period is divided into 7 intervals of 16 L sequence bit times each and one interval of 15 L sequence bit times.

The three word detectors attached to the counter form the three required bit sequences. The bit sequence

L_{8k+1} is retimed by LCL to form the bit sequence L_{8k+2} . The bit sequence L_{16N+1} and L_{16N+9} are combined with the data input signal according to the following equation to form the steering signal, S-D';

$$S-D' = (DATA)(L_{16N+1}) + (\overline{DATA})(L_{16N+9}).$$

This signal is then retimed by LCL to form the D' signal.

GR Gates

In addition to buffering three timing signals, this module is required to form the interval between H_{385} and H_{151} for use in deriving the GR Gating signal. The bit pattern 0110__0000 in stages H_{N-1} through H_{N-9} , respectively, is detected and retimed to become the pattern 00110__000. This is the pattern at bit times H_{151} or H_{384} depending on the output of H_{N-6} . This pattern is then combined with H_{N-6} so that the output flip-flop is set to "one" if H_{N-6} is "zero" and is set to "zero" if H_{N-6} is "one." The flip-flop is clocked by HCL so that its output, P-GR, will become a "one" at the leading edge of H_{385} and a "zero" at the trailing edge of H_{151} .

Retimer

The function of this module is to retime various timing signals, to form the GI and GR gating signals, and to combine the H sequence with the 6.4 MHz square wave (F_H).

The steering signals for F_L and $F_L/2$ from the code

clock generator are retimed by HCL to supply sufficient fanout for these signals. L_{16N+1} , L_{16N+9} , L_{N-6} and L_{126} are retimed with LCL to become L_{16N+2} , L_{16N+10} , L_{N-7} , B, and L_{127} , A, respectively. In addition, L_{127} and LCL are used to reset and toggle a flip-flop whose output is L_{2N} . This signal is a "one" during the even numbered L sequence bits and "zero" elsewhere.

The steering signal for $F_L \oplus F_{L/2}$ is retimed by HCL and then combined with functions of the program states V-0, V-1, V-2, V-3 and V-4 to form the steering for the G_I gate signal. $F_L \oplus F_{L/2}$, the program states, and signal P-GR are combined to form the steering for the G_I gate signal.

Buffer Module

The function of this module is to buffer program state signals and timing signals used by the System Control Logic, Data Readout, and Vehicle Tracking Receiver subsystems. In addition, the L Sync, L Search, and R/A-D signals are formed in this module. The L Sync signal is formed as the logical "and" function of program state V-0 and the Vehicle Transmitter L_{127} pulse, while L Search signal is the logical "or" function of program states V-0, V-2, V-3, V-4 and the L Sequence correlation level A_{LI} . A_{LI} will be "zero" until the received L sequence bits match the receiver L sequence bits.

The R/A-D signal is taken as the true output of a flip-flop which is set to "one" by a signal dropout in states V-3 or V-4 (this signal is denoted logically by the signal, V-3/DO + V-4/DO) and which is set to "zero" when A_L becomes a "one" or when the R/A timer runs down.

Input Control

The function of this module is to generate timing signals synchronous with the subsystem clock from the following input signals:

- (a) A_H
- (b) A_L
- (c) ON
- (d) DRC
- (e) Go To V-0

Each input circuit consists of a two stage shift register and appropriate gates to detect transitions of these input signals. All registers shift at LCL time except the first stage of the A_L input circuit which is shifted at "zero" to "one" transitions of $F_L/2$. Thus, all derived timing signals will be one L sequence bit wide except the pulses at transitions of A_L which will be one half of an L sequence bit width.

A_H transition pulses will occur only during L_{120} time while A_{HI} will make transitions only at the leading edge of

L₁₂₀. Note that A_H transition pulses are inhibited in any state but V-3 while A_{HI} is inhibited in program state V-0.

A_L transition pulses will occur only during the last half of L₁₁₉ time, while A_{LI} will make transitions only at "zero" to "one" transitions of F_L/2 during L₁₁₉ bit time. Note that A_{LI} and A_L→0 are inhibited in state V-0, A_L→1 clock pulse is inhibited in every state but V-1, and A_L→1 reset pulse is never inhibited. The ON timing pulse can occur during any L sequence bit time but only in state V-0. The DRC timing pulse can also occur at any L sequence bit time but only in state V-2. The Go To V-0 timing pulse can occur at any L sequence bit time in any state. The Go To V-3 control signal will be "zero" except during the first complete L sequence bit period after the input DRC signal goes to "one" when the subsystem is in state V-2. The Go To V-0 control signal will be "zero" except during the first complete L sequence bit period after the input Go To V-0 signal goes to "one." The Return to V-0 signal is the logical "or" function of the Go To V-0 control signal, the V-2/DO signal (which is the occurrence of signal dropout in state V-2), and the R/A signal (see Section 3.9). The CCCL signal is the logical "or" function of the R/A signal, the ON timing signal (Go To V-1 control signal), the A_L→1 clock pulse, the A_H→1 clock pulse, the Go To V-3 control signal, the Go To V-0 control signal, and the V-2 and V-4 dropout signals. These signals occur when the subsystem is to change status.

Program Counter and DO Timer

This module consists of a five stage shift register (the program counter) driven by a timing signal which is the logic "and" function of $F_L \oplus F_{L/2}$ and CCCL description (refer to INPUT CONTROL above) and a three stage synchronous counter.

The five stage program counter is arranged so that normally, each stage corresponds to a program state and only one flip-flop will be set to a "one" at any particular time. No circuit is included to prevent more than one stage being set to a "one," however, since the initial step in code acquisition will be a command to Go To V-0. This signal is part of the Return to V-0 signal which sets the first stage to a "one" and the remaining stages to "zero" regardless of their previous state. This "one" is then shifted to stage 2 on receipt of the ON signal and to stage 3 when A_L becomes a "one." On receipt of the DRC signal the "one" is shifted to stage 4 and to stage 5 when A_H becomes a "one." If the program is in state V-4 (the "one" is in the fifth stage), and a signal dropout is recorded; the signal V-4/DO will go to a "one" and the fifth stage is set to "zero" while the fourth stage is set to "one" and the first, second, and third stages remain set to "zero." Thus a V-4/DO signal causes the subsystem to change from state V-4 to state V-3. The three stage counter is normally locked in the all "zero" stage. A "one" is inserted in the first stage when A_L goes

to a "zero" level. The counter will then progress through the rest of its states until it contains all "zeroes" again or until A_L goes back to "one" which sets all counter stages to "zero." The counter is clocked by L_{127} and A_L can make transitions only at L_{119} . The first L_{127} pulse after the counter has returned to all "zero" is denoted as DO. Note that the DO signal is inhibited by A_{LI} and that the DO pulse will be generated by the seventh L_{127} pulse after A_L became "zero." Thus the DO timer (dropout time delay) has a period of 0.123 seconds.

R/A Timer

The function of this module is to provide an additional delay (called the reacquisition time) after the generation of the DO signal if the subsystem is in state V-3 or state V-4. A seven stage synchronous counter clocked at L_{127} rate is employed for this purpose. Normally this counter is locked in the all "zero" condition. When either signal V-3/DO or V-4/DO is generated, a one is inserted in the first stage and the counter will cycle through all its states until either A_L becomes a "one" or until the counter contains all "zeroes" again. In case A_L becomes a "one" before the counter runs down, the counter will be reset to contain all "zeroes." The first L_{127} pulse which occurs after the counter reaches the "all-zero" condition is gated out to become the R/A

signal. This signal is inhibited by A_{LI} . The R/A signal is, then, a "one" for the duration of L_{127} ; and becomes a "one" 2.57 seconds after a V-3/D0 or a V-4/D0 pulse unless A_L is a "one."

Gate Generator

Gating signals D1, D2, GC1, GC2, GH1 and GH2 are formed in this module. Each of these signals is a logical function of some of the program state signals and timing signals F_L , $F_{L/2}$, L_{2N} , L_{16N+2} , and L_{16N+10} . These functions are given in Table 1.

Each signal is retimed by HCL, which introduces a 160 nanosecond delay from the basic sequence reference, and buffered by a gate. The actual gate signal outputs supplied to the receiver are the logical inverses of those listed except for D1, D2, GH1 and GH2.

In addition to these gating signals, two signals, which are the inverses of GC1 and GC2 inhibited by R/A-D, are also made available as outputs.

Code Combiner

The two basic sequences are combined with program states and timing signals to form the code given in Table 5-2 as VR-Z. The combining is accomplished within the two modules called Code Combiner No. 1 and Code Combiner No. 2. In addition to forming the final code, the number two code combiner retimes

and buffers the GR and GI gating signals so that the same delay is introduced (160 nanoseconds) and so that the logical inverses of these signals are supplied to the receiver.

The initial combining of the code components is accomplished in module number one. Signals which contain F_H as a component must be retimed by $2F_H$ to preserve the waveform, and so no more than one level of logic may be performed before these signals are retimed. In addition, these signals must be retimed exactly twice for every time the remaining components are retimed by HCL in order to line up properly when the final logic is performed. As a result, the entire combined code appears at the steering inputs to the interface circuit delayed by five cycles of the $2F_H$ signal from the basic sequence reference. A further delay, called the interface retiming delay is introduced in the output circuit.

Range Extraction Interface

This module supplies the receiver timing signals required by the range extraction subsystem. In addition, various signals are buffered for use by other modules of this subsystem as well as by other subsystems.

L_{127} is delayed by 4 cycles of $2F_H$, buffered, and supplied to the range extraction subsystem together with $2F_H$. F_H is retimed by a high speed flip-flop and also buffered

by a gate. Both outputs, F_H and F_{HS} , are made available to the range extraction subsystem. Thus, the same interface retiming delay as introduced in the code is introduced in the F_{HS} signal path.

5.5.3.3 Test Results

For purposes of this discussion, the following nomenclature will be used:

Subsystem #	S/N	
	Board #1	Board #2
1	2	1
2	4	3
3	3	2
4	1	4

Looking at the data sheets, it will be seen that subsystem 1 was tested at $+80^{\circ}\text{C}$ rather than $+85^{\circ}\text{C}$. The subsystem will operate at $+85^{\circ}\text{C}$ providing the $+V_{CC}$ voltage does not exceed 3.5v. It was decided to use this subsystem

"as is" rather than try to repair it as $+80^{\circ}\text{C}$ is still higher than the required operating temperature for the airborne equipment. Also, if the $+V_{\text{CC}}$ varied from nominal of $+3.5\text{v}$, it will probably vary downward, thereby extending the operating temperature range.

Apparently the $+V_{\text{CC}}$ was low for the first part of the $+25^{\circ}\text{C}$ test on subsystem 3. Indications of this can be seen in the $+V_{\text{CC}}$ current, VR-A_L and VR-A_H time delays, and the VR-DATA time delay. The logic "one" levels of the Z codes taken near the end of the test, however, indicates that the $+V_{\text{CC}}$ was back near nominal at this time. Because these subsystems are normally more sensitive to temperature variations than voltage variations, the data taken during the first part of the test with low $+V_{\text{CC}}$ is considered good as the subsystem operated correctly over the full temperature range.

Because of a large amount of jitter on the scope trace, the time relationship between VR-L₁₂₇ and VR-2F_H could only be measured with an accuracy of ± 5 nanoseconds. This accounts for the large variation of this parameter within each subsystem over temperature. The variation from one subsystem to another was not analyzed as the only requirement on this signal is that VR-L₁₂₇ makes its negative transition while VR-2F_H is at a logic "one" level. This condition is met in every case.

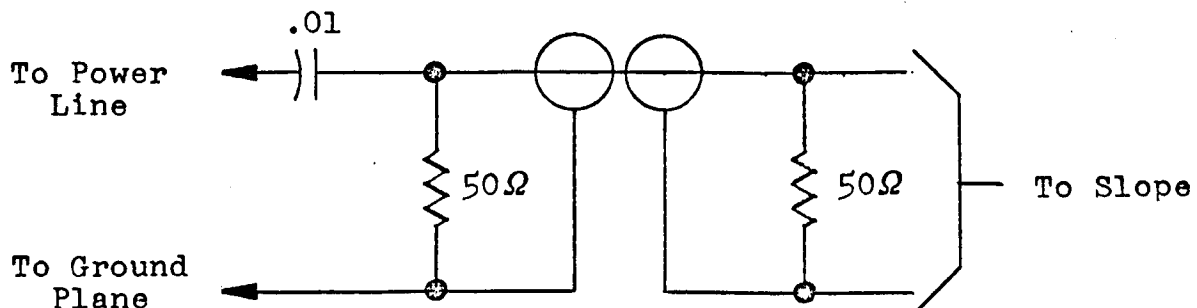
The large variation in noise level on both the Z-code signals and the power line was to be expected because as each

subsystem was tested, a different ground system was plugged together connecting the subsystem, power supplies and tester.

After discussion with the engineers responsible for the subsystems utilizing the VR-Z, VR- \bar{Z} , and VR-F_{HS} signals, it was decided that the original noise specification of 50 mv was unnecessarily tight and that the noise level could be well in excess of 100 mv. Since the maximum noise level measured was 114 mv, no further investigation was made.

A note on the data sheets can be seen indicating that the VR-F_{HS} signal is jumpered such that the actual output signal is VR- \bar{F} . The motherboard is laid out so that this signal can be changed simply by moving one wire and changing a jumper.

The power line noise inside filter measurement was made with the following circuit.



Due to the pulse nature of much of the noise, the rms value is considerably lower than the peak-to-peak value given.

It is suspected that the accuracy of these measurements is not much better than $\pm 20\%$ because that much variation could be seen by making the measurement at different points

on the motherboard.

On future units it is suggested that the Philco I/C's used for 12.8 MHz signals be replaced with I/C's having less propagation time. This will result in a subsystem less sensitive to variations in temperature and voltage. This could also eliminate the necessity to select special I/C's for the Code Clock Generator.

5.6 FREQUENCY SYNTHESIZER

This document is the final engineering report on the AROD Vehicle Frequency Synthesizer. The Frequency Synthesizer, operating from a single master oscillator, generates all the required frequencies for the remaining vehicle subsystems. Frequency coherence is maintained between all the output signals.

The frequencies generated and their function are listed in Table 5-3A.

Table 5-3A. Frequency Synthesizer Output Signals

Frequency Synthesizer Output Signals	
Frequency	Subsystem Reference
100 KHz	Timing Unit
300 KHz	Control Data Modulator
6.4 MHz	Tracking Receiver Frequency Preset
7.2 MHz	Tracking Receiver Channel A Phase Detector
7.6 MHz	Tracking Receiver Channel B Phase Detector
8.0 MHz	Tracking Receiver Channel C Phase Detector
8.4 MHz	Tracking Receiver Channel D Phase Detector
12.8 MHz	Transmitter Code Control Unit
44.8 MHz	Tracking Receiver Bias
34.5 MHz	Station Control Transmitter Carrier
217.7 MHz	Tracking Receiver Local Oscillator
276.75 MHz	Tracking Transmitter Carrier

Frequency versatility for the AROD system is derived in the synthesizer. The added flexibility permits system operation throughout the

following frequency ranges:

- a) Vehicle Station Control Transmitter - 135 to 150 MHz in steps of 25 KHz
- b) Vehicle Tracking Transmitter - 2200 to 2450 MHz in steps of 400 KHz
- c) Vehicle Tracking Receiver - 1692 to 1790.8 MHz in steps of 400 KHz.

Operation at these frequencies requires the synthesizer to deliver the following signals, any one of which can be varied independently with respect to the other two still maintaining frequency coherence:

- a) Station Control Transmitter Carrier Reference - 33.75 to 37.5 MHz in steps of 6.25 KHz
- b) Tracking Transmitter Carrier Reference - 275 to 306.25 MHz in steps of 50 KHz
- c) Tracking Receiver Local Oscillator Reference - 211.5 to 223.85 MHz in steps of 50 KHz

The synthesizer is packaged in three frame assemblies located in Case 1 of the Vehicle borne package. Figure 5-13 is a photograph of the completed assembly. The circuitry is packaged in 18 cordwood modules, 6 digital I/C modules, and 6 power supply filter modules. In addition, the master oscillator and 217.7 MHz X2 multiplier and helical resonator are mounted on the printed circuit motherboards.

The physical characteristics of the synthesizer are summarized as follows:

Size: 2.7" x 4" x 6.2"

Weight: 1444 grams

Power: 5.13 watts

The detailed physical breakdown is included in Section 4.0.

5.6.1 Technical Approach

Figure 5-78 is a block diagram of the Frequency Synthesizer which also includes an indication of the circuitry within the enclosed blocks. The enclosed blocks represent the packaging breakdown into modules. The A-43, 44, and 16 symbols represent hybrid integrated circuit differential amplifiers developed expressly for use on the AROD program. The MC1530 is a monolithic integrated circuit operational amplifier.

There are four basic types of circuit functions utilized:

- 1) Frequency doubler
- 2) Frequency converter
- 3) Odd order frequency multiplier
- 4) Phase-locked loop

These are described in detail in Section 5.5.2. All of the signals are derived from a 3.2 MHz temperature compensated master oscillator. This was a subcontracted item purchased from Bendix Corporation. All of the fixed frequency signals are generated by doubling, odd order multiplying or by up-conversion. The variable output frequencies are generated in the three phase locked loops. Integrated circuits were utilized throughout the design employing microminiature packaging techniques. These items are discussed in greater detail in the following sections.

5.6.1.1 Hybrid Integrated Circuits

The synthesizer was designed so that the individual circuit requirements were not extremely critical. The passive LC filter bandwidths were 10% or more of the center frequency. The active element requirements were for low gain (20 db) amplifiers operating in a limited mode that could provide two buffered outputs with a good degree of isolation.

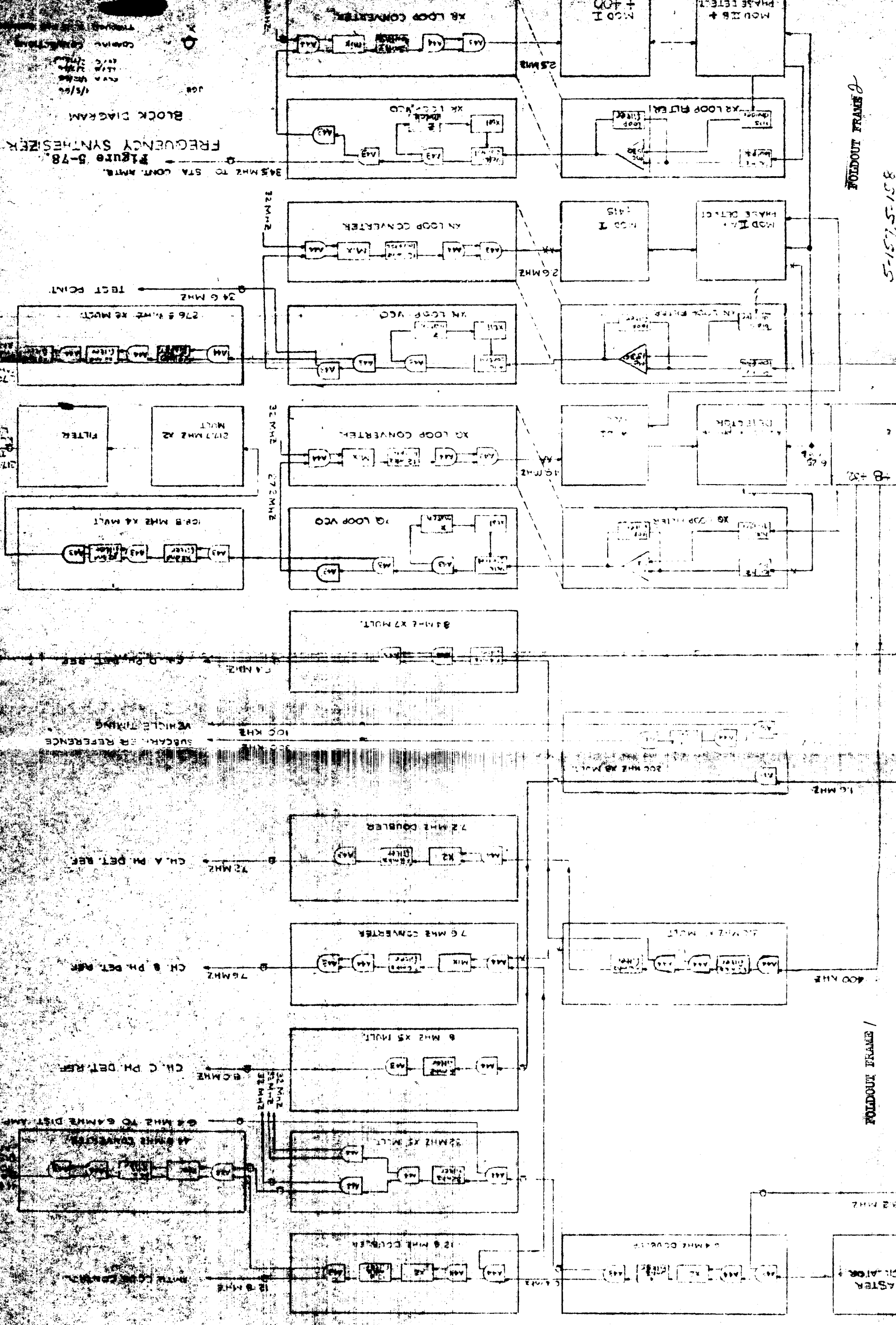


Figure 5-78. FREQUENCY SYNTHESIZER BLOCK DIAGRAM

34.5 MHz TO STA CONT. ANTENNA
 1/5/56
 DATA FROM
 1/10/56
 COPIED FROM
 ORIGINAL

FOLDOUT FRAME 8

5-157.5-15.8

FOLDOUT FRAME 1

FOLDOUT FRAME 9

A hybrid integrated circuit differential amplifier was developed for use as the standard building block throughout the AROD system. This versatile circuit was utilized as a mixer, odd order multiplier, distribution amplifier and buffer within the synthesizer. This approach had the advantages of conserving circuit design time through standardization, as well as making possible a considerable savings in size of the final equipment.

A total of 53 of these hybrid circuits are used in the Frequency Synthesizer. The circuit is basically a differential amplifier with grounded base outputs. This configuration provides a high input impedance and good isolation of the output signals. Available in three difference power levels, the circuit conserves DC power where higher level outputs are not required. The unit is useful over a frequency range of 1 KHz to 300 MHz.

5.6.1.2 Temperature Compensated Master Oscillator

The AROD Vehicle borne equipment operates from a single master oscillator to maintain frequency coherence between the subsystems. This oscillator must have an adequate short and long term stability as given in Table 5-3, in order not to impair system performance.

Also, the oscillator must consume as little as possible of the limited vehicle supply power. A typical oven controlled oscillator consumes 10 to 15 watts at turn-on, and 3 to 5 watts after initial warm-up.

A temperature compensated oscillator uses thermistors and resistors in the feedback path to control the frequency over a given temperature range. Little added power is consumed within the thermistor-resistor network compared to the oven control. With a voltage regulator, temperature compensation network and oscillator, the total unit consumes only 168 milliwatts. Table 5-3B is a summary of the oscillator test specification.

Table 5-3B. Temperature Compensated Master Oscillator Specification Summary

Temperature Compensated Master Oscillator Specification Summary	
Stability:	±1 part in 10^9 /day long term ±1 part in 10^7 for all combinations of temperature, supply voltage, and loading ±5 parts in 10^{10} /50 ms short term
Operating Temperature Range:	0° to +60°C
Size:	5.6 cubic inches
Weight:	6 ounces
Power:	-28 vdc @ 6 ma = 168 mw
Warm-up:	Time to reach operating frequency is less than 1 second.

5.6.1.3 Frequency Synthesis Using Phase Locked Loops

Frequency versatility is attained by using phase locked loops for the three variable outputs. The advantages of this approach are that spurious responses associated with most multiply and add techniques are reduced due to the narrow loop bandwidth, while frequency coherence is maintained by locking the loops to the master oscillator. All non-integral harmonics must be greater than 100 db below the desired output. Also, the frequency may be varied in the required steps by merely replacing the VCO module and altering the DC inputs to the digital programmable pulse frequency divider. The selected frequency increments of 6.25 KHz for each loop permit the use of identical types of modules for each of the loops.

The basic frequency for accomplishing the synthesis is in the 26 to 38 MHz frequency range for the ease of establishing long time coherence crystal controlled oscillators. The loop parameters are set to lock automatically to the reference signals by setting the loop bandwidth greater than the sum of the uncertainties. This requires that the loop noise bandwidth be

greater than 5 Hz referred to the detector frequency.

Figure 5-79 is a block diagram of the synthesis technique, utilizing a phase locked loop.

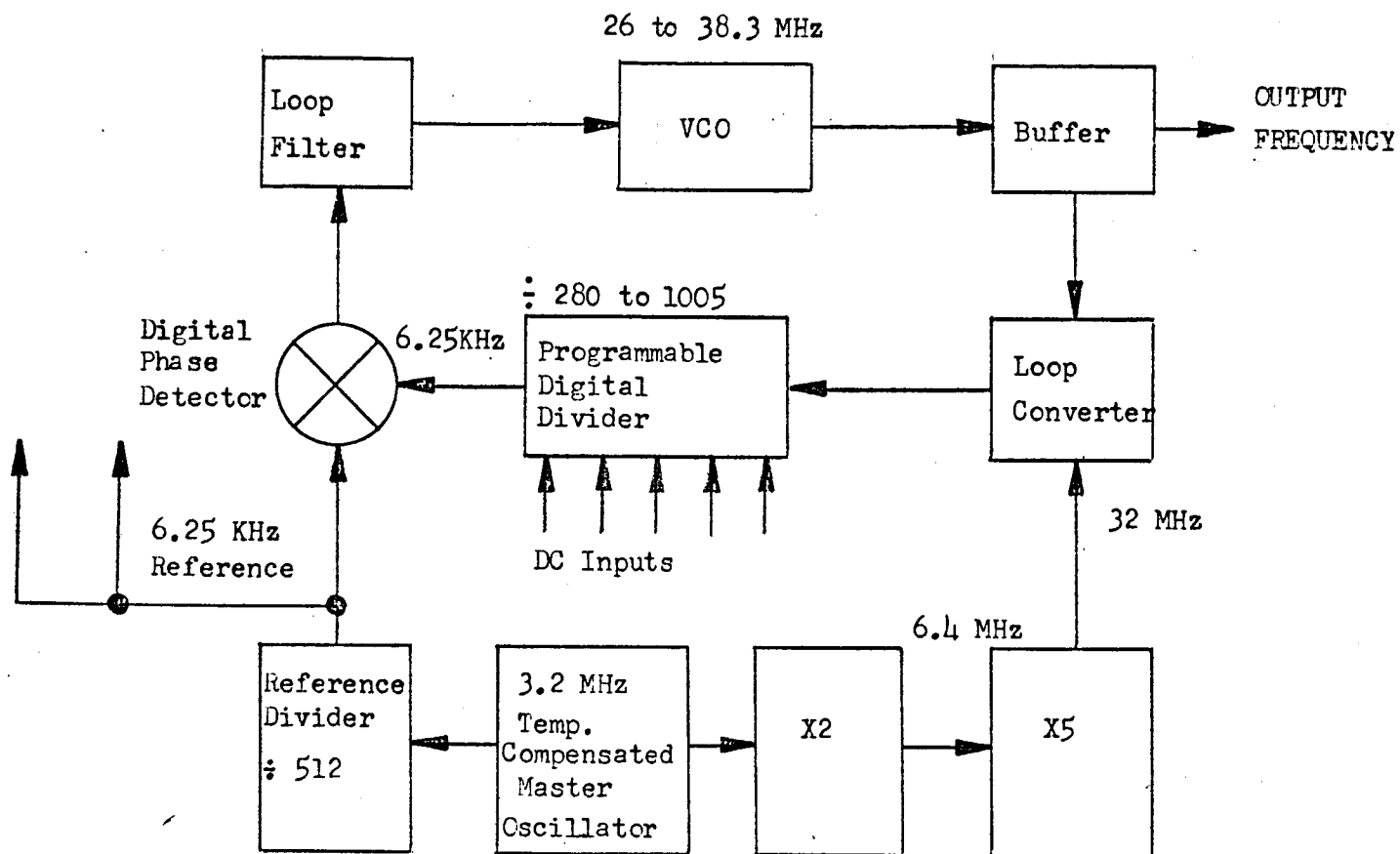


Figure 5-79. Phase Locked Loop Synthesis Technique

The master oscillator frequency is divided by 512 in a fixed divider to generate a reference 6.25 KHz from all three loops. The master oscillator frequency is also multiplied by 10 and mixed with the VCO frequency in the loop converter. The difference frequency is divided by the proper integer relationship to produce 6.25 KHz for the phase detector. The phase difference between this signal and the reference is filtered and the filter output used to drive the VCO. The VCO crystal frequencies required to provide the proper synthesizer output frequencies range from 26 to 38.28125 MHz. The

digital divider required to cover this range is programmed by the DC inputs to divide by every integer from 280 to 1005. The divider was actually designed so that it is capable of any division ratio between 3 and 2049.

5.6.1.4 Computer Aided Filter Design

The other frequencies required in the vehicle borne system are simple low order multiples of the master oscillator frequency. They are generated in a straightforward manner with frequency multiplication and mixing followed by bandpass or low pass filters to reduce the spurious signals to an acceptable level.

In order to conserve design time and eliminate the multitude of tedious computations required, a computer program was written for designing and analyzing a particular type of passive, L-C filter. The effects of stray capacitance, component self resonance, and electrical tolerance were rapidly computed and listed so that unsatisfactory conditions could be eliminated at the earliest possible stages.

As an example, the filter for the 8 MHz X5 multiplier module is shown in Figure 5-80.

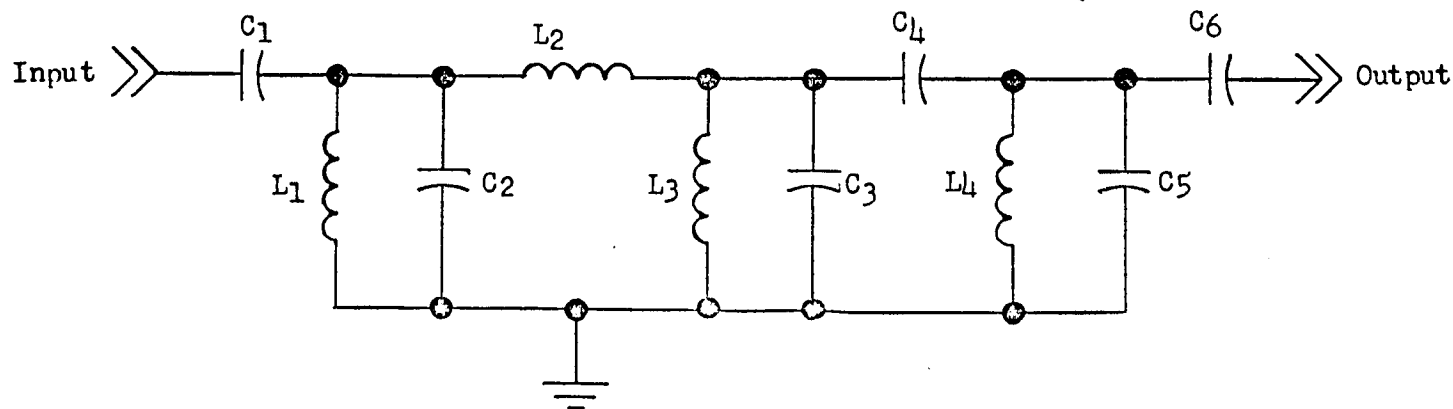


Figure 5-80. 8 MHz X5 Multiplier Filter

The filter is a 3 pole, 1/2 db ripple Tschebysheff design. The inductors L_1 , L_3 , and L_4 are the same value. The internal impedance of the filter is the product of the impedance of each resonator inductor at center frequency times the loaded "Q". C_1 and C_2 match the differential amplifier output impedance while C_5 and C_6 match the differential amplifier input impedance to the internal impedance of the filter.

The number of poles, passband ripple and loaded "Q" were chosen to give the required filtering action with a minimum attenuation at the center frequency.

With a minimum unloaded Q of 50 and a ripple of 0.25 db, the computed center frequency loss was 2.0 db while the actual loss measured was 2.5 db.

The loaded Q chosen was 8 and the computer predicted an attenuation of the 4.8 MHz spurious signal of 57 db. The actual loss measured was 53 db. Thus the filter performance proved to be quite predictable and the success of the computer aided design led to minimum design time. All of the filters were fixed tuned, an advantage which would not have been achieved for the same amount of effort without the aid of the computer.

5.6.1.5 RFI and Susceptibility Considerations

The design of the Frequency Synthesizer was coordinated with the other AROD subsystems in the area of radio frequency interference and susceptibility. The interference signals generated at the relatively higher frequencies were decoupled from the power lines within the circuit module package at their source. The lower frequencies (which require large physical size components for effective filtering) were held to low levels by including separate modules on each frame for decoupling each supply voltage separately. Conducted interference on each supply line was held to 35 microvolts or less.

In addition, tests were conducted to determine that module performance was not degraded by significant amounts (1 mv rms) of interference artificially imposed on the power lines.

5.6.2 Circuit Descriptions

The following circuit descriptions are for representative examples of each type of circuit designed for the Frequency Synthesizer. The circuits not included differ only slightly from the examples.

5.6.2.1 Doppler

Figure 5-81 is a diagram of the 7.2 MHz frequency doubler.

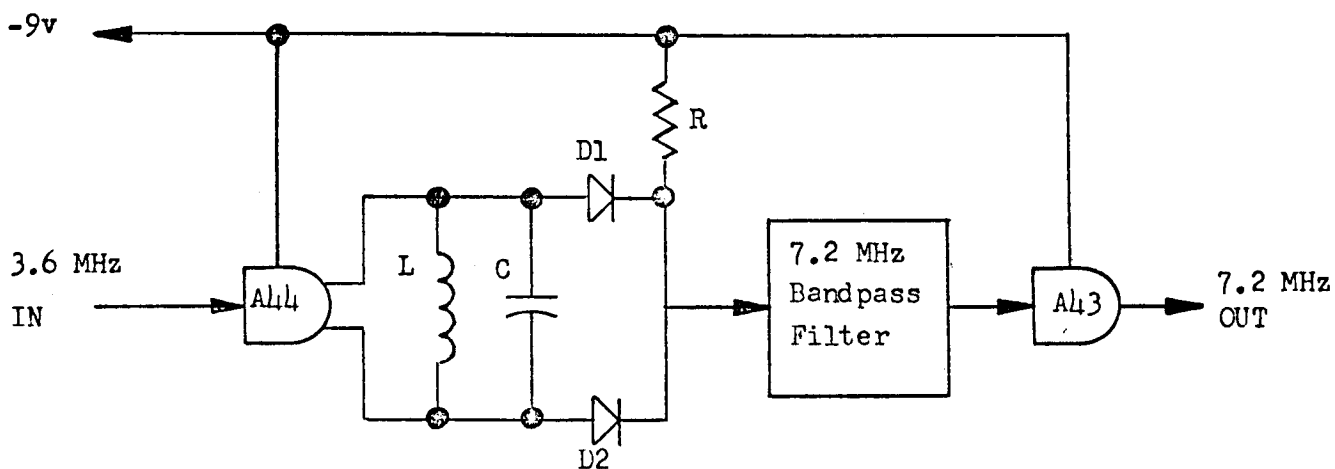


Figure 5-81. 7.2 MHz Doppler

The A14 and A13 are a low and a medium power hybrid integrated circuit differential amplifier respectively. D1 and D2 are biased slightly into conduction with no applied signal. L and C resonate at 3.6 MHz, remove the higher signal harmonics and increase the amplifier output-to-output balance. On the anode side of the diodes, the signal is a 3.6 MHz sine wave.

On the cathode side, the signal is a full wave rectified 3.6 MHz sine wave. The bandpass filter rejects the unwanted signals, passes the second harmonic of 3.6 MHz, and delivers it to the A43 buffer. The output appears as a 7.2 MHz sine wave. The synthesizer contains 4 other even order multipliers:

6.4 MHz Doubler	108 MHz X4 Multiplier
12.8 MHz Doubler	276 MHz X8 Multiplier

Their operation is similar to the 7.2 MHz Doubler explained above.

5.6.2.2 MIXER

Figure 5-82 is a diagram of the 44.8 MHz converter.

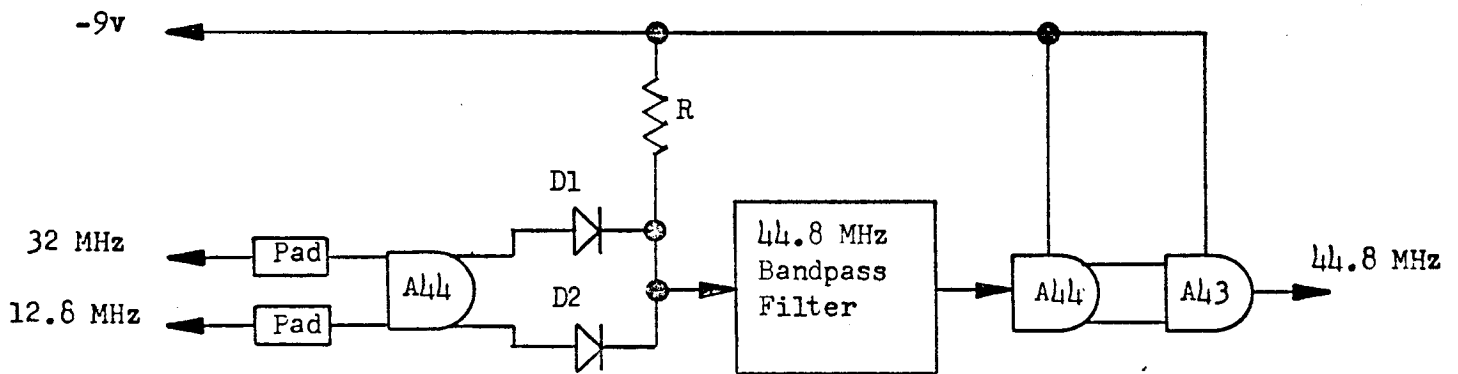


Figure 5-82. 44.8 MHz Converter

The input signals are padded to .1 volts p/p. The diodes are biased slightly into conduction with no applied signal. The amplifier gain of 20 db gives an input to the diodes of 1 volt p/p. A 4-pole bandpass filter delivers 44.8 MHz to the final amplifiers. This type of mixing is relatively inefficient but very simple and reproducible compared with a diode quad and balanced transformers. The synthesizer contains the following similar converters:

7.6 MHz Converter	XN Loop Converter
XQ Loop Converter	XR Loop Converter

5.6.2.3 Odd Order Frequency Multiplier

The odd order multiplier makes use of the very good limiting characteristics of the differential amplifier. A sine wave input at 0 dbm will give a square wave output with better than 10% rise and fall times. An example is the 8 MHz X5 multiplier shown in Figure 5-83.

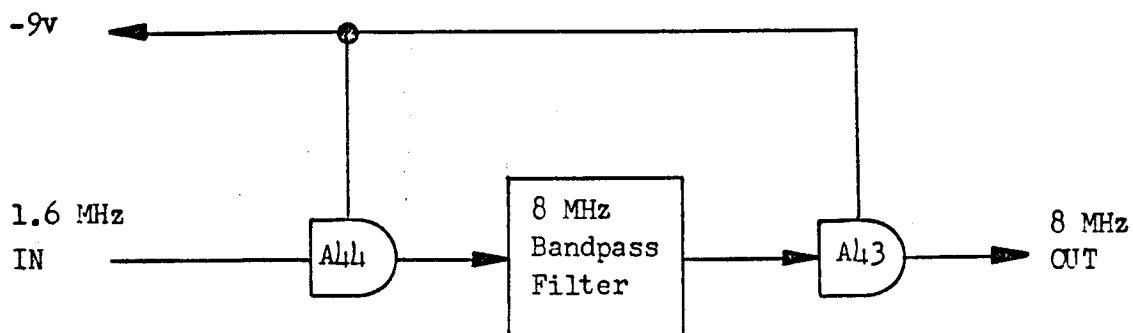


FIGURE 5-83. 8 MHz X5 MULTIPLIER

The 1.6 MHz square wave input from a digital divider is buffered and put through a 3-pole filter which extracts the fifth harmonic. The last amplifier isolates the filter from external circuitry. Multiplication ratios of 3, 7, and 9 are obtained in this manner in other modules. The synthesizer contains the following similar odd order multipliers:

- 8.4 MHz X7 Multiplier
- 3.6 MHz X9 Multiplier
- 300 KHz X3 Multiplier

5.6.2.4 Phase-Locked Loop Circuit Descriptions

Each of the three phase-locked loops consists of a digital divider, phase detector, loop filter, VCO, and frequency converter. An explanation

of the frequency converter operations was given in section 5.6.2.2. The operation of the other circuits is explained in the following sections. Table 5-4 lists the parameters of the three phase locked loops used in the Frequency Synthesizer.

Digital Dividers

The vehicle reference divider module is a fixed binary ripple counter which divides 3.2 MHz from the master oscillator by 512 to yield 6.25 KHz. The divider is tapped at 1.6 MHz ($\div 2$), 400 KHz ($\div 8$), and 100 KHz ($\div 32$). These outputs are used elsewhere in the system. The lowest output frequency of this divider is a pulse rate at a 6.25 KHz rate with a pulse width equal to the period of the input frequency, 3.2 MHz. This pulse output is provided as the reference input to the phase detector of each of the three phase locked loops.

The programmable dividers are used to allow ease in changing the output frequencies of the three phase locked loops. Division by any integer from 3 to 2049 can be obtained by applying the appropriate DC level to the programming inputs. The programmable dividers are binary ripple counters, counting from the programmed number to the zero state and then resetting. A pulse output results each time the counter resets. This occurs at a repetition rate of 6.25 KHz with a pulse width equal to one period of the input frequency. The pulse output is applied to the other input of the loop phase detector for comparison with the reference.

The digital divider circuitry is packaged in module configuration so as to provide for maximum versatility in applying the technique while maintaining standardized modules which consume minimum space. Figure 5-84

TABLE 5-4

PHASE LOCKED LOOP PARAMETERS

Synthesizer Output Signal	PLL Design	VCO f(MHz)	Converter Output f(MHz)	Programmable Divider Ratio	Noise BW B_L (Hz)	K_V	KDC	KVCO H_3 /volt	K_ϕ mv/deg.	T_1 sec.	T_2 sec.
Station Control Transmitter Carrier Ref.	XR	34.5	2.5	- 400	5	100	20	900	6.25	1.09	.15
Tracking Receiver Local Oscillator Ref. 217.7 MHz	XQ	27.2125	4.7875	- 766	5	116	66	600	6.25	1.27	.15
Tracking Transmitter Carrier Ref. 276.75 MHz	XN	34.59375	2.59375	- 415	5	100	20	900	6.25	1.09	.15

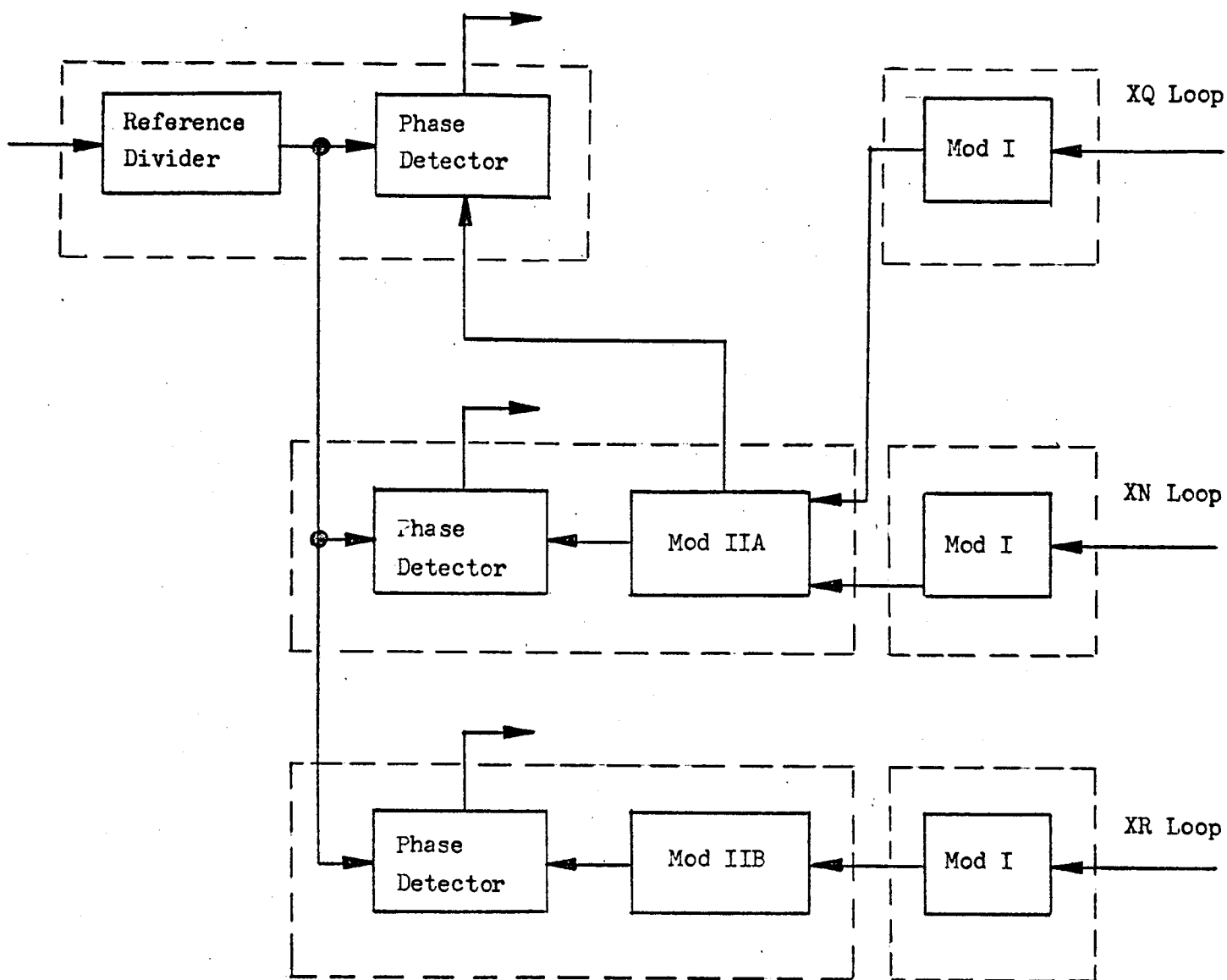


FIGURE 5-84. DIGITAL DIVIDER MODULE PACKAGING

will aid in describing the packaging configuration.

The reference divider is packaged in one module which also contains a phase detector. There are three types of modules which are used for the programmable divider function. They are termed MOD I, MOD IIA, and MOD IIB. A MOD I contains only the first part of the divider and must be used in conjunction with a MOD IIA or MOD IIB. The MOD IIB contains the last part of a divider plus a phase detector. The MOD IIA contains two separate last portions of dividers plus a phase detector. Thus the $\div 766$ is implemented with a MOD I, and one portion of a MOD IIA. The phase detector used for this configuration is the one in the reference divider. The $\div 415$ consists of a MOD I and the other portion of the MOD IIA. The phase detector in the MOD IIA is used for this loop. The $\div 400$ is made up of a MOD I and the MOD IIB. The phase detector for this loop is in the MOD IIB.

In summary, the total number of digital modules required to implement the three loops is six -- one reference divider, three MOD I dividers, one MOD IIA and one MOD IIB divider.

Phase Detector

Each of the three phase detectors is implemented with an R-S flip-flop. The output of the reference divider is applied to one side of the flip-flop while the output of the programmable divider is applied to the other side. The flip-flop changes state with each DC level change at the inputs. The output is a variable width pulse occurring at a 6.25 KHz repetition rate. The pulse width depends upon the relative phase difference between the VCO and the master oscillator.

Loop Filter

The loop filter has the same configuration for all three loops. Figure 5-85 is a simplified circuit diagram of a loop filter.

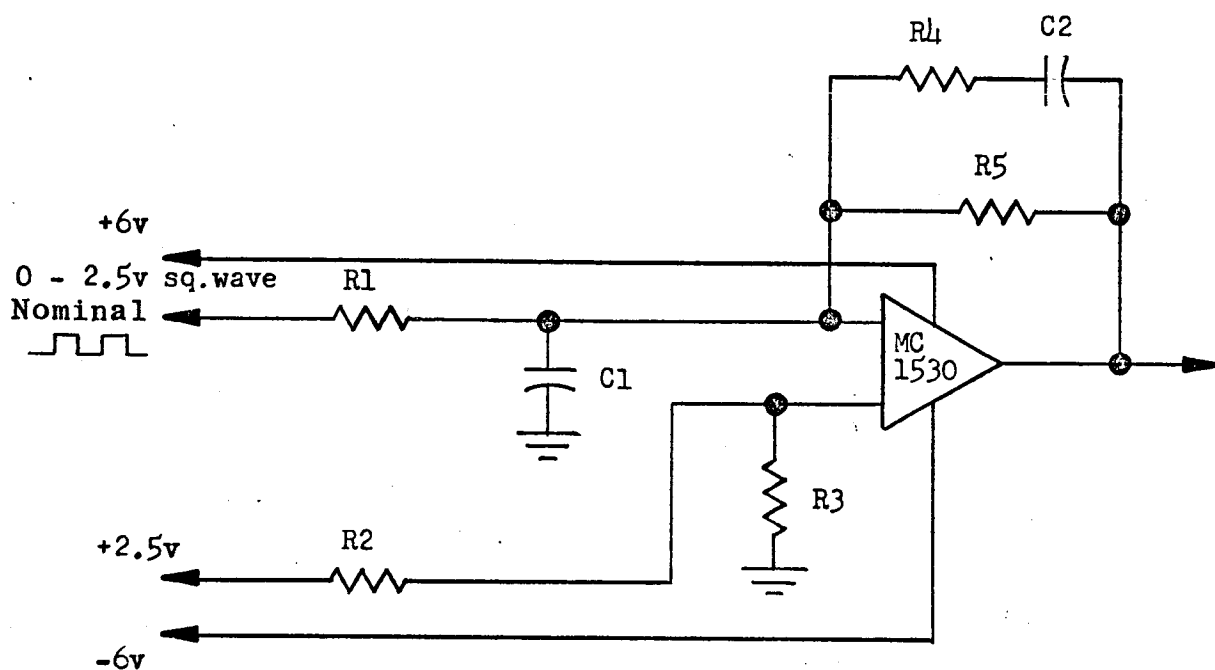


FIGURE 5-85. LOOP FILTER

R1 and C1 comprise the 100 Hz low pass filter. When the loop is locked, the input from the phase detector is a 6.25 KHz, 0 to +2.5 volt square wave from a digital buffer. The bias input, used as a DC reference for the operational amplifier, is a +2.5 volt DC signal from a forward biased diode contained within the phase detector module to compensate for temperature drifts. R2 and R3 divide this voltage to +1.25 volts at the amplifier input.

The pulse width from the phase detector is dependent upon the phase difference between the VCO and master oscillator. The loop filter converts this phase difference to an offset voltage that drives the VCO.

VCO

The VCO's are of conventional design except perhaps for the use of the hybrid integrated circuit differential amplifier as the active element. A simplified schematic is shown below in Figure 5-86.

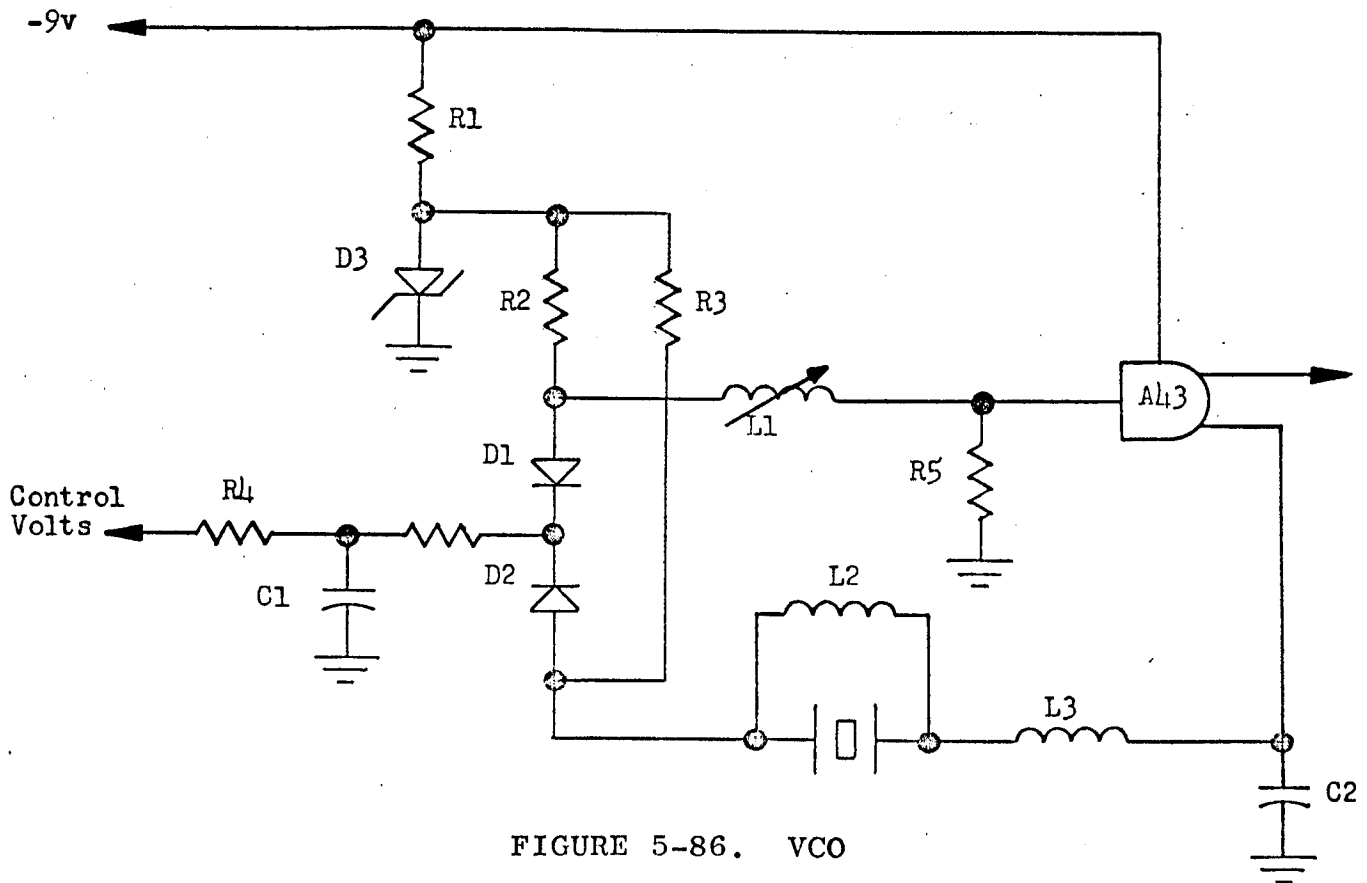


FIGURE 5-86. VCO

R4 and C1 are a 90 Hz low pass filter to provide additional discrimination against the 6.25 KHz leakage from the phase detector through the loop filter which would cause modulation of the VCO with resulting spurious signals in close proximity to the VCO frequency. D1 and D2 are low capacity varicaps. D3 is a temperature compensated Zener fixing the varicap bias through R2 and R3 at 4.7 volts. C2 and L3 match the crystal impedance to the amplifier output. The crystal itself is a standard AT cut mounted in

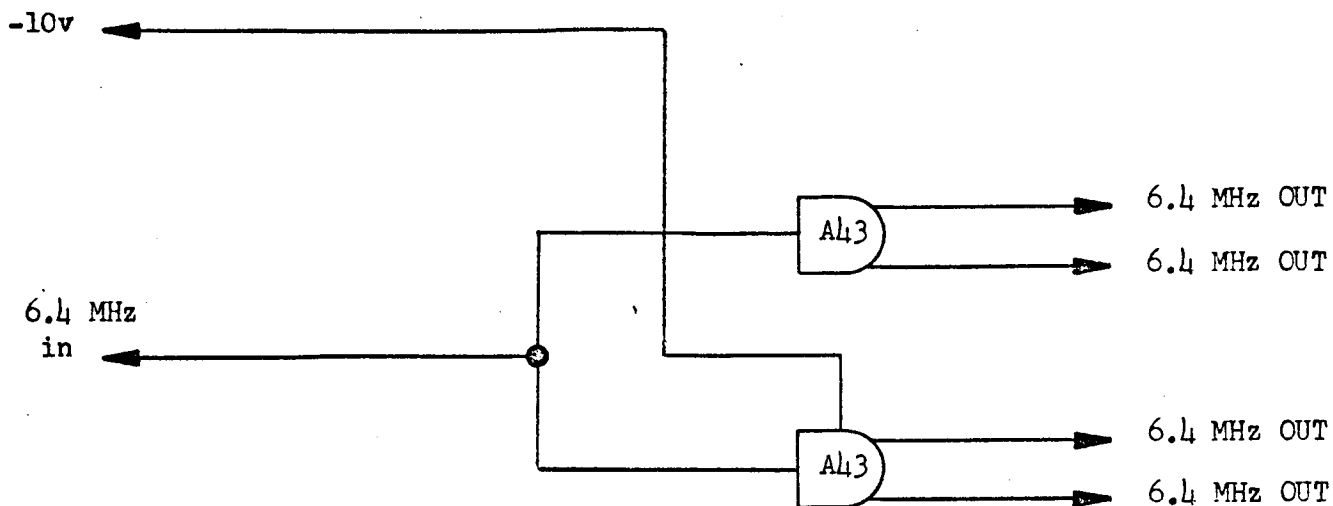
a TO-5 can. L2 tunes out the stray capacity of the crystal container and also compensates the frequency vs voltage curve to make it more linear. L1 tunes the VCO to its design center.

5.6.2.5 Distribution Amplifier

The Distribution Amplifier was included as part of the Frequency Synthesizer task, but is physically located in Case 2. The function of the Distribution Amplifier is to distribute three signals generated in Case 1 to twelve places located in Case 2. The Distribution Amplifier is designed to provide proper isolation between all of the signals as well as a convenient mounting panel for the many coaxial connectors required. Figure 5-87 is a photograph of the Distribution Amplifier.

The Distribution Amplifier has three input signals - 6.4 MHz and 44.8 MHz from the Frequency Synthesizer, and 58 MHz from the RF Converter. There are twelve outputs -- four for each of the three input frequencies. The 6.4 MHz is distributed to each of the four channel frequency preset circuits. The 44.8 MHz supplies the four Tracking Receiver bias frequencies. The 58 MHz signal is the first IF frequency containing the transponder modulation for each received channel. They are distributed to each of the four Tracking Receiver demodulators.

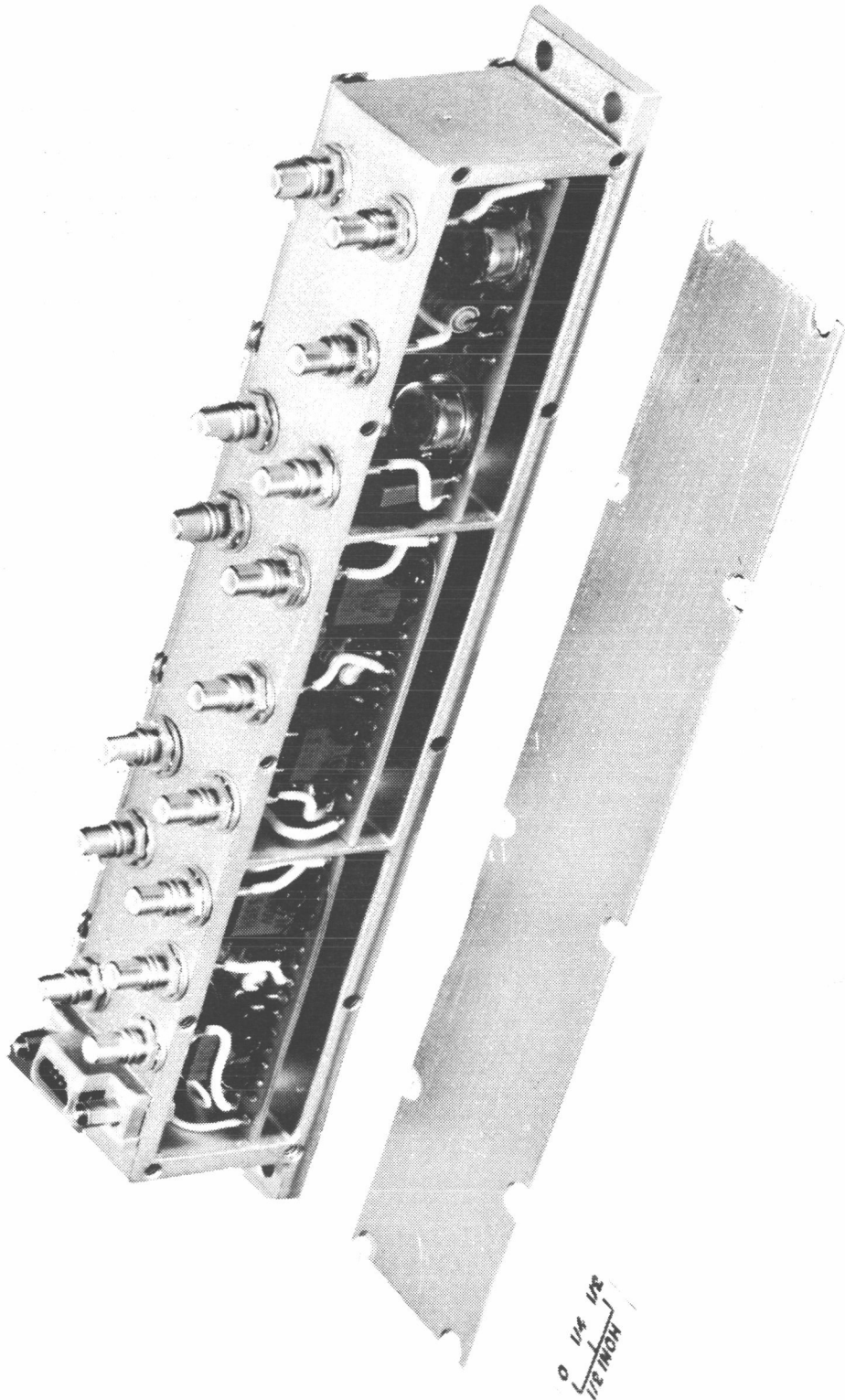
A diagram of the 6.4 MHz portion of the Distribution Amplifier is shown below. The other two portions are identical to this. The 6.4 MHz input signal drives two hybrid integrated circuit differential amplifiers in parallel. The four outputs are isolated from each other by approximately 20 db.



5.6.3 Physical Description

Table 5-5 lists the different package types which make up the frequency synthesizer. Also, the typical size, weight and component count are included for comparison purposes.

Table 5-6 lists the size, weight, and power of the three synthesizer frames.



0 1/4 1/2
1 1/2 INCH

6-2291

Figure 5-87. AROD Distribution Amplifier

TABLE 5-5. PACKAGE CONFIGURATIONS

Unit	<u>Size</u>	Typical Weight (grams)	Number of Components
RF Cordwood Module	.7" x .55" x 3.15"	28	35
Digital I/C Module	.7" x .35" x 3.15"	13.5	18
Power Supply Filter Module	.7" x .35" x 1.55"	9	7
Master Oscillator	.7" x 2.5" x 3.15"	170	40
X2 Multiplier	.7" x 1.1" x 3.05"	90	33
Helical Resonator	.7" x .34" x 1.1"	50	--
Frame Assembly	.9" x 4" x 6.2"	450	300

TABLE 5-6

Frequency Synthesizer Power and Weight Requirements

Reference Designation	Unit	Power Consumption				Weight
		-28v	+10v	+3.5v	-10v	
1A2	Frequency Synthesizer #1 Master Oscillator 5 - RF Cordwood Modules 1 Power Supply Filter Module	6 ma 168 mw			79 ma 790 mw	458 g
1A3	Frequency Synthesizer #2 6 - Digital I/C Modules 6 - RF Cordwood Modules 3 Power Supply Filter Modules		24 ma 240 mw	410 ma 1435 mw	72 ma 720 mw	489 g
1A4	Frequency Synthesizer #3 7 - RF Cordwood Modules 217 MHz X2 Multiplier and Helical Resonator 2 Power Supply Filter Modules		12 ma 120 mw		166 ma 1660 mw	498 g
	TOTAL	6 ma 168 mw	36 ma 360 mw	410 ma 1435 mw	317 ma 3170 mw	1444 g

5.13 watts

5.6.4 Performance Deviations

5.6.4.1 System Performance Deviations

The synthesizer performance was judged acceptable. Some deviations to the specification are noted below in Table 5-7. These deviations are not serious enough to impair the over-all performance.

TABLE 5-7. DEVIATIONS FROM SPECIFIED PERFORMANCE

Parameter or Signal	Design Goal	Measured Performance
12.8 MHz	rise time <10 nsec. fall time <10 nsec.	15 nsec. - rise time 20 nsec. - fall time
8.4 MHz	non-integral spurs >40 db below f_0	8 MHz is 33 db below f_0
276 MHz	278 MHz spur greater than 100 db below f_0	68 db
6.4 MHz	rise time <15 nsec. fall time <15 nsec.	20 nsec. - rise time 25 nsec. - fall time
Conducted interference on -10 volt line	less than 20 μ v	217 MHz spur = 35 μ v

5.6.4.2 Master Oscillator Performance Deviations

The master oscillator mentioned in Section 5.5.1.2 was purchased from Bendix Pioneer Central Division. Table 5-8 lists the observed deviations from the specifiable performance.

Table 5-8. Performance Deviations of Master Oscillator

	Specified Performance	Performance Deviations
1	$\pm 1 \times 10^{-7}$ frequency stability for all combinations of frequency, supply voltage and loading	$\pm 1.5 \times 10^{-7}$
2	0 dbm $\begin{matrix} +0 \\ -2 \end{matrix}$ db output power	-5 dbm output power

5.6.5 Conclusion and Results

The frequency synthesizer was designed to provide coherent frequencies required by the rest of the vehicle subsystems.

Each frequency was specified as having a given spectral purity, rise and fall time, and output level.

The master reference frequency was required to have a certain stability over temperature, supply voltage, and time.

These requirements were, in general, met quite adequately. The deviations to specifications mentioned in Sections 5.5.4.1 and 5.5.4.2 do not seriously degrade system performance.

5.7 DATA MEASUREMENTS SUBGROUP

This section is the final Engineering Report on the Data Measurements Subgroup, which was developed for use in the AROD subsystem. Table 5-9 presents a compilation of the subsystems included in the Data Measurements Subgroup and the electrical performance specifications document numbers for the corresponding subsystem.

Table 5-9. Summarization of the Data Measurements Subgroup Documentation

<u>Subsystem</u>	<u>Specification No.</u>
Vehicle Timing Unit	12-24497G
Data Readout Subsystem	12-29129G
Velocity Extraction Unit	12-29115G
Range Extraction Unit	12-24687G
Transmitter Code Control Subsystem	12-24607G

The Data Measurements Subgroup contains the data extraction logic for the AROD system. The Vehicle Timing Unit generates measurement and readout commands and provides a reference time label for the data. The Velocity Extraction Unit derives the velocity measurement data from its specified inputs. The Range Extraction Unit derives the range measurement data from its specified inputs. The Transmitter Code Control is included because it is closely associated with the range extraction technique. The function of the Data Readout Subsystem is to accumulate all of the measured data and the system status data and to organize this data into a format that is acceptable to an interfacing telemetry unit. In addition to the advantages of logically grouping this subgroup, a significant advantage in packaging was obtained. A large number of the several hundred data interconnections between the subsystems can then be made on printed circuit boards. This reduces the wiring harness size to a level that is compatible with the overall packaging scheme.

Figure 5-88 is a photograph of the Data Measurements Subgroup hardware. The equipment consists of four frame assemblies containing 10 standard power filter modules in addition to 900 integrated circuits and 150 discrete components, which are packaged in 50 I/C logic modules and 1 cordwood RF module. The combined weight is 1655 grams (3.648 lbs). The unit has the following current requirements:

- a. 3.75 amps @ +3.5 VDC,
- b. 52 ma @ -3.5 VDC,
- c. 115 ma @ +10 VDC,
- d. 20 ma @ -10 VDC.

5.7.1 Vehicle Timing Unit

This section is the final Engineering Report on the Vehicle Timing Unit Subsystem, which was developed for use in the AROD system. The basic electrical requirements for the Vehicle Timing Unit are outlined in Document No. 12-25618F.

This subsystem has two basic functions. A time label is provided as a time reference for the AROD output data. The time label must be unambiguous for a period of 5 minutes, must have a resolution of ± 10 microseconds, and must have the capability of being externally reset on external real time input. In addition, the Timing Unit must provide the necessary timing signals to control the AROD measurement cycle and accompanying signals to synchronize the Data Readout Subsystem to the measurement cycle.

This subsystem will synchronize the data readout cycle to the telemetry system if a synchronization pulse is provided by the telemetry system. If not, an internal cycle reset control is generated, which is synchronous to the L code sequence time base in the AROD system. A capability for synchronizing the measurement and data readout cycles is thus provided, which also is capable of supplying a synchronous interface between the AROD and Telemetry systems.

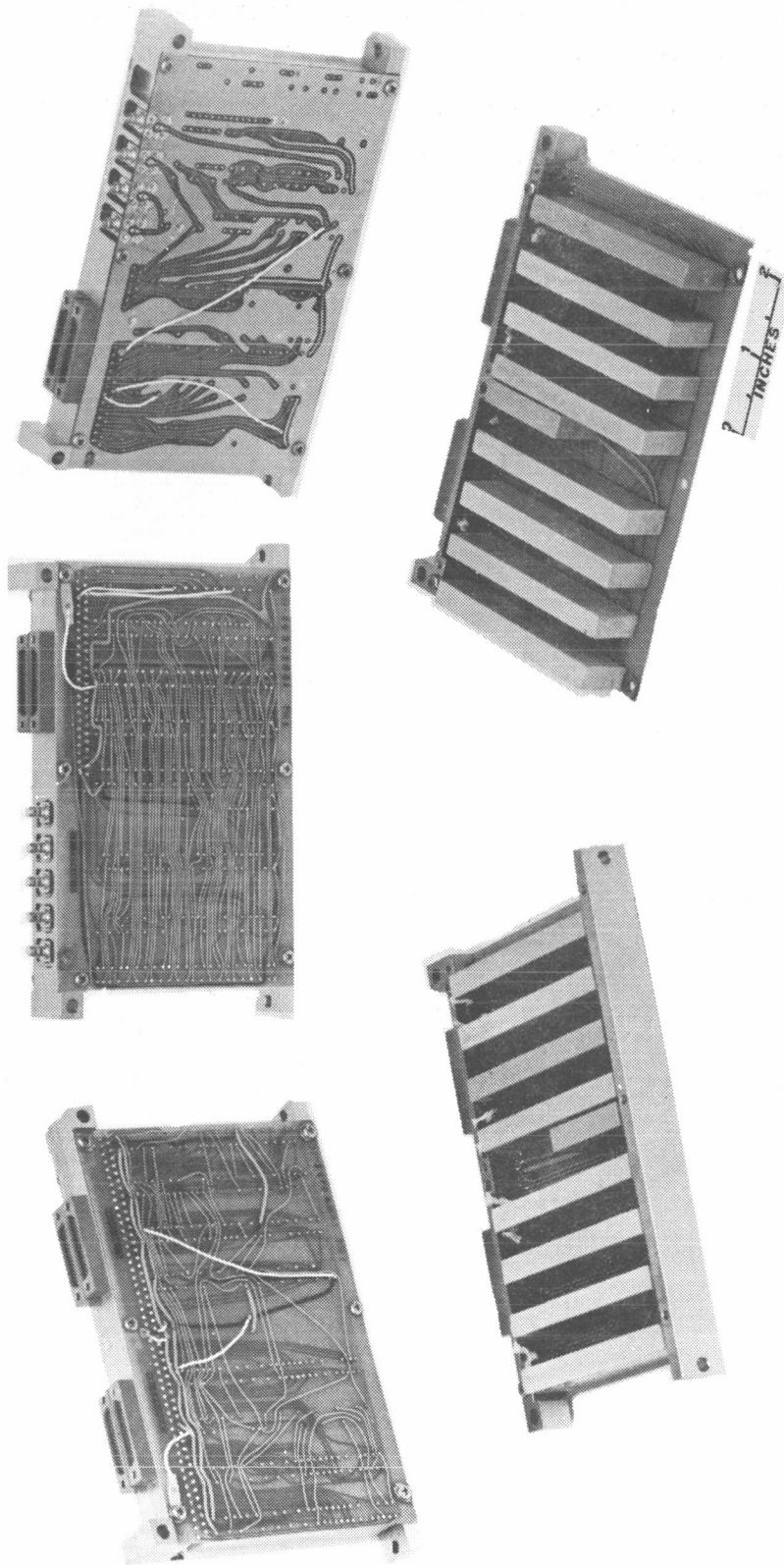


Figure 5-88. Data Measurements Subgroup

The equipment consists of four frame assemblies containing 10 standard power filter modules in addition to 900 integrated circuits and 150 discrete components, which are packaged in 59 I/C logic modules and 1 cordwood RF module. The combined weight is 1655 grams.

The Vehicle Timing Unit Subsystem uses 115 Philco integrated circuits and 9 discrete components. It is packaged in 7 I/C logic modules. This represents about 10% of the Data Measurements Subgroup. The various subsystems are intermixed on the motherboards to minimize the interconnections and noise problems. The Timing Unit subsystem requires 430 ma at 3.5 VDC, a total power consumption of 1.51 watts.

5.7.1.1 Technical Approach

A block diagram of the Vehicle Timing Unit is shown in Figure 5-89. The configuration shown represents the final implementation of the subsystem. This section presents a discussion of the technical considerations and constraints that influenced the design of the Vehicle Timing Unit Subsystem. The general factors that were considered are the specified time label requirements, the timing requirements for measurements and data processing, and the necessary interfaces for proper functioning of the AROD system.

The approach to the design of the time label source is largely established by the basic time label requirements. The most efficient method of establishing a time reference is to accumulate pulses of a stable clock signal in a simple counter. The accuracy requirement on the time label of ± 10 microseconds dictates a basic clock frequency of 100 kHz (10 microseconds per cycle). To meet the unambiguous condition of five minutes, 30,000,000 counts must be accumulated. This requires a 25 stage binary counter that resets automatically after the proper number of counts. In addition, some means of resetting from an external source, RESET-RT, must be provided.

The measurement cycle for the AROD system is controlled by the Vehicle Timing Unit. A cycle reset signal, RESET-C, is generated internal to the Timing Unit. This signal occurs in response to a 4 Hz synchronizing signal from telemetry (optional) or every 13 L₁₂₇ periods if no telemetry signal is available. RESET-C marks the beginning of a measurement cycle and is used to initiate a readout cycle in the Data Readout Subsystem. The measurement cycle proceeds as follows:

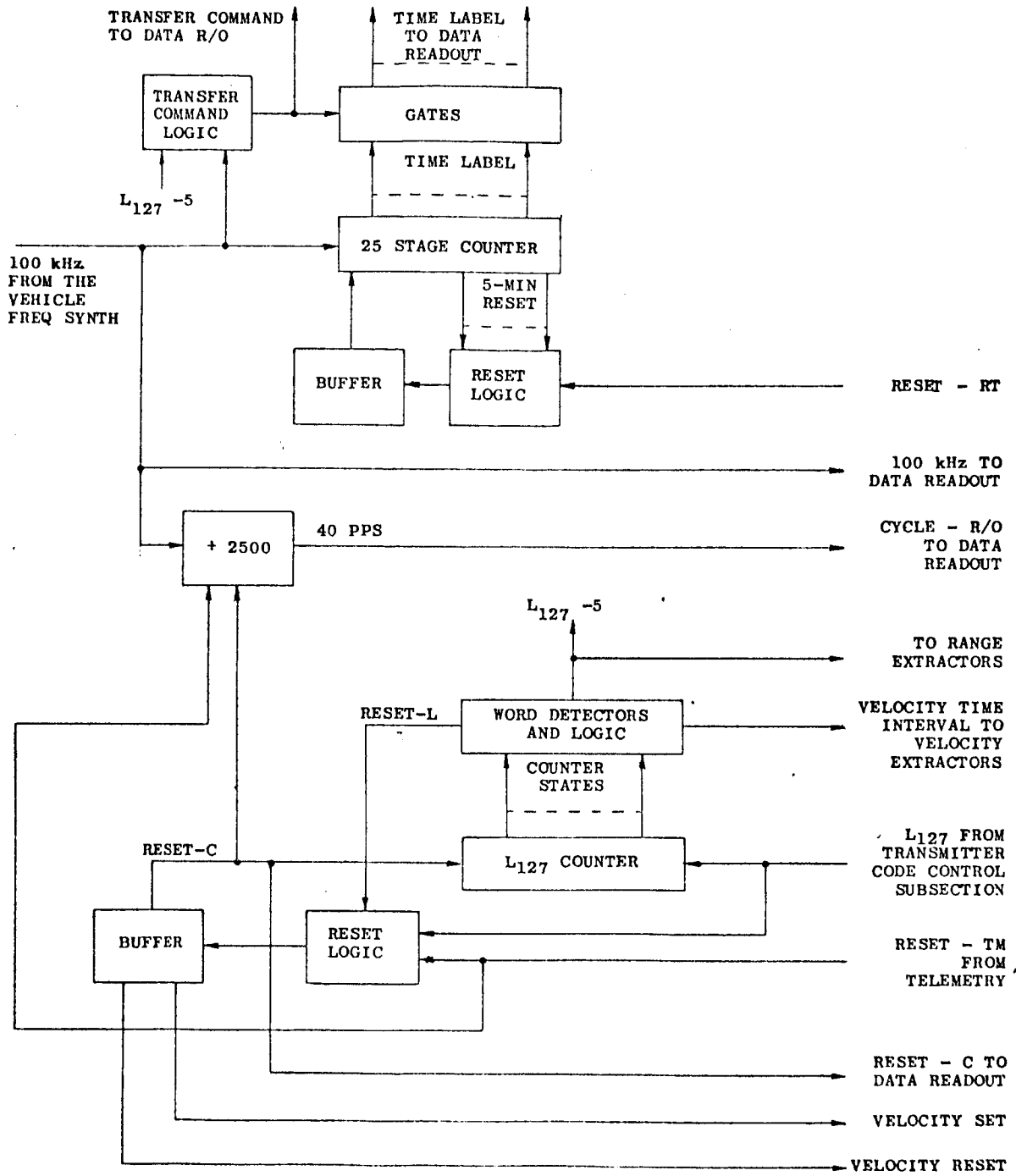


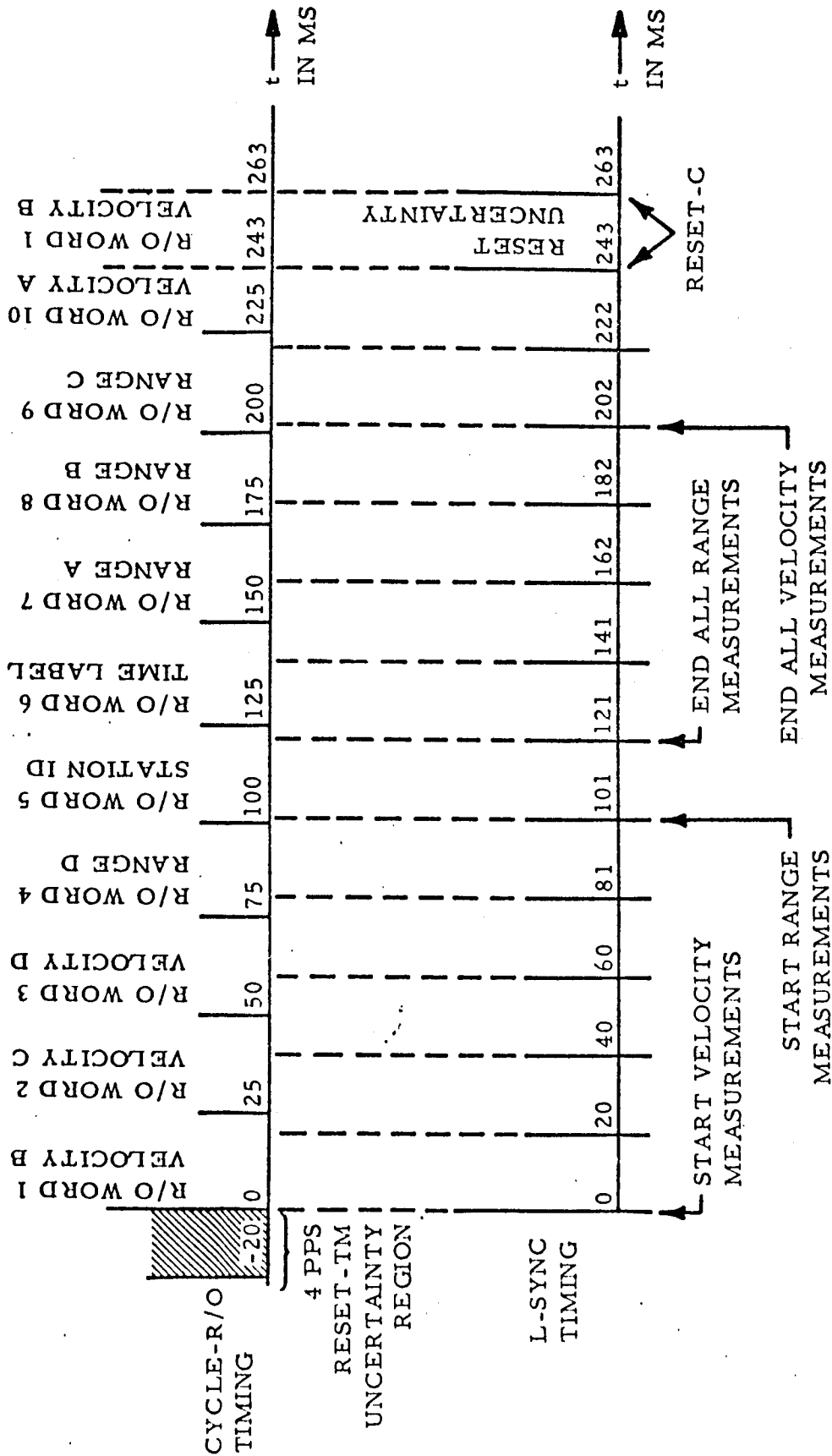
Figure 5-89. Vehicle Timing Unit

- a. The velocity measurements are initiated by the negative transition of the first L_{127} pulse to follow the RESET-C signal;
- b. The range measurements are initiated by the negative transition of the sixth L_{127} pulse to follow RESET-C and are completed during the subsequent L_{127} period;
- c. The velocity measurements are terminated by the negative transition of the eleventh L_{127} pulse to follow RESET-C.

The timing diagram of the entire measurement and readout cycle for the AROD system is shown in Figure 5-90. A detailed discussion of the readout cycle may be found in Section 5.7.2.

The timing function of the Vehicle Timing Unit incorporates two basic reference clock signals, the 100 kHz clock and the L code sequence clock (L_{127}). The data readout synchronization signals are derived from the 100 kHz signal and are coherent with this clock. All measurement commands are derived from the L_{127} signal. The various reset commands to the Range and Velocity Extraction Units are time related to the L_{127} signal, but the transitions of the reset signals are synchronous with the 100 kHz clock. The purpose for such an arrangement is to provide a pseudo-synchronism and some defined time relationships between the various AROD subsystems.

Several logic function elements are required to establish the logic references used in performing the timing function as described above. A Divide by 2500 Counter is necessary to derive a 40 Hz Data Readout sequencing signal, CYCLE-RO, from the 100 kHz input clock. The L_{127} pulses must be accumulated in a counter to maintain a reference for the various measurements. The Timing Command Logic utilizes the accumulated timing information in the forming of the reset and measurement commands, which include:



NOTE: CASE SHOWN IS FOR RESET-TM AVAILABLE. WITH NO RESET-TM, RESET-C WILL OCCUR EVERY 13 L-SYNC PULSES WITH NO UNCERTAINTY

Figure 5-90. Timing Diagram for Data Readout Cycle

5348-16

- a. SET-VEL, a signal used in presetting the proper number in the velocity counters,
- b. RESET-VEL, a signal used to reset the velocity counters,
- c. VELOCITY TIMING INTERVAL, the precise timing signal which controls the duration of the velocity measurement,
- d. START RANGE MEASUREMENT COMMAND, a signal that is used to reset the range counters and mark the proper L code sequence to be used in range measurements.

This method of implementing the Vehicle Timing Unit is technically complete. Each requirement that is imposed by the system has been fulfilled and no critical areas exist, either in timing or in actual hardware implementation. The Timing Unit will, as described herein, be fully adequate for the AROD system.

5.7.1.2 Logic Description

In this section, the logic design of the Vehicle Timing Unit will be discussed. Refer to Figure 5-89 for a basic block diagram of the subsystem. The design will be discussed on a general, functional basis.

Time Label Counter

The time label counter is a 25 stage ripple counter. It accumulates counts of the 100 kHz input clock, as supplied by the Frequency Synthesizer Subsystem. When a count of 30,000,000 is detected, the counter is reset, thereby providing an unambiguous time interval of 5 minutes. A parallel reset function is supplied for use in externally resetting the time label as a means of providing a real time reference for the time label. Both reset signals are reclocked by the complement of the 100 kHz clock in a logic circuit that may be referred to as a synchronous monostable multivibrator.

Figure 5-91 shows the logic implementation of the synchronous monostable multivibrator. A timing diagram of the input and output signals is shown in Figure 5-92.

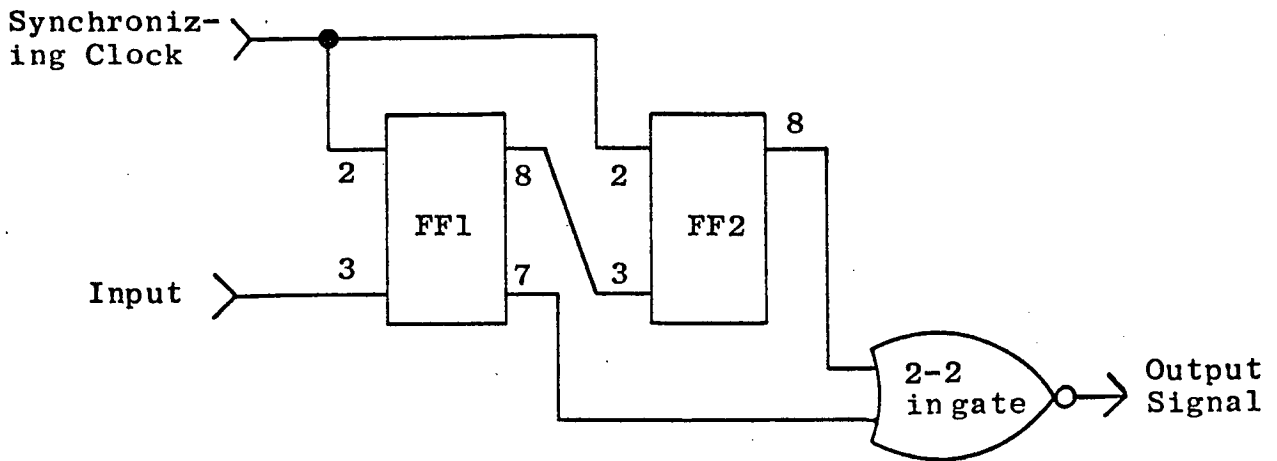


Figure 5-91. Synchronous Monostable Multivibrator

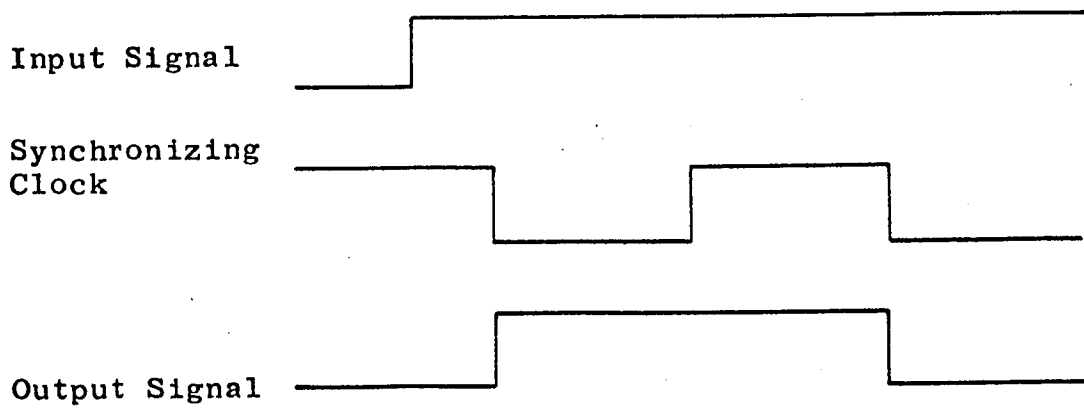


Figure 5-92. Timing Diagram for the Synchronous Monostable Multivibrator

Proper operation of this logic device depends upon having a clock transition in both the logic "one" and "zero" states of the input signal. If this condition is met, the output pulse will occur as shown. This pulse is generated by detecting, in G1, the FF1, FF2 condition of 1,0 respectively. Such a condition will occur only after the first clock pulse to follow a positive transition of the input signal.

The false outputs of the time label counter flip-flops are presented to the transfer gates. An enabling signal, TRANSFER-TL, is generated by detecting the sixth count in the L_{127} counter, inhibiting this signal until L_{127} returns to the "zero" state, and reclocking the resultant signal in a synchronous monostable multivibrator with the complement of the 100 kHz clock. This procedure presents the time label to the Data Readout Subsystem immediately after it is updated by the first clock pulse to follow the start of the range measurements, which started with the negative transition of the sixth L_{127} signal.

L_{127} Counter

The L_{127} counter is a four stage binary counter that accumulates counts based on the leading edge of L_{127} pulses. The counter is reset to the all "ones" state by RESET-C. This establishes a reference for the timing of the data measurement cycle. Three states of this counter are detected and the information is used to control the generation of the required timing pulses. When the sixth count is detected, the START RANGE MEASUREMENT COMMAND is generated on the leading edge of the L_{127} pulse and the TRANSFER-TL signal is generated on the trailing edge of the L_{127} pulse. The START RANGE MEASUREMENT COMMAND is synchronously reclocked by the 100 kHz clock. When the tenth count is detected, a pulse, L_{127} -10, is generated on the trailing edge of the L_{127} pulse. L_{127} -10 is used to end the velocity measurements. The twelfth count is detected and a signal, RESET-L, is generated on the trailing edge of the L_{127} pulse. This signal is used to generate RESET-C if no telemetry synchronization signal is available. The next L_{127} would, in this case, mark the beginning of a new measurement cycle.

Reset-C Logic

RESET-C is the start command for the data measurement and read-out cycles. It is generated when a telemetry reset pulse, RESET-TM, occurs or when RESET-L occurs if the RESET-TM signal is not available. Both signals are reclocked by the complement of the 100 kHz clock and have 10 microsecond pulse widths. The RESET-TM signal sets up an inhibit command to the RESET-L signal. This inhibit is reset by RESET-L, but it requires one cycle to reset the inhibit command. As long as the RESET-TM pulse is present, no RESET-L signal will be effective.

The two parallel reset functions are then combined in an "or" gate and used to set the output of a Philco register to a logic "zero". After 10 microseconds, the reset pulses return to the "zero" state and the 100 kHz clock resets the flip-flop output to the logic "one" state, provided L_{127} is at the logic "zero" level. The output of the flip-flop is presented to a 15 microsecond monostable multivibrator. The output of the multivibrator, RESET-C, is synchronized to the complement of the 100 kHz clock in a synchronous monostable multivibrator. The resultant signal is RESET-C. The intermediate RESET-C' signal is required by Data Readout to stop the velocity data transfer before the RESET-C resets the velocity counters.

Velocity Measurement Control

The velocity measurement control signal, VELOCITY TIMING INTERVAL, is provided by the Vehicle Timing Unit. RESET-C sets up an enable gating sequence for the first L_{127} pulse to follow. The negative transition of this first L_{127} pulse is used to set the output of a flip-flop to a logic "one" and to re-establish an inhibit gating sequence for the L_{127} signal. The flip-flop output then remains high until L_{127}^{-10} causes the flip-flop output to return to the "zero" level. The flip-flop output is inverted in a Philco buffer element to provide the necessary timing signal. The minimization of propagation delays between L_{127} transitions and the VELOCITY TIMING INTERVAL was a determining factor in the actual logic configuration. The purpose

for this was to maintain a precise interval period by minimizing the effect of delay variations in Philco logic elements.

The Vehicle Timing Unit also provides the signals used to preset the velocity counters. RESET-C is gated with both phases of the 100 kHz clock to provide SET-VEL and RESET-VEL. The three signals are then provided to the Velocity Extraction Units with a timing relationship as shown in Figure 5-93.

Divide By 2500 Counter

The Divide by 2500 Counter is a straightforward 12 stage counter that accumulates counts of the 100 kHz clock. The count, 2500, is detected and a reset signal is generated that resets the counter to the all "ones" state. A 40 Hz pulse of 10 microseconds duration is generated. This signal, CYCLE-RO, is used to sequence the Data Readout Timing Generator. RESET-C also resets the counter in order to reference the sequencing of Data Readout.

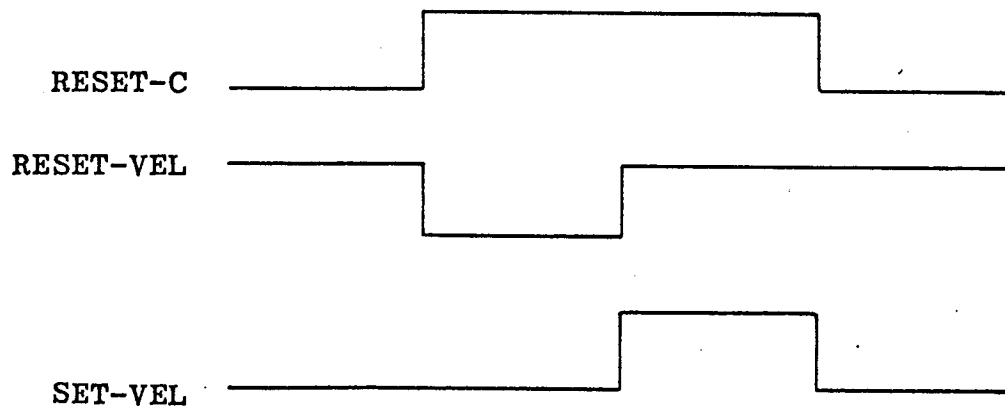


Figure 5-93. Timing Diagram of the Velocity Preset Signals

5.7.1.3 Discrete Component Circuits

The use of discrete components was limited to the telemetry interface circuits in the Vehicle Timing Unit. Two such circuits are used in the subsystem for the RESET-TM and RESET-RT signals, as provided by the Telemetry System. The initial phase of the AROD program defined the Digital Multiplexer, Model 410, as the unit with which the AROD system would interface. The specifications of the Digital Multiplexer have been interpreted by the AROD personnel to require the following input signal properties in interfacing the telemetry system to the AROD system:

Input voltage levels:

Logic "1", 7 ± 1 volts,

Logic "0", 0 ± 1 volts;

Input Impedance: 100 K ohms, minimum;

Transition times: 30 microseconds, maximum;

Pulse widths: 130 ± 20 microseconds.

The circuit that was designed to provide this function is shown in Figure 5-94.

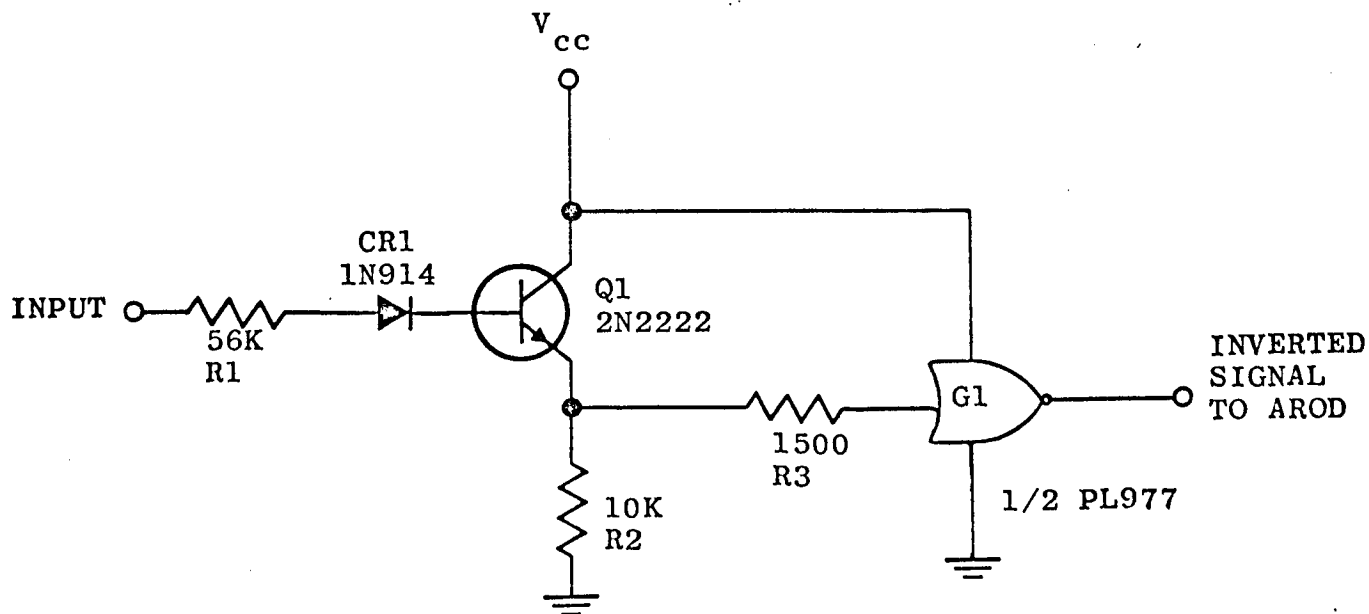


Figure 5-94. Interface Circuit for Telemetry to AROD Interfacing

The circuit is basically a low current, emitter follower stage that activates a Philco logic inverting gate. R1 is used to limit the base current and to drop part of the 7 volt logic "one" voltage swing. CR1 is used to provide reverse bias protection for the transistor. R3 is used to further limit the voltage and current levels into the Philco unit.

This circuit was tested over $\pm 10\%$ power supply limits and under all specified input signal conditions. The circuit performed without marginal conditions over the full -25° to $+85^{\circ}\text{C}$ temperature range. The circuit is completely adequate for this application and is easily adaptable to other interface sources.

5.7.1.4 Test Results

This section is intended to summarize the testing that was performed upon the Vehicle Timing Unit Subsystem and to evaluate the performance of the subsystem with respect to system requirements.

Each of the 7 I/C modules was subjected to pre-weld and post-pot testing. The purpose of these tests was to verify the logic design and to assure that all assembly documentation was in order. The next phase of testing was at the subsystem level.

At this point, the subsystem was tested as a workable unit. Inputs were supplied from either Philco logic in the test fixture or from standard pulse generators. Signal parameters were established that would verify that the logic would perform under all specified Philco signal parameter conditions. All subsystem outputs were checked for logic accuracy and against specified standard parameters required in the Philco logic family. The subsystem was subjected to the full environmental temperature range from -25°C to $+85^{\circ}\text{C}$.

In addition, the Vehicle Timing Unit was used in the testing of the Data Readout Subsystem and again used in the Data Measurements Subgroup acceptance testing. The latter test also included environmental temperature testing. Minor interface problems were

encountered at this level, but minor changes in the logic remedied this problem. No problem was encountered in actual operation of the unit at any time during these tests.

A review of the test data reveals that only one minor problem exists in the unit. Stage 17 of the time label counter will not operate at -25°C and low power supply tolerance of 3.16 volts. The failure mode is a latching to a "one" level by the flip-flop. Measurements were made which showed that the unit was fully operational over the entire power supply tolerance range at -15°C . Since the minimum specified ambient operating temperature is 0°C , and since the equipment experiences an internal temperature rise to some point above this, the decision was made to bypass the repair of this module on the basis that it was quite acceptable for current system requirements. It should be stressed, however, that this is not a design defect and the problem will not reoccur on other units since a better integrated circuit screening process is now in effect.

At the end of the Data Measurements test phase, it was concluded that the Vehicle Timing Unit would very adequately meet the AROD system requirements. The unit met all functional requirements and provides output signals to other AROD subsystems that will meet the specifications for the Philco logic family. Except as noted, the unit performed over the full temperature with no marginal operational conditions in evidence. Power supply variations of $\pm 10\%$ will not degrade the performance of the subsystem. The subsystem requires 430 ma, which is within the design limits. The unit is thoroughly tested and its performance assures that it is acceptable and adequate for the AROD system application.

5.7.2 Data Readout System

This section is the final Engineering Report on the Vehicle Data Readout Subsystem, which was developed for use in the AROD system. The basic electrical requirements for the Data Readout Subsystem are outlined in Document No. 12-25616F.

This subsystem has the function of non-computational processing of the measured data into a format which is acceptable to an existing telemetry system. This processing includes data transfer, data storage, word formatting and output interface buffering. The data inputs to the Data Readout Subsystem include the four channels of range data, the four channels of velocity data, the vehicle time label, the channel site identification data, the vhf control message data and various system status data during the acquisition mode.

The data is organized into ten data words, with each word consisting of 30 bits. The ten word readout cycle is synchronized to a data measurement cycle. Four such measurement and readout cycles per second are performed, which results in a 40 Hz word rate to the telemetry system. Where it is useful in the control of system operations, certain data is also routed to the System Control Logic.

The Data Readout Subsystem uses 375 Philco integrated circuits and is packaged in 23 I/C logic modules. This represents about 35% of the Data Measurement Subgroup. The various subsystems are intermixed on the motherboards to minimize the interconnection and noise problems. The Data Readout subsystem requires 1515 ma at 3.5 VDC at 55 ma at +10 VDC for a total power consumption of 5.85 watts.

5.7.2.1 Technical Approach

A block diagram of the Data Readout Subsystem is shown in Figure 5-95. The configuration represents the final implementation of the subsystem. This section presents a discussion of the various technical considerations and constraints that influenced the system organization of the Data Readout unit. The

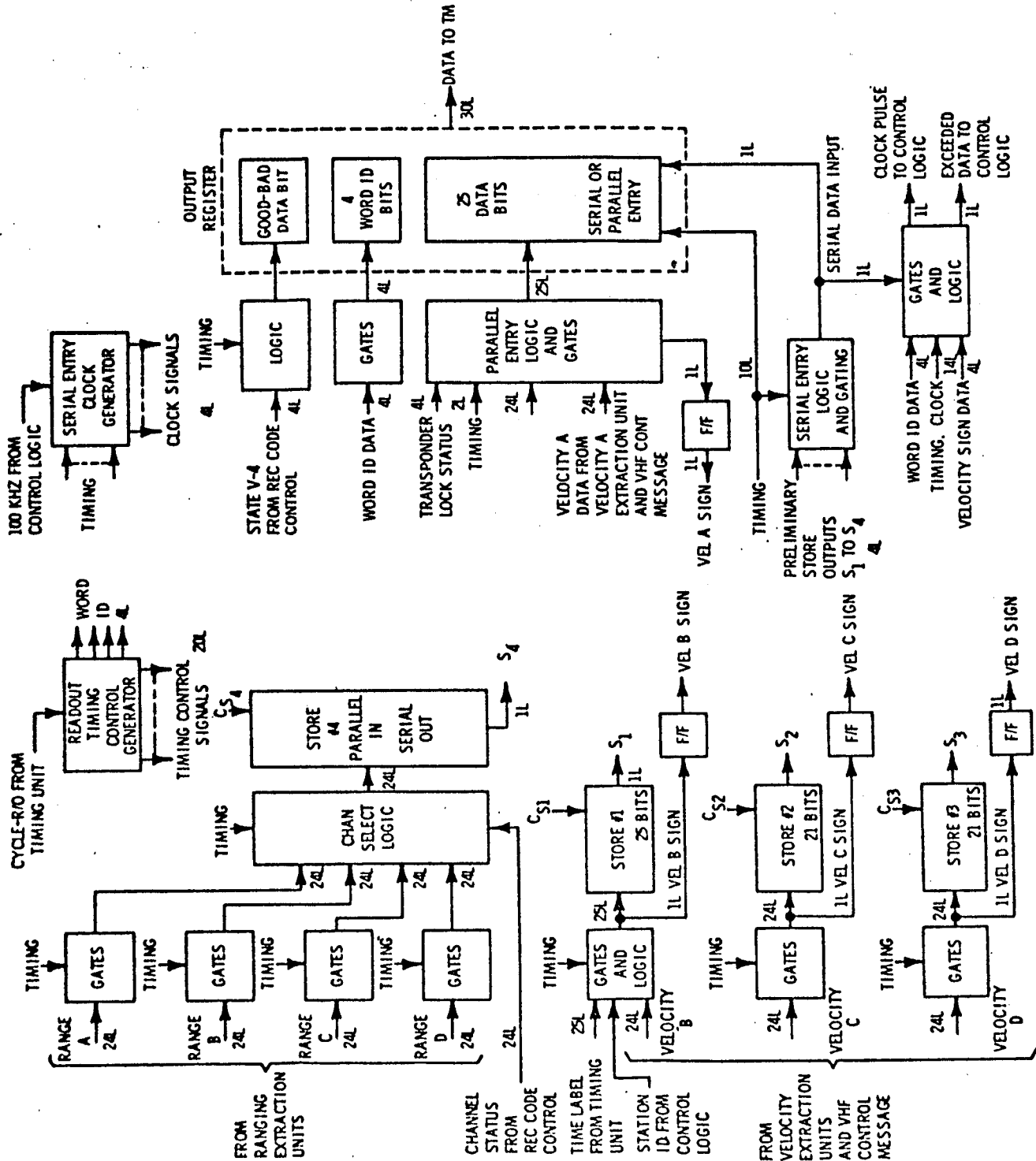


Figure 5-95. Data Readout Unit - Block Diagram

general factors that were considered are output data timing and signal parameters, input data timing and signal parameters, data formats, quantities of data and availability of data.

The output data requirements establish the basic guidelines for the Data Readout implementation. Ten data words are required to transfer to telemetry a block of time related data, which consists of the time label, the site identification data, four measured velocities and four range measurements. Other data is also processed, but it is processed in unused word bits or is substituted for the basic data at appropriate times and will be discussed later in a detailed word format description. The telemetry multiplexer accepts data in groups of ten parallel bits, with each of ten such groups being sampled at a 40 Hz rate. The AROD system is allotted the use of three such data groups, effectively establishing a word rate of 40 wps at 30 bits per word. A complete block of data is therefore transferred in 250 ms. Since the maximum time required by the AROD system for any measurement is 223.3 ms including ambiguities, the 250 ms readout cycle period is adequate as far as obtaining the data is concerned.

In order to achieve an optimum interface with the telemetry system, it is necessary to synchronize the output word sequence to the telemetry sampling signal to avoid the readout of data during transition periods or other inappropriate times. It is also desirable to synchronize the readout and measurement cycles to assure a fixed time relationship between the two functions. Since the telemetry system must operate in conjunction with many systems and cannot be modified specifically for any one system, a 4 Hz synchronizing reset signal is provided by the telemetry system (optional). The AROD system will generate a similar signal internally should there be no telemetry command input. It should be noted, however, that the internal period is 13 L code periods (263.64 ms) and is asynchronous to the telemetry system. A complete description of the timing of the measurement and readout cycles is contained in Section 5.6.1.

The Vehicle Timing Unit controls the timing of specific measurements during the measurement cycle. The measurements are synchronized to the beginning of the L code sequence and are therefore asynchronous to the telemetry requirements. The duration of the measurements directly affects the Data Readout unit, since the quantity of data that is available for readout and the duration of the availability of the data is therein controlled. The four velocity measurements start at the beginning of the first complete L code sequence to follow the measurement cycle reset signal, RESET-C, which is a composite of both the internal and external reset commands. Ten complete L code sequences later, the velocity measurements are completed. Within 223.3 ms, including the ambiguity, the velocity data is present for readout until the velocity data counters are reset by the next measurement cycle reset pulse (17-47 ms later). At the beginning of the sixth L code sequence, the range data counters are reset and a new measurement is started. That measurement is completed within one L code sequence (20.28 ms) and the range data is presented for readout until midway through the next measurement cycle. The time label data is transferred to the Data Readout Subsystem at the beginning of the range measurements. The site identification and vhf code data is available at any time, provided a minimum of 20 ms is allowed for the data transfer. The latter condition is necessary in order to bracket an inhibit signal that indicates a transitional period for the associated data. Other supplemental data is always available and may be used at any time during the readout cycle.

When the output data flow requirements are reviewed with respect to the input data flow, it becomes obvious that

several data words must be stored by the Data Readout unit until they can be conveniently inserted into the overall output data format. A data storage readout sequence was developed with minimization of total Data Readout storage requirements and compatibility with the 4 Hz measurement cycle rate being the controlling factors in the subsystem design. This sequence of operations utilizes the Output Register, which interfaces with the telemetry unit and four storage elements, Store #1, Store #2, Store #3, and Store #4. In the following discussion, the readout process refers to the serial or parallel transfer of a data word into the output register, where it is presented to the telemetry system, within 250 μ s after the readout command, for the duration of word time. The storage readout sequence of operations is as follows:

$t = 0$ A RESET-C pulse will occur which initiates the readout of the first word, velocity B, which was stored in Store #1 during the previous cycle. A readout cycle reference time, $t_r = 0$, is established. The velocity counters are reset.

$t_r = 0$ to 20.3 ms (Measurement-Readout time ambiguity)

The first L code sequence of the cycle will begin, thereby initiating the four velocity measurements. A measurement cycle reference time, $t_m = 0$, is established.

$t_r = 25$ ms

The readout of the velocity C word, which was stored in Store #2 during the previous cycle, will occur.

$t_r = 50$ ms

The readout of the velocity D word, which was stored in Store #3 during the previous cycle, will occur.

$t_r = 75$ ms

The range D word, which is available in the range data counters, will be read out, incorporating Store #4, that is functionally a parallel to serial data converter.

$t_r = 75$ to 100 ms

The site identification data will be stored in Store #1, which is not in use. The 25 ms storage period assures that the data will be enabled and transferred into the storage element.

$t_r = 100$ ms

The site identification data will be read out from Store #1.

$t_m = 101.4$ ms

The range counters are reset and all range measurements are started. The time label will be stored in Store #1, that is again available. This event corresponds to $t_r = 101.4$ to 121.68 ms.

$t_m = 121.68$ ms

All range measurements are completed and the data is available for readout. The data will remain in the range counters until the appropriate readout times.

$t_r = 125$ ms

The readout of the time label word from Store #1 will occur.

$t_r = 150$ ms

The readout of the range A word will occur, incorporating Store #4.

$t_r = 175$ ms

The readout of the range B word will occur, incorporating Store #4.

$t_r = 200$ ms

The readout of the range C word will occur, incorporating Store #4.

$t_m = 202.8$ ms

All velocity measurements are completed and the data are available for readout until the next RESET-C pulse occurs. This event corresponds to $t_r = 202.8$ to 223.08 ms.

$t_r = 225$ ms

Direct readout of the velocity A word will occur.

The velocity B word is stored in Store #1.

The velocity C word is stored in Store #2.

The velocity D word is stored in Store #3.

$t_r = 250$ ms

A RESET-C pulse will occur if a telemetry interface synchronization signal is provided.

$t_r = 263.64$ ms

A RESET-C pulse will occur if no telemetry interface synchronization signal is provided.

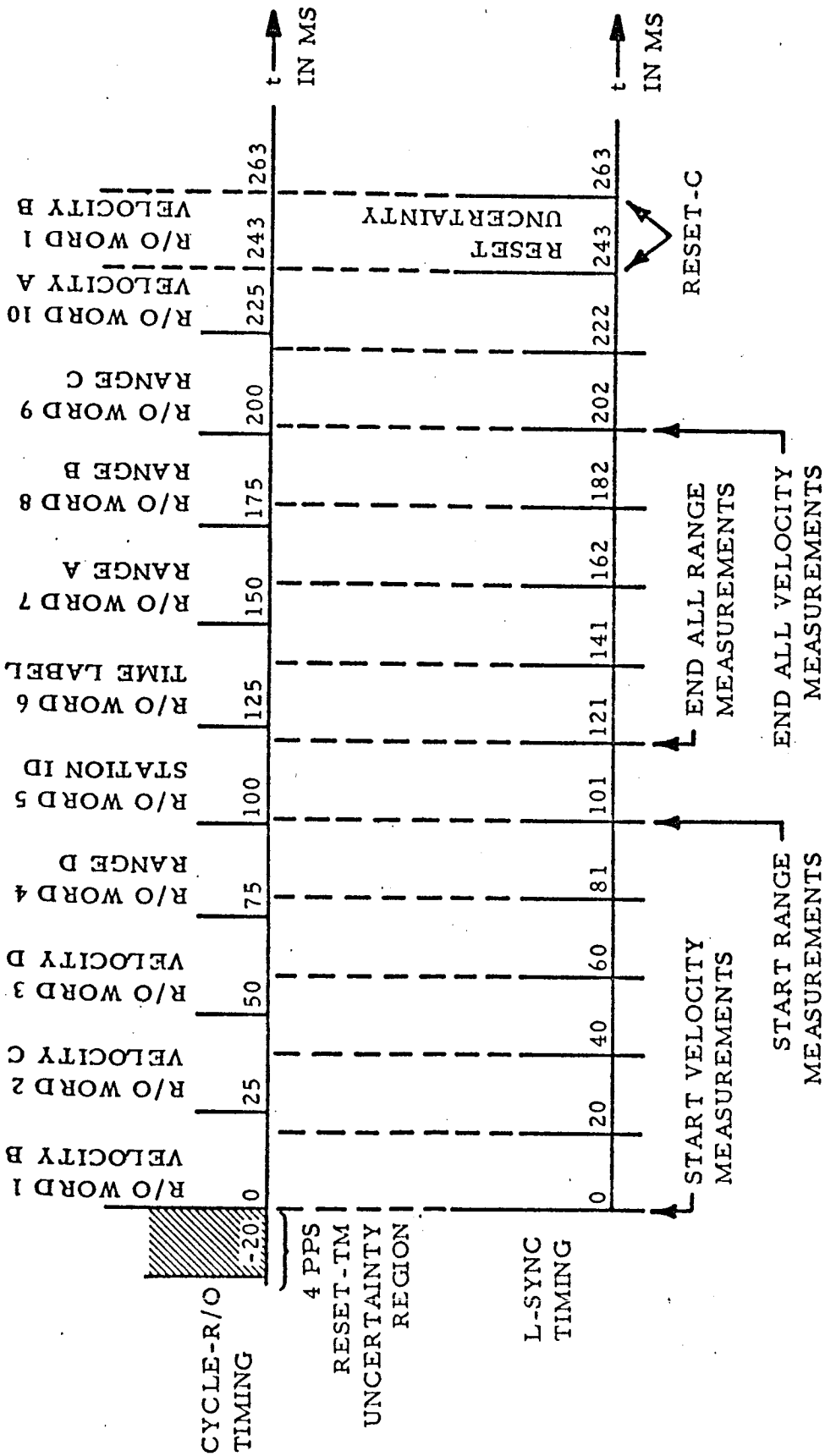
The preceding sequence of operations defines both the basic hardware requirements and the Data Block format; i.e., a

set of time related output data words. The site identification word marks the beginning of a Data Block. A timing diagram of the Data Readout cycle is presented in Figure 5-96. Referring to Figure 5-96, RESET-TM is the telemetry reset signal, L-SYNC marks the start of an L code sequence and CYCLE-RO is the word sequence command for the Data Readout Subsystem.

All input data is in parallel form and all stored data is read out serially. Such a processing scheme requires various timing signals for word identification and data transfer, as well as a system of gated clock pulses to control the serial data flow. The timing signals are internally derived from the RESET-C and CYCLE-RO signals. The timing signals are used in conjunction with the basic 100 KHz clock to generate the required gated clock signals. These functions are performed by the Timing and Clock Pulse Generators. Several other supplemental functions are performed, but these are best discussed in the logic description in Section 5.7.2.2.

At this point, the functional elements that are required have been derived. The final logic design constraints are defined by establishing given word formats for the various data words. The final Data Block format is shown in Figure 5-97. Several points should be made about Figure 5-97. These are:

1. Bits 25-28 are the word identification code.
2. Bit 0 of each velocity word contains the transponder H code lock status information as decoded by the system control logic.
3. The vhf control code is the three bit control message that is being transmitted to the respective transponder via the vhf link at the time



NOTE: CASE SHOWN IS FOR RESET-TM AVAILABLE.
 WITH NO RESET-TM, RESET-C WILL OCCUR
 EVERY 13 L-SYNC PULSES WITH NO UNCERTAINTY

Figure 5-96. Timing Diagram for Data Readout Cycle

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
---	---	---	---	---	---	---	---	---	---	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----

WORD 5 STATION I. D. DATA	1	CHAN A	CHAN B	CHAN C	CHAN D	0	1	0	0	0
---------------------------------	---	--------	--------	--------	--------	---	---	---	---	---

WORD 6 TIME LABEL	M S B	25 BITS														L S B	0	1	0	1	0
-------------------------	-------------	---------	--	--	--	--	--	--	--	--	--	--	--	--	--	-------------	---	---	---	---	---

WORD 7 CH A RANGE DATA	M S B	18 BITS (COARSE)										L S B	M S B	6 BITS (FINE)	L S B	0	1	1	0
---------------------------------	-------------	------------------	--	--	--	--	--	--	--	--	--	-------------	-------------	------------------	-------------	---	---	---	---

WORD 8 CH B RANGE DATA	M S B	18 BITS (COARSE)										L S B	M S B	6 BITS (FINE)	L S B	0	1	1	1
---------------------------------	-------------	------------------	--	--	--	--	--	--	--	--	--	-------------	-------------	------------------	-------------	---	---	---	---

WORD 9 CH C RANGE DATA	M S B	18 BITS (COARSE)										L S B	M S B	6 BITS (FINE)	L S B	1	0	0	0
---------------------------------	-------------	------------------	--	--	--	--	--	--	--	--	--	-------------	-------------	------------------	-------------	---	---	---	---

WORD 10 CH A VELOCITY DATA	VHF CONT CODE	M S B	21 BITS														L S B	1	0	0	1
-------------------------------------	---------------------	-------------	---------	--	--	--	--	--	--	--	--	--	--	--	--	--	-------------	---	---	---	---

WORD 1 CH B VELOCITY DATA	VHF CONT CODE	M S B	21 BITS														L S B	0	0	0	0
------------------------------------	---------------------	-------------	---------	--	--	--	--	--	--	--	--	--	--	--	--	--	-------------	---	---	---	---

WORD 2 CH C VELOCITY DATA	VHF CONT CODE	M S B	21 BITS														L S B	0	0	0	1
------------------------------------	---------------------	-------------	---------	--	--	--	--	--	--	--	--	--	--	--	--	--	-------------	---	---	---	---

WORD 3 CH D VELOCITY DATA	VHF CONT CODE	M S B	21 BITS														L S B	0	0	1	0
------------------------------------	---------------------	-------------	---------	--	--	--	--	--	--	--	--	--	--	--	--	--	-------------	---	---	---	---

WORD 4 CH D RANGE DATA	M S B	18 BITS (COARSE)										L S B	M S B	6 BITS (FINE)	L S B	0	0	1	1
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Figure 5-97. Word Order and Format

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that the word is formed and stored.

4. Bit 29 of the range and velocity words contains the state V-4 status of the respective channel as stored at the beginning of the Word Block. Bit 0 of the range word contains the state V-4 status of the respective channel at the word readout time. The channel lock status may then be evaluated according to the following truth table:

Range Bit 0	Range Bit 29	Data Evaluation
0	0	channel not locked; status bits are inserted
0	1	channel in lock at word 5; status bits inserted; data are questionable
1	0	channel not locked at word 5; locked before range readout; status bits not inserted; data are questionable
1	1	channel in lock for the measured cycle; data are valid

A logic "one" in bit 29 of the velocity word marks that word as valid. If bit 29 is a logic "zero", the range status information will help determine the usefulness of the data, if any.

5. The status bits referred to are the various acquisition status information inputs as supplied by the Receiver Code Control. These are substituted for the six least significant bits of range data if the respective channel is not in state V-4 at the beginning of a Data Block. The bit assignments are:

state $\overline{V-0}$ in bit 19, state $\overline{V-1}$ in bit 20, state $\overline{V-2}$ in bit 21, state $\overline{V-3}$ in bit 22, $\overline{A_L}$ in bit 23 and $\overline{A_H}$ in bit 24, the latter two being indicators on low and high speed code acquisition status. The data for the respective channel may then be evaluated, based upon the acquisition status.

This approach to the implementation of the Data Readout Subsystem is technically sound. The unit adequately interfaces with the telemetry system and the data sources. The data is presented to telemetry for a maximum percentage of the total allotted time. This is done with a minimum of hardware and with no critical timing relationships in the data flow sequence.

5.7.2.2 Logic Description

In this section the logic design of the Data Readout Subsystem will be discussed. Refer to Figure 5-95 for a basic block diagram of the unit. The design will be discussed on a general functional basis, with "X" subscripts being used to indicate general signal title subscripts.

Timing And Clock Pulse Generators

The Timing Command Generator has the function of generating ten timing pulses, T_X , and their complements, $\overline{T_X}$. These pulses correspond directly to the word interval periods and are used in the control of the data flow. The Timing Command Generator is basically a ten stage shift register.

The RESET-C signal clears the register and enables a logic "one" control bit to be clocked into the first stage. Each CYCLE-RO pulse, the word sequencing command, enables one clock pulse to activate the register and shift the control bit to the next stage. Since the steering input to the first stage is maintained at a logic "zero" level, only one stage at a time will contain a logic "one". The tenth stage is transferred into a separate flip-flop, which maintains T_{10} and $\overline{T_{10}}$ until the next RESET-C pulse occurs. The true and false outputs of each register are buffered to provide the required fanout for the timing signals.

The clock pulse generator has the function of generating the gated clocks that are used in the internal flow of data from the various Stores to the Output Register. The basic clock is the 100 KHz signal as supplied by the Vehicle Timing Unit. Twenty-five data bits are processed serially; therefore, this clock is converted into a series of 25 clock pulse bursts that start within 15 μ sec. of the beginning of each T_x period. The occurrence of either a RESET-C or a CYCLE-RO pulse causes the clock inhibit signal, DATA STATUS, to go to a logic "zero" level, thereby enabling the basic clock frequency to occur on the C_L signal line. The clock transitions are counted in a five stage ripple counter. The twenty-fifth count is detected and DATA STATUS is forced to the logic "one" or inhibit level. The resultant gated clock, C_L , is normally at the logic "one" level when inhibited, a condition that is imposed by the data loading procedures in

in the preliminary storage registers. A second phase of C_L is generated by activating a 2 μ sec. monostable circuit with C_L . The output of the monostable is inverted and buffered, resulting in the signal, C_G , a delayed gated clock. The timing of T_X , C_G , and C_L is shown in Figure 5-98.

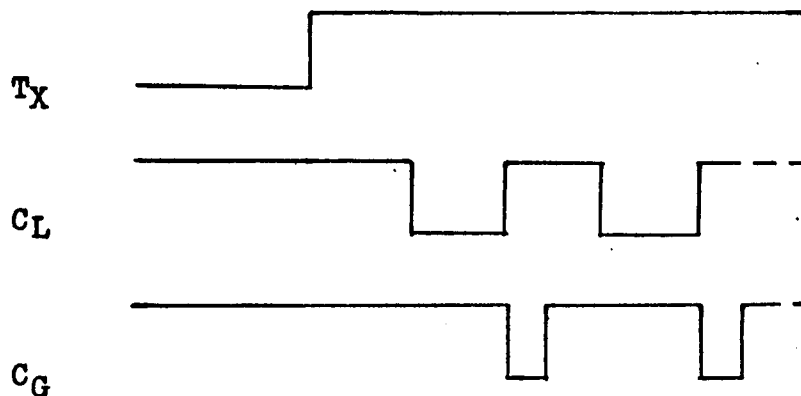


Figure 5-98.

Timing Diagram for the Generation of the Gated Clock Signals

The basic gated clock signals, C_G and C_L are then combined with the timing pulses to produce clocks for the Output Register and the four preliminary storage registers. The Output Register clock, C_S , is logically expressed as:

$$C_S = C_L (T_1 + T_2 + T_3 + T_4 + T_5 + T_6 + T_7 + T_8 + T_9).$$

The Store #1 clock, C_{S1} , is logically expressed as:

$$C_{S1} = C_G (T_1 + T_5 + T_6).$$

The Store #2 clock, C_{S2} , is logically expressed as:

$$C_{S2} = C_G (T_2)$$

The Store #3 clock, C_{S3} , is logically expressed as:

$$C_{S3} = C_G (T_3)$$

The Store #4 clock, C_{S4} , is logically expressed as:

$$C_{S4} = C_G (T_4 + T_7 + T_8 + T_9)$$

The control of the maximum range data flow is an auxiliary function that is performed in the Timing and Clock Pulse Generators. In the previously mentioned 5 stage counter, the nineteenth and twenty-fourth counts are also detected. An enable signal, INHIBIT C_{SMR} , is generated that is at a logic "zero" level between these two counts. The sign bits of the four velocity words, VSX, are stored at word time, T_{10} . The phasing of the velocity sign data is such that a logic "zero" indicates negative doppler. The System Control Logic is then provided with the clock, C_G , and an inhibit signal, $CHAN X MRD = T_X (\overline{VSX})(\overline{INHIBIT C_{SMR}})$. These signals are then used by the System Control Logic to extract the maximum range data from the serial input data to the output register, whose complement, $\overline{D_S}$, is also provided to the control logic.

Output Register

The Output Register is a 25 stage shift register with capabilities for parallel or serial loading. Inputs to the Output Register include the complemented velocity A word bits and the 4 preliminary storage register outputs. At time T_{10} , the velocity A word is loaded in parallel into the register. A straight forward two gate scheme which incorporates the d-c set and reset inputs of the flip-flops is used. This allows

the loading of both "ones" and "zeros" without a presetting operation. Words T_1 through T_9 are loaded into the Output Register serially from the preliminary storage registers. The serial input data may be expressed logically as:

$$D_S = (T_1 + T_5 + T_6) S_1 + S_2 (T_2) + S_3 (T_3) + S_4 (T_4 + T_7 + T_8 + T_9),$$

where S_1 , S_3 and S_4 represent the four storage register outputs.

The remaining five bits of the output word are formed in a logic gating array. The T_x signals are gated to form the complement of the binary word identification code. The logic expressions for bits 25-28 of the data word are:

$$\text{Bit 28} = (T_2 + T_4 + T_6 + T_8 + T_{10})$$

$$\text{Bit 27} = (T_3 + T_4 + T_7 + T_8)$$

$$\text{Bit 26} = (T_5 + T_6 + T_7 + T_8)$$

$$\text{Bit 25} = (T_9 + T_{10})$$

Bit 29 is formed by gating the stored state V-4 data with the timing signals to form the complement of the expression.

$$\begin{aligned} \text{Bit 29} = & (T_7 + T_{10})(V-4A) + (T_8 + T_1)(V-4B) + \\ & (T_9 + T_2)(V-4C) + T_3 + T_4)(V-4D). \end{aligned}$$

The complements of all 30 bits of data are then inverted in the output interface gates and provided to telemetry.

The output interface gates are standard Philco two input gates which are operated with a +5.6 vdc power source. The units are, when operated in this manner, capable of providing the required five volt output logic swing when loaded with the specified 10 kilohm impedance. The logic elements will still interface with normally operated logic elements. A small, highly compatible interface circuit is thereby obtained, which incorporates the use of the logic elements at a stress that is reasonably lower than the specified maximum of +8.0 vdc.

Store #1

Store #1 is a 25 stage, parallel loading, shift register that is used for preliminary storage of the velocity B word, the site identification word, and the time label word. The input data is presented in complement form, except for the gated time label inputs which are presented in their true state. The vehicle timing unit provides a STORE-TL command that is used to enable the time label data transfer. The velocity B word transfer command is $\overline{T_{10}}$. The site identification word data is enabled by a composite of T_4 and IN-SID-X, T_4 (IN-SID-X), where IN-SID-X is the inhibit signal that accompanies the site identification data for a given channel. A load register signal is generated to transfer the composite gated data into the register flip-flops. This may be described in general as:

$$S1-DT-X = (\text{STORE-TL}) + \overline{T_{10}} + T_4 (\text{IN-SID-X})$$

A separate set of control signals is required for each channel of site identification.

At the appropriate time the input clock C_{31} , activates the shift register and the data is transferred serially into the output register. The arrangement of the first stage causes the register to be loaded with "ones" as the data is removed from the register. A double gating scheme that loads both "ones" and "zeros" is used; however, since the time label count is incremented in the center of the transfer signal enable period and the stored data must be updated to account for this. The possibility of ambiguity during the transfer signal transitions, which are derived from the time label clock, is thereby eliminated.

Stores #2 and #3

Stores #2 and #3 are identical 24 stage shift registers. They are used for the storage of the velocity C and velocity D words. The parallel storage gating is very simple, incorporating only one gate and loading only logic "one" data bits. This is made possible by grounding the steering input to the first stage, which loads the register with "zeros" as the data word is transferred to the Output Register. Since no time sharing of the register is incorporated and the data is stable and unchanging, only "ones" need be transferred during the load cycle.

Store #4

Store #4 is a parallel load, 25 stage shift register. It is used as a parallel to serial converter for the four range words. The data for each channel is gated, using the

appropriate $\overline{T_X}$ signal as the enable signal. The four enabled outputs are then combined in an "or" gate and presented to the transfer and load gates. The load command is expressed as:

$$S_{4-DT} = (T_4 + T_7 + T_8 + T_9) (\overline{\text{LOAD RANGE}}),$$

where $\overline{\text{LOAD RANGE}}$ is a 100 ns pulse that is generated on the trailing edge of $\text{CYCLE-RO} + \text{RESET-C}$. Five microseconds after the data is loaded into the register, $C_S 4$ activates the register and transfers the data serially into the Output Register.

The state $V-4$ signal for each channel is used to control the status information for that channel. Should $V-4$ be at a logic "zero" level at the time of data transfer for the respective channel, the six least significant data bits are inhibited and the system acquisition status information is gated to the transfer and load gates as part of the range word. Bit 0 of the word is set at a logic "zero" to reference this action. The word format discussion of section 5.6.2.1 describes the use of the data under conditions other than the full lock mode.

5.7.2.3 Discrete Component Circuits

Only one significant circuit was designed with discrete components in the Data Readout Subsystem. This was the +5.6 VDC power source that is used by the output interface circuits. It is a simple zener diode power supply that

converts +10 VDC to +5.6 VDC. The circuit diagram is presented in Figure 5-99. The zener diode, CR1, is a 1 watt, 5.6 volt silicon diode used to establish the proper voltage level. R1, an 82 ohm, 1 watt Allen Bradley resistor, is used to limit the current to 55 ma. The capacitor, C1, is a 3.3 μ f, 20 volt tantalum capacitor that is used to filter the output voltage.

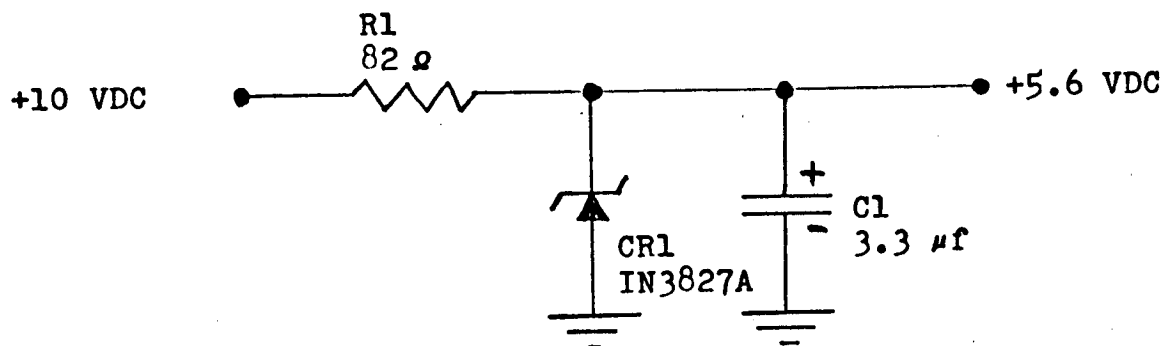


Figure 5-99

+5.6 VDC Power Source

Three other discrete components were used. These were used as timing components in integrated circuit monostable multivibrators, however, and are not of significance in this discussion.

5.7.2.4 Test Results

This section is intended to summarize the testing that was performed upon the Data Readout Subsystem and to evaluate its performance with respect to system requirements.

Each of the 23 I/C modules was subjected to pre-weld and post-pot testing. The purpose of these tests was to verify the logic design and to assure that all assembly documentation was in order. The next phase of testing was at the subgroup level.

At this point, using the Vehicle Timing Unit to synchronize the operations, the Timing and Clock Pulse Generators were tested as a unit. Each of the four storage units and the output register were then tested in conjunction with the timing and clocking functions. The primary purpose of this testing effort was to verify the operation of each subgroup. The logic interfaces were also verified as being correct at this level.

Several problems were noted at this point. Two bad Philco units were detected, one register or flip-flop and one three input gate. Both units were replaced. The two minor logic errors that are noted in the data were corrected and new modules were produced. The noise problem that was associated with the subgroup D testing was isolated to test fixture and grounding problems. It did not reoccur in later testing. The Data Readout output word connectors were shielded in the final and breadboard test harnesses as a precaution against large noise pickup from these leads.

The third and final phase of testing was the Data Measurements Subsystem hardware acceptance test. In this test the assembled frames of the Data Measurements Subsystem were connected with a breadboard test harness and actual operational conditions were simulated. The test included

environmental temperature extremes as a means of uncovering critical timing areas and as a final test of each of the four modules that underwent minor repair after the subsystem test effort -- i.e., subgroup tests on Data Readout were not specifically repeated after the module rework.

At the end of the Data Measurements test phase, it was concluded that the Data Readout Subsystem would very adequately meet the requirements of the AROD system. The unit met all functional requirements and provides signal outputs to other AROD subsystems that will meet the specifications for the Philco logic family. The telemetry interface outputs are on the low tolerance of the specified level but are adequate. The unit performed well over the entire specified temperature range with no marginal conditions in evidence. Power supply tolerances of $\pm 10\%$ in any combination will not degrade the subsystem performance. The total required current of 1515 ma at 3.5 VDC is within the preliminary estimated range and is below the specified limit. The required current of 55 ma at $\pm 10\%$ VDC is below the required limit. The timing and interface problems which did occur have been remedied, the unit has been thoroughly tested and the Data Readout Subsystem is completely adequate for the AROD system application.

5.7.3 Velocity Extraction Unit

The Vehicle Velocity Extraction Unit is required to provide a capability of measuring velocities ranging from -12,000 m/sec to +12,000 m/sec with a resolution of approximately 0.02 m/sec.

The Velocity Extraction Unit obtains the velocity information by counting a clock frequency containing the Doppler information for a fixed period of time. The velocity timing interval is obtained by counting ten L-code periods or 202.803125 milliseconds. The clock which is counted by the velocity extraction unit is obtained by removing the Doppler frequency from the transponder to vehicle S-band frequency, multiplying it by 8, and frequency deviating a bias frequency of 3.2 MHz.

The 3.2 MHz bias frequency is used to obtain Doppler sign information. Prior to the counting period, the 20 bit counter will be preset to a binary count equivalent to 923,894. Since the accumulated count resulting from the 3.2 MHz offset frequency is 648,970 in the counting interval, the final count will be 1,572,864 if the Doppler frequency is zero. The counter will overflow at a count equivalent to 1,048,576 leaving a count of 524,288 which corresponds to a binary number of 100 000 000 000 000 000 00. From this it can be seen that if the Doppler is positive the 20 bit will be a one and the remaining 19 bits represent the velocity, and if

the Doppler is negative the 20 bit will be a zero and the remaining 19 bits represent the binary 2's complement of the velocity data.

Multiplication of the contents of the velocity counter by two at the end of the counting interval is accomplished by a shift of each stage of the counter to the right (or labeling the outputs of the counter; i.e., the first bit is labeled 2 and the last bit labeled 21). The value of the least significant bit is determined from the polarity of the shaped input signal. If this signal is a ONE (corresponding to an input signal phase between 0° and 180° at the end of the counting interval), a ZERO is inserted into the bit 1 register. Conversely, if this signal is a ZERO (indicating the input signal phase between 180° and 360°), a ONE is inserted into this register. The complement of the velocity data is presented to the Data Readout Subsystem.

The resolution is a function of the transponder transmitter frequency and will also vary as a function of the velocity. Four identical velocity extraction channels are used in the Vehicle Velocity Extraction Unit.

The Velocity Extraction Unit is part of the Data Measurements Subgroup and is packaged with data measurements modules in four frames.

5.7.3.1 Logic Description

Figure 5-100 is the block diagram of channels A and B of the Vehicle Velocity Extraction Unit. Each channel of the velocity extractor has an identical Velocity Extract Module 1 (Figure 5-101) which contains the first 13 bits for that channel. Channels A and B share a common Velocity Extract Module 2 (Figure 5-102) which contains the last eight bits for these two velocity channels. Channels C and D are packaged in the same manner. The entire velocity extraction unit is contained in six (6) digital modules.

Due to the inability to preset the Philco PL984 flip-flop to either state, three timing signals were needed for the preset function. These three signals, which are generated in the Vehicle Timing Unit are RESET C, SET VEL and RESET VEL. The timing of these signals is shown in Figure 5-103.

RESET C is used to inhibit the gates in the feedback path of bits 4, 6, 13 and 19. The RESET VEL pulse is inverted by D1 and resets all the counter stages to a "1" level. The SET VEL pulse is used to reset counter stages 2, 5, 10 and 15. The SET VEL pulse will cause the "0" level reset to propagate through the counter until it reaches a stage in which the feedback path has been inhibited by the RESET C pulse. This will preset the counter to a 111 000 011 000 111 101 01 and the start of the VEL TIMING INTERVAL with add one count resulting in a 111 000 011 000 111 101 10 in the counter which is the correct preset number.

The velocity input signal is shaped by the hybrid amplifier ST1 and is combined in gate G1 with the velocity timing interval to form the velocity counter clock. Flip-flop FF1 records the phase of VEL INPUT at the start of velocity timing interval.

5.7.3.2 Test Results

Test results show that the velocity extraction unit will perform to its specifications under its expected environmental conditions.

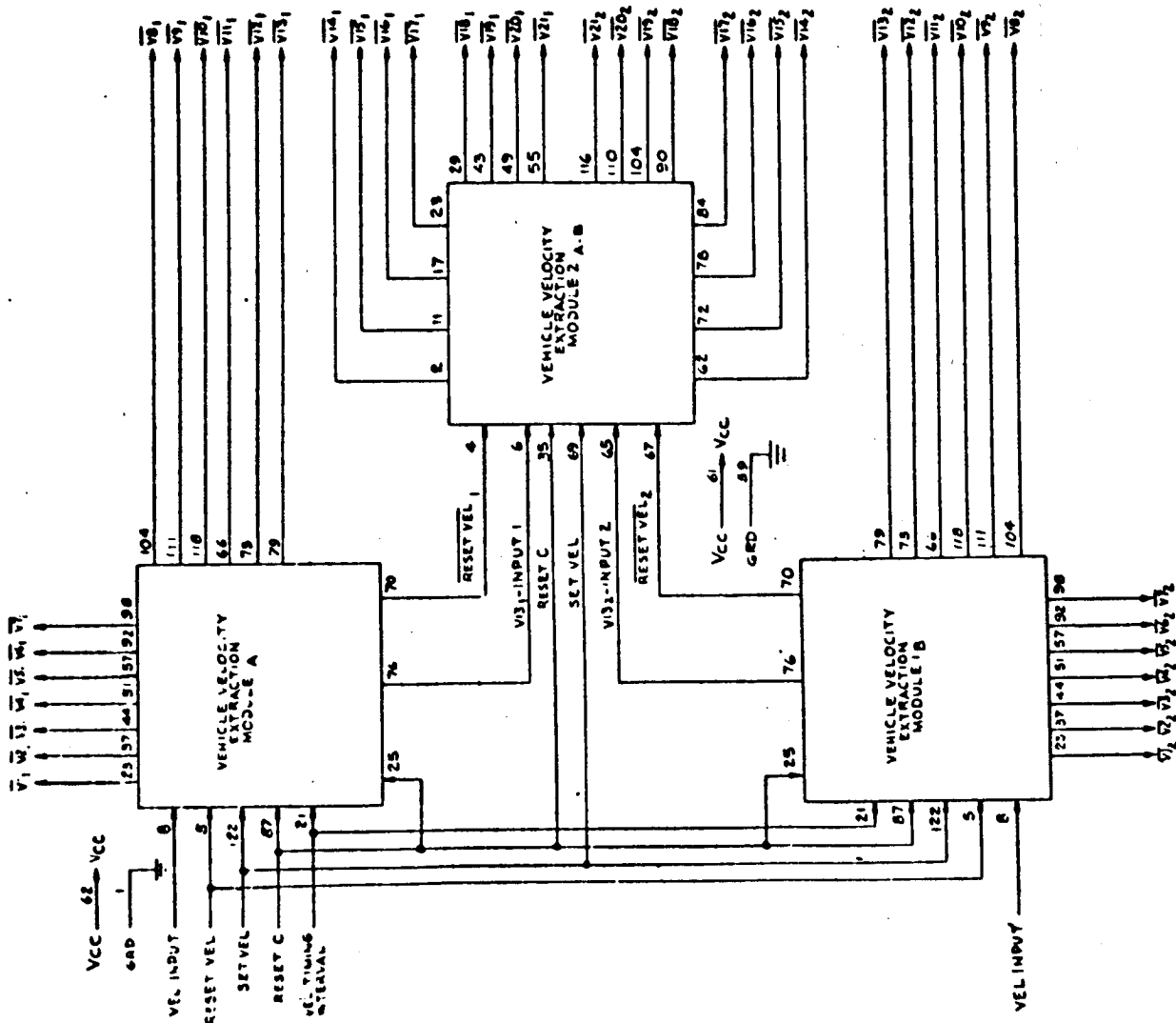
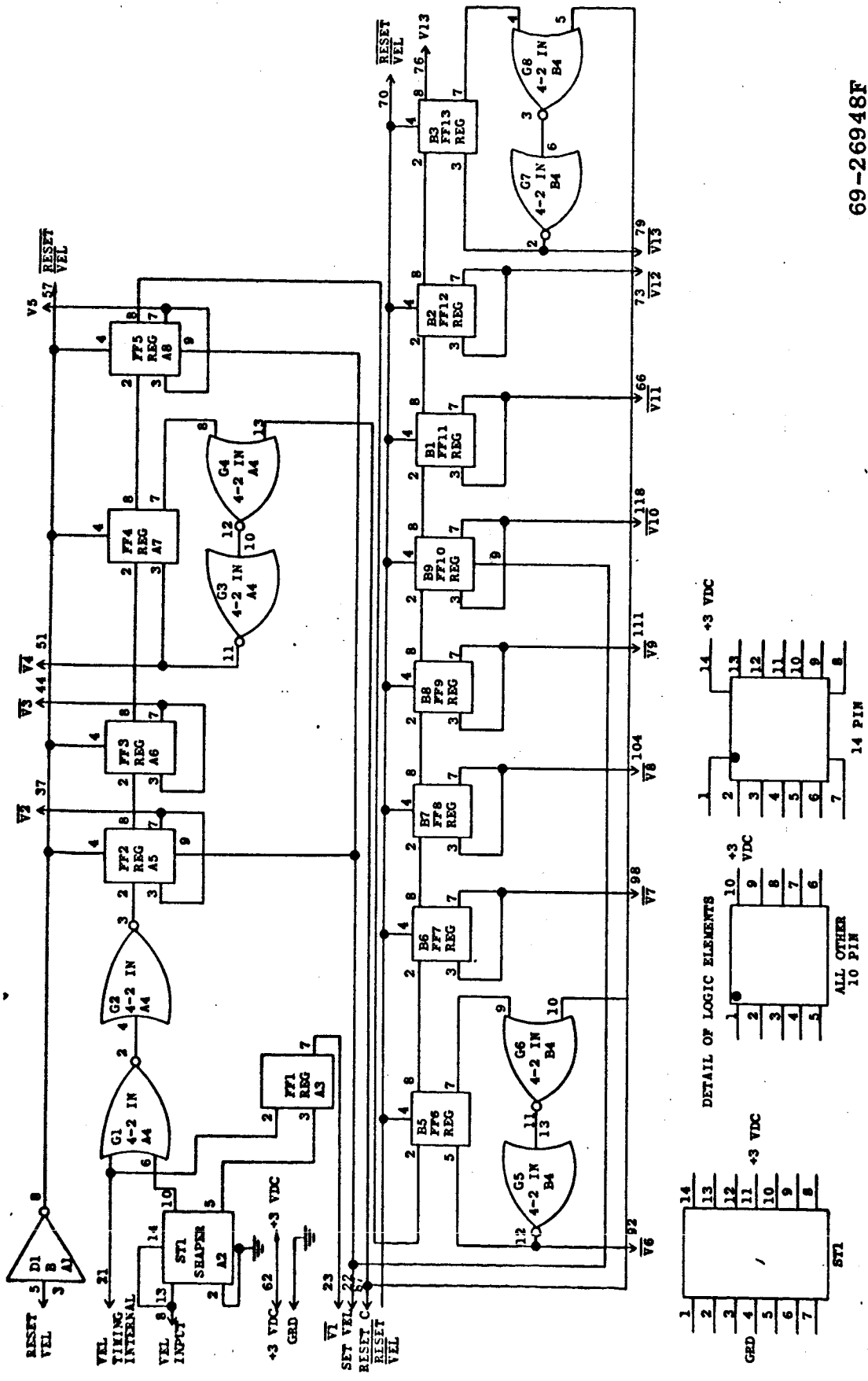


Figure 5-100. Velocity Extraction Unit, Block Diagram



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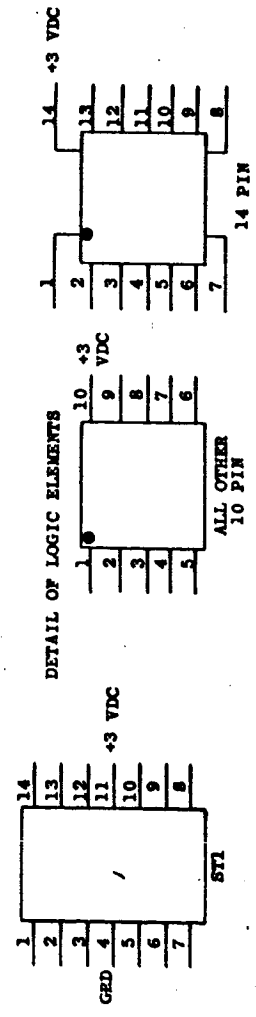


Figure 5-101. Vehicle Velocity Extraction Module 1, Logic Diagram

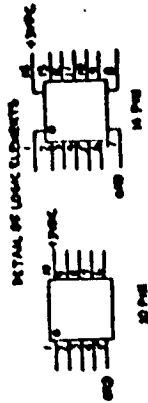
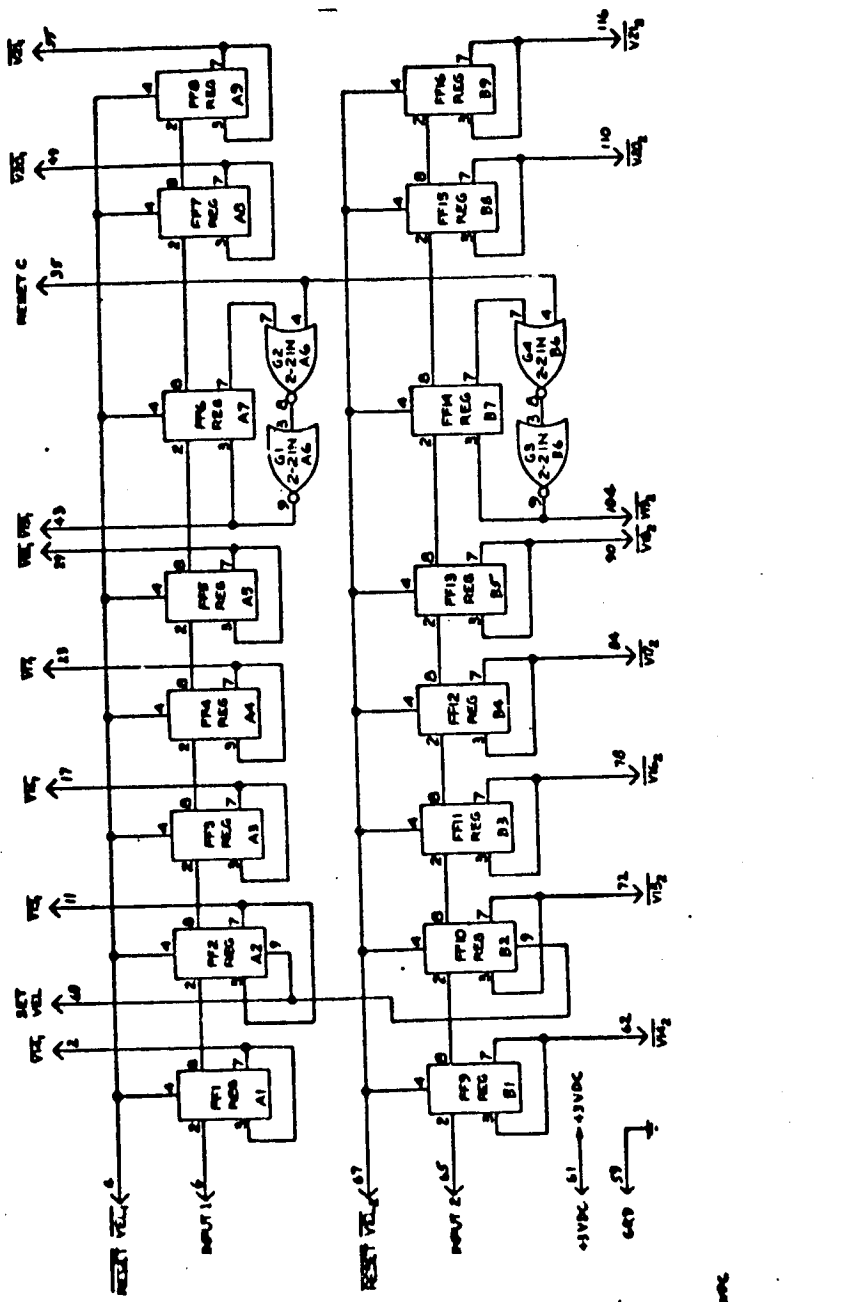


Figure 5-102. Vehicle Velocity Extraction, Module 2

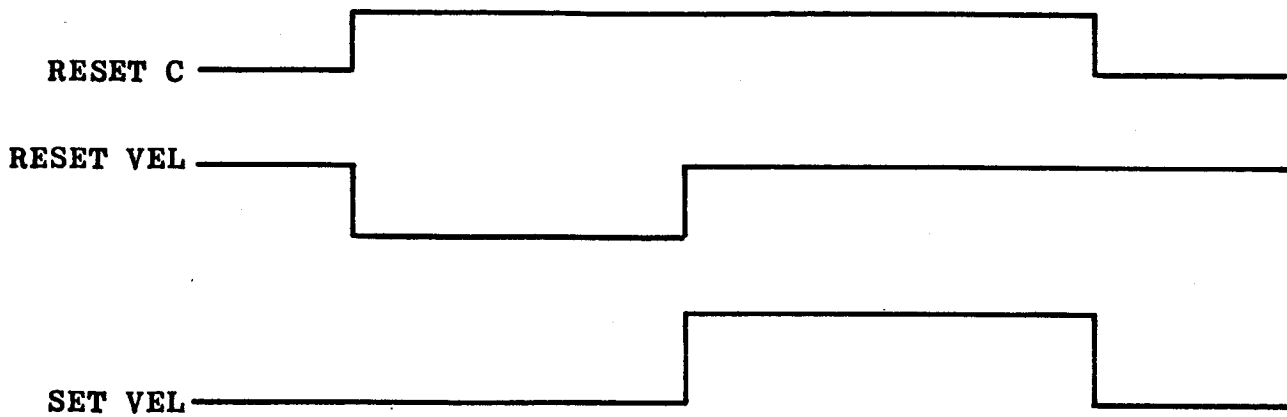


Figure 5-103. Timing Signals

Some simplification in the velocity counter and input signals could be made if a binary element which could be preset to either a "1" or "0" level were used. In the present packaging scheme, however, this would not result in any reduced size and would not improve the operation of the counter itself.

The velocity extraction unit will operate with supply voltages between 2.7 vdc and 4.0 vdc and velocity input signals as low as 82 mv rms. Current drain at nominal supply voltage is 220 ma.

5.7.4 RANGE EXTRACTION UNIT

The Range Extraction Unit measures range by determining the time delay between the transmitted signal and the received signal. A PN code sequence is generated in the vehicle and is used to modulate the transmitted carrier signal and also to demodulate the received signal using correlation techniques. The time delay measured is that delay between a unique point in the transmitted code sequence and the same point in the received code sequence. The unique point in both codes is the negative transition of the last bit in the L Code Sequence (L_{127}).

Each receiver channel contains an identical set of four modules which measures the time delay in that particular channel. In addition, the Range Extraction Unit contains two modules which are shared by all four channels. The Range Extraction Unit consists of 18 modules, 17 digital I/C modules and one RF cordwood module. These 18 modules contain 191 integrated circuits, 29 hybrid circuits, and 130 discrete components. The Range Extraction Unit is packaged in the Data Measurement sub-group which is shown in Figure 5-88.

The total range readout, a combination of coarse and fine range count, is presented in compliment form as a 24-bit binary number to the Data Readout subsystem. The Range Extraction

Unit has a resolution of 0.183 meters/bit and a total capacity greater than 3,072 kilometers. Since the modulation code provides an ambiguity resolution of 3,042 kilometers, its full range can be accommodated by the range register.

5.7.4.1 TECHNICAL APPROACH

Figure 5-104 is a functional logic diagram of the modulation generator for the transmitter and one receiver channel, along with the coarse and fine range time interval counters.

During one of the L_{127} pulses from the transmitter coder, a START RANGE MEASUREMENT pulse is provided by the Vehicle Timing Unit. This pulse enables the proper L_{127} to start the coarse range measurement interval. This L_{127} pulse is denoted by RESET (T). The next received L_{127} , denoted by RESET (R-i), is used to stop the coarse range measurement interval. Since the receiver modulation generator is tracking the received modulation, the time interval between RESET (T) and RESET (R-i) is a measure of the phase difference between the transmitted range modulation and the range modulation receiver on channel i. The coarse range measurement is made by counting the integral number of zero crossings of $f_H(t)$ which occur between the transmitter range marker, RESET (T), and the receiver range marker, RESET (R-i).

The coarse range interval has a resolution of one cycle of the code clock. Further resolution is obtained by comparing the phase of the transmitter clock $f_H(t)$ and the

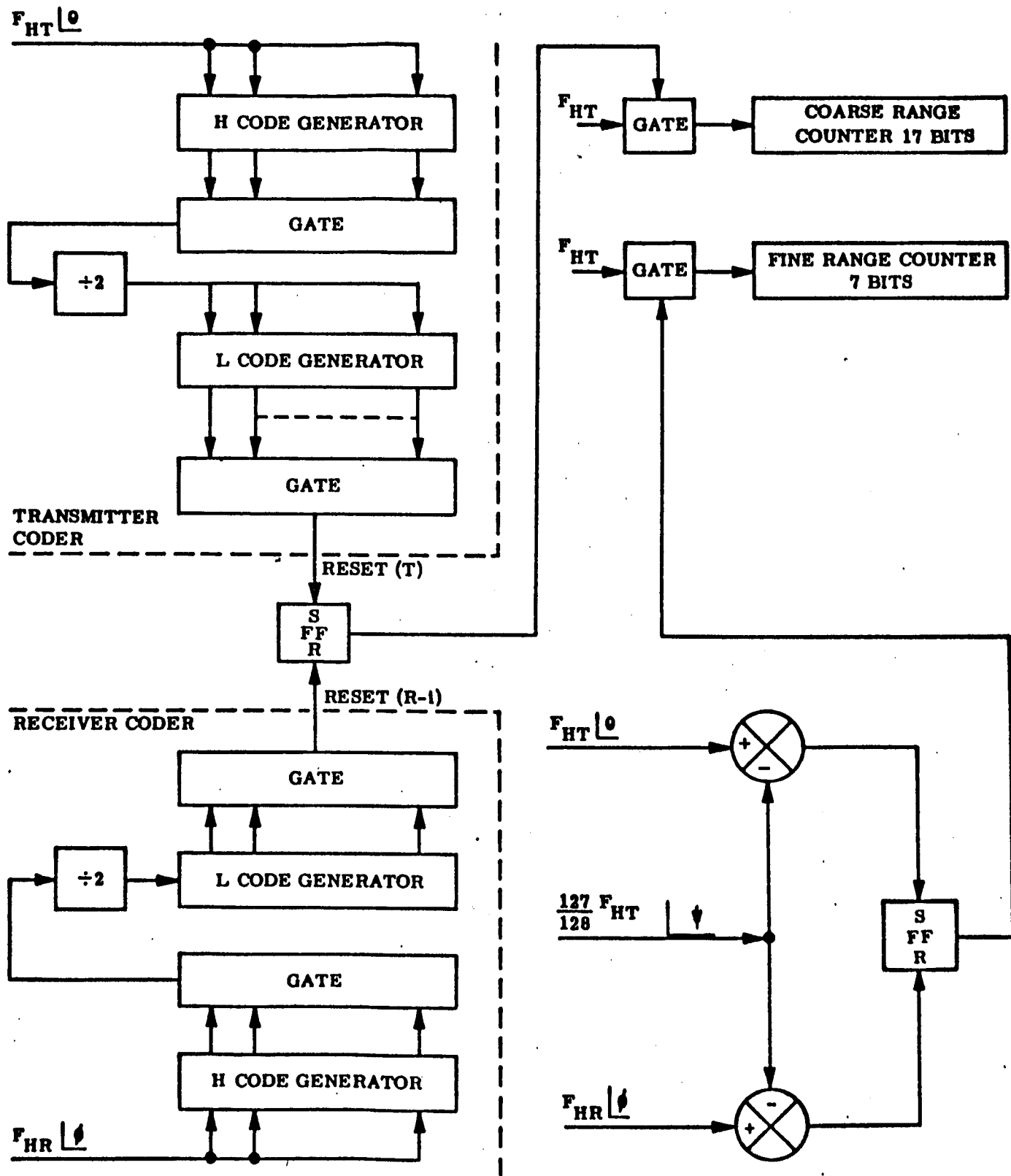


Figure 5-104. Functional Block Diagram of the Range Extraction Unit

receiver clock $f_H(R-i)$. This fine range measurement is refined to the desired accuracy by quantizing one period of $f_H(t)$ into 128 intervals. This is accomplished by mixing the transmitter and receiver clock signals with a common signal of 6.35 MHz or approximately $127/128$ of $f_H(t)$, and then employing the original clock signal as the quantization signal. This, in effect, translates the phase of the $f_H(t)$ and $f_H(R-i)$ to a frequency of $1/128 f_H(t)$. This translation extends the time delay between $f_H(R-i)$ and $f_H(t)$ to 128 times the value at $f_H(t)$. The zero crossing of the mixed $f_H(t)$ is used to start the fine range counter and the zero crossing of $f_H(R-i)$ is used to stop the counter. The fine range counter is a 7-bit counter and counts $f_H(t)$, thereby providing a maximum count of 128 for 360° of phase difference between $f_H(t)$ and $f_H(R-i)$.

An ambiguity exists between the coarse and fine range counters due to the ± 1 bit accuracy of the coarse range counter. This ± 1 bit count error is caused by the asynchronous received L_{127} , which is used to stop the coarse range clock. A second factor is the finite and variable set up and release time of the counting element. Resolving this ambiguity requires an overlap of coarse and fine range counters.

The technique used in the AROD Range Extraction Unit overlaps the coarse and fine range counters by one bit and using the overlap bit information to correct, if necessary, the count in the coarse range counter. The overlap is imple-

mented by dividing $VT-2F_H$ (12.8 MHz) by two to form the coarse range clock (6.4 MHz). This divide-by-two element then becomes a 1/2 cycle counter with respect to the coarse range counter.

Figure 5-105 shows the timing of the $VT-2F_H$ signal and the coarse range clock which is the output of the 1/2 cycle counter (Q1). Since the contents of the fine range counter contain a number representing the portion of the coarse range clock at which the actual range measurement should have ended. For purpose of explanation, assume the full cycle of the coarse range clock divided into six time segments over the two full cycles of $VT-2F_H$ which form the coarse range clock. The fine range counter contents for each of the six segments is given in Table 5-10 where the full counter contents are represented by 1.0.

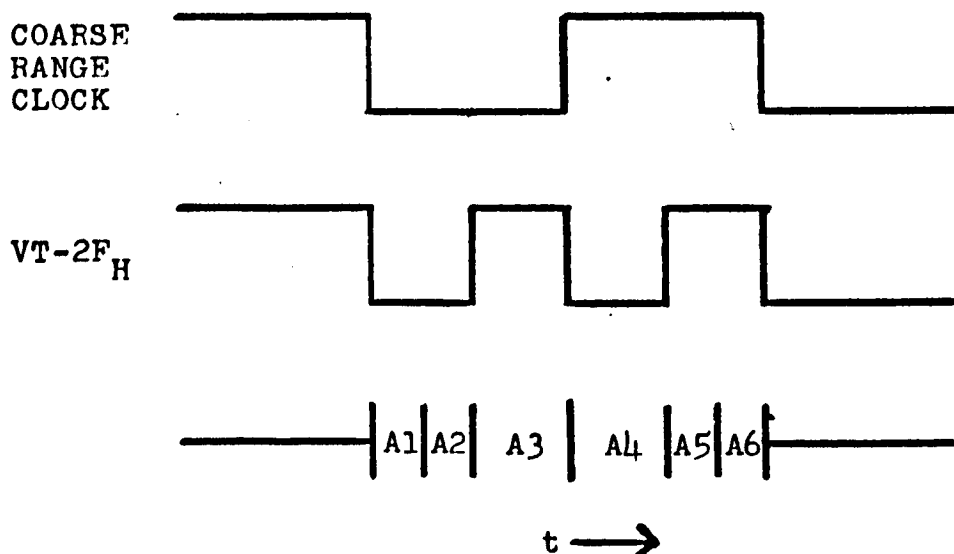


Figure 5-105. $VT-2F_H$ Signal Timing

Table 5-10. Fine Range Counter Output

Time	Fine Range Counter					
	Decimal			Binary		
A1	0	FR	.1250	0000000	FR	0001000
A2	.1250	FR	.2500	0001001	FR	0010000
A3	.2500	FR	.5000	0010001	FR	0100000
A4	.5000	FR	.7500	0100001	FR	0110000
A5	.7500	FR	.8750	0110001	FR	0111000
A6	.8750	FR	.9999	0111001	FR	1111111

Assuming the coarse range counter will toggle on the negative transitions of the coarse range clock, Table 5-11 shows how the output conditions of Q1 and fine range counter can be combined to correct the coarse range count.

Table 5-11. Q1 Output

Fine Range Counter	Q1	Result
A1	1	Missed 1 count
A1	0	Correct
A2	1	Error
A2	0	Correct

TABLE 5-11 (cont'd)

Fine Range Counter	Q1	Result
A3	1	Correct
A3	0	Correct
A4	1	Correct
A4	0	Correct
A5	1	Correct
A5	0	Error
A6	1	Correct
A6	0	Added 1 count

The conditions for which an error is noted can never occur with the constraints that are placed upon the timing of the various input signals. These constraints which were used to obtain the six time segments of fine range counter are listed below:

- (1) $VT-2F_H$ and $VR-2F_H$ have the same phase relationship to $VT-F_{HS}$ and $VR-F_{HS}$ respectively within ± 10 degrees.
- (2) Start and stop pulses for the coarse range measurement have the same relationship to $VT-2F_H$ and $VR-2F_H$ respectively within ± 8 nanoseconds.
- (3) Maximum setup and release times of input binary counter to the coarse range register are 30 nsec

and 0 nsec, respectively.

The first condition is accomplished in the Transmitter and Vehicle Code Control Units by retiming the $VT-F_H$ and $VR-F_H$ with $VT-2F_H$ and $VR-2F_H$ in high speed flip-flops to form $VT-F_{HS}$ and $VR-F_{HS}$.

The timing of the start and stop signals for the coarse range counter is done in module 1 of each range channel. This is done by defining the start as the first negative transition of $VT-2F_H$ after $VT-L_{127}$ goes to a "0" level and defining the stop as the first negative transition of $VR-2F_H$ after $VR-L_{127}$ goes to a "0" level. A start and stop pulse can then be formed which will have the propagation delay of only one logic element. This propagation can be matched within ± 8 nanoseconds. The third condition is a manufacturer's specification for the flip-flop used as the first stage of the coarse range counter.

Ambiguity correction is accomplished by comparing the conditions as given in Table 5-11 and making a correction when necessary. The coarse range counter is preset to all "1" levels such that it starts one count low. A "missed 1 count" results in two counts added to the coarse register while "correct" results will add one count and "added 1 count" results will add no counts to the register.

The fine range time interval is obtained by mixing $VT-F_{HS}$ (6.4 MHz) and a crystal controlled 6.35 MHz oscillator to produce a 50 KHz reference signal. This signal is used to

start fine range counter. VR-F_HS (6.4 MHz) is mixed with the same 6.35 MHz oscillator to produce a 50 KHz signal used to stop the fine range counter. The fine range counter uses VT-F_H (6.4 MHz) as the clock frequency.

The total range extraction cycle is completed in three steps. The coarse range interval is between the negative transitions of the first transmitted and received L₁₂₇ pulses after the START RANGE MEASUREMENT pulse has occurred. The received L₁₂₇ pulse also produces a pulse which starts the fine range interval on the first negative transition of the 50 KHz reference signal. The fine range interval is ended by the first negative transition of the 50 KHz from the received channel mixer after the start has occurred. Ambiguity corrections are started 20 microseconds after the end of the fine range interval and last for a maximum of 30 microseconds.

5.7.4.2 LOGIC DESCRIPTION

Figure 5-106 shows the Range Extraction Unit Block Diagram. Each of the four range channels contain an identical set of four modules. The module titles are listed below.

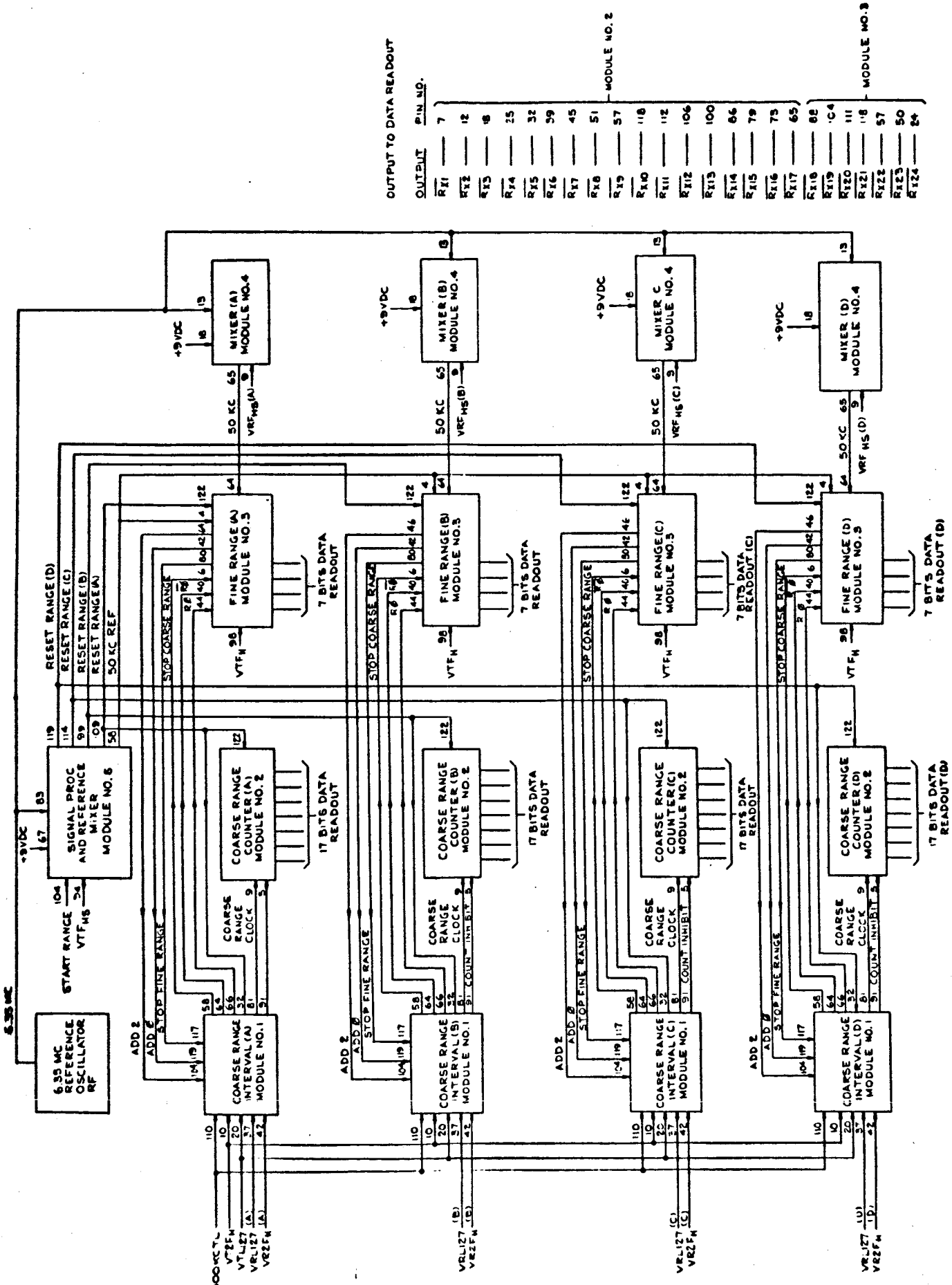


Figure 5-106. Range Extraction Unit, Block Diagram

<u>Module Number</u>	<u>Title</u>
1	Coarse Range Interval
2	Coarse Range Register
3	Fine Range Interval
4	Range Channel Mixer
5	Signal Processor & Reference Mixer
6	6.35 MHz Oscillator

Two modules, the Signal Processor & Reference Mixer and the 6.35 MHz Oscillator, are common to all four range channels.

Extraction of the range data is completed in three steps. The coarse range data is obtained first. The START RANGE MEASUREMENT pulse is provided by the Vehicle Timing Unit during the transmitted VT-L₁₂₇ pulse that starts the coarse range interval. The START RANGE MEASUREMENT pulse is buffered in the Signal Processor and Reference Mixer module and distributed to each of the range channels as the RESET RANGE pulse. The pulse is used to reset both the coarse and fine registers and to enable the coarse range interval. The coarse range interval will then start on the first negative transition of VT-L₁₂₇. This negative transition of VT-L₁₂₇ sets a flip-flop which gates VT-2F_H (12.8 MHz) to form the clock for the 1/2 bit counter of the coarse range

register. The RESET RANGE pulse and the start of the coarse range interval enable flip-flops which allow the next negative transition of VR-L₁₂₇ to stop the coarse range interval. VR-L₁₂₇ gates VR-2F_H to produce the STOP COARSE RANGE pulse. This pulse resets the coarse range interval flip-flop ending the coarse range interval.

The output of the 1/2 bit counter and the count addition circuitry for ambiguity correction are connected in an "OR" gate to form the coarse range clock. The count addition circuitry is inhibited until after the fine range interval so the output to the 17 bit coarse range register is VT-2F_H/2 during the coarse range interval.

The Coarse Range Register module contains a standard 17-bit binary divider. This register is preset to all "1" levels by the RESET RANGE pulse. This starts the coarse range register one count short allowing the ambiguity correction to be made. The output of the coarse range register is presented in compliment form to the Data Readout subsystem.

The STOP COARSE RANGE pulse is used to enable the fine range interval. The fine range interval begins on the first negative transition of the 50 KHz Reference signal after the STOP COARSE RANGE pulse. The 50 KHz Reference signal is obtained from the Signal Processor and Reference Mixer module. The clock for the vehicle coder VT-F_{HS}

(6.4 MHz) is mixed with a 6.35 MHz signal to form the 50 KHz Reference signal. A 50 KHz signal is obtained for each of the range channels by mixing the clock from the received code VR-F_{HS} (6.4 MHz) and the same 6.35 MHz signal. This 50 KHz signal is used to end the fine range interval. The fine range interval flip-flop, set by the 50 KHz Reference and reset by the 50 KHz signal, gates the fine range clock, VT-F_H.

The fine range register is a standard 7-bit binary counter. This register is preset to all "1" levels by the RESET RANGE pulse. The start of the fine range interval produces an extra count which presets this register to all "0" levels.

The output of the fine range register and the outputs of the 1/2 bit counter, R0 and $\overline{R0}$, are compared and generate either an ADD 2 COUNTS command or an ADD 0 COUNTS command. An ADD 2 COUNTS signal gates two 100 KHz pulses into the COARSE CLOCK line, adding 2 counts to coarse range register. An ADD 0 COUNTS signal causes no pulses to be added, while absence of both the commands will cause one 100 KHz pulse to be added to the coarse range register. These additional counts are added to the coarse range register after the STOP FINE RANGE pulse has occurred. This pulse is produced by the first negative transition of the 50 KHz signal after the fine range interval has ended.

5.7.4.3 DISCRETE COMPONENT CIRCUITS

Discrete components were used in conjunction with hybrid integrated differential amplifiers to perform the mixing function for the reference mixer and each of the range channel mixers (01-26157G, 69-26152G). Each mixer utilizes three hybrid differential amplifiers (A38). The first hybrid is used as a down mixer for the 6.35 MHz signal and VT-F_{HS} (6.4 MHz). The second hybrid is connected as a low pass amplifier to further attenuate the fundamental and upper sidebands on the mixed signal. Since the mixer output is 50 KHz, the hybrid circuits are connected by external capacitors. The third hybrid is used as a limit amplifier to shape the signal. The signal is then fed to an A16 hybrid level converter and to a PL976 buffer to further square the output. Decoupling for the +9 vdc power line is provided by a dropping resistor and three filter capacitors.

The 6.35 MHz oscillator is used as the reference frequency for the fine range mixers. The oscillator is crystal controlled to maintain a stability better than ± 20 ppm required for the AROD application. A stability of ± 20 ppm will result in a range inaccuracy of less than .06 meters. The frequency variation of the oscillator versus temperature is shown in Figure 5-107.

The DC voltage to the oscillator is supplied through a low pass filter section consisting of L2, C3 and C4. Further

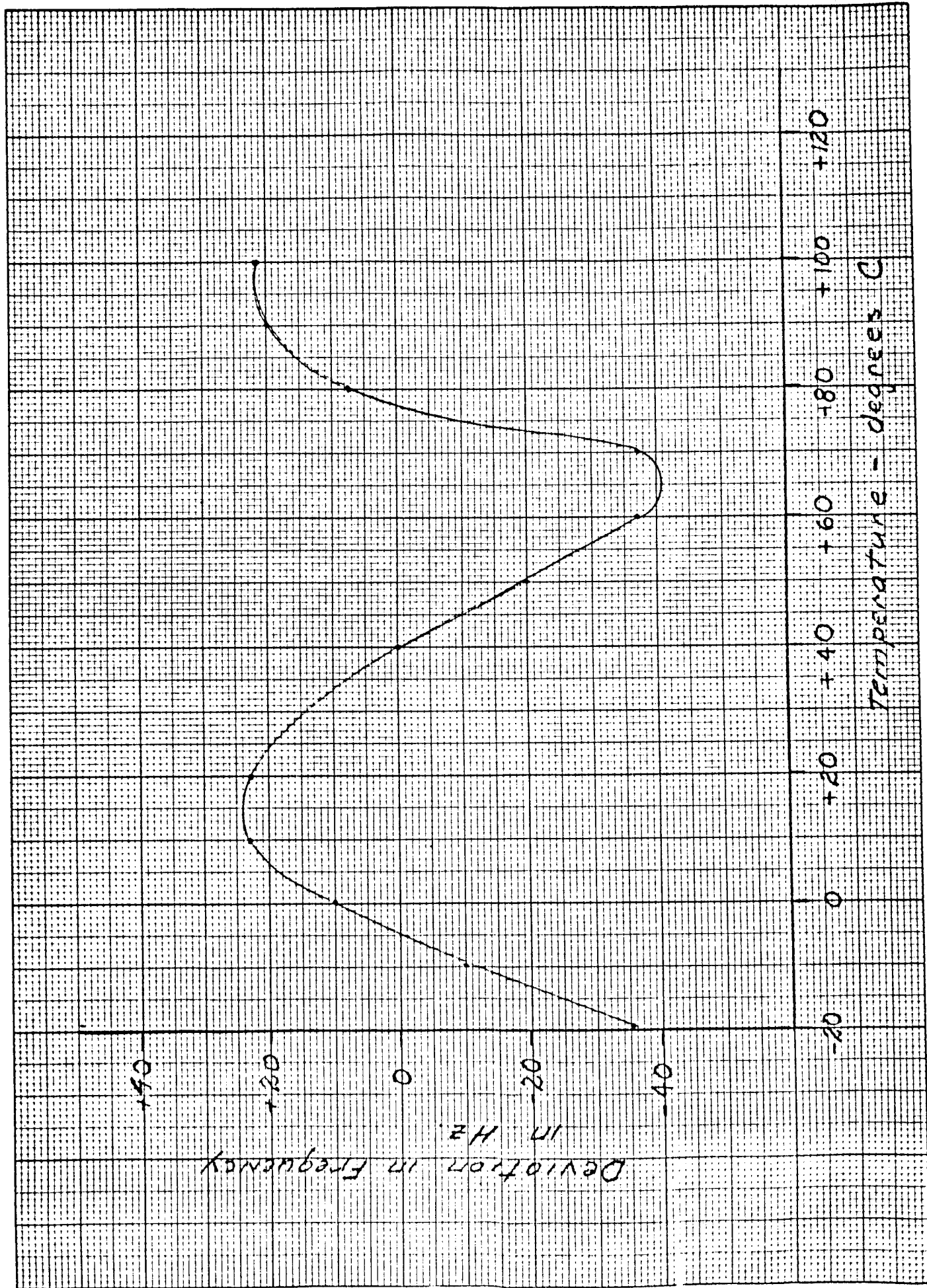


Figure 5-197. Oscillator Frequency Variation vs Temperature

reduction of power line noise is provided by the low pass section of L2 and C7.

The oscillator uses a hybrid differential amplifier (A43) to provide the necessary gain for the circuit. Inductors L1, L3, L4 and L5 together with the varicap capacitors CR2 and CR3 provide the necessary phase shift for the 6.35 MHz crystal Y1. The input impedance variations of the amplifier are damped by the resistance of R3. Transistor Q2 operates as a DC amplifier to control the DC bias on the varicaps CR2 and CR3. The amplifier multiplies the temperature coefficient of the base emitter junction of Q2 by approximately 20. The output of the amplifier is used to bias the varicaps and provide temperature compensation for the oscillator.

5.7.4.4 Test Results

Test results indicate that the conditions set forth in Section 5.7.4.1 are met by the various parts of the Range Extraction Unit.

During the test phase indication of a problem area was discovered. The length of the signal paths for the fine range mixers was found to be quite critical. The VR-F_{HS} signals from each of the receivers should contain approximately the same delay before reaching the fine range mixers. The track location and length on the motherboard on which the fine range mixers are located seemed to have a noticeable effect on the delay of each of the VT-F_{HS} signals. These lengths were made approximately equal by shunting wires across the tracks. It would be desirable in future layouts to keep the tracks the same length.

Because of the difficulty in packaging a large number of passive components in the microharness package, it would also be desirable to repackage the fine range mixers in an RF module.

5.8 SYSTEM CONTROL LOGIC

This section is the final engineering report on the Vehicle System Control Logic (SCL) designed and developed for the AROD system.

The function of the SCL is to control the acquisition and release of ground stations. This is accomplished by using information stored in a core memory and inputs from the Vehicle Transmitter and Receiver Code Control subsystems and the Data Readout subsystem. The SCL has a series data input from a ground station on each of the four channels of the S-Band up-link. The outputs of the SCL are: (1) a serial data output which is transmitted over the VHF link to all ground stations, (2) commands to the Receiver Code Control subsystems, and (3) parallel readout lines to the Data Readout subsystem of the site ID being called, the control command being transmitted, and the state of T-A_H of the ground station.

The decisions and actions pertinent to the operation of the system control logic are based upon information stored in the memory and information obtained from other sections of the AROD system.

The System Control Logic Figure 5-16 is packaged with the memory in three AROD frames. The SCL is comprised of five 4" x 6" motherboards, while the memory requires the remaining one motherboard. THE SCL requires 29 I/C modules and a 1/2 size I/C module containing a power supply filter is packaged on each motherboard. The total SCL (including the memory) weighs 2.53 lbs. Power consumption in the 5 motherboards of the System Control Logic is 1.60 amps at 3.5 vdc (5.6 watts).

Complete specifications on the SCL can be found in Document No. 12-25611F, Electrical Performance Requirements for the System Control Logic.

Figure 5-108 is a simplified functional block diagram of the system control logic. The functional blocks above the dashed

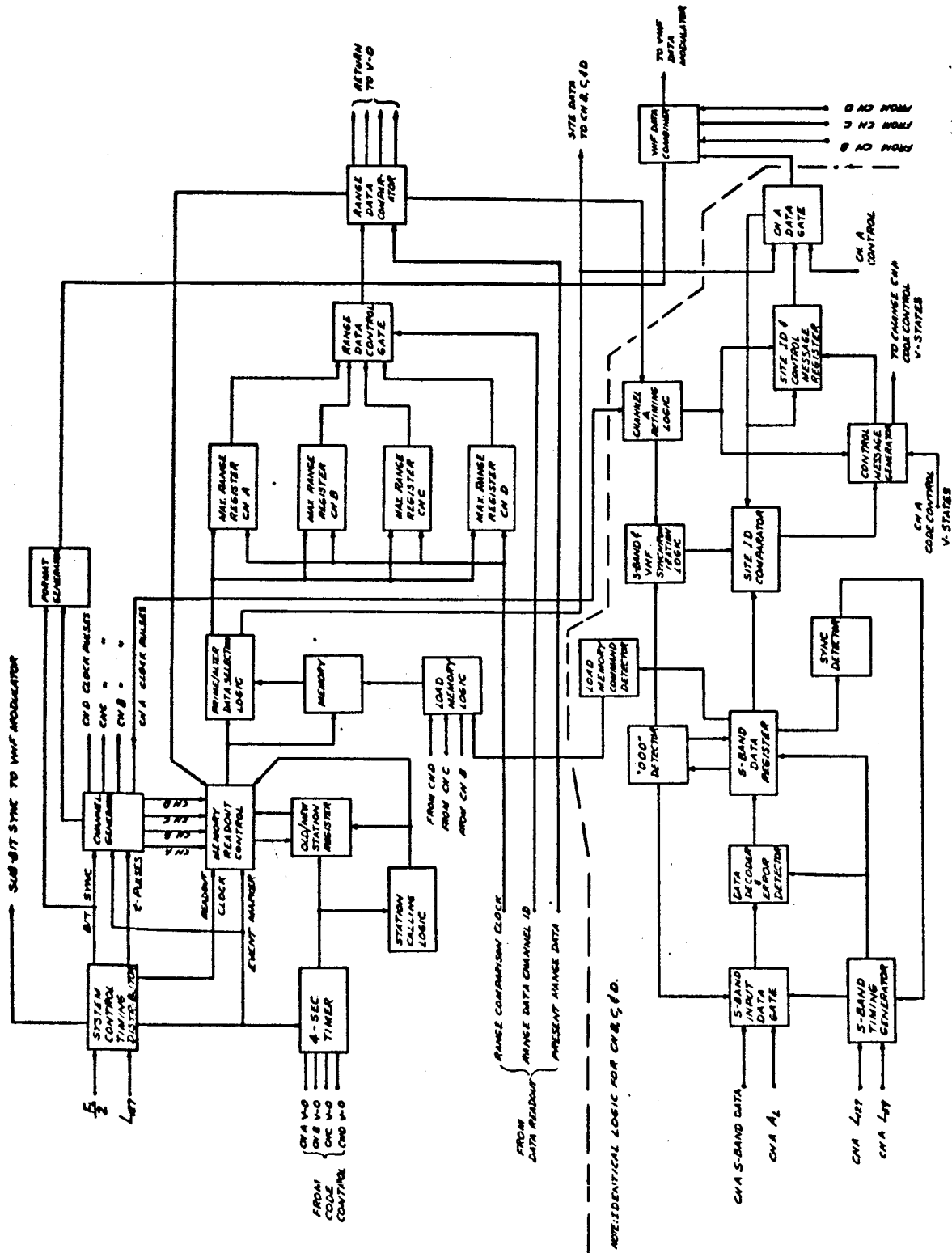


Figure 5-108. AROD System Control Logic Block Diagram

line are common for the four channels. Those below the dashed line are pertinent to a particular channel only. Since there are four such identical but independent channels, only channel A is shown in Figure 5-108.

5.8.1 System Philosophy and Requirements

The system control logic is designed to meet a specific set of requirements. It is not a general purpose computer which may be programmed to solve any preconceived problem or event. The system control logic is not capable of performing such a task. The specified set of requirements is as follows:

1. Store the site identification code and associated maximum range data for each transponder,
2. provide automatic transponder acquisition and reacquisition, whenever the system is in operation,
3. send STANDBY to all transponders within range at approximately 25 times per second,
4. assign channel and frequency to stations being called,
5. ready to operate on the next station in the memory program when a channel becomes available,
6. verify the response from the transponder station, to insure that the correct transponder has answered the call,
7. compare the measured ranges with the respective maximum ranges and operate on the results,
8. provide input to re-load the memory,
9. accept and re-route external S-Band data for other auxiliary subsystem uses.

5.8.2 Detailed Functional Description

Assume all interface signals are in their normal states and are available. Detailed description of these signals may be found in the AROD System Description Manual. For the purpose of describing

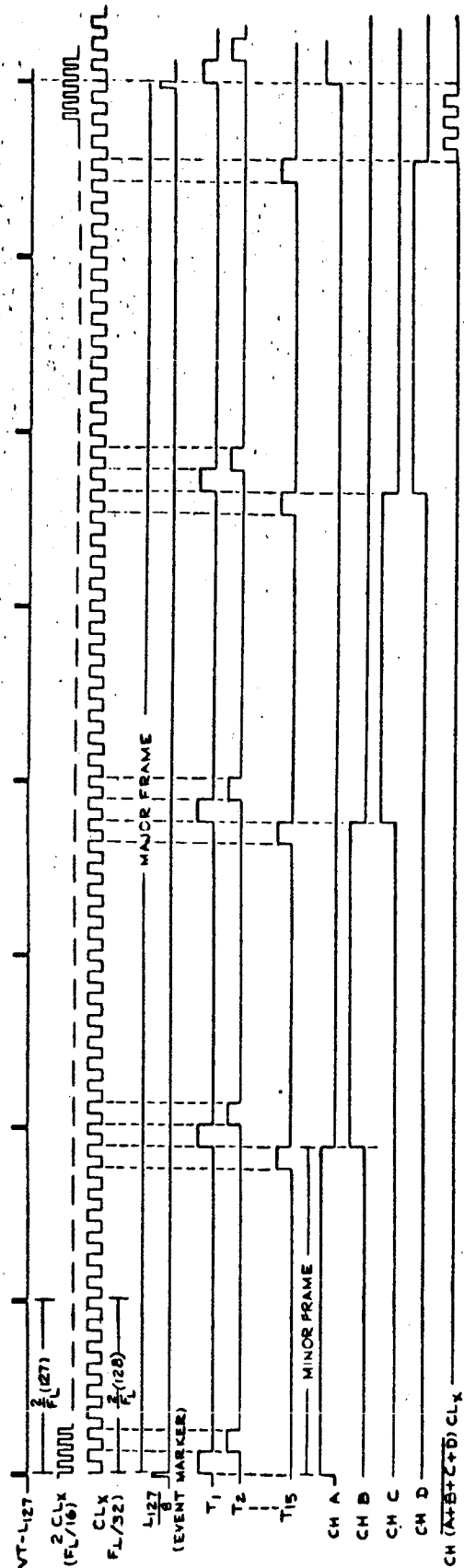


Figure 5-109. Vehicle System Control, Logic Output Signal Timing Diagram

the system control logic, it is sufficient to list these signals by their proper names and briefly describe their functions related to the operation of the system control logic.

5.8.2.1 VHF Data Format

All control messages from the vehicle to the transponder stations are transmitted through the VHF link in a fixed data format. The data format is generated by $F_L/2$ and the transmitter L127 pulses in the system control logic. $F_L/2$ divided by 8, or $F_L/16$, is defined as the sub bit sync, which is labeled as $2CL_x$ in the logic drawings. $F_L/32$, $F_L/16$ divided by 2, is defined as the bit sync, which is designated as CL_x in the logic drawings. L127 divided by 8 is defined as the event marker. There are 127 sub bit pulses between any two event markers. This period is defined as a major frame. Since there are 4 transmitter channels time multiplexed within a major frame, the first 30 sub bit sync period is arbitrarily assigned to channel A, which is followed by channels B, C, and D, with 7 sub bit sync pulses left over. The period occupied by each channel is defined as a minor frame. Each minor frame contains 15 t-pulses. The relationship between the various timing pulses is given in Figure 5-109.

Since the four channels are time multiplexed, the data format for all four channels are made identical as shown in Figure 5-110. The first 3 bits (6 sub bits) are used as word sync, or simply sync. Bit 4 of channel A is used to transmit the event marker, while the complement of the event marker is transmitted in the other 3

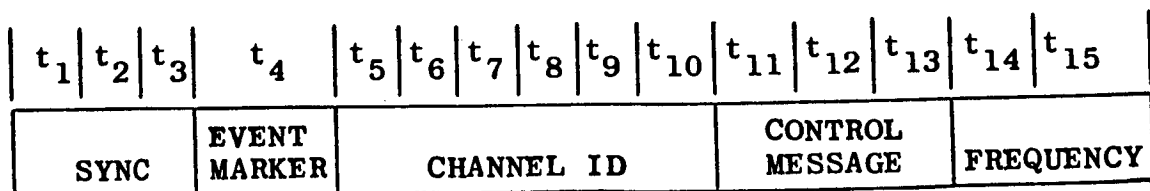


Figure 5-110. VHF Data Format

channels. The 6 channel identification bits are transmitted from t_5 through t_{10} . The next 3 bits, t_{11} through t_{13} , are the control and information messages. These messages are given in Table 5-12. The frequencies associated with the respective channels are given in Table 5-13. These frequencies are fixed with the channels.

TABLE 5-12. Control and Information Messages

MESSAGES	t_{11}	t_{12}	t_{13}
RETURN TO STANDBY	0	0	0
ON	1	1	1
TRACK	1	0	1
LOAD MEMORY	1	0	0
LOAD MEMORY ERROR	1	1	1

TABLE 5-13. Channel-Frequency Assignments

CHANNELS	t_{14}	t_{15}
A	0	0
B	1	1
C	0	1
D	1	0

The VHF data rate is approximately 400 bits per second. The one to two relationship between bit and sub bit sync pulses is used to encode each data bit into two sub bits. A binary ZERO is encoded into a ONE followed by a ZERO. The 3-bit sync is uniquely encoded into 6 sub bits as 1 1 1 0 0 0. The resulting transmission rate is approximately 800 sub bits per second.

5.8.2.2 Initial Acquisition

Assumed that the acquisition switch is in the OFF position and all interface signals are in their initial states. The VHF link has been transmitting standby (sync) signals to all transponder stations within range and RETURN TO STANDBY control message to whatever site ID's may be left in the output registers. Once

the acquisition switch is changed from OFF to ACQUISITION, the very next event marker pulse starts initial acquisition. During the first minor frame the site ID for channel A is read out of the memory and transmitted along with the ON control message. Site ID's for channels B, C, and D are similarly transmitted during the subsequent three minor frames. As the site ID's and control messages are transmitted, they are also recirculating in the respective channel output register for later operations. The associated maximum range data are stored in their respective registers. If all four transponders respond in 4 seconds or less, the initial acquisition cycle is over and the system control logic progresses to normal acquisition and release of transponder stations. If no response is received from any of the 4 transponder stations at the end of 4 seconds, they are advised to return to standby. A set of new ID's and maximum range data are obtained from the memory. The above procedures are repeated until at least one transponder station responds. Table 5-14 outlines the initial acquisition procedures and responses.

The 16 cases listed in Table 5-14 are all possible combinations of responses at the end of the first 4 seconds of initial acquisition. Regardless of what the ending response may be, it will eventually work its way to case 16. The initial acquisition procedures may be summarized as follows:

1. Whenever no response is received from the transponder stations at the end of 4 seconds, the site ID's being called are replaced by a set of 4 new site ID's taken out from the memory. Only prime sites are called during this phase of the initial acquisition cycle.
2. Once one or more transponder stations respond to their calls, the site ID of each responding station is examined to see whether it is the oldest of the 4 current site ID. The oldest site ID is defined as one of the four that comes out of the memory first and the newest site ID comes

TABLE 5-14. Transponder Responses at the End of 4 Seconds

Case	Ch. A	Ch. B	Ch. C	Ch. D	Remarks
1	No response	No response	No response	No response	Get new set of ID's from memory
2	No response	No response	No response	Response	Get new ID's for Ch. A, B, and C, hold on Ch. D.
3	No response	No response	Response	No response	Get new ID's for Ch. A and B and continue to call that of Ch. D, hold on Ch. C.
4	No response	Response	No response	No response	Get new ID for Ch. A and continue to call ID's in Ch. C, and D, hold on to Ch. B.
5	Response	No response	No response	No response	Hold on to Ch. A, continue to call ID's in Chs. B and C, call Ch. D alternate.
6	Response	Response	No response	No response	Hold on to Chs. A and B while continue to call Ch. C, call Ch. D alternate.
7	No response	Response	Response	No response	Get new ID for Ch. A, hold on to Ch. B and C, continue to call Ch. D.
8	No response	No response	Response	Response	Get new ID's for Ch. A and B hold on to Ch. C and D.
9	Response	No response	No response	Response	Hold on to Ch. A and D while continue to call Ch. B and C.
10	Response	No response	Response	No response	Hold on to Ch. A and C, continue to call Ch. B, call Ch. D alternate.
11	No response	Response	No response	Response	Get new ID for Ch. A, hold on to Ch. B and D, continue to call Ch. C.

TABLE 5-14. Transponder Responses at the End of 4 Seconds (con't)

Case	Ch. A	Ch. B	Ch. C	Ch. D	Remarks
12	No response	Response	Response	Response	Get new ID for Ch. A, hold on to Ch. B, C, and D.
13	Response	No response	Response	Response	Holding on to Ch. A, C, and D while continue to call Ch. B.
14	Response	Response	No response	Response	Holding on to Ch. A, B, and D while continue to call Ch. C.
15	Response	Response	Response	No response	Call Ch. D alternate while holding on to Ch. A, B, and C.
16	Response	Response	Response	Response	Go to normal acquisition and release of transponder stations.

out last. If the responding transponder station is the newest, the oldest station is then sequentially replaced by new site ID's until the responding station becomes the oldest station. This procedure will eventually lead to case 16.

As an example, let site ID's 1, 2, 3, and 4 be respectively channels A, B, C, and D. At the end of the first 4 seconds, channels A and C have no response, case 11. Since site ID #1 is the oldest, it is then replaced by site ID #5 from the memory, which makes site ID #2 in channel B the oldest. For the next 4 seconds, channels B and D will go on to perform their normal operating routine while channels A and C are still trying to receive response from their respective transponders. If neither site ID #3, channel C, nor site ID #5, channel A, responds to their call at the end of this 4 second period, the ending response is identical to case 10 with the channels rotated somewhat. From on site ID #5 and its alternate site ID are being called alternately at 4 second intervals until a response is received from either site ID #5 or its alternate or site ID #2 in channel B is released. Once channel B releases site ID #2, a new site ID, #6, is then read out from the memory into channel B. Once site ID #6 gets into channel B, site ID #3 in channel C becomes the oldest site ID. If it still has not responded to its call it is then released and replaced by site ID #7 from the memory at the end of the next 4 second period. As old and non-responsive site ID's are sequentially released and replaced by new ones from the memory, it is always possible to locate the proper transponder stations.

5.8.2.3 Normal Acquisition

Once the system control logic acquires 4 transponder stations, it goes into the normal acquisition mode. Under normal operating conditions, a transponder station is released when its range exceeds its stored or programmed maximum range and the doppler sign is negative. It is then necessary to acquire a new transponder station. Figure 5-110 is the acquisition data flow diagram.

When a new site ID is read out of the memory, the system control logic generates an ON control message in the appropriate time slot to call the new transponder station to come on. At the same time the code control logic is told to advance from state V-0 to V-1 which starts the 4 second timer. If the transponder station receives the decodes the data word correctly, it transmits its site ID and the station status modulated with the L code back to the vehicle at approximately 50 bits a second. Negative doppler shift is also inserted in the transponder carrier frequency. The transponder station data format consists of 10 bits, 3 bits for sync, 6 bits for site ID, and 1 bit for station status. While the transponder station is performing its housekeeping functions in preparation to transmit its site ID and status, the vehicle system control logic is continuously transmitting the ON control message once per major frame. All this time the code control is searching to lock on the transponder L-code.

After the vehicle achieves coarse L code lock, the vehicle code control goes to state V-2, which enables the system control logic to receive the transponder data. The system control logic decodes and verifies the transponder site ID. If verification is accomplished in less than 4 seconds, the system control logic changes the control message from ON to TRACK. Once TRACK is transmitted, the transponder station is considered to have responded. The 4 second timer has no further effects on the operation of this channel. If the transponder site ID is not verified at the end of the 4 second interval, and since this is the newest site ID, system control logic then signals the memory to read out the alternate site ID and the above operations are repeated on the alternate site ID for the next 4 second interval.

When the transponder station receives and decodes the TRACK correctly, it removes the negative doppler shift. While the transponder station is sweeping the transmitter frequency to the true doppler shift, the vehicle system control logic continues to send TRACK and the code control remains in state V-2. When

the transponder station completely removes its negative doppler, it is then considered in full tracking operation, and signals the vehicle control logic by modifying the station status bit. The vehicle system control logic decodes the change in station status and instructs the vehicle code control to go to state V-3, where it is searching for the H code. The normal acquisition cycle is complete once the code control acquires the H code at which time it goes to state V-4. This particular channel is now in full track.

During the full track mode, the system control logic continues to send TRACK and check the station status. If the complete channel is functioning properly, the system control logic is then ready to decode the load memory address. Whenever such an address is received from the transponder station the system control logic instructs the memory subsystem to accept new site ID data. If such an address is not present, the system control logic compares the present range data R with the stored maximum range data R_{max} . If $R < R_{max}$ the comparison result is ignored as though nothing has happened. When $R \geq R_{max}$ and the doppler sign is negative, the system control logic changes the control message from TRACK to RETURN TO STANDBY. This releases the transponder station and reverts it back to the standby mode. Once the system control logic decides to release the transponder station, the vehicle code control is instructed to go to state V-0 and the memory subsystem is instructed to provide a new site ID. The channel is then available to be assigned to the new site ID and the above procedure is repeated.

5.8.2.4 Drop Out and Reacquisition

Whenever a drop out occurs to a transponder station that has responded, the system control logic always tries to reacquire that particular transponder station. The reacquisition procedure varies somewhat depending upon the vehicle code control state at which the drop out occurs. Assume that the drop out occurs at state V-2 before or after the transponder station ID has been

verified, the vehicle code control automatically returns to state V-0. The system control logic changes the control message from either ON or TRACK to RETURN TO STANDBY and resets the 4 second timer. On the next major frame, an ON control message is substituted for that of RETURN TO STANDBY. If the transponder station responds in less than 4 seconds, all subsequent operations are identical to those of normal acquisition. If the drop out transponder station has not responded at the end of the 4 second reacquisition interval, and it is the oldest transponder station, the system control logic then releases it and instructs the memory to read out a new site ID. However, if it is the newest transponder station, it is then replaced by its alternate. If it is neither the oldest nor the newest, the above calling cycle is repeated at every 4 second interval until either the transponder station responds or finally becomes the oldest station.

If a drop out occurs while the vehicle code control is in state V-3 or V-4, the system control logic does nothing until the code control returns to state V-0. The above reacquisition procedure is then applied.

5.8.2.5 Load Memory

While the vehicle is in flight, it is possible to reload the memory with a complete new program of site ID's and range data. In order to reload the memory via a particular channel, its transponder station must be in the full track mode. Such an operation is initiated by the transponder station which transmits the load memory code and its complement followed by the desired memory data. When the system control logic receives and decodes the messages correctly, the memory data are then routed to the memory subsystem. The system control logic changes the control message from TRACK to LOAD MEMORY so as to acknowledge receipt of the load memory address. This signal is sent as long as load memory is in progress. If at any time a parity error is detected while the memory is being reloaded, the system control logic changes the control message from LOAD MEMORY to ERROR. When this

happens the transponder station must retransmit the load memory signals. In the absence of the ERROR control message, the memory is considered successfully reloaded.

5.8.3 Implementation

This section contains a detailed description of the logic diagrams of the System Control Logic. The drawings referred to are detailed logic diagram and are quite bulky; therefore, they are not contained in this report. The complete System Control Logic is contained on DWG 69-24630G (sheet 1 and sheet 2).

5.8.3.1 Timing Generation and Distribution

Control timing pulses for the system control logic are generated by three modules. These modules are called timing distributor module 1, timing distributor module 2, and timing buffer module, drawings numbers, 69-23388G, 69-23392G, and 69-24380G respectively. The two main inputs for timing generation are $VT-F_L/2$ and $VT-\overline{L}_{127}$ from the vehicle transmitter code control. Flip Flops FF1, FF2 and FF3 (refer to drawing No. 69-23388G) are connected to form a ripple type binary counter which divides $VT-F_L/2$ by 8 to obtain $F_L/16$. The sub bit sync (SBS) and its complement (\overline{SBS}) are derived from the outputs of FF3. The event marker pulse is generated by the coincidence of \overline{L}_{127} and the three flip flops at G8. This coincidence occurs every 8th L_{127} pulse (see Figure 5-109). FF4 is reset by the event marker pulse through FF9 of 69-23392G so as to readjust CLx with respect to the start of a major frame.

Flip flops FF5, FF6, FF7 and FF8 are connected as a 4 stage shift register which generates the 4 minor frames associated with the 4 VHF channels. The CLx pulses are separated by the 4 minor frames such that channel A operates on the first minor frame, channel B is the second minor frame, etc. The event marker pulse shifts a ONE into FF5 to start the minor frame generator and at the same time a ONE is shifted into FF1 of the T-pulse generator (timing distributor module 2). Since the T-pulse generator is always

shifting at CLx rate, 15 CLx pulses later, the output of FF16 (t_{15}) is fed back to FF1 through gates G3 and G2 and simultaneously advances the minor frame generator to the next channel. The feedback operation is repeated while the system control logic is operating on channel A, B, and C. The $\overline{CH(A + B + C)}$ signals inhibits t_{15} at gate G3 during remaining portion of the major frame so that the T-pulse generator is at the reset state prior to the start of the next major frame.

At no time should there be more than a single ONE in either the minor frame generator or the T-pulse generator. If either generator should get into a confusing state, $\overline{CH(A + B + C)}$ enables them to get out of trouble.

The timing buffer module, 69-24380G, contains a number of gates and buffers so as to increase the driving capabilities of the various timing pulses.

5.8.3.2 Site ID Data Selection Logic

The lower left hand portion of DWG 69-24630G (sheet 2) contains all the required logic for the memory subsystem to read out the proper sequence of transponder stations ID's. The event marker pulse shifts the acquisition switch position into FF1 (see 69-23554G). If FF1 is in the set state (acquisition switch in the OFF position), the output of buffer D1 presets the memory to the last site ID position. So long as the acquisition switch is in the OFF position, the system control logic is relatively idle.

Assume that the acquisition switch has just changed from OFF to ON, the very next event marker pulse shifts a ZERO into FF1 which inhibits future preset pulses from D1 to the memory. FF1 and FF2 are now in the same state which signifies initial acquisition. The output of G11, which is a positive pulse of one major frame duration, enables D3 to advance the memory. \overline{T}_3 is allowed to go through D3 to advance the memory. \overline{T}_3 is allowed to go through D3 to advance the memory counter, which has been resting on the last memory position to the first position during the first minor frame,

second position during the second minor frame, etc. This same pulse is routed to set FF6 of 69-23548G which allows 24 sub bit sync pulses for the memory subsystem to read out the prime and alternate site ID's and the associated range data. FF5 is triggered to accept only the prime site ID and its range data only at this time.

Each memory position contains 24 data bits. All prime site ID data are stored in the odd bit positions and alternate site ID data in the even bit positions. The first 12 bits are the prime and alternate site ID codes and the last 12 bits are the maximum range data. As site data are read out of the memory the odd bits are temporarily stored in FF2 and the even bits in FF4. CLx shifts the odd bits from FF2 to FF3 so that the prime and alternate site data appear at the input of A3 at the same time and last for the same duration. FF5 allows the selected site data to go through A3 to the output data register. Similarly the maximum range data are allowed to go through A4 to the maximum range data register. FF7, G16 and G19 enable the selected site ID data to be shifted into the pertinent output data register between T5 and T13 at CLx rate. The maximum range data are shifted into the R_{max} register between T10 and T15. The control signal is generated in FF8 and G12. Since both output data and R_{max} registers are controlled by the particular channel clock pulse during memory read out the selected data are always read into the pertinent channel registers.

5.8.3.3 VHF Data Control Logic

As the selected site ID data pass through A3 of 69-23536G, FF12 lets 9 $\overline{Ch_n} \overline{CL_x}$ pulses through D1. The first 6 pulses shift the selected site ID into the output data register FF1 through FF6. The last 3 pulses shift the ON control message out of the register and at the same time position the 9 data bits in the proper flip flops for future transmission. Any time the output data register is shifting, the outputs of A3 are gated through G10 and G11 to the data gates in the encoder module. The ON and

RETURN TO STANDBY control messages are inserted through A1, all others through A2. These control messages are generated by selecting the proper combinations of T pulses and clock pulses gated with the proper channel information and/or code control states.

The output data from the various channels are combined and encoded in the encoder module, 69-24388G. The 1 1 1 0 0 0 is generated by combining $T_1 + \overline{CL_x} T_2$ and waiting until T_4 to generate the event marker or its complement. Event marker is coded into a sub bit ZERO followed by a sub bit ONE for channel A, and the complement is transmitted for the other 3 channels. The site ID data and control messages are similarly coded between T_5 and T_{13} as these data are shifted out of the output data registers. The frequency data are encoded by selection of the appropriate combinations of T_{14} , T_{15} , the outputs of FF1 and the four minor frames. The dead period between the end of channel D and the beginning of channel A is filled in by $CH \overline{(A+B+C+D)} CL_x$ so as to obtain a continuous data pulse train.

The site ID data and control messages stored in the output data register are recirculated once per major frame. During this period, 18/127 of a major frame, the data readout subsystem is inhibited from sampling the site ID and the associated data of that particular channel.

5.8.3.4 Site ID Verification Logic

The received S-band data for a given channel are strobed into the sync and ID register, 69-23532G, by VR L_{59} and VR L_{127} when A_L is a ONE. The strobe rate is determined by the particular function the register is required to perform. To receive and detect the S-band sync, the register is shifting at the sub bit rate $2CL_R (VR L_{59} + VR L_{127})$. This is accomplished by letting $\overline{VR L_{59} + VR L_{127}}$ through gates G4 and G5 as shown in 69-23544G. When the S-band sync is correctly detected by the combination of G7, G8, and G9 (69-23532G), flip flop FF2 (69-23544G) is reset so as to insure proper decoding of the site ID data. The sync pulse also sets FF3 which changes the register shift rate from $2CL_R$ to CL_R by interchanging the roles of gates G2 and G4 for the

next 6 bits. The received site ID data is now assumed to be in the register between FF3 and FF8. The CL_R shift pulses to the register are then inhibited by G13 of 69-23544G. This is accomplished by setting FF4 when the 0 0 0 portion of the received sync word reaches the last 3 stages of the register (6 S-band data bit after the sync word). FF4 also inhibits the sync word detector so that there is no possibility for the received site ID to be mistaken for the sync word. The received site ID data are ready to be compared with those in the output data register when the pertinent minor frame arrives.

To compare the two site ID data, FF5 and FF6 of 69-23544G are set at T4 by the pertinent channel clock pulses, $\overline{CH_N} CL_X$, via gates G24 and G29 respectively. The output of FF5 allows exactly 6 CL_X pulses to go through G19 and G5 to shift the receiver site ID data out of the sync and ID register in synchronization with the VHF output data register. The actual serial comparison is accomplished by G26, G27, and G22. If an error is detected any time during the comparison period, FF6 is immediately reset, while FF4 and FF5 are automatically reset at the end of T10. The above sync and ID verification operations are repeated until the received site ID is successfully verified.

Once the site ID is verified, FF6 remains in the set state which enables G33 and G34 to change the present ON control message to TRACK. At the end of T12, FF7 is set to indicate that TRACK control message has been sent and the received ID verified. All subsequent site ID comparisons are inhibited by G18. The VHF portion of the control logic continues to send the TRACK control message until the code control logic instructs it to do otherwise. At the same time the S-band section of the control logic continues to detect sync and decode the site ID data and begins to check the station status, the last data bit (2 sub bits) in the S-band data format. The significance of the 2 sub bits of bit 10 is as follows:

1. The first sub bit indicates the status of the transponder station A_H .

2. The last sub bit indicates $\overline{\text{DRC}}$ the complement of reverse Doppler complete.

The status of A_H is stored in a flip flop for the data readout subsystem. $\overline{\text{DRC}}$ is detected at G1, which instructs the code control to advance to state V-3 when reverse Doppler is completely removed. The code control starts to search the H-code and proceeds to V-4 when H code lock is achieved. The transponder station acquisition cycle is now completed. The channel is now considered in full track mode.

5.8.3.5 Range Data Comparison Logic

There are four maximum range data registers, one per channel, 69-23396G. The 6 bit R_{max} data are read into the pertinent register when the selected site data are read out of the memory. After the transponder site ID has been verified and the vehicle is going away from the transponder site, the 6 most significant bits of the range data are then compared with the R_{max} data. The actual comparison is accomplished by subtracting R from R_{max} , more precisely adding \bar{R} to R_{max} and detect the final carry state. If $R \geq R_{\text{max}}$, the final carry is always a ZERO, otherwise a ONE. The timing pulses for the range comparison operations are derived from the data readout subsystem.

When it is time to compare the range data of a particular channel with its R_{max} data, G2 and G4 of 69-23396G are enabled by CHAN-N-MRD from the data readout subsystem. G2 allows 6 comparison pulses, CL_C , to shift R_{max} through G4 and to recirculate it through G7. The output of G4 is serially added to the 6 most significant bits of \bar{R} , low order bit first. At the end of the 6th CL_C pulse R_{max} is once again in its normal order in the register. FF7 effectively delays the CHAN-N-MRD signal by one CL_C period so that G9 allows only the last carry through to FF8. If $R \geq R_{\text{max}}$, a ONE is stored in FF8 so as to synchronize with the particular channel timing. The pertinent T3 then sets FF9 and instructs the code control to return to state V-0. If the instruction is faithfully executed by the code control, FF8 is then reset by CL_C and a RETURN TO STANDBY control message is transmitted to the transponder station. On the same T3 pulse of

the next major frame, FF9 is reset set and G10 signals the memory counter to advance to a new position which contains the prime and alternate site data of the next transponder in the sequence.

5.8.3.6 Station Sequence Register and 4-Second Timer

As transponder station site ID's are read out of the memory, the order in which they come out are stored in four 3-stage shift registers, one per channel. FF10, FF11, and FF12 of 69-23396G represent a typical channel. The complete arrangement of these registers is given on Dwg 69-24630G. The shift pulses to these registers are the advance memory pulses and the inputs are the respective channels (minor frames). After 4 site ID's, the registers always have the information to identify the oldest and newest of the four current ID's.

Since the memory is advanced and read out in the same minor frame, a ONE in the first stage of a particular register represents that the newest site ID is in that channel. The all ZERO state represents the oldest site ID. For example, four site ID's are read out of the memory during the first major frame of initial acquisition. Since the ID's are read out one per minor frame, beginning with channel A, the states of the four registers at the end of the first major frame are given in Table 5-15. Channel A has the oldest station, 0 0 0, while channel D has the newest, 1 0 0.

Channel	FF10	FF11	FF12
A	0	0	0
B	0	0	1
C	0	1	0
D	1	0	0

Table 5-15. Station Sequence Registers

The registers retain their respective states for at least the next 4 seconds. Since channel A is the oldest of the 4 current site ID, CH_A T3 is gated through G15 once per major frame until the channel has responded. The output of G15 indicates the particular

channel with the oldest site ID. Similarly G19 of channel D indicates that the newest site ID is in that channel. Once a channel has responded to its call, gate G17 associated with that channel is disabled which in turn inhibits G15 and G19. As long as the transponder has not responded to its call, the code control of the corresponding channel is continuously instructed to return to state V-0 by the output of G18. However, this output is inhibited by G12 of 69-24384G until the end of the 4 second acquisition interval. At which time G12 enables the return to state V-0 signal to the code control. If the non-responsive site ID is the oldest, it is then released and replaced by a new site ID from the memory. The station sequence registers are rotated one more step which essentially makes channel B the oldest and channel A the newest, etc.

The 4 second timer controls the basic acquisition cycle. There is only one such timer in the system. It's main function is to keep track of the elapsed acquisition time from the last V-0 state. The 4 second timer and its associated control logic are shown in 69-24384G. It consists of a 5 state binary counter which counts major frames (event markers). Since each major frame is approximately equal to 0.16 seconds, the 4 second timer output is only approximate. G2 and G3 are arranged to detect a count of 25 (1 1 0 0 1), which is approximately equal to 4 seconds. Whenever the code control of one or more channels are in state V-0, the counter is reset by $\overline{CH(A+B+C+D)}CL_x$, the period between the end of minor frame D and the beginning of the next major frame. The event marker pulses to the counter are inhibited at gate G17 until all code controls are no longer in state V-0. The last of such a transition is reflected through G18 so that the counter always starts from the all ZERO state.

At a count of 25 (1 1 0 0 1), the 4 second timer flip flop FF6 is set by the next event mark pulse. The setting of FF6 signifies that 4 seconds have been elapsed since the last site ID has been in the acquisition cycle. This site ID can be any of the four current site ID's, depending on the acquisition mode. Once FF6 is set, the code control of all non-responsive site ID's

is sequentially instructed to return to state V-0 through the appropriate gates G8, G13, G14, and G15. If the non-responsive site ID is the oldest, it is then released and replaced by a new site ID from the memory. If the non-responsive site ID is the newest, its alternate replaces it for the next 4 second interval. All other non-responsive site ID's are given additional 4 second intervals to answer their calls. However, the 4 second timer has no effects on the operation of the channel whose transponder site ID has been verified. When all 4 channels are in TRACK, the 4 second timer keeps on counting beyond 25 and finally recycles itself.

To understand the operation of the 4 second timer, assume the system control logic has just started on the initial acquisition cycle, and the code control of the respective channels has just advanced to state V-4. As soon as the last V-0 state (channel D) becomes a ZERO, the negation output (pin #8) of G5 inhibits all $\overline{\text{CH(A+B+C+D)CL}_x}$ pulses at G19 and G20. At the same time the positive output (pin #9) of G5 becomes a ZERO. The transition from ONE to ZERO enables G18 to reset the 4 second counter to the all ZERO state. The counter is now ready to count the event marker pulses. As the system control logic is trying to acquire the transponder stations, the counter keeps on counting event marker pulses until G2 and G3 detect a count of 25 (1 1 0 0 1). The next EM pulse shift a ONE into FF6, which enables G8, G13, G14 and G15 for one major frame. During this major frame, the code control of the non-responsive channels is instructed to return to state V-0 at T3 of the pertinent minor frame, as RETURN TO STANDBY is sent to the appropriate transponder stations. If a transponder station has responded, the associated RET to V-0 (4-SEC) is inhibited at G17 of 69-23396G. The operation of that particular code control follows its normal acquisition procedure. Once the code control of the non-responsive channels returns to state V-0, the 4 second timer is reset to the ready state by CH(A+B+C+D)CL_x toward the end of this major frame.

Beginning with the next major frame, the second one after a count of 25, the EM pulse shifts the state of FF6 into FF7 to

start a new 4 second acquisition cycle for the vacant channels. Assume channels A, B and D are available while channel C is in TRACK. Since channel A still has the oldest site ID in its output data register, it must be released and replaced by a new prime site ID from the memory. This is accomplished by letting CH_A T3 through gate G22 of the 4 second timer logic. The output signal of G22 is used to advance the memory, set prime site ID data selection logic, and rotate the station sequence registers. Once the station sequence registers are rotated, the site ID in channel B automatically becomes the oldest and that of channel A the newest. Channel B is then similarly operated upon by the CH_B T3 pulse during the second minor frame. Since channel C is assumed in TRACK, CH_C T3 is inhibited by the TRACK SENT signal so that channel C continues to perform its normal routine. The site ID in channel D is now neither the newest nor the oldest. The system control logic simply tries once more to acquire that transponder station starting from the standby mode. Beginning with the next major frame, the 4 second timer starts a new acquisition cycle for channel A, B, and D. As long as the oldest transponder station, site ID in channel C, remains acquired, the non-responsive transponder stations are given additional time, at 4 second intervals, to respond to their respective ON control message, except the newest site ID, channel B in this case, which alternates with its alternate site ID. The above acquisition procedures always locks on to any transponder station that responds to its call. The first station in the sequence so acquired automatically becomes the oldest station for the subsequent 4 second acquisition intervals.

If all transponder stations are in good working order, the above acquisition procedures eventually leads to a set of 4 responsive stations. Once a station has been successfully acquired, it is released only if its range exceeds the programmed maximum range and the Doppler sign is negative. When such a station is released a new prime site ID is selected to replace it. The new prime site ID is given a 4 second time period to respond. If no response is received at the end of the 4 second interval, its

alternate site ID is then selected for the next 4 second interval. If the transponder stations are released no faster than one station in approximately every 4 seconds, the alternate site ID of a non-responsive prime site is always given at least one 4 second interval to respond. If all prime site transponder stations respond to their calls in less than 4 seconds, no alternates are called, unless such alternates are also primes for some other site ID's.

5.8.3.7 Drop Out and Reacquisition Logic

Occasionally the vehicle code control may return to state V-0 due to signal drop out. This may occur in any of the V states, except V-0. In any case the system control logic always tries to reacquire the drop out station for at least 4 seconds. If a drop out occurs in states V-1 or V-2 (see AROD System Description for definitions of drop out and reacquisition), the code control subsystem automatically returns to V-0. The 4 second timer is reset and a RETURN TO STANDBY control message is transmitted to the transponder station, so as to acquire the transponder station from its standby mode. The 4 second timer starts again only if the code control advances to V-1. Resetting the 4 second timer is in essence to shift the 4 second interval to coincide with the beginning of the reacquisition cycle.

If a drop out occurs at states V-3 or V-4, the code control subsystem tries to reacquire the transponder station independent of the system control logic. If the code control fails to reacquire the transponder station in 2.5 seconds, then it returns to state V-0 and signals the system control logic to reacquire. As far as the system control logic is concerned, there is no difference in the acquisition procedures whether a loss of signal occurs at V-1, V-2, V-3 or V-4. Once the code control returns to V-0 due to the loss of signal, the system control logic always applies the normal acquisition procedures during the next 4 second interval. If the drop out transponder responds before the end of the 4 second interval, it is considered reacquired. If no response is received at the end of the 4 second period, one of the following steps is taken:

1. If it is the oldest transponder station, release it and replace it with a new one from the memory.
2. If it is the newest transponder station, release it and replace it with its alternate.
3. If it is neither 1 nor 2 above, continue to call the particular transponder station at 4 second intervals until it finally becomes the oldest station, 1 above.

The system control logic always goes through its normal acquisition cycle whenever a particular code control is at state V-0. The main difference between acquisition and reacquisition is that the former involves getting a new site ID from the memory, while the latter requires keeping the 4 current site ID intact. The control logic must therefore inhibit all signals which may change the current site ID's and memory position.

The drop out and reacquisition signals may occur any time in relation to the 4 second timer. If either of these two signals occur while the 4 second timer flip flop FF6 (69-24384G) is set, it is then necessary to inhibit G22 and G23. If the drop out or reacquisition occurs any other time the 4 second timer resets itself to start a new 4 second interval. The drop out and reacquisition control logic is shown in 69-23554G. The DO and RA signals are combined to enable flip flops FF4 and FF5 to generate a pulse DO + RA of variable pulse width at G14. The output of G14 may be one or two major frames wide, is used to inhibit G6 so that the next event marker pulse keeps FF3 in the reset state. DO + RA is similarly utilized to inhibit the 4 second time flip flop from setting FF7 of 69-24384G. This is in essence to disable the Drop Oldest Station or readout Newest Memory Data signals from entering the memory subsystem during the drop out or reacquisition operations. The system control logic resumes its normal operating routine at the conclusion of the reacquisition cycle.

5.8.3.8 Load Memory Logic

A new program of site ID data may be loaded into the memory while the vehicle is in flight. Such an action must be initiated

from the ground transponder station via the S-band link. The load memory address consists of two S-band data words as shown in Figure 5-111. Data bits 1, 2, and 3 are the first of two

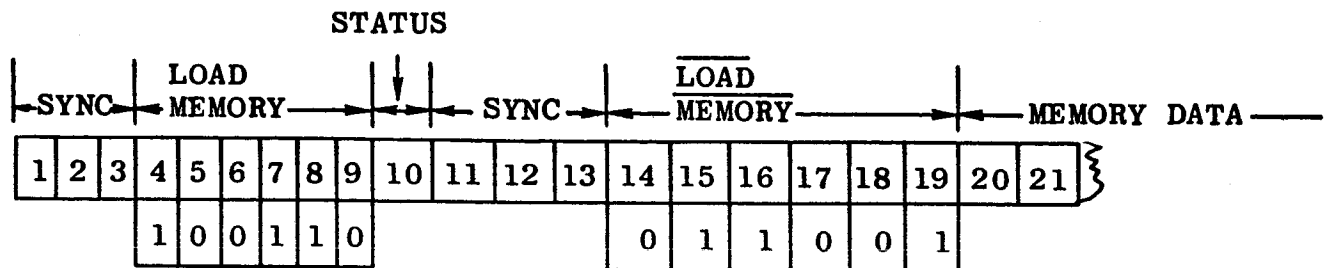


Figure 5-111. Load Memory Address

data word sync. Data bits 4 through 9 are the load memory code which is 1 0 0 1 1 0. Bit 10 is the normal transponder station status. Data bits 11, 12, and 13 are the second S-band data word sync within the load memory address. Bits 14 through 19 are the complement of the load memory code (0 1 1 0 0 1). The new program of site ID data for loading into the memory starts with bit 20 and lasts until the memory is completely loaded. The transponder station may then resume its normal tracking operation. All data associated with the load memory operation must be coded according to the two for one coding technique as defined in the AROD System Description.

The load memory address detection and verification logic is given in 69-23528G. The combination of G22, G23 and G26 is arranged to detect the LOAD MEMORY code and that of G24, G25 and G27 detects the complement. The sync pulse gated with $2CL_x$ (SYNC $2CL_x$) normally resets flip flops FF4, FF5, FF6 and FF7. When the LOAD MEMORY code is properly detected, a ONE is read into flip flops FF4 and FF5. The function of FF4 is to inhibit the second sync pulse in the load memory address so as not to reset FF5. The complement of the LOAD MEMORY code sets FF6 and presets the memory counter to the last memory position. The ZERO output of FF5 and FF6 is gated with $\overline{\text{TRACK SENT}}$ at G21. The output of G21 is the load memory enable signal. It enables G15 to read parity error into FF7. The output of G21 is also used to set FF10 of the Output Data Register module which changes the control message from TRACK (1 0 1) to LOAD MEMORY (1 0 0). All

subsequent S-band data and pertinent clock pulses of the particular channel are also gated by the load memory enable signal to the memory subsystem.

When the memory is completely loaded, the memory subsystem sends a memory loaded pulse to G19 to reset FF4, FF5, and FF6. The output of G21 immediately becomes a ZERO which enables FF10 of the Output Data Register module to return the control message from LOAD MEMORY to TRACK. If no parity error is detected while the memory is being loaded, the memory is then considered successfully loaded. However, if a parity error is detected during the load memory operation, FF7 stores the error signal for the remaining portion of the load memory cycle. The content of FF7 is transferred to FF11 of the Output Data Register module by the channel clock at T10, so as to change the control message from LOAD MEMORY (1 0 0) to ERROR (1 1 1). When the ground transponder station receives such a sequence of control messages, it must retransmit the load memory address and memory data until the memory is successfully loaded. The implementation of the memory subsystem is given in another Technical Memorandum.

5.8.4 Memory

The function of the AROD Memory is to provide non-volatile storage of the programmed site ID and corresponding maximum range words for each ground station.

Each word of the Memory contains site ID and maximum usable range for both a prime and an alternate station. This requires a 24 bit word. The bits are arranged such that the prime station data are the odd bits and the alternate station data the even bits. This is done to facilitate the System Control Logic readout from the Memory. For the AROD test model, only six words are required and only enough drive electronics for six words have been provided. However, the design is readily expandable.

The AROD Memory consists of a plane of wide temperature ferrite cores and six microharness modules. They are mounted on a 4" x 6" printed circuit board (1A8A2) in Case 1 of the system. Figure 5-16 shows the Memory as it is packaged with the System Control Logic.

Complete specifications for the System Control Memory can be found in Document No. 12-25623F, Electrical Performance Requirements for the System Control Memory.

5.8.4.1 Sub-System Requirements and Technical Approach

The information to be stored for AROD need only be accessible in a semi-serial manner. The bits of each word are always read-out serially, but it is sometimes required that any word be read-out repeatedly before advancing to the next. This requirement and the small size of the AROD memory suggested an electronic memory (Delay line, I.C., etc.) as being more practical. However, the requirement for non-volatile storage of the data and the requirement for expandability dictated a magnetic storage device. The most economical choice of magnetic storage devices was a core memory.

The memory is a simple magnetic core plane in which the bits are selected one at a time by the coincidence of two currents. A single sense winding links all cores in the array. The operation of the memory is the normal read-restore type of non-destructive readout. The memory plane was purchased from the Fabri-Tek Company and the electronics were designed and built by Motorola.

A basic design goal was to package all memory electronics in integrated circuit form to be compatible with the other subsystems of AROD. However, there were no monolithic or hybrid circuits available on the market that would meet the current requirements for memory drive circuits. By specifying the new RCA core 0140M5, a full switching current of only 450 ma and a full switching time of 2 μ s was required. This means that for bit rates less than 10 kHz, the power dissipation requirements of the memory drivers are well within the limits for integrated circuit packaging. This core also has very stable operating characteristics over the required temperature range.

The memory drive electronics were designed in hybrid chip form and were packaged in 14 pin flat packs in the Motorola hybrid circuit shop. Three circuits were required for the memory electronics:

AROD CURRENT LIMITER - A18

To maintain a disturb ratio of less than 0.6 during core switching, a pulse current regulation of less than $\pm 10\%$ is required. This regulation could be provided by use of a series resistor only. However, this would require a reasonably high voltage supply that was quite stable. For this reason a rather unique current limiter was designed for the AROD Memory. A circuit of the current limiter is shown in Drawing No. 63-24714F. The circuit is simply used as a series resistor in the power supply input to the memory lines. The circuit permits the use of a low voltage (+10v) wide tolerance ($\pm 10\%$) power supply. It also improves the current rise time and provides some temperature compensation. One current limiter is used in each of the two selection axes of the memory.

AROD CORE DRIVERS - A19

Each core driver must handle half of the full select current (225 ma). This circuit is shown in Drawing No. 63-25715F. It is a two input gate that controls an output transistor switch. Two such circuits are used on each end of a memory line for connection to either ground or the power supply. In this way current can be drawn through the line in either direction by enabling the proper combination of the gate inputs. This is necessary for the read and write operations.

AROD DIODE MATRIX - A20

A two diode per memory line selection scheme was determined to be the most feasible for the AROD memory. Each diode in the matrix must handle 225 ma of peak forward current. The A20 diode matrix is packaged such that six pairs of diodes are contained in each flat pack. Drawing No. 63-25716F is a schematic of this circuit. Schematics and test procedures for these three circuits are contained in Document No. 12-24623H (see Appendix 3).

Several good monolithic sense amplifiers were available on the market. The T.I. sense amplifier SN5500 was selected primarily because of the packaging configuration and because it

offered both time and amplitude discrimination capability built into a single package.

The Philco MW3 monolithic circuitry was used in all the memory addressing and control logic to be compatible with the other AROD subsystems.

5.8.4.2 Logic Description

A logic diagram of the memory subsystem is shown in Drawing No. 69-24631G. A block diagram of the memory motherboard is shown on Drawing No. 69-26326G.

The memory decoding logic consists of a bit counter and a word counter. The bit counter is comprised of a 4-stage and a 6-stage counter which are then combined in the diode matrix to provide drive to 24 digit lines in the memory. The word counter is a 6-stage counter which provides drive directly to 6-word lines in the memory. The word capacity could be expanded by using a diode matrix decoding scheme like that of the bit counter.

The memory is operated by first providing a "PRESET" pulse which positions the bit and word counters to the proper initial state. To load the memory the "LOAD MEMORY COMMAND" input is made a logic "1" and "DATA" and "CLOCK" inputs are provided. On each clock pulse the bit counter is advanced one position. After 24 clock pulses the word counter is advanced one position. The bit and word counter outputs enable the X and Y selection lines for one core in the memory for each combination of counter positions. Shortly after the leading edge of the clock pulse (approximately 10 μ s) a 2 μ s read pulse is generated which turns one set of the enabled line drivers. The state of the memory core is sensed by the T.I. sense amplifier and the output flip-flop is set accordingly. Approximately 5 μ s later a write pulse is generated using the state of the output flip-flop so that the same polarity bit is written back into the memory. The write pulse is also a 2 μ s pulse which turns on the opposite set of enabled line drivers. Write current flows in the opposite direction through the memory lines. The read-restore cycle is completed in this manner.

During the 2 μ s pulse, a narrow strobe pulse is generated which enables the sense amplifier. Since the sense amplifier has an amplitude discrimination capability, the output from the core is then strobed in both time and amplitude. This provides a high effective signal to noise ratio of the output signal.

An output signal, "LAST BIT LOADED", is provided from the memory by sensing the last state of the bit and word counters.

To read data from the memory, the operation is identical except that the word counter will only be advanced by applying an external "ADVANCE MEMORY" signal. Applying a clock signal only will readout the same word repeatedly.

5.8.5 Test Results

The memory was tested at -25°C , $+25^{\circ}\text{C}$, and $+85^{\circ}\text{C}$. Operation was very satisfactory from -25°C to $+70^{\circ}\text{C}$. Above $+70^{\circ}\text{C}$ the hybrid core driver circuits did not have sufficient noise immunity to the Philco MW/3 circuitry which provides the input to the drivers. This problem could be corrected by changing the input impedance at the expense of slightly higher power dissipation. However, in reviewing the operational temperature requirements with the Systems Engineering group, it was determined that the $+70^{\circ}\text{C}$ operating point would never be exceeded in normal operation. This correction would be made in any future systems.

The bit-error rate tests of the memory selection system yielded very satisfactory results as indicated on the data sheets.

The SCL subsystem excluding the memory was tested at three environmental temperatures; -25°C , $+25^{\circ}\text{C}$, and $+85^{\circ}\text{C}$. It operated satisfactorily over this range. No problems were encountered with the logic design. The design appears very adequate to meet the requirements and no improvement is particularly needed.

5.9 POWER CONVERTER

This section is the final engineering report on the DC to DC Power Converter designed and developed for the Vehicle-Borne portion of the AROD System.

The Power Converter is packaged within Case 1 of the Vehicle-Borne Equipment which is to be mounted on the cold plate within the Space Vehicle. Operating from the 28v prime power supply, the Power Converter develops all the voltages necessary to operate the Vehicle-Borne AROD System with the exception of the TWTA, which contains a separate power supply in the present configuration.

The Power Converter was designed to have an overall efficiency of approximately 60% while operating at the nominal 28v prime input supply. The power supplied through six separate output voltages totals 89 watts. The Power Converter dimensions are roughly 8" x 4" x 1-3/4", and the unit weighs approximately 1545 grams. (See Figure 5-17).

5.9.1 Requirements

The requirements for the AROD Power Converter are given in the Design Specification No. 12-26176G. The summary of these requirements is listed below.

Input:	28.0 \pm 4 volts
Output:	+10v \pm 3% at 1.3A
	+3.5v \pm 3% at 12A
	-3.5v \pm 3% at .2A
	-10v \pm 3% at 1.4A
	-15v \pm 3% at 0.2A
	-28v \pm 3% at 0.5A

The output ripple shall be less than:

3 mv rms without ripple on the prime supply
10 mv rms with ripple on the prime supply

5.9.2 Technical Approach

Three approaches were considered in the design of the Power Converter. These approaches were:

1. A pulse width modulated supply with a post regulator on each output line to remove the ripple.
2. A pulse width modulated pre-regulator followed by a series regulator to remove the prime power ripple followed by a DC-DC converter.
3. A series regulator followed by a DC-DC converter.

The block diagrams of the three systems and the expected efficiencies are shown in Figures 5-112, 5-113, 5-114. The three approaches all had approximately the same efficiency at the nominal voltage. The third approach was considerably smaller and lighter than the other two since it did not need the inductance required by the pulse width supplies. Mainly for this reason, the series regulator approach was chosen for the AROD System.

5.9.3 Theory of Operation

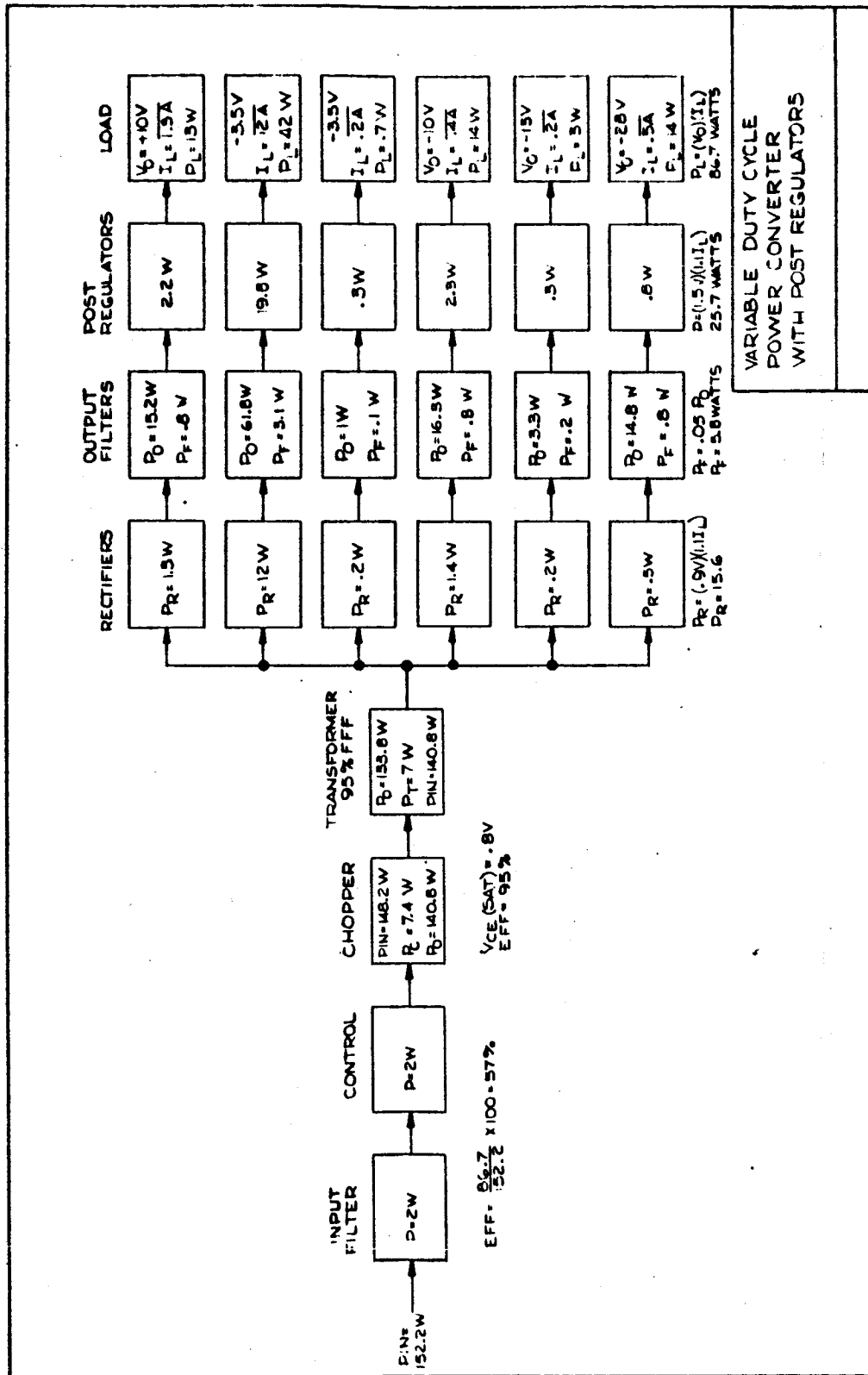
The theory of operation is separated into five sections:

1. Series regulator.
2. Oscillator.
3. Power transformer and choppers.
4. Output filters.
5. Current sensors and monostable.

Figure 5-115 is the electrical schematic diagram of the Power Converter, 63-24523H.

5.9.3.1 Series Regulator

The Series Regulator is the voltage control unit for the Power Converter. It must pass the primary current of approximately 6 amps and reduce the input ripple to the 10 mv required in the output. The Series Regulator is a conventional regulator with a



VARIABLE DUTY CYCLE
POWER CONVERTER
WITH POST REGULATORS

Figure 5-112. Variable Duty Cycle Power Converter With Post Regulators

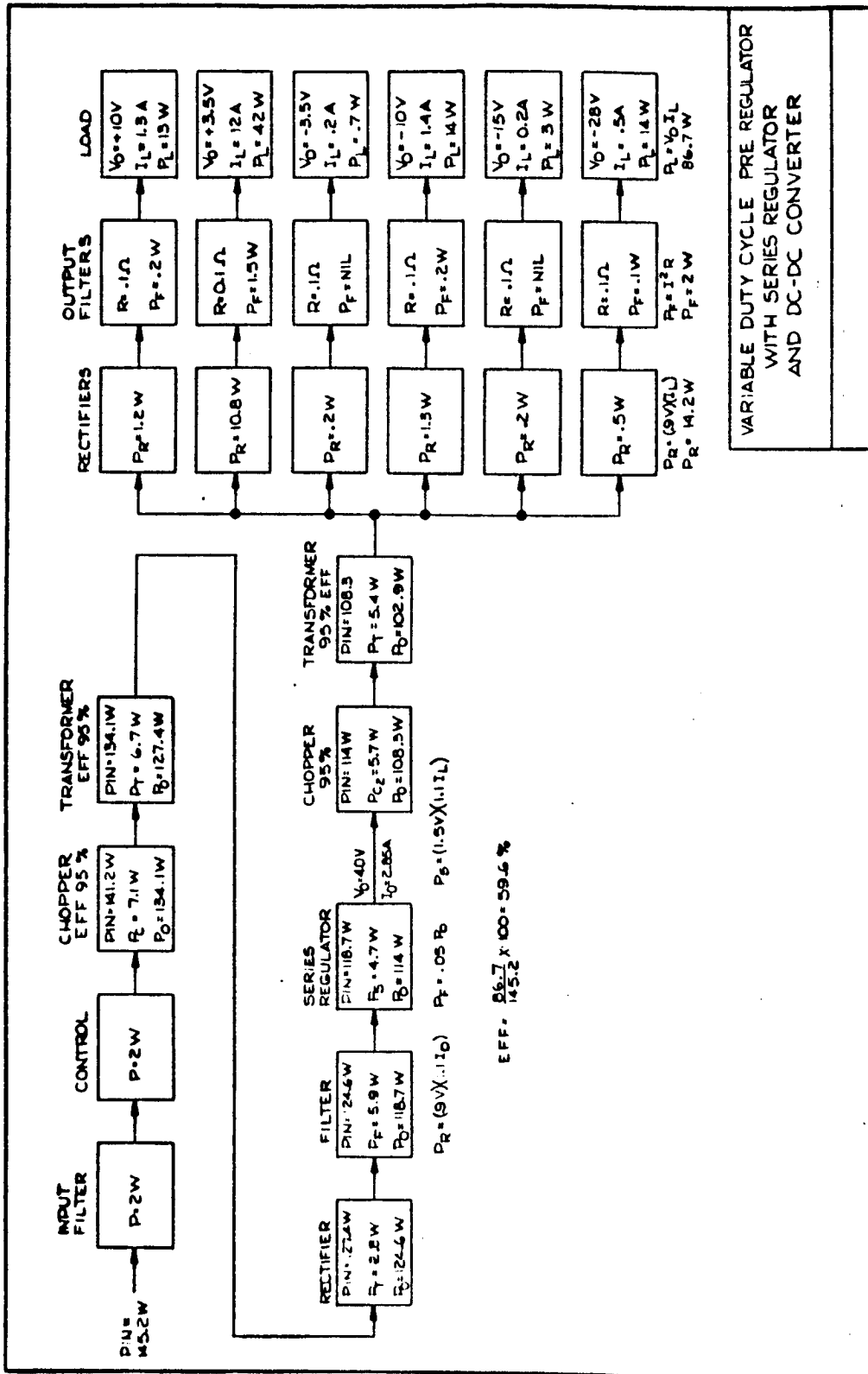


Figure 5-113. Variable Duty Cycle Pre Regulator With Series Regulator and DC-DC Converter

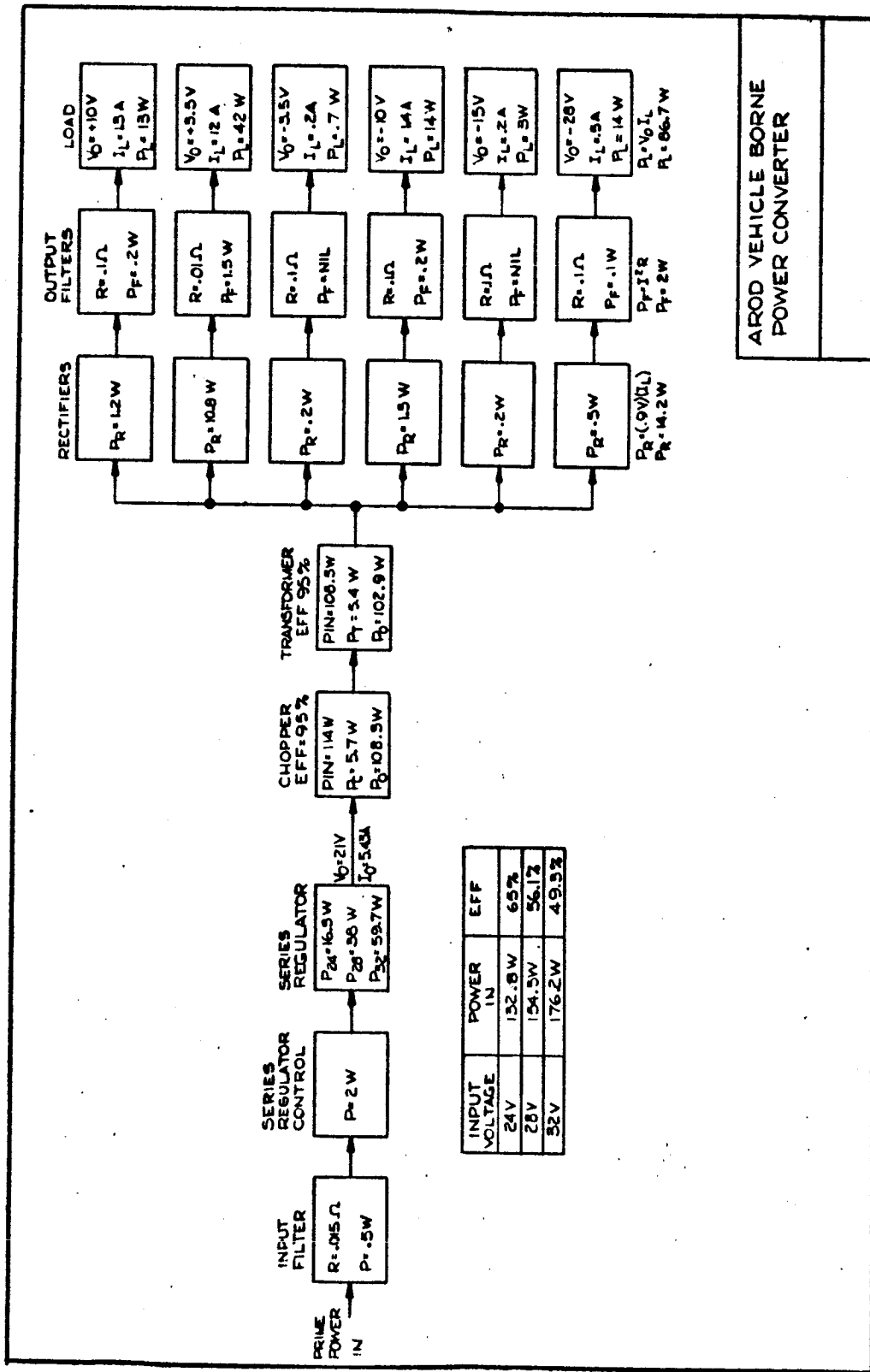


Figure 5-114. AROD Vehicle-Borne Power Converter

delay circuit consisting of R3 and C3. This circuit reduces the drive to the pass circuit until capacitor C3 is charged to a voltage equal to the base voltage of the pass circuit. This same circuit is used to shut off the Series Regulator during over-current load. When the over-current circuit detects a high current condition, capacitor C3 is discharged and the base of the pass transistor is held at ground. The primary winding voltage is rectified to provide a regulated feedback voltage for the base drive of the Series Regulator.

5.9.3.2 Power Oscillator

The Power Oscillator is a transformer coupled astable circuit. The base circuits are connected to the input voltage through a high impedance to insure self-starting. During operation, the low end of the base windings are connected to ground by means of diode CR1. The oscillator supplies base drive to the chopper transistors.

5.9.3.3 Transformers and Choppers

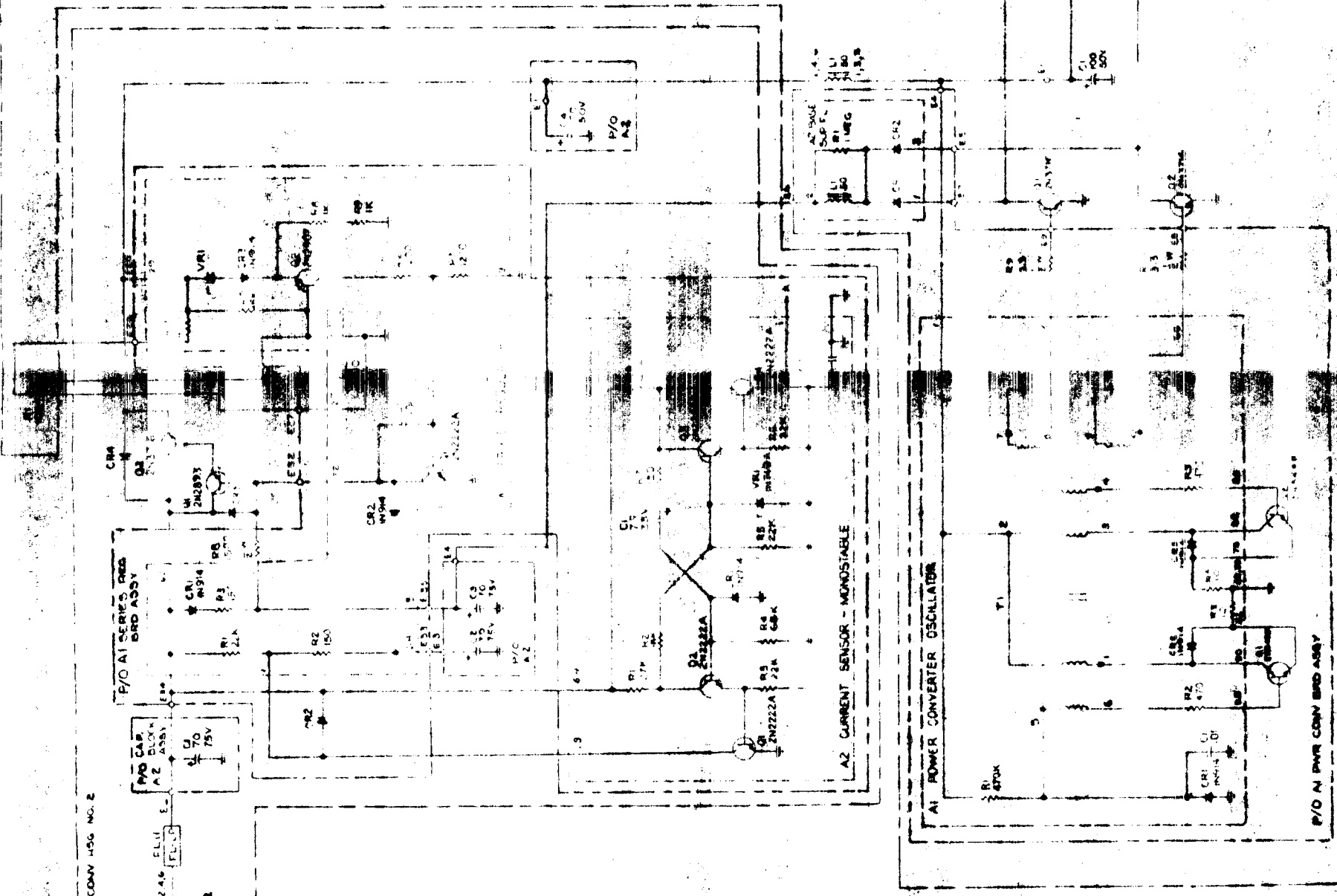
The transformer is driven by a pair of 2N3716 transistors which are, in turn, driven by the Power Oscillator. The Power Transformer has a common winding for the plus and minus 10 volt supplies and separate windings for each of the other four supplies.

5.9.3.4 Rectifier and Output Filters

The +3.5 volt supply, which must produce 12 amps, is split into two circuits so that the rectifiers may be derated to approximately half of their current rating. Each pair of rectifiers supplies current for a separate choke filter section. The outputs of the chokes are connected together to produce a combined 12 amp supply. All output currents pass through a low pass bulkhead mounted RFI filter to remove the chopping spikes before delivery to the circuits.

1. ALL DIMENSIONS ARE IN INCHES.
 2. ALL DIMENSIONS ARE TO CENTER UNLESS OTHERWISE SPECIFIED.
 3. ALL DIMENSIONS ARE TO CENTER UNLESS OTHERWISE SPECIFIED.
 4. ALL DIMENSIONS ARE TO CENTER UNLESS OTHERWISE SPECIFIED.
 5. ALL DIMENSIONS ARE TO CENTER UNLESS OTHERWISE SPECIFIED.

FIG A-2 PWR CONV HSG NO. 2



A1 PWR CONV HSG NO. 1

5.9.3.5 Over-Current Circuit

Over-current detection is accomplished by a current transformer in the rectifier circuit of each output. The current transformers turn ratios are such that approximately 10 milliamperes will flow in the 100 ohm transformer load resistor. All six of the current sensor voltages are combined by diode coupling to the current sensor monostable. The monostable will trip with 2 to 3 volts input which is about 2 to 3 times the nominal current of any output. When the monostable trips it discharges the time delay capacitor of the Series Regulator causing the regulator to shut off power to the chopper circuit, thereby removing the output voltages. The monostable has a quasi-stable state of about 1 second. After the monostable returns to the stable state, the Series Regulator will recover and the output voltages will reappear. In case of a continued short or heavy load on one output, the monostable will continue to cycle, causing the converter to try to supply power about every second.

5.9.4 Breadboard Test Results

5.9.4.1 Series Regulator

The results of the breadboard test of the Series Regulator are shown in Figure 5-116.

5.9.4.2 Temperature Test

The results of the temperature test are:

Temp	Output Voltage					
	-28v	-15v	-10v	-3.5v	+3.5v	+10v
-20°C	27.98	14.50	9.75	3.54	3.26	9.57
+30°C	28.00	14.47	9.72	3.58	3.26	9.53
+55°C	27.92	14.44	9.69	3.57	3.25	9.50

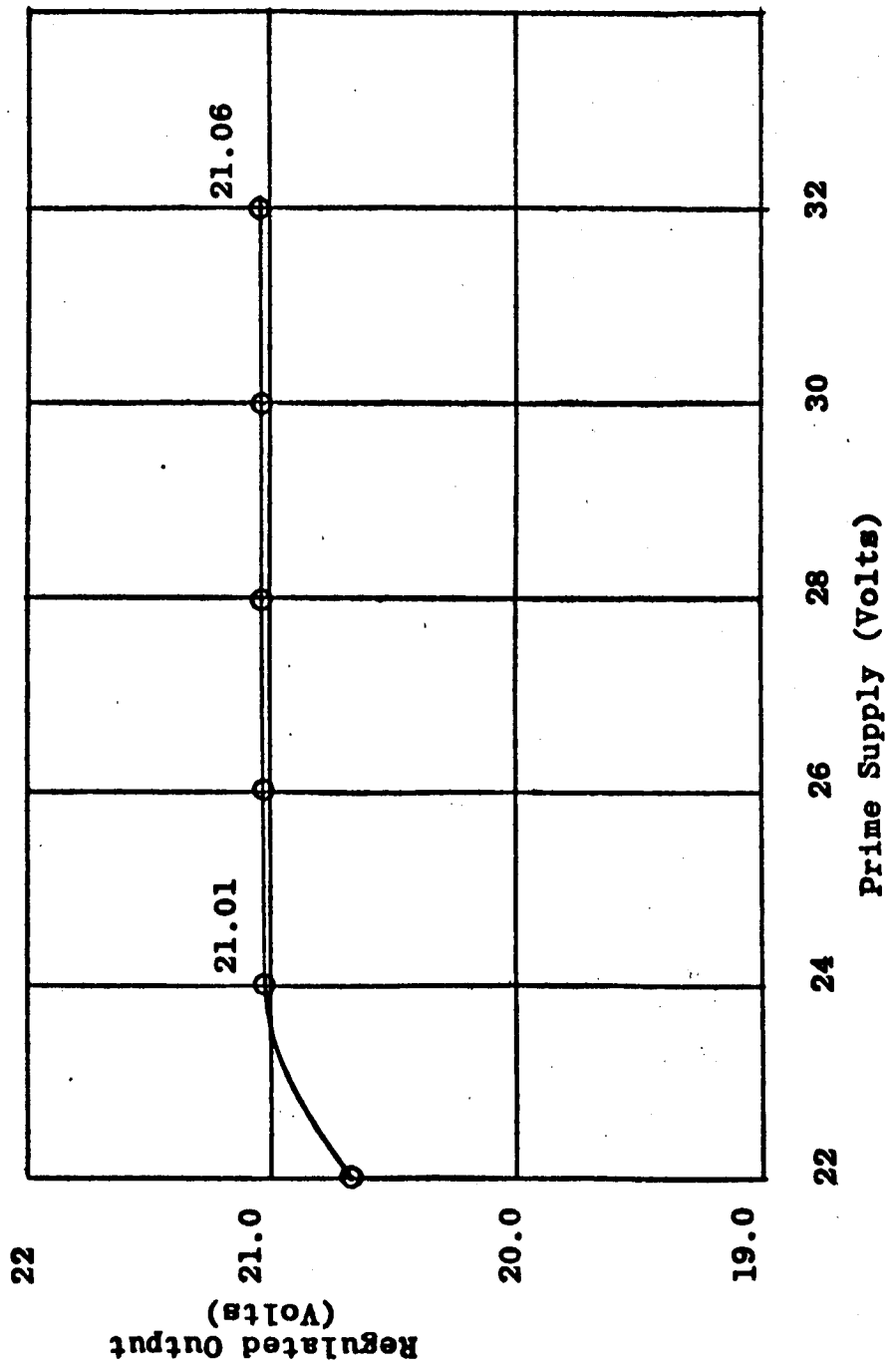


Figure 5-116. Regulation of Breadboard Series Regulator

5.9.4.3 Regulations With Line Voltage

The regulations with input line voltage are:

Input Voltage	Output Voltage					
	-28v	-15v	-10v	-3.5	+3.5	+10v
24	26.63	13.9	9.34	3.42	3.12	9.18
28	27.93	14.79	9.95	3.67	3.36	9.79
32	27.87	14.78	9.94	3.67	3.36	9.78

5.9.4.4 Audio Susceptibility

The results of the audio susceptibility test are with line voltage set at 28 volts.

<u>Frequency</u>	<u>Ripple Peak-to-Peak on -28 Volt Line</u>
100	1.2
200	.90
400	.53
800	.20
1,000	.14
2,000	.06
3,000	.01
5,000	0
15,000	0

When the prime voltage was raised to 28.6 volts, there was no ripple in the output.

5.9.5 Test Results

The test results on the final Power Converter are shown below. The Power Converter was connected to a resistive load while the final tests were conducted.

5.9.5.1 Regulation With Input Voltage Variations

The output voltages were measured when the prime power voltage was adjusted to 24, 28, and 32 volts. The input current remains constant at 5.35 amps for all prime voltage inputs.

Input Voltage	Output Voltages					
	+10v	+3.5v	-3.5v	-10v	-16v	-28v
24	9.58	3.38	3.69	9.75	16.01	28.31
28	9.85	3.37	3.70	9.75	16.01	28.30
32	9.87	3.36	3.69	9.75	16.00	28.28

5.9.5.2 Regulation With Output Load

The prime power input was adjusted to 25 vdc. The load resistance was adjusted to plus and minus 10 percent of the nominal load value and the output voltage measured.

Output Current	Output Voltage					
	+10v	-3.5v	-3.5v	-10v	-16v	-28v
Low	9.94	3.48	3.72	9.81	16.2	28.6
High	9.83	3.36	3.69	9.70	16.0	28.5

5.9.5.3 Regulation With Temperature Variations

The high temperature measurements were made with the power converter frame temperature at +50°C. The cold temperature readings were measured within 2 minutes after startup after a 30 minute soak at the cold temperature.

Temp	Output Voltage					
	+10v	+3.5v	-3.5v	-10v	-16v	-28v
+50°C	9.88	3.40	3.68	9.72	15.97	28.33
-20°C	9.81	3.40	3.64	9.68	16.04	28.42
-30°C	9.74	3.39	3.61	9.63	16.01	28.27

5.9.5.4 Audio Susceptibility

Audio power was applied to the prime power input and the resulting ripple on the -28 volt line measured. The audio equipment does not have the required 0.5 ohm output impedance. The output impedance was adjusted by loading the output of the power amplifier with a resistive load. A plot of the output impedance with the load resistor is shown in Figure 5-117. With the prime power set at 28 volt, the maximum ripple was 8 millivolts rms. The ripple on the -28 volt line was 3.5 millivolts without audio applied.

5.9.5.5 Conducted Interference

The conducted interference was measured by the RFI lab. The results of the tests are shown in Figure 5-118. An Erie RFI filter was added to make the converter meet the specifications.

5.9.5.6 Over-Current Protection

Each output was loaded with a resistor to increase the output current to 2, 3 or 4 times nominal current. The 28 volt current sensor trips the supply off with approximately 2 times nominal current. The 16 volt and -3.5 volt current sensors trip at approximately 3 times nominal current. The two 10 volt current sensors trip at approximately 4 times nominal current. The +3.5 volt current sensor will sometimes trip with a short circuit and sometimes will not trip. Since the load is set at 380 milliohms, it is difficult to obtain a condition which would double the output current. For this reason, the value of the 3.5 volt current sensor is questionable.

5.9.5.7 Efficiency

The efficiency was computed from the measured voltages and currents.

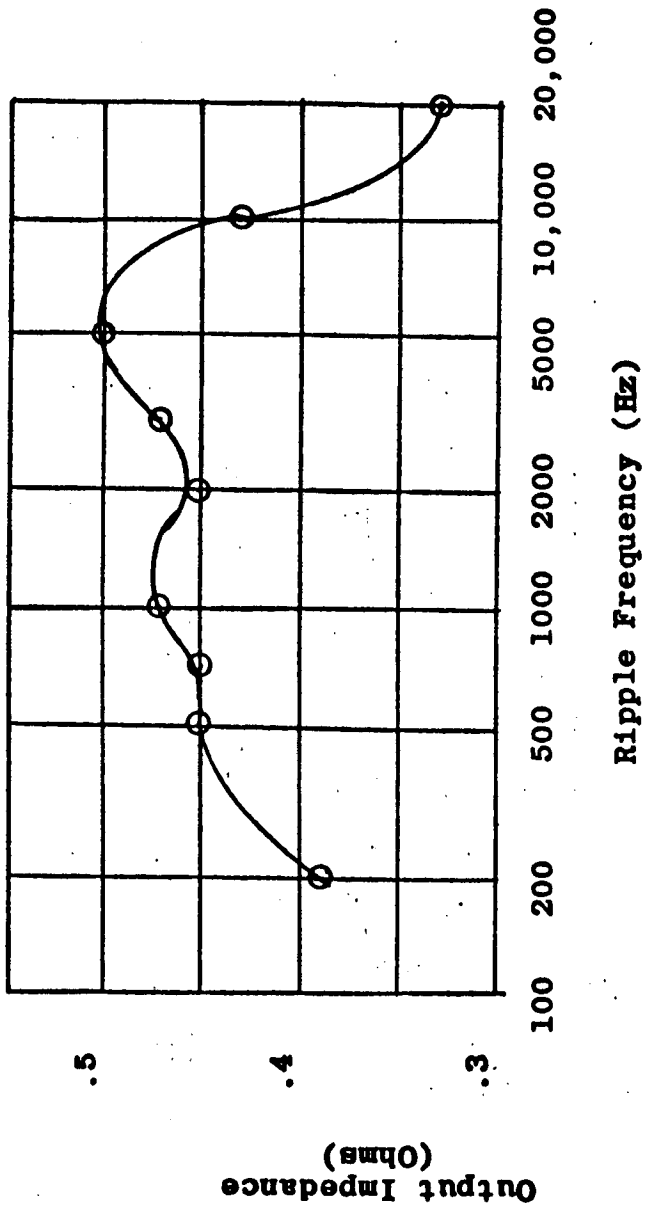


Figure 5-117. Output Impedance of Power Amplifier Used for Audio Susceptibility When Loaded With 2 Ohms

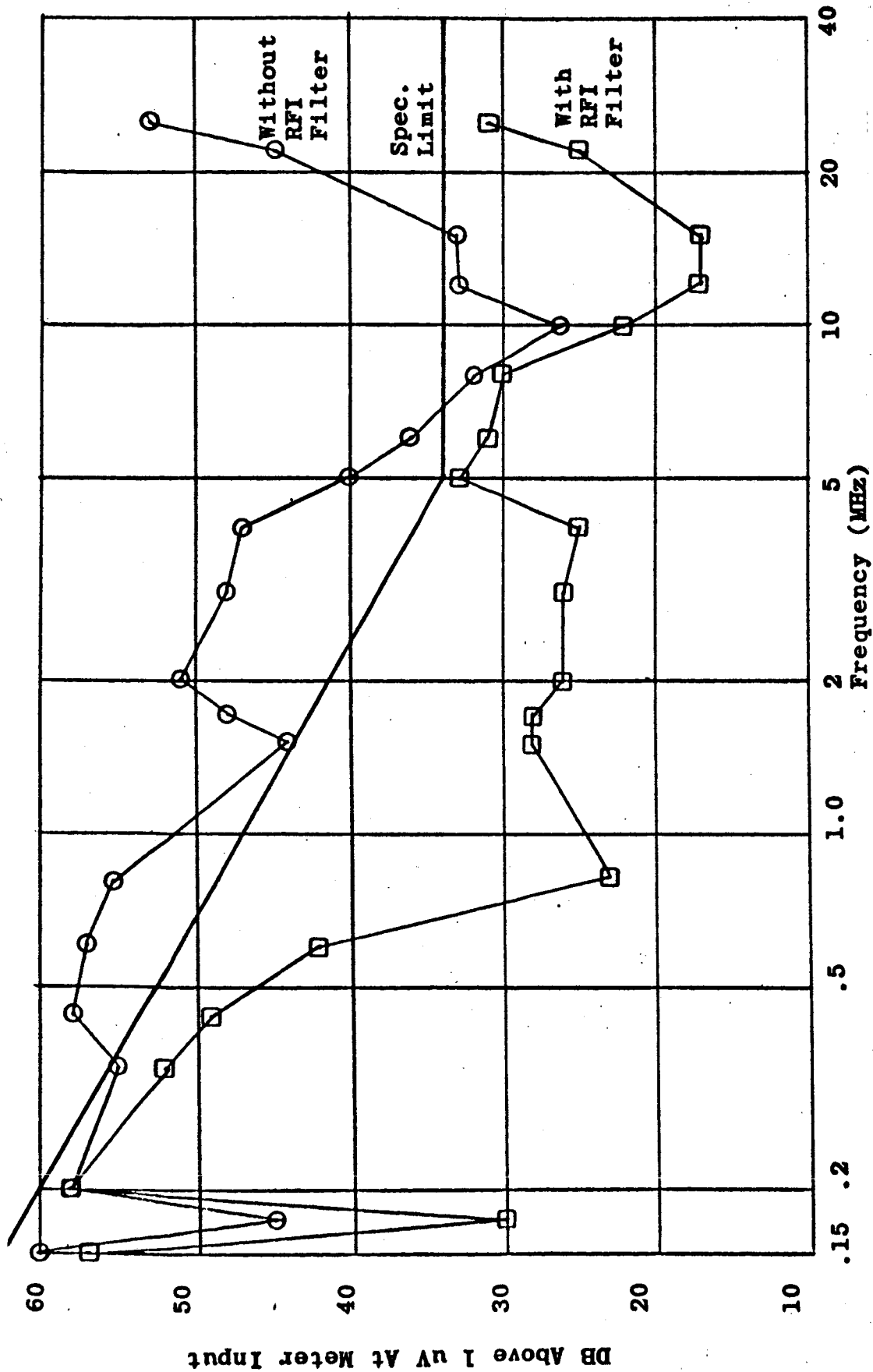


Figure 5-118. Conducted Interference Using LSN (CW)

Prime Voltage	Input Current	Input Power Watts	Output Power Watts	Efficiency
24	5.3	125.5	89	70.7
28		146.3	89	60.7
32		167.0	89	53.3

5.9.6 Design Changes

Three significant design changes were incorporated into the Power Converter during checkout and testing.

1. The filters of the +3.5 volt, and 10 volt supplies were changed from choke input to capacitor input. This change increased the output voltage, reduced the ripple and reduced the chopper current spikes.
2. A heat sink was installed on the series regulator transistor to more efficiently remove heat from the regulator transistor.
3. A low pass broadband RFI filter was incorporated in the input filter section to reduce the conducted line interference.

5.9.7 Conclusions

The Power Converter meets the design requirements with the expected efficiency and regulation. The series regulator approach provides the desired level of audio susceptibility and conducted interference but causes the system to be somewhat inefficient, as well as generating a temperature problem. For future AROD systems these items should be re-evaluated toward a more optimum design. Considerable improvement could also be incorporated within the packaging of the unit.

5.10 VEHICLE TRANSMITTER CODE CONTROL

The Vehicle Transmitter Code Control Subsystem is part of the flight hardware of AROD. It generates the ranging code that is transmitted to the ground station and supplies accurate timing signals to other subsystems. In order to achieve the high phase stability required for the ranging code and timing signals, it was necessary to use a maximum clock frequency of 12.8 MHz. Special hybrid high speed flip-flop output circuits were used to minimize phase shift and insure fast rise and fall times for the ranging code.

The eight digital modules making up this subsystem plus two of the Range Extraction modules are contained on one 4 x 6 inch printed circuit motherboard. The power consumption of the Transmitter Code Control Subsystem, excluding the Range Extraction modules, is approximately 400 ma at +3.5 vdc and 53 ma at -3.5 vdc (total of 1.6 watts). The two Range Extractor modules require an additional 120 ma at +3.5 vdc.

5.10.1 Subsystem Requirements

The primary requirement for this subsystem is to generate a stable ranging code. The code must have a period of approximately 20 milliseconds, be capable of fast acquisition and accurate tracking, and be capable of having digital data inserted into its format. In addition, this subsystem is required to supply certain timing signals to other subsystems and highly accurate information concerning the phase of the transmitted ranging code to the Range Extraction Subsystem.

The ranging code generated by this subsystem is a combination of two pseudo-noise sequences. The high speed component, called the H sequence, has a bit rate of 6.4 MHz and a period of 511; while the low speed component, called the L sequence, has a bit rate of 6.4/1022 MHz and a period of 127. The combination utilized for the Vehicle Transmitter output code, denoted by VT-Z, is given by the following equation:

$$VT-Z = L \oplus H(F_L \oplus F_{L/2}) \oplus D'$$

where $F_L \oplus F_{L/2}$ is a "one" during the second and third quarters of each L sequence bit, \oplus is the "exclusive-or" operation, and D' is the data waveform described in the following paragraph.

D' is normally held at a logic "zero." If it is desired to transmit data with the ranging code, D' becomes the bit sequence defined by:

$$D' = (DATA) (L_{16N+2}) + \overline{(DATA)} (L_{16N+10})$$

where L_{16N+2} is a "one" only during every 16th bit of the L sequence beginning with L_2 , L_{16N+10} is a "one" only during every 16th bit of the L sequence beginning with L_{10} , and DATA is the data bit stream to be transmitted (approximately 100 bits per second).

All timing signals are derived from the 12.8 MHz input frequency, whose analog form is denoted by $VT-2f_H$ and whose digital form is denoted by $VT-2F_H$.

All circuits used are of the standard digital family (Philco MW3), except the square wave generator (A16 hybrid circuit) used to buffer the $VT-2f_H$ input, and the two high speed flip-flops and interface circuits (A33 and A56 hybrid circuits) used to retime the output code, $VT-Z$, and the 6.4 MHz square wave output, $VT-F_{HS}$, output to the Range Extraction Subsystem.

5.10.2 Functional Logic Description

This subsystem is composed of six modules listed below plus two power line filter modules.

<u>Module</u>	<u>Logic Diagram</u>
Code Clock Generator	69-26956F
GR Gates	69-26253G
H Sequence Generator	69-27100F
L Sequence Generator	69-27104F
S-Band Data Encoder	69-27112F
Code Combiner and Output Buffer	69-27108F

In the discussion which follows, signals are called out without the prefix, VT, given on the logic diagrams.

Before discussing the logic design in detail, some definitions and conventions will be stated.

1. Buffer elements perform NOR logic so that an enable signal input to a buffer element is considered to enable the element when the signal is at the "zero" level.
2. H_{N-i} and L_{N-j} are the outputs of the i -th stage of the H sequence generator and the j -th of the L sequence generator, respectively.
3. The bits of the H and L sequences are defined by the following recursion formula and initial conditions:

a. $H_k = H_{k-9} \oplus H_{k-4} \quad k = 10, 11, 12, \dots, 511$

$$H_1 = H_2 = H_3 = H_4 = H_5 = H_6 = H_7 = H_9 = 0$$

$$H_8 = 1$$

b. $L_m = L_{m-7} \oplus L_{m-6} \quad m = 8, 9, 10, \dots, 127$

$$L_1 = L_2 = L_3 = L_4 = L_5 = L_7 = 0$$

$$L_6 = 1$$

Note that when H_k appears as the output of H_{N-9} , H_{k+1} through H_{k+8} are the outputs of H_{N-8} through H_{N-1} , respectively; and similarly, when L_m appears as the output of L_{N-7} , L_{m+1} through L_{m+6} are the outputs of L_{N-6} through L_{N-1} , respectively. The notation, H_k and L_m , will be used interchangeably to denote the k -th or m -th bit of the H or L sequence, respectively, or to denote signals which are "one" when H_k or L_m appear as outputs of H_{N-9} or L_{N-7} and "zero" at all other times. Thus L_{127} might refer to the 127th bit of the L sequence, or to a signal which is a "one" only when L_{127} is the output of the last stage of the L sequence generator. This usage should cause no confusion since the context in which the notation is used will clearly indicate whether the bit or the signal is referred to.

5.10.2.1 Clock Signal Generation

All fundamental clock and timing signals are generated by using three modules consisting of the Code Clock Generator, the GR Gates, and the H Sequence Generator. The input signal, $2f_H$, is shaped and buffered by an A16 shaper circuit and two buffer elements to form the signal $\overline{2F_H}$. This signal is further divided by two and buffered to form HCL Enable. $\overline{2F_H}$ is inverted by a buffer element to form $2F_H$ and is combined with HCL Enable to form the 6.4 MHz clock signal denoted by HCL. $\overline{2F_H}$ is also combined with LCL Enable to form the 6.4/1022 MHz clock signal denoted by LCL. By forming clock signals in this manner, the only timing variations (or clock skew) will be the differential propagation delay through different buffer elements. A 6.4 MHz square wave is reclocked by $2F_H$ to form the F_H signal. These signals are shown in the Timing Diagram, Figure 5-76.

The following list identifies the signals of interest on this drawing.

<u>Signal Number</u>	<u>Signal Name</u>
2	$\overline{2F_H}$
4	HCL ENABLE
5	HCL
6	$2F_H$
7	F_H
9	$\overline{H_{511}}$
10	LCL ENABLE

It should be remembered that only every other H_{511} pulse will generate an LCL Enable interval.

The H Sequence Generator module contains a standard linear shift register generator of nine stages and three word detectors. The three word detectors are connected so that one has a "one" output during code bit H_{255} , one has a "one" output during code

bit H_{510} , and one has a "one" output anytime the first eight stages contain "zero." This latter word detector is used to insure that the generator will not lock up in the "all-zero" condition. H_{510} and H_{255} are used by the Code Clock Generator to generate F_L , $F_{L/2}$, $F_L \oplus F_{L/2}$, and LCL Enable as described below. This sequence generator includes provision for changing the phase of the sequence. This provision is the H Shift input. This signal line is normally held at a "zero" level, and when the signal is raised to a "one," a "zero" will be shifted into the second stage. If this signal is made a "one" for one cycle of HCL following H_{510} , the sequence generator will contain the following sequence:

H Shift	H_{N-1}	H_{N-2}	H_{N-3}	H_{N-4}	H_{N-5}	H_{N-6}	H_{N-7}	H_{N-8}	N_{N-9}	
0	0	0	0	0	0	0	0	0	1	H_{510}
1	1	0	0	0	0	0	0	0	0	H_{511}
0	0	0	0	0	0	0	0	0	0	H_0
0	1	0	0	0	0	0	0	0	0	H_{511}
0	0	1	0	0	0	0	0	0	0	H_1

It is seen that two additional states have been added to the sequence in that H_0 has been forced into the register H_{511} has been repeated. Hence H_1 appears 2 bit times later and the sequence has been delayed by 2 bits. Since the sequence length is odd, any delay from 1 to 510 bits, inclusive, may be accomplished.

H_{510} and H_{255}^* are retimed by HCL in the Code Clock Generator to become H_{511} and H_{256} respectively. The "one" to "zero" transition of F_L will coincide with the "one" to "zero" transition of H_{511} , and the "zero" to "one" transition of F_L will coincide with the "one" to "zero" transition of H_{256} . Transitions of $F_{L/2}$ will

* Note that these signals are defined to be a "one" when H_{510} and H_{255} , respectively, appear as outputs of stage H_{N-9} , and "zero" otherwise.

coincide with the "one" to "zero" transitions of H_{511} , while transitions of $F_L \oplus F_{L/2}$ will coincide with the "one" to "zero" transitions of H_{256} . Note that H_{256} , H_{511} , F_L , $F_{L/2}$, and $F_L \oplus F_{L/2}$ appear at the output terminals of register elements which are all clocked by the same HCL. H_{511} , $F_{L/2}$, and F_H are combined to form LCL Enable in a manner which will allow LCL to be coincident with the HCL pulse which caused $F_{L/2}$ to make a "one" to "zero" transition.

5.10.2.2 L Sequence Generator

The module consists of a 7 stage shift register generator with synchronous preset capability, three word detectors, and a re-timing circuit. One word detector is to prevent lock up in the "all-zero" state and detects "zeroes" in the first six stages of the register. Another word detector is connected to detect "zeroes" in the first six stages and "one" in the last stage. This state of the generator occurs during bit time L_{126} . The signal from this detector is retimed and becomes the L_{127} signal. The remaining word detector is set to detect "ones" in the first six stages and "zero" in the last stage which occurs at bit time L_{119} . When the L Search signal is "zero," this L_{119} signal will force the next state of the register to be L_{121} instead of L_{120} by causing a "zero" to be set in the first stage instead of a "one." Thus, the phase of the L sequence will change at a rate of one L sequence bit per L sequence period when the L Search signal is at a "zero" level. When this signal is at a "one" level, the L sequence phase shifting circuits are inhibited.

The synchronous preset capabilities are utilized when the EM + L SYNC signal goes to "one" or when both this signal and the L SYNC signal goes to "one." When both signals are held at a "one" level, the 7 bit word 100 000 0 is continuously set into the first through the seventh stages by LCL until both signals go to a "zero" level. This condition sets the L sequence generator, such that the first full L sequence bit after the EM + L SYNC and L SYNC signals go to a "zero," is 010 000 0 which is the L_1 bit time. In a similar manner, making only the EM + L SYNC

signal a "one" will cause the state 101 011 0 to be set into the register. The first full L sequence bit after the EM + L SYNC signal goes to "zero" will then be 110 101 1 which is the L_{75} bit time.

5.10.2.3 S-Band Data Encoder

This module contains an L Sequence Generator word detector for detecting L_{58} , three retiming circuits, and a four-stage presettable counter with logic for generating the bit sequence L_{16N+1} , L_{16N+9} , and L_{8k+1} (for $N = 0, 1, \dots, 7$ and $k = 0, 1, \dots, 15$) and the bit stream, D'.

The word detector is connected to the L Sequence Generator module to detect the bit pattern 001 110 0 which occurs during bit time L_{58} . This detector output is retimed by LCL to yield the signal called L59.

The four-stage counter is preset by L_{127} and synchronously divides the LCL rate by 16 so that the L Sequence period is divided into 7 intervals of 16 L sequence bit times each and one interval of 15 L sequence bit times.

The three word detectors attached to the counter form the three required bit sequences. The bit sequence L_{8k+1} is retimed by LCL to form the bit sequence L_{8k+2} . The bit sequence L_{16N+1} and L_{16N+9} are combined with the Data input signal according to the following equation to form the steering signal, S-D';

$$S-D' = (DATA)(L_{16N+1}) + (\overline{DATA})(L_{16N+9})$$

This signal is then retimed by LCL to form the D' signal.

5.10.2.4 Code Combiner and Buffer

This module contains the necessary logic and retiming circuits required to form the Vehicle Transmitter output code and certain timing signals required by other subsystems. \overline{L}_{N-6} is retimed by LCL, forming \overline{L}_{N-7} , and then combined with \overline{D}' to form $L_{N-7} \oplus D'$.

If it is not required to add data into the code, the \bar{D}' input signal should be wired to a "one"; while, if data is required, this signal is to be connected to the corresponding signal out of the S-Band Data Encoder.

\bar{H}_{N-8} is retimed by HCL, forming \bar{H}_{N-9} , and then combined with $F_L \oplus F_{L/2}$ to form $H_{N-9} (F_L \oplus F_{L/2})$. Now this signal and $L_{N-7} \oplus D'$ are retimed by HCL forming $L \oplus D'$ and $H(F_L \oplus F_{L/2})$ and then combined to form the final code, $L \oplus H (F_L \oplus F_{L/2}) \oplus D'$. This signal is again retimed by HCL and then used as a steering signal for the final output flip-flop (an A33 hybrid circuit). F_H is used as a steering signal for another A33 circuit, and both of these high speed flip-flops are clocked by $\overline{2F_H}$ to obtain the required time relation between clock and steering signals. Note that this reclocking of the transmitter clock introduces a delay of two H Sequence bits plus a time interval defined as the interface delay time. The phase relationship between the transmitter code output and the F_{HS} output (a 6.4 MHz square wave) is such that F_{HS} is "zero" during the first half of every H sequence bit of the output code.

In addition to these outputs, L_{126} is retimed and buffered to form L_{127} outputs for various other subsystems.

5.10.3 Discrete Component Circuits

The only discrete components in this subsystem are two resistors. The first (R1) is a 680 ohm resistor and is used as a series current limited from the $+V_{CC}$ buss. The second (R2) is a 120 ohm resistor and is used to load the output of a Philco buffer. This buffer was originally loaded with only three unit loads and resulted in an excessive voltage swing. The finite rise and fall times of the buffer caused the $VT-\overline{2F_H}-I$ signal to be unsymmetrical at the half-volt level. The addition of the load resistor restored the $VT-\overline{2F_H}-I$ signal's symmetry.

5.10.4 Test Results

The rise and fall times of the VT-F_{HS}, VT-Z, and VT-Z̄ signals as well as the time interval measurement T-1 was difficult to measure due to jitter of the scope trace. This jitter varied between ±1 and ±2 nanoseconds and was the dominate factor in measurement accuracy. Because of this, the time measurements were made on the conservative side.

Time interval measurements T-2, T-3, T-4, T-5 and T-6 were made with an accuracy of ±5% which is more than adequate for the gross type measurement required.

The supply voltage variations actually used during the input signal dynamics and supply voltage variation test was ±3.35 vdc and ±3.55 vdc. In addition, at both high and low voltage extremes the peak-to-peak amplitude of the VT-2f_H signal was varied ±10%. No change in phase between the VT-F_{HS} and VT-Z signals was observed at any of the voltage extremes. Due to the jitter, however, this phase measurement could only be made with an accuracy of ±1 nanosecond.

On future units it is suggested that R1 resistor be incorporated into one of the microharness modules and that the Philco I/C's used for 12.8 MHz signals be replaced with I/C's having less propagation time. This will eliminate the necessity for R2 resistor.