Ka BAND SOLID STATE TRANSMITTER/DRIVER

Final Report

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(See p 2)

Sylvania Electronic Systems
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TABLE OF CONTENTS

TABLE OF CONTENTS - Continued

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS - Continued

1.0 INTRODUCTION

1.1 Program Objective

The objective of this program was to design, develop and fabricate a prototype, space-qualified, model of a solid state source producing 100 mw cw power at 35 GHz. The source must have a long term stability of ±1 part in 10^7 while traversing the thermal limits of -20°C to +85°C, and an output signal/noise ratio of 60 dB. Below is a summary of the design specifications.

Electrical

Output Frequency	35 GHz
Output Power	100 mw at 50° ambient 50 mw over environmental and input voltage limits
Supply Voltage	36 VDC ±4.75 V
Input Power (primary)	90 watts maximum
Frequency Stability	
Long Term	5 part in 10^8 at 50°C
Short Term	1 part in 10^6 over 1 second under worst environment
Traversing Thermal Limits	±1 part in 10^7
RF Bandwidth	.2% minimum
Modulation	FM - 400 cps to 100 kHz 125 kHz/volt
Spurious Frequencies	40 dB S/N within ±16 kHz of 35 GHz output
	60 dB S/N beyond ±16 kHz but within 3 dB passband of final multiplier
R.F.I.	MIL-I-6181D
Reliability - MTBF	10,000 hours at 50°C 3,600 hours at -20°C to +85°C

Environmental

Temperature	-20°C to +85°C
Acceleration	10 g for 3 minutes in both directions of three mutually perpendicular planes
Humidity	No effect from external water or frost
Random Vibration	20-59 cps 0.04 g^2/cps 59-126 cps +9 dB/octave 126-700 cps 0.40 g^2/cps 700-900 cps -18 dB/octave 900-2000 cps 0.09 g^2/cps
Vacuum and Pressurization	Leakage no greater than 1.0 psi/24 hours with internal pressure 15 PSIg and external vacuum of 1.5 x 10^{-6} mm of mercury.
Vibration Transmissibility	Vibration level on components shall not exceed 5 times input vibration level.
Sinusoidal Sweep	Two sweeps in each axis (1 increasing, 1 decreasing) at 1 octave per minute to locate internal resonances.
	5-48 cps at 0.125 inches double ampl. 48-165 cps at 15.0 g peak 165-2000 cps at 10.0 g peak

Physical

Housing - Pressurized, of aluminum or magnesium

Dimensions - 10 x 10 x 6 inches maximum

Weight - 12 pounds maximum

1.2 Applications

The source was to be used in conjunction with a millimeter wave TWT to provide a communications link for Saturn V spacecraft boosters. The development was being performed under Contract NAS 8-20599 for the Marshall Space Flight Center,

National Aeronautics and Space Administration. The purpose of the link was to provide reliable radio transmissions through the ionized gas cloud produced by the ignition of retro-rockets at booster staging. Millimeter wave signals are expected to penetrate this plasma, whereas lower frequency signals experience a radio blackout under this condition.

1.3 Summary of Result

One engineering model Ka Band Solid State Transmitter/Driver was built and delivered to the Marshall Space Flight Center, National Aeronautics and Space Administration, Huntsville Alabama. A photograph of this unit is shown in Figure 1. The unit produced a stable crystal-controlled output at approximately 35 GHz of 100 mw. The total DC input power required was 60 watts. The spurious and noise outputs were at least 30 dB below the carrier at 35 GHz. The unit contained an FM modulation capability. The approximate dimensions of the unit was 8" wide x 10" long x 5.5" high and the weight was approximately 18 pounds.

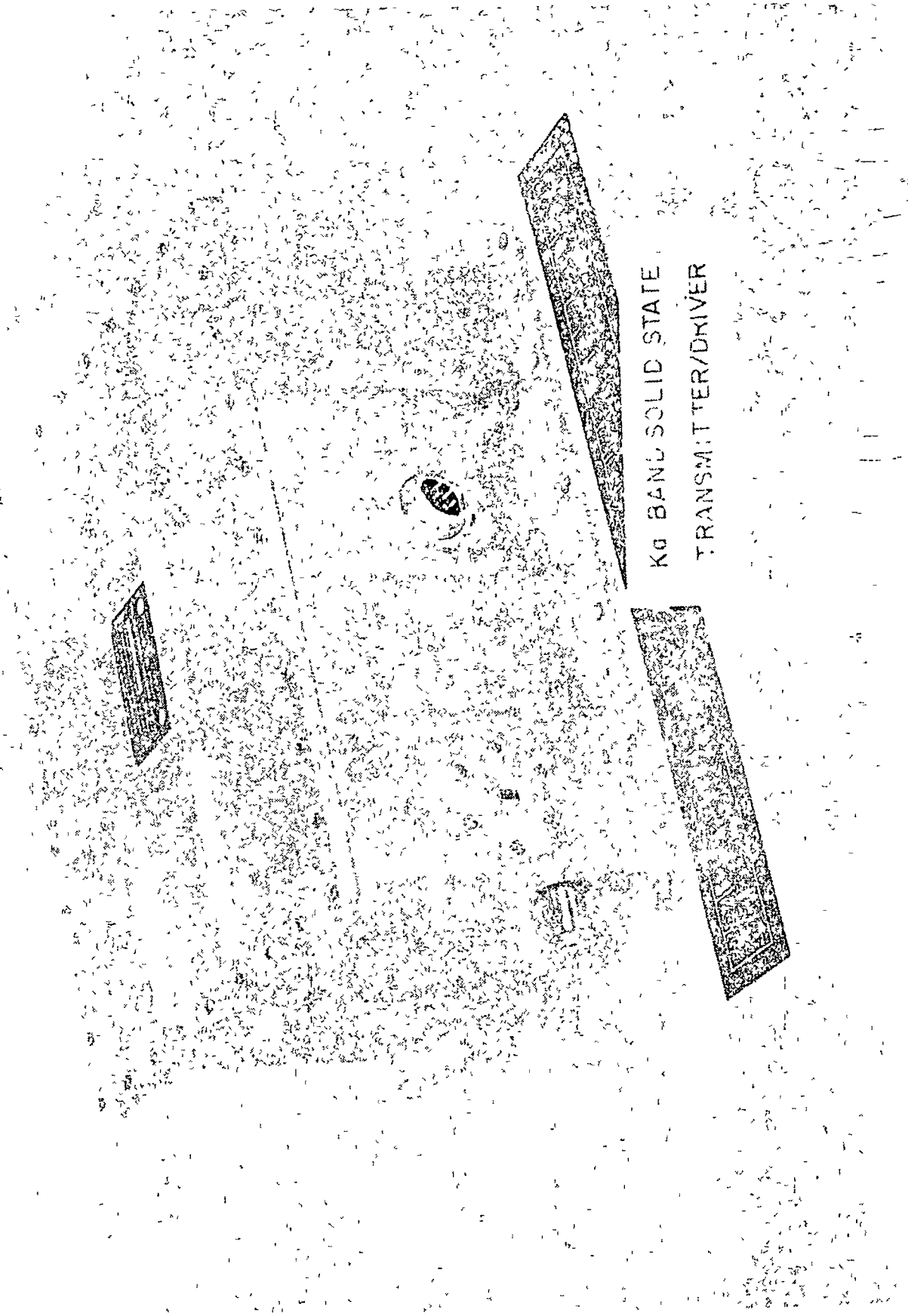


Figure 1

Engineering Model, 35 GHz Transmitter

2.0 TECHNICAL DISCUSSION

2.1 Basic Theory of Operation

The Ka-Band transmitter/driver consists of a series of semiconductor amplifiers and multipliers which produce a stable crystal-controlled drive power of approximately 18 watts at 325 MHz. This drive is then applied to a chain of varactor multipliers to a frequency of 35 GHz. The total frequency multiplication factor is 864. Printed-circuit, coaxial, stripline, and waveguide techniques are used for the various amplifiers and multipliers. A phase modulation exciter is included in the source for telemetry signals.

2.1.1 Description of Block Diagram

As shown in the block diagram of Figure 2, the multiplier chain starts with a crystal controlled oscillator operating at 40.5 MHz. A bandpass filter of 0.02% bandwidth is provided within the oscillator module to limit the noise bandwidth. Following the oscillator, a phase modulator is incorporated to allow frequency modulation of the output. The frequency response of the modulator is 400 Hz to 100 kHz, and it will produce a maximum deviation of ±215 kHz from the 35 GHz output frequency.

A limiter-amplifier follows the modulator to remove any amplitude modulation produced in the modulator.

After limiting, an AGC controlled driver amplifier is used to drive a X4 varactor multiplier to produce a stable 20 mw output at 162 MHz. An m-derived bandpass filter is then employed to suppress the third and fifth harmonics of 40.5 MHz created by the X4 multiplier. Adequate suppression of the spurious harmonics is especially important in the lower end of the chain since amplification

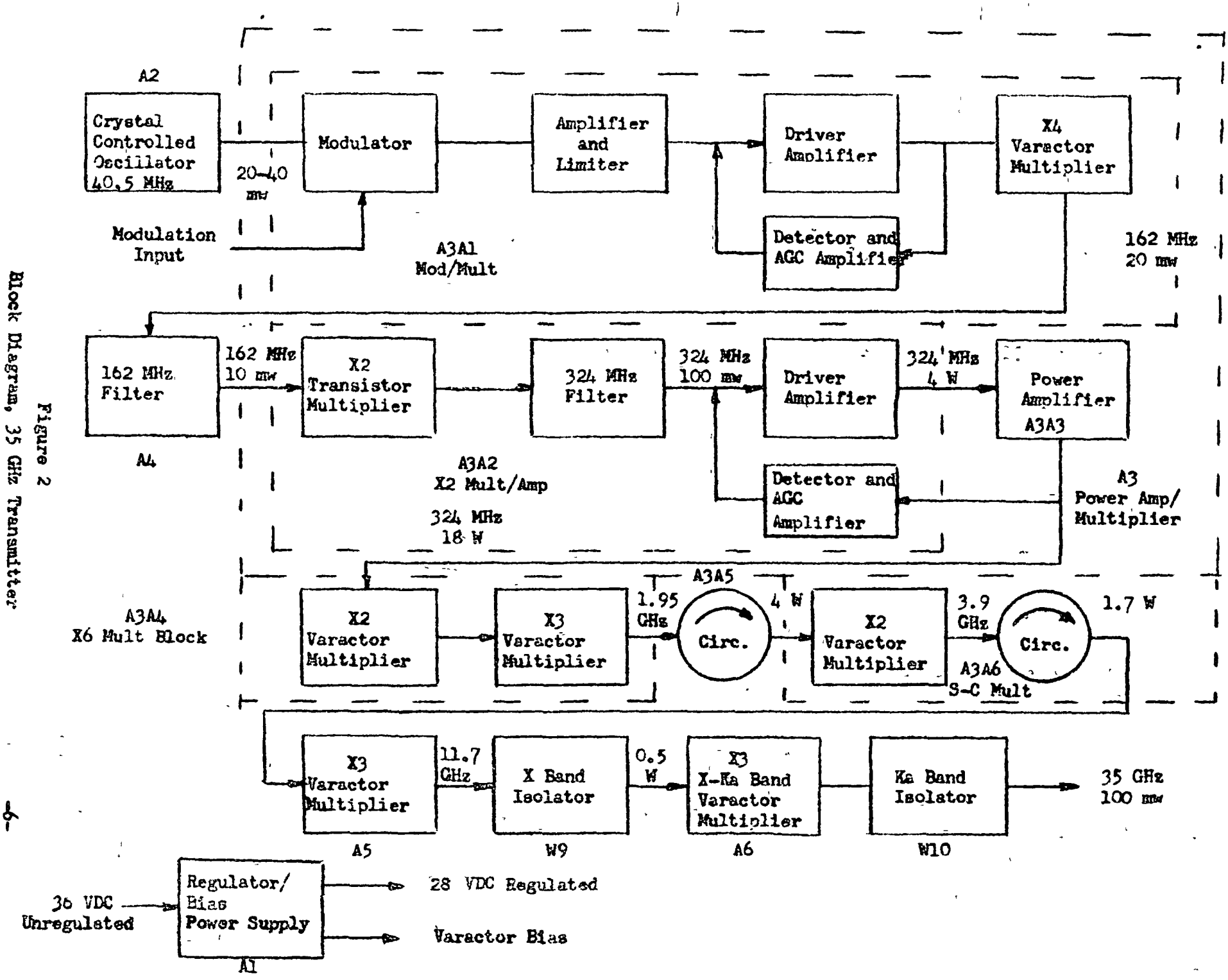


Figure 2
Block Diagram, 35 GHz Transmitter

of these (spurious enhancement) is a function of the square of the multiplication factor of the multiplier chain.

A transistor doubler is then employed to multiply the frequency to 324 MHz and is followed by a 2 section bandpass filter for additional harmonic suppression.

The resulting 324 MHz, 100 mw signal is then amplified to 18 watts by a linear driver and power amplifier string. An AGC loop around this amplifier insures a constant drive to the following multiplier regardless of temperature variations.

Following the power amplifier, two lumped element varactor multipliers, a doubler and a tripler, are used to multiply the frequency to 1.95 GHz. A stripline circulator is used to isolate these multipliers from the following stripline S-C band doubler/circulator module. The output of this module is 3.9 GHz at 1.7 watts.

A transition to Ku Band waveguide is accomplished in the following C-X band tripler. The output of this unit is over 500 mw at 11.7 GHz. A waveguide isolator is used between this multiplier and the final multiplier in the chain. This final multiplication from 11.7 GHz to 35 GHz is accomplished by a cavity type tripler which provides 125 mw output power. With the inclusion of a final waveguide isolator and the output waveguide, a power output of 100 mw at 35 GHz is available at the output of the unit.

Under normal operating conditions, the source described will consume 60 watts of primary power from an unregulated 36 VDC supply in the booster. A regulator circuit has been incorporated in the unit to provide the stable 28 VDC power source required for operation of the multiplier chain.

2.2 Component Description

2.2.1 Regulator/Bias Power Supply (A1)

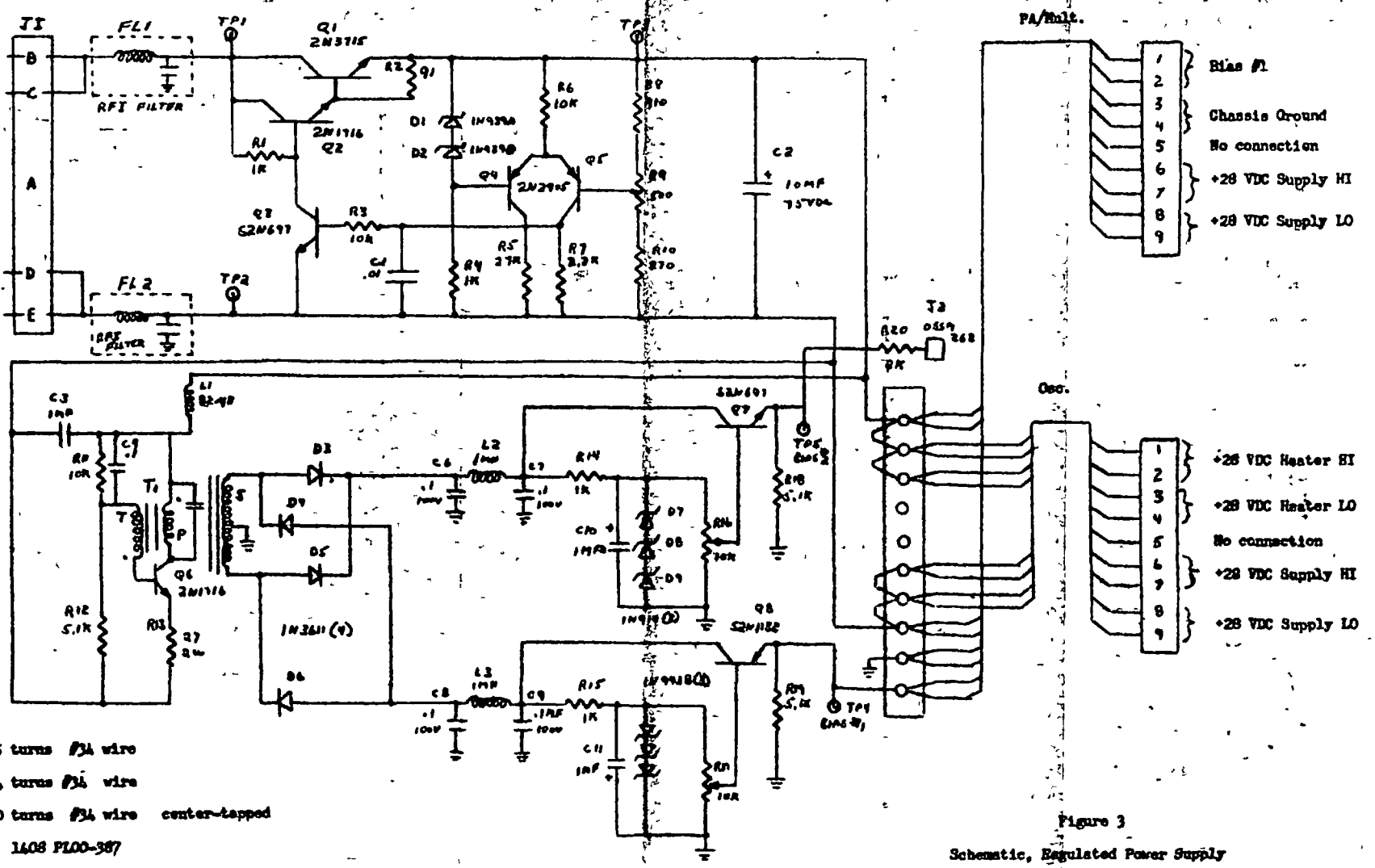
This module provides the regulated 28 VDC secondary power for the transistor amplifier circuits and bias voltages for two varactor multipliers. A simple series regulator is employed to regulate the 36 ±4.75 VDC primary power to 28 VDC. To meet the specified grounding requirements, both sides of the input power lines are isolated from chassis ground and EMI filters are employed.

Two of the varactor multipliers in the source originally required an adjustable negative bias voltage of 30 VDC maximum. Since these bias supplies had to be referenced to chassis ground, they were developed from a blocking oscillator power supply operating from the 28V source. The output of the oscillator is taken from a secondary winding referenced to chassis ground and is rectified and filtered. This DC output is then zener stabilized and then applied to an emitter follower voltage control circuit. The two voltage outputs are stable to within ±0.3V over a temperature range of -20 to +100°C for load variations of 0-8.5 mA.

The main 28V regulator controls the voltage to ±0.75V over the combined input voltage range of 30 ±4.75 VDC, a load current range of 0 to 2.5 amps, and a temperature range of -20 to +100°C. Complete performance curves are shown in Figure 4. A schematic of the regulated power supply is shown in Figure 3.

2.2.2 Crystal Oscillator (A2)

The crystal oscillator assembly is the basis for the highly stable output at 35 GHz. The frequency of this oscillator is 40 MHz and is then multiplied 864 times to obtain the 35 GHz frequency. The module consists of a crystal controlled oscillator followed by a tuned buffer/driver amplifier stage and a final narrow band



T_1 P - 15 turns #34 wire

T - 4 turns #34 wire

S - 80 turns #34 wire center-tapped

Elna Ferrite Core 1408 P100-3E7

Bobbin 1811P1D

Figure 3

Schematic, Regulated Power Supply

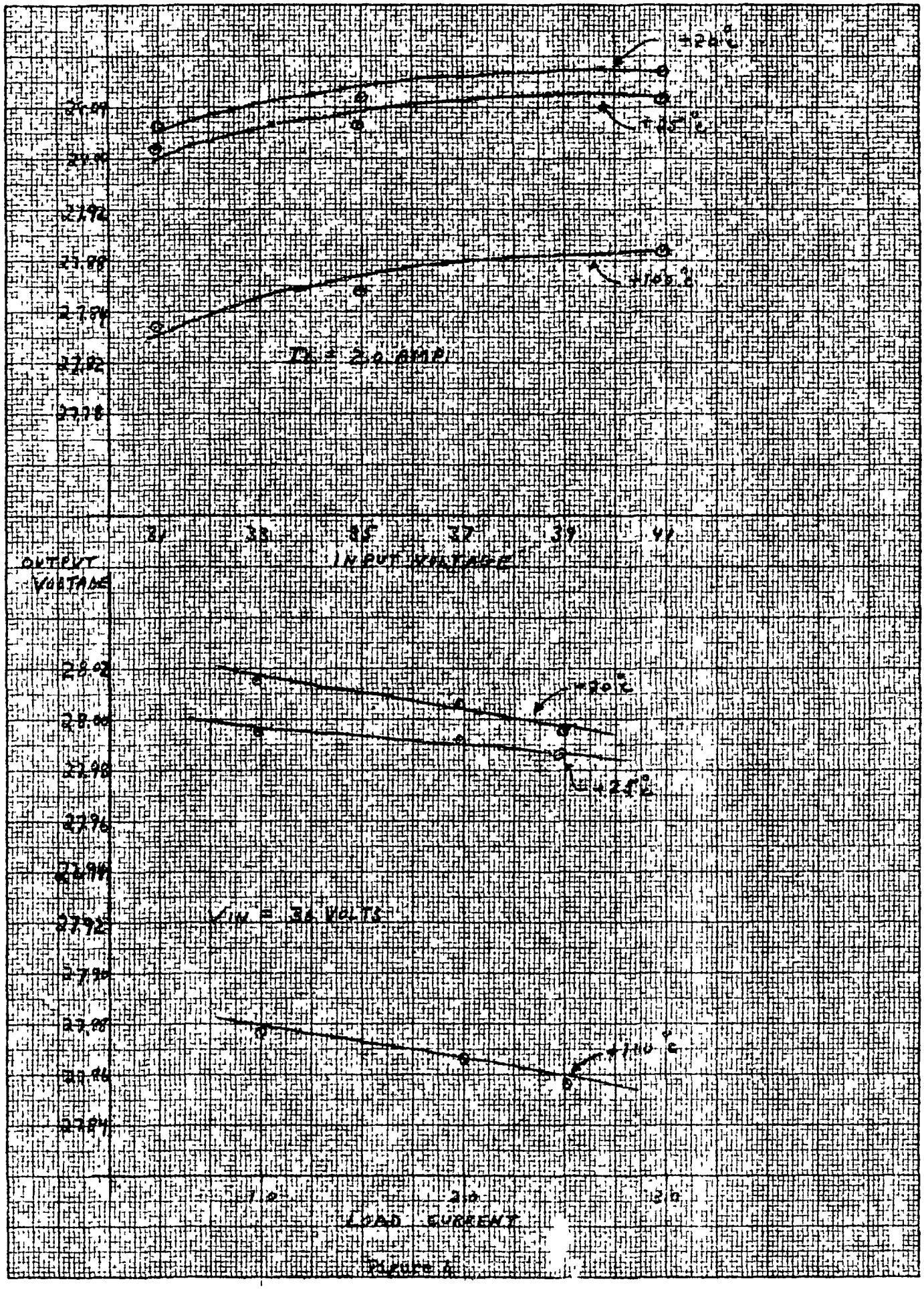


Figure 4

Performance of Power Supply Over Temperature

crystal filter. Figure 5 shows a schematic of the final oscillators assembly. The crystal filter is incorporated to reduce the noise output to a value less than 100 dB below the 40 MHz signal amplitude. The overall stability is achieved by operating the oscillator circuit in a proportionally controlled oven. The electrical performance specifications of the crystal oscillator assembly are as follows:

Frequency	40.509259 MHz
Frequency trimming	±10 parts in 10^6
Long term frequency stability	
at 50°C	5 parts in 10^8 per day
Short term frequency stability	
at 50°C	1 part in 10^8 per 10 seconds
Frequency stability while traversing thermal limits (-20°C to +85°C)	±1 part in 10^7
Output power	20-40 mw into 50 ohms
Noise output	100 dB below output, maximum

2.2.3 Amplifier/Multiplier Assembly (A3)

2.2.3.1 Modulator/Multiplier (A3A1)

(A) 40 MHz FM Modulator

The complete modulator consists of a 10 dB pad, a phase modulator, a limiter, and an audio amplifier and integrator. These elements are shown in block diagram form in Figure 6 and schematically in Figure 7.

The amount of power the phase modulator can handle linearily will depend almost completely on the bias level. As negative bias on the varactor diodes

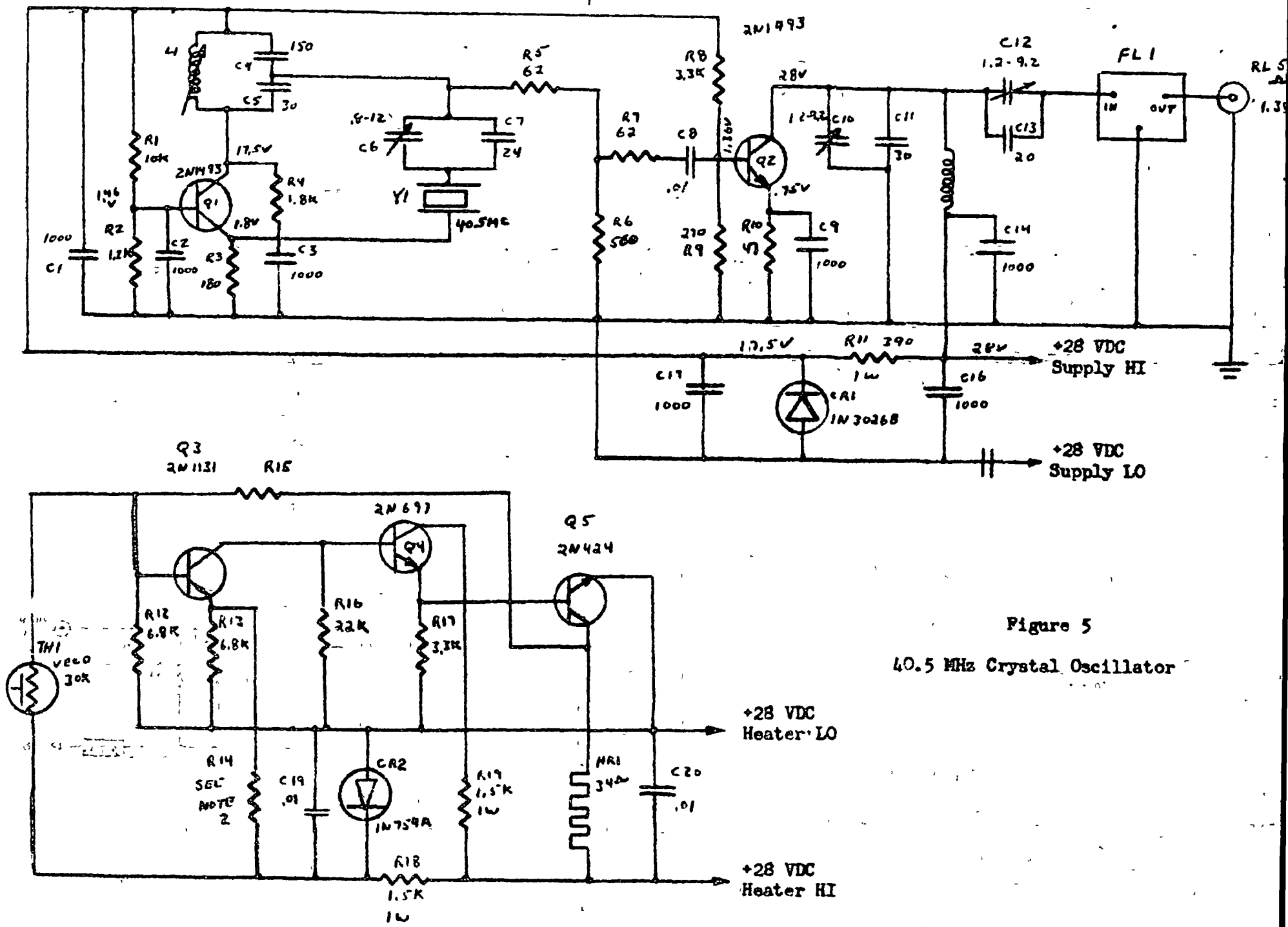


Figure 5

40.5 MHz Crystal Oscillator

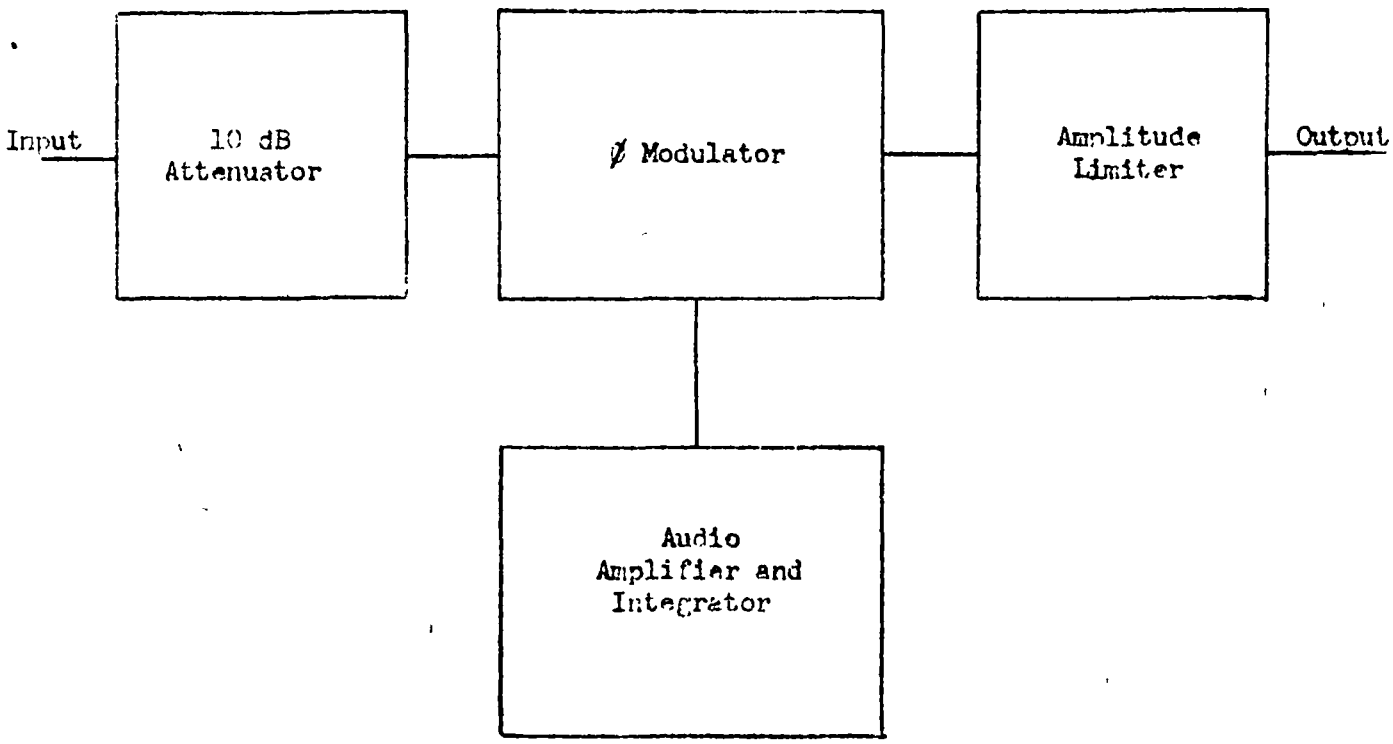
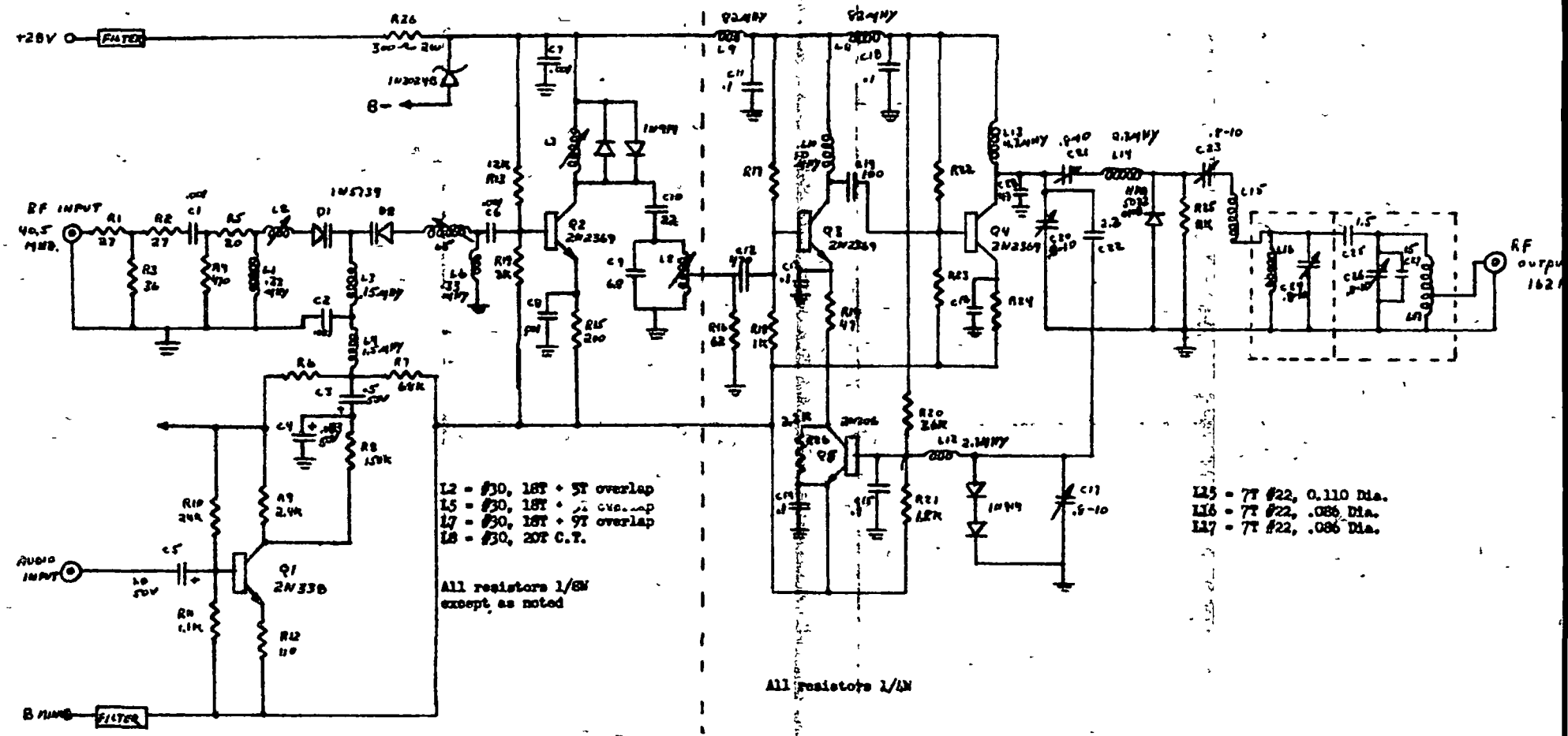


Figure 6

Block Diagram, 40 MHz FM Modulation

Buffer Amplifier and Modulator

Amplifier and X4 Multiplier



L2 = #30, 18T + 5T overlap
L5 = #30, 18T + 5T overlap
L7 = #30, 18T + 9T overlap
L8 = #30, 20T C.T.

All resistors 1/8W except as noted

All resistors 1/4W

L25 = 7T #22, 0.110 Dia.
L16 = 7T #22, .086 Dia.
L17 = 7T #22, .086 Dia.

Figure 7

Schematic, FM Modulator and X4 Multiplier

increases, the power handling capability increases, but the modulation sensitivity decreases because of the decrease in capacitance. Thus, a compromise is required. In this modulator a bias level of -6V was used limiting input RF level to about 0 dBm. Since the RF level available is +13 dBm, a 13 dB pad is required ahead of the modulator. This attenuator is a symmetric resistive T with 50 ohm input and output impedances.

The phase modulator consists of a pair of resonant circuits made up of the varactor diodes and associated tunable coils. Modulation voltages are superimposed on the DC bias voltage shifting the center frequency of these resonant circuits. Such a shift produces changes in the phase characteristics thereby changing the phase of the carrier. When modulating voltage is small with respect to the bias, the modulator operates in a linear region of phase change. Phase deviation is proportional to both modulating voltage and frequency in this type of modulator.

To obtain true frequency modulation, that is, deviation dependent only on the modulating voltage, an integrator is inserted in the modulation line. This integrator is an R-C network located in the collector circuit of an audio amplifier which provides an 18 volt peak to peak audio signal for a 1.2 volt peak to peak applied signal.

Because of the tuned circuit nature of the phase modulator, both phase and amplitude modulation are introduced. The amplitude modulation is undesirable in many respects so a limiter follows the modulator. It consists of a transistor amplifier and a pair of silicon diodes placed in the collector circuit. Limiting action is obtained at a modulator input level of -5 dBm.

Deviation and linearity of the modulator were measured with a Marconi TF 791D deviation meter for modulating frequencies up to 35 kHz. Above 35 kHz

a Hewlett Packard spectrum analyzer was utilized. Figure 8 shows the deviation versus modulation frequency for a fixed modulation drive level. Figure 9 shows the deviation as a function of modulation drive level at 30 kHz, a typical curve. Since the deviation meter only measures modulation frequencies less than 35 kHz, the spectrum analyzer was used to check deviation above 35 kHz. On the analyzer, the magnitude of the carrier and sidebands determines the modulation index and, therefore, the deviation. The modulation index, β, is the argument of the Bessel function $J_o(\beta)$ or $J_1(\beta)$ corresponding to carrier magnitude and first sideband magnitude respectively. Table I shows the variation of β as a function of modulation frequency when a β of 0.5 is set up at 30 kHz. Modulation voltage was held constant during this test. When operated as a true frequency modulator the results shown in Table II are obtained. Above 35 kHz the modulation voltages are too small to show any sidebands on the analyzer. The data shown was obtained with the deviation meter. Table III shows the variation of deviation with temperature.

(B) X4 Multiplier

The X4 multiplier following the modulator consists of a step recovery diode driven by an AGC controlled two stage amplifier. A double tuned resonant cavity on the output of the step recovery diode passes the 4th harmonic of 40 MHz and rejects all other harmonics. Further rejection to 100 dB is provided by the following module (A4), a 162 MHz filter. AGC control was built into the driving amplifier to produce a more constant output power level. The performance of the step recovery diode is much improved when driven by a more constant power over the temperature range. A schematic of this circuit is shown in Figure 7. The performance of the circuit over temperature is shown in Figure 10.

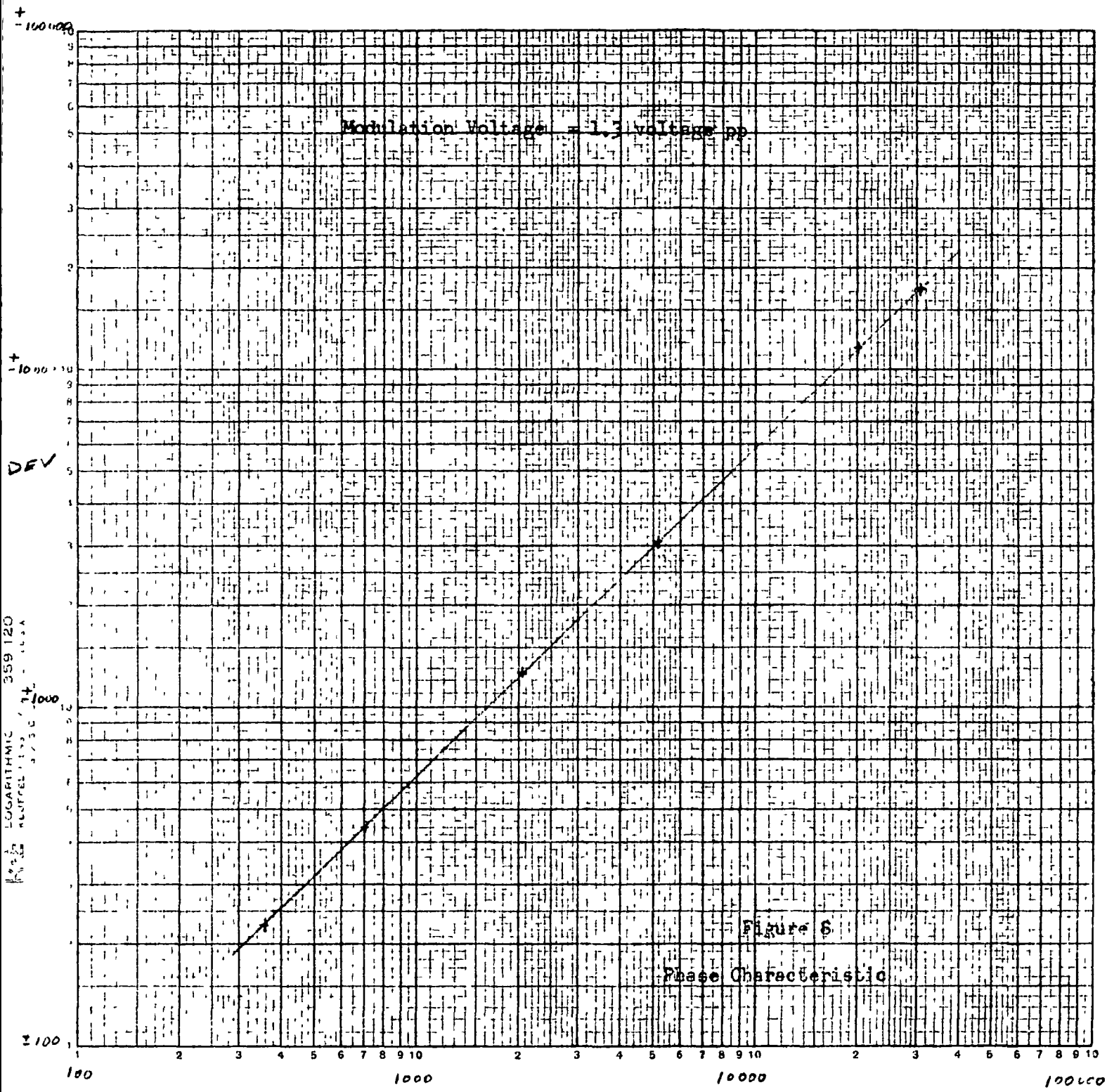


Figure 6

Phase Characteristic

Figure 9

Deviation vs Modulation Voltage

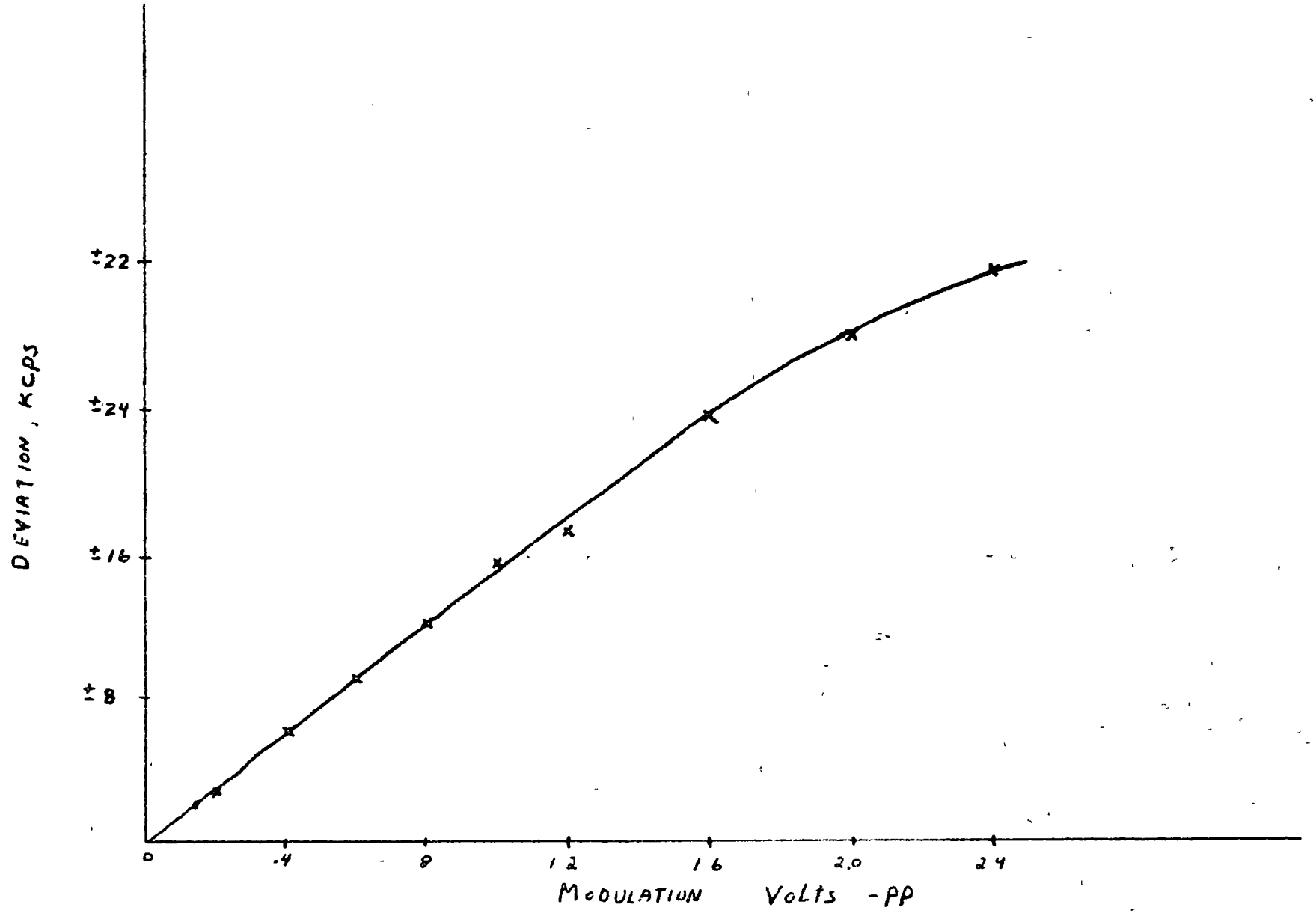


Table I

Variation of β With Modulating Frequency

Set up for β = 0.5 at 30 kHz on deviation meter

$J_o(\beta) = .94 \quad J_1(\beta) = .25$ on analyzer

Modulating Frequency	$J_o(\beta)$	$J_1(\beta)$
40 kHz	.93	.24
50 kHz	.93	.24
75 kHz	.93	.24
100 kHz	.93	.24

Table II

Frequency Modulated Deviation vs Modulating Frequency

Modulating Frequency cps	Deviation cps	$\beta = \frac{\text{dev.}}{f_m}$
300	±250	.835
400	±250	.625
500	±250	.500
750	±250	.333
1000	±250	.250
2000	±250	.125
5000	±250	.050
7500	±250	.033
10000	±250	.025
20000	±250	.012
35000	±250	.007

Table III

Deviation vs Modulating Voltage Over Temperature

Modulation p-p Voltage	-20°C Dev. (kHz)	0°C Dev. (kHz)	20°C Dev. (kHz)	40°C Dev. (kHz)	60°C Dev. (kHz)	80°C Dev. (kHz)	100°C Dev. (kHz)
0.14	2.20	1.9	1.86	1.80	1.54	1.26	
0.2	3.20	2.8	2.82	2.58	2.22	1.66	
0.3	4.74	4.2	4.12	3.90	3.40	2.56	
0.4	6.20	5.7	5.6	5.20	4.44	3.42	
0.6	9.4	8.2	8.2	7.80	6.7	5.0	1.2
0.8	12.6	10.8	11.1	10.3	9.1	6.8	1.8
1.0	15.9	14.6	14.2	13.2	11.6	8.3	2.2
1.5	22.7	21.0	21.0	19.8	18.0	12.8	4.4
2.0		28.8	27.6	26.1	24.3	17.7	8.2
2.5		35.4					

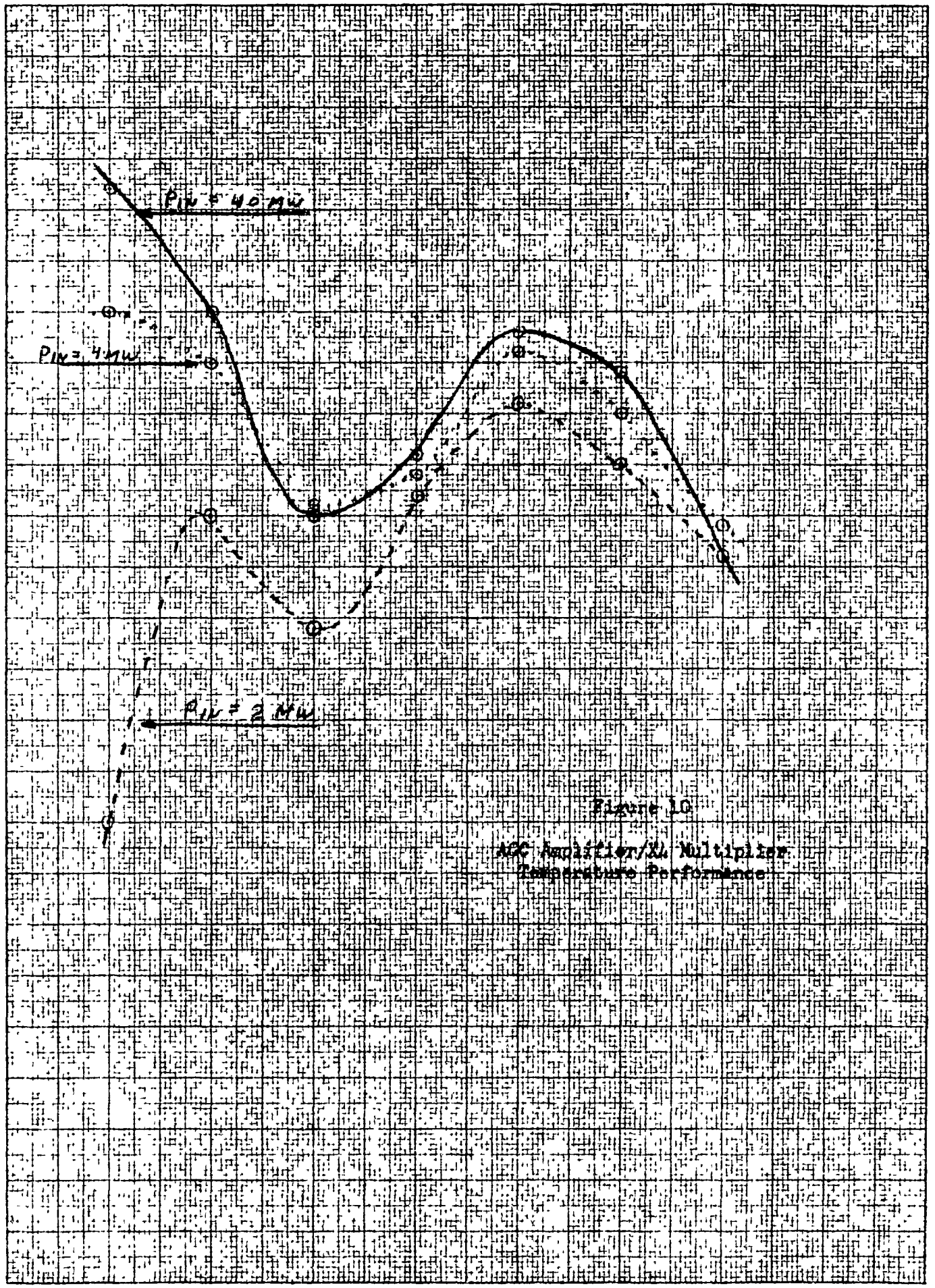


Figure 10

APC Amplifier/XL Multiplier
Temperature Performance

2.2.3.2 X2 Multiplier/Driver Amplifier

(A) Breadboard

This circuit consists of a transistor doubler (2N4429) and a 2 section bandpass filter, the output of which drives a two stage driver amplifier utilizing a 2N4429 and a 2N4431 transistor as shown in Figure 11. The doubler amplifies and multiplies to 524 MHz from 162 MHz producing an output of 80 mw with a conversion gain of 9 dB. The filter section provided better than 30 dB rejection to the 162 MHz side bands. Figure 12 shows the power output variation over temperature.

The Driver section consists of 2 amplifiers, the first class A, and second class SB (signal biased), having an overall gain of about 20 dB. The amplifier was designed on a broad bandwidth basis to improve stability over temperature. To obtain the bandwidth, special matching was required on the input of the 2N4431 or output stage. A quarter wave matching impedance transformer was used which consisted of a piece of 22 ohm coaxial transmission line. A pin diode was added to the input side of the 2N4429 with a control transistor to provide an eventual AGC control around this driver section and the final power amplifier. Data on the complete AGC performance will be discussed later. The temperature performance with no AGC control is shown in Figure 13.

(B) Final Model

A final model of the X2 multiplier and driver was laid out in the allocated space as shown in Figure 14.

Printed circuit board design was used for this circuit as well as for all the other low frequency transistor circuits. The circuit was modified slightly and the schematic is shown in Figure 15. The main modification that was made was

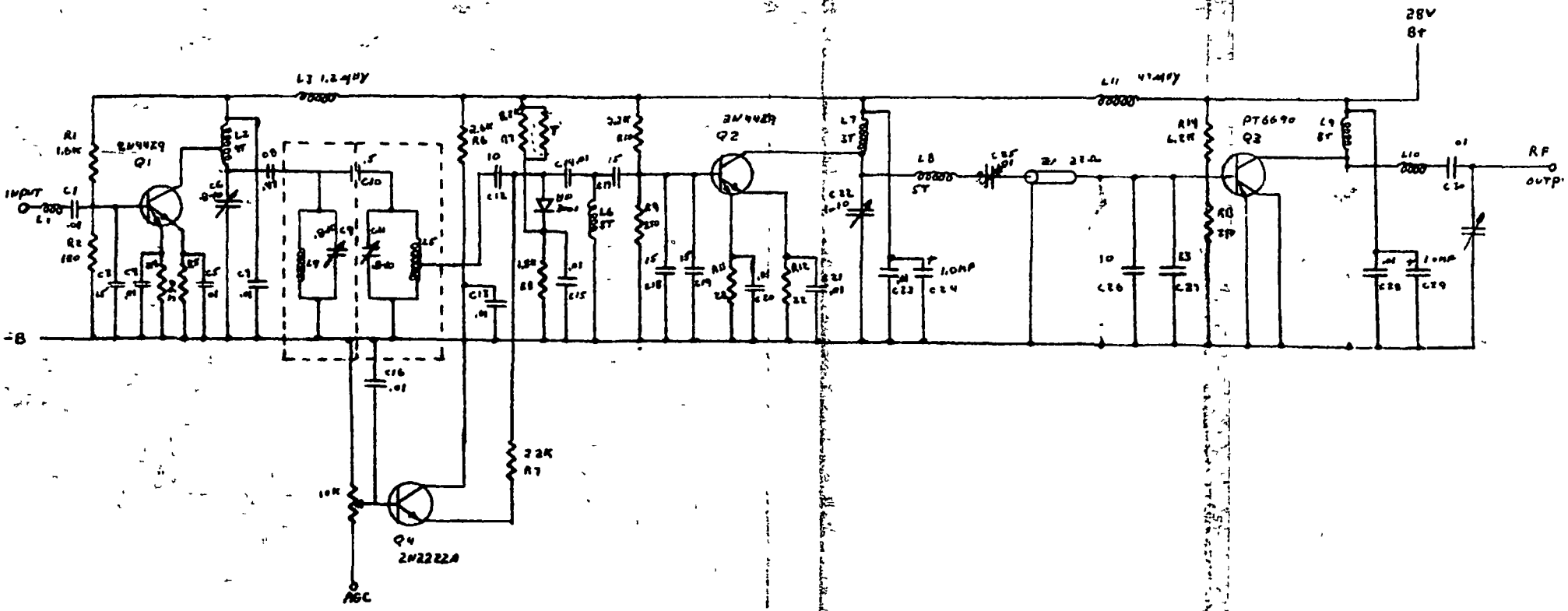


Figure 11

Schematic, X2 Multiplier/Driver Breadboard

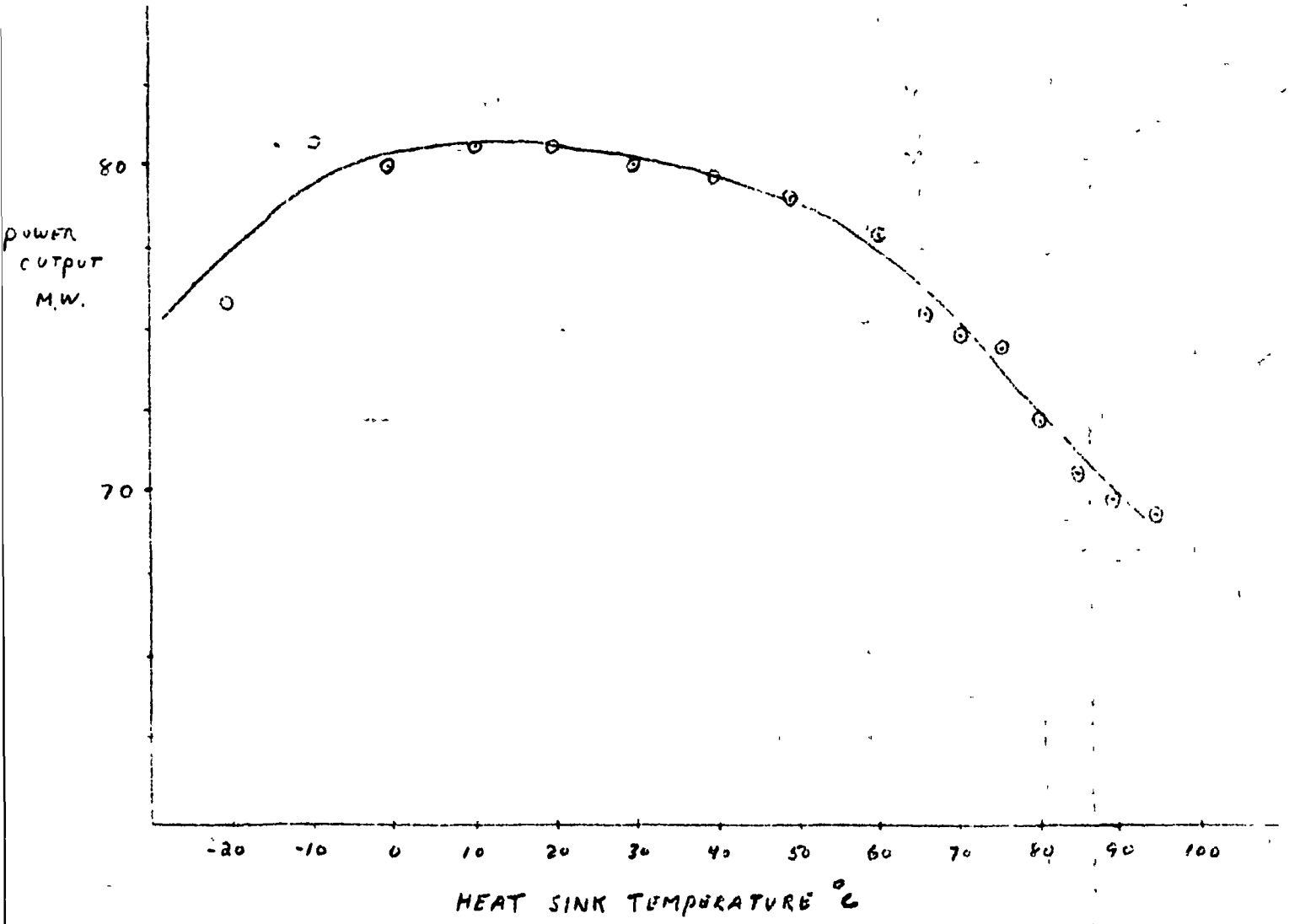


Figure 12

162-324 MHz Doubler, Power Output vs Temperature

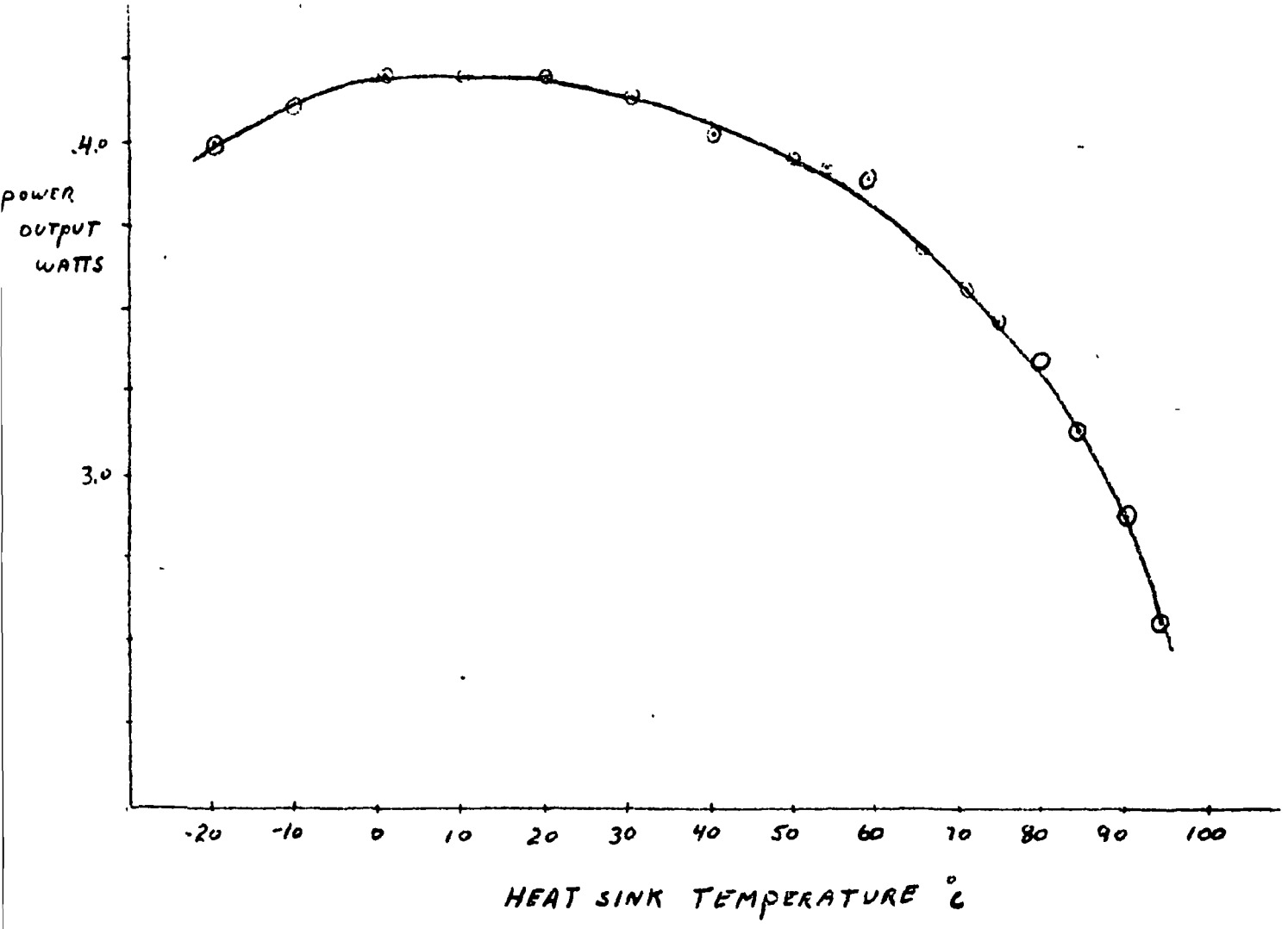


Figure 13

325 MHz Driver, Power Output vs Temperature

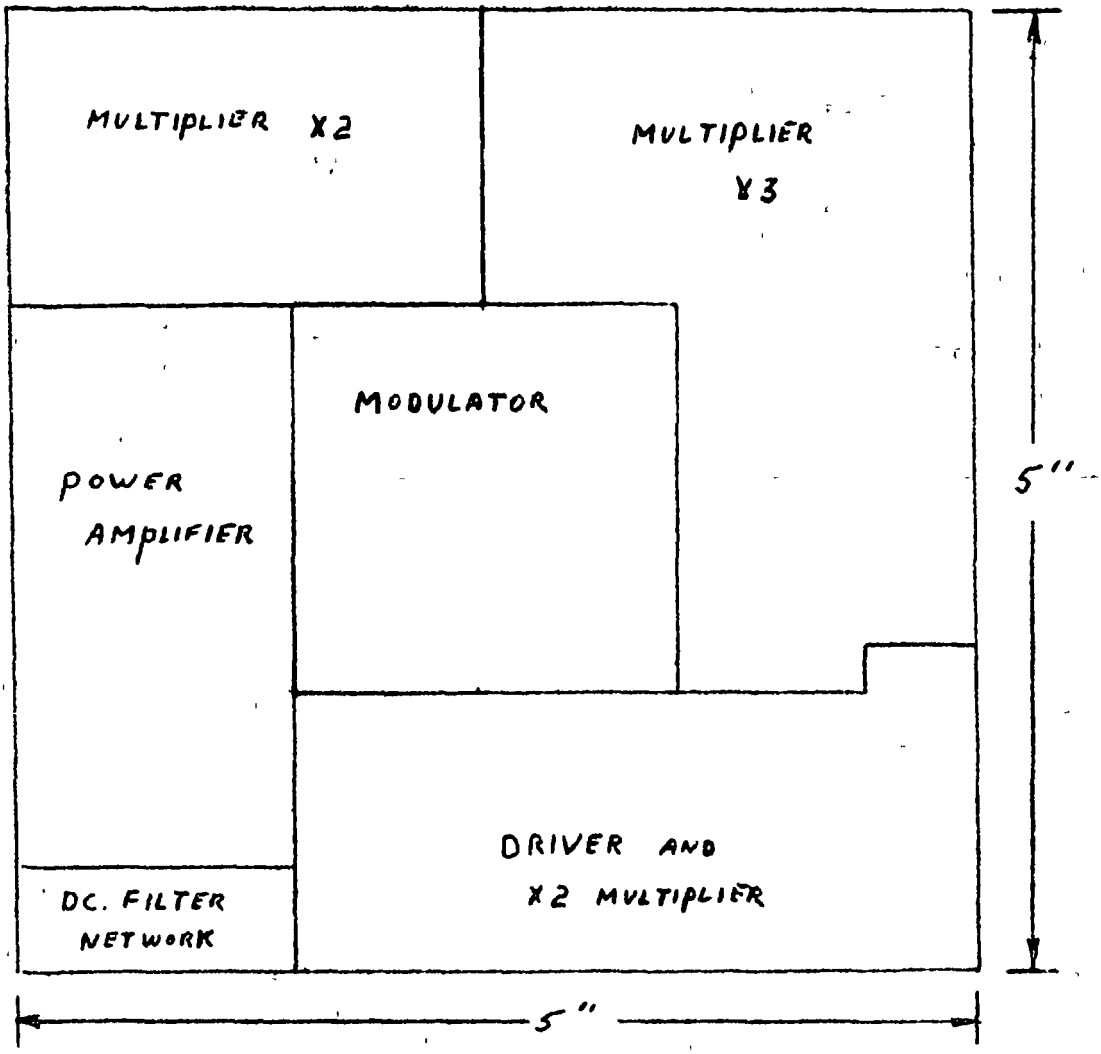


Figure 14

Module Layout of Complete Power Amplifier/Multiplier (A3)

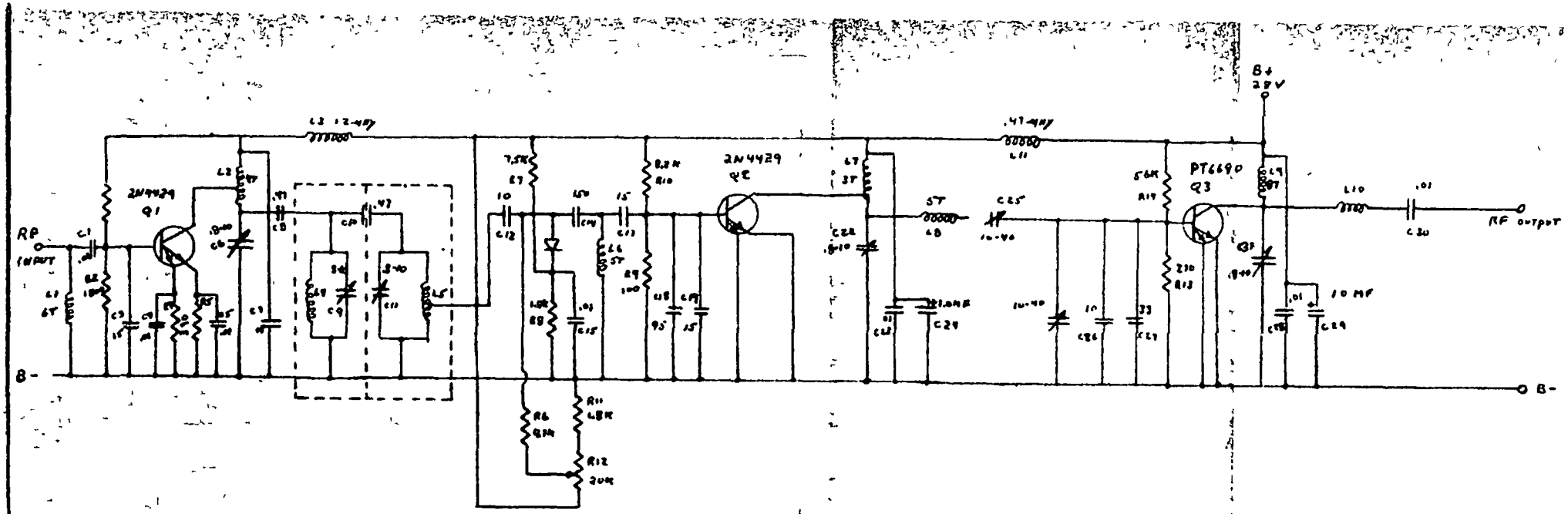


Figure 15

Schematic, Final Model - X2 Multiplier/Driver

to narrow band the coupling circuits between stages which helped eliminate spurious problems associated with broadband amplifiers, since broad bandwidth was not necessary. The performance was slightly better than the breadboard. The doubler and driver produced 100 mw at 324 MHz for 10 mw drive. The driver output was 8 watts maximum and could be varied down to 0.5 watts without any spurious breakup.

2.2.3.3 Power Amplifier (A3A3)

(A) Breadboard

The breadboard model was designed on the same broadband basis as the driver. It contained two transistors (2N4431) in parallel with special quarter wave matching lines on the input and output as shown by the schematic in Figure 16. The two transistors were operated grounded emitter in class C operation. The amplifier yielded an output in excess of 20 watts with a gain of 7 dB. The temperature performance of the amplifier is shown in Figure 17. The power drop off with temperature is in itself quite good, only 1.2 dB. However, since the multiplier chain following the power drop has a similar curve only much more severe, at least a flat power output from the power amplifier would be desirable and one which steadily increases with temperature would be ideal. An AGC loop was implemented from the power amplifier output back to the input of the first stage of the driver in an attempt to control the power output curve. After considerable testing and many variations of this AGC circuit the power output curve was successfully shaped to that desired as shown in Figure 18.

(B) Final Model

The breadboard unit performed quite successfully as long as it was properly loaded at all times. It was found, however, that a multiplier does not provide a good load under all conditions of drive, frequency and temperature.

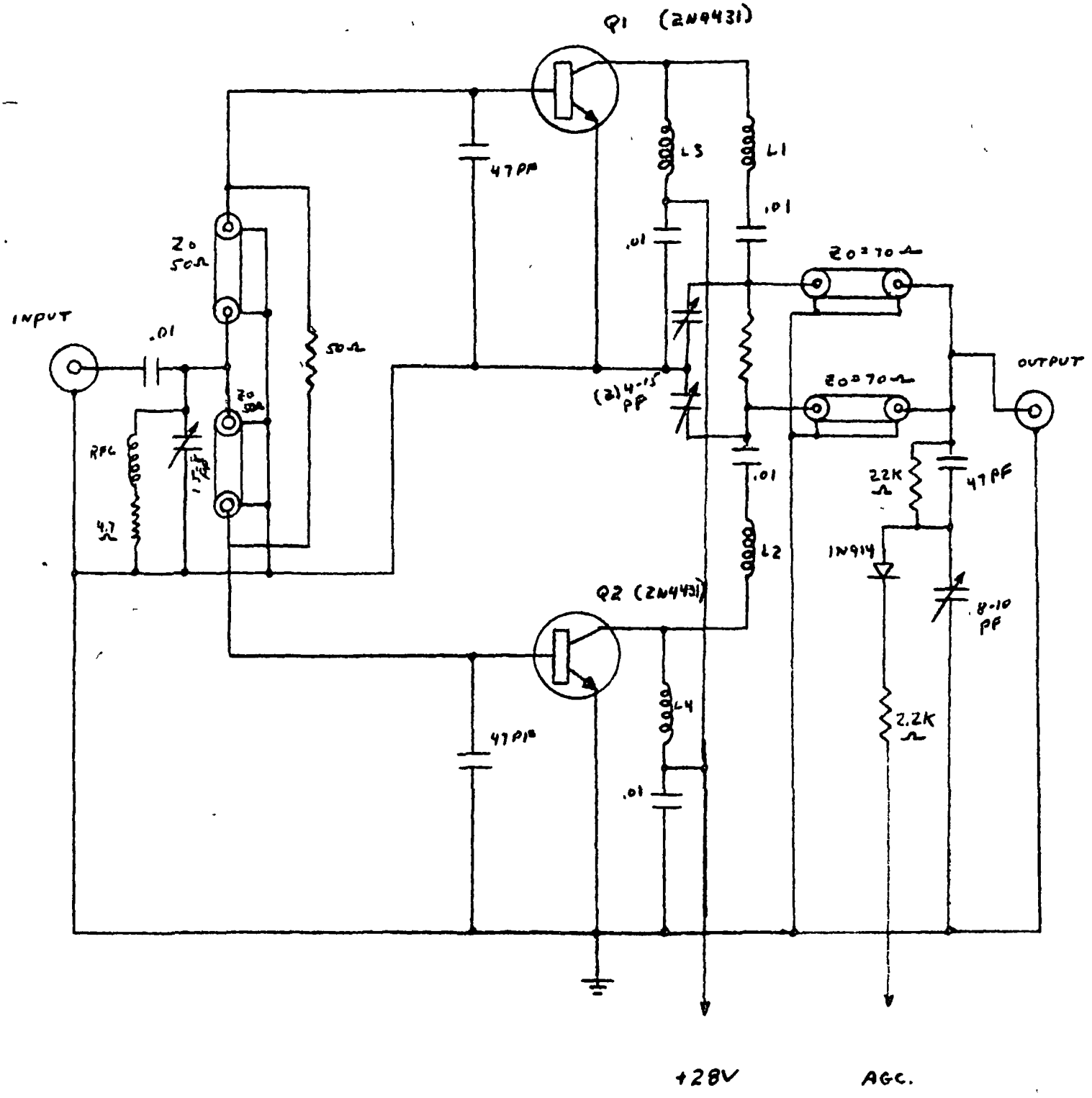


Figure 16

Schematic, Power Amp Breadboard

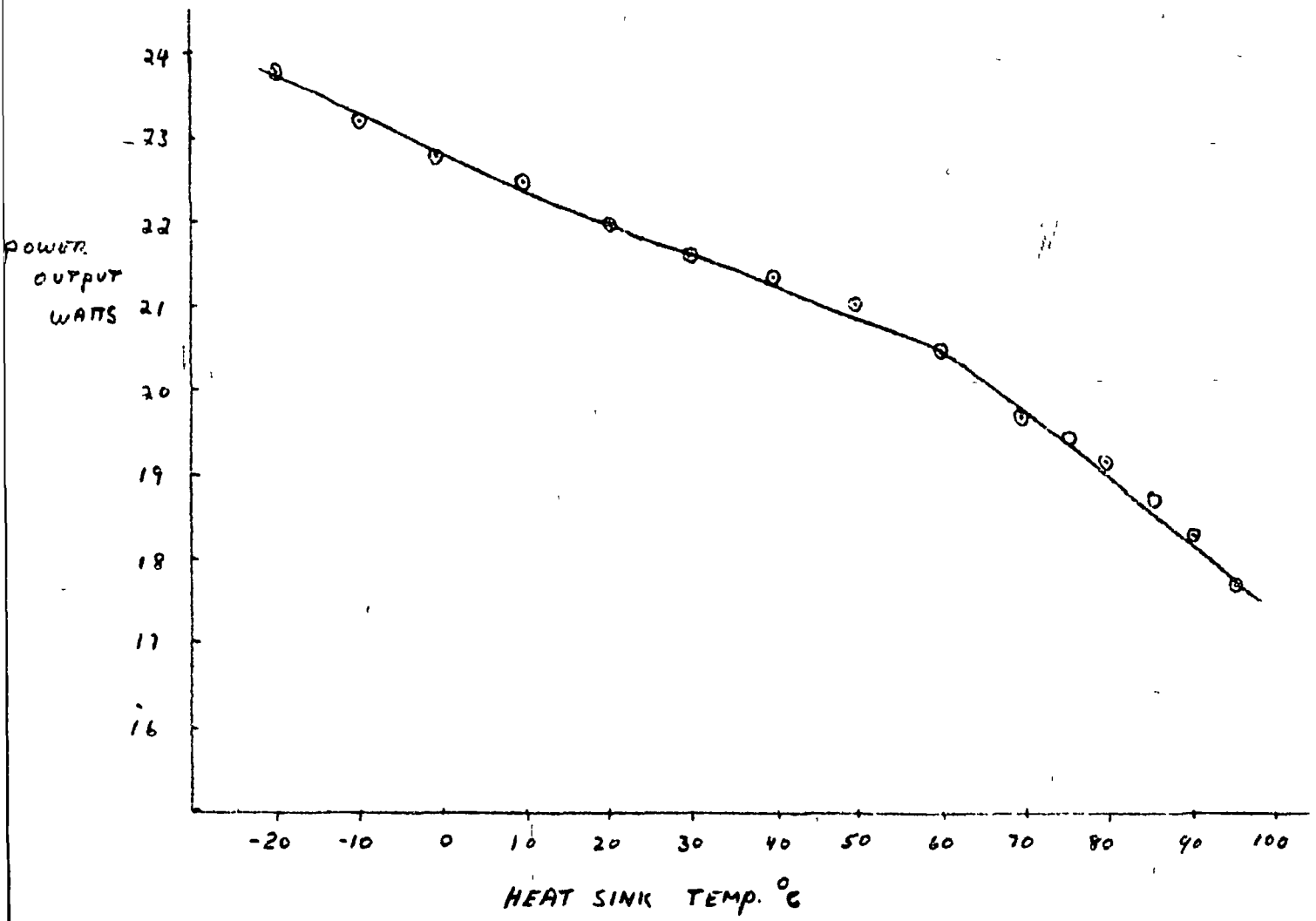


Figure 17

324 MHz Power Amplifier Output vs Temperature

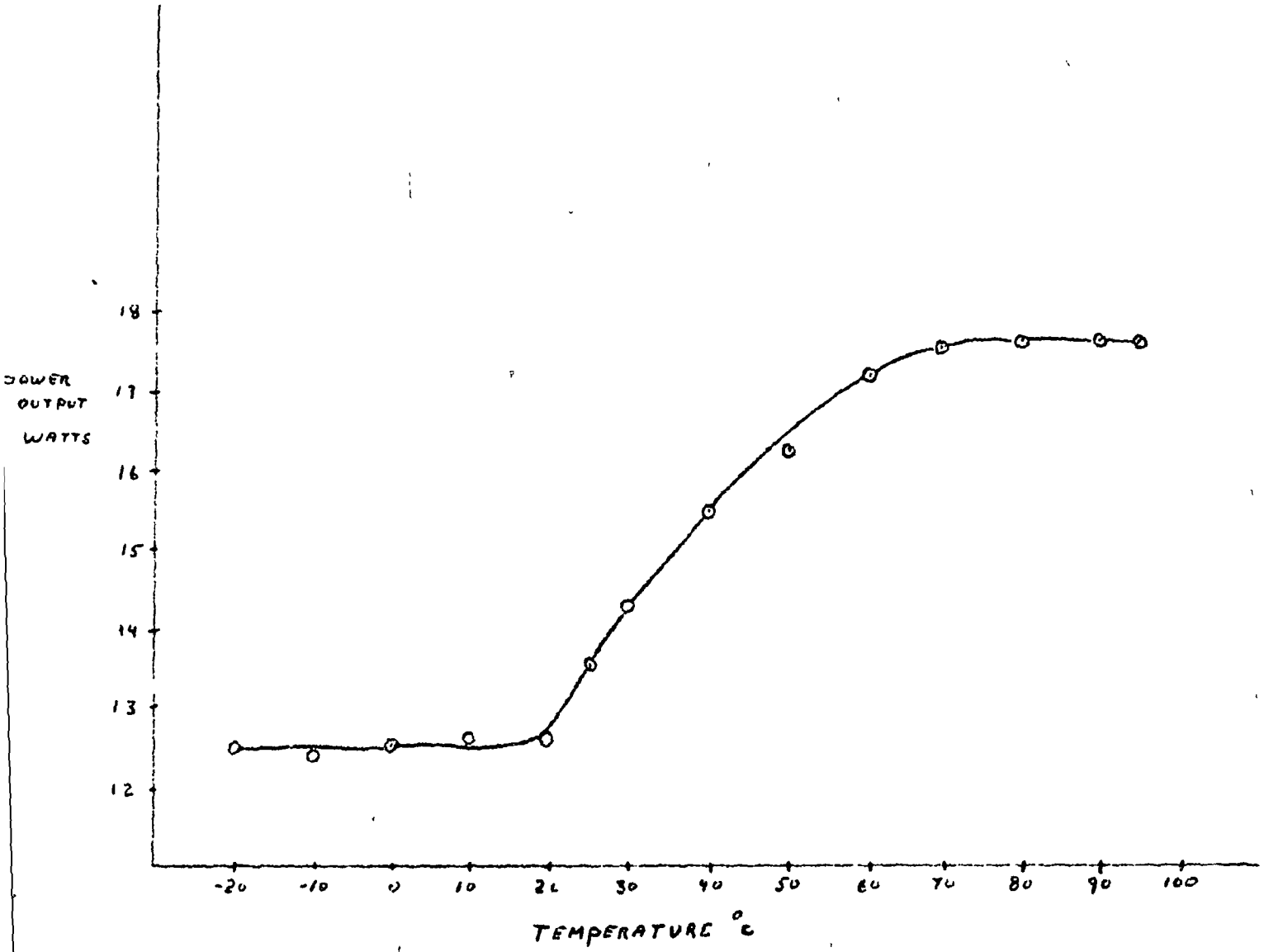


Figure 18

Temperature Controlled Output of Power Amplifier With AGC

In fact the match can vary over a very large value. It was found that the TRW 2N4431 power transistors would not realiably take this mismatch. Additionally, the method of power detection used at the power amp output for the AGC circuit ceased to function properly under a mismatch condition. Based on these findings a new power amplifier circuit was utilized and the AGC function discarded. A higher dissipation rated transistor was tried, the RCA 2N5016. The new circuit was laid out in the allotted space as shown in Figure 14 on a printed circuit board. The schematic of the new design is shown in Figure 19. The circuit was designed on a narrow band basis to again suppress the spurious frequencies generated in wide band amplifiers under poor loading conditions. A special coaxial output matching network was found to work satisfactorily for matching the amplifier to the varying load conditions. The amplifier produced 8 dB gain at a maximum power output of 26 watts. The normal operating level was about 16 to 20 watts.

2.2.3.4 X6 Multiplier Assembly (A3A4)

The X6 multiplier section is an integration of two multipliers, a doubler and a tripler into a cast aluminum block. The doubler from 325 to 650 MHz is a push-push or balanced type of circuit utilizing two varactors. The tripler represents a transition from lumped to distributed circuit parameters. The tripler contains one varactor in a series connected circuit with special provisions for heat sinking. An output coaxial cavity is used to match and filter the diode. A schematic of the X6 is shown in Figure 20.

(A) Breadboard Model

The performance of the breadboard model agreed reasonably well with the design at normal operating temperature. The doubler yielded a conversion loss of 1.5 dB and the tripler a 3 dB loss. An output at 1950 MHz of 4.5 watts could be obtained for an input of 15 watts. The varactors used for the doubler were VAB 801

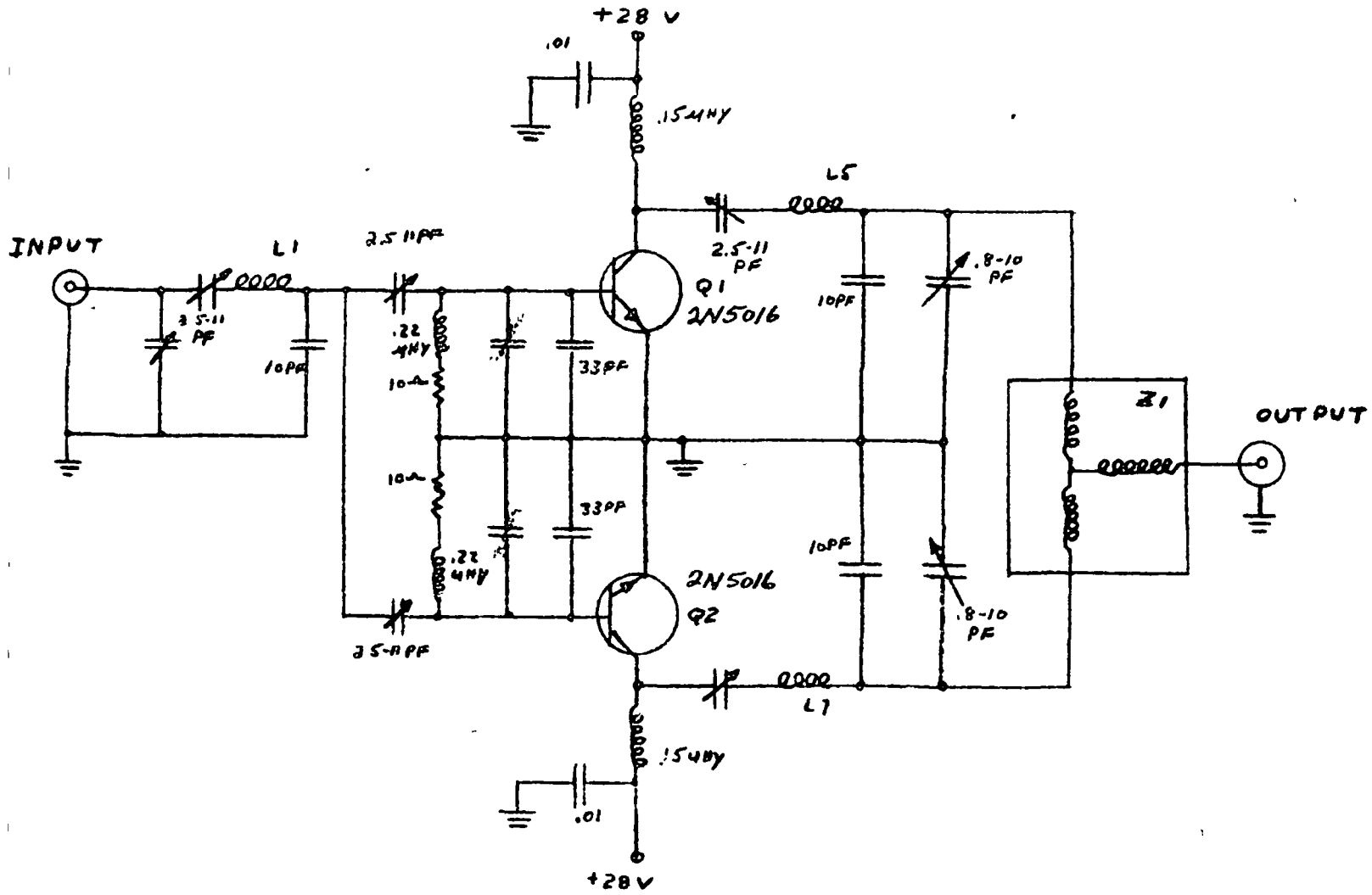
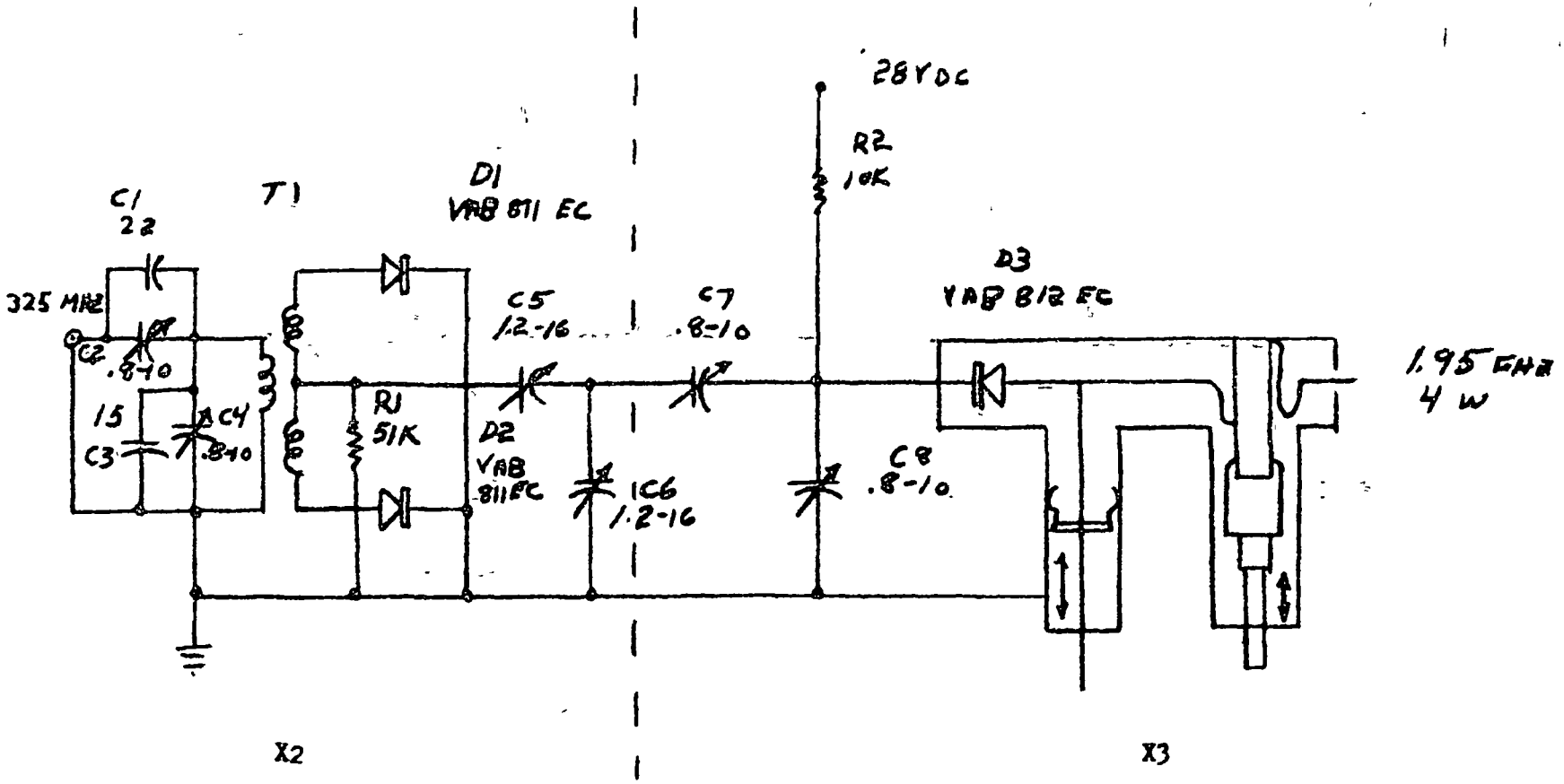


Figure 19

Power Amplifier/Final Model



T1

RRI: 1t #16 wire

SEC: 2t #16 wire C.T.

Figure 20

X6 Multiplier Schematic

and the tripler VAB 802. The X6 multiplier was found to drop considerably at the extreme hot temperature, a value of about 2.5 dB at 95°C (Figure 21). The amount of thermal drop, by itself is not very severe, but when added to the drop off of other following multipliers could mount to an intollerable value. Therefore, it was imperative that every effort be taken to reduce the thermal drop of the X6. The X2 stage was operated by itself over temperature and found to have very little drop as shown by Figure 22.

An attempt was made to improve the thermal problem by utilizing a higher power varactor. The Varian "Super Bi-Mode" varactors VAB 811A and 812A were tried in the X6. The improvement to the doubler was very slight, only several tenths of a dB at 95°C. However, a significant improvement was noted for the tripler as shown in Figure 23. The performance up to 85°C was improved considerably, about .8 dB. However, from this point on, the power output dropped off very rapidly to about the same value as before. Tests were conducted on the diode heat sink and it was found to be satisfactory and not the cause of the thermal drop. It was also noted that a slow thermal drop occurred above 85°C after power was applied to the X3. For example, at 95°C the output was only 1.2 dB down from room temperature upon application of RF drive and then slowly over several minutes dropped on additional 1.2 dB. This was concluded to be a thermal problem internal to the varactor itself and could not be improved by external heat sink methods.

(B) Final Model

The final X6 multiplier section incorporating the various improvements performed equally well as the breadboard. An output of 5.2W was obtained for a drive of 17.0 watts, a conversion of 5.2 dB.

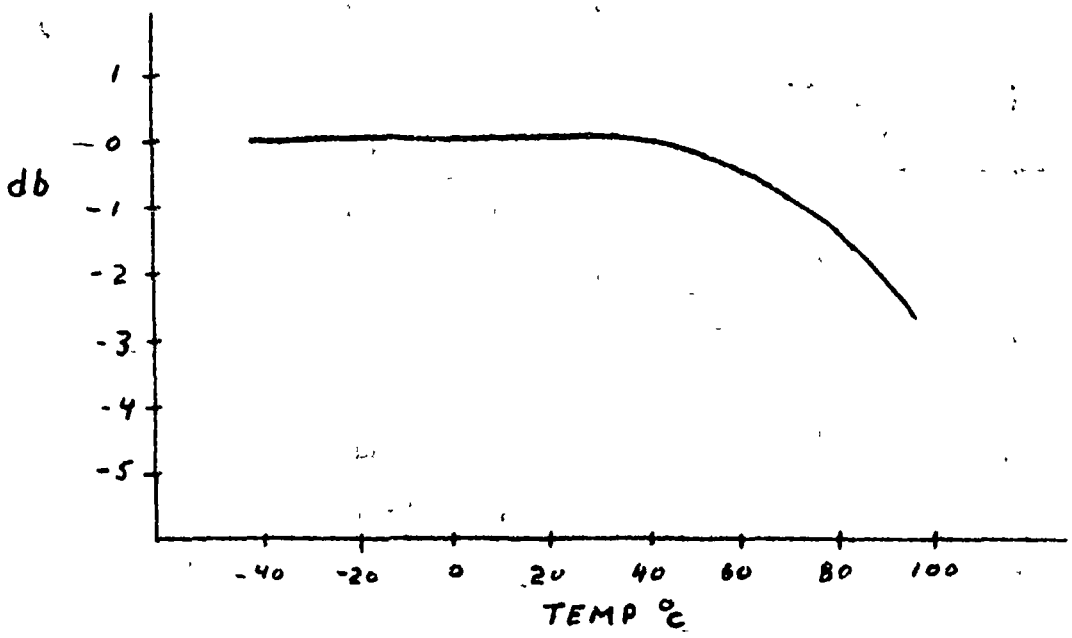


Figure 21

X6 Temperature vs Power Output

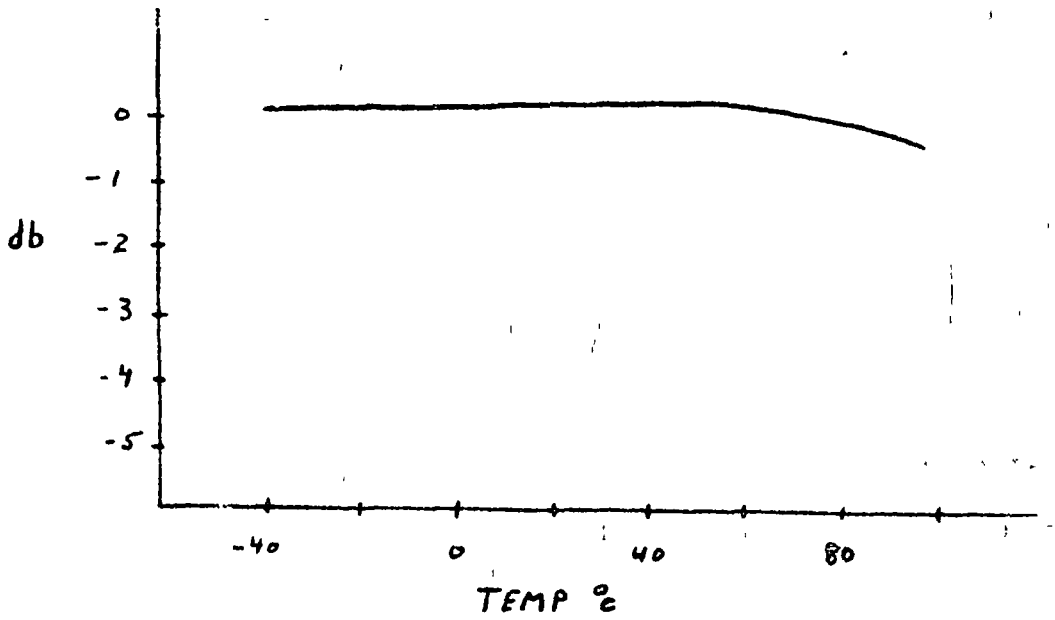


Figure 22

325-650 GHz Doubler Temperature Performance

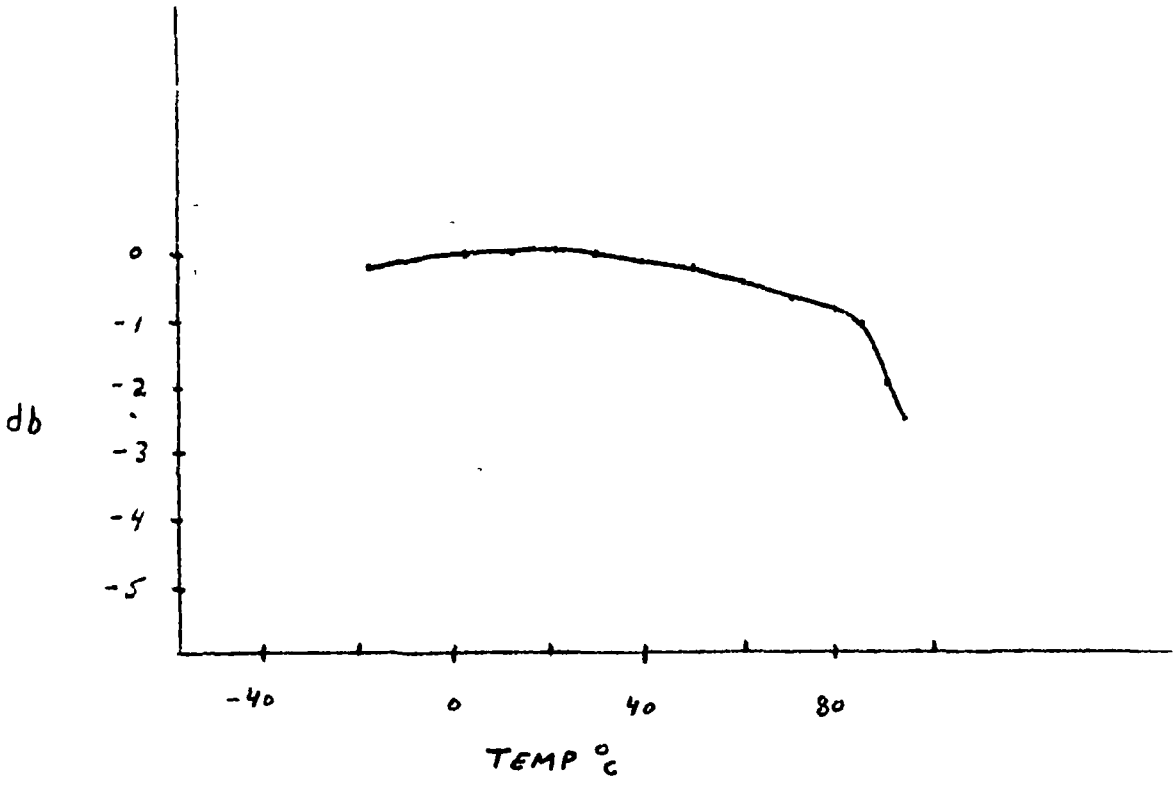


Figure 23

X6 Temperature Performance Utilizing New Varactors

2.2.3.5 1.95 GHz Circulator (A3A4)

This device is a 3 port Y-junction circulator constructed in stripline. The 3rd port is loaded with a 50 ohm resistor which is placed internal with the stripline. A Y-matching wing is placed at the center of the Y-junction which matches the 50 ohm stripline runner to the ferrite. Two ferrite disks are placed on either side of the matching wing. A permanent magnet provides the magnetic bias for the ferrite.

This type of circulator was chosen because of its inherent small thickness, approximately 1/4 inch. The circulator was fitted with right angle connections which allowed considerable space saving by "stacking" it with other stripline devices.

The circulator provided an isolation of 20 dB and an insertion loss of 0.6 dB.

2.2.3.6 S-C Band Multiplier/Circulator (A3A5)

The 1950 to 3900 MHz multiplier and circulator was designed in stripline in order to produce a thin package consistent with the basic overall design concept of "stripline component stacking". The complete multiplier and circulator was designed in to a package 1/4 inch thick, and 5 inches square. Right angle connections were again planned such as to mate with the 1950 MHz circulator.

The circulator design was the same as the 1950 MHz unit, the only difference being its smaller size and, therefore, smaller ferrite garnets. The performance obtained was 22 dB isolation and 0.65 dB insertion loss.

The basic design of the stripline doubler was a shunt-diode configuration with the varactor placed between the input filter and the bandpass filter, as shown in Figure 24. For both electrical and mechanical reasons the shunt-diode configuration

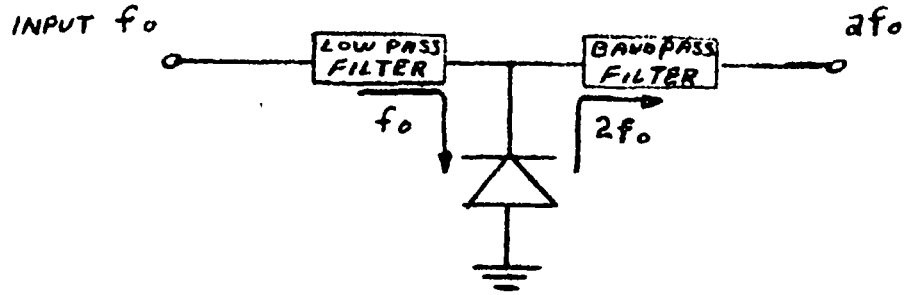


Figure 24

Varactor Doubler

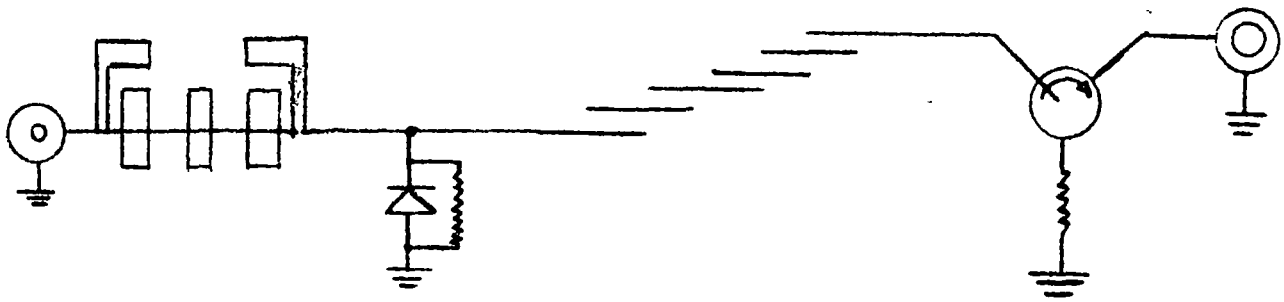


Figure 25

Varactor Doubler Schematic

is the best for strip transmission line work. In this configuration, one end of the varactor is physically grounded, with the ground plane acting as an excellent heat sink. Tuning and access to the diode are also easier with the shunt configuration. Location of the diode between filters depends both on the reflected impedance of the filters and the reactances of the diode. For the doubler, the first approximation was to place the diode between the filters at a point which satisfies two conditions - namely, that the input low-pass filter present an open circuit to the diode junction at the 2nd harmonic frequency and that the output bandpass filter present an open circuit to the diode junction at the fundamental frequency. These conditions prevent dissipation of the 2nd harmonic and the fundamental at the input and output filters. Fine tuning was achieved by capacitive tuning screws placed on each side of the diode. The distances between the diode and the two filters were slightly foreshortened to accommodate the tuning screws. Diode self bias was obtained by utilizing a DC blocking joint on the input to the low pass filter and a 10K 1/8W carbon resistor from the center conductor to the outside of the package. The 10K resistor provided part of the needed self bias resistance and RF isolation.

The input low pass filter for the doubler is illustrated in Figure 25. The characteristic impedance of the filter was set at 50 ohms to match the input source. The 50 ohms impedance was carried through the filter and no attempt was made to match to the diode since, in the over-driven condition, the diode impedance is difficult to predict accurately. The cutoff frequency f_c of the filter was set at about 2100 MHz sufficiently above the required frequency to have a low insertion loss. The design of the filter was based on an elementary lumped-constant filter consisting of three constant K prototype L-C sections between M derived end sections.

The bandpass output filter was based on the Chebyshev response which is characterized by equal ripples in the passband. The filter is a parallel coupled

resonator type consisting of quarter-wave length sections at the mid-band frequency. The bandpass filter was required to have low insertion loss in the passband and attenuate the fundamental, 3rd and 4th harmonics by at least 50 dB. A five section filter was used which gave at least 60 dB attenuation and less than 0.5 dB insertion loss in the passband.

(A) Breadboard Design

The first model built was an inline design where no bends were encountered. This unit yielded an efficiency of 2.7 dB for an output of 1.7 watts. The 3 dB bandwidth was about 20 MHz or 0.5%.

The circuit was relaid out to conform to the final 5 inch square package size. At first the efficiency was found to be rather poor. By adding sufficient tuning screws the efficiency was improved to 4.5 dB. The bandpass was still quite narrow, about 0.4%.

A circuit modification was made which consisted of series resonating the diode. This series resonance of the diode was accomplished by adding a small capacitance in series with the diode. This series capacitance was provided by modifying the diode package to have a larger flat surface on the end terminal touching the stripline and positioning the diode over the stripline circuit such as to form a small capacitance between the diode and stripline. A very thin sheet of mica insulation was used to prevent shorting the diode to the stripline trace. The diode was secured in a collet, which was designed to be capable of being screwed in and out of the holder mounted to the stripline board to permit adjustment, or tuning, of the series capacitance. Diode self bias was provided by securing a very small carbon resistor across the varactor itself as shown in Figure 26.

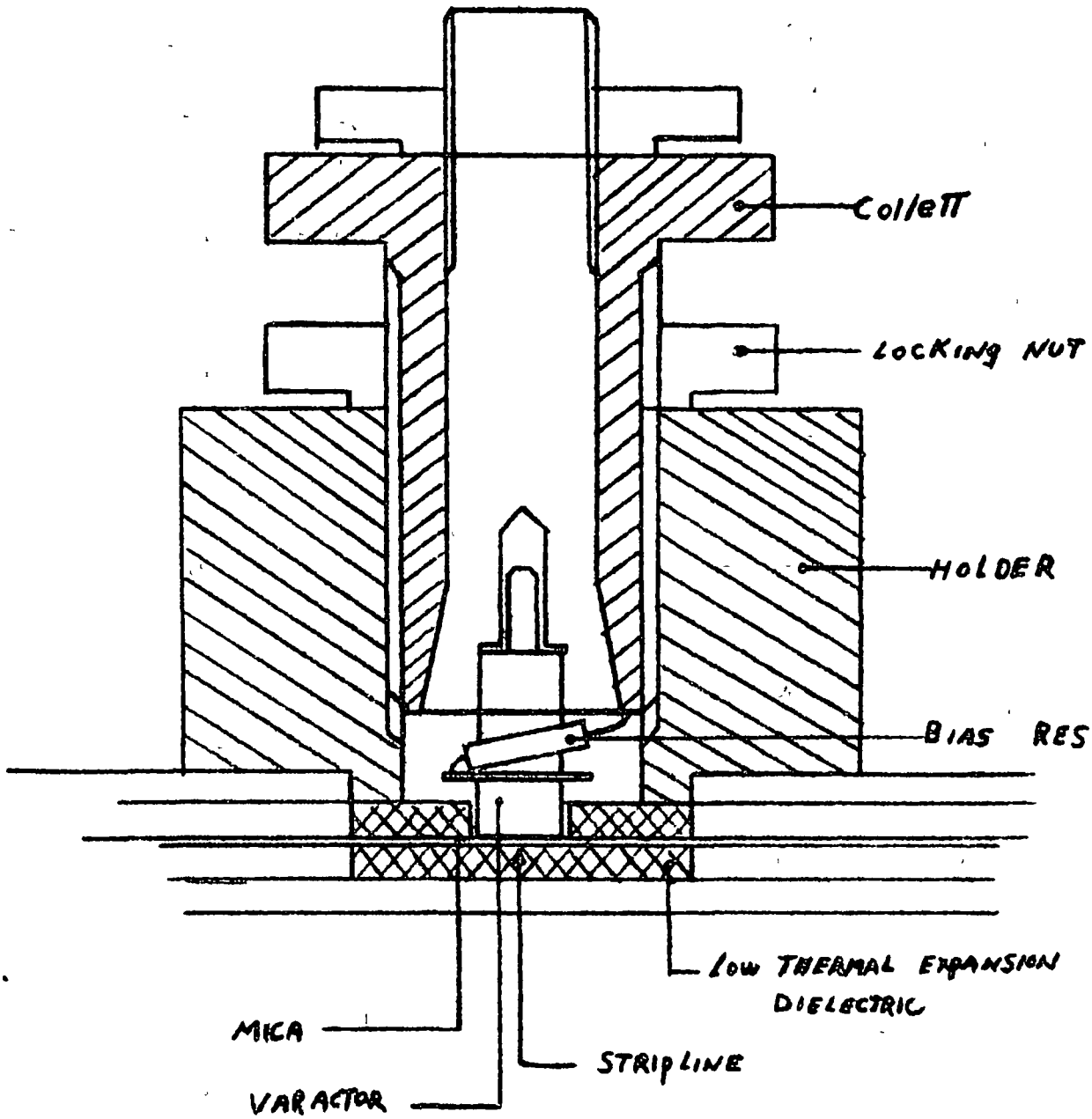


Figure 26

Varactor Series Tuning

The operation of the multiplier was significantly improved over the previous design in both efficiency, bandwidth and spurious free operation. The 3 dB bandwidth was increased to 7% with an efficiency of 4.5 dB conversion. By peaking the circuit slightly with the tuning screws the efficiency was increased to 3.2 dB with only a slight decrease in bandwidth. In the presence of large temperature variations, however, considerable detuning of the circuit was observed. This detuning effect was found to be caused by variation of the series capacitance gap between the diode and stripline circuit due to high thermal expansion and cold flow of the dielectric material. This thermal problem was eliminated almost completely by inserting small disks of dielectric material, having a lower thermal expansion and no cold flow properties to support the stripline trace beneath the diode. The final temperature performance is shown in Figure 27. This method, however, produced a slight loss in efficiency because of the more lossy dielectric added to prevent the temperature problem. A better solution to this temperature problem was found at a later date on another project where the cold flow of the dielectric was eliminated by restricting the clamping action of the ground planes around the diode holder by utilizing metal spacers.

2.2.4 162 MHz Filter Assembly (A4)

The 162 MHz filter is a two section "M" derived bandpass filter designed for a 3 dB insertion loss at the center frequency of 162 MHz and an insertion loss of 100 dB maximized at the 3rd and 5th harmonics of 40 MHz. Figure 29 shows the schematic of the complete filter. The high rejection at the point of these frequencies is to offset the spurious enhancement of the multiplier chain and keep these spurious below 60 dB at the 35 GHz output frequency. Figure 28 shows the frequency response of a single section of the 2 section filter. The following table lists the insertion loss values as a function of frequency and temperature.

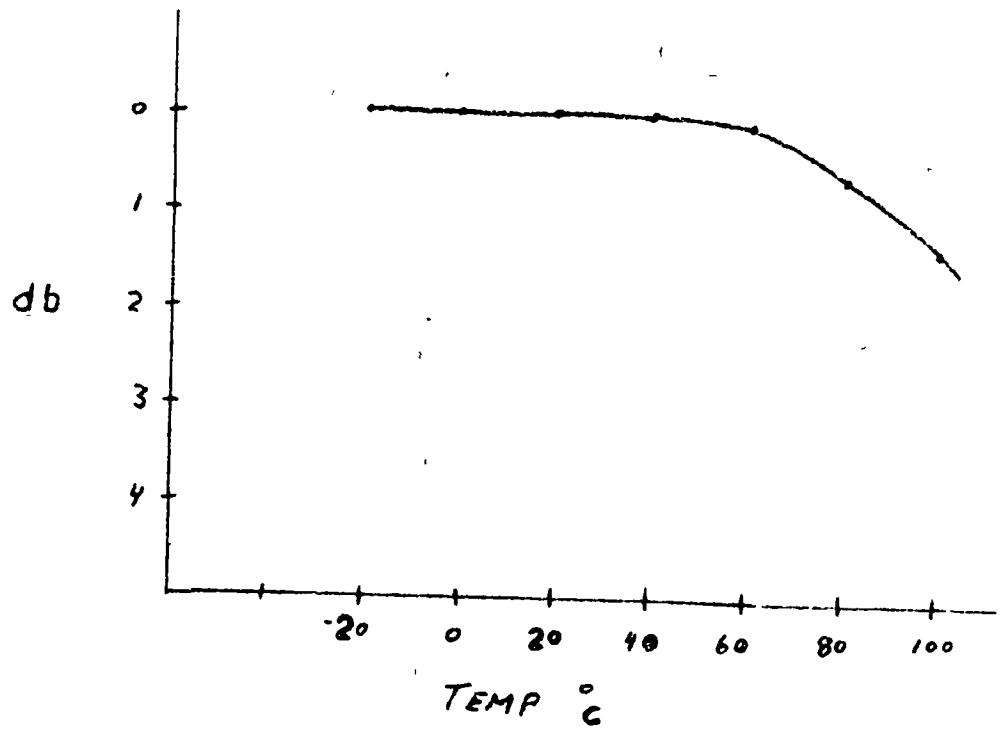


Figure 27

Output vs Temperature of Strioline Doubler

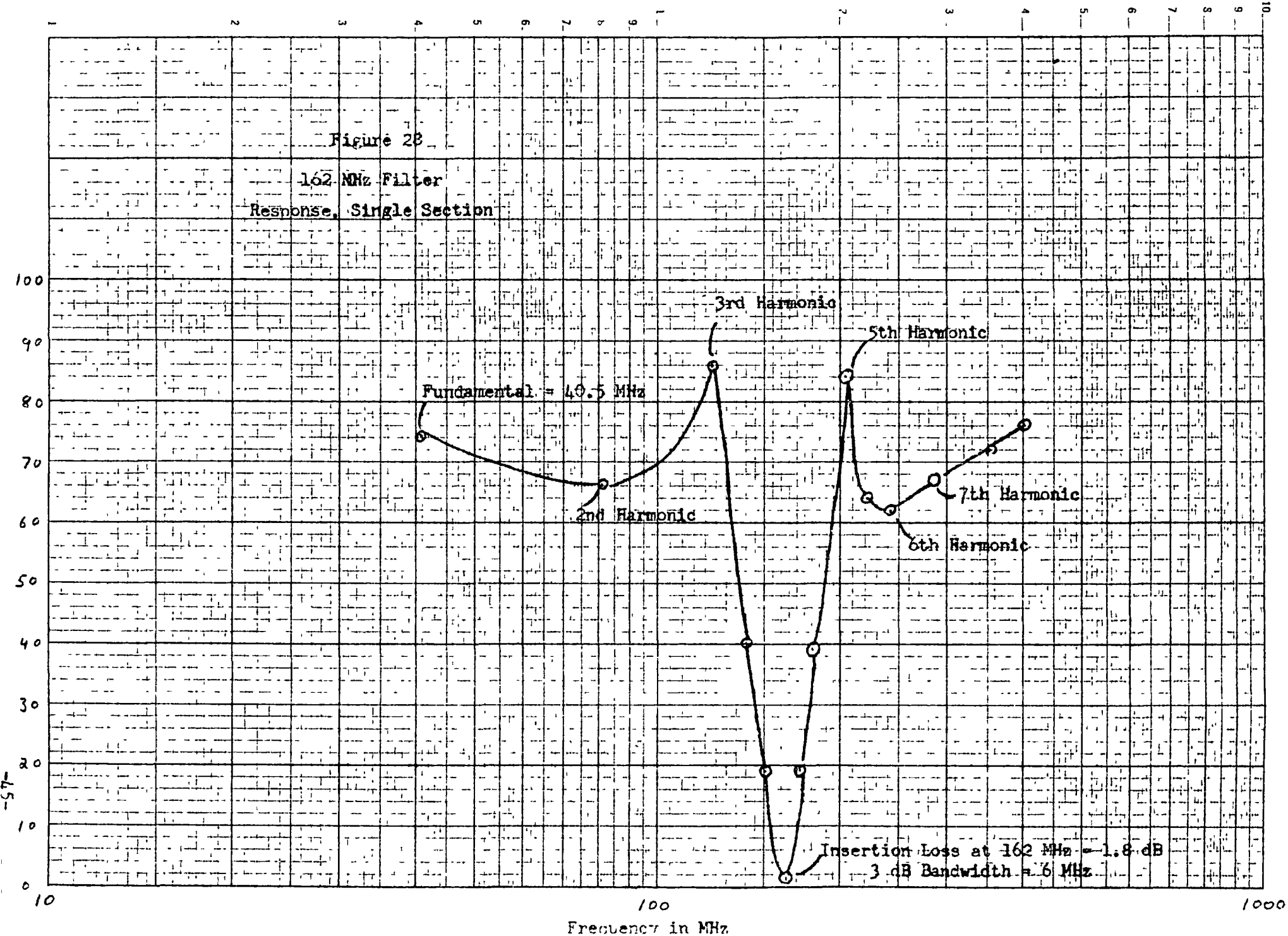
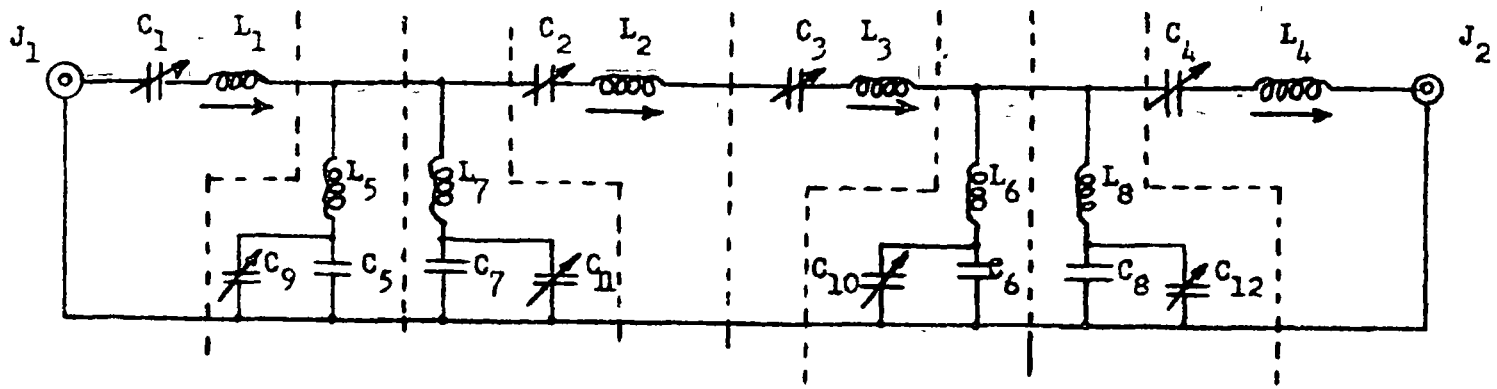


Figure 29

Schematic, 162 MHz Filter



$L_1 - L_4$	.644
$L_5 - L_6$	.017
$L_7 - L_8$	.014
$C_1 - C_4$	.8 - 1.5
$C_5 - C_6$	82
$C_7 - C_8$	39
$C_9 - C_{10}$	1 - 36
$C_{11} - C_{12}$	1 - 16

All L's in microhenries

All C's in picofarads

These results pertain to the complete filter, or two cascaded sections. Insertion loss and attenuation at measurable points were checked to determine a shift in the attenuation curve. All harmonic frequencies have an attenuation greater than 110 dB.

Temperature Test Results

Frequency (MHz)	Insertion Loss (dB) -35°C	20°C	110°C
135	98	100	98
140	83	84	82
150	35	35	33
160	8.0	7.5	7.8
162	3.4	3.2	3.6
164	4.6	4.8	4.6
170	25	33	25
180	82	75	82
185	89	90	89

2.2.5 C- to X-Band Tripler (A5)

The objective of this task was to develop an efficient, high power, narrow band coaxial to waveguide C- to X-band tripler. The requirements for efficient operation of a coax to waveguide multiplier are the same as any other multiplier, and consist of the following:

(1) Efficient input match to the varactor at ω_o.

(2) Efficient output match at $3\ \omega_o$.

(3) Idling of $2\ \omega_o$.

(4) Effective isolation of $2\ \omega_o$ and $3\ \omega_o$ from the input.

(5) Effective isolation of ω_o and $2\ \omega_o$ from the output.

Since both coaxial and waveguide techniques are available to implement the various circuit requirements the design variations possible in this type of multiplier are limitless. Two models were built which are described below.

(A) Preliminary Model

Figure 30 is a diagram of the first model. Radial choke filters were utilized in the coaxial section just prior to the waveguide preventing the propagation of either of these harmonics back toward the generator. The output waveguide is cut off for both the fundamental and second harmonic, preventing their propagation toward the output. In the region of the diode, a variable length section of ridged waveguide was utilized which would propagate the second harmonic and provide the idling. Tests with this multiplier indicated that the varactor diode was not being idled effectively at the second harmonic. The problem appeared to be one of effective diode-to-waveguide coupling at the second harmonic as well as the possibility of excessive losses in the waveguide shorts utilized. A modification was made to introduce a coaxial idler stub at the junction of the coax and the waveguide which verified that the poor conversion loss was due to ineffective idling.

(B) Final Model

The indicated changes were incorporated into a second model, which is diagramed in Figure 31. The position of the idler was carefully calculated so that the length of the idler stub would be one half wavelength at the second harmonic. This idler stub length is a quarter and three quarter wavelengths at the fundamental and third harmonics and thus is effectively open circuited at both frequencies. At the same time the input tranamission line is shorted at the second harmonic preventing propagation of the second harmonic toward the input. A dual choke rejection filter was utilized at the third harmonic rather than a single choke filter to provide a broader band rejection. This eliminated a need for adjustment

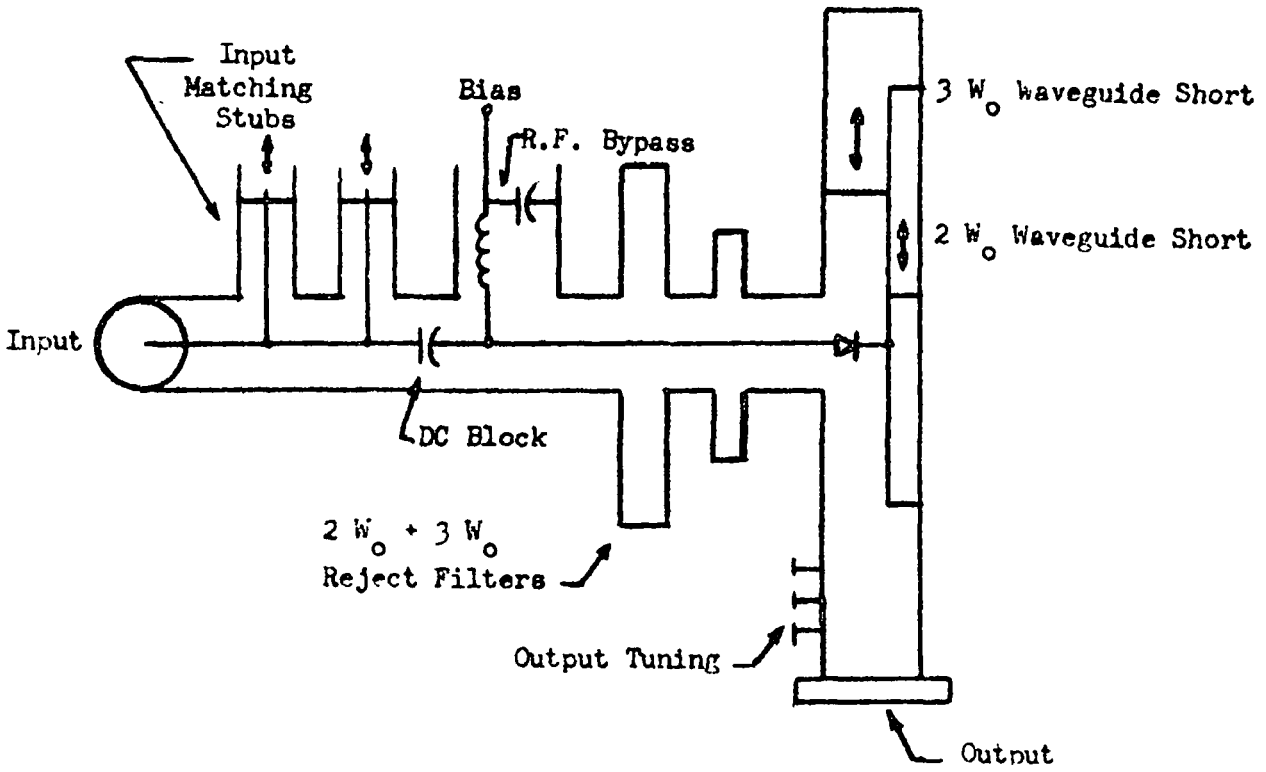


Figure 30

Preliminary Model of C to X Band Tripler

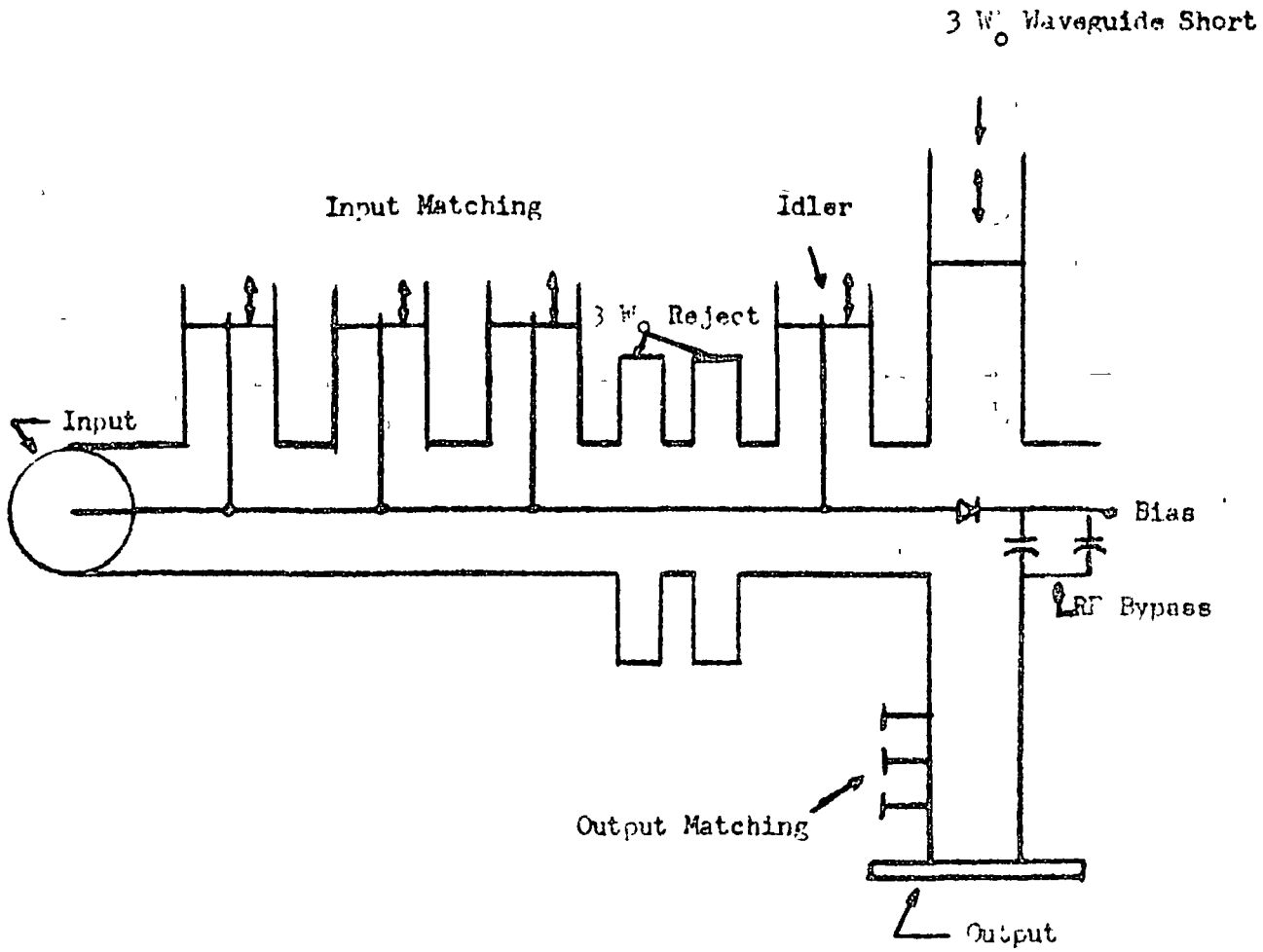


Figure 31

Final Model of C to X Band Tripler

of the single narrow band choke to the precise operating frequency. This multiplier was tested extensively. Variations in diodes, input power temperature and bias supply were investigated. Power output of 570 mw was achieved with an input of 1.5W. Typical conversion loss was in the order of 3.4 to 3.6 dB with moderate variation over temperature extremes. A curve of the typical temperature performance is shown in Figure 32 and the response curve in Figure 33. In conclusion, it is felt that the present design is nearly optimum in performance.

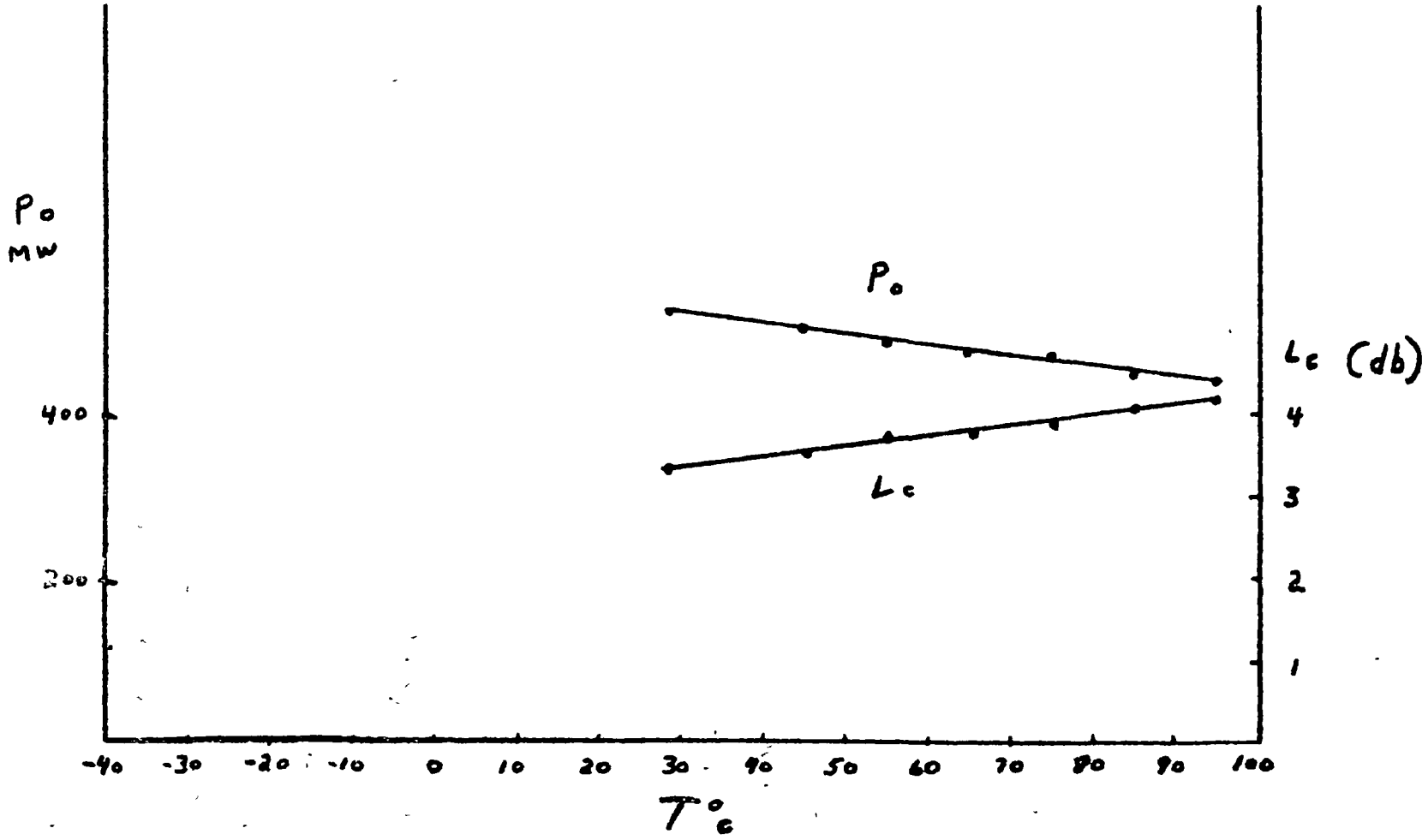
Multiple Diode X-Band Tripler Discussion

In the frequency domain of 10 GHz and above, the diode characteristics become the limiting factor in producing efficient, high power multipliers. For a particular power handling capability it is desirable for $C_j V_B^2$ to be approximately constant. For best conversion loss it is desirable to have as high a cut off frequency as possible. For the C to X multiplier diode described above, junction capacitance at six volts is about 1 pfd; V_B is about 60 volts and fc is 100 GHz to produce a 4.2 dB conversion loss and a 500 mw or more output. A multiple diode multiplier could be made to improve on the performance of the above multiplier in two ways. Efficiency may be kept approximately constant and power output increased proportionally to the number of diodes utilized, or efficiency can be improved to yield more power with a constant input power.

If efficiency is kept constant, greater power input is required to produce a proportionally greater power output. The power output capability can be multiplied by any small integer by utilizing more of the presently used D4852H diodes. This in turn increased the DC input power requirement proportionally. Since the present trend in many applications is to minimize DC input power, efficiency improvement becomes a very worthwhile goal. There is a practical limit to the degree of improvement that can be expected since the diode cutoff frequency rapidly tends towards infinity as the efficiency improves.

Figure 32

C-X Band Tripler Temperature Performance



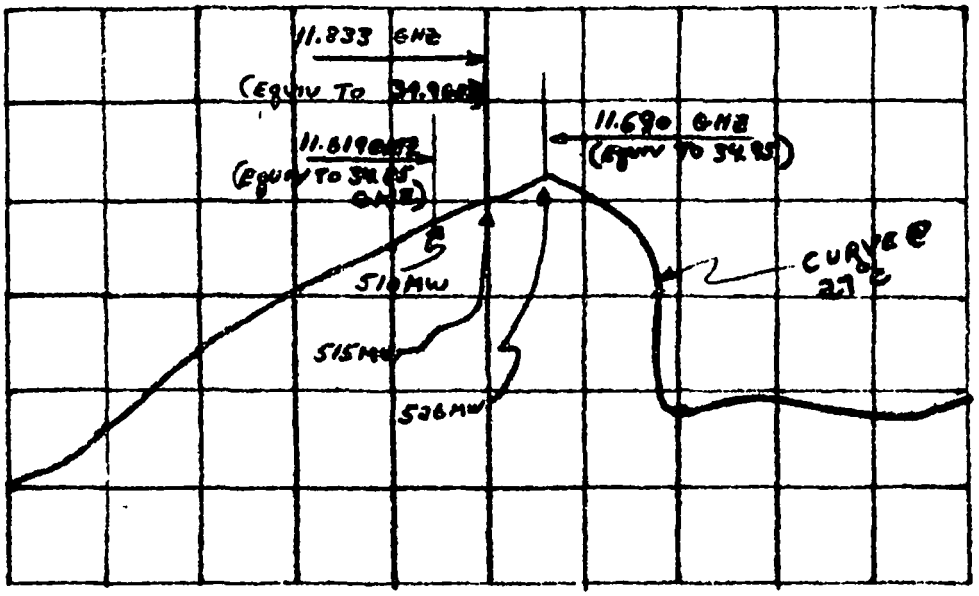


Figure 33

C-X Tripler Frequency Response Curve

2.2.6 X-Band Isolator (W9)

The X-band isolator is a two port waveguide device used to provide isolation between the C-X band tripler and the X-Ka band tripler. The unit was a purchased item supplied by Microwave Associates. The unit met the specifications of 20 dB isolation and 0.5 dB insertion loss.

2.2.7 X to Ka-Band Tripler (A6)

The circuit configuration chosen for this multiplier is shown in Figure 34 and is as follows. The varactor diode is mounted in an open-circuit self-biased configuration in a rectangular waveguide cavity which provides coupling to the varactor at the input frequency through a resonant iris and at the third harmonic output through a waveguide section cut off to the second harmonic. The cavity is resonant, approximately one wavelength long, at the second harmonic.

Breadboard Design

The tripler was designed for 35 GHz center frequency with input in WR-62 waveguide, and was built in aluminum. The rectangular cavity was machined from a one-piece aluminum block by a broach, a technique which leads to cheaper quantity production and can also result in a smoother surface finish than with other machining methods. The output waveguide cut off section, incorporating a three screw tuner, was dimensioned to be applicable for output frequencies in the 34-38 GHz range.

The tripler was tested using two Sylvania type D5245B varactors chosen for best efficiency at 250 mw input. The input matching tuner design was based on measured diode input impedances at the 250 mw drive level. It consists of a fixed inductive post doublet with several capacitive tuning screws giving a limited range of adjustment, for changes in diode or operating conditions. Several cavity tuning screws and provision for rotation and adjustable insertion of the diode in the cavity was included along with input/output impedance matching.

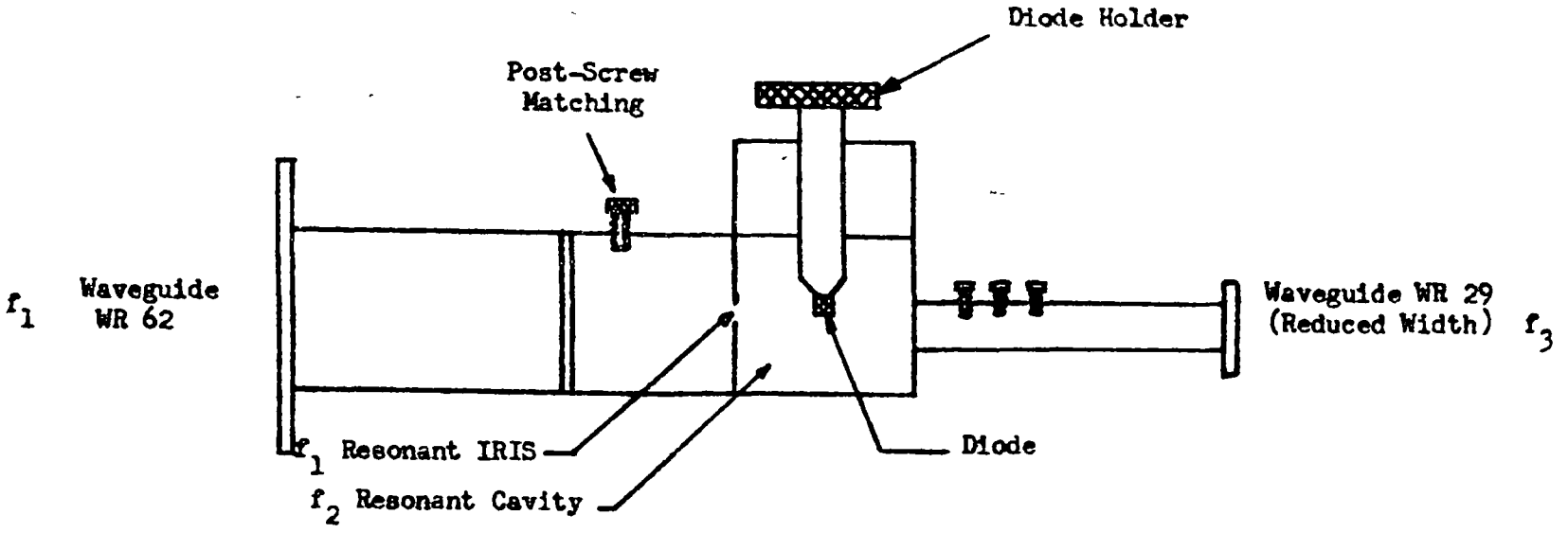


Figure 34

Final Model X to Ka Band Tripler

Test Data

With each of the D5245B diodes, best conversion loss obtained was 6.4 dB at 250-300 mw input. At 350 mw, the highest input power tested, conversion loss was 6.5 dB, the 35 GHz output power being 78 mw.

At 250 mw, constant input, the tripler output was measured as a function of temperature over the range -20°C to +100°C. Output power increased at low temperature, by a maximum of 0.7 dB at -20°C. The decreasing output power with increasing temperature was 1.3 dB at +85°C. The tripler 3 dB bandwidth was approximately 250 MHz.

In the tests with the two D5245B diodes, and subsequently with others, it was found that with the anode grounded, conversion loss was several dB better than with the diode cathode grounded.

Other Related Test Data

Three triplers virtually identical to the unit described, but with cavity length scaled for a center frequency of 34.59 GHz, were ultimately built on another project. These were made in brass and gold plated. Power output of the complete Ka-band source was measured, with the tripler followed by an isolator with approximately 0.3 dB insertion loss. With the two diodes previously tested, power outputs were approximately 85 mw and 75 mw. The X-band input power was in the range of 320-400 mw. Direct data on tripler efficiency was not taken, but it may be concluded that the gold plating improved conversion loss by 0.5 dB or less.

Tripler Modifications

The major change attempted in the tripler design above was addition of a bias resistor and fixed bias. An 1/8W resistor was placed in the body of the diode

holder shaft, and one resistor lead attached to the floating end of the diode, while the other lead was brought out to a bias supply. Coaxial line capacitance effectively filtered RF from the bias line.

The intent was to arrive at a resistor value and bias which would optimise tripler performance, particularly as a function of temperature. However, the addition of the resistor lead to the proximity of the diode degraded the tripler performance, and in no set of circumstances could the performance of the tripler without the resistor be duplicated. Since the tripler output vs temperature is quite satisfactory so long as input power remains high, the bias resistor is not essential.

During tests of the breadboard tripler, it was found that the attainable output depended critically on the spring finger contact between the diode holder shaft and the waveguide. In order to obtain maximum power, the contact had to be made so tight that it became difficult to position.

Final Model

The final model was again constructed of aluminum with the addition of gold plating to reduce losses. The diode holder was redesigned to allow for better RF ground contact during diode tuning or positioning. This redesign was found to work quite well, thereby greatly reducing the grounding contact problem which existed in the breadboard. An output power of 120 mw was obtained for 500 mw drive, considerably better than the breadboard. Figures 35, 36, and 37 indicate the typical performance of the tripler. During final temperature testing it was observed that a major part of the thermal power drop off was due to an apparent resonant frequency shift. Swept frequency curves taken over a temperature variation of -20°C to +90°C showed that the passband shifted downward in frequency as the temperature increased.

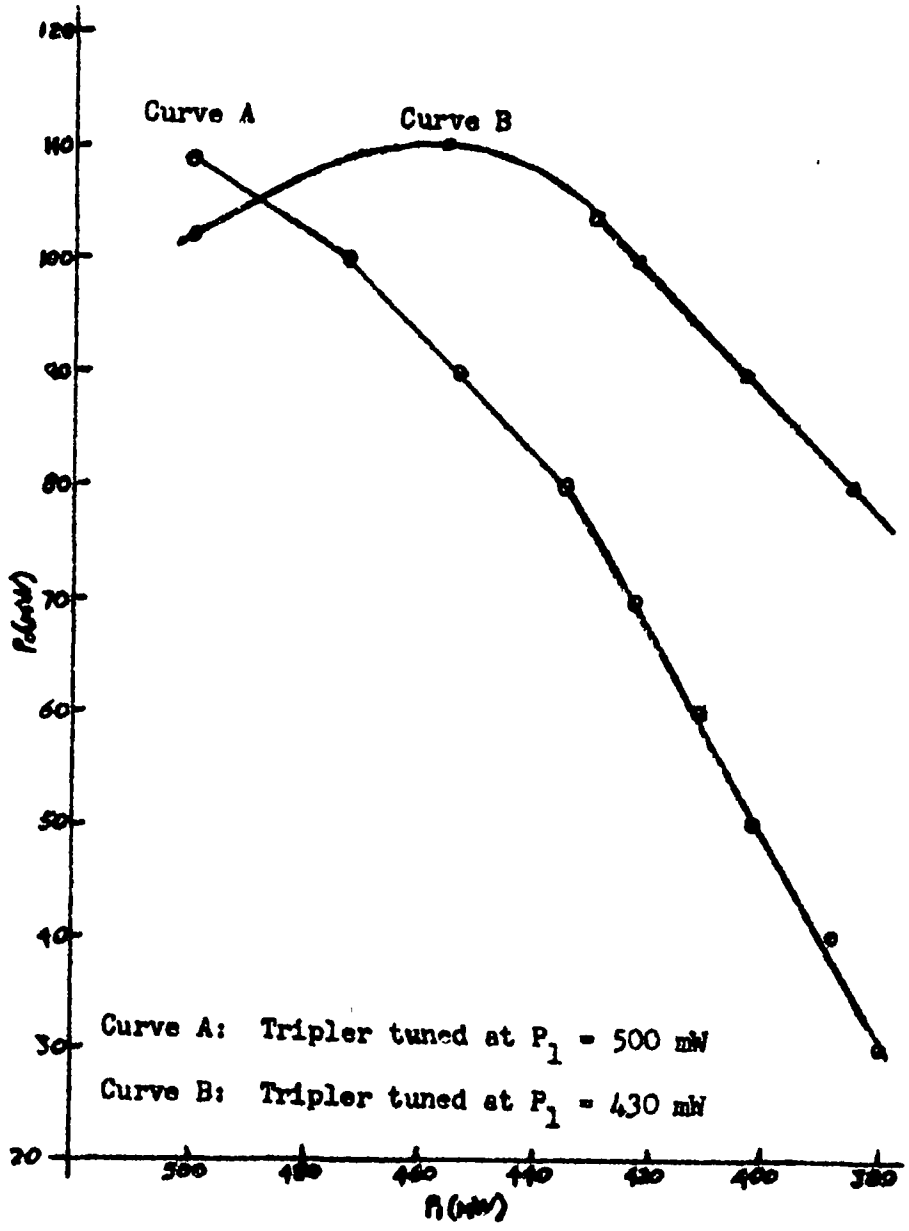


Figure 35

35.0 GHz Tripler Output Power (P_o) vs Input (P_1)
Temperature (T) = 27°C

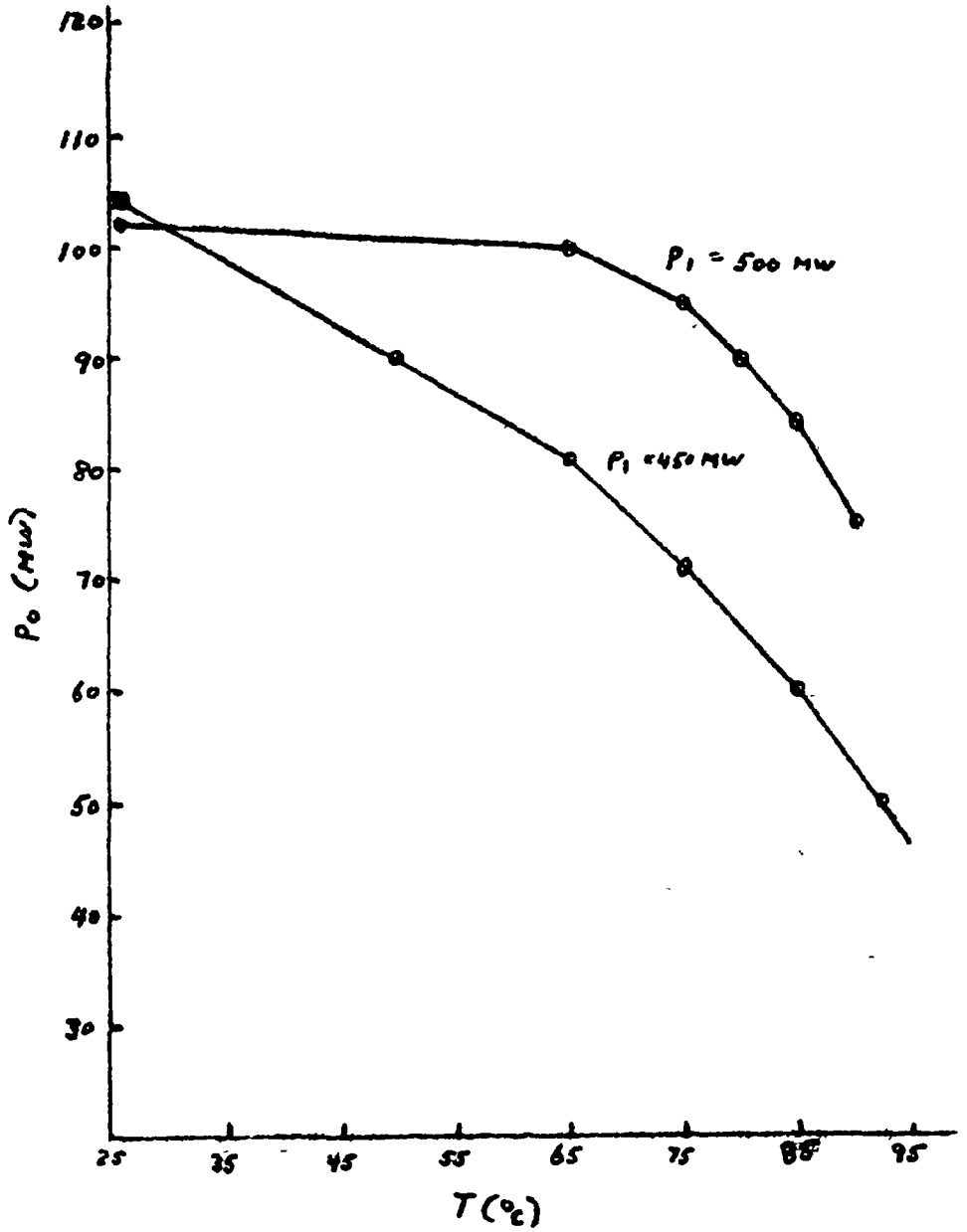


Figure 36

35.0 GHz Tripler Output (P_o) vs Temperature (V)
Tripler Tuned at P_1 = 430 mW, T = 26°C P_1 held
Constant at Values Indicated

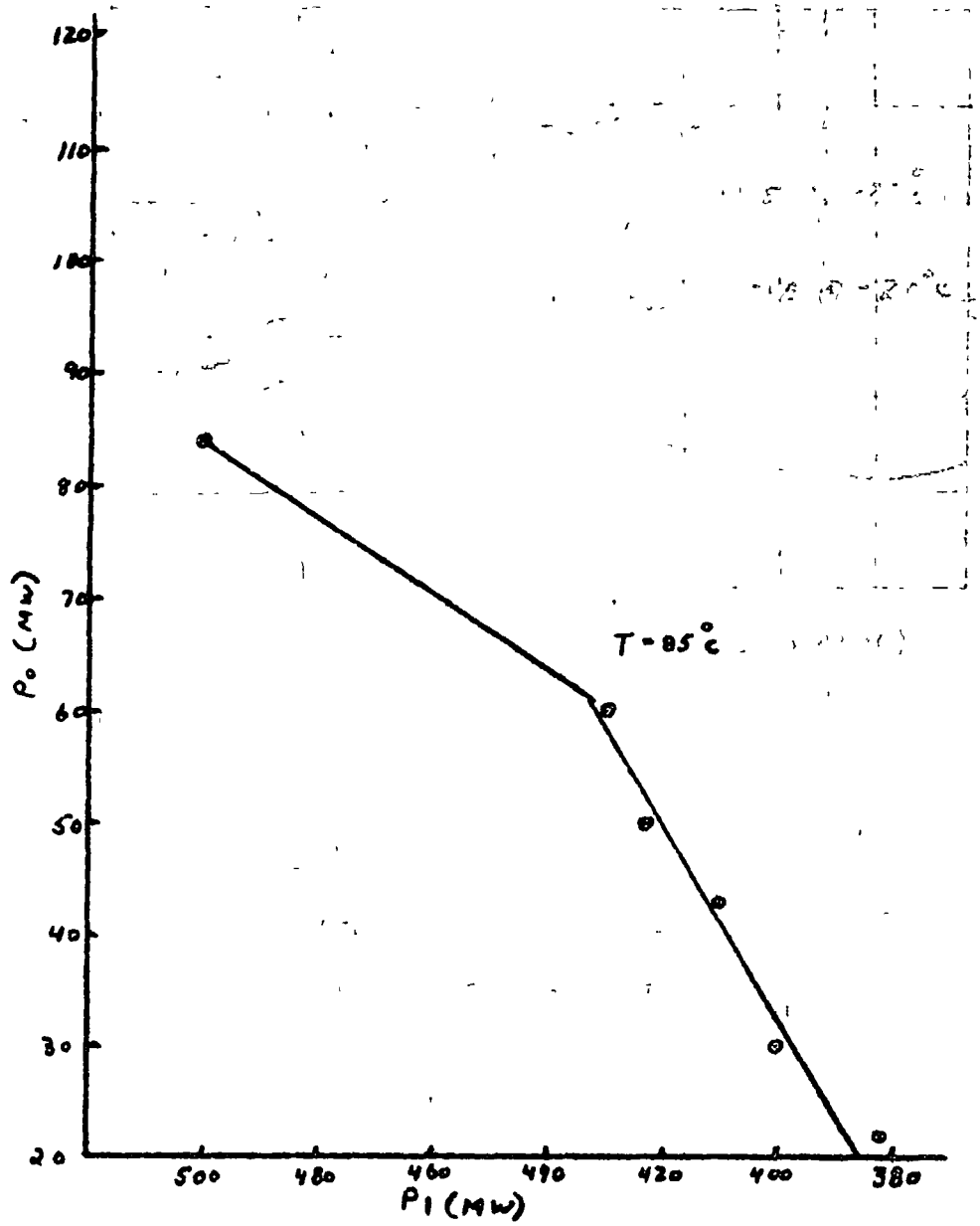


Figure 37

35.0 GHz Tripler Output (P_o) vs Input (P_1)
Temperature = 85°C Tripler Tuned at T = 27°C
P_1 = 430 mW

Further investigation showed a 100 MHz change for a 100°C change in temperature as shown in Figure 38. The possibility that this change resulted from thermal expansion of the cavity block was investigated and a direct correlation was obtained as follows:

$$\Delta f = f \times \alpha \times \Delta t$$

$$\Delta f = 35 \times 10^{9} \times 28 \times 10^{-6} \times 115$$

$$\Delta f = 113 \times 10^{6} = 113 \text{ MHz}$$

where f = frequency

Δf = frequency change

α = thermal coefficient of expansion (aluminum 28×10^{-6})

Δt = temperature change (-20°C to 95°C)

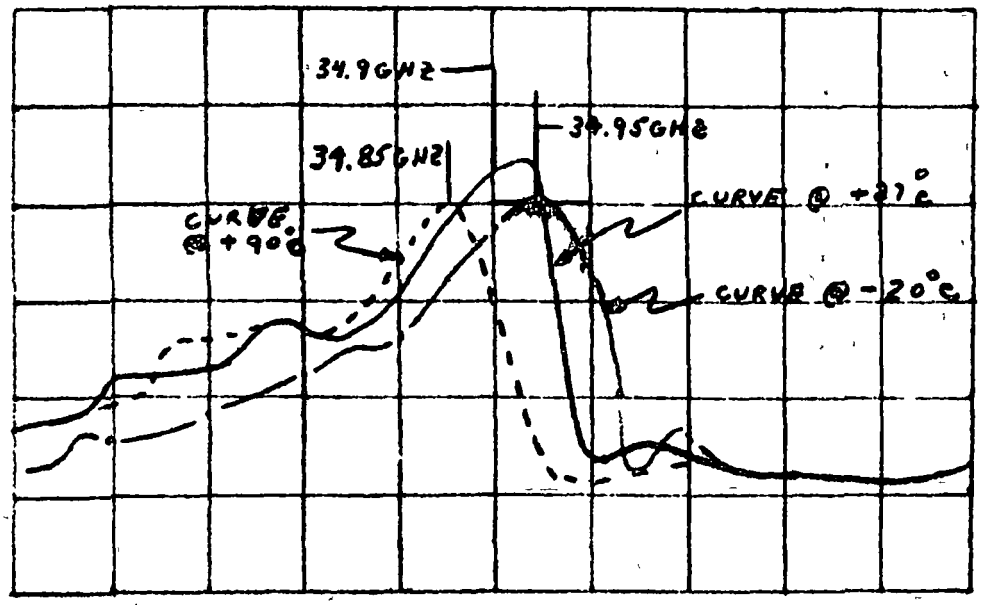
It is recommended that this multiplier block be constructed of a metal having a much lower expansion rate such as annealed Invar (thermal coefficient 2.01×10^{-6}) thereby reducing the frequency shift to 8.1 MHz.

2.2.8 Ka-Band Isolator (W10)

The Ka band isolator is a two port waveguide device used to isolate the last multiplier, X-Ka tripler, to the output of the system at 35 GHz and provide a constant loading for this multiplier. The unit was supplied by Ferrotec Inc. The unit had a measured isolation of 27 dB, and an insertion loss of 0.2 dB.

2.2.9 Output Waveguide (W11, 12, 13)

This portion of the system consisted of RG 96/U waveguide which connected the output of the last multiplier/circulator to the outside of the sealed transmitter case. The waveguide portion consisted of a short piece of "flex" guide to allow for misalignment, a quartz pressure window to provide hermetic sealing and a waveguide bulkhead adapter which sealed the guide to the case via an "O" ring seal.



X-Ka Tripler Frequency Response Curve (-20°C to +90°C)

Power Output vs Temp.

	Frequency (GHz)	
Temp.	34.9	34.85
-20°C	85.5 mw	—
+27°C	103 mw	—
+90°C	20.8 mw	70 mw

Figure 38

3.0 SYSTEM PERFORMANCE

3.1 Breadboard Bench Tests

A complete RF chain up to 35 GHz consisting of the individual breadboard modules was assembled together and tested. The assembly was done in steps such that mating problems would be immediately apparent. One significant problem which occurred during these tests was the mating of the power amplifier to the first multiplier section, the X6 block. It was found that the changing mismatch of the multiplier input produced such erratic operation of the AGC power level control that mating could not be accomplished. The AGC was then disconnected and a manual gain control added for further testing and adjustment. After successful operation up to C band it was observed that the multipliers up to this point exhibited a saturation effect which would tend to nullify the AGC power control and temperature compensation originally designed into the power amplifier.

The remaining system modules were assembled to the chain and an output of 110 mw at 35 GHz was obtained.

An attempt was then made to operate the entire system over temperature. This attempt was unsuccessful because of an apparent frequency correlation problem between the various modules during individual tune up. This meant that the entire chain had to be retuned as a system. During the process of retune up the power amplifier transistors exhibited several failures. A successful tune up and temperature test was obtained up to C band before additional transistor failures stopped further testing. This performance is shown in Figure 39.

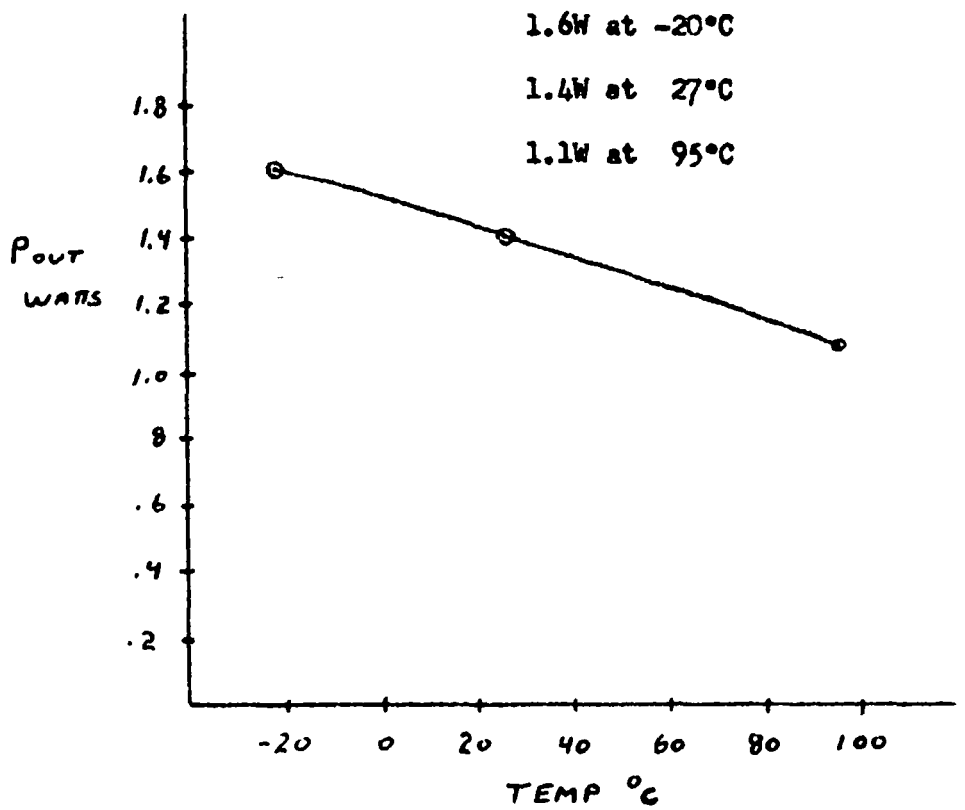


Figure 39

Temperature Performance of Complete System Up to 3.9 GHz

3.2 Engineering Model Bench Tests

A limited number of tests were performed on the engineering model as shown in Figure 1 before delivery to NASA. Below is a listing of the performance obtained at room temperature.

Output Frequency	34.99984 GHz
Output Power	90 mw - cold
	80 mw - warm
RF Bandwidth	≈.6%
Modulation Sensitivity	52 to 120 kHz/volt
Maximum Deviation	120 kHz
Power Consumption	61.6 watts at 28 VDC

Figures 40 and 41 show the spectrum of the output signal at 35 GHz. Figure 40 shows the spurious noise peaking at ±2 MHz from the carrier about 35-40 dB down from the carrier. Figure 41 shows a second noise burst at ±60 kHz which is about 30 dB down from the carrier. Tests were conducted to determine the source of this noise. The ±2 MHz noise appeared to originate in the modulator circuit and the ±60 kHz noise originated in the multiplier/driver section. It was felt that these noise outputs could have been reduced substantially through further investigation and retuning of the suspected trouble areas. The difficulty of course, is the fact that the noise cannot be observed at its source because of the enhancement or gain imported to the noise through the multiplier. Therefore, the entire chain must be used such that the noise can be observed at 35 GHz. Because of the compact arrangement of the engineering model such an investigation would have been rather difficult to accomplish.

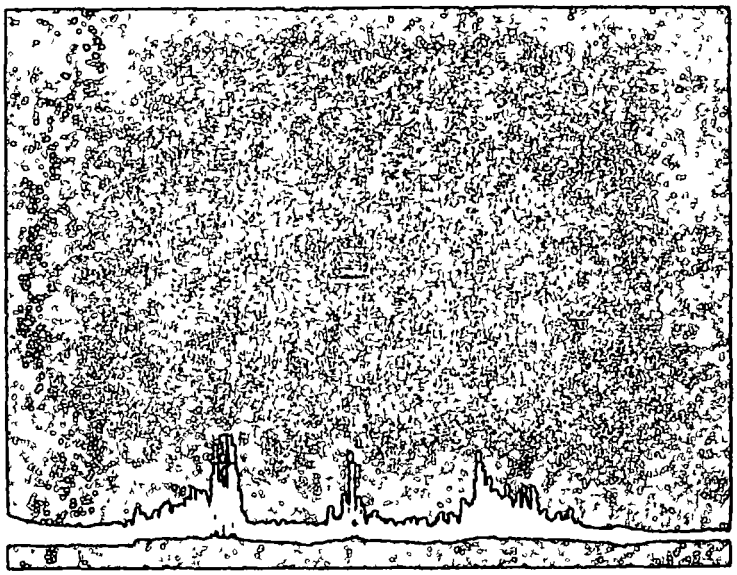


FIG. 40 SPECTRUM AT 35 GHz

(Spectrum width 1 MHz/cm)
(Log Vertical Display)

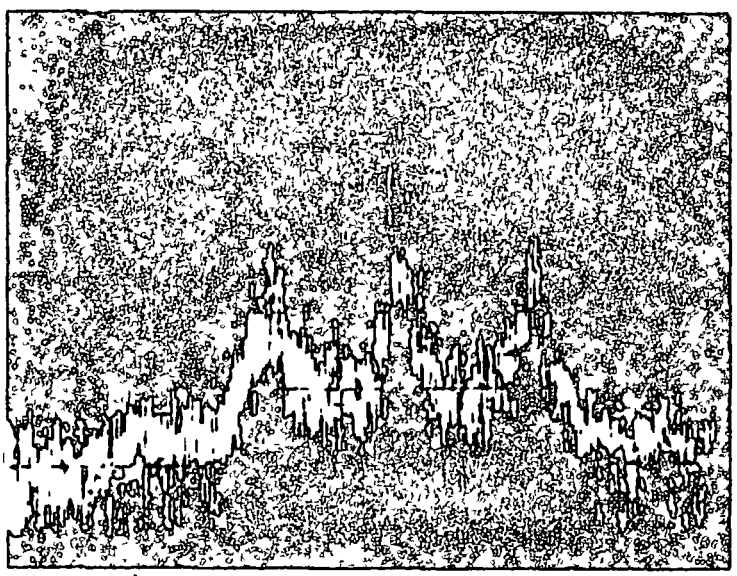


FIG. 41 SPECTRUM AT 35 GHz

(Spectrum width 30 kHz/cm)
(Log Vertical Display)

4.0 PROGRAM SUMMARY

4.1 Conclusions

The final engineering model of the 35 GHz source that was delivered to NASA did not meet all of the originally imposed environmental specifications. (It did, however, demonstrate with reasonable certainty that such a stable frequency source was practical and could eventually be made to meet reasonable environmental conditions consistant with such a state-of-the-art device.

The most difficult environment imposed on this device was the high temperature of 85°C. Any such device having a series of cascaded stages, each operating at or near the maximum power level will exhibit high temperature degradation. The degradation of each stage by itself may be small, but when many are cascaded the overall degradation may be quite high. In several stages, the most advanced high power varactors available at the time were utilized in an attempt to reduce the high temperature degradation. Even though a substantial improvement was obtained, the degradation was still somewhat marginal.

The power amplifier stage provided considerable trouble throughout the program, not so much as an amplifier by itself but as a varactor multiplier driver. The breadboard design proved inadequate because of the transistor type used. This transistor (2N4431) was found to be very sensitive to load variations, which is a unique distinction of varactor multipliers. A redesign was made for the engineering model utilizing a different transistor with much better results. However, elaborate temperature testing was not done to completely substantiate the new design. It was concluded that the power amplifier frequency should be at the lower frequency of 162 MHz. The main reason being that transistors with a lower cutoff frequency can be utilized which are less sensitive to load variators and do not generate low frequency spurious as readily.

4.2 Recommendations

The engineering model in general performed reasonably well under normal operating conditions. There are two possible areas or modules which may require additional redesign to improve overall performance with temperature.

(A) The need for a more stable and spurious free power amplifier could be obtained by lowering its frequency to 162 MHz and adding a high power doubler to the X6 multiplier block.

(B) Control the frequency drift with temperature of the X to Ka band tripler by fabricating it of annealed invar or redesign to increase the bandwidth.