final report

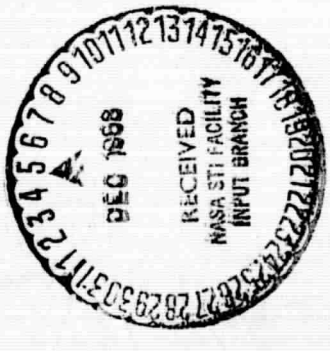
mariner mars power system optimization study

Prepared by
FRED S. OSUGI

JPL CONTRACT NO. 952151

TRW NO. 10247-6001-T0-00
1968 NOVEMBER 11

Prepared for
JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE OF TECHNOLOGY
Pasadena, California



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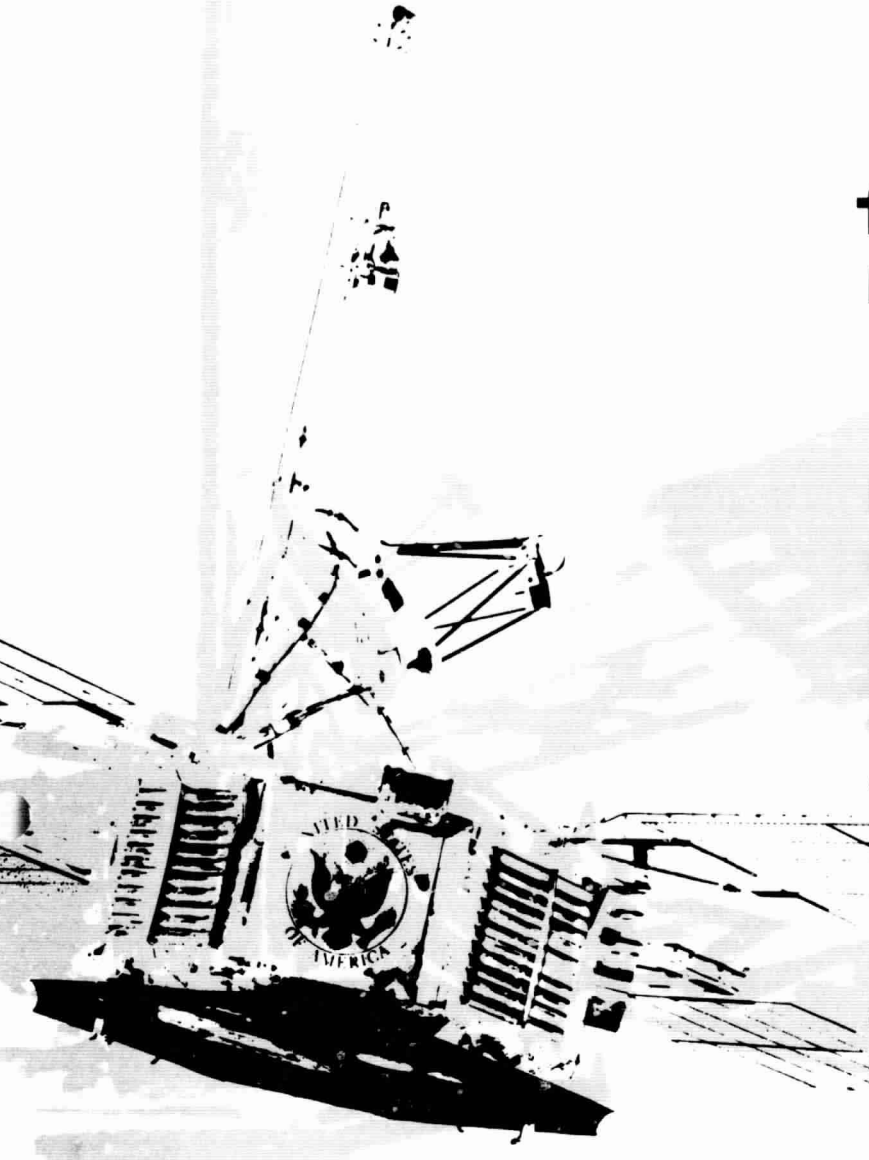

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ABSTRACT

An optimum Mariner-Class spacecraft electric power system which provides improved utilization of solar array power and greater reliability than the present Mariner Mars power system is presented. The optimum system is applicable to both a Mars flyby and orbiter mission and is characterized in terms of weight, size, parts, power/energy margins, telemetry requirements, circuit types and redundancy, major performance characteristics, and functional features. A multiplicity of possible solar photovoltaic power system configurations were fully synthesized and evaluated. The recommended design incorporates redundancy, automatic protection and limiting, and failure mode detection and switching to improve power system reliability. Areas where improvements can be made in the existing Mariner power system are discussed.

FOREWORD

This Technical Report, Mariner Mars Power System Optimization Study, was prepared by Members of the Technical Staff of TRW Systems for the Jet Propulsion Laboratory under JPL Contract 952151. Acknowledgment is expressed to the personnel named below for their valuable contributions to this effort: H. M. Wick, JPL technical representative, for his technical direction and guidance; J. J. Biess, W. G. Binckley, D. L. Cronin, J. E. de Castro, H. E. Gavira, S. Green, C. C. McCraven, K. H. Meissner, M. J. Milden, R. A. Rubin, W. H. Wright, who provided significant technical contributions to this study; and S. P. Petralia for editorial direction.

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1. INTRODUCTION

This final report covers work performed by TRW Systems under JPL Contract 952151 entitled, "Mariner-Mars Power System Optimization Study." The report covers the period of 1968 March 4 through 1968 August 30.

The prime objective of the study was directed toward the development of an optimum Mariner-class spacecraft power system to provide improved utilization of solar array power, greater reliability, and higher performance than the present Mariner-Mars power system.

The present Mariner-Mars power system design draws heavily on the design and techniques utilized on past JPL spacecraft, namely Mariner-Venus and Mariner-Mars. The basic power system configuration can be traced back to the early Venus mission (1962). The power system has been utilized successfully on previous Mariner missions namely, Venus (1962), Mars (1964), and Venus (1967). A Mars flyby is scheduled for launch in 1969. Due to time and schedule limitations, the existing power system design has been restricted to earlier hardware technology. The present study, "Mariner-Mars Power System Optimization Study," was undertaken for the purpose of analyzing the present Mariner-Mars power system and developing a significantly improved design for the next generation (1970 to 1975), Mars spacecraft power system. The ultimate goal of this study was to develop a power system design sufficiently detailed that it can be used as a hard reference from which a feasibility model (engineering model/breadboard) can be constructed.

2. SUMMARY

Primary consideration was given to circuit configurations which would result in maximum utilization of solar array power and provide maximum reliability for both normal and abnormal modes of operation. Weight, reliability, solar array power utilization, system and equipment interactions, complexity, cost, testability, performance, and availability of equipment were factors considered in arriving at the optimum system.

An optimum system applicable to both the flyby and orbiter mission has been developed and characterized in terms of weight, size, parts, power/energy margins, command and telemetry requirements, circuit types and redundancy, and major performance characteristics, along with a functional description. Detailed comparisons of the advantages and disadvantages of the recommended system with respect to the existing Mariner-Mars system have been made. Section 3, Recommended System, covers the aforementioned items.

Section 4, Mission and Spacecraft Analysis, covers the mission characteristics, the selection criteria, design guidelines, and load power requirements as a function of mission phase.

A multiplicity of possible solar photovoltaic power system configurations (Section 5) for the specified spacecraft power requirements were synthesized, evaluated, and screened. A computer program developed by TRW on JPL Contract No. 951574 was utilized during the preliminary power system configuration tradeoffs to select desirable systems with respect to weight, reliability and power utilization. The initial screening process culminated in the selection of five model systems (including the existing Mariner-Mars system) which were subjected to further detailed design tradeoffs.

Section 6, Analysis of the Model System Equipment, covers in detail the design and performance characteristics of the equipment comprising the power systems: solar array, battery, array control, power conditioning, battery charger, and power switching and control. The existing Mariner-Mars equipment design has been evaluated. Areas where improvements can be made are identified.

No attempt has been made in this study to optimize the existing solar array design nor extend the solar array technology. These areas require extensive effort and are considered beyond the scope of this study. Electrical output characteristics (I-V curves) based on the existing MM '69 solar panel design have been computed to allow for power system configuration tradeoffs. All the factors necessary for power output predictions, such as cell characteristics, temperature, fabrication losses, radiation damage, etc., have been accounted for.

A silver-zinc (Ag-Zn) battery type is a logical choice for the missions of concern because of the requirement for a low number of charge/discharge cycles, a relatively short life, and the weight constraints. The primary analysis was oriented toward improving battery reliability and providing proper charge control to extend battery life.

The power source control is utilized to condition/control solar array or battery power in a form compatible with the power user voltage regulation requirements. There are two basic approaches for source control: (1) separate controls for both solar array and battery and (2) single control. There are numerous ways in which circuits can be configured to perform these functions, depending on the solar array voltage variations, battery voltage characteristics, and load voltage requirements. The advantages and disadvantages of these circuit approaches such as shunt regulators, zener limiters, series bucking regulators, boost regulators, buck-boost regulators, and maximum power tracking regulators have been fully evaluated both on an equipment level and on a system level.

Load power conditioning is used to convert bus power to a form suitable for spacecraft power users. The power distribution approach (ac) dictated by the Mariner-Mars spacecraft user equipment restricted the power conditioning equipment to what are commonly known as inverters. Various inverter configurations were analyzed and evaluated. In addition, tradeoffs were made to determine the optimum frequency to distribute ac power to the user loads.

Unlike earth-orbit missions, battery charging efficiency is not of primary concern for the identified missions. Emphasis was directed toward simple and reliable battery-charging circuits such as series dissipative regulators and resistors. Various switching type chargers were eliminated since the efficiency improvement was not worth the additional circuit complexity.

The function of the power distribution circuitry is to switch power on and off to spacecraft users in response to onboard or ground-initiated commands. Because these functions are essential to mission success, a reliable circuit design is highly desirable. Various circuit approaches, ranging from nonredundant to fully redundant designs have been synthesized and evaluated.

Section 7, Systems Comparison and Selection, describes the significant advantages, disadvantages, weight, and reliability tradeoffs for each of the five model power systems.

Section 8, Failure Modes and Effects Analysis, describes the analysis performed in determining the modes of failures for a power system and developing techniques and methods capable of detecting these potential or actual failures. After detection, remedial action must be taken to isolate the fault, and adequate protection must be provided to prevent damage to other power system components. Detailed evaluation has also been made of actual circuit design techniques to circumvent failures via approaches such as standby/parallel redundancy, majority voting, and quad redundancy.

The reliability assessments for the various power systems, including the Mariner system, are included in the appendices.

3. RECOMMENDED SYSTEM

3.1 SUMMARY

The establishment of an optimum power subsystem configuration for a Mariner-class spacecraft is governed primarily by the need for improvements in solar array utilization and reliability over that of the existing Mariner-Mars power system.

The functions of the electric power subsystem are to:

- Provide continuously all electrical power to the Mariner spacecraft during all phases of the mission.
- Control the electric power, convert it to various voltages, and regulate it as necessary.
- Provide load power switching and control.
- Provide a master frequency reference.

The chief characteristics of the recommended electric power subsystem are summarized in Table 3-1. The subsystem consists of a solar array, two Ag -Zn batteries, redundant buck-boost regulator, power source logic, power control unit (battery chargers, momentary booster, current monitors), power distribution unit, 2.4 kHz inverter, and 1ϕ, 3ϕ, 400 Hz inverter.

The recommended system is as shown in the block diagram of Figure 3-1. This system provides a regulated 50 Vdc ±1% bus for spacecraft loads such as heaters, TWT converter, and the ac power-conditioning inverters. The buck-boost regulator is used to convert either the solar array or battery voltage to the regulated dc level. The major advantages of the buck-boost approach are its conversion efficiency (92%) and ability to perform the power source regulation in just one unit. The present system requires zener diodes to limit the maximum solar-array voltage and requires a boost regulator for conversion of solar array or battery voltage to the regulated dc level.

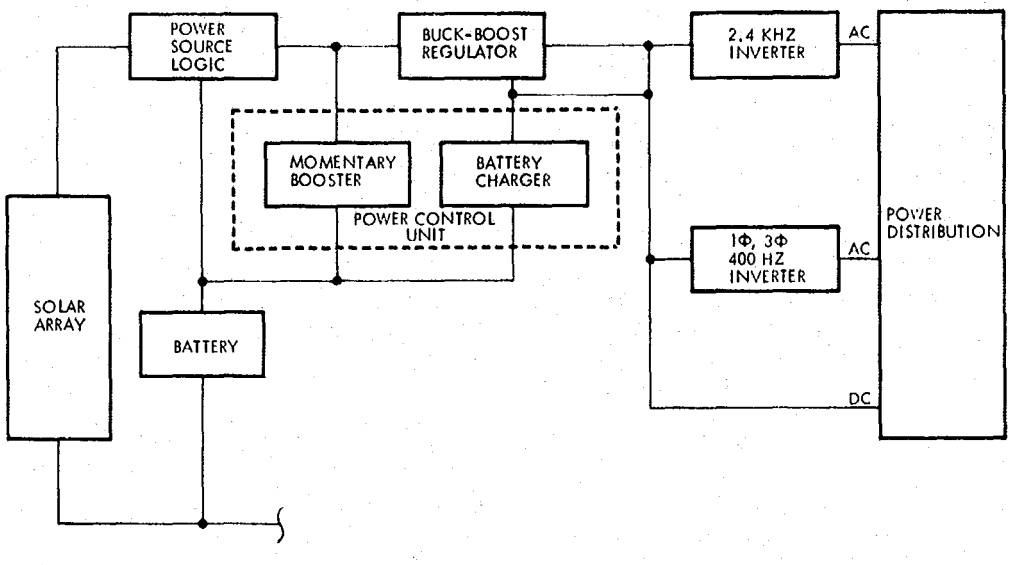
Battery discharge is performed via quad diodes. System failure modes and effects analysis has clearly shown the mission catastrophic effects due to either an open or shorted battery discharge diode. The battery-charging scheme is characterized by its simplicity, that is, using a current-limiting resistor and a switch used to terminate charging. Ground-backup capability is provided to override the automatic charge circuitry and allow manual battery charge control.

Power-system reliability has been enhanced through incorporation of current limiting in the buck-boost regulator and incorporation of a heater bus. The power to the heaters can be switched off by ground commands to assure the ability of the power system to elude a current-sharing mode (in event of a momentary booster failure) and also to permit the system to be powered down in event of an overload malfunction.

The failure detector requirements in the main power chain have been simplified and fail-safe circuitry has been incorporated. Power distribution circuitry has been made near fail-safe and is also protected against command failures. The number of power-conditioning units has been minimized (six units compared to the existing eleven units, including the zener diodes on the panels).

The 2.4 kHz inverter provides $^{+2}_{-3\%}$ ac squarewave power to the spacecraft engineering subsystems and the experiments. 3ϕ 400 Hz power feeds the gyro

Table 3-1. Preliminary Specification, Electric Power Subsystem



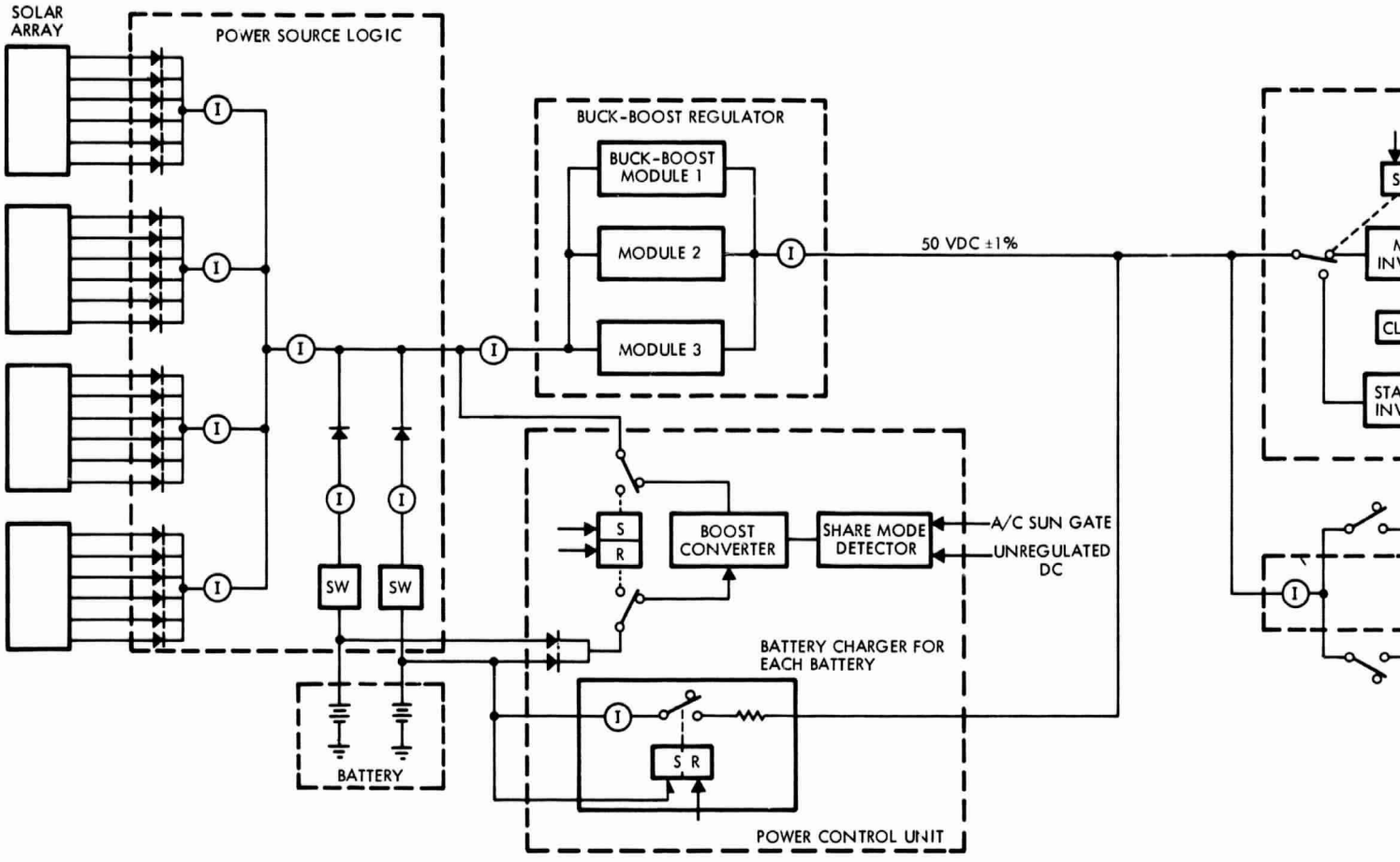
Subsystem Function: Generate, control, and condition electric power for the loads. Provide load switching. Store electric power in battery and control battery charging.

Performance Characteristics:

Solar array power (1.0 AU)	830 W
Solar array power after 3 mo in orbit (1.612 AU)	371 W
Main bus voltage	+50 Vdc ±1%
Main bus impedance	0 to 50 kHz, ≤1 ohm
Power regulation	Active buck-boost regulator utilizing parallel and majority voting redundancy
Reliability:	0.9706 for 1 yr

Physical Characteristics:

Total subsystem weight	113.77 lb, excluding solar array substrate and battery chassis



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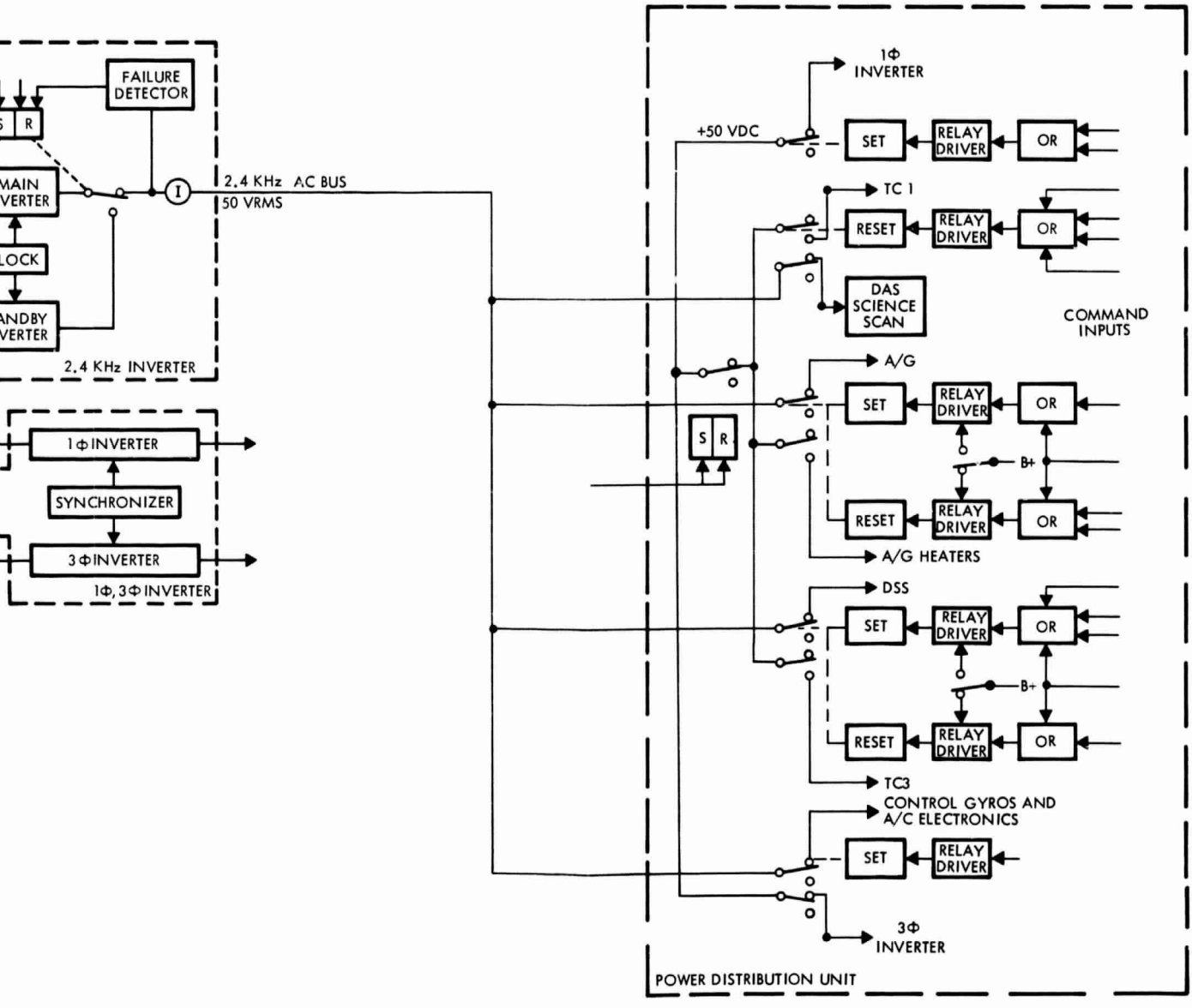


Figure 3-1. Recommended System Functional Block Diagram

Foldout Frame 2

assembly, and 1ϕ 400 Hz power is used for both the IR spectrometer and scan motors. A more complete functioning of the system and physical characteristics of its components are given in Subsection 3.2. Changes from the existing MM design are summarized in Table 3-2.

This section describes the operation and characteristics of the proposed design. Reference will be made to the appropriate sections in the report describing the alternative approaches that were investigated.

3.2 SUBSYSTEM CONFIGURATION

Of the many possible system configurations subjected to detailed investigations, the regulated bus approach utilizing an energy ladling buck-boost regulator offered the best overall system advantages. The comparisons between other competitive power systems are delineated in Section 7. The recommended design is based upon a regulated dc bus (50 Vdc ±1%), followed by conversion and regulation of that part requiring conditioning. A functional block diagram of the electric power system is shown in Figure 3-1.

3.2.1 Solar Array

The selected power system configuration is compatible with the voltage characteristics of the existing Mariner solar array. The solar array (summarized in Table 3-3) consists of four panels containing 78 solar cells in series and a total of 224 cells in parallel. The electrical output of the solar array has been computed, based on the existing panel characteristics. Details of these computations including the various degradation factors are described in Subsection 6.1. The calculated I-V characteristics at 1.0, 1.45, and 1.612 AU are shown in Figure 3-2. Maximum power vs AU is depicted in Figure 3-3.

3.2.2 Battery

The recommended battery design (summarized in Table 3-4) consists of two Ag-Zn batteries operating in parallel with individual charge control circuitry and discharge circuitry. Each battery consists of 18 cells in series and contains a nominal 25 A-H capacity, which is approximately half the capacity of the present Mariner '69 design. Reliability analysis has shown major overall system reliability improvements with redundant batteries. Each battery is sized to handle the maximum spacecraft loads for all modes requiring battery power. Weight estimates show a net weight increase of 6.1 lb (cell weight, charge/discharge control) compared to the existing nonredundant battery approach.

3.2.3 Solar Array/Battery Power Margins

Solar array power and battery energy margins were determined on the basis of the furnished load power requirements for a Mars Orbiter mission, the existing solar-panel design, and the performance characteristics of the recommended power-system design.

3.2.3.1 Battery Energy Requirements

Battery energy requirements for the various mission phases are calculated below:

Launch:	Unregulated dc:	68.3 W (Heaters + TWT converter output) = 27 + 41.3
	2.4 kHz:	188.95 W
	3ϕ 400 Hz:	9.0 W
		266.25 W

Table 3-2. Changes from Existing Design

Item	Existing MM Design	Recommended Design
1. Method of power source regulation	Zener limiter and boost line regulators	Buck-boost regulator
2. Power source current limiting	None	Current limiting in buck-boost
3. Unregulated load bus voltage	25 to 50 Vdc	50 Vdc ±1% (regulated bus)
4. Battery discharge diode	Single	Quad diodes
5. Battery charger	Series dissipative voltage regulator with current limiting	Current limiting resistor plus a switch to terminate charge
6. Charging current	≤ 1 amp	300 ±50 milliamp
7. Noncritical bus	None	Heater bus to allow temporary removal of heater power
8. Packaging	8.1 Power distribution dc heater distribution	Combined in one unit
	8.2 Power control battery charger	Combined in one unit
	8.3 Zener diodes, main boost regulator, standby boost regulator	Functions combined in one unit — buck-boost regulator
	8.4 Main 2.4 kHz inverter, standby 2.4 kHz inverter	Combined in one unit
9. TWT converter	Efficiency of 75%	• Redesign to increase efficiency to 92% • Reduce filter weights as a result of operating off regulated dc bus • Incorporate current limiting

Table 3-2. Changes from Existing Design (Continued)

Item	Existing MM Design	Recommended Design
10. Number of power conditioning units	10	6
11. Number of batteries	1	2
12. Reliability	0.8544	0.9706
13. Power distribution	Nonredundant	Redundant
14. 2.4 kHz failure detector	Nonredundant	Fail-safe design
15. Weight summary		
Zener diodes	4.0	
Main and standby boost line regulators	12.24	
Buck-boost regulator (redundant)		9.1
Power source logic	8.43	7.4
Power distribution	2.0	4.5 (includes redundant circuitry)
Heater and dc power distribution	2.0	
Power control	3.0	4.6
Battery charger	2.31	
Main and standby 2.4 kHz inverters	5.88	6.8 (includes failure detector and current monitor)
1ϕ, 3ϕ, 400 Hz inverter	3.87	3.87
Total power conditioning	43.73	36.27
Battery (less cover and chassis)	28.0	31.5
Solar array (less zener diodes and substrate)	46.0	46.0
TOTAL	117.73 lb	113.77 lb

Table 3-3. Preliminary Specification, Solar Array

Performance Characteristics	
Initial power output (1.0 AU)	830 W
Power output after 3 mo in MARS orbit (1.612 AU)	371 W
Reliability	1.0 for 1 yr
Physical Characteristics	
Total array area	83 ft^2
Total array weight (excluding substrate)	46.0 lb
Number array panels	4 per spacecraft
Cells per spacecraft	17,472
Cells per panel	4,368
Cells in series	78
Cells in parallel per panel	56
Solar Cell Characteristics	
Type	N on P silicon
Output	60.0 mW AMO at +28°C
Bulk resistivity	1 ohm-cm
Cell size	2 x 2 cm
Cell thickness	0.018 in.
Cover glass	Fused silica 0.020 in. thick
Ultraviolet reflective coating	0.410 micron cutoff

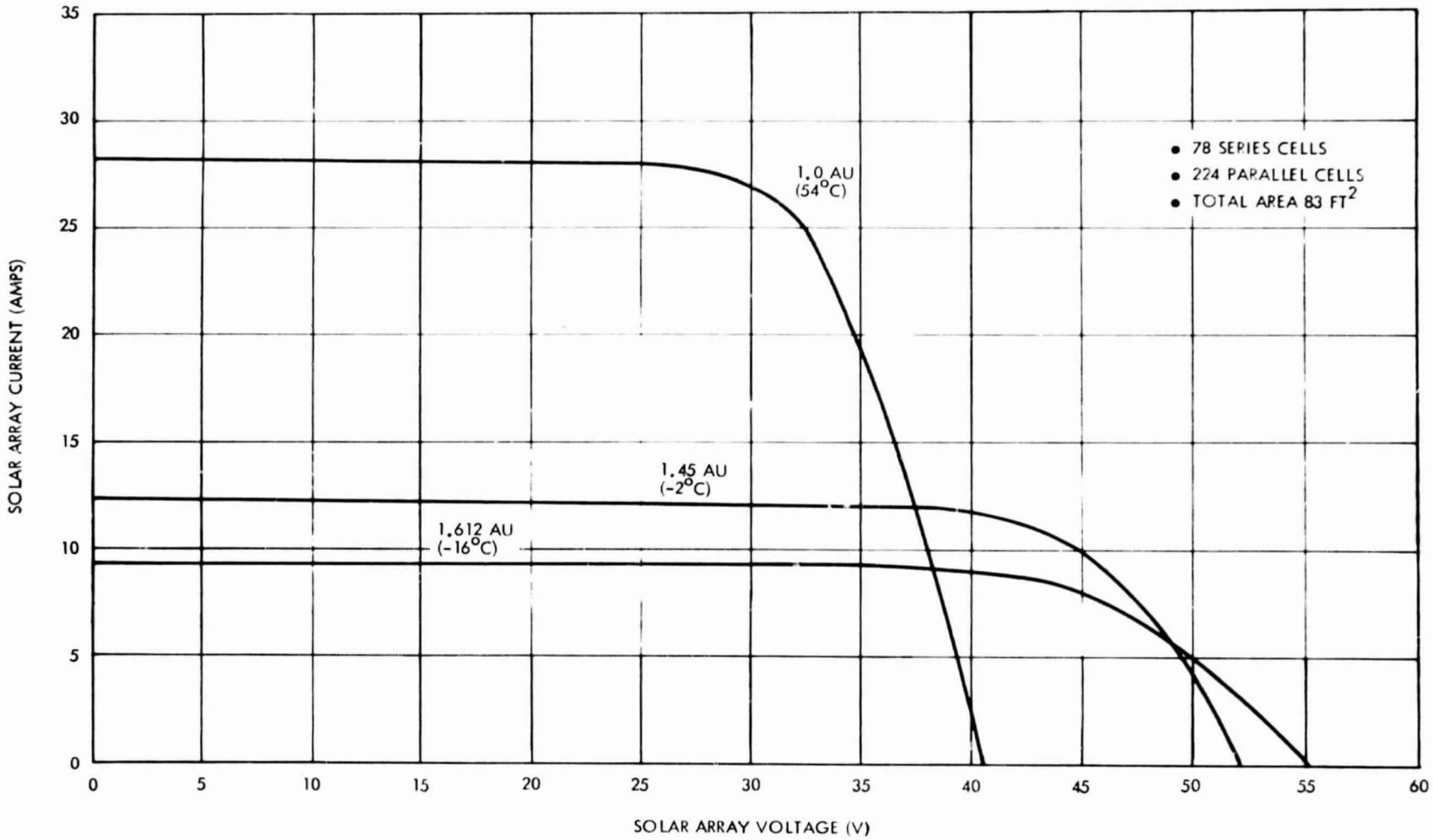


Figure 3-2. Solar Array I-V Characteristics for Existing Mariner '69 Design (Predicted)

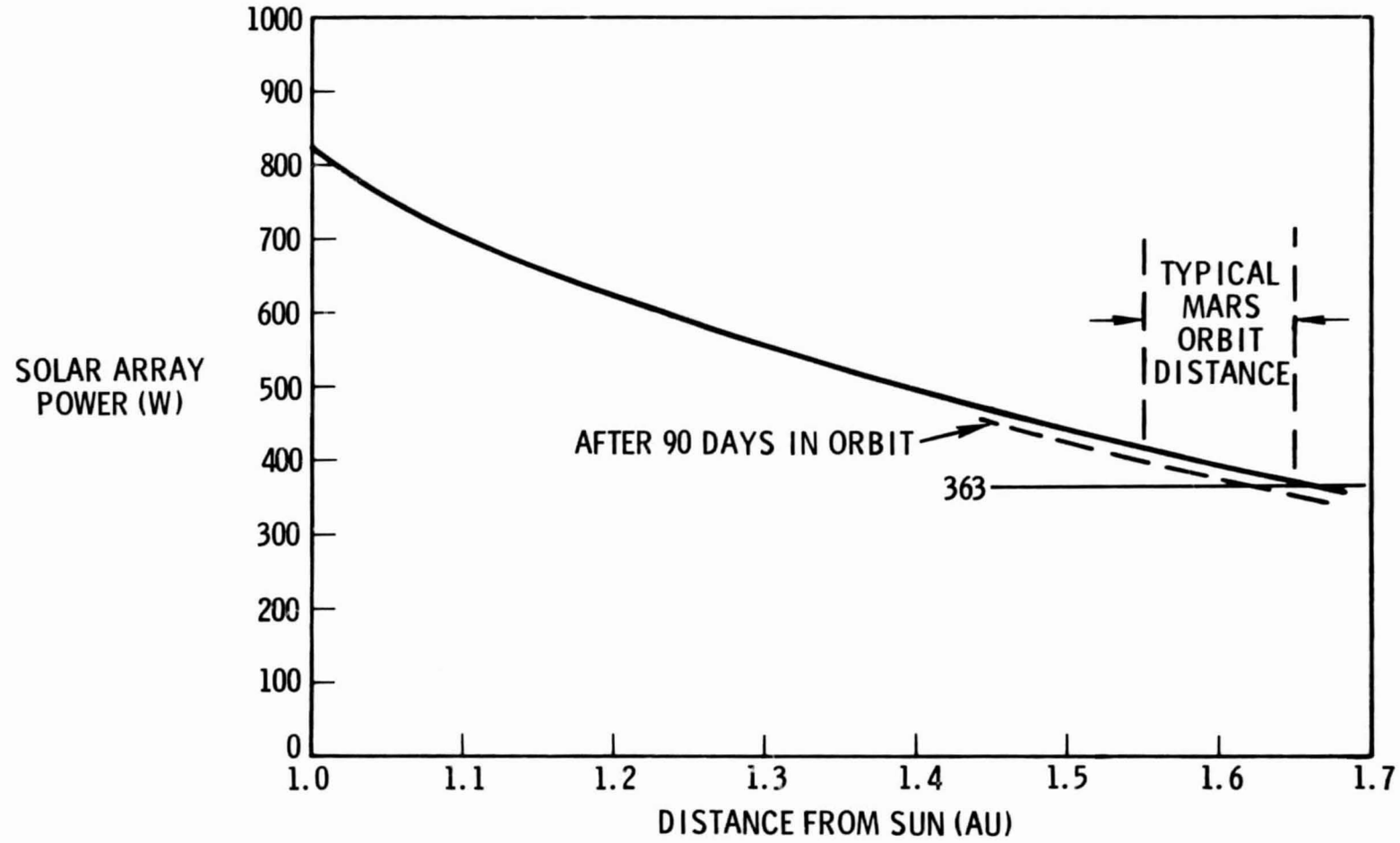


Figure 3-3. Solar Array Maximum Power Versus AU

Table 3-4. Preliminary Specification, Battery

Performance Characteristics	
Nominal capacity	50 amp-hr (total)
Voltage	25.8 - 34.6 Vdc
Average discharge current	15 amp (total)
Reliability	0.9917 for 1 yr
Physical Characteristics	
Battery type	Silver-zinc
Number of batteries	2
Number of cells	18 series connected per battery
Charge control sensing	Battery terminal voltage
Charge current	300 ±50 ma per battery
Size	11 x 9 x 8 in. for two batteries contained in common chassis
Weight	31.5 lb total (excludes cover and chassis)

From Table 7-2 the solar array utilization factor for the buck-boost system is 84.4% (with improved TWT converter efficiency). The battery utilization will be lower on account of two factors:

a. Lower buck-boost efficiency when operating at battery voltages: -2%

b. Losses in quad battery discharge diodes: -7%

Battery utilization factor for the recommended system is: 84.4% less 9% losses $\approx$ 84.4% (91%) = 76.7%.

$$\text{Required energy} = \frac{110 \text{ min}}{60 \text{ min/hr}} \frac{266.25}{0.767} = 638 \text{ W-hr}$$

The energy requirements for the various Mars Orbiter mission phase are tabulated in Table 3-5.

Table 3-5. Battery Energy Requirements

Mission Mode	Duration (min)	Energy (W-hr)	Available (W-hr)	Depth of Discharge (%)
Launch and acquisition	110	638	1350	47.2
Midcourse maneuver	65	512	1150*	44.5
Orbit insertion	65	468	950**	49.3
Orbit time	65	468	950	49.3

*Assumption: 15% capacity degradation
**Assumption: 30% capacity degradation

3.2.3.2 Solar Array Power Requirements

Calculations have been made on the solar array power requirements for the major mission modes, based on the power profile (Table 4-2) and solar-array power utilization of 84.4% (see Section 7 for details). Figure 3-4 depicts the power requirements for both the battery and the solar array as a function of mission phase. The sizing of the solar array is dictated by the TV sequence mode (363 W). The solar array margin at the critical design point (TV sequence) is the difference between the solar array capabilities (shown in Figure 3-3) and 363 W. Previous studies performed by TRW on the Voyager progran show that, for a Mars Orbiter mission, AU distances can vary from 1.55 to 1.65. The crossover point is 1.62 AU at which the solar array just satisfies the TV sequence load requirement; as such, the array power margin is highly dependent on the actual launch date with the present solar panel area constraint of 83 sq ft.

Examination of the load profile (Figure 3-4) and the solar array power availability (Figure 3-3) shows that substantial power margins exist for other mission modes. For example, during cruise, the power available is 450 to 700 W, while the required power, including battery charging, is merely 370 W. At encounter, the power available at 1.55 to 1.60 AU is 420 to 390 W, respectively; as such, ample power is available for both the far encounter and for encounter playback modes. During Mars orbit, substantial power margins exist for the cruise, Earth occulation, and playback modes since these loads are approximately 60 to 100 W less than the TV sequence load (which the solar array is sized to meet).

Figure 3-4. Solar Array/Battery Requirements Versus Mission Phase

3.2.4 Buck-Boost Regulator

The primary requirement of the unit is to convert either battery or solar array voltage (25 to 65 Vdc) to a regulated 50 Vdc ±1%. The main features of the regulator are summarized in Table 3-6.

3.2.4.1 Basic Operation

Figure 3-5 illustrates the basic energy ladling circuit, supplying a load resistance, R. The energy-storage inductor, L, has a linear flux versus MMF characteristic with a slope, K. It has a primary winding, N_1, and a secondary winding, N_2, with magnetizing inductances, $L_1 = K N_1^2$ and $L_2 = KN_2^2$, respectively. The transistor switch, Q, is externally controlled to turn on and off cyclically within a time period, T. A steady-state operating cycle of this circuit with input voltage e_{in} and output voltage e_o is described in the following paragraphs.

During the time interval T_{on} when Q, the transistor, is switched on by the base drive circuit, the current i_1 in N_1 causes the inductor to absorb energy from the input source. Meanwhile, diode CR blocks any current in N_2. Thus, a given quantity of energy is stored in the inductor during T_{on}. When Q is turned off, the MMF continuity demanded by the inductor causes i_2 to flow immediately through the diode to charge the filter capacitor, C, and load, R. The energy stored in the inductor during T_{on} is thus released to C and R during T_{off}.

Figure 3-6 illustrates the circuit waveforms during one steady-state operating cycle, assuming ideal components in Figure 3-5. Voltage $e_1 = e_{in}$ across N_1 during T_{on} causes i_1 to increase from i_a to i_b at a constant rate e_{in}/KN_1^2, while i_2 is 0 in N_2. At the end of T_{on}, the continuous MMF acting on the inductor causes $i_2 = N_1 i_b / N_2$ to start flowing in N, and decreasing at a constant rate e_o/KN_2^2. During this time interval, T_{off}, $i_1 = 0$. Since the increase of MMF $N_1 \Delta i_1$ during T_{on} should be identical to its decrease during T_{off} for a steady-state operation to exist,

$$N_1 \, T_{on} \, e_{in}/KN_1^2 = N_2 \, T_{off} \, e_o/KN_2^2$$

from which

$$e_o = N_2/N_1 \, T_{on}/T_{off} \, e_{in}$$

Thus, despite a variation in input voltage, a constant output voltage can be maintained by controlling accordingly the ratio T_{on}/T_{off} with the base drive circuit.

Figure 3-7 shows the circuit waveforms before and after the occurrence of an output short at $t = t_1$ when the power transistor, Q, is conducting. Current i_1 does not increase abruptly, as Q sees only the inductor with inductance L1 and not the short circuit in the output. While $N_1 \, T_{on} \Delta i_1 = N_2 \, T_{off} \, \Delta i_2$ for each cycle before the short condition at $t = t_1$, $N_1 \, T_{on} \Delta i_1 \, N_2 \, T_{off} \, \Delta i_2 = 0$ after $t = t_1$ as the output voltage becomes 0 during T_{off}. Therefore, the current level of i_1 is steadily increased on each succeeding cycle. Current limiting is provided as shown in Figure 5-2. Thus during either a startup or a severe output short, no power-conditioning component is subject to excessive stress of any voltage or current transients. This is in contrast to the more conventional designs where heavy inrush current may occur during startup and an output short is reflected back to the power source within a half-cycle of the operating frequency. This immunity of the power components in the energy ladling circuit to high-voltage and/or high-current transients greatly enhances the system reliability.

Table 3-6. Preliminary Specification, Buck-Boost Regulator

Functions

- Conditions raw power from the solar array or battery to a regulated dc voltage.
- Provides current and voltage telemetry.

Performance Characteristics

Input voltage	25 to 65 Vdc
Output power	240 to 340 W
Output voltage	50 Vdc
Regulation	±1 percent where regulation is defined as the maximum deviation of output voltage from the nominal due to combined effects of initial adjustment, input line variation, temperature coefficient, load range, and stability.
Rated efficiency	92 percent at 340 W output and input voltage range 45 to 50 Vdc
Ripple	400 mV peak-to-peak
Spikes	700 mV peak-to-peak
Transient response	Maximum voltage deviation of ±7% for 50-W load change, ±1% regulation within 20 msec

Reliability	0.9998 for 1 yr
Redundancy	Parallel-operating power stages and majority-voting control circuitry

Physical Characteristics

Size	5 x 7 x 6 in.
Weight	9.1 lb

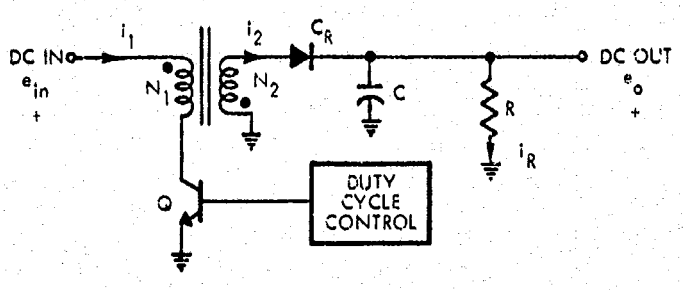
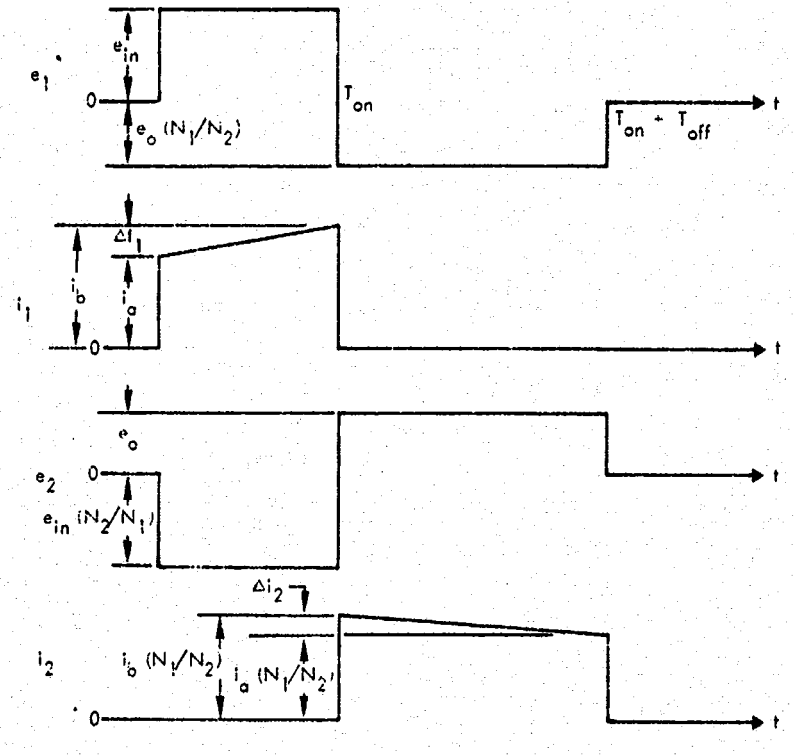


Figure 3-5. Basic Energy Ladling Circuit



CIRCUIT WAVEFORMS

BASIC OPERATING EQUATION

$$e_o = e_{in} \frac{t_{on}}{t_{off}} \frac{N_2}{N_1}$$

Figure 3-6. Circuit Waveforms

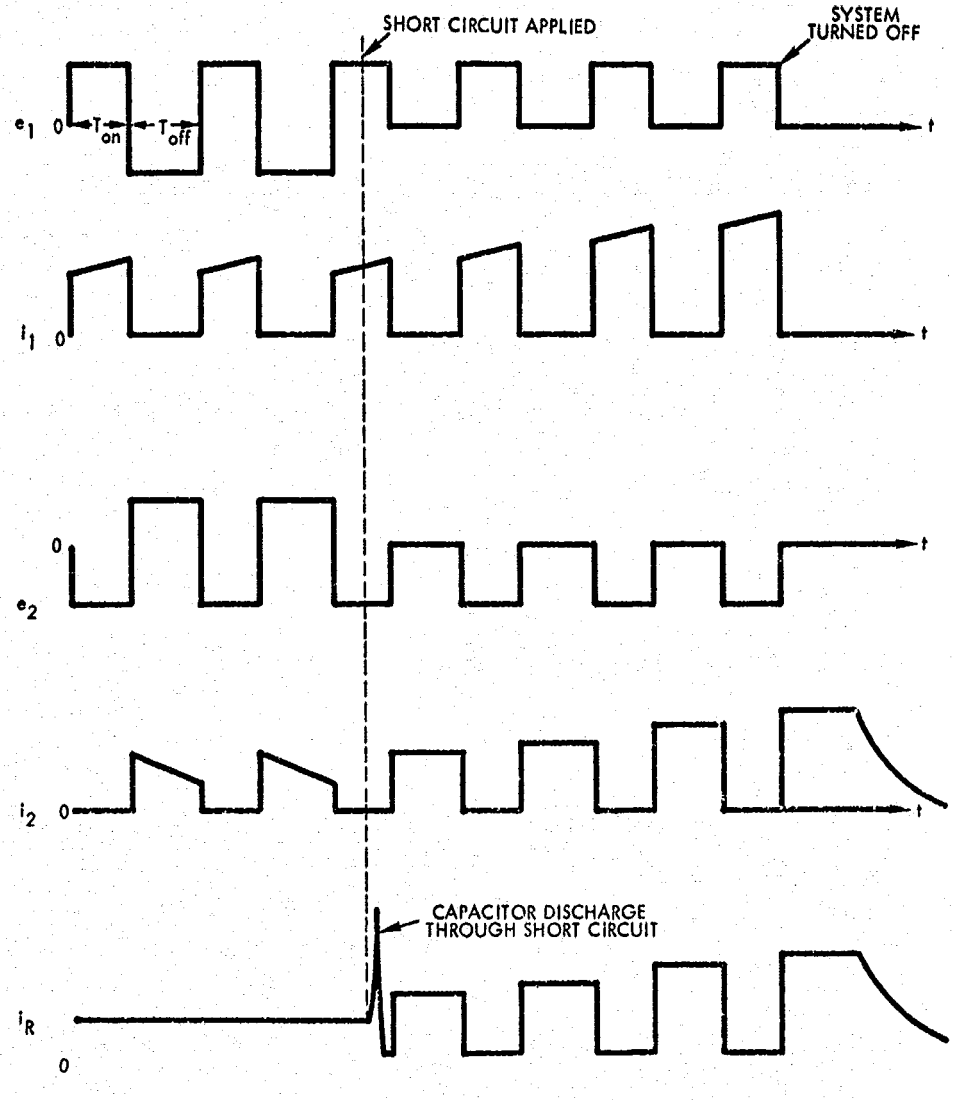


Figure 3-7. Circuit Waveforms During Output Short

In addition, unlike some of the more conventional approaches, the output power of the energy ladling circuit is handled only by a single dc-to-ac inversion process into which nondissipative regulation can be easily incorporated. This feature generally results in a simpler and more efficient circuit for the power-conditioning system.

3.2.5 Battery Charger

The proposed charger consists of a current-limiting resistor (quad), a majority voting battery voltage sensor, a relay, and relay driver. The circuit operates as follows:

a. Battery charging is initiated by a command from the CC&S or by a ground command.

b. Battery current limiting is provided by the current-limiting resistor between the regulated 50-Vdc bus and the battery. A 60Ω resistor will limit the charging current to 300 ±50 ma.

c. Battery charging is terminated when the terminal voltage reaches 35.4 Vdc. Two-out-of-three majority voting circuits are provided for fail-safe operation.

d. The relay driver circuitry is also redundant which is similar to the relay driver configuration in the power distribution circuitry.

e. Ground back-up for charge termination is provided.

The primary advantages of this approach are:

1. Simplicity in charging
2. No active series voltage limiter nor current limiter
3. Control is done at a low power level, enhancing redundancy methods with low attendant weight increases.

Alternative battery-charger schemes, both passive and active, have been evaluated and discussed in Subsection 6.10. Both the battery charger and the momentary booster (described in an ensuing section) will be contained in a unit known as a power control unit (summarized in Table 3-7).

3.2.6 Momentary Booster

The momentary booster is similar to the existing Mariner unit. The booster is energized wherever undesirable load-current sharing exists between an oriented solar array and the battery. The logic consists of an "AND" function occurrence of a sun signal (array oriented) and the solar-array operating voltage dropping toward battery voltage. Ground backup capability is provided to get out of the sharing mode via removal of the experiment and heater loads. A discussion of such follows:

3.2.6.1 Load Sharing

An analysis has been made to determine whether the existing MM '69 configuration has the capability to remove sufficient loads to get out of a load-sharing mode.

Table 3-7. Preliminary Specification, Power Control Unit

Functions

- Controls battery charging and termination.
- Provides momentary boosting during load-sharing mode.

Performance Characteristics

Battery Charger

Input voltage	50 Vdc ±1%
Charging current	300 ±50 ma/battery
Charge termination voltage	35.4 ±0.2 Vdc

Momentary Booster

Input voltage	25 to 35.4 Vdc
Output voltage	44 Vdc min
Output power	150 W at 26 Vdc
Output impedance	4.5 ohms

Reliability 0.996 for 1 yr

Redundancy

Momentary booster:	Nonredundant
Battery charger:	Majority voting and component redundancy

Physical Characteristics

Size:	7 x 7 x 6 in.
Weight:	4.6 lb

Table 3-8 lists the fixed loads and the loads which can be switched.

Table 3-8. Fixed and Switchable Loads

Fixed Loads	
Equipment	2.4 kHz
TWT (Hi)	89 W
RFS	32.2
CC&S	19.0
FTS	15.0
FCS	3.2
PWRD	2.25
Total	160.65 W
dc Heaters	15 W
Total Fixed Loads:	2.4 kHz 160.65 W dc 15.0 W

Switchable Loads	
DSS (on)	10-23 W (2.4 kHz)
DSS (off)	10 W (dc)
Experiments (on)	71 W (2.4 kHz)
Experiments (off)	50 W (dc)

$$\text{Solar Array Power} = \frac{160.65}{\eta_{2.4}\eta_{BR}} + 15$$

$\eta_{2.4}$ = Efficiency of 2.4 kHz inverter

= 91%

η_{BR} = Efficiency of boost regulator = 89%

The minimum switchable load condition is when the DSS and experiments are turned off; as such, the heaters will consume 60 W.

Solar array power requirements:

$$\text{Fixed loads: } \frac{160.65}{0.91\,(0.89)} + 15 = 198 + 15 = 213 \text{ W}$$

$$\text{Heater power} = \frac{60}{0.91\,(0.89)} = 74.0$$

Total array power required = 213 + 74 = 287

The array capability (during a load-sharing mode) at the unregulated bus voltage of 25 V (for minimum battery voltage) is 25 V (12A) = 300 W at 1.45 AU and 25(9.25) = 231 W at 1.612 AU. These power capability computations are based on the solar array I-V characteristics depicted in Figure 3-2. As such, for the Mars Orbiter mission where the AU range can extend to 1.612 and greater, load sharing cannot be terminated unless the loads can be reduced to 231 W or less. For the flyby mission (1.45 AU), the present MM system design is adequate for ground backup control of the undesirable load sharing condition. Spacecraft loads for the proposed power system design can be reduced to 197 W by removing heater power momentarily via ground command. This is accomplished by a switchable (on-off) heater bus. Therefore, with this backup capability, redundancy is not essential in the momentary booster design.

3.2.7 2.4 kHz Inverter

The 2.4 kHz inverter (summarized in Table 3-9) consists of a main and standby inverter, which converts the regulated input (50 Vdc) to 50 Vrms $^{+2}_{-3}$% ac. Included in this unit is a frequency standard created by a crystal oscillator, inverter failure detector, and a current monitor. The primary failure detector requirements have been greatly simplified as discussed in Subsection 6.7.

3.2.8 1ϕ, 3ϕ Inverter

The 1ϕ, 3ϕ 400 Hz inverters (summarized in Table 3-10) convert the regulated 50 Vdc into single and three-phase 400 Hz square wave outputs that are synchronous with the 2.4 kHz square wave. Tradeoff studies on TRW spacecraft designs have shown that a nonredundant gyro package is usually less reliable than a nonredundant 3ϕ inverter; as such, overall spacecraft system reliability tradeoffs would show that making the 3ϕ inverter redundant is not warranted. The relatively low power stresses (15.5 W), the low operating duty cycle operation of the 1ϕ inverter, and its inherent design simplicity does not warrant full redundancy (standby) unit with a failure detector. Partial redundancy, as described in Subsection 6.8, can be incorporated for a small weight increase.

3.2.9 Power Source Logic

The power source logic (summarized in Table 3-11) contains the solar cell string blocking diodes, battery discharge diodes, internal/external power control, and current and voltage telemetry.

3.2.10 Power Distribution

The proposed power distribution (summarized in Table 3-12) consists of the following:

a. Redundant switching and control circuitry for DAS, science, scan on/off, approach guidance on/off, DSS on/off, attitude control on/off, heater bus power on/off.

Table 3-9. Preliminary Specification, 2.4 kHz Inverter

Functions

- Converts the main bus voltage to 50 Vrms ac at 2.4 kHz.
- Provides reference frequency source.

Performance Characteristics

Input voltage	50 Vdc ±1%
Output	
Voltage	50 Vrms
Regulation	+2, -3%
Load	90 min/195 max W
Spikes	5 V max, 5 μsec duration
Rise/fall time	5 ±4 μsec
Power factor	0.95 lag min
Efficiency	91 percent at 187 W output
Frequency	
Sync	2400 Hz ±0.01%
Free run	2800 Hz ±5%

Reliability 0.9994 for 1 yr

Redundancy

Power handling stages	Standby
Frequency source and low level drive	Fail-safe
Failure detector	Fail-safe

Physical Characteristics

Size	6 x 6 x 7 in.
Weight	6.8 lb

Table 3-10. Preliminary Specification, 1φ, 3φ, 400 Hz Inverter

Function

- Converts main bus voltage to 1φ and 3φ ac power synchronous with the 2.4 kHz frequency.

Performance Characteristics

	1φ	3φ
Input voltage	50 Vdc ±1%	50 Vdc ±1%
Output		
Voltage	28 Vrms ±5%	27.2 Vrms ±5% line-to-line
Load	12 min/21 max W	9 min/15 max W
Wave shape	Square wave	Quasi-square wave, no third harmonic
Rise/fall time	≤ 20 μsec	To be determined
Lagging power power	0.8 min	0.5 min
Spikes	2 V max	To be determined
Efficiency	83% at 15 W	77% at 9 W
Frequency	400 ±0.01%	400 ±0.01%

Reliability 0.9967 for 1 yr for 1φ and 3φ inverter

Redundancy

- Fully redundant bias supply and 2.4 kHz excitation for synchronizer
- Majority voting synchronizer

Physical Characteristics

Size	6 x 5 x 4.5 in.
Weight	3.87 lb

Table 3-11. Preliminary Specification, Power Source Logic

Functions

- Provides diode isolation for solar panel sections
- Provides battery discharge
- Provides control for external power source or internal battery to the system
- Provides current and voltage telemetry

Performance characteristics

Maximum power dissipation (sunlight)	6.5 W in blocking diodes
Maximum power dissipation (maneuver)	20 W in quad battery discharge diodes
Reliability	0.9904 for 1 yr
Redundancy	Quad battery discharge diodes

Physical characteristics

Size	5 x 7 x 4.5 in.
Weight	7.4 lb

Table 3-12. Preliminary Specification, Power Distribution Unit

Functions	
• Controls and distributes ac and dc power to experiments, heaters, and spacecraft power users.	
Performance characteristics	
Input voltage	50 Vdc ±1%
	50 Vrms +2/-3%, 2.4 kHz
Command signal	100 msec, 30-Vdc pulse
Output voltage	50 Vdc ±1%
	50 Vrms +2/-3%, 2.4 kHz
Reliability	0.999 for 1 yr
Redundancy	Fail-safe design
Physical characteristics	
Size	6 x 6 x 6.5 in.
Weight	4.5 lb

b. Dc heater fuses and distribution

c. Dc current monitor

The details of the selected redundant circuit design of the power distribution circuitry and the alternative approaches are described in Subsection 6.9.

3.2.11 Critical/Noncritical Buses

The investigation of the Mariner power distribution revealed only two types of subsystems whose busses can clearly be labeled noncritical: experiments and heaters. However, several other busses can be termed not quite critical either because they are used only in the beginning of the mission or because their failure would still leave some usefulness in the mission. These busses are:

a. Data Storage Subsystem (DSS): A failure of this subsystem would leave real-time telemetry available, but all stored data would be lost.

b. Inertial Platform: This assembly is not used after orbit insertion and orbit trim modes.

c. Flight Command Subsystem (FCS): After trajectory corrections, the mission can (should) be fully automatic, controlled by the upgraded CC&S Subsystem.

d. Scan Control Logic: This bus is almost critical because three out of four experiments lose most of their meaning without pointing at Mars.

e. Pyro: Most of this subsystem's functions are performed early in the mission and the remaining functions (actuation of scan platform, IRS motor) occur at/near Mars encounter. It is doubtful that something can be gained by fusing the pyro bus, because the pyro subsystem includes current limiting resistors.

3.2.11.1 Undervoltage Protection

Undervoltage protection is usually incorporated in systems where repeated battery charge/discharge cycles occur (low-earth orbits, for example) in order to protect the spacecraft system from losing primary power. Protection is provided by automatically removing nonessential loads whenever the source bus voltage (battery) drops below a preset value. Undervoltage protection is not recommended for the flyby/orbiter mission for the following reasons:

a. Loads are either current limited or fused to protect against excessive power drains.

b. Telemetry and ground commands are available to remove nonessential loads in the event of system faults.

c. Current limiting is provided in the buck-boost regulator to allow sufficient time for corrective action to be taken.

Note: In low earth orbits battery, undervoltage can occur due to gradual capacity degradation as a function of cycling or insufficient recharge in a given orbit for various reasons such as low array capacity, load malfunction, battery charger malfunction. The probability of the occurrence of battery undervoltage for a Mars flyby/orbiter mission is minimized by the long recharge time, the relatively low depths-of-discharge ($\leq 50\%$), and by only four charge/discharge cycles.

3.2.11.2 Power Subsystem Grounding

The proposed power subsystem will have three classes of buses which are dc decoupled from each other: the primary bus, connecting array and battery to the buck-boost regulator; an intermediate bus connecting the buck-boost regulator to the inverters and to the TWT converters; and secondary buses beyond these points.

The secondary buses are outside the scope of this study, but the grounding of the intermediate bus must be considered. There are three choices: to leave it floating, to ground it to the spacecraft reference plane at an optimum point, or to return the ground lead and combine the ground with the primary bus. It is not practical to leave it floating, but the two other choices warrant some discussion.

The intermediate bus contains rather noisy loads and one EMC consideration demands the placement of the ground as close as possible to either the noisiest or to the most susceptible unit in the (sub) system. It is probable that the TWT converter will satisfy both these requirements.

Whether this point should be made the single primary return point by grounding battery and array to it or whether there should be two ground points, one for the primary and one for the intermediate bus, is a question that depends on many system parameters, such as:

- Spacecraft equipment layout
- Bonding consistency and extent in the spacecraft reference plane
- Interference characteristics of end users (TWT, etc.)
- Isolation in inverters and converters
- Overall isolation between primary and intermediate bus.

The preliminary recommendation is to ground the intermediate bus near the TWT converters and to ground the primary bus near the battery separately. A final decision needs additional analysis and system tests to answer questions on the above parameters.

3.2.12 Telemetry Requirements

Due to the limited capacity of the MM '69 (or any) telemetry system, priorities must be developed for the parameters competing for assignments. Usually, the more important parameters are sampled at the faster rates, but there are exceptions; for instance, battery temperature which, in spite of its prime importance, can be sampled at fairly long intervals because of its slowly varying condition.

Telemetry priorities for the existing Mariner spacecraft are established in general terms. Engineering measurements are grouped as follows:

a. Measurements necessary for flight operations during a no-failure mission.

b. Verification of onboard events.

c. Measurements required for selecting between alternate modes of operation.

d. Measurements of subsystem parameters directly affecting system performance.

e. Measurements necessary to evaluate the performance of subsystems not previously flown.

f. Measurements necessary to evaluate the performance of subsystems previously flown.

This range of priorities has been used in Table 3-13 to establish a priority matrix for the electrical power subsystem parameters. Existing channels are shown with their number and proposed additional channels are shown with a P.

In the list of priorities given in the TRW proposal for this study, three priorities regarding power subsystem were given:

a. Measurements to evaluate subsystem performance and the need for backup modes.

b. Measurements necessary for ground checkout.

c. Performance check of black box parameters.

Priority b. warrants some further discussion. While it may appear desirable to have all parameters checked out through the telemetry system, it is not desirable to burden the telemetry system with data that is required only rarely or is of lesser importance. Several desirable measurements for ground checkout are the following:

a. Main/standby power select

b. 400 Hz, 3ϕ, output voltage

c. 400 Hz, 1ϕ, output voltage

The first of these parameters should be included in the telemetry assignments. A crude check of the 400-Hz equipment operation is available through telemetry of inverter input and/or output interfaces; therefore specific 400-Hz output voltage telemetry is not deemed mandatory.

Table 3-14 lists ranges and accuracies of the chosen analog parameters. Since the influence of other subsystems (thermal, etc.) is not known, the ranges listed are rather wide and can probably be narrowed during a spacecraft system study. The accuracies are a compromise between the aim of the component designer (usually 0.5 to 1%) and the realities of an economic telemetry system end to end (2 to 5%). In most cases, absolute accuracy is not as important as is the ability to show drift from an initial flight condition.

The limited engineering channel capacity of Mariner '69 has been almost fully assigned. Per the existing MM telemetry allocations, four Type 200 channels remain open as spares. Additional telemetry of power subsystem parameters must, therefore, be either programmed for these spares or it must displace a present channel assignment.

The following parameters, which are not telemetered now, are worth serious consideration. Most of them fall into Categories b and c listed in Paragraph 3.2.11.

A temperature monitor on the main inverter may permit temporary cooling (by switching off noncritical loads) in case of a partial overload.

A discrete signal showing the actuation of the A/C enable relay is recommended. This is necessary because only the start up of gyros is telemetered by a discrete in the attitude control subsystem and, in case of failure, the existing discrete would

Table 3-13. Priority Matrix for Electrical Power Subsystem

Description	Channel	a	b	c	d	e	f	Notes	Numerical Priority
PSL output voltage	114		x						4
Battery voltage	206	x						Note 2	1
Battery charger output current	216	x						Note 2	5
Array + X panel, current	221				x				14
Array + Y panel, current	223				x				15
Battery output current	225				x			Note 2	8
Array - X panel, current	222				x				16
Array - Y panel, current	224				x				17
Inverter output current	204		x					Note 2	2
Inverter output voltage	203			x					25
Boost regulator input current	226				x				9
Boost regulator output current	215			x				Note 1	24
400 Hz inverters, input current	205		x					Note 1	23
PSL dc bus current	300		x					Note 2	6
Standard cell current	424						x		20
Standard cell voltage	423						x		21
Rad res cell current	425						x		22
Battery temperature	405	x							3
+ X panel inboard temperature	439						x		18
+ X panel outboard temperature	419						x		19
+ X panel open	EC 1		x						10
+ Y panel open	EC 2		x						11
- X panel open	EC 3		x						12
- Y panel open	EC 4		x						13
Gyros ON	EC 1		x						7
Inverter temperature	P			x					14a
A/C enable discrete	P		x						7a
Main/standby channel discrete	P	x						Note 3	13a
Regulated dc voltage	P		x						3a
400 Hz, 1φ, output, discrete	P		x						23a
400 Hz, 3φ, output, discrete	P		x						22a
Battery cell voltage (3 cells)	P(x6)						x		25a

Note 1 — These channels could be eliminated, if absolutely necessary.
Note 2 — Higher sampling rate desirable.
Note 3 — Requires ground backup command.

Table 3-14. Analog Parameter Ranges and Accuracies

Description	Parameter	Range (max)	Desired Accuracy
PSL output voltage	V	20 to 80	±2%
Battery voltage	V	20 to 40	±2%
Battery charger output current	A	0.1 to 2	±3%
Array +X panel, current	A	1 to 8	±5%
Array +Y panel, current	A	1 to 8	±5%
Battery output current	A	0 to 30	±3%
Array -X panel, current	A	1 to 8	±5%
Array -Y panel, current	A	1 to 8	±5%
Inverter output current	Vrms	2.5 to 5	±3%
Inverter output voltage	Vrms	40 to 60	±2%
Buck-boost/regulator input current	A	5 to 30	±5%
Buck-boost/regulator output current	A	2 to 15	±5%
400 Hz inverters, input current	A	0.2 to 1.2	±5%
PSL dc bus current	A	5 to 30	+3%
Standard cell voltage	mV	200 to 800	±3%
Standard cell current	ma	0 to 300	±3%
Rad res cell current	ma	0 to 300	±3%
Battery temperature	^{o}F	20 to 100	$\pm 2^{o}$
Panel inboard temperature	^{o}F	-260^{o} to $+200^{o}$	$\pm 5^{o}$
Panel outboard temperature	^{o}F	-260^{o} to $+250^{o}$	$\pm 5^{o}$
Inverter temperature	^{o}F	0 to 150	$\pm 3^{o}$
Battery cell voltage	V	1 to 2	±2%

not reveal whether the failure was in the A/C enable relay, the 400 Hz 3ϕ inverter, or the gyro platform. A 400-Hz output voltage monitor seems desirable, but not mandatory.

The position of several power subsystem relays should be considered for telemetry of discretes. Several such measurements can be grouped into one channel. Examples are the main/standby switch for the 2.4-kHz inverter and the momentary boost converter relay. The latter is difficult to implement, because of the momentary mode of operation.

The telemetry of the boost regulator (B/R) and inverter chain of the existing Mariner system has some drawbacks. Only the main B/R has output current telemetry. There is no indication other than this indirect one) which B/R and inverter are ON. These comments would not be applicable on the proposed design that uses a parallel-operating, redundant, buck-boost regulator.

The RF Subsystem (RFS) load on the dc power bus is one of the biggest and most critical loads on the spacecraft. The assignment of its current monitor to Class 300 may yield measurement intervals of over 1 hr in Mode II. Transfer of this channel to Class 200 and use of the 300 Channel for the discretes mentioned above are suggested.

Output measurements of the main inverter and of the battery charger should be made more often, but no Type 100 channels are presently available.

It would be desirable to monitor battery cell voltage. Range is 1.2 to 2.0 V with ±2% accuracy desirable. Since it seems almost impossible to provide 18 new analog monitors, three such cells could be combined for one measurement. Cell voltage behavior is a very good indicator of the battery state-of-health. When charging the battery with limited constant current to a fixed voltage level, charging current telemetry becomes of less importance.

A discrete telemetry point and an on-off ground command is proposed to disconnect the highest-powered heaters from the power source in case of emergency. The two groups of heaters to be ground switchable are the dc group which consumes about 25 W and services IRS, platforms, and narrow TV; and the T/C-1 group, which consumes 50 W and services IRS, TV, UVS, and Bay 7 (Reference Tables 4-1 and 4-2). Heaters being simple resistive devices, current or voltage monitor does not seem warranted on these busses. In case of a short, the heater busses are protected by fuses.

A discrete telemetry point is proposed on the main/standby switch. In the proposed new configuration this switch would switch only the main inverter since the buck-boost regulator is part-redundant.

If available power or other telemetry requirements force a reduction of power subsystem telemetry channels, the following channels could be eliminated:

a. Battery Current. In spite of its importance, this parameter can be computed from the other current measurements. Only in the battery test load mode would no current reading be available. The elimination of current telemetry usually offers a greater saving in power and parts than elimination of voltage or temperature telemetry.

b. 400-Hz Input Current. This current monitor could be replaced with a voltage monitor on one or both 400-Hz inverters. These monitors could be on-off discretes rather than analog channels.

3.2.13 Weight and Volume Analysis

The weight density (lb/part) and volumetric density (in.^{3}/part) utilized in the following estimates are based on TRW's past experience with similar electronic hardware designs.

3.2.13-1 Buck-Boost Regulator

Weight estimate:	Magnetics	4.3 lb	4.3 lb
	Chassis	2.5 lb	2.5 lb
235 components at		0.01 lb/part	2.3 lb
		Total Weight:	9.1 lb

Volume = 0.8 in.^{3}/part = 210 in.^{3}

Total envelope = 5 x 7 x 6 in.

3.2.13-2 Power Source Logic

Total component count for this unit, including 14 magnetics and 24 diodes, is 134 parts.

Estimated size:	Height	4.5 in.	
	Width	7.0 in. 158 in.^{3} at 1.17 in.^{3} part	
	Length	5.0 in.	
Estimated weight:	7 current monitors (85 components)		1.5 lb
	24 power diodes		1.0 lb
	Remainder of unit including:		
	49 components		0.3
	Wire		0.5
	6 connectors		0.3
	Enclosure		1.8
	Kinetics switch (2 ea)		2.0
		Total Weight:	7.4 lb

3.2.13-3 Power Distribution and Heater Distribution

This unit contains the redundant switching and control circuitry for the following:

a. DAS, science, scan on-off

b. Approach guidance (A/G) on-off

c. Data storage subsystem (DSS) on-off

d. Attitude control (A/C) on-off

e. Dc heater on-off

Also, it contains the following:

f. Dc heater fuses and power distribution

g. Dc current monitor

The estimated weight and volume of 525 total parts, including fuses, is

Weight = 4.5 lb at 0.0086 lb./part

Volume = 0.45 $in.^3$/part = 236 $in.^3$

Envelope = 6 x 6 x 6.5 in.

3.2.13-4 Power Control Unit

The weight estimate is based upon the following functions in one black box:

a. Share mode detector

b. Momentary booster

c. Two current monitors

d. Battery charger

1. Redundant relay driver

2. Majority voting differential amplifiers

3. Charging resistors

Total number of parts: 650

Estimated weight: 4.6 lb at 0.007 lb/part

Estimated volume: 290 $in.^3$ 7 x 7 x 6 in.

3.2.13-5 Redundant 2.4 kHz Inverter

The unit is comprised of the following:

a. Main and standby 2.4 kHz inverter

b. Failure sensor

c. Current monitor

Magnetics:	1.8 lb
Chassis:	1.5
406 components:	3.5
at 0.0086 lb/part	6.8 lb
Volume:	250 $in.^3$ at 0.6 $in.^3$/part
Size:	6 x 6 x 7 in.

4. MISSION AND SPACECRAFT ANALYSES

4.1 INTRODUCTION

The initial effort involved the definition of the mission and spacecraft characteristics, the requirements imposed on the power system, and the establishment of design tradeoff criteria and guidelines to be applied toward the design and selection of the optimum power system.

Two missions have been identified for this study: Mars Flyby and Mars Orbiter. The orbiter will be based on 90 days in Mars orbit with no eclipse seasons. Specific launch dates have not been determined, but an early 1970 period is assumed. Launch dates and time will be considered in the comparative analysis as variables. Analyses performed in the course of TRW's Voyager studies show a range of Mars-Sun distance (AU) dependent on the launch date. Typical values for arrival are 1.388 to 1.612 AU and 1.47 to 1.66 AU for arrival plus 90 days in orbit. Transit times can vary from 110 to 230 days. The spacecraft configuration will be the Mariner '69 which is fully attitude-stabilized in three axes and uses the Sun and Canopus as referenced objects. The spacecraft carries scientific instruments to obtain data on the Martian environment, atmosphere, surface properties, and biological life. The spacecraft body is octagonal in shape with four fixed solar panels comprising a total area of 83 sq ft. Louvers on the equipment bay provide thermal control. The spacecraft engineering equipment and experiments will be very similar to the Mariner-Mars '69 except for valve and gimbal equipment for orbit insertion (orbiter mission).

4.1.1 Selection Criteria

The selection criteria applied to the various model power system configurations are discussed in the following paragraphs.

4.1.1.1 Solar Array Power Utilization

Utilization of the maximum available power is highly desirable as it results in spacecraft load growth capability, increased allowance for array degradation, or successful operation in flight with higher than normal loads. The constraint on the power system design is to satisfy all power requirements with an 83 sq ft array.

4.1.1.2 Reliability

Other than the minimum assessment goal of ≥ 0.90, the following aspects of reliability are applicable:

a. Ability of system to detect failures and provide corrective action

b. Failure modes and effects

c. Testability

d. Utilization of proven components and derating of components

e. Complexity

4.1.1.3 Weight

Weight is a parameter to be traded off with system reliability. The weight allocations are as follows:

Solar array (less structure)	50.0 lb
Battery (less chassis and cover) plus power processing equipment	71.7 lb
Total	121.7 lb

4.1.1.4 Demonstrated Design

Demonstrated design is highly desirable for it minimizes design risk and development time, and narrows the uncertainty in the performance calculations.

4.1.1.5 Interface Simplicity

Simplicity in the electrical, mechanical, and especially the thermal interface with the spacecraft configuration and power user equipment is desirable.

4.1.1.6 Flexibility

Effects of launch/arrival dates, solar array temperature predictions, and solar array degradation are to be minimized as well as dependence on predicting battery charge/discharge voltage within narrow tolerances. The capability of the system to operate over wide limits of load, source voltages, environment, and abnormal mode operation is to be provided.

4.1.1.7 Unregulated Bus Voltage

Minimization of the present 2:1 swing in unregulated bus voltage will provide advantages as follows:

a. Allow for ease in design (greater reliability) for users of unregulated bus voltage (TWT's, heaters, low-level circuitry).

b. Allow for increase in power utilization via reduction of TWT power (TWT converter efficiency decreases for wider input voltage range) and reduce the variability in power consumption of unregulated bus power users.

4.1.1.8 Transient Response

The ability of the power system to provide a low source impedance continuously will minimize load switching transients. Many loads (TWT, heaters, experiments, etc.) are switched on/off during the mission.

4.1.2 Design Guidelines

Several selected design guidelines to be applied to the model power system configurations are delineated below:

a. Backup redundancy techniques shall be employed to the extent that those events, functions, or sequences critical to the mission success may be initiated by two separate and independent means.

b. To assure increased reliability, the battery shall be required only for normal mission modes in which the array is not sun-oriented (e.g. launch, maneuvers, orbit insertion).

c. The solar array zener diode voltage limiter shall be eliminated.

d. Isolation of command inputs and fail-safe control circuitry shall be provided.

e. The two stable operating points which are characteristic of a solar array with pulsewidth modulated power conditioning equipment shall be eliminated.

f. The electrical interface with the user equipment (e.g. 25-50 Vdc unregulated dc, 27.2 ±5% Vrms, 1-ϕ, 400-Hz power) is to be considered firm; however, internal power system characteristics are flexible.

4.2 SPACECRAFT POWER REQUIREMENTS

Tables 4-1 and 4-2 show the load/power requirements for each subsystem and equipment categories as a function of major mission phases for the flyby and orbiter missions, respectively. These tables were based on JPL-furnished load information. Analysis of the load requirements for the flyby mission shows that the majority of the spacecraft engineering subsystems and all the experiments require regulated ac power from the 2.4 kHz inverter. A large portion of ac power (50 W) goes toward TCFM power and cruise heaters. Opportunities for reduction of required source power may be realized by regulated bus voltage systems supplying heater power directly, eliminating the losses in the conditioners (i.e., boost regulator and 2.4 kHz inverter). Requirements for 1ϕ and 3ϕ power are relatively low and are required only during certain mission phases. The primary user of unregulated dc power is the TWT power amplifier. It requires a dc/dc converter for conversion to high voltages required by the TWT. Other users of unregulated power include heaters and battery charging. The power requirements for the orbiter mission are similar to the flyby except for the gimbal and valve equipment that is required for Mars orbit insertion.

4.3 LOAD PROFILE ANALYSIS

Analyses were performed to compare the solar array load power capability and the total conditioned load power requirement as functions of mission time to define the critical design point (CDP). The CDP is defined as the condition of minimum power margin between load power and solar array capability. The CDP can be ascertained, knowing the solar array characteristics, by examination of the load requirements tabulated in Tables 4-1 and 4-2. For the flyby mission, the CDP occurs at near encounter with high level TWT's operating. The CDP for the orbiter mission occurs during the TV sequence near the end of mission life where the solar array power capability is minimum. For both CDP's, it is assumed that available battery power will not be credited toward sharing the load requirements with the solar array.

Item	Subsystem	Acronym	Equipment	Unreg DC	2.4 KHz	3φ 400 Hz	1φ 400 Hz	Other	1 Launch	2 Star Acq.	3 Cruise Batt Chg
1	Science	DAS	Data Automation Subsystem		▲						
2	↓	TV	Television		▲						
3		IRR	Infrared Radiometer		▲						
4		IRS	Infrared Spectrometer		▲						
5		UVS	Ultraviolet Spectrometer		▲						
6		IRSM	Infrared Spectrometer Motor				▲				
7	Attitude Control	A/C-1	Attitude Control		▲				13	25	4
8	↓	A/C-2	Autopilot Control		▲						
9		GYRO 1	Gyro Electronics		▲				8	8	
10		GYRO 2	Gyro			▲			9	9	
11	Scan Control	SCAN-1	Scan Control Electronics		▲				5.3	5.3	5.3
12	↓	SCAN-2	Scan Control Motor				▲				
13	N/A										
14	N/A										
15	Radio Frequency	RFS	Radio Frequency Subsystem (except TWT)		▲				32.2	32.2	32.2
16	↓	TWT	TWT (Power Amplifier)	▲					60	60	60
17	Central Computer and Sequencer	CC & S	Central Command and Sequencer		▲				32.4	17.0	17.0
18	Flight Telemetry	FTS	Flight Telemetry Subsystem		▲				15.0	15.0	15.0
19	Flight Command	FCS	Flight Command Subsystem		▲				3.2	3.2	3.2
20	Data Storage	DSS	Data Storage Subsystem		▲				21.0	21.0	17.7
21	Pyrotechnic	PYRO	Pyrotechnic		▲					1.0	1.0
22	Thermal Control	T/C-1	TCFM Power and Cruise AC Heater		▲				54.0	54.0	54.0
23	↓	T/C-2	DC Heater	▲					26.0	26.0	26.0
24	N/A										
25	Power	PWR	Power Distribution		▲				2.25	2.25	2.25
26	↓	BTCG	Battery Charger/ Booster	▲					0.5	0.5	25.0

Abnormal Gyro-On Loads

GYRS 1	8.0	2.4 KHz	For All Phases Except 1, 2, 5
GYRS 2	9.0	3φ, 400 Hz	
ACS 1	16.0	2.4 KHz	
TCS 2	9.8	Unreg DC	

Summary of Power Requirements

Unreg DC	86.50	86.50	111.00
2.4 KHz	186.35	183.95	151.65
3φ 400 Hz	9.00	9.00	0
1φ 400 Hz	0	0	0

FOLDOUT FRAME 1

Table 4-1. Power Requirements (W) as a Function of Mission Phase — Flyby Mission

MISSION PHASE									
4 Cruise	5 Maneuver	6 Enc Appr	7 Far Enc	8 Far Enc Hi Pwr TWT	9 Far Enc Low Pwr TWT	10 Near Enc	11 Near Enc Hi Pwr TWT	12 Near Enc Low Pwr TWT	13 Playback
			20	20	20	20	20	20	
			32	32	32	32	32	32	
			3	3	3	3	3	3	
			4	4	4	4	4	4	
			12	12	12	12	12	12	
							2	2	
4	23	4	4	4	4	4	4	4	4
	29								
	8								
	9								
5.3	5.3	5.3	26.5	28.5	28.5	26.5	16.5	16.5	5.3
			12	12	12	12	12	12	
32.2	32.2	32.2	32.2	32.2	32.2	32.2	32.2	32.2	32.2
60	60	60	60	99.0	60	60	99.0	60	99.0
17.0	17.0	17.0	17.0	17.0	17.0	17.0	17.0	17.0	17.0
15.0	15.0	15.0	15.0	15.0	15.0	15.0	15.0	15.0	15.0
3.2	3.2	3.2	3.2	3.2	3.2	3.2	3.2	3.2	3.2
17.7	17.7	17.7	18.0	18.0	18.0	23.0	23.0	23.0	21.0
1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
54.0	54.0	54.0							54.0
26.0	26.0	26.0	26.0	26.0	26.0	26.0	26.0		
2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25
0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5
86.50	86.50	86.50	86.50	125.50	86.50	86.50	125.50	86.50	125.50
151.65	207.65	151.65	190.15	192.15	192.15	195.15	185.15	185.15	154.95
0	9.00	0	0	0	0	0	0	0	0
0	0	0	12.0	12.0	12.0	12.0	14.0	14.0	0

Item	Subsystem	Acronym	Equipment	Unreg DC	2.4 KHz	3φ 400 Hz	1φ 400 Hz	+28 VDC	1 Launch	2 Star Acq	3 Cruise I Batt Chg
1	Science	DAS	Data Automation Subsystem		▲						
2	↓	TVS	Televisions		▲						
3		IRR	Infrared Radiometer		▲						
4		IRS	Infrared Spectrometer		▲						
5		UVS	Ultraviolet Spectrometer		▲						
6	Science	IRSM	Infrared Spectrometer Motor				▲				
7	Attitude Control	A/C 1	Attitude Control		▲				13	25.0	4.0
8	↓	A/C 2	Attitude Control		▲						
9		GYRE	Gyro Electronics		▲				8.0	8.0	
10	Attitude Control	GYRO	Gyro			▲			9.0	9.0	
11	Scan Control	SCNE	Scan Control Electronics		▲				5.3	5.3	5.3
12	Scan Control	SCNM	Scan Control Motor				▲				
13	Propulsion	VALV	Valve					▲			
14	Propulsion	GIMB	Gimbal					▲			
15	Radio Frequency	RFS	Radio Frequency Subsystem (exc. TWT)		▲				32.2	32.2	32.2
16	Radio Frequency	TWT	TWT (Power Amplifier)	▲					55.0	55.0	55.0
17	Central Comp and Sequencer	CC & S	Central Command and Sequencer		▲				39.0	19.0	19.0
18	Flight TLM	FTS	Flight Telemetry Subsystem		▲				15.0	15.0	15.0
19	Flight Command	FCS	Flight Command Subsystem		▲				3.2	3.2	3.2
20	Data Storage	DSS	Data Storage Subsystem		▲				21.0	22.0	10.0
21	Pyrotechnic	PYRO	Pyrotechnic		▲					1.0	1.0
22	Thermal Control	T/C 1	TCFM Power and Cruise ACHtr		▲				50.0	50.0	50.0
23	↓	T/C 2	DC Heater	▲					15.0	15.0	15.0
24	Thermal Control	T/C 3	DC Heater	▲					10.0	10.0	10.0
25	Power	BTCG	Battery Charge/ Booster	▲					0.5	0.5	25.0
26	↓	BRFS	Battery Regulator Fail Sensor	▲					1.5	1.5	1.5
27	Power	PWRD	Power Distribution		▲				2.25	2.25	2.25

Abnormal Gyro-On Loads

ACS1	16.0	2.4 KHz
GYSE	8.0	2.4 KHz
GYSO	9.0	3φ 400 Hz

Summary of Power Requirements

Unregulated DC	82.00	82.00	106.50
2.4 KHz	188.95	182.95	141.95
3φ 400 Hz	9.00	9.00	0.00
1φ 400 Hz	0.00	0.00	0.00
+28 VDC	0.00	0.00	0.00

FOLDOUT FRAME 1

Table 4-2. Power Requirements (W) as a Function of Mission Phase — Orbiter Mission

MISSION PHASE										
4 Cruise Chg Off	5 Maneuver	6 Far Enc	7 Orbit Insertion	8 Far Enc Playback	9 Orbit Trim	10 Orbit Cruise	11 TV Sequence	12 Earth Occultation	13 Playback ATR	14 Playback DTR
		20.0					20.0			
		32.0					32.0			
		3.0					3.0			
		4.0					4.0			
		12.0					12.0			
							3.5			
4.0	23.0	4.0	23.0	4.0	23.0	4.0	4.0	4.0	4.0	4.0
	10.5		10.5		10.5					
	8.0		8.0		8.0					
	9.0		9.0		9.0					
5.3	5.3	28.5	5.3	5.3	5.3	5.3	16.5	5.3	5.3	5.3
		12.0					12.0			
	30.0		30.0		30.0					
	35.0		35.0		35.0					
32.2	32.2	32.2	32.2	32.2	32.2	32.2	32.2	32.2	32.2	32.2
55.0	55.0	89.0	89.0	89.0	55.0	55.0	89.0	55.0	89.0	55.0
19.0	19.0	19.0	19.0	19.0	19.0	19.0	19.0	19.0	19.0	19.0
15.0	15.0	15.0	15.0	15.0	15.0	15.0	15.0	15.0	15.0	15.0
3.2	3.2	3.2	3.2	3.2	3.2	3.2	3.2	3.2	3.2	3.2
10.0	10.0	18.0	10.0	19.0	10.0	10.0	23.0	15.0	19.0	18.0
1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
50.0	50.0		50.0	50.0	50.0	50.0		50.0	50.0	50.0
15.0	15.0	15.0	15.0	15.0	15.0	15.0	15.0	15.0	15.0	15.0
10.0	10.0	10.0	10.0	10.0	10.0	10.0	10.0	10.0	10.0	10.0
0.5	0.5	0.5	0.5	25.0	0.5	25.0	0.5	0.5	0.5	0.5
1.50	1.5	1.50	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5
2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25
82.00	82.00	116.00	116.00	140.50	82.00	106.50	116.00	82.00	116.00	82.00
41.95	179.45	194.15	179.45	150.95	179.45	141.95	187.15	146.95	150.95	149.95
0.00	9.00	0.00	9.00	0.00	9.00	0.00	0.00	0.00	0.00	0.00
0.00	0.00	12.00	0.00	0.00	0.00	0.00	15.50	0.00	0.00	0.00
0.00	65.00	0.00	65.00	0.00	65.00	0.00	0.00	0.00	0.00	0.00

FOLDOUT FRAME 2

5. SELECTION OF MODEL SYSTEM CONFIGURATIONS

5.1 SELECTION CRITERIA

The selection of the model systems involved screening the various power system configuration possibilities to eliminate the less desirable ones. The selection process progressed from the examination of 78 baseline power system configurations to the selected number of five. Table 5-1 is a matrix of power system configurations and Table 5-2 shows the justification for deletions of known system configurations. The synthesis of the configurations and the rationale are detailed in Final Report No. 07171-6001-R000, "Power System Configuration Study and Reliability Analysis" dated 18 September 1967. This work was performed by TRW for the Jet Propulsion Laboratory under Contract No. 951574.

The criteria for initial selection primarily included power utilization, weight, and reliability assessments (computer aided), complexity, flexibility, and demonstrated design. Table 5-3 summarizes the rationale in eliminating certain power system configurations. Figure 5-1 depicts the selected model power system configurations in simplified form. Figure 5-2 shows the existing Mariner '69 power system configuration. All relays are shown in the set position; also, telemetry current monitors are shown. Table 5-4 designates the cross-reference for the commands and some of the abbreviations utilized in the block diagrams.

5.2 WEIGHT-RELIABILITY OPTIMIZATION

A computer program (modification of a program developed by TRW for JPL on Contract No. 951574) has been developed to provide an efficient instrument for quick evaluation of various power system configurations and the multitude of possible combinations of redundant elements for a given configuration. A brief description of the program and some typical printouts are delineated below.

A space power system consists of the following major components combined with a suitable solar array:

a. Power conditioning units

b. Line regulator

c. Array control

d. Energy storage

These units can be implemented in several distinct basic designs (types). Furthermore, each type could have several redundancy scheme alternates to improve reliability. The problem, then, is to evaluate each system design (case) to determine the optimum reliability alternates for each unit to achieve the highest reliability for prescribed subsystem weight constraints.

The TRW 940 Fortran 2 program is adaptable to this approach and operates in the following manner. The parameter information for each alternate of each type of each basic component is stored in a master data file. The program accesses this master file and reads a case specification from the input file. The alternate information for each type specified for each component is extracted from the master data file and the combinatorial search for that case is begun. Each possible combination of the alternatives is generated and the resulting subsystem weight and reliability are calculated by a subroutine. The weight and reliability of the system for this combination are stored along with alternate indicators. When all combinations have been evaluated, they are sorted by weight. An option in the program permits the output to be all the combinations or alternatively suppresses the output

Table 5-1. Summary of Selected Baseline Power System Configurations

Note

- Each configuration (combination of battery control, line regulator and array control) may be used with either AC or DC distribution.
- Applicable array controls indicated by uncircled numbers in each cell.
- Circled numbers in each cell designate reason for deleting certain configurations as listed in Table 5-2.

BATTERY CONTROLS			LINE REGULATION				
			1	2	3	4	5
			PWM Buck Line Reg	Diss Line Reg	Boost Line Reg	Bk-Boost Line Reg	No Reg
	1	Switch + Resistor	3 ⑦ ⑨	NA ③	3, 4, 5 ⑦ ⑫	3 ⑦ ⑨	NA ②
	2	Same + Dischg Booster	3 ⑦ ⑨	NA ③	3, 4 ⑦ ⑪ ⑫	3 ⑦ ⑨	NA ②
	3	Dissipative Chg'r & Dischg. Sw.	1, 2, 3 ⑨	NA ③	2, 3, 4 ⑥ ⑩ ⑫	1, 2, 3 ⑨	NA ②
	4	Same + Dischg. Booster	1, 2, 3 ⑨	NA ③	2, 3, 4 ⑥ ⑪ ⑫	1, 2, 3 ⑨	NA ②
	5	PWM Buck Chg'r & Dischg. Sw.	1, 2, 3 ⑨	NA ③	2, 3, 4 ⑥ ⑩ ⑫	1, 2, 3 ⑨	NA ②
	6	Same + Dischg. Booster	1, 2, 3 ⑨	NA ③	2, 3, 4 ⑥ ⑪ ⑫	1, 2, 3 ⑨	NA ②
	7	PWM Boost Chg'r & Disch. Sw.	1, 2, 3 ⑨	2, 3 ⑤ ⑨	2, 3, 4, 5 ⑥ ⑫	1, 2, 3 ⑨	NA ②
	8	Same + Dischg. Booster	1, 2, 3 ⑨	NA ④	2, 3, 4 ⑥ ⑪ ⑫	1, 2, 3 ⑨	NA ②
	9	Diss. Chg. & Boost Dischg. Regulators	NA ①	NA ①	NA ①	NA ①	3, 4, 5, 6 ⑧
	10	PWM Buck Chg. & Boost Dischg. Regulators	NA ①	NA ①	NA ①	NA ①	3, 4, 5, 6 ⑧
	11	Same with Low Voltage Battery	NA ①	NA ①	NA ①	NA ①	3, 4, 5, 6 ⑧

ARRAY CONTROL LEGEND

1. None
2. Zener
3. Active Shunt
4. PWM Buck Series
5. PWM Buck Series + P_{max} Track
6. PWM Series Buck-Boost

Table 5-2. Justifications for Deletions of Power System Configurations

Circled Number (Table 5-1)	Reason for Deletion
1	**Not applicable. Array and battery controls provide regulated bus.** Additional line regulation is not required.
2	**Not applicable. Required bus voltage regulation cannot be provided by these battery controls.**
3	**Not applicable. Power loss in line regulator with maximum voltage at unregulated bus considered excessive.**
4	**Not applicable. Series dissipative regulator tends to produce constant current load and eliminate possibility of undesirable load sharing.**
5	**Array control 1 deleted. Unregulated bus voltage must be limited to minimize voltage drop across dissipative line regulator.**
6	Array control 1 deleted. Unregulated bus voltage must be limited to prevent overvoltage at regulated bus.
7	**Array controls 1 and 2 deleted. Active regulator required by battery charge control to provide accurate voltage limit.**
8	Array controls 1 and 2 deleted. They will not provide required ±1/2% bus voltage regulation.
9	Array controls 4, 5, and 6 deleted. It is illogical to use two series bucking regulators in series.
10	Array control 5 deleted. It is illogical to use line regulator if solar array output well regulated. With bucking charge control, array voltage must always exceed battery voltage. Boosting required only during battery discharge and should be included in battery controls.
11	Array control 5 deleted. It is illogical to use discharge booster with maximum power tracking solar array control. Both prevent undesirable load sharing between array and battery.
12	Array control 6 deleted. It is illogical to use two boost regulators in series.

Table 5-3. Reasons for Eliminating Power System Configurations

Systems	Reasons
1. All system configurations with energy storage 1, 3, 5, and 7	1. These systems do not have the capability to prevent undesirable load sharing between the solar array and battery near the end of the mission. Solar array power availability constraints prohibit such a power system design.
2. All systems with a dissipative line regulator	2. The low efficiency of the dissipative regulator near the critical design point makes it undesirable.
3. All systems with a PWM buck line regulator	3. The boost line regulator offers weight advantages since it is not to handle the full power. It also offers efficiency advantages at the critical design point. The PWM buck line regulator requires a higher voltage battery than a boost for the same regulated voltage.
4. All systems with switch and resistor battery controls	4. The dissipative charger systems offer more flexibility and control in terms of current limiting and charge voltage control. The switch and resistor approach is very highly dependent on charging source voltage and is thus not flexible.
5. All systems with PWM buck charger	5. The systems do not require highly efficient battery charging; therefore, the more simple and reliable dissipative charger is desirable.
6. All systems with PWM buck charger and battery boost discharge regulator	6. Same reason as in 5.
7. All systems with PWM boost charger	7. Selected configurations do not require a PWM boost charger. Reasons delineated in 5 also apply.

Table 5-3. Reasons for Eliminating Power System Configurations (Cont)

Systems	Reasons
8. All systems with low voltage battery (battery controls 11)	8. For a nonredundant battery system, the low voltage battery system is not competitive from a weight standpoint (higher conversion losses with resulting increase in power conversion and battery weight). Low voltage systems are primarily applicable to long-life, high-reliability requirements or where partial success is acceptable with loss of a portion of the battery power.
9. PWM buck array control with line regulator	9. It is generally not desirable to have two series power-handling elements for reasons of lower reliability and increased losses.
10. PWM buck series $+P_{max}$ tracker	10. Maximum power trackers are generally applicable to low orbits where advantage can be taken of the transient (temperature) characteristics of the solar array. The boost regulator is more desirable since its efficiency is higher at the critical design point and is a simpler design.
11. Buck-boost array control	11. The active shunt limiter offers higher reliability and increased solar array power utilization.
12. Zener limiter	12. The active shunt limiter offers higher reliability and flexibility in adjusting the limiting voltage and provides narrow limiting voltage regulation.

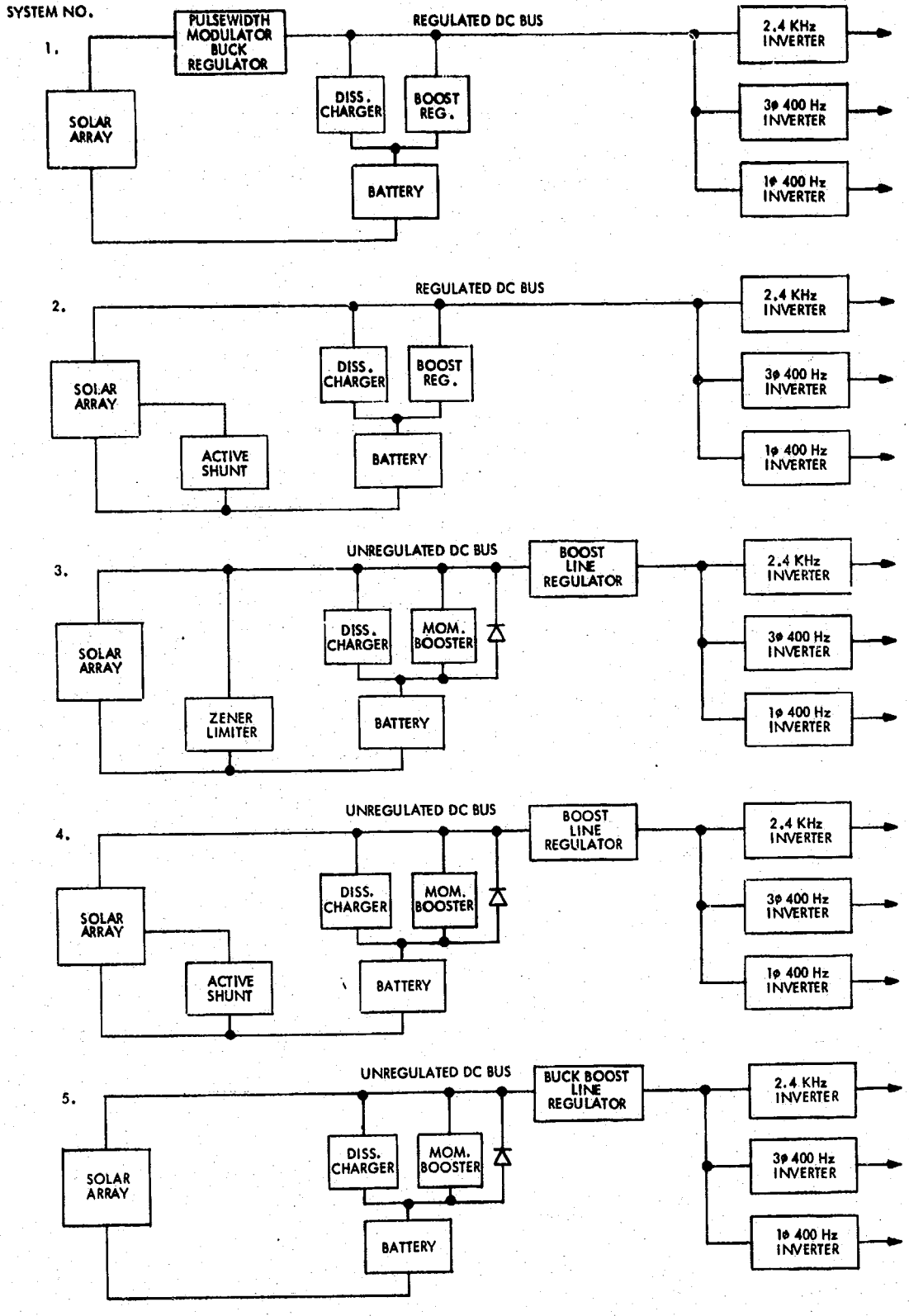


Figure 5-1. Selected Power System Configurations, Simplified Block Diagram

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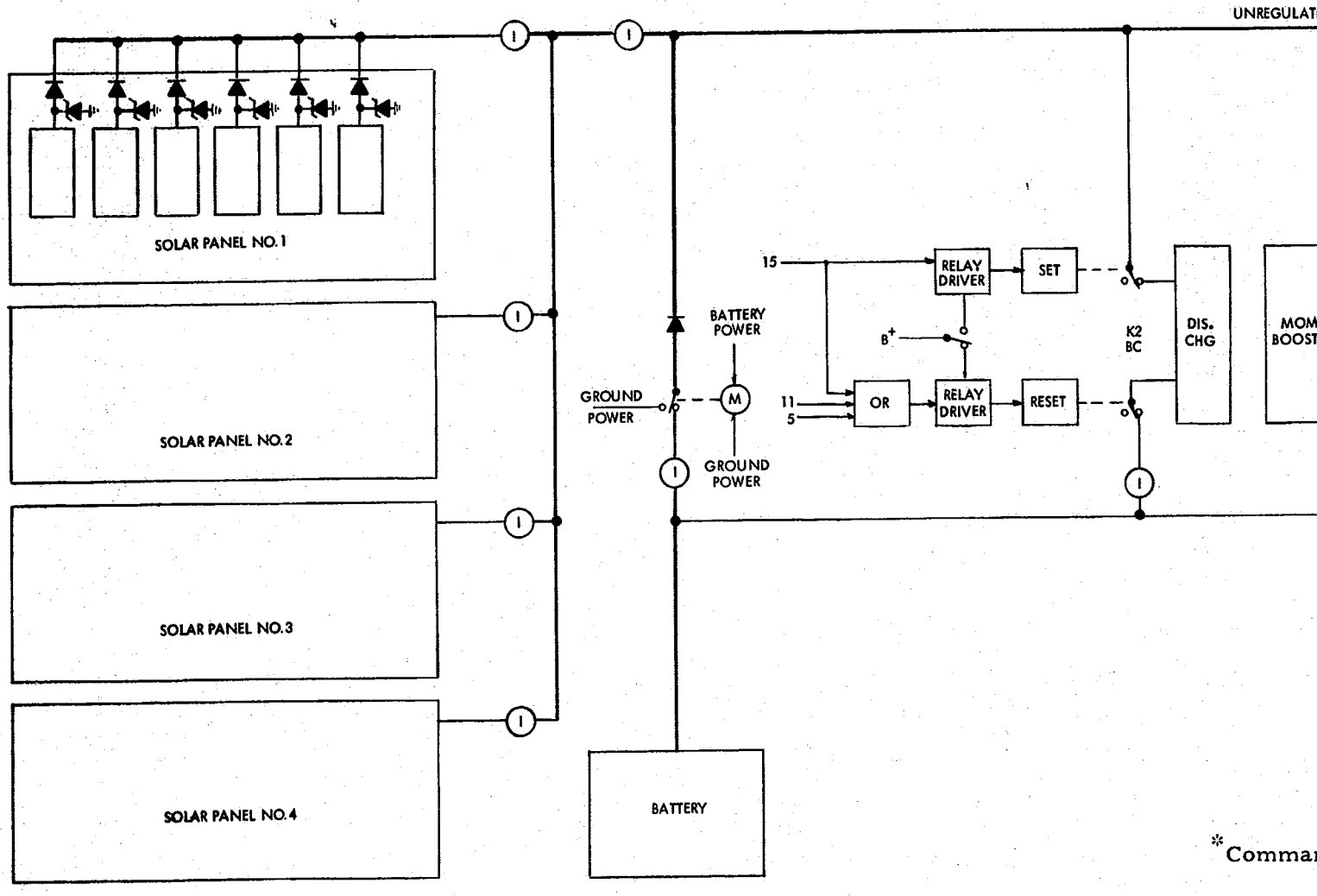

*Comma

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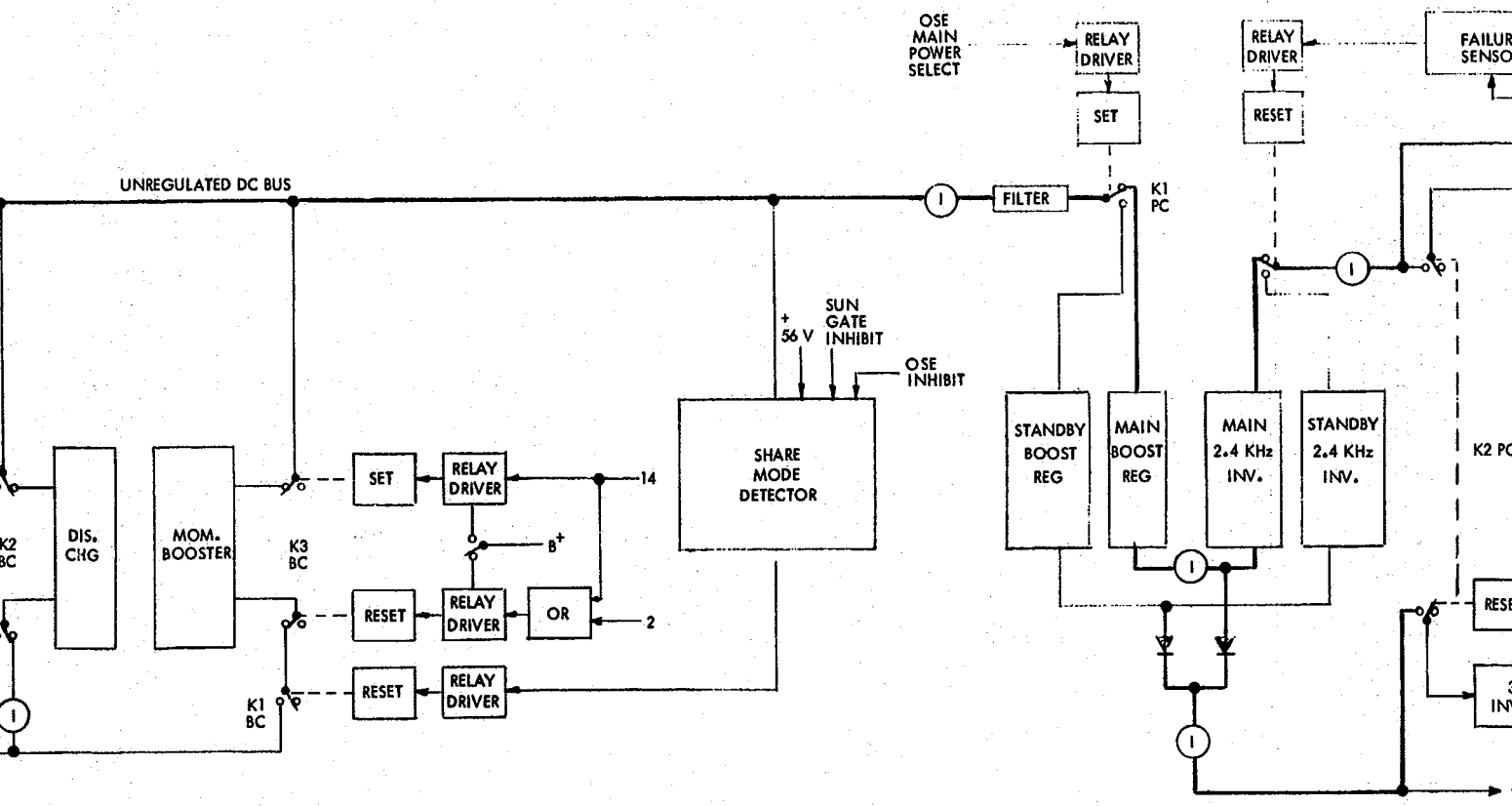
FOLDOUT FRAME 2



*Command designations; refer to Table 5-4.

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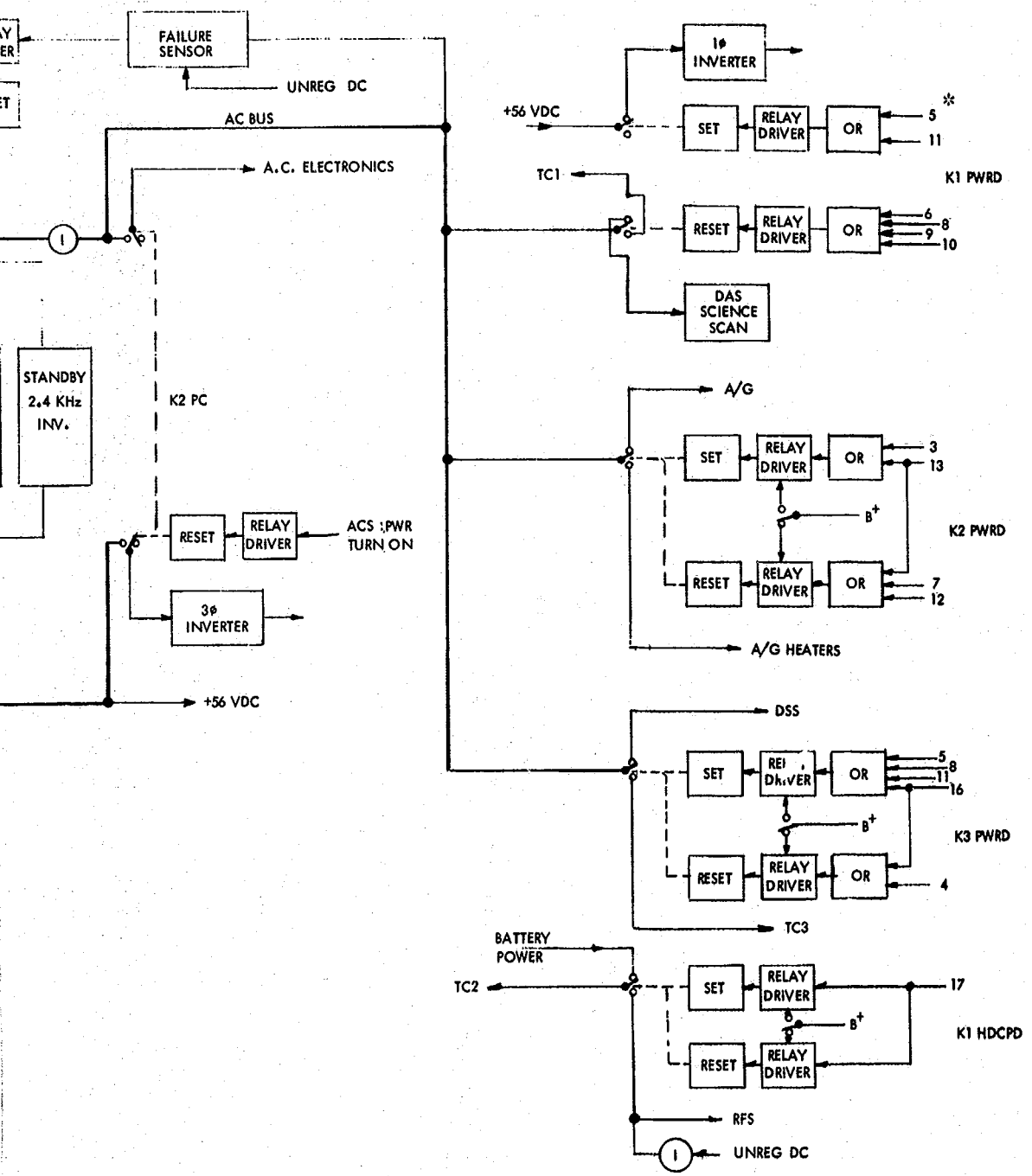

Figure 5-2. Unregulated DC Bus with Zener Limiter and Boost Line Regulator

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Table 5-4. Command Designation

Command	Name	Source*	Type of Signal	Method of Actuation					
				(1) Relay	Set or Reset	Relay Location†			
						Pwr Dist.	BC	PC	HDCPD
1	Gyros On	A/C	+28 V Referred to A/C Ground	K2*	R			▲	
2	Sun Gate Enable/Disable	A/C G1	Isolated Circuit Closure	K3	R		▲		
3	Approach Guidance (A/G) On	CC and S C4		K2	S	▲			
4	Data Storage Subsystem (DSS) Off	CC and S L3		K3	R	▲			
5	Encounter (ENC) Phase	CC and S N1		K1	S	▲			
				K3	S	▲			
				K2	R		▲		
6	Near-Enc., Terminate	CC and S N5		K1	R	▲			
7	Near-Enc. Sequence Enable	CC and S N6		K2	R	▲			
8	Start Playback	CC and S P1		K1	R	▲			
				K3	S	▲			
9	Cruise Mode	DC-1	Isolated Circuit Closure (IS, IP, or Relay)	K1	R	▲			
10	Playback Mode	DC-3	Isolated Circuit Closure	K1	R	▲			
11	Enc. Phase	DC-25		K1	S	▲			
				K2	R		▲		
				K3	S	▲			
12	Near-Enc Sequence Enable	DC-26		K2	R	▲			
13	A/G On/Off	DC-34		K2	S	▲			
				K2	R	▲			
14	Boost Mode Enable/Disable	DC-37		K3	S		▲		
				K3	R		▲		
15	Battery Charger On/Off	DC-38		K2	S		▲		
				K2	R		▲		
16	DSS On/Off	DC-47		K3	S	▲			
				K3	R	▲			
17	Battery/DC Bus DC Heater Toggle	DC-50		K1	S				▲
				K1	R				▲

(1) Relays magnetic latching except for K2 in PC

* Nonlatching

† Nomenclature — Description

PWR DIST	Power Distribution Unit
BC	Battery Charger
PC	Power Control
HDCPD	Heater and DC Power Distribution (4A19)

of dominated combinations. (A combination is dominated if a combination exists that has lower weight and an equal or greater reliability.) After the program finishes one case and the output is received, the program reads the input file for another case and repeats the above until all case specifications have been processed.

A subroutine computes the subsystem weight after a complete subsystem has been specified by the main program. Essentially, unit weights and efficiencies are given functions of the unit power. The computation proceeds backwards, from power conditioning equipment to solar array, and sizes each unit according to its power requirement as determined by previous unit power requirements; others on average power requirements and inputs are provided accordingly.

The subsystem reliability is taken as the product of the unit reliabilities (any unit failure causes subsystem failure). The unit reliabilities as input are assumed independent of the unit power in that the unit is sized according to its power requirement and hence piece-part stress ratios are roughly invariant.

A typical example of the computer printout for one of the selected configurations is shown in Table 5-5. The system (flyby mission) consists of a shunt limiter array control (AC3), a boost line regulator (LR3), a dissipative charger and momentary booster and battery (ES2), and power conditioning units. The first column is the total weight of the power system including the solar array structure for 1.45 AU arrival. The second column is the system reliability. The third column (PSA) is the required solar array power at the critical design point. The fourth column (PBAT) is the required battery power during mid-course maneuver. The fifth column (WGT2) is the total system weight including solar panel substrate for 1.62 AU arrival. The sixth column (WGT3) is the total system weight less solar panel structure at 1.45 AU arrival. The last column (CONFIG.) designates the redundancy for each major element. The first digit in the last column corresponds to the 2.4-kHz inverter. A zero or one indicates redundant or nonredundant inverter. Proceeding to the right, the digits indicate the 3ϕ inverter, 1ϕ inverter, array control, line regulator, and the last two digits, the energy storage. The energy storage for this example has four combinations of redundant/nonredundant battery or charging control. For this particular case, 128 combinations were possible; however, the computer selectively prints out the nondominated combinations (20). A combination is dominated if a combination exists that has lower weight and an equal or greater reliability.

Table 5-5. Typical Computer Printout for One Selected Power System for the Flyby Mission

MMPSØS "PØWER SUBSYSTEM ØPTIMIZATIØN STUDY" (DATA AS ØF 29MAY68)

AC LR ES
3 3 2

WEIGHT	REL	PSA	PBAT	WGT2	WGT3	CØNFIG.
137.37	.8922182	370.15	339.46	149.95	97.20	000 0 0 00
138.37	.9137268	370.15	339.46	150.96	98.21	000 0 0 01
142.28	.9297178	374.04	343.51	154.99	101.69	000 0 1 01
146.32	.9379195	374.04	343.77	159.04	105.74	010 0 1 01
150.41	.9461935	374.39	343.77	163.14	109.79	011 0 1 01
151.56	.9461935	379.29	349.34	164.46	110.41	110 0 1 01
155.65	.9545406	379.64	349.34	168.56	114.46	111 0 1 01
162.41	.9604525	385.51	349.34	175.52	120.58	111 1 1 01
173.06	.9640567	374.04	343.51	185.77	132.47	000 0 1 10
174.99	.9661254	374.04	343.51	187.70	134.40	000 0 1 11
177.12	.9725613	374.04	343.77	189.84	136.54	010 0 1 10

179.05	.9746483	374.04	343.77	191.77	138.47	010 0 1 11
179.08	.9746483	374.39	343.51	191.81	138.46	001 0 1 11
181.21	.9811409	374.39	343.77	193.94	140.59	011 0 1 10
183.14	.9832463	374.39	343.77	195.87	142.52	011 0 1 11
184.77	.9832463	379.29	349.34	197.67	143.62	110 0 1 11
186.93	.9897963	379.64	349.34	199.84	145.74	111 0 1 10
188.86	.9919202	379.64	349.34	201.77	147.67	111 0 1 11
193.65	.9959266	385.51	349.34	206.76	151.82	111 1 1 10
195.62	.9980637	385.51	349.34	208.73	153.79	111 1 1 11

6. ANALYSIS OF MODEL SYSTEM EQUIPMENT

6.1 SOLAR ARRAY CHARACTERISTICS

The electrical output of the solar array, based on the existing Mariner solar panel total area of 83 sq ft with 78 cells in series and 224 cells in parallel, has been determined.

The pertinent characteristics of the components are shown in Table 6-1.

6.1.1 Electrical Output Characteristics

The electrical output, shown in Table 6-2, was calculated for the string-pair (consists of a pair of 78 series by 3 parallel cells) based upon orbital conditions given in Table 6-3, component characteristics shown in Table 6-1, nominal time-independent power adjustment factors (50% probability) shown in Table 6-4, temperatures given in Table 6-5, and nominal time-dependent loss factors described in Paragraph 6.1.1.2. Results of these calculations, including scaling to 224 parallel cells, are shown in Figure 6-1 for 1.0 AU and 1.45 AU distances (array life 150 days). Preliminary correlations between the calculated values and JPL-furnished test data on a preproduction solar panel are very good, e.g., within 2% at maximum power value (for same set of conditions).

6.1.1.1 Temperature

The temperatures corresponding to the various distances from the sun are shown in Table 6-5 for an uninsulated array. These values are based on studies performed by TRW on the Voyager program.

6.1.1.2 Time-Dependent Loss Factors

Radiation. The nominal (50% confidence) yearly dosage based upon "Voyager Environmental Standards," dated 1967 September 25 from NASA, Voyager Project Office, is 5×10^8 30 MeV protons/cm^2. This amounts to 3×10^{13} 1 MeV equivalent electrons at the cell for 20 mils cover-glass thickness. The nominal degradation factors (50% confidence) based on the above data are shown in Table 6-6.

6.1.1.3 Wiring and Diode Voltage Drop

Wiring	0.38 V
Diode	0.87 V

6.1.1.4 Weight

The weight analyses for a module and the string pair are shown in Tables 6-7 and 6-8, respectively.

Based on the foregoing analysis, the total weight of the panel (less structure) for 224 strings is estimated to be

$$\frac{224}{6} (1189.55 \times 10^{-3}) \text{ lb}$$

or 44.4 lb.

Table 6-1. Component Characteristics

Solar Cells	
Type	N-on-P silicon soldered covered
Size	2 cm x 2 cm x 0.016 in.
Weight	550 mg
Electrical characteristics at AMO, 28°C	I_p = 0.125A
	V_p = 0.480V
	I_{sc} = 0.134A
	V_{oc} = 0.598V
Resistivity	1 ohm-cm
Series resistance	0.4 ohm
Current temperature coefficient	74 x 10^{-6} A/°C
Voltage temperature coefficient	2.2 x 10^{-3} V/°C
Efficiency	11.2 percent average
Cover Slides	
Type	Fused silica
Size	2 cm x 2 cm x 0.020 in.
Cutoff wavelength	0.410 μ
Blocking Diode	
Type	Silicon, glass
Peak inverse voltage	100 V
Reverse leakage current	3μA at PIV, 25°C
	50μA at PIV, 100°C
Forward voltage drop	0.87 V at 1A, 25°C
Current	2A

Table 6-2. Electrical Characteristics of Solar Cell String-Pair for Various Orbital Conditions and Times Based on Nominal Time-Dependent and Time-Independent Factors (50-Percent Confidence)

Time (Days)	AU	Temperature (°C)	Electrical Characteristics			
			I_p (Amps)	V_p (Volts)	I_{sc} (Amps)	V_{oc} (Volts)
0	1.00	+28°C	0.683	36.5	0.737	45.1
0	1.00	+54	0.695	32.1	0.749	40.7
0	1.388	+ 4	0.319	42.5	0.373	51.1
150	1.388	+ 4	0.302	42.5	0.353	51.1
0	1.612	-16	0.210	46.4	0.264	55.0
150	1.612	-16	0.199	46.4	0.250	55.0
0	1.586	-14	0.220	46.0	0.274	54.6
240	1.586	-14	0.200	46.0	0.249	54.6
0	1.67	-21	0.188	47.4	0.242	56.0
240	1.67	-21	0.171	47.4	0.220	56.0

Table 6-3. Sun-Spacecraft-Distance and Array-Operating Life

Distance from Sun (AU)	Array Life (Days)
1.00	0
1.388	150
1.612	150
1.586	240
1.67	240

Table 6-4 Time Independent Power Adjustment Factors

I_{sc}	
Cover installation losses (a)	*0.955
Module assembly losses (b)	*0.960
Cell efficiency (c)	1.00
Uncertainty in solar constant (d)	1.00
Random solar intensity (e)	1.00
Product (abcde)	0.9168
V_{oc}	
Measurement error	0

*Based on TRW's experience

Table 6-5. Temperatures Based on Distance from the Sun

Distance from Sun (AU)	Solar Array Temperature (°C)
1.00	+54
1.388	+ 4
1.612	-16
1.586	-14
1.67	-21

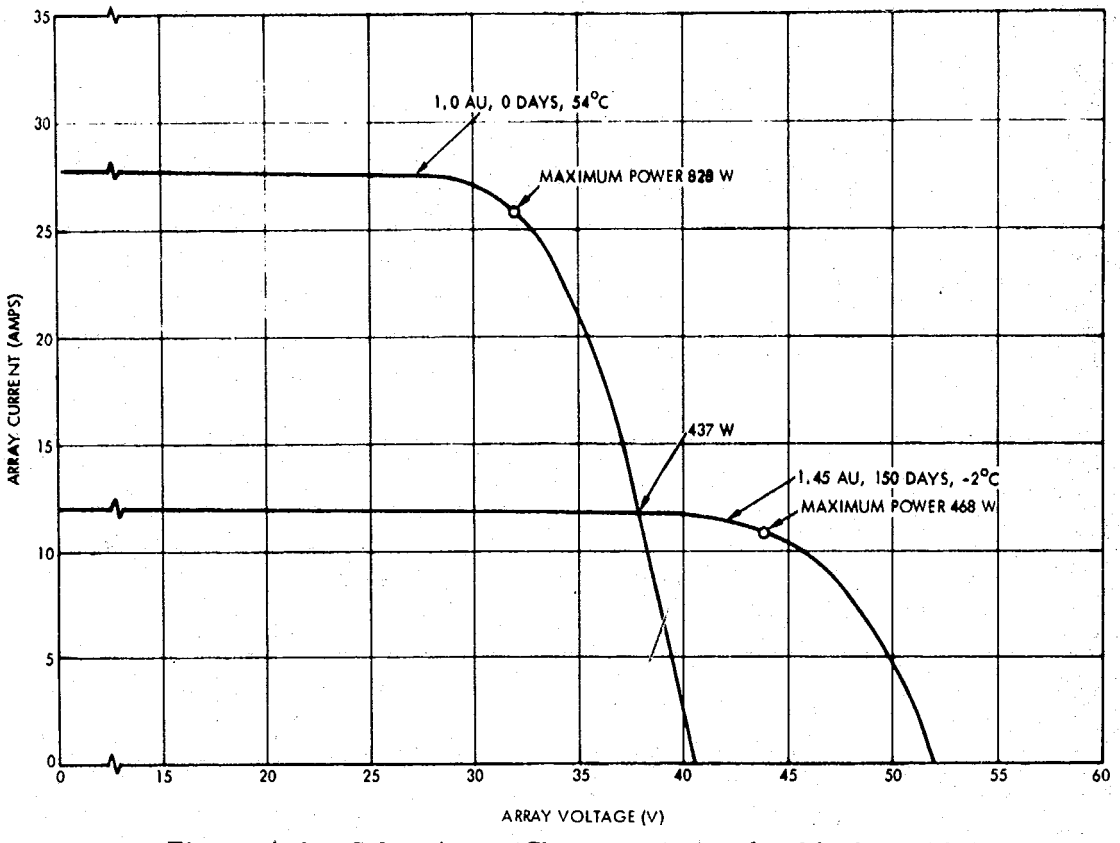


Figure 6-1. Solar Array Characteristics for Mariner-Mars Solar Panel (Predicted)

Table 6-6. Nominal Voltage and Current Degradation for Yearly Dosages of 3×10^{13} Equivalent 1 MeV Electrons per cm^2

Time (Days)	Equivalent 1 MeV Electrons per cm^2	Factor V_{oc}		Factor I_{sc}	
		Before	After	Before	After
0	0	1.00	1.00	1.00	1.00
150	1.23×10^{13}	1.00	1.00	1.00	0.962
240	1.97×10^{13}	1.00	1.00	1.00	0.930

Cover Slide Transmittance Degradation due to Micrometeoroid Fluence

Time (Days)	Factor
0	1.00
150	0.995
240	0.992

Adhesive and Cover Slide Degradation due to Ultraviolet Radiation

Time (Days)	Factor
0	1.00
150	0.988
240	0.985

Table 6-7. Solar Cell Module Weight Analysis

Unit	Quantity	Unit Weight (Lb x 10^{-3})	Total Weight (Lb x 10^{-3})
Solar cell	18	1.21	21.78
Cover slide	18	0.99	17.82
Cell interconnect	20	0.026	0.52
Module interconnect	4	0.035	0.14
Bus bar	1	--	1.27
			41.58

Table 6-8. String-Pair Weight Analysis

Unit	Quantity	Unit Weight (Lb x 10^{-3})	Total Weight (Lb x 10^{-3})
Substrate	1	Unknown	Unknown
Module	26	41.58	1081.1
Diodes	2	0.606	1.21
Connector	1	Unknown	Unknown
Terminals	6	0.14	0.84
Terminal board	1	1.6	1.6
Module adhesive	As required	--	46.8
Wire	--	--	33.0
Miscellaneous	--	--	25.0
			1189.55

6.2 BATTERY ANALYSIS

6.2.1 Mariner-Mars Requirements

There are two missions presently under consideration: A flyby and an orbiter. In the flyby mission, the battery must provide essentially the same level of performance expected of the present Mariner '69 battery. It was determined that the present Mariner '69 battery should satisfy the electrical and life requirements of a flyby mission.

However, on an orbiter mission, battery power will be required at 150 and 160 days into the mission, and two additional charge/discharge cycles will be required. It is therefore recommended that consideration be given either to upgrading the present battery to meet the more severe requirements of the orbiter mission or to designing a new battery incorporating recent developments in silver-zinc battery technology. This subsection discusses the major design considerations and recommends possible methods of improving the present Mariner battery to meet the requirements of a future Mariner spacecraft.

6.2.2 Mariner-Mars Characteristics

6.2.2.1 Description

The Mariner '69 battery is nominally a 50-AH design with up to 65 AH of actual capacity available from a new, freshly charged battery (measured at room temperature, 10A discharge rate to a final battery voltage of 25.8 V). The watt-hour output is nominally 1200 WH with an actual capacity of about 1350 WH. The battery consists of 18 series-connected silver-zinc cells (Electric Storage Battery Model 257-20138), which are produced in three cell monoblocks. Cells are individually sealed and completely potted into a battery canister. Battery weight is 34.95 lb with the cell pack alone weighing 28 lb.

During forming battery charging is accomplished by using a two-step constant current charge. The battery is first charged at 2.0 A to 1.97 V/cell; then it is charged at 600 ma until 1.97 V/cell is again reached. The present spacecraft charger characteristics result in a modified constant potential charge where current is initially limited to 600 ma, and after about 80% of charge energy has been returned, the current tapers off at a fixed constant potential of 34.6 V.

The present Mariner battery must provide two discharges of up to 1200 WH and be capable of one recharge in flight during the first 120 days of flight. Batteries stored fully charged have lost capacity at about 1% per month at room ambient, while storage at 50°F for up to 4 years has resulted in very little capacity loss (5 to 10% observed). It has been found that storage on open circuit in the fully charged state results in the longest life. Extended trickle charge has been found to shorten life.

6.2.3 Recommendations

Recommended improvements to increase battery life and cycle capability are presented below in order of ease of implementation:

a. Maintain battery temperature over the temperature range 60 to 90°F during usage and below 50°F when not in use.

b. Limit battery overcharge.

c. Charge battery at C/20 rate or lower to a voltage cutoff.

d. Charge battery using an asymmetric dc regime.

e. Replace one or more layers of existing separator with materials more resistant to zinc dendrite penetration.

f. Reduce possible occurrence of cell leakage by improving cell design.

The implications of these recommendations, the detailed results of testing, and the TRW analysis are discussed in the remainder of this subsection.

6.2.3.1 Battery Temperature Limits

The present battery temperature control anticipated during the flight of Mariner '69 will provide a suitable environment for battery operation. It is important, however, to consider the deleterious effects that extremes of temperature have on silver-zinc batteries. At temperatures below 32°F, divergence of cell characteristics can cause gas evolution during charge. At temperatures above 100°F, degradation of separator material and dissolution of negative active material can cause premature failures. Operation at temperature extremes can be tolerated but should be limited, particularly at high temperatures as the degradations are cumulative. Batteries under storage should be maintained at or below 50°F for best results.

Since heat is evolved during battery discharge, it is necessary to provide adequate paths for conducting heat away from the battery. Heat generation can be estimated by using the expression:

$$q = (Erev-E)\, I + \frac{4.186\, IT\, |\Delta S|}{ZF}$$

where

q = W of heat

E = V

I = amp

T = ^{o}k

ΔS = Cal/mole ^{o}k (or entropy units)

4.186 = conversion factor, calories to joules

Z = number of electrons transferred in the chemical reaction

F = Faraday's constant (96,500 A-sec/g equivalent)

E_{rev} = battery reversable potential (V)

The center of heat evolution is the electrode pack, and temperatures at the pack center may be 15 to 20°F higher than the cells outside surface temperature. Thus, it is desirable when operations at the 2-hr rate or above are anticipated, to provide intercell heat transfer fins. In the present Mariner design this would not be possible because the cells are fabricated in three-cell monoblock units. An additional benefit gained with heat transfer fins is the stiffening of the plastic intercell walls.

6.2.3.2 Limit Battery Overcharge

By tabulating the battery discharge and charge usage on an A-H basis, battery recharge may be terminated when A-H charge input just balances discharge output. On an A-H basis, the silver-zinc system is approximately 95% efficient (over the temperature range of 60 to 90°F) with some variations due to differences in internal cell construction; so by integrating the current-time telemetry it would be possible to terminate charge at 105 to 110% A-H returned.

The effects of excess charge on life are discussed later. Overcharge not only adds very little energy to the battery but promotes degradation since zinc dendrite growth is severe on overcharge.

6.2.3.3 Battery Charge Rate

To minimize battery degradation it is best to charge at the most rapid rate available which will not result in gas evolution or excessive heating. The C/20 rate (about 2.5 amp for a Mariner '69 battery) normally provides an optimum charge rate for silver-zinc batteries. Charging rates may vary from the C/10 rate to the C/50 rate, depending on internal cell design and available power.

When charging at a constant current, the approach of full charge is signified by a rise in battery voltage and pressure. Charge termination voltage will depend on the charge rate and internal cell construction. Review of the literature indicates that charge termination voltages of 1.94 to 2.00 V have been used.

An optimum charge termination voltage should be determined by a limited test program utilizing prototype cells fabricated into a battery. For different charge-current and termination-voltage combinations, the battery A-H capacity is determined and the selected termination voltage should be the value which returns sufficient capacity (plus a safety margin) over the anticipated temperature range. In the past, charge termination voltages have been selected to maximize charge return while sacrificing battery life. On the Mariner-Mars Orbiter mission, the useful battery life required will be 50% greater than that required for a flyby battery, so operations should be designed for extending life.

6.2.3.4 Separator Changes

The present battery life is limited by zinc dendrite penetration of the one layer of polypropylene and six layers of battery-grade cellophane.

Materials presently available for use in battery separators have shown zinc dendrite penetration resistance superior to cellophane (Weiss, Kelly, "Alkaline Battery Separator Study, NAS-5-2860, Final Report, 31 July 1964").

Some superior materials are shown in Table 6-9, with cellophane shown as a reference. Other materials presently in use which have also shown superior zinc penetration resistance but not covered in this report are of the modified polyethylene type.

It should be noted that many materials showing superior zinc penetration resistance are found to depress cell voltage because of high resistivity. Thus a judicious replacement of one or two turns of cellophane with a zinc stopper may extend useful battery life without appreciably affecting voltage levels. A limited amount of cell and battery pack testing would be desirable to adequately identify any performance variations when a change is contemplated in cell separator materials.

Table 6-9. Zinc Penetration Resistant Materials

Material	(A) Wet Thickness (cm x 10^{-4})	(B) Time to Penetration (min)	(C) Ratio B/A (min/cm x 10^{-4})
Cellophane (PUDO-300)	71	117	1.6
Cellophane PUDO-600 Ag. treated (NASA C-19-600)	112	310	2.8
Permion 600 (Modified cellophane)	79	158	2.0
Clear sausage casing	216	1336	6.2
Fibrous sausage casing (smooth side facing Zn)	178	425	2.4
Permion 300 (modified polyethylene)	36	117	3.2

(Source: "Alkaline Battery Separator Study," NASA-5-2860, Final Report, 31 July 1964, p 43).

6.2.3.5 Asymmetric DC Charge

Asymmetric dc charging where charge current is varied periodically (with short periods of discharge between charge periods) will produce a more uniform zinc electrode deposit with a possible reduction in dendrite formation.

6.2.3.6 Reducing Possibility of Cell Leakage

a. Monoblock Redesign

The present three-cell monoblock used by Electric Storage Battery Company results in an unequal wall thickness between the two center cells of a monoblock and cells in adjacent monoblocks. If gas evolution occurs in one of the center cells, an unbalance in pressure between the cells will cause the cell wall to deflect and eventually crack (most likely at the side and proceeding along the cell height), causing a common electrolyte path between cells and loss of two cells. By eliminating the monoblock approach and substituting individual cells, the individual cell walls will offer additional rigidity and require the rupture of two separate structures for intercell leakage. When using separate cells, it is also possible to insert lightweight metal or honeycomb stiffeners between cells to provide support for the cell walls. An additional benefit gained by using metal stiffeners is the transfer of heat from the cell stack center to the battery base and then away from the battery. Yardney Electric Company used this approach in work done under JPL Contract 950959.

b. Charge Control

In a normally operative silver-zinc cell, pressure is generated when the positive electrode reaches full charge and all additional energy supplied produces oxygen gas. Continuous overcharge at rates of C/1000 for 15 days was demonstrated under JPL Contracts 950811 (Whittaker Corporation, Power Sources Division), 950959 (Yardney Electric Company), and 950495 (Electric Storage Battery Company, Missile Battery Division) at the cell level. During one test run (ESD Report E 41-63), ESB had a four-cell pack under test with a shorted cell. The shorted cell operated at about 1.61 V throughout the test, resulting in severe gassing in two cells and the shorting of a third cell. Pressure in the two good cells had risen to between 45 and 55 psi after 80 hours of overcharge. In a less extreme case than is created by a failed cell, it would appear likely that some cells may be overcharged while others are undercharged due to normal production variation between cells. This is borne out by a review of the constant potential charge voltages of cells on test by ESB. Variations of 50 mV between cells in a four-cell battery were quite common on test (ESB Report E 35-63).

Charge performance of batteries may be improved by:

a. Producing a more uniform cell

b. Matching cells on initial cycle electrical performance

c. Monitoring cell voltages individually

d. Controlling individual cell charge

e. Modifying charging technique

f. Monitoring pressure.

Cell construction methods can be improved by 100% parts inspection and closer tolerance control on individual components. Typically, silver-zinc cell electrodes are manufactured to about ±5% weight tolerance. It is entirely possible to control plate weight to ±1%, and this was demonstrated on nickel cadmium and silver cadmium batteries by Wagner and Enters ("Development of Manufacturing Methods and Techniques for the Production of Improved Alkaline Batteries," Wagner and Enters, AF33(615)-2578).

In addition, material lot control of components going into a battery can help provide homogeneity between cells. During work on the Surveyor main battery, it was found that cell failures within a battery could often be traced to differences in positive electrode production lots. After manufacture of all cells within a particular battery from a single electrode production lot, an improvement in life was noticed; and cell voltages on float charge were found to be closer than for earlier mixed-production-lot batteries.

Matching of cells on initial cycle electrical performance is normal practice for nickel-cadmium and silver-cadmium batteries that must operate for a large number of cycles without failure. Silver-zinc batteries normally are not matched because only one or, at most, two cycles are required in most applications. In the Mariner-Mars Orbiter application, a total of four charge/discharge cycles will be required in flight. Thus it would be desirable to match individual cell

performance to produce a well-matched battery. The present Mariner '69 battery, consisting of six three-cell monoblocks, can at best be matched to the average monoblock performance.

As an in-flight diagnostic tool it would be desirable to monitor individual cell voltages. Since impending failures may be preceded by an unsteady cell voltage (about 0.1 V swings), cell-level monitoring could permit detection (0.1 V is about 5% of the nominal value); while battery level monitoring (0.1 V is about 0.3% of the nominal value) would not allow detection. With cell-level monitoring, charge could be limited to avoid overcharging the normal cells and discharge could be terminated before the shorted cell reversed voltage and started generating gas.

By the use of cell bypass electronics, it would be possible to limit cell reversal voltage to levels where excessive gas is not evolved. The bypass circuit essentially shunts current around the cell during discharge. Thus, a shorted cell contributes energy only over the useful voltage range but is restrained from operating in regions causing battery failure by open circuit.

Charge time and particularly overcharge time should be minimized. The normally recommended charge rate for silver-zinc batteries is approximately the 20-hr rate. Work at JPL has indicated the adverse affects that overcharge has on life. Work done by Leesona-Moos (NAS 5-3908) clearly points out that dendrite growth occurs during conditions normally encountered on overcharge. Thus, charging should be conducted at the maximum available rate to a voltage limit. The exact voltage limit would be dependent on charge rate and, to a lesser extent, on temperature over the range 60 to 100°F. Charge termination voltages reported in the literature vary between 1.94 and 2.00 V per cell.

The Leesona-Moos studies pointed out the desirability of periodically varying charge current to produce a smooth, more dendrite-free zinc electrode in silver-zinc cells. Work by Wales (Wales, "Charging the Silver Electrode with Periodically Varying Current," J. Electrochemical Society, 1968 July indicates that, by using an asymmetric charge regime where discharge periods are interspersed between charge periods, increased A-H capacities were obtained over those obtained with continuous dc charge. Wales does not comment on life expectancy, but 23 to 53 cycles were obtained on individual cells. In U.S. Patent 2,678,909, it is pointed out that by using an asymmetric charge method similar to that used by Wales, smooth deposits of zinc were obtained for commercial zinc plating. It would appear that use of a periodically varying charge current where there is a small amount of discharge between current cycles would tend to prolong battery life while providing greater available battery energy.

Monitoring of battery pressure could provide a useful diagnostic tool for establishing battery condition. The evolution of oxygen gas at the completion of charge could be used for control purposes. In the event a cell shorts on charge, gas evolution could be used as a more sensitive detector than battery voltage (depending on battery-free volume). This technique was used on the Surveyor main battery where battery pressure was monitored and used in conjunction with battery voltage (in flight) and cell voltage (during test).

To implement battery pressure sensing, it would be necessary to provide a common gas path between cells leading to a pressure transducer. Design of a common gas manifold presents problems in preventing electrolyte from entering the gas space and in providing an effective seal between adjacent cells and the outside environment.

6.3 UNDESIRABLE SOLAR ARRAY BATTERY LOAD SHARING

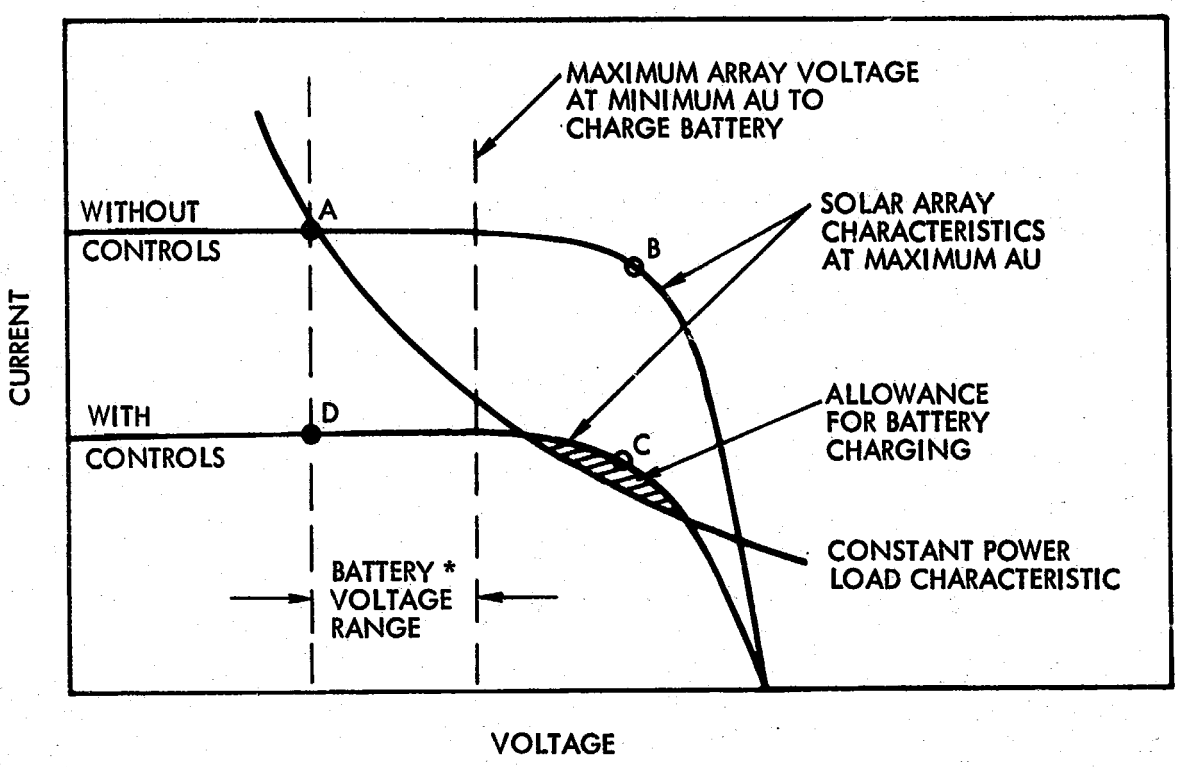
A potentially large penalty in solar array sizing results from those system configurations which combine the battery and solar array electrically at an unregulated bus. In this type of a system, the bus voltage will vary from minimum battery discharge voltage to a maximum equal to or greater than maximum battery charging voltage. As a result, the solar array when oriented must be capable of supporting the load over a relatively wide range of voltage. In a typical case, the load connected to the unregulated bus approaches a constant power characteristic as a function of bus voltage; therefore, at lower voltages, current demand is considerably higher than at the higher end of the bus voltage range. Unless the solar array is designed to supply adequate load current at minimum unregulated bus voltage, or unless appropriate controls are included in the system, a stable operating condition exists in which the battery is required to share the load with the solar array, even though the solar array power capability at higher voltage is adequate to support the entire load.

Figure 6-2 illustrates the difference in required solar-array capability between a system designed with appropriate controls to overcome this undesirable load-sharing condition and a system without such controls.

In a simple case, such as initial solar array orientation, the battery is normally discharging to support the total load and the bus voltage is at the lower end of its range. As the solar array is oriented, it will deliver current to the load and, neglecting battery voltage regulation characteristics, must be sized to supply the total load current at the minimum operating voltage. When the array current capability builds to the point (Figure 6-2, Point A) at which battery discharge is no longer required, the bus voltage will rise, the load current will reduce, and the battery will begin accepting charge from the solar array. Since battery-charging current requirements for the specified Mars mission are low and a large difference in voltage can exist between battery discharge voltage and array maximum power point voltage (Point B), an array designed in this manner will severely penalize solar-array power utilization and, therefore, weight.

To improve the utilization of array power, a momentary battery discharge booster may be employed to force the bus voltage to a higher level when an unnecessary load-sharing condition exists. With this approach, the solar array may be designed to provide required load current only at voltages closer to its maximum power point (Figure 6-2, Point C). The booster power capability need only be adequate enough to supply the difference in power between the load requirement at battery discharge voltage (Point A) and the solar array capability at that same voltage (Point D).

Power systems which generate a regulated dc bus directly by regulating both battery and solar array outputs independently require a continuous boosting regulator for battery discharge. This approach, of course, eliminates the problem of undesirable load sharing.



* BATTERY VOLTAGE RANGE DETERMINED BY ARRAY VOLTAGE CAPABILITY AT MIN AU

Figure 6-2. Comparison of Required Solar Array Capabilities With and Without Controls to Prevent Undesirable Load Sharing

6.4 LINE REGULATORS

6.4.1 Description of Functions

The basic function of the line regulator is to accept an unregulated power input from either the solar array or the battery, and then to electrically condition the output voltage or the output current, or both, in order to power the loads in an adequate manner. It must function effectively in conjunction with the current-sharing-mode sensor, battery controls, logic circuitry, and failure detectors.

6.4.2 Analysis of Existing Mariner Design*

6.4.2.1 Areas for Improvement

6.4.2.1.1 Current Limiting. There is no current limiting in the existing design; therefore, the system is unable to avoid the propagation of certain failures associated with the flow of high currents once they have originated at any of the circuits powered by the boost regulator.

Current limiting, in itself, is a good practice whenever the circuit configuration involves relays that must switch under fault conditions. This is so because the failure rate of a pair of contacts in a relay increases from about 12 failures/10^9 cycles at rated load, to approximately 500 failures/10^9 cycles for a short (few hundreds of msec) 300% overload. Overloads exceeding the latter condition have a much higher failure rate which is further evidenced by the fact that the relay manufacturers are unwilling to disclose any failure data for overloads exceeding 300%.

Assume, for instance, that one of the power transistors in the 2.4-kHz inverter shorts, and that the fault impedance is in the order of 0.5 ohm (which is realistic for the circuit under consideration). The boost regulator will sense a decrease of output voltage and will attempt to restore to normal voltage level by increasing duty cycle. This means that the power transistors in the boost regulator will not only carry an overload of 300 to 400% or higher, but will be in a conductive state for a longer time, and therefore could be expected to fail in fewer cycles. This first propagation of a failure will result in the low fault impedance (short) being extended now to the boost regulator itself. This will occur regardless of whether the transistor first fails shorted or open, since either failure will reflect an effective short back to the power sources (an open power transistor in a center-tap auto-transformer causes the saturation of the latter). Although the existing Mariner approach has provisions to replace the entire main power chain in case of failure, the fact remains that the extended or propagated fault may well cause a further reduction of the short impedance, thus worsening the high current-failure conditions that the DPDT relay has to see while switching.

6.4.2.1.2 Drift of Voltage Regulation Point. Although the Mariner booster regulator relies on a differential amplifier to sense the magnitude of the error, the collectors have different levels of dissipation. This causes a temperature difference between both transistors that eventually leads to an unbalance of electrical characteristics within the differential amplifier. Such an unbalance is amplified by the fact that the differential amplifier has a single-ended output.

An improvement would be to consider the following:

- Balance the impedances connected to both collectors to equalize their dissipation as much as possible.
- Substitute a differential output connection for the single-ended one. This could be implemented by substituting a complementary pair of transistors for Q6.

*Existing Mariner designs are referenced in Appendix A.

6.4.2.1.3 Regulator Transient Response. The circuit stability of the existing Mariner configuration appears to be satisfactory in the sense that the circuit is free of any oscillatory mode of operation. However, the transient response, occurring during the rejection or sudden application of loads, does not appear to be optimum in terms of voltage overshoots, voltage dips, and recovery time, or it may be optimum only for certain load and input/output voltage conditions.

The negative feedback windings shown in Figure 6-3 allow an optimization of output voltage dip and overshoot over a broad range of temperature, load, and input/output voltage conditions.

6.4.2.1.4 Fuses in the Main Power Chain. The risk of losing the mission due to the high failure rate of the relays when switching currents much in excess of their ratings can be circumvented by fusing the main power chain and by providing separate relays to activate the main and the standby boost regulator. This way, if the relays associated with the main power chain fail to open due to arcing of contact welding, the fuses will isolate the failed chain. An independent set of relays for the standby boost regulator would allow the transfer of power from the main chain to the standby chain without trouble.

6.4.2.1.5 Maximum Duty Cycle Capability. The existing boost regulator does not have maximum duty cycle control capability (allows for regulation over wide input voltage range) due to certain limitations in the self-saturating magnetic amplifier.

The following techniques will improve the duty cycle range by improvement in the steepness of the leading edge of the magamp's waveform:

- Increase amplitude of excitation voltage.
- Rise time of excitation voltage must be as small as possible. This in turn depends on the rise time of transistors Q1 and Q2 and on minimization of leakage inductance in transformer T2.
- The magnetic material used for T3 must have a squareness as close to unity as possible.
- The core geometry and the winding techniques chosen for T3 must result in a minimum saturated inductance.

Note: Once maximization of the duty cycle capability for the magamp has been obtained, verify that the on-state of transistors Q7 and Q8 does not overlap for the condition of maximum duty cycle.

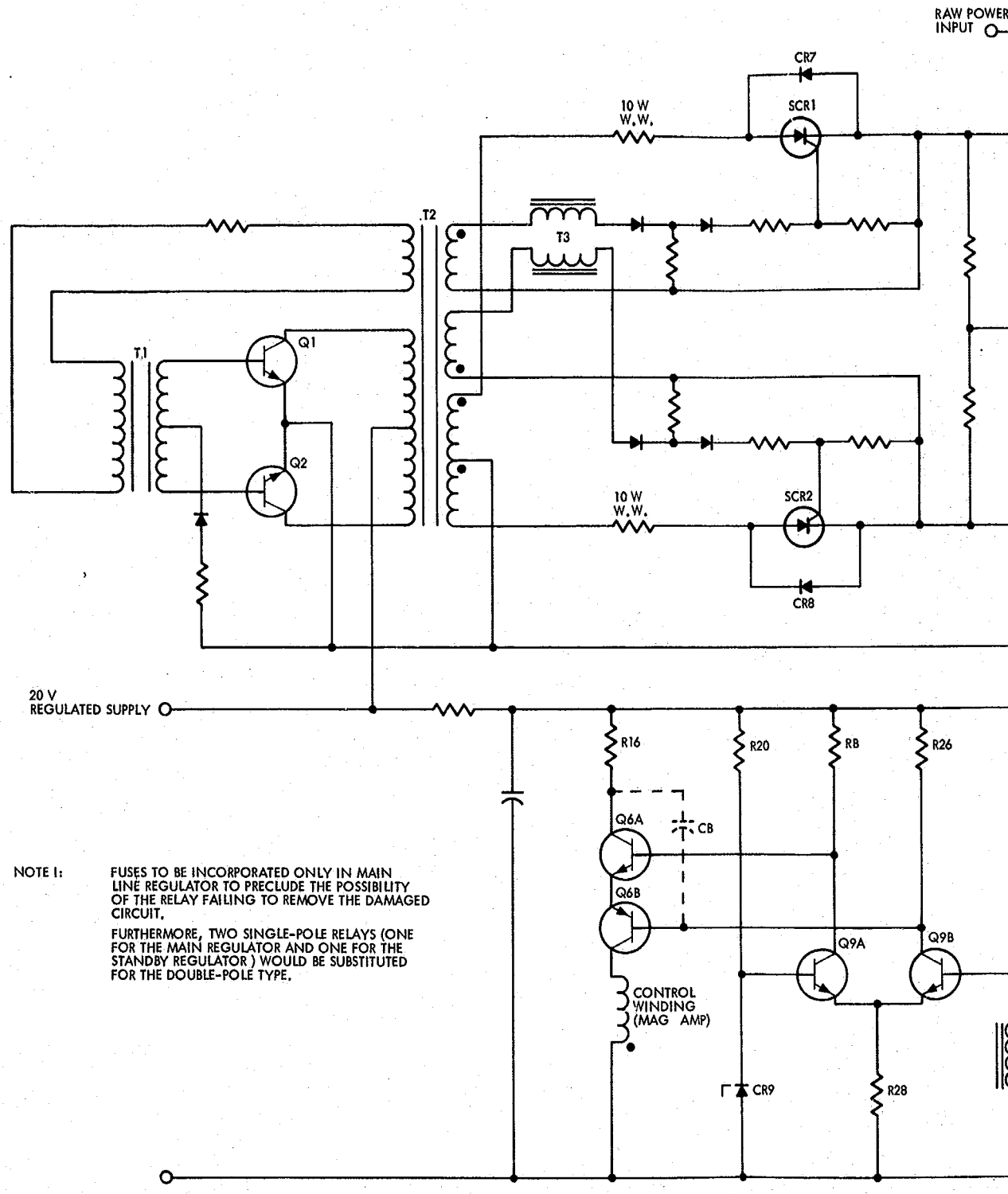
6.4.2.1.6 Frequency Failure Detection. At present, any frequency failure occurring in another element (the 2.4-kHz inverter) causes the substitution of the standby boost regulator for the good main boost regulator (the entire power chain being substituted). This is conceptually unreliable since the boost regulator is the most relevant link, in terms of power handling, of the power chain.

6.4.3 Approaches Considered

6.4.3.1 Preliminary Screening

6.4.3.1.1 Basic Circuit Configurations Considered

a. Autotransformer type (Mariner) approach . This approach consists basically of a boosting, center-tapped autotrans-



NOTE 1: FUSES TO BE INCORPORATED ONLY IN MAIN LINE REGULATOR TO PRECLUDE THE POSSIBILITY OF THE RELAY FAILING TO REMOVE THE DAMAGED CIRCUIT.

FURTHERMORE, TWO SINGLE-POLE RELAYS (ONE FOR THE MAIN REGULATOR AND ONE FOR THE STANDBY REGULATOR) WOULD BE SUBSTITUTED FOR THE DOUBLE-POLE TYPE.

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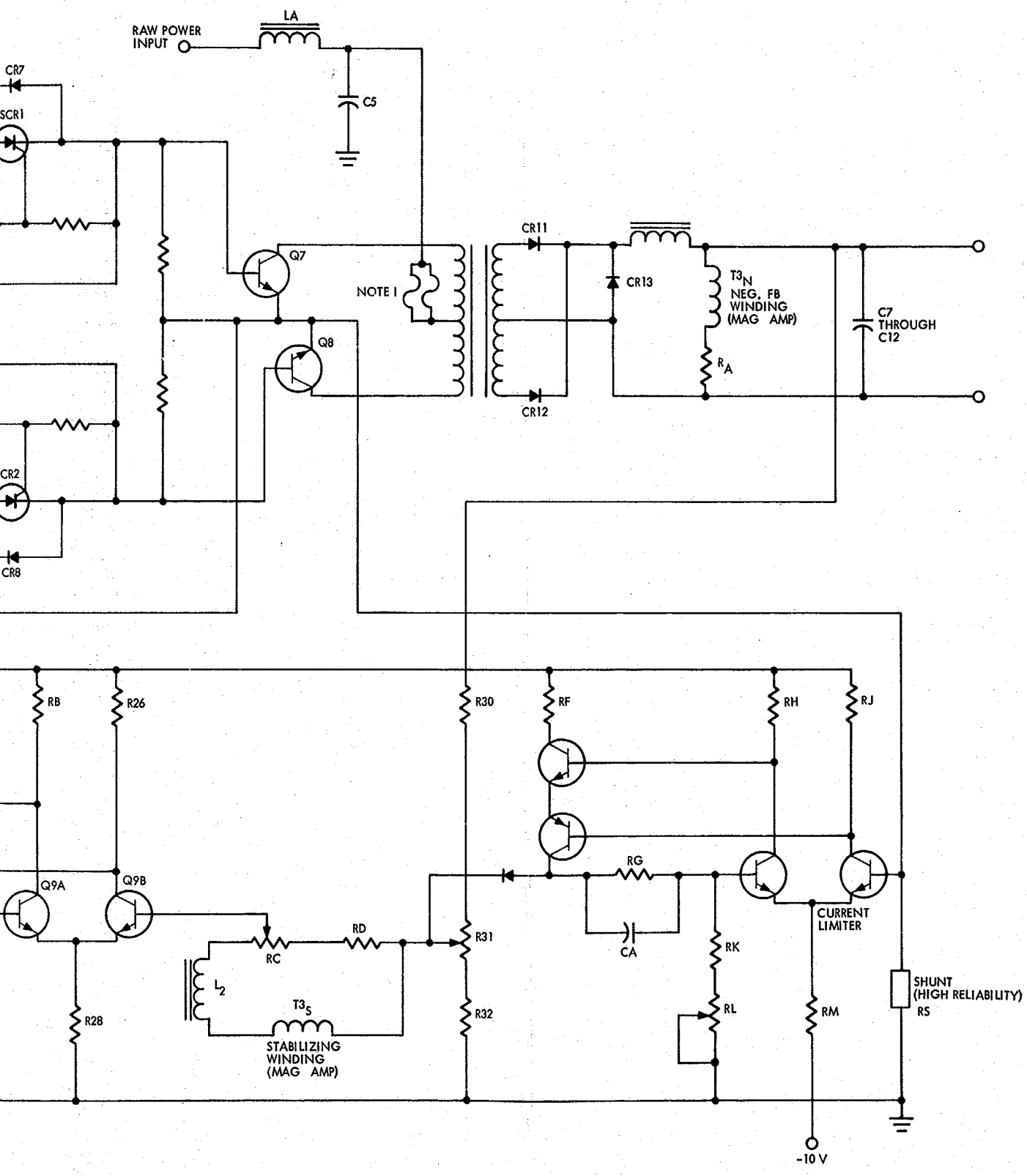

Figure 6-3. Fully Stabilized Boost Transformer Regulator

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former being powered by the unregulated bus voltage and transistors. For minimum duty cycle, the output voltage is equal to the input voltage minus the forward voltage drop across rectifier CR13. For maximum duty cycle the ratio of output-to-input voltage approaches the autotransformer ratio.

The output filter is composed of L1 and the output capacitor bank that filters the output voltage of the autotransformer, and a saturable transformer oscillator that sets the operating frequency.

The regulating loop is mechanized by means of a differential amplifier that compares the output voltage against a temperature-compensated zener diode, CR9. The single-ended output of the differential amplifier is followed by a current amplifier, Q6, that drives a self-saturable magnetic amplifier, T3. The duty cycle of T3 decreases as the control current increases, and it undergoes a process of current amplification via SCR_1 and SCR_2 before controlling the duty cycle of the power transistors, Q7 and Q8.

b. Converter transformer approach. See Figure 6-3, Fully Stabilized Boost Transformer Regulator. This approach has a similar principle of operation to a., differing from it only in certain specific features:

- The use of a transformer makes the circuit apt for current limiting.
- A differential amplifier having a differential output, followed by a complementary pair, optimizes the balancing properties of the differential amplifier, resulting in less voltage drift as a function of temperature and life.
- Stabilizing winding T3's determine circuit stability with maximum speed by taking advantage of a magamp winding that couples the circuit in a transformer fashion, thus by-passing the slow magamp properties in the feedback mechanism.
- Winding T3's aids in minimizing the dip and overshoot occurring during the application and rejection of steploads.

c. Transformerless approach. See Figure 6-4. In this circuit the energy delivered to the load is controlled by the duty cycle of transistor Q1. The output-to-input voltage ratio is related to the transistor operation as follows:

$$\frac{Eo}{Ein} = \frac{T}{Toff}$$

where

Eo = output voltage

Ein = input voltage

T = duration of one full cycle

Toff = portion of the cycle when the power transistor remains off.

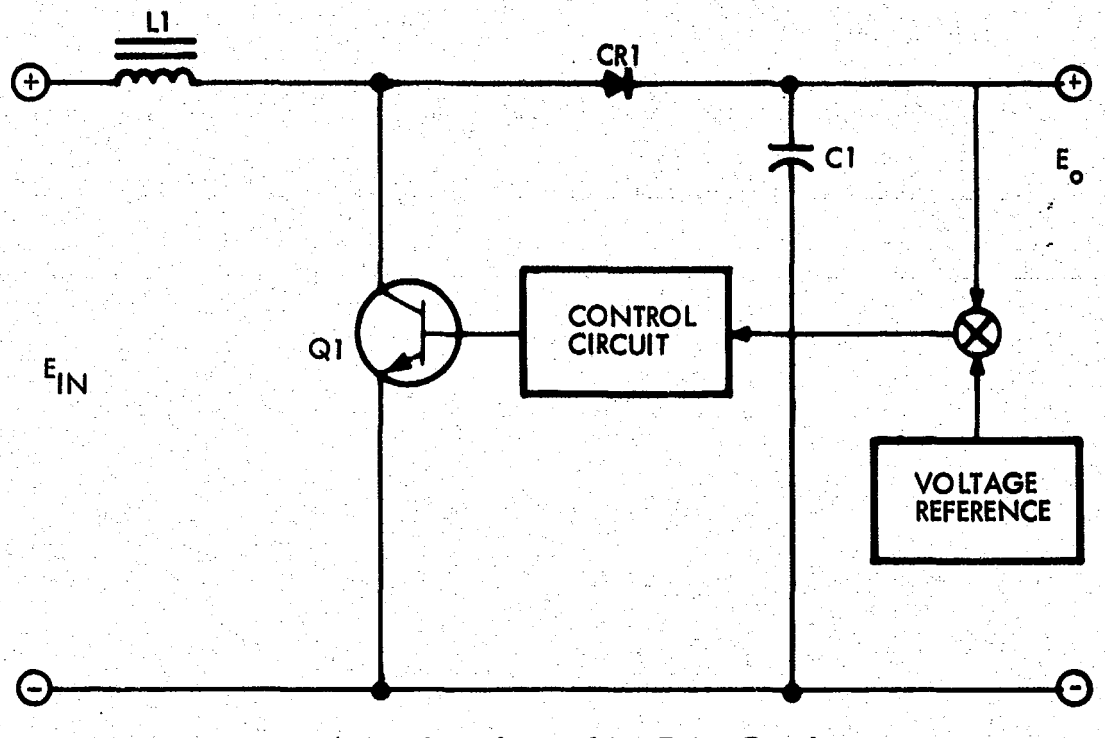

Figure 6-4. Transformerless Boost Regulator

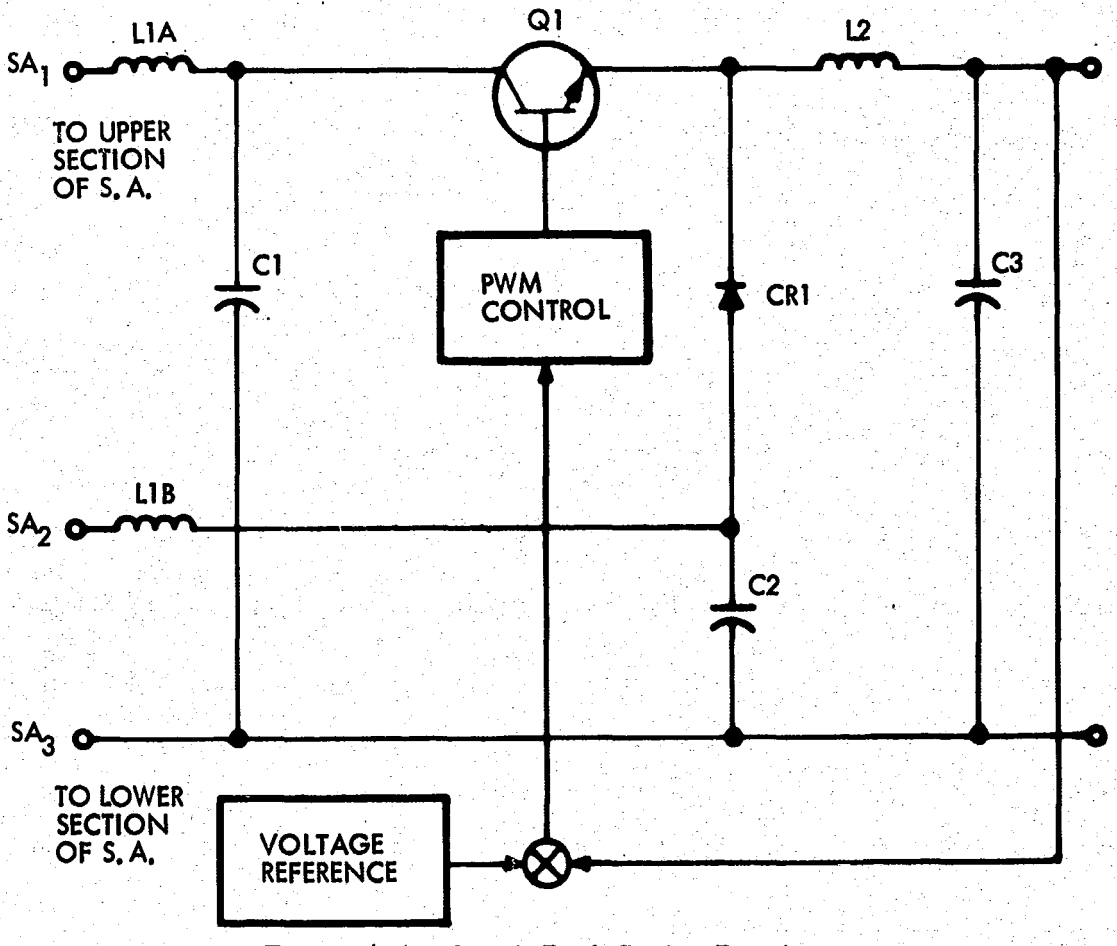

Figure 6-5. Quasi-Buck Series Regulator

d. Quasi-buck series regulator. See Figure 6-5. This approach is a variation from the well-known buck series regulator. The functional differences from the buck type can be stated as follows:

- Q1 and CR1 do not have to support the entire solar-array voltage, but just a fraction of it.
- The output filter is more effective in the sense that it has to filter only the ac component of a fraction of the solar-array voltage.
- Although incapable to current-limit the solar array itself, it can current-limit any power source (like a battery) connected to the collector of Q1.

e. Buck-boost regulator. See Figure 6-8. The many attractive features of this circuit include the following inherent capabilities:

- Input-output isolation and current-limiting.
- Ability to step up or step down the input voltage.
- Ability to conveniently operate in either half-wave or full-wave fashion.

f. Dissipative shunt regulator. See Figure 6-6. This circuit is capable of precisely regulating the output voltage of a solar array by linearly loading a portion of the solar array. The error amplifier and driver stage (transistor Q2) comprise the regulating loop. The power transistors used in this scheme function within a Class A type of operation.

6.4.3.1.2 Comparisons. A comparison of the configurations described in Paragraph 6.6.3.1.1 is shown in the Comparison Chart, Table 6-10. Table 6-11, Relative Merits of Individual Approaches, compares the regulator approaches on a qualitative basis.

6.4.4 Analysis of Buck-Boost Regulator

6.4.4.1 Basic Operation

Figure 6-7 illustrates the energy-ladling circuit. The energy-storage transformer-inductor, T3, has a linear flux versus MMF characteristic. The transistor switch, Q1, is controlled by a closed-loop circuit to turn on and off cyclically within a time period, T. A block diagram of the back-boost regulator is shown in Figure 6-8.

Figure 6-9 illustrates the circuit current waveforms during one steady-state operating cycle. Voltage $e_1 = e_{1n}$ across N1 (number of primary turns in T3) during T_{on} causes i to increase from i_a to i_b at a constant rate $e_{in}/L_1 = e_{in}/KN_1^2$, while i_2 is zero in N_2 (number of secondary turns in T3).

At the end of T_{on}, the continuous MMF, acting on the inductor, causes $i_2 = i_b \times N_1/N_2$ to start flowing in N_2 and decreasing at a constant rate e_o/KN_2 (where e_o is the dc average voltage across the output capacitor). During this interval, T_{off}, $i_1 = 0$.

Since the increase of MMF $N_1 \Delta i_1$ during T_{on} should be identical to its decrease during T_{off} for a steady-state operation to exist,

$$N_1 T_{on} \left(e_{in}/KN_1^2\right) = N_2 T_{off} \left(e_o/KN_2^2\right)$$

K ≡ proportionality constant relating to core material and geometry, resulting in

$$\frac{e_o}{e_{in}} = \frac{N_2}{N_1} \times \frac{T_{on}}{T_{off}}$$

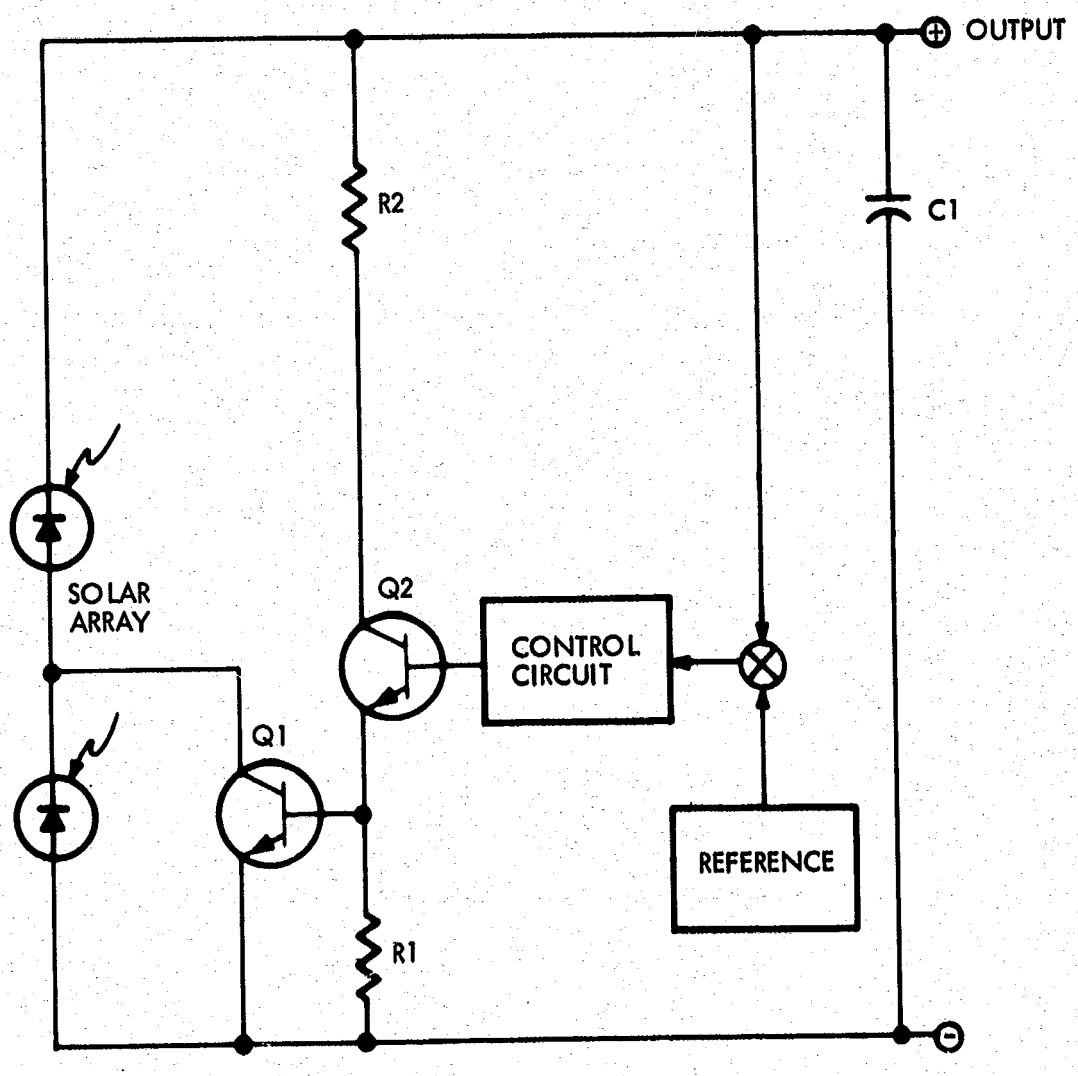

Figure 6-6. Dissipative Shunt Regulator

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System Type	Solar Array Control	Main Voltage Regulator						Fault Co		
								Series Element Shorted (N		
		Type	Weight	Efficiency	E_{in}	E_o	Redundancy	Current Amplitude	Propagation	E_o when Switcl to Standby Red
1	Zener type	Boost autot.	100%	92% (Note 2)	25-50 vdc	56 vdc	Standby	> 75 amps	a) Battery (> 50 amps) b) Solar array ≈30 amps	0
2	Zener type	Boost transf.	100% Note 3	88%	25-50 vdc	56 vdc	Standby	> 75 amps	a) Battery (> 50 amps) b) Solar array (≈ 30 amps)	0
3	Zener type	Boost transformerless	100%	88%	25-50 vdc	56 vdc	Standby	> 75 amps	a) Battery (> 50 amps) b) Solar array (≈30 amps)	0
4	None	Quasi-Buck series regulator consists of 2 sections: a) One unregulat. connected to a tap in Sol. A. through diode. b) One regulated by means of a buck pwm. (see Fig. 8)	66%	92 %	55-100 vdc	50 vdc	Standby	≈20 amps > 50 A	Sol. Array only a) Battery (> 30 A) b) S. A. (≈ 20 A)	50 vdc or E_{OS}, whichever is hi 0 However, E_o in the interim
5	None	Buck-boost	100% (Note 6)	92 (Note 7)	25-65 vdc	50 vdc	Active redundancy	≈30 A (Note 8)	a) Battery (< 30 A) b) Sol. A. (< 30 A) (Note 8)	Not applic. (T approach relie active redunda rather than sta redundancy

Note 1: Faults considered as "series element shorted" include
a) one or more pwr transistors shorted (boost, buck or buck-boost reg.)
b) one transistor open (transformer or autotr. push-pull type)

Note 2: Computed value.

Note 3: The 100 weight assumes that only one transformer is used in conjunction with two complete sets of electronic parts to complete two boost regulators (this is because the weight of an autotransformer is approximately 1/2 of that of a transf. for the ratio being considered).

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Fault Conditions								
Shorted (Note 1)		Series	Element Open	Free Wheel Rectifier Shorted				
When Switching Standby Redund.	Delay before Switching to Standby Redun.	E_o when Switching to Standby Redun.	Delay when Switching to Standby Redundan.	Current Amplitude	Propagation	E_o when Switching to Standby Redun.	Delay Before Switching to Standby Redun.	Advantage
0	≈1 sec	$E_{solar\ array}$	≈1 sec	> 75 amps	a) Battery > 50 amps b) Sol. Array ≈30 amps	0	≈1 sec	a) Simplicity in the config. of b) Few parameters to be mo
0	≈1 sec	0	≈1 sec	> 75 amps	a) Battery (> 50 amps) b) Sol. Array (≈ 30 amps)	0	≈1 sec	a) Thermally balanced differe gain and better utilization b) Stability and frequency res means of two mag amp sta (Note 4). c) Current limiting capability d) Design simplicity of failur redundancy thereof. e) Fuses incorporated in mai preclude the possibility of remove the damaged circu f) Two SPDT relays are subs type to ensure a successfu unit into the circuit after t associated SPDT relay) ha g) Input output isolation
0	≈1 sec	0	≈1 sec	> 75 amps	a) Battery (> 50 amps) b) Sol. Array (≈30 amps)	0	≈1 sec	a) Power transformer is elim
dc or $E_{OS.A.}$ hever is higher 0 ever, $E_o \geq$ 56 v e interim	≈1 sec ≈1 sec	50 vdc 0	≈1 sec However, $E_o \geq$ 56 vdc in the interim. ≈1 sec	< 20 amps > 50 amps	Sol. Array only a) Battery (> 30 amps) b) Sol. Array (≈20 amps)	50 vdc Battery booster provides output in the interim 0	≈1 sec ≈1 sec	a) Highest efficiency b) Lightest approach to provi a solar array c) Current limiting capability d) This system yields itself c voltage blackout for certai the battery is inoperative. e) Simplicity in the implement redundancy since there is f) The collector voltage ratin has only to account for the terminals SA_1 and SA_2 of t g) More effective output filter terminal of L2 experiences equal to the voltage betwee
applic. (This oach relies on ve redundancy er than standby ndancy	(Note 9)	(Note 9)	No effect	> 75 amps	a) Battery < 30 amps b) Sol. Array < 30 amps	(Note 9)	(Note 9)	a) No idle weight since all mo The circuit remains operat loosing one module. b) Incorporation of current lin this circuit does not have t currents due to shorts occu in the power inverter circu c) This configuration is fail-s it does not require standby detectors other than fuses d) This principle can operate thus increasing the effectiv

Note 4: The advantages (a) and (b) would prevail whether a transformer or an autotransf. boost regulator is used.

Note 5: A simple fail safe voltage comparator in the Quasi-buck series regulator opens transistor Q1 (see Fig. 6-5 whenever V_{c1} decreases below certain value so that an emergency voltage is available across C_1 during failures that otherwise would find the entire solar array feeding a short circuit.

Note 6: The comparison of weights takes into account the two voltage regulators (one main and another standby) of Mariner system type vs six buck-boost voltage regulator modules (all active).

Note 7: This efficiency has been calculat It is possible to either increase efficie frequencies higher than 2.4 kHz are u

Note 8: The shorting of a lower transisto fuse (connected at the input of the indiv fault currents in excess of 30 amps to

Note 9: The output voltage of the buck-bo in value before the fuse clears. The c impedance. However, the transient sh second or less.

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Table 6-10. Synoptic Comparison of Five Configurations

Delay Before Switching to Standby Redun.	Advantages	Disadvantages
≈1 sec	a) Simplicity in the config. of pwr. components b) Few parameters to be monitored by failure detector	a) No current limiting b) Double pole D. T. relays most likely will fail when switching under fault currents in excess of 75 amps. c) Fault currents occurring at the load or 2. 4 kHz inverter have to flow through the voltage regulator d) Any fault occurring at the 2. 4 kHz inv. will also result in the loss of one line voltage regulator e) Transient response cannot readily be optimized. f) Failure detector very critical for lack of redundancy
≈1 sec	a) Thermally balanced differential amplifier, higher gain and better utilization of the error amplifier. b) Stability and frequency response optimization by means of two mag amp stabilizating windings. (Note 4). c) Current limiting capability d) Design simplicity of failure detector and full redundancy thereof. e) Fuses incorporated in main line regulator to preclude the possibility of the relay failing to remove the damaged circuit. f) Two SPDT relays are substituted for the DPDT type to ensure a successful switching of the standby unit into the circuit after the main unit (and its associated SPDT relay) has shorted out. g) Input output isolation	a) Less efficient (88% instead of 92%) because a transformer has higher losses than an autotransf.
≈1 sec	a) Power transformer is eliminated	a) No current limiting b) Fault currents occurring at the load or the 2, 4 kHz inv. have to flow through the voltage regulator
≈1 sec ≈1 sec	a) Highest efficiency b) Lightest approach to provide a regulated bus from a solar array c) Current limiting capability d) This system yields itself conveniently to prevent a voltage blackout for certain failures occurring when the battery is inoperative, (see Note 5) e) Simplicity in the implementation of the standby redundancy since there is no transformer f) The collector voltage rating of Q1 (see Fig. 6-5) has only to account for the max. voltage between terminals SA_1 and SA_2 of the solar array. g) More effective output filtering since the input terminal of L2 experiences only a voltage swing equal to the voltage between SA_1 and SA_2.	a) Requires a tapped solar array. b) Requires high voltage battery
(Note 9)	a) No idle weight since all modules are active. The circuit remains operative even after loosing one module. b) Incorporation of current limiting. Therefore, this circuit does not have to support heavy fault currents due to shorts occurring in the load or in the power inverter circuits. c) This configuration is fail-safe in the sense that it does not require standby units or failure detectors other than fuses d) This principle can operate in a fullwave fashion thus increasing the effectiveness of the filters.	a) The inductor-transformer is a relatively heavy component. Therefore, an operating frequency of 6 kHz to 10 kHz is necessary for weight/efficiency optimization b)

Note 7: This efficiency has been calculated using 2, 4 kHz as switching frequency. It is possible to either increase efficiency or decrease weight if operating frequencies higher than 2, 4 kHz are used.

Note 8: The shorting of a lower transistor or the input filter capacitor cause the fuse (connected at the input of the individual module) to open. This may cause fault currents in excess of 30 amps to flow before the fuse is cleared.

Note 9: The output voltage of the buck-boost regulator will experience a decrease in value before the fuse clears. The clearing time depends on the short circuit impedance. However, the transient should be completed in approximately one second or less.

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Table 6-11. Relative Merits of Individual Approaches

Concept	Approach					
	(a)	(b)	(c)	(d)	(e)	(f)
Efficiency: 1 = very high, 2 = high, 3 = medium	1	2	2	1	2	3
Weight: 1 = light, 2 = not as light, 3 = medium	2	3	2	1	2	3
Current limiting: 0 = incapable of, 1 = easy to implement, 2 = it current-limits the battery but not the S. A.	0	1	0	2	1	0
Fail-safe transfer of modules in case of any type of failure:	No	Yes	No	Yes	Yes	Yes
Input/output isolation:	No	Yes	No	No	Yes	No
Minimum voltage drift: 1 = excellent, 2 = intermediate	2	1	1	1	1	1
Transient response optimization: 1 = optimum, 2 = intermediate	2	1	2	1	2	1
Failure-detector simplicity and ease of incorporating redundant failure detectors: 1 = best, 2 = intermediate, 3 = poor	3	2	3	1	1	1
Failure propagation:	Yes	No	Yes	No	No	No
Incorporates transformer or auto-transformer:	Yes	Yes	No	No	Yes	No
Type of redundancy: A = active, S = standby	S	S	S	A	A	A
Requires tapped solar array:	No	No	No	Yes	No	Yes

NOTES: 1. Definition of approaches

(a) Auto-transformer type (JPL approach)
(b) Converter transformer
(c) Transformerless
(d) Quasi-buck
(e) Buck-boost
(f) Dissipative shunt

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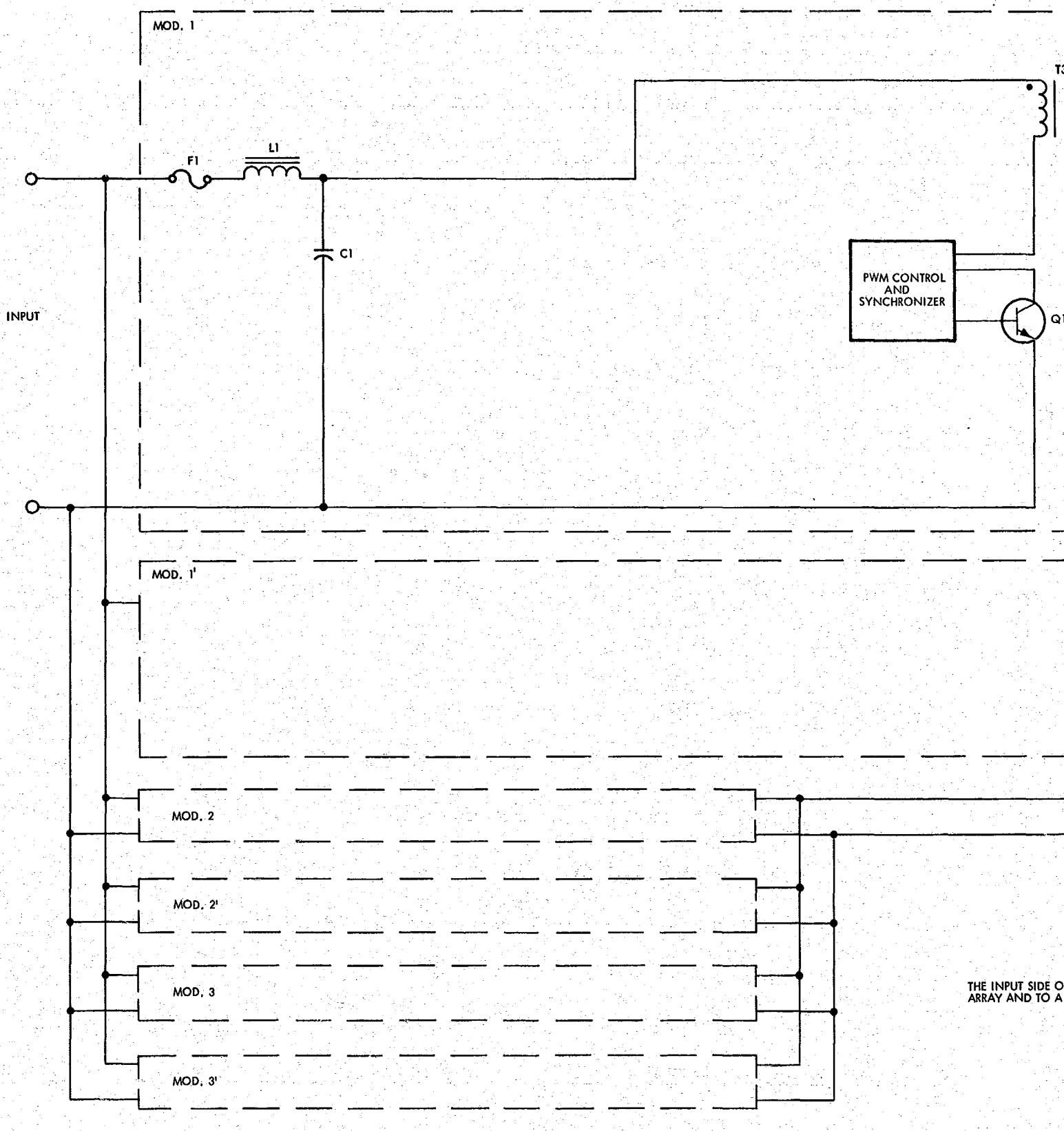

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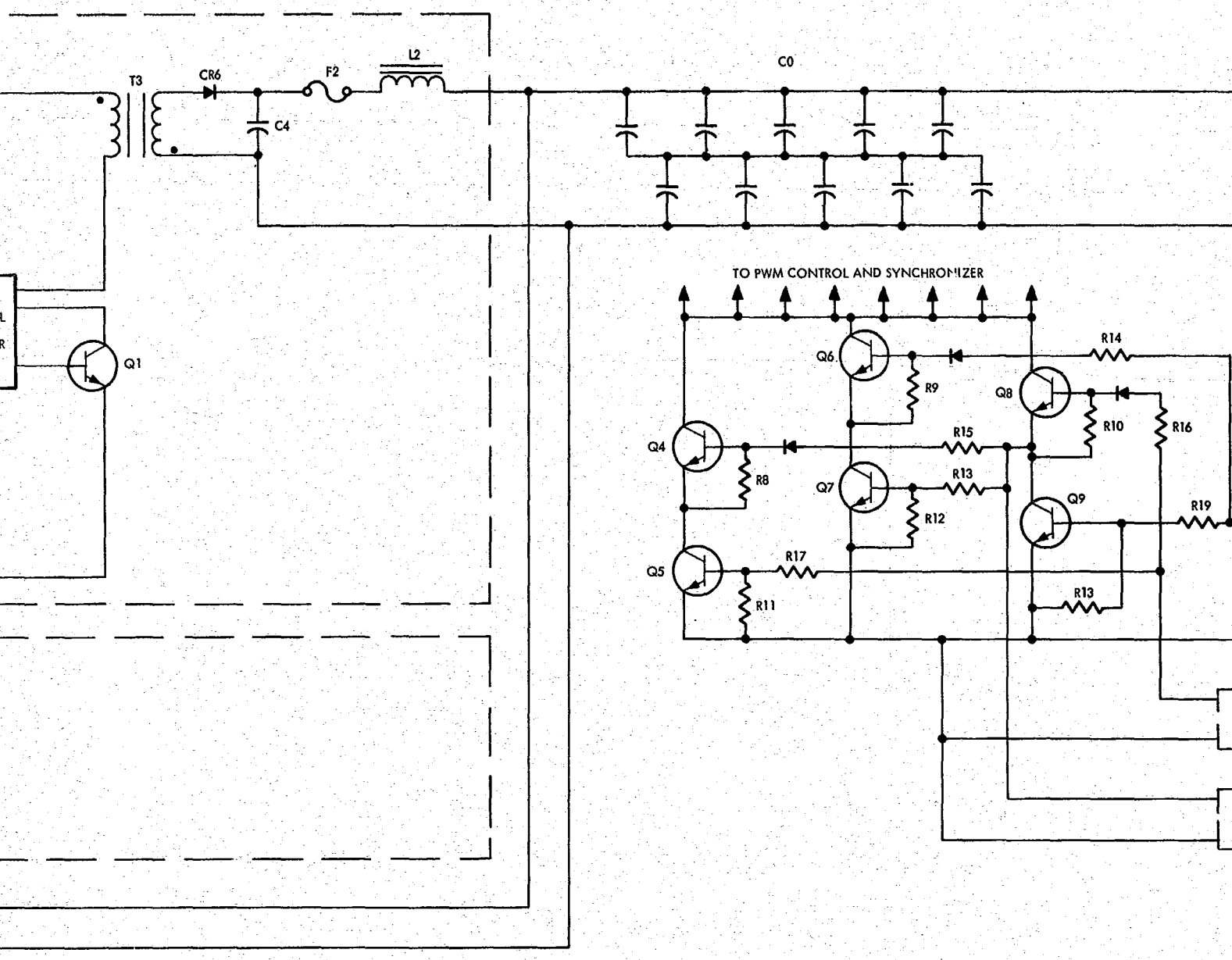

THE INPUT SIDE OF EACH MODULE IS CONNECTED TO THE SOLAR ARRAY AND TO A RECTIFIER QUAD GOING TO THE BATTERY.

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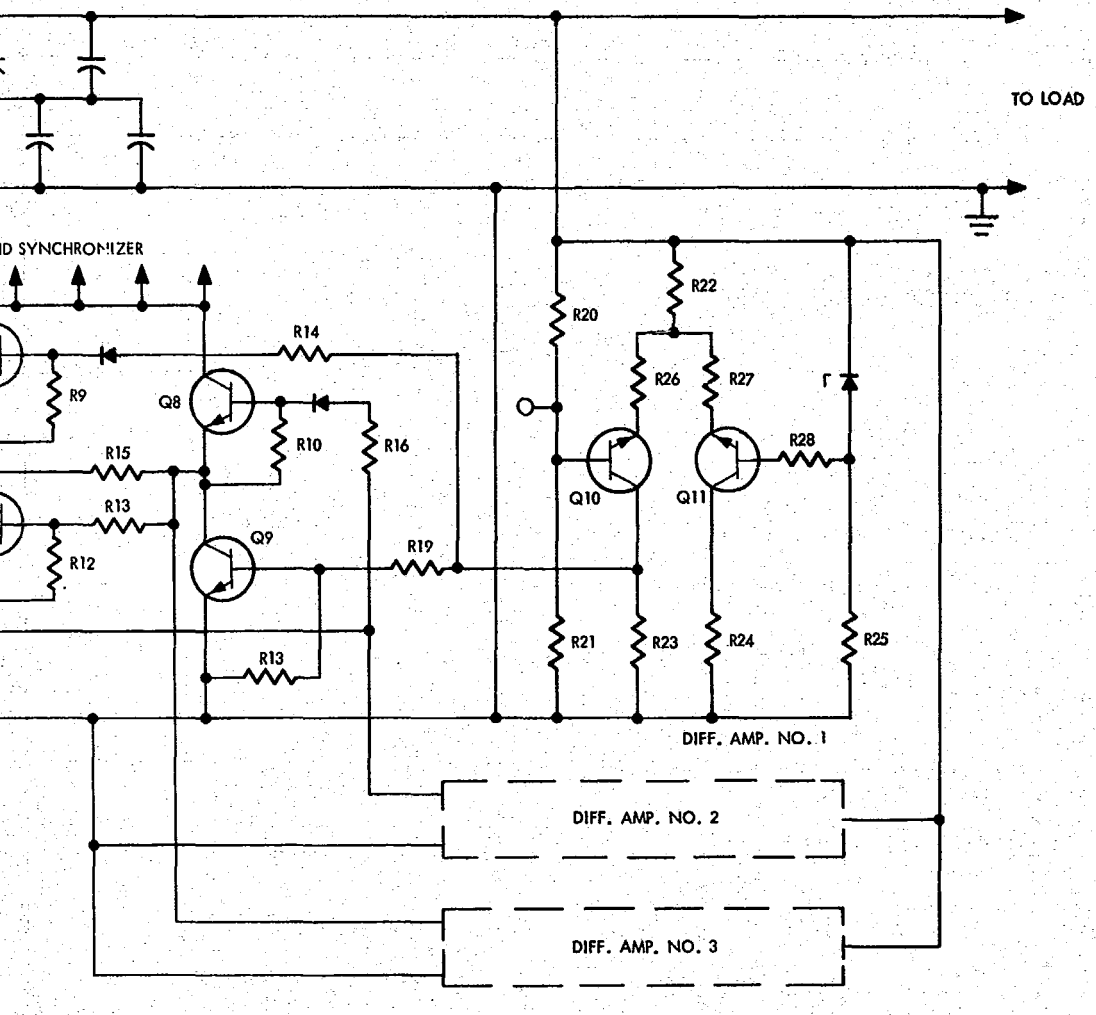


Figure 6-7. Actively Redundant Energy Ladling Buck-Boost Regulator

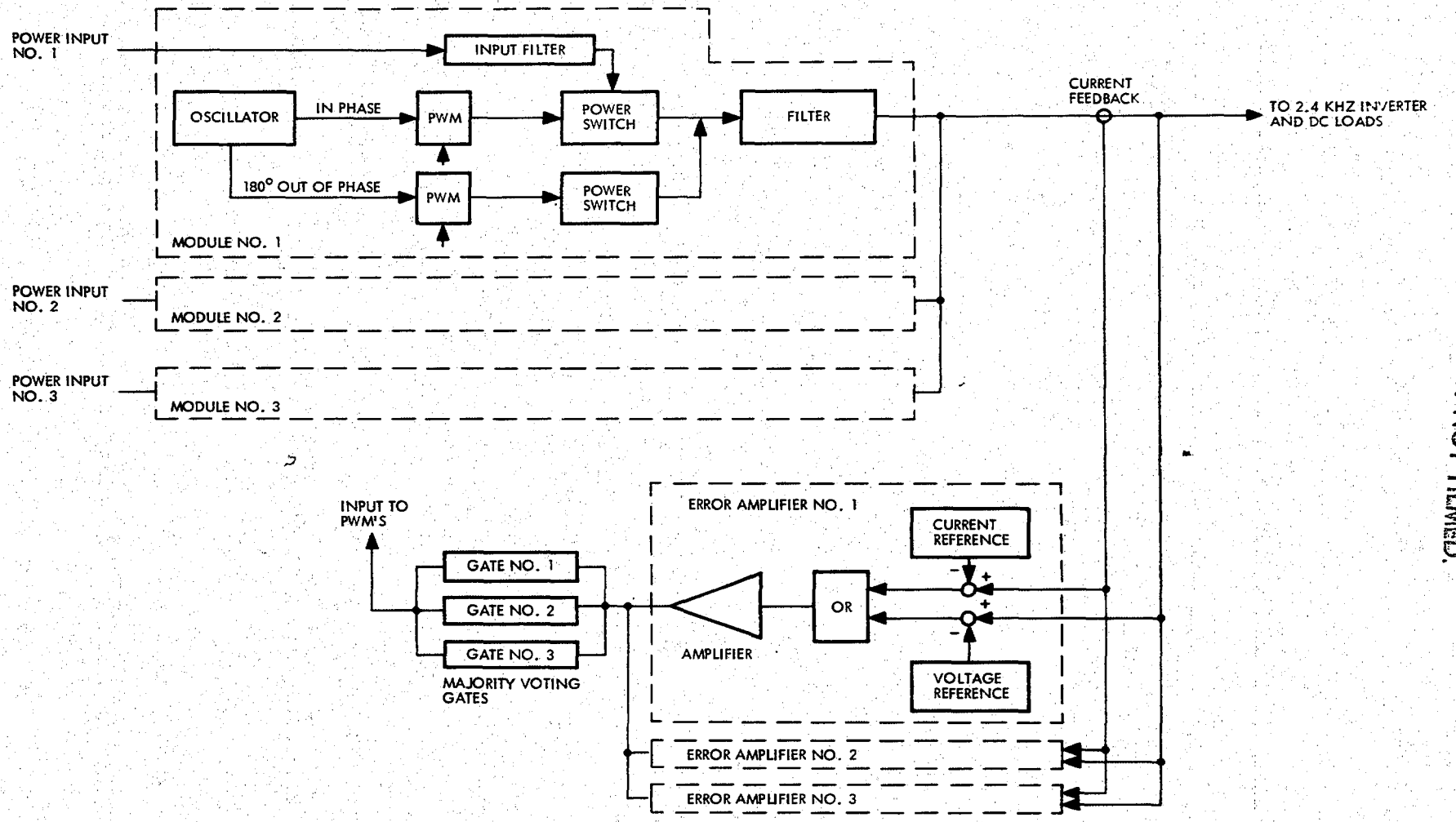


Figure 6-8. Buck-Boost Regulator Block Diagram

6.4.4.2 Weight

An experimental TRW model based on the energy ladling concept has already demonstrated an electrical component weight of less than 4 lb/kW. Preliminary estimates for the finished unit, including packaging, indicates that the overall system weight will be 12 to 16 lb/kW or less.

6.4.4.3 Reliability

The reliability calculations have considered three energy-ladling module-pairs arranged in two pairs of supplementary circuits. The two circuits within one pair operate in such a manner that their switching operations are 180° out of phase. Therefore, if the switching frequency of transistor switch, Q1, is 2.4 kHz, the frequency of the ripple voltage across the output capacitor is 4.8 kHz. The ratings and the design of the three individual power modules assure that adequate performance will be maintained in the event of losing one module.

Furthermore, the error amplifier (the portion shown at the right hand side of Figure 6-7), the overload detector, and the intermittent current disconnect circuit (Figure 6-9) feature a majority voting redundancy.

6.4.4.4 Efficiency

The ensuing analysis deals with the most relevant components in terms of power handling within the buck-boost line voltage regulator. The ground rules have been derived from the calculations and experimental results obtained from a 300-W experimental breadboard developed by TRW.

6.4.4.4.1 Assumptions

a. Number of power modules. For worst-case efficiency, five out of six modules are assumed to be operative.

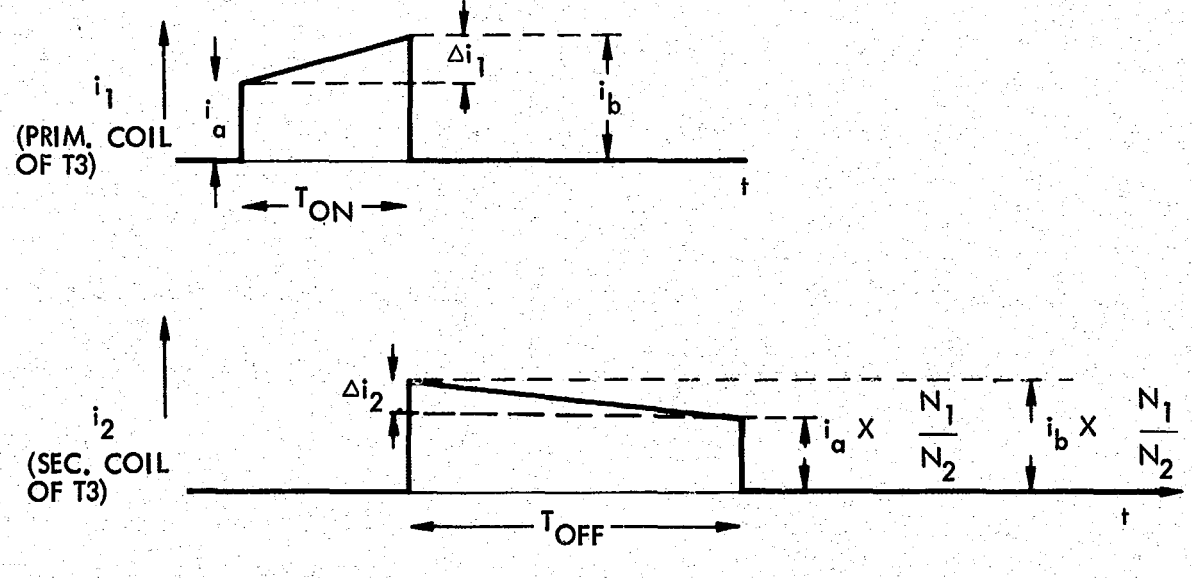


Figure 6-9. Circuit Current Waveforms During One Steady-State Operating Cycle

b. Load handled by each module. Each module is assumed to be capable to handle a 50% overload, or

$$\frac{340}{6} \times 1.5 = 85 \text{ W/module}$$

c. Under normal conditions, each module handles 340/6 = 56.66 W (number of modules = 6)

d. The switching frequency of the semiconductor switch is assumed to be 2.4 kHz.

e. Input voltage e_{in}. The input voltage range is from 25 to 65 V. For the purpose of this analysis, an input voltage of e_{in} = 40 V is utilized.

6.4.4.4.2 Transformer-Inductor Losses

Copper losses

The average input current per module is

$$I_1 = \frac{P_o \cdot T}{M \cdot E_1 \cdot T_{on}} \qquad (6\text{-}1)$$

where

P_o = output power = 340 W

T = switching period = 416 μsec

M = number of power modules = 3

E_1 = 40 Vdc

E_o = 56 Vdc

T_{on} = 208 μsec (this further assumes that N2/N1 = 56/40 = 1.4)

Note: Equation (6-1) assumes unity efficiency as a first approximation. Solving for I_1

$$I_1 = \frac{340 \times 416}{6 \times 40 \times 208} = 2.83 \text{ amps}$$

To evaluate the copper losses, assume a linear rate of current change of

$$\frac{di_1}{dt} = 0.01 \text{ amp/μsec} \qquad (6\text{-}2)$$

Therefore, the waveform of the current flowing in the primary winding of the inductor transformer is as shown in Figure 6-10. In Figure 6-10, the square of rms current is

$$(I_{rms})^2 \text{ primary} = \left(\frac{T_{on}}{3T}\right)\left(I_a^2 + I_b^2 + I_a I_b\right) \qquad (6\text{-}3)$$

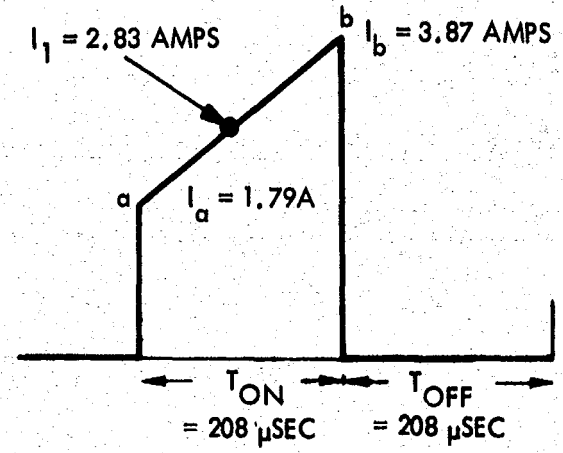


Figure 6-10. Inductor Transformer Waveform

The expression for the square of rms current in the secondary winding is

$$(I_{rms})^2 \text{ secondary} = \left(\frac{T_{off}}{3T}\right)\left(\frac{N_1}{N_2}\right)^2 \left(I_a{}^2 + I_b{}^2 + I_a I_b\right) \qquad (6\text{-}4)$$

Although the winding resistance depends on the wire size and length of conductor used (which in turn is a function of the core dimensions), the present evaluation of copper losses will proceed under the assumption that the equivalent resistance referred to the primary side of the transformer is of the same order of magnitude as that obtained for the experimental breadboard developed by TRW. This assumption is not unrealistic in view of the rather lightweight units built for the breadboard module (i.e., $\leqq$ 2 lb/kW).

Therefore, assume the following winding resistances:

$$R_P = 0.045\,\Omega \qquad (6\text{-}5)$$

$$R_S = 0.045 \times 1.4^2 = 0.088\,\Omega \qquad (6\text{-}6)$$

Thus, the total transformer copper loss P_c is

$$P_c = \frac{208}{3 \times 416}\left(1.79^2 + 3.87^2 + 1.79 \times 3.87\right) \times 0.045$$

$$+ \frac{208}{3 \times 416} \times \left(\frac{1}{1.4}\right)^2 \left(1.79^2 + 3.87^2 + 1.79 \times 3.87\right) \times 0.088$$

$$= \frac{2 \times 208}{3 \times 416}\left(1.79^2 + 3.87^2 + 1.79 \times 3.87\right) \times 0.045$$

$$= 0.377 \text{ watts}$$

Core loss

The loss per cycle is represented by the area enclosed by abcd in Figure 6-11.

$$\text{Area abcd} = \Delta i \times N \times \Delta\phi = \Delta i \times E_1 \times T_{on} \qquad (6\text{-}7)$$

For permalloy powder core operating at 2.4 kHz, the magnetizing force $N_1 \Delta i/\ell$ is about 16 amp-turns/meter (or approximately 0.2 oersteds).

Therefore, assuming a molybdenum permalloy powder core with the following geometry

OD = 2.25 in. = outside diameter

ID = 1.4 in. = inside diameter

h = 0.55 in. = height

ℓ = 5.73 in. = mean length of magnetic path

The width of the hysteresis loop is

$$\Delta i = 16 \times \frac{0.146}{120} = 0.0195 \text{ amps}$$

where 120 primary turns are capable of supporting a 70-V primary voltage.

Core loss per cycle is therefore

$$E_{in}\, T_{on} \times \Delta i = 40 \times 208 \times 10^{-6} \times 0.0195$$

$$= 16.2 \times 10^{-5} \text{ joules}$$

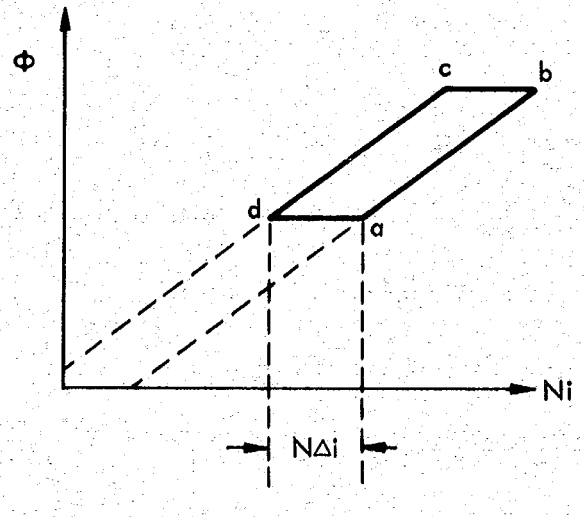


Figure 6-11. BH Loop for Core Losses

Consequently, the total power loss P_i in the iron becomes

$$P_i = 16.2 \times 10^{-5} \times 2.4 \times 10^3$$

$$= 0.38 \text{ W per transformer}$$

where 2.4 kHz is the operating frequency.

Since Δi and $E_1 \times T_{on}$ in Equation (6-7) are independent of the line and load conditions in the buck-boost inductor-transformer, the core loss is essentially fixed.

6.4.4.4.3 Losses of Power Transistor. If it is assumed that the current required to commutate rectifier CR6 (Figure 6-7) is negligible compared to its forward current, it is possible to establish the equations to calculate the transistor losses by referring to the current and voltage waveforms shown in Figure 6-12.

The average energy loss for the transistor is (neglecting losses due to leakage current):

$$P_{TR} \times T = \frac{I_a}{2} V_T t_r + \left(V_T - V_{SAT}\right) t_v + V_{SAT}\left(t_c - t_r - t_v\right)$$

$$+ \frac{I_b}{2} V_{SAT}\left(t_c - t_r - t_v\right) + \left(V_T - V_{SAT}\right) t_s + V_T t_f \qquad (6\text{-}8)$$

$$+ I_{DR} V_{eb} t_c$$

where

T = period of switching frequency = 416 μsec

I_a = 1.79 A

I_b = 3.87 A

I_{DR} = 0.387 A (assuming forced $\beta = 10$)

V_{eb} = amplitude of emitter-to-base voltage

= 1.2 V

V_{SAT} = 0.7 V

V_T = 80 V

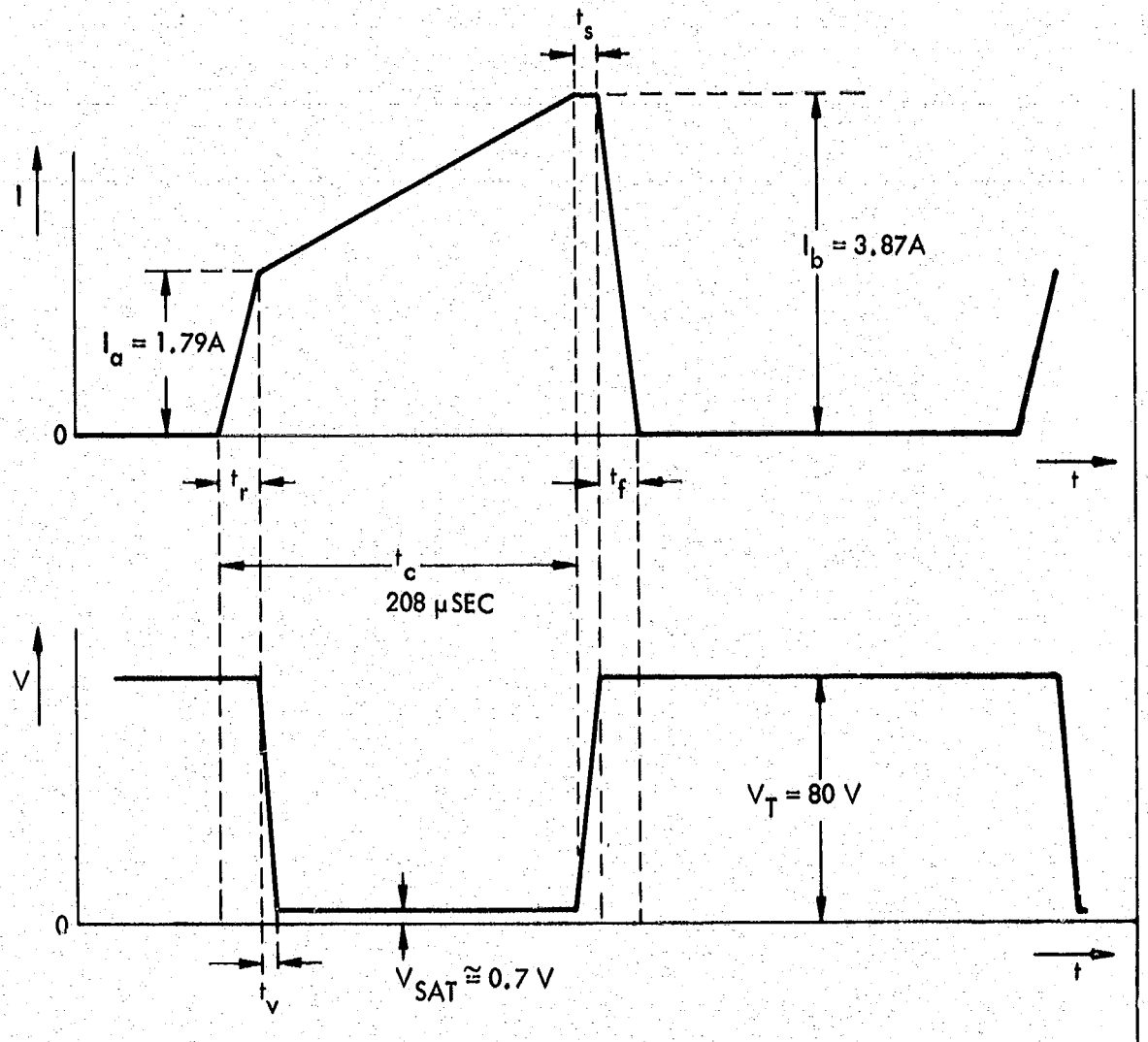
t_r = 1 μsec (typical)

t_v = 0.5 μsec, approximately

t_c = 208 μsec

t_s = 0.5 μsec (typical)

t_f = 1 μsec (typical)



ASSUMPTIONS

$t_r = 1$ μSEC
$t_f = 1$ μSEC
$t_s = 0.5$ μSEC
$t_v = 0.5$ μSEC

Figure 6-12. Power Transistor Current and Voltage Waveforms

substituting numerical values:

$$P_{TR} \times T = \frac{1.79}{2} (80 \times 1 + 79.3 \times 0.5 + 0.7 \times 206.5)$$

$$+ \frac{3.87}{2} (0.7 \times 206.5 + 79.3 \times 0.5 + 80 \times 1)$$

$$+ 0.387 \times 1.2 \times 208$$

$$= 0.895 (264.20) + 1.935 (264.20) + 96.6$$

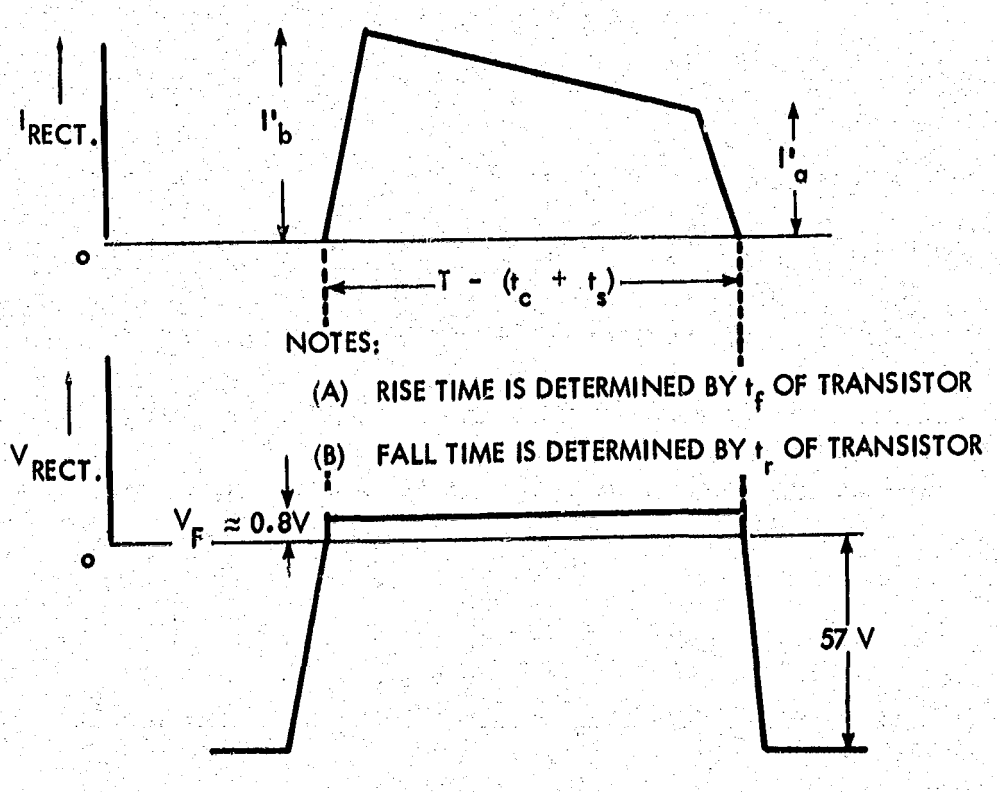
$$= 747.5 + 96.6$$

$$= 844.1 \text{ W-}\mu\text{sec}$$

therefore:

$$P_{TR} = \frac{844.1}{416} = 2.03 \text{ W}$$

6.4.4.4.4 Losses of Free-Wheeling Rectifier (CR6), Assuming Negligible Commutating Current



where

$$I_a' = I_a \times \frac{N_1}{N_2} \tag{6-9}$$

$$I_b' = I_b \times \frac{N_1}{N_2} \tag{6-10}$$

substituting

$$I_a' = 1.28 \text{ A}$$

$$I_b' = 2.77 \text{ A}$$

$$P_{CA6} \times T = \frac{1}{2} V_f \left(I_b' \times t_f + I_a' \times t_r\right) + V_f \left[I_a' + \frac{1}{2}\left(I_b' - I_a'\right)\right] \left[T - \left(t_c + t_s + t_r + t_f\right)\right] \tag{6-11}$$

$$P_{CR6} \times T = \frac{1}{2} V_f \left(I_b' t_f + I_a' t_r\right) + \left(I_a' + I_b'\right) \left[T - \left(t_c + t_s + t_r + t_f\right)\right]$$

making substitutions

$$P_{CR6} \times T = 0.4 (2.77 \times 1 + 1.28 \times 1) + 405 (416 - 210.5)$$

$$= 0.4 (4.05 + 832)$$

$$= 335 \text{ W-}\mu\text{sec}$$

$$P_{CR6} = \frac{335}{416} = 0.805 \text{ W}$$

6.4.4.4.5 Losses of Output Filter Inductor, L2. To compute the loss of L2, it is first necessary to evaluate C4 and the output filter (L2 and output capacitor bank).

$$C_4 = \frac{I_b' - I_a'}{\frac{V_{C_4}}{\Delta t}} \tag{6-12}$$

Where V_{C_4} is the amplitude of the ac voltage across Cμ (this can be near 10 V, for maximum effectiveness in the combination of Cμ and the output filter), Δt = 208 μsec for the duty cycle being assumed. Solving for C_4 in Equation (6-11),

$$C_4 = 31 \ \mu\text{F}$$

A standard size is 33 μF 100 V.

Attenuating now the voltage ripple by a factor of 30 and using Co = 300 μF for the output capacitor bank, inductor L2 can be calculated as follows:

$$L_2 = \frac{(ATT + 1) \times n}{(2\pi f_1)^2 C_o} \qquad (6\text{-}13)$$

where

$ATT = 30 \equiv \frac{X_L}{X_C} - 1 \equiv$ attenuation

$n = 6$ = no. of modules

$f_1 = 2.4$ kHz x 2

$C_o = 300$

$L2 \approx 0.75$ mhy

A suitable powder core is Magnetics, Inc., 55894 with 100 turns of Awg No. 20 wire size.

$$R_{DC} = \frac{W_1 \times lwm \times N}{1000 \times 12} \qquad (6\text{-}14)$$

where

W_1 = Res./1000 ft of Awg No. 20 wire

= 10.3Ω at 25°C

lwm = mean turn length = 1.25 in.

substituting values

$$R_{DC} = 0.108\Omega$$

and the copper losses are

$$P_{cu_{L2}} = R_{DC} \times I_{L2}^2$$

$$= 0.13 \text{ W}$$

Evaluation of iron losses:

$$\Delta i = \frac{16 \times 0.065}{100} = 0.0104 \text{ amp}$$

where

16 = magnetizing force, amp-turns/meter

0.065 = length of magnetic path, meter

100 = turns

Therefore, the iron losses are

$$P_{Fe_{L2}} = V \times T_{on} \times \Delta i \times F \qquad (6\text{-}15)$$

$$= 0.052 \text{ W}$$

Total losses of L2 = 0.182 W

L1 has approximately the same losses as L2. Therefore the total losses are as follows:

Component	Losses (W)
T3	0.757
L1	0.182
Power transistor	2.030
CR_4	0.805
L2	0.182
Miscellaneous	1.000
	4.956

$$\text{Efficiency/module} = \frac{56.6}{56.66 + 4.956} \times 100\% = 92\%$$

6.5 2.4 KHZ INVERTER

6.5.1 Description of Functions

The following functions describe the 2.4-kHz inverter.

a. Convert the regulated 50 Vdc from the boost regulator to 50 Vrms at 2.4 kHz. This power is distributed and utilized as prime power for the spacecraft.

b. Operate at the frequency generated by a crystal oscillator and, in the absence of this frequency source, have the capability to free run at a prescribed frequency.

c. Accept either resistive loads or reactive loads which exhibit a lagging power factor.

d. Work in conjunction with an undervoltage failure detector and a frequency failure detector to continuously monitor the quality of its voltage and frequency.

e. Include standby redundancy for improved reliability.

6.5.2 Analysis of Existing Mariner Design

6.5.2.1 Reactive Current Bypass Rectifiers

The effect of these rectifiers is depicted in Figure 6-13. Diodes must be of the fast recovery type. Although these type of diodes have more junction capacitance than normal diodes, they do have also faster forward recovery time due to the bonded construction.

6.5.2.2 Independent Frequency Failure Detector

Independent frequency failure detector can be realized from two viewpoints:

a. As a matter of reliability, a substitution of a power stage when a power stage component fails and a substitution of an oscillator when the oscillator circuit fails appears to be a more effective procedure than the substitution of both when either one has failed

b. From the design point of view, the configuration of a single failure detector that should encompass sensitivity to both voltage and frequency failures presents two weaknesses: circuit complexity and, particularly, great difficulty to achieve redundancy because of the incompatibility of parameters and failure modes being detected. A more reliable way to detect failures in the bridge oscillator is to sense directly the performance of the crystal oscillator in terms of its distinct failure modes.

   The expected failure modes of the crystal oscillator are as follows:

   1. Crystal opens. Cessation of operation can readily be detected and corrected by the automatic insertion of the standby crystal oscillator and countdown stage (see Figure 6-14).

   2. Collapse of amplitude and deterioration of the output signal waveshape (with fundamental frequency remaining unchanged) due to a failure of the electronics directly associated with crystal (capacitors, transistors, and resistors). This type of failure will cause a decrease of the dc signal obtained from the rectification and filtering of the ac squarewave at the output of the bridge oscillator. This dc signal is fed to an accurate voltage comparator (see the three differential amplifiers connected in a majority voting configuration (Figure 6-14) that has the further advantage of being failsafe. Such a signal, when decreasing below a well-chosen threshold level, will enable the standby oscillator and associated countdown binary circuit, and simultaneously disable the output of the malfunctioning oscillator. Furthermore, the testability and resetability (or capability of the circuit to be reset) of the oscillator are easy to accomplish, and the binary countdown circuitry can be made failsafe.

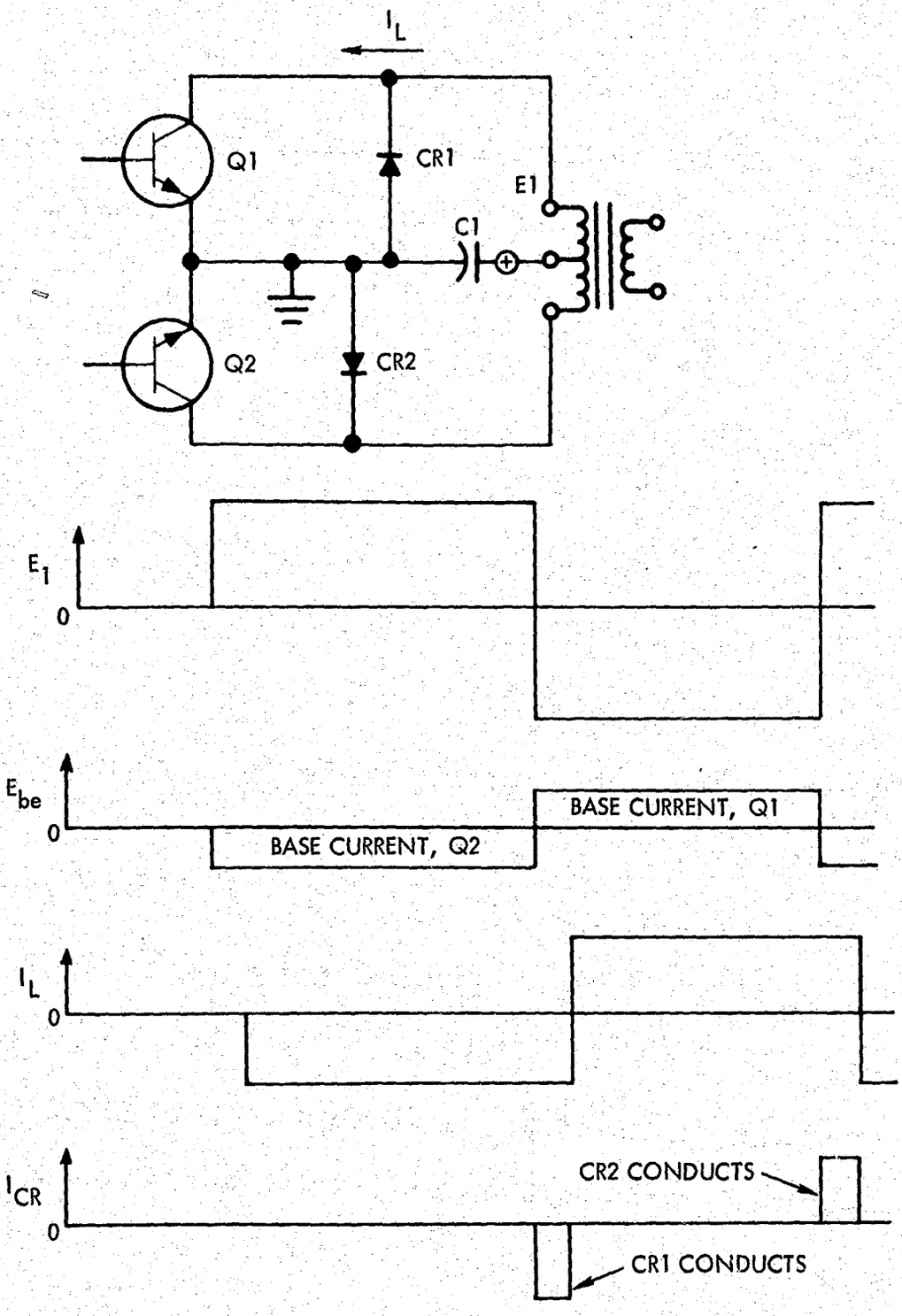


Figure 6-13. Reactive Current Bypass Mechanism

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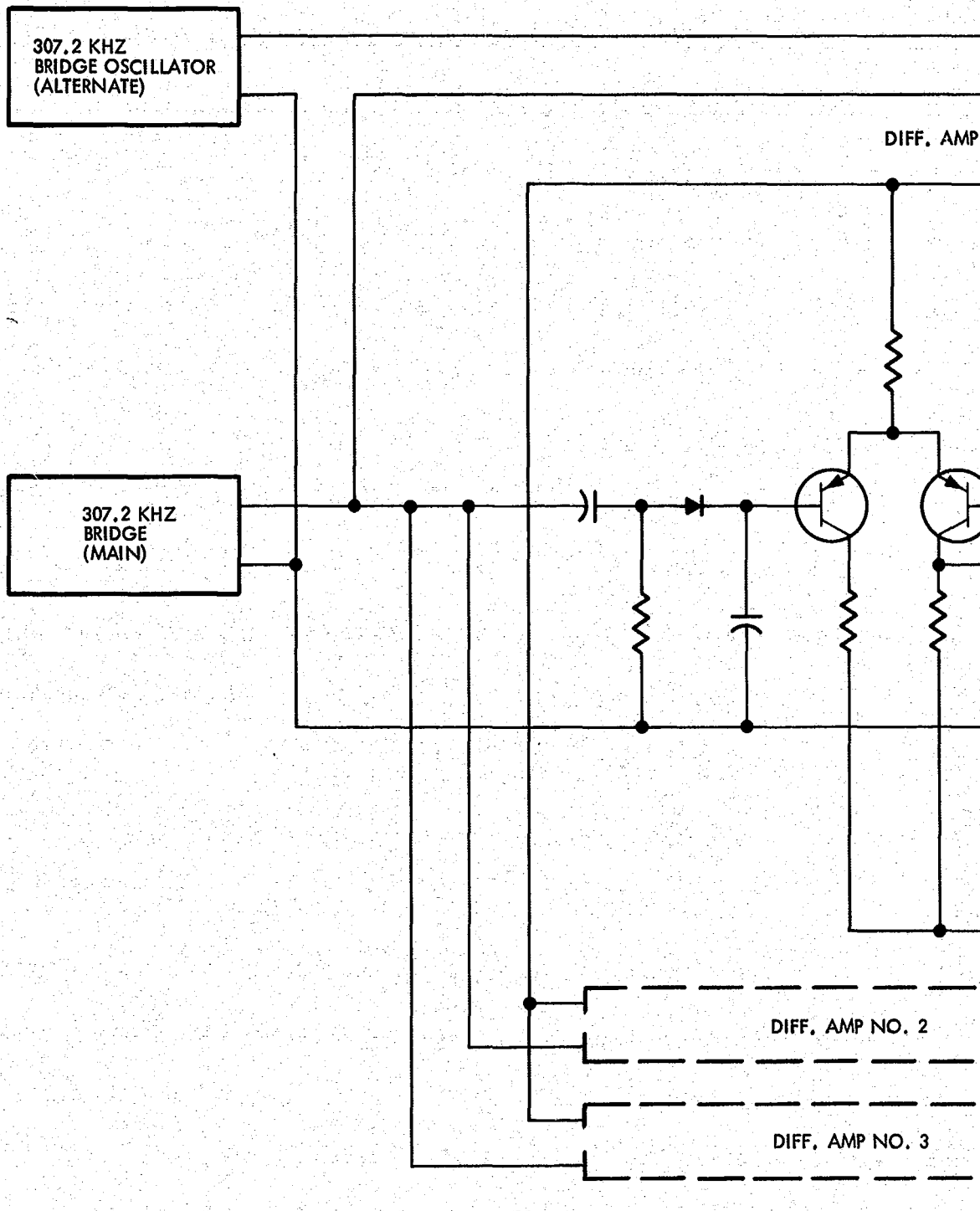

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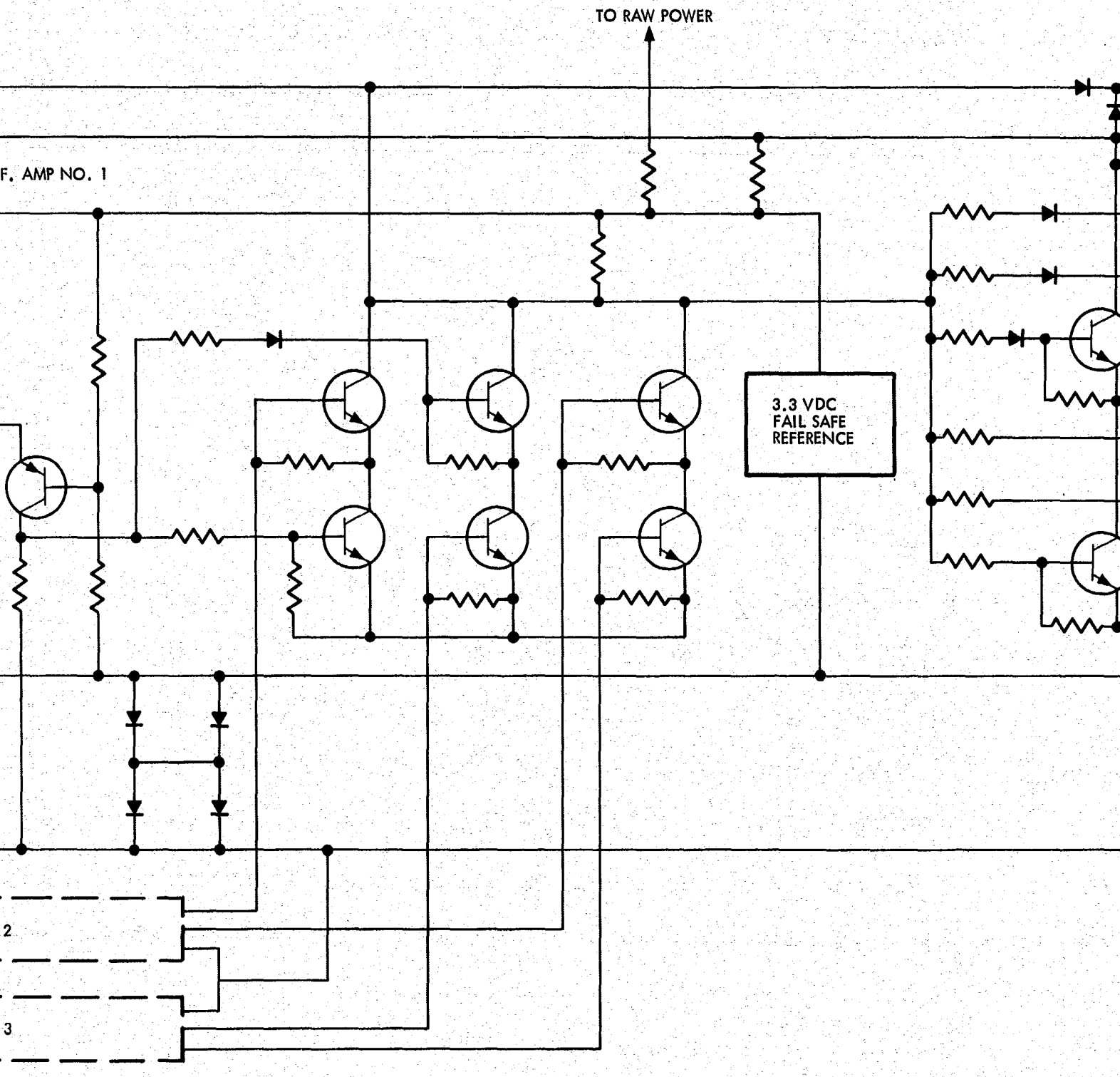

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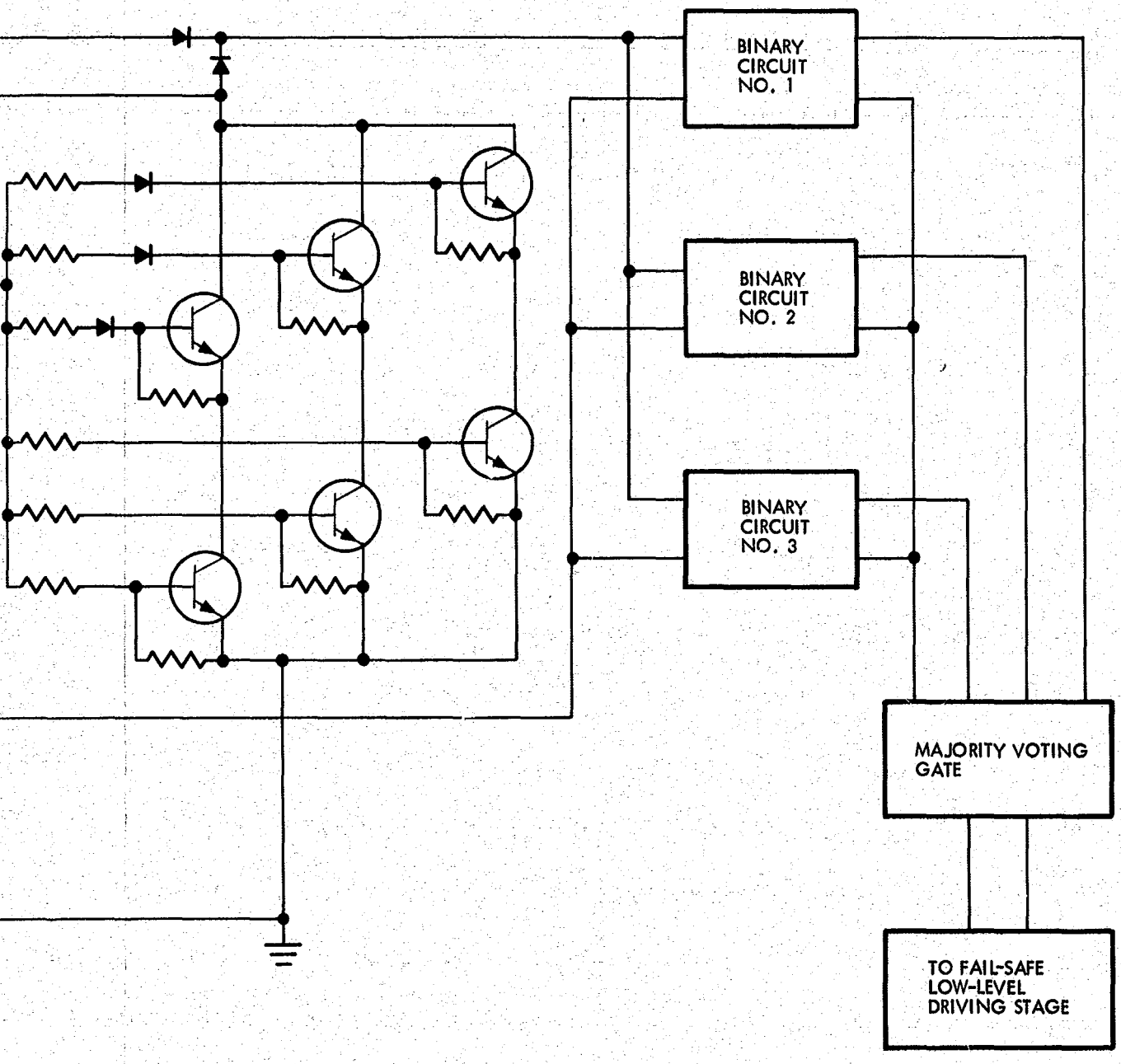

Figure 6-14. Fail-Safe Failure Detector and Solid-State Switching. Crystal Oscillator Including Majority Voting Binary Counter

The result of this convenient and redundant configuration is a compact (could be made of integrated circuits in its entirety) and failsafe circuit without the use of any relay. See:

- Figure 6-14. Failsafe Failure Detector and Solid-State Switching.
- Figure 6-15. Block Diagram of 2.4 kHz Inverter.
- Figure 6-16. Failsafe Low-Level Driver Stage.

c. Although the Mariner approach incorporates a technique that minimizes the on-state overlap, it causes an undesirable delay during the off-switching. As a result, the delaying of the on-stage must account for both the carrier storage plus the off-switching delay caused by such a technique. This is a small loss in the utilization of the power transistors by approximately 90 nsec off switching delay = $C_1 \times (R_{\text{sec of T3}} + R_{CR6})$. A recommended technique is shown in Paragraph 6.9.3.1a.

6.5.3 Approaches Considered

6.5.3.1 Preliminary Screening

a. Bridge type

b. Center-tap type (JPL approach)

c. Center-tap type including refinements (the refinements referred to are those delineated in Paragraph 6.5.2)

The relative merits of these circuit approaches are summarized in Table 6-12.

6.6 1ø, 3ø INVERTERS

6.6.1 Description of Functions

The following functions describe the 1ø and 3ø inverters.

a. Convert the regulated dc voltage from the output of the line-voltage regulator into single and 3ø 400-Hz square-wave power outputs that are synchronous with the 2.4 kHz squarewave.

b. In the case of the 3ø inverter, provide an output voltage waveform with a supressed third harmonic in order to prevent the loads from dissipating it.

c. Accept either resistive loads or reactive loads which exhibit a lagging power factor.

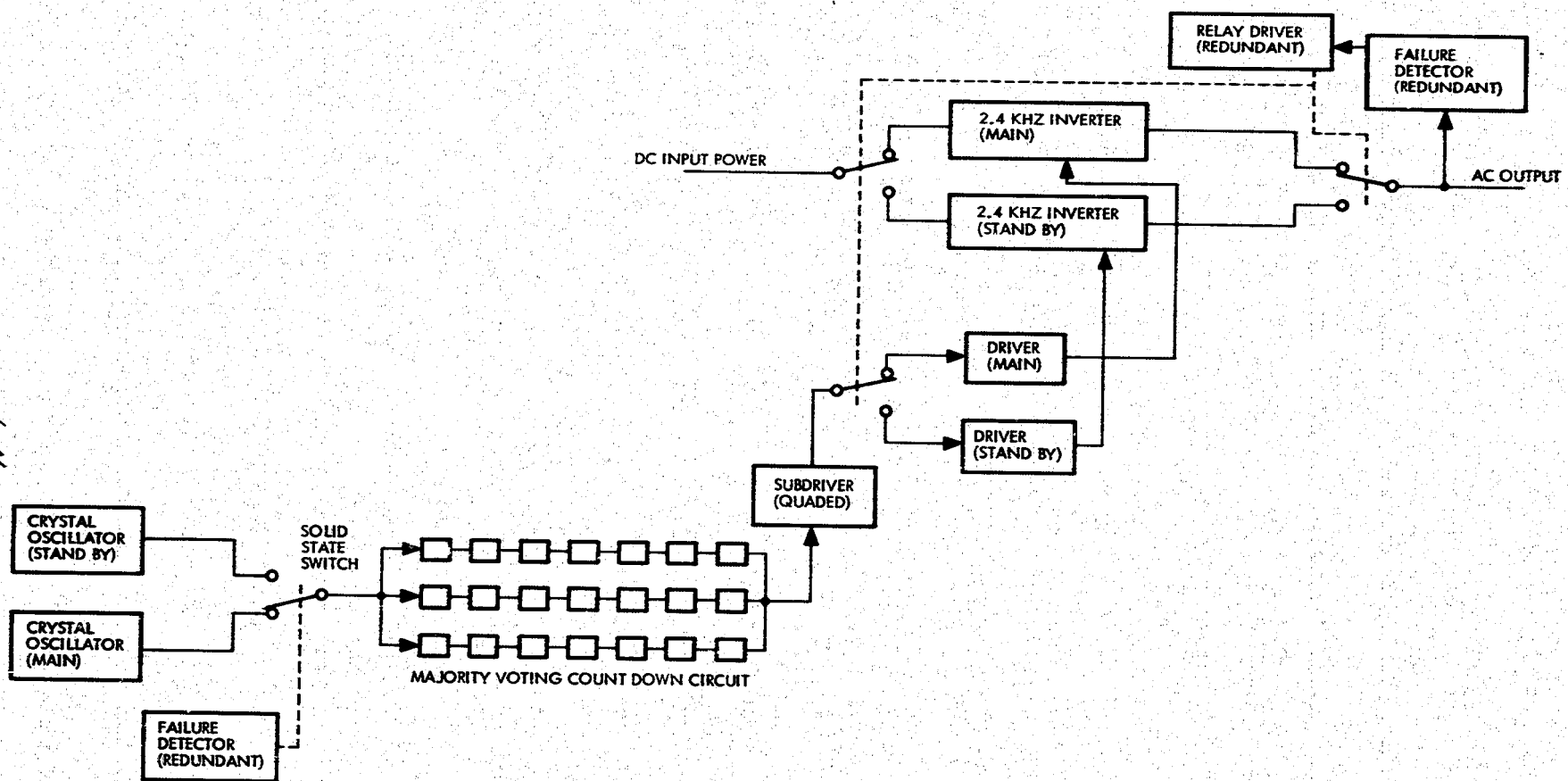

Figure 6-15. 2.4 kHz Inverter Block Diagram

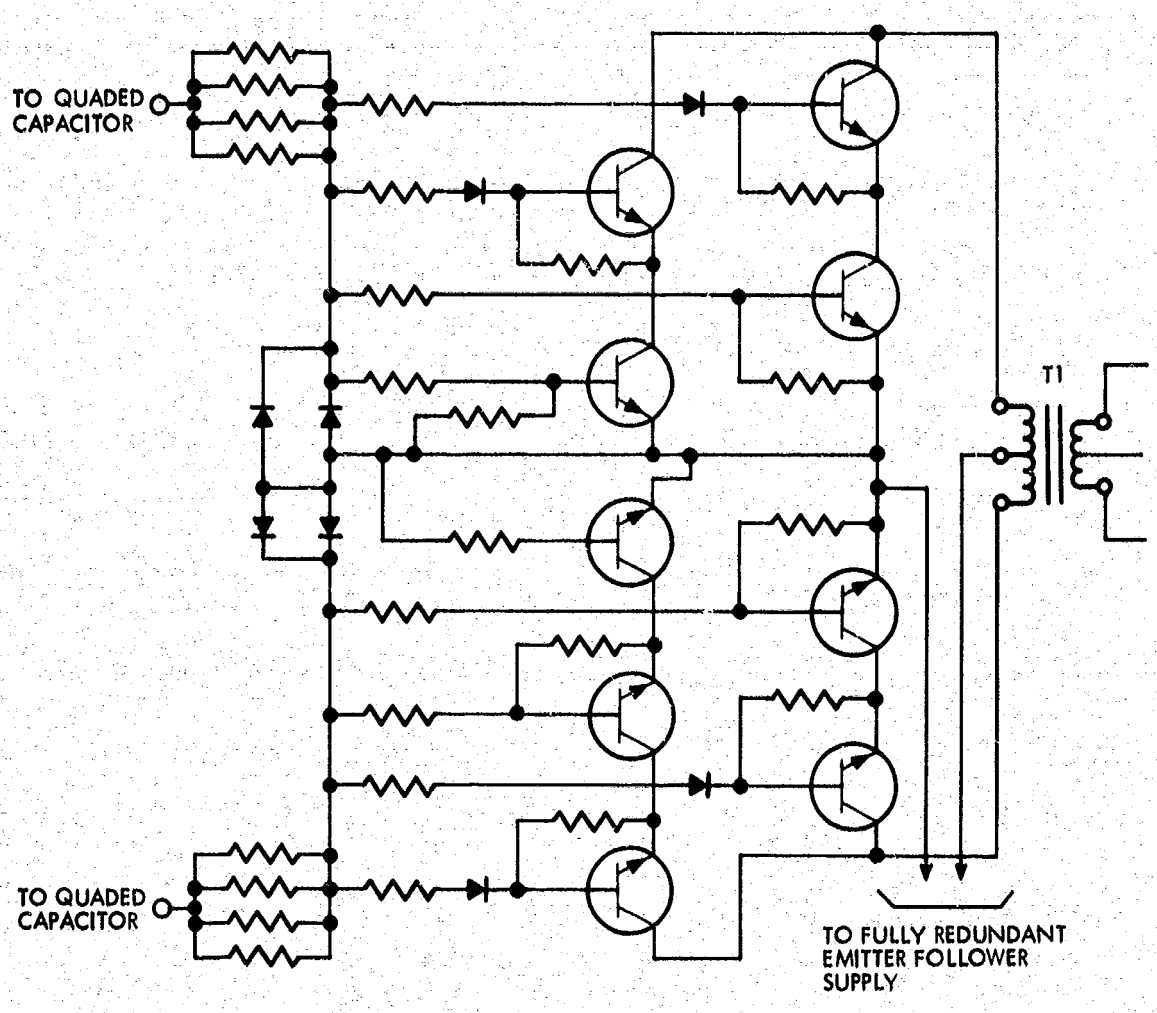

Figure 6-16. Fail-Safe Low Level Driver Stage

Table 6-12. Relative Merits of Individual Approaches

Concept	Approach		
	(a) Bridge Type	(b) Center-Tap (JPL)	(c) Center-Tap (improved)
Power transistor voltage rating: L = low, H = high	L	H	H
Weight of power transformer	80%	100%	100%
Transistor losses: L = low, M = medium, H = high	H	M	L
Reliability: H = higher, M = medium	M	M	H
Simplicity and dependability of failure detectors: H = high, M = medium	M	M	H

Note: It has been assumed that the bridge type has the same failure detector, base-driving technique, and lack of reactive current rectifiers as the Mariner approach.

6.6.2 Analysis of Existing Mariner Design

6.6.2.1 Identify Areas for Improvement

a. Need for reactive current bypass rectifiers. Circuit recommendations presented in Paragraph 6.5.2 are also applicable in this case.

b. A partial redundancy could increase considerably the dependability of these inverters. This partial redundancy would include the following:

1. A failsafe bias and exciter circuit; see Figure 6-17 (bias supply and 2.4-kHz excitation for synchronizer, fully redundant).

2. A majority voting synchronizer; see Figure 6-18.

6.6.3 Approaches Considered

6.6.3.1 Preliminary Screening

a. For the single phase inverter

1. Bridge type, nonredundant

2. Center-tap, nonredundant

3. Center-tap, partially redundant

b. For the 3ϕ inverter

1. Nonredundant type

2. Partially redundant type

The relative merits of these approaches are summarized in Table 6-13.

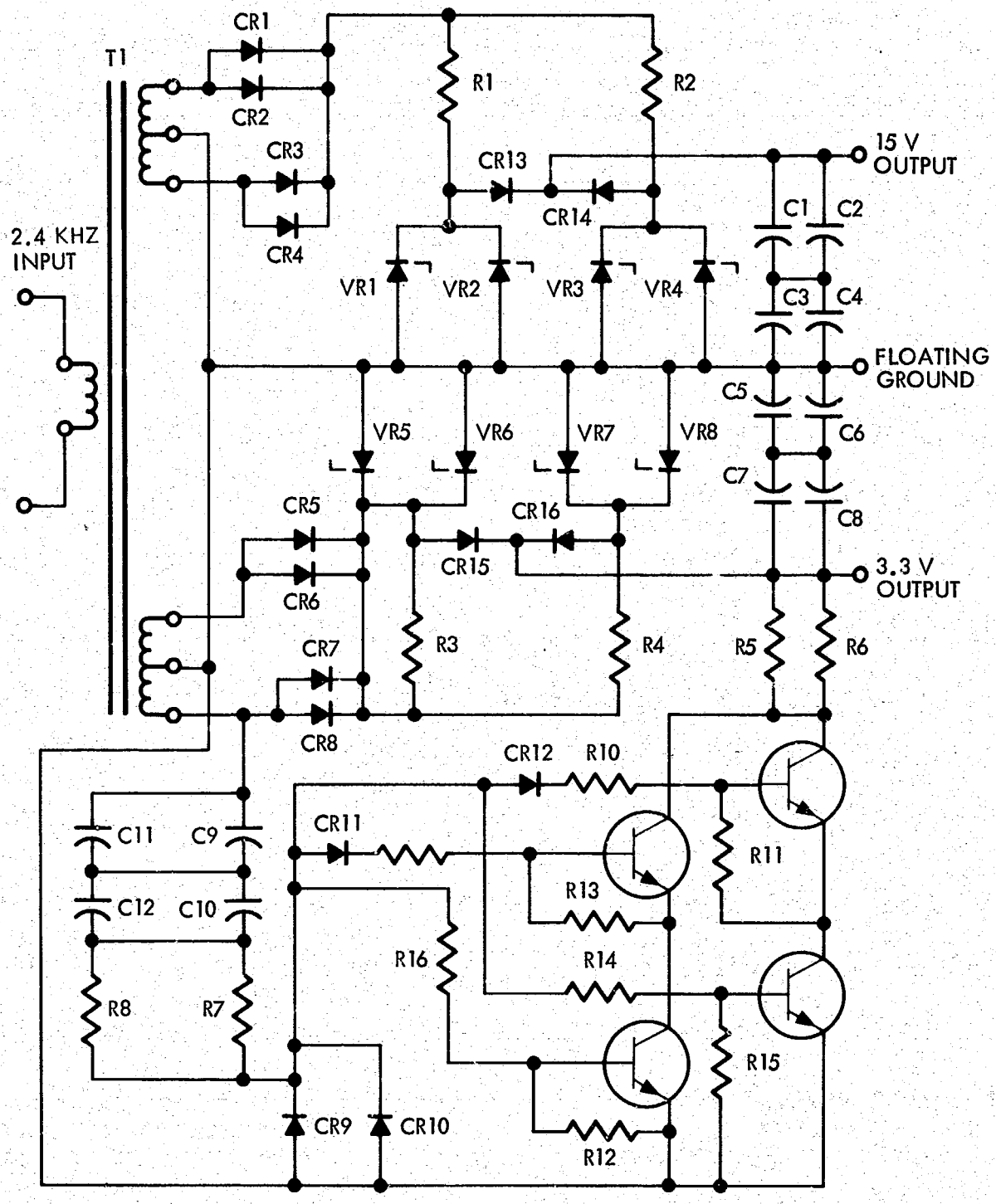

Figure 6-17. Bias Supply and 2.4 kHz Excitation for Synchronizer (Fully Redundant)

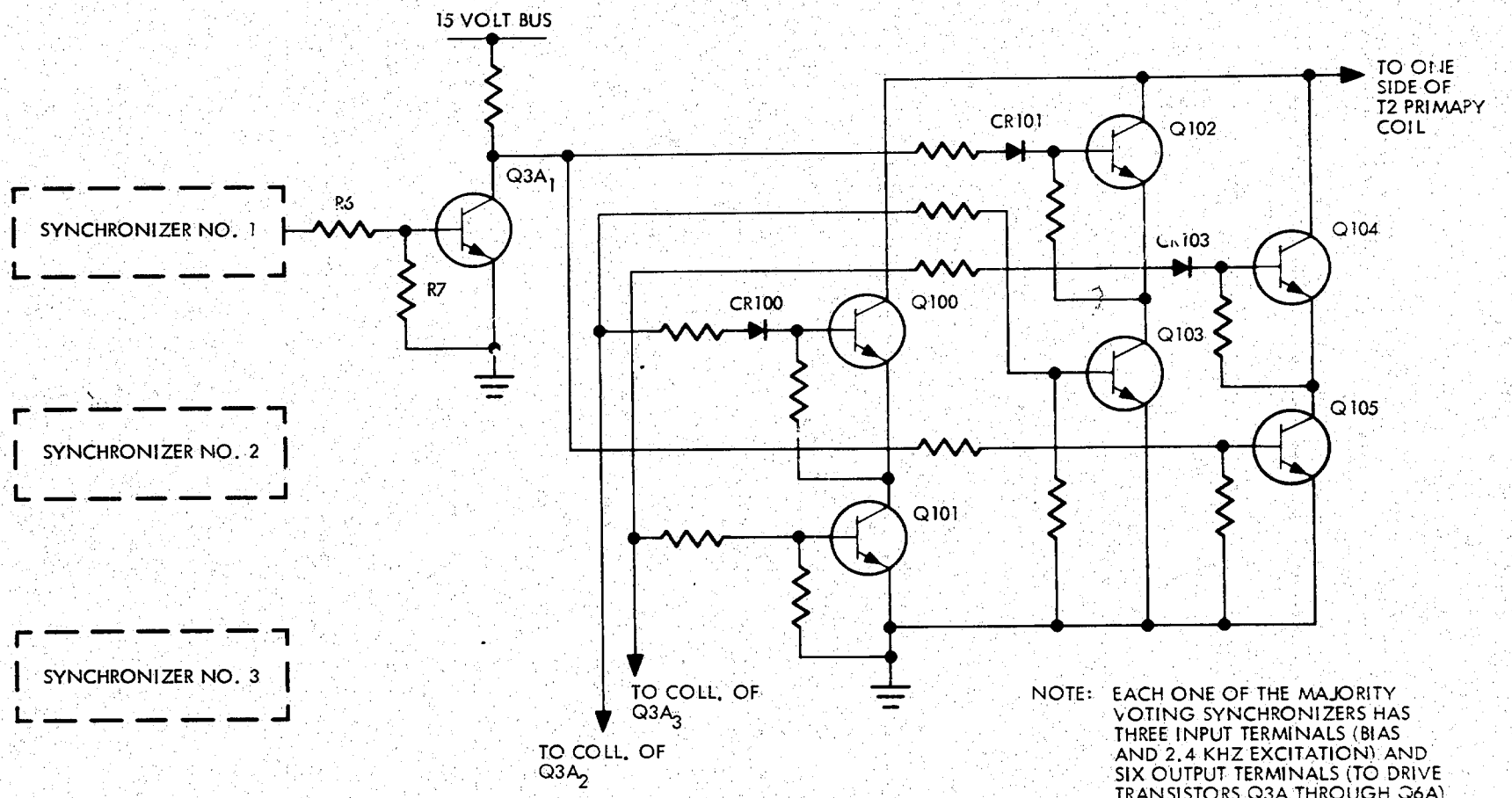

Figure 6-18. Majority Voting Synchronizer

Table 6-13. Comparison of 1ϕ and 3ϕ Inverter Design Approaches

Concept	1 Phase			3 Phase	
	1	2	3	1	2
Voltage ratings for power transistors: L = low, H = high	L	H	H	L	L
Size and weight of output transformer	80%	100%	100%	100%	100%
On-state transistor losses: L = low, H = High	H	L	L	L	L
Reliability: M = medium, H = high	M	M	H	M	H
Need of failure detectors	No	No	No	No	No

1-Phase

1. Bridge type, nonredundant
2. Center-tap, nonredundant
3. Center-tap, partially redundant

3-Phase

1. Nonredundant type
2. Partially redundant type

6.7 POWER DISTRIBUTION

6.7.1 Description of Functions

The primary function is the basic distribution of power, in response to ground-initiated or on-board command signals. This power falls into two basic categories characteristic of this system:

- Regulated dc
- Regulated ac

Typical functions include the command operation of battery charging, momentary boosting, ACS control, heater control, 2.4 kHz inverter selection, experiment control and others. To conserve power, it is required that a commanded state be attained during the command duration and that this state be maintained with minimum power consumption until another command is received. To conserve on the number of commands, some functions must toggle alternately from one state to the other on successive commands received on a single input line. Basically, two types of commands are used:

a. 100-msec pulses from isolated switch transistors.

b. Relay contact closures.

Both types are powered from a single 30 Vdc supply distributed to the isolated switches, relays, and relay drivers. Additionally, the relays and related driver circuitry must exhibit immunity to noise and stray signals, so that spurious or random undesired operation does not occur.

Because of the critical, in-line nature of the power distribution system to mission success, it is highly desirable that a reliable method be implemented, consistent with interfacing functions and circuits. Additionally, information is provided to telemetry about the command function state.

6.7.2 Requirements

Reference Table 3-1, Preliminary Specification, Power Distribution and Table 5-4, Command Designation.

6.7.3 Analysis of Existing Mariner Design

6.7.3.1 Areas of Improvement

Since the present circuit includes no part redundancy, failure of almost any single part results in the inability to command the function. Circuit redundancy could be implemented to allow normal operation to continue in the event of any single pa :t failure, and in selected cases multiple part failures.

When a function responds to more than one command, these signals are combined by diode-resistor OR gates. These gates have the property that the output signal amplitude corresponds to the largest of the input signal amplitudes. Therefore, if one of several command signals failed in the ON condition, the related relay driver would be continuously energized, preventing any further command response of that function. Capacitive coupling of parallel command signals could prevent this particular failure mode and subsequent loss of command control.

Since the 30-Vdc supply is in line to all commands and relay drivers, the necessity for reliable, fail-safe design is apparent. The present MM '69 circuit

protects against some part failures but not against all; i. e., an open zener diode causes the output voltage to increase toward +56 Vdc, limited only by voltage divider action of the zener bias resistor and the load resistance. Additional circuit redundancy could be implemented to allow this critical circuit to provide continued in-specification performance for all single and selected multiple part failures. Alternately, the supply could be eliminated if the related circuits were designed to operate directly from the regulated dc bus. Since this supply provides power to circuits in several boxes, it is susceptible to cable shorts to ground or other potentials. Incorporation of resistive decoupling to limit loading by grounds, and diode decoupling to protect against connections to higher potentials could eliminate this problem.

6.7.4 Approaches Considered

The basic circuit configurations considered fall into four categories:

- Nonredundant — single part circuits.
- Fail safe — Circuits employing series or parallel redundancy where the predominant part failure mode is considered so that the circuit failure is biased toward a preferred failure mode when one exists.
- Quad — Substitution of four parts for one in either a series or bar-quad connection, enabling operation to continue for any single and some multiple part failures.
- Majority voting — Logic combination of the outputs of three or more circuits performing the same function, whereby the overall output reflects the output of the majority of the circuits.

Since resistors are generally considered to fail in the open condition only, this allows parallel connection instead of quad connection in quad circuits. As a general rule, more relay contact sets (poles) are required in redundant circuits than are required in the single part circuit, i.e., (1) to quad a single-pole, double-throw relay (SPDT) requires four, double-pole, double-throw (DPDT) relays (2) to majority vote a SPDT requires three DPDT relays. For the quad circuit, the number of relays increased by four and the contact sets by eight. For the majority voting circuit, the number of relays increased by three and the contact sets by six. For the case where a four-pole, double-throw relay is completely utilized, four eight-pole, double-throw relays would be required for a quad connection (or eight four-pole double-throw relays). However, this is a maximum indicating the weight and size trend when employing component redundancy for relays. When contact stress and operational life are well within the relay capability, the contacts are assumed highly reliable and the coil is assumed as the primary cause of failure.

Since two-coil, magnetic-latch relays can be operated to both states by reversing the voltage polarity on either coil, it follows that improved reliability can be achieved by additional driver complexity without increasing the number of relays. Table 6-14 compares the total parts of different circuit configurations vs. the basic Mariner relay driver.

Table 6-14. Part Count and Failure Mode Comparison

Type	Total Parts	Failure Mode Survival*
Mariner '69 (Figure 6-19)	20	Worst: Almost all part failures disable the circuit.
Quad (Figure 6-20)	70	Best: Continued operation after all single and many multiple part failures.
Fail-Safe (Figure 6-21)	41	Fair: Predominant failure occurs in a preferred mode. Can operate normally for some part failures.
Majority Voting (Figure 6-22)	92	Best: Continued operation after all single and many multiple part failures.
Bridge (Figure 6-23)	66	Very Good: Continued operation after all single and many multiple part failures. Relay contacts are not redundant.
*Exclusive of relays which were discussed previously		

6.7.5 Summary

The selected circuit (Figure 6-24) depicts a bridge driver with ac signal coupling and improves the problems discussed in Paragraph 6.7.3.1. The block diagram of the selected relay driver is shown in Figure 6-25.

- AC coupling allows normal operation to continue after one or more parallel input commands fail in the ON condition.
- The parts required for toggle operation are in line only for the toggle command, increasing the reliability for parallel commands.
- The 30-Vdc supply is
  1) Eliminated by design for operation directly from the regulated dc
  2) Improved through additional redundancy and discoupling to survive all single part failures and cable faults (if other constraints preclude (1) above).

The advantages and disadvantages are summarized in Table 6-15.

6.7.5.1 Description of Selected Relay Driver Circuit (Figure 6-24)

- Relay Driver. Each relay driver consists of two pairs of complementary transistors connected in a bridge fashion to provide current to the relay coil in a bidirectional manner, i.e., the relay will close or set (current entering dot) when transistors Q8 and Q9 are turned on for 10 msec. Accordingly, the relay will open or reject when transistors Q7 and Q10 are turned on for an equal period of time.

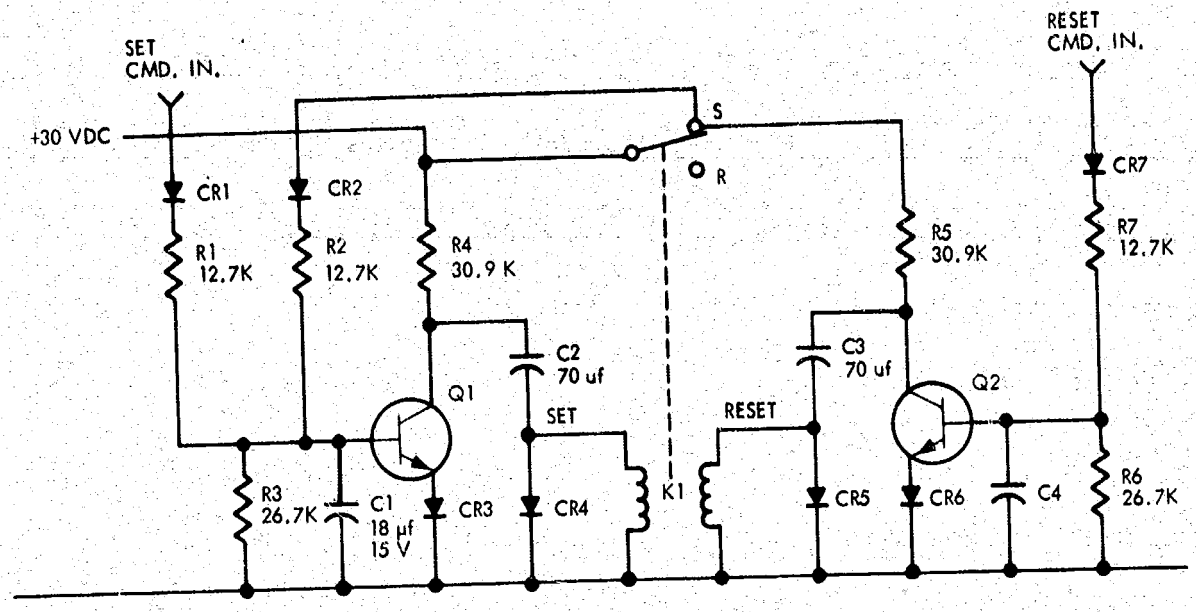

Figure 6-19. Mariner Relay Driver

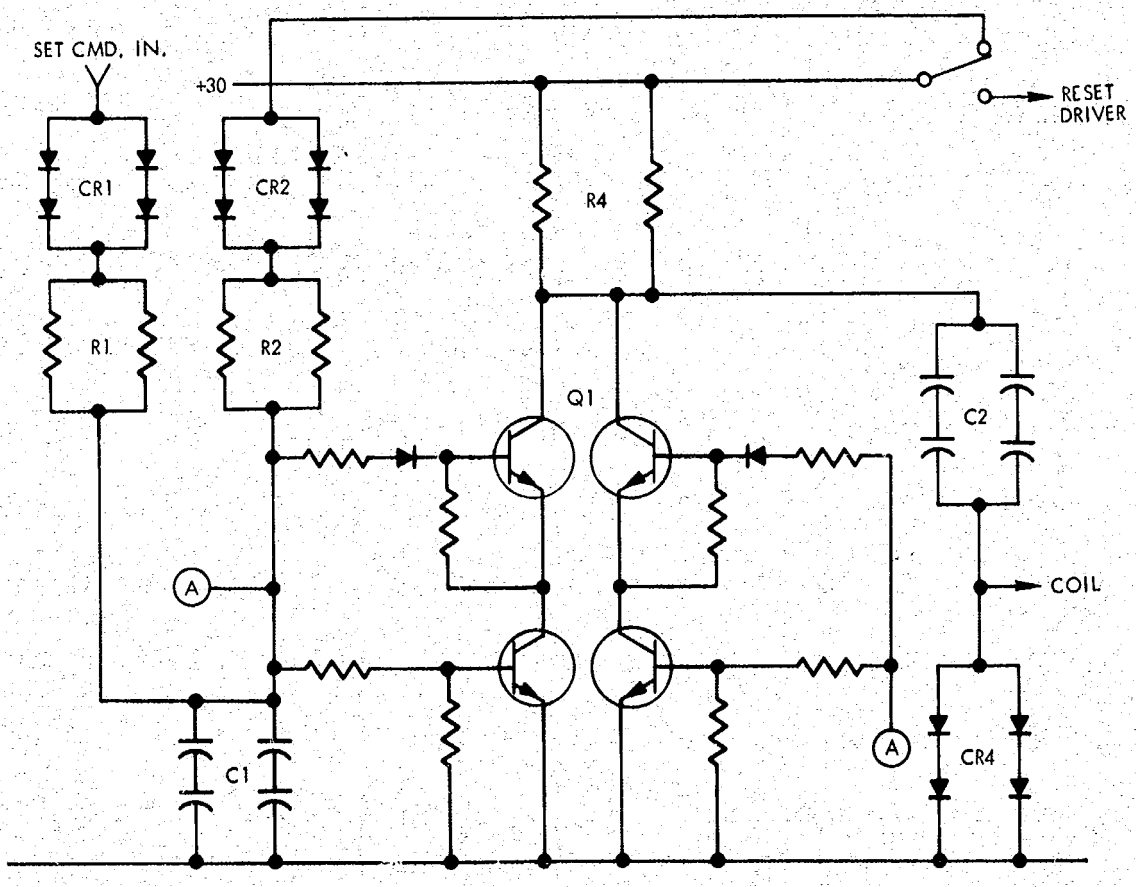

Figure 6-20. Quad Relay Driver

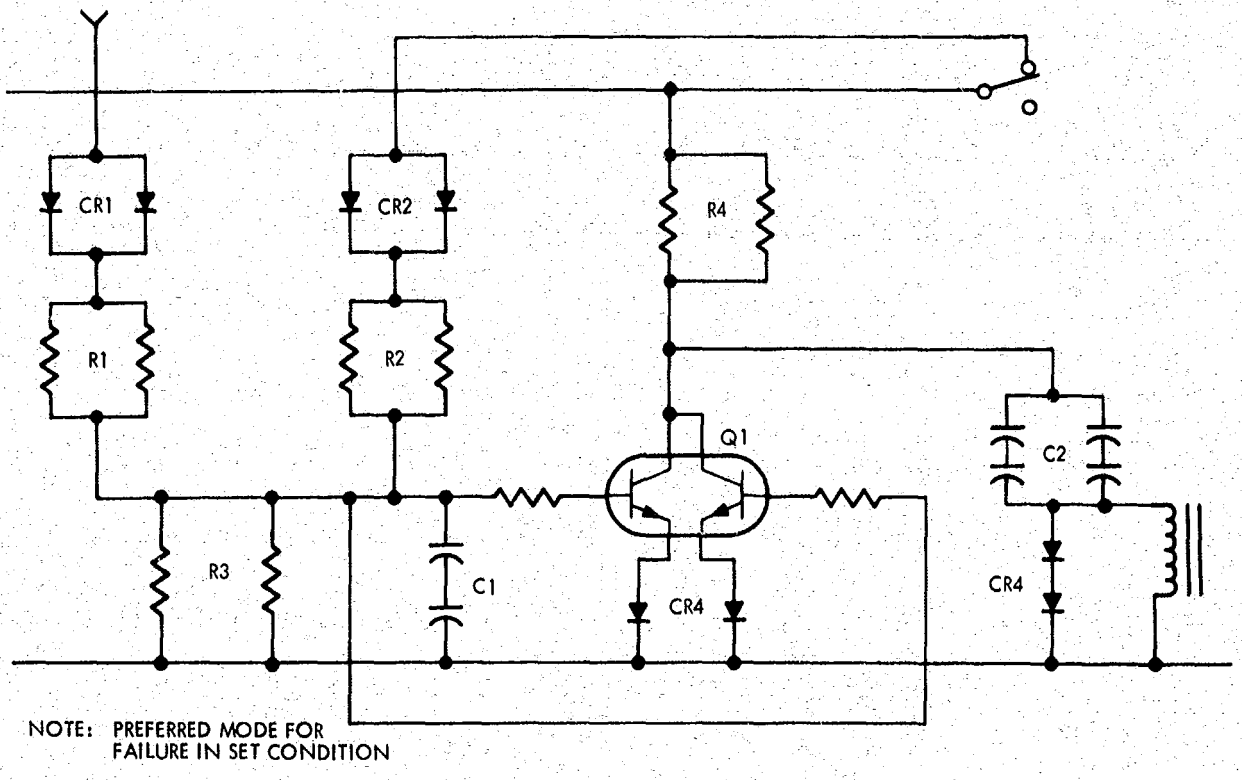

Figure 6-21a. Fail-Safe Relay Driver

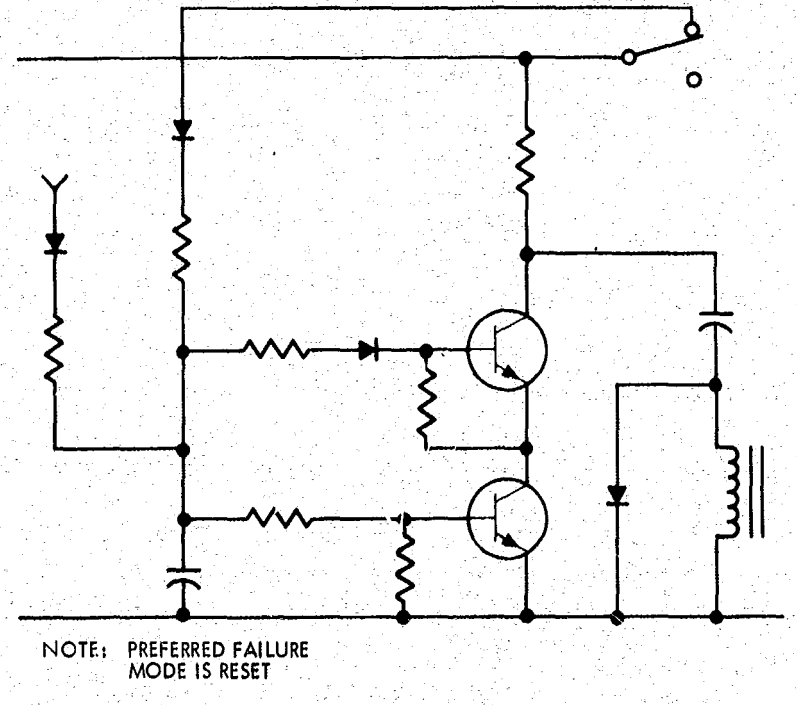

Figure 6-21b. Fail-Safe Relay Driver

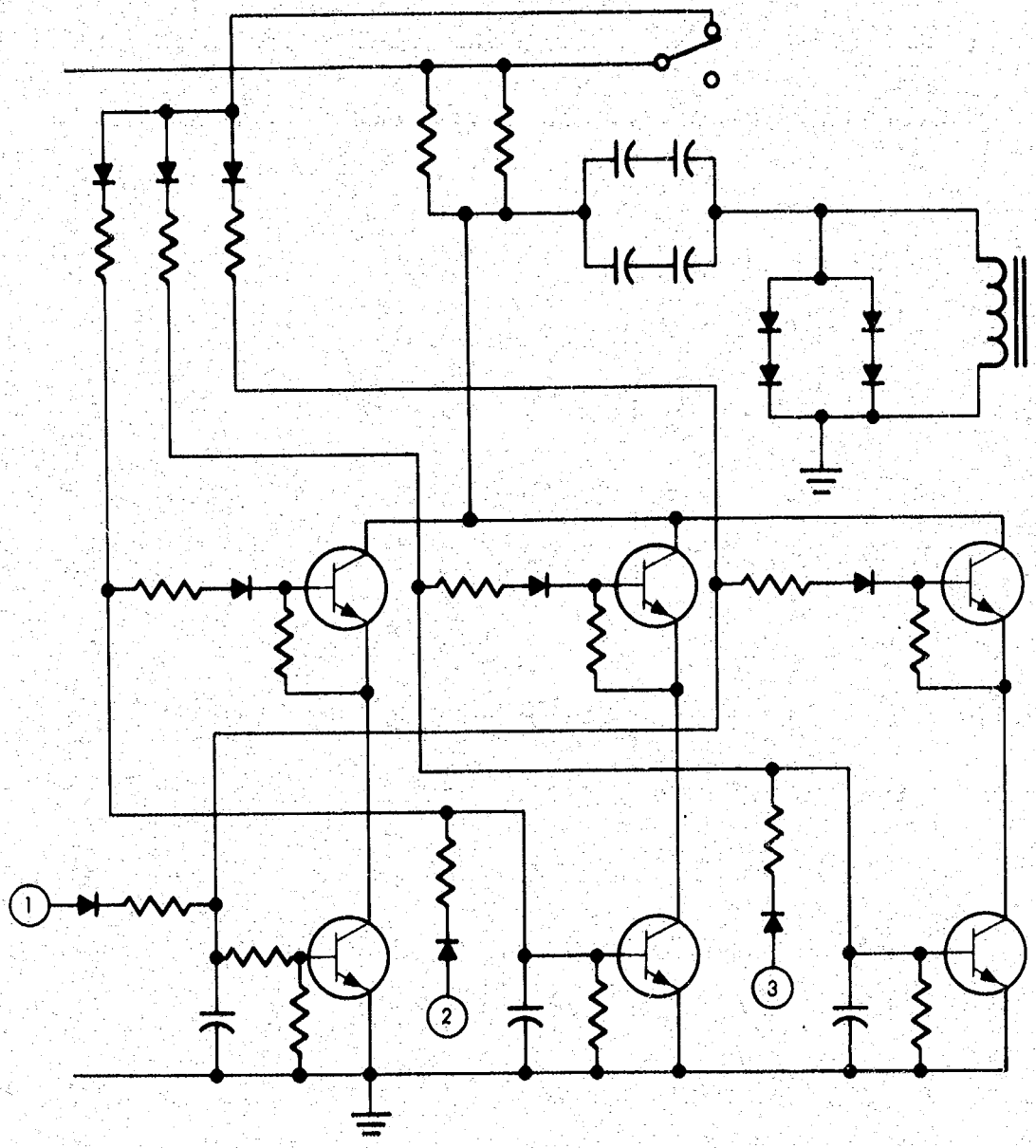

Figure 6-22. Majority Voting Relay Driver

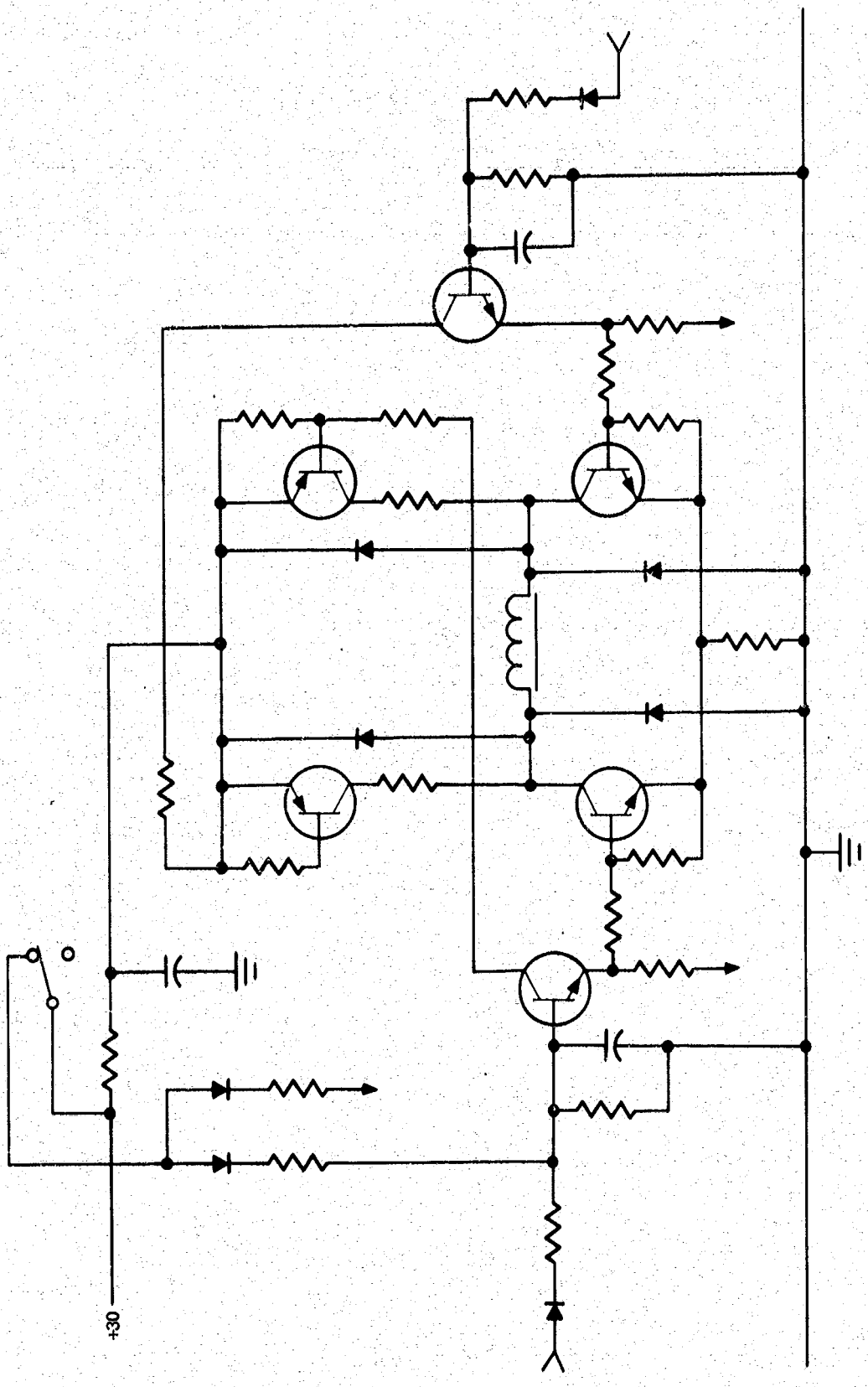

Figure 6-23. Bridge Relay Driver

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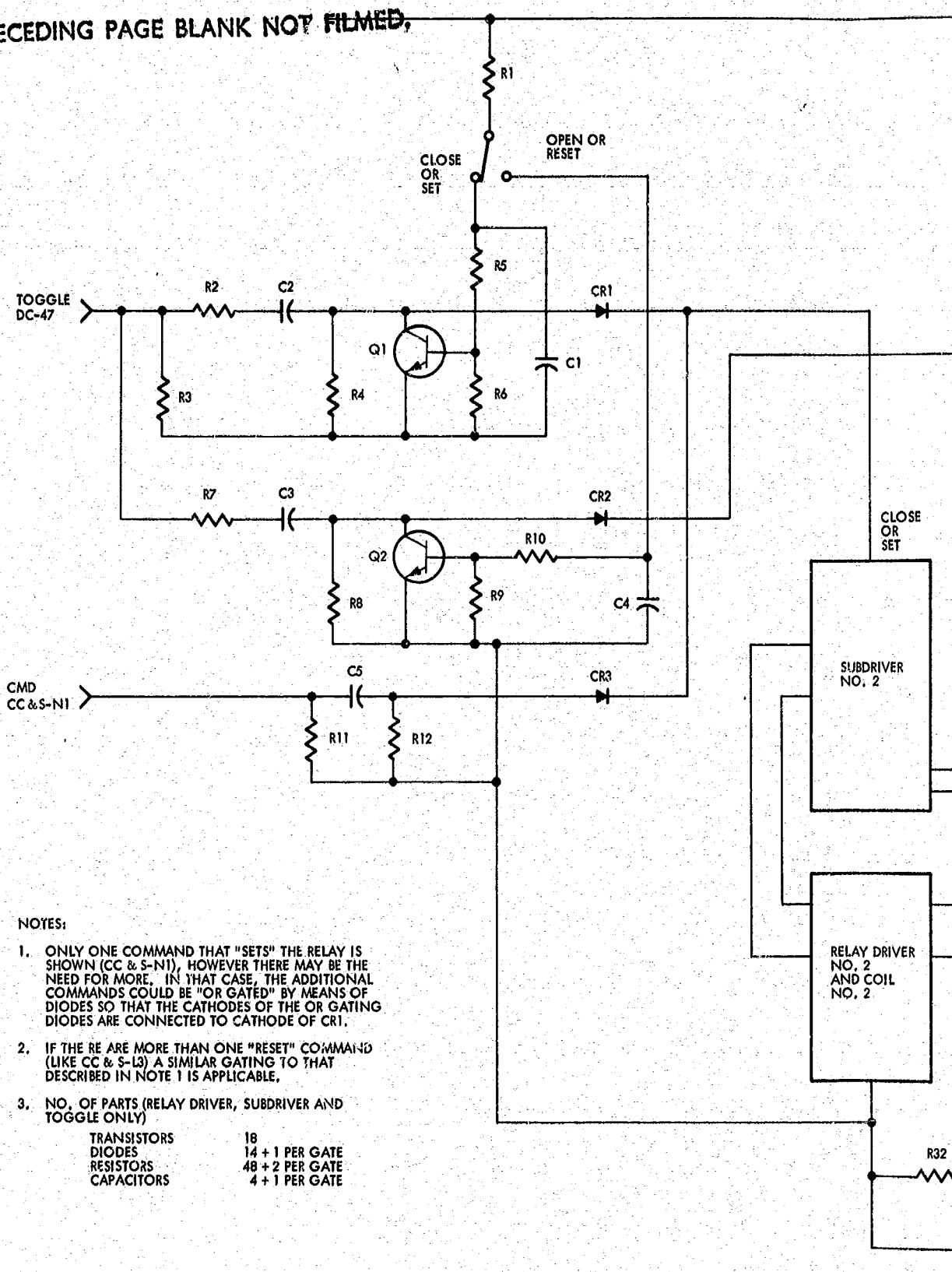


NOTES:

1. ONLY ONE COMMAND THAT "SETS" THE RELAY IS SHOWN (CC & S-N1), HOWEVER THERE MAY BE THE NEED FOR MORE. IN THAT CASE, THE ADDITIONAL COMMANDS COULD BE "OR GATED" BY MEANS OF DIODES SO THAT THE CATHODES OF THE OR GATING DIODES ARE CONNECTED TO CATHODE OF CR1.

2. IF THE RE ARE MORE THAN ONE "RESET" COMMAND (LIKE CC & S-L3) A SIMILAR GATING TO THAT DESCRIBED IN NOTE 1 IS APPLICABLE.

3. NO. OF PARTS (RELAY DRIVER, SUBDRIVER AND TOGGLE ONLY)

TRANSISTORS	18
DIODES	14 + 1 PER GATE
RESISTORS	48 + 2 PER GATE
CAPACITORS	4 + 1 PER GATE

FOLDOUT FRAME 1

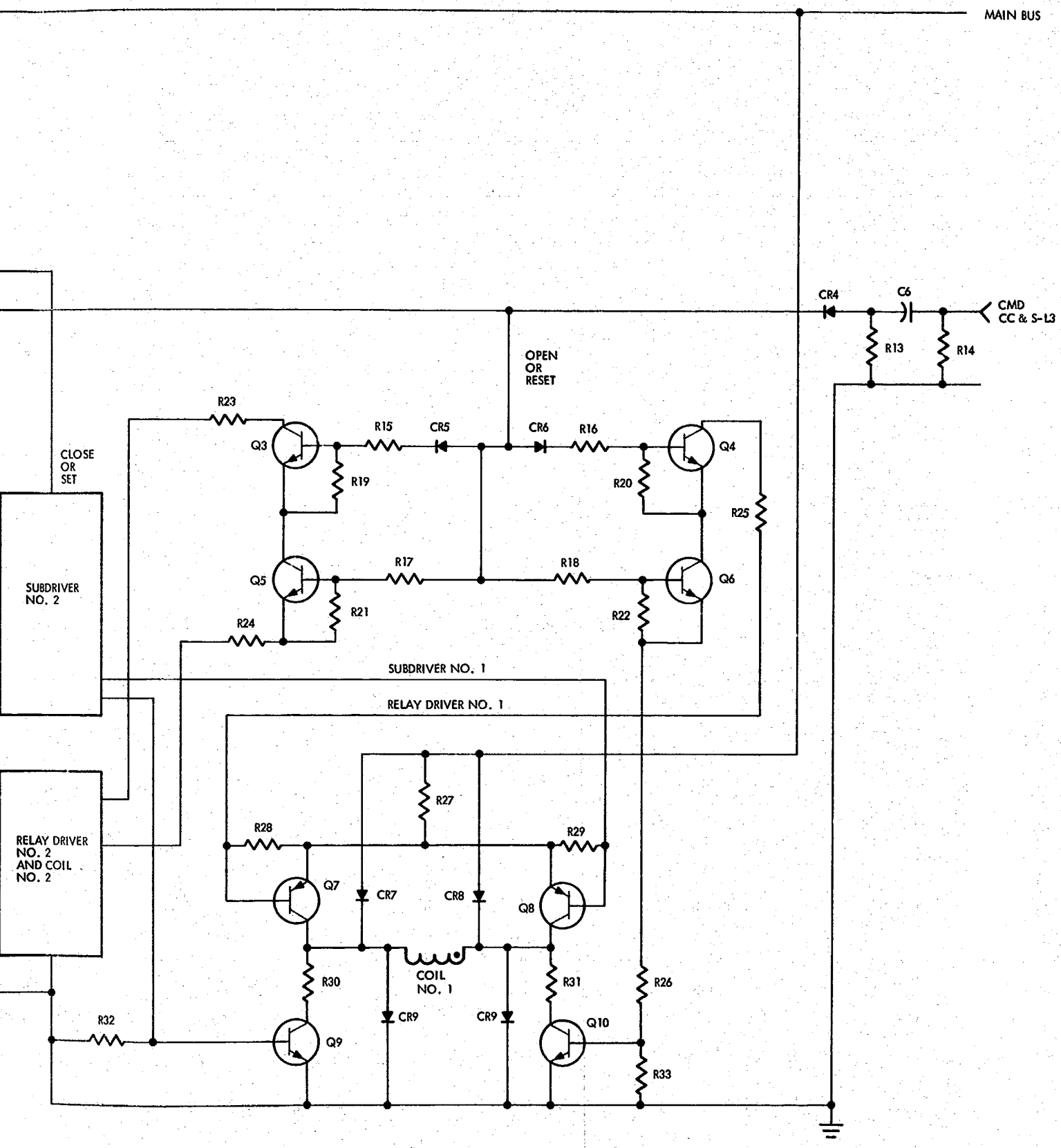


Figure 6-24. Command-Relay Driver Controls

FOLDOUT FRAME 2

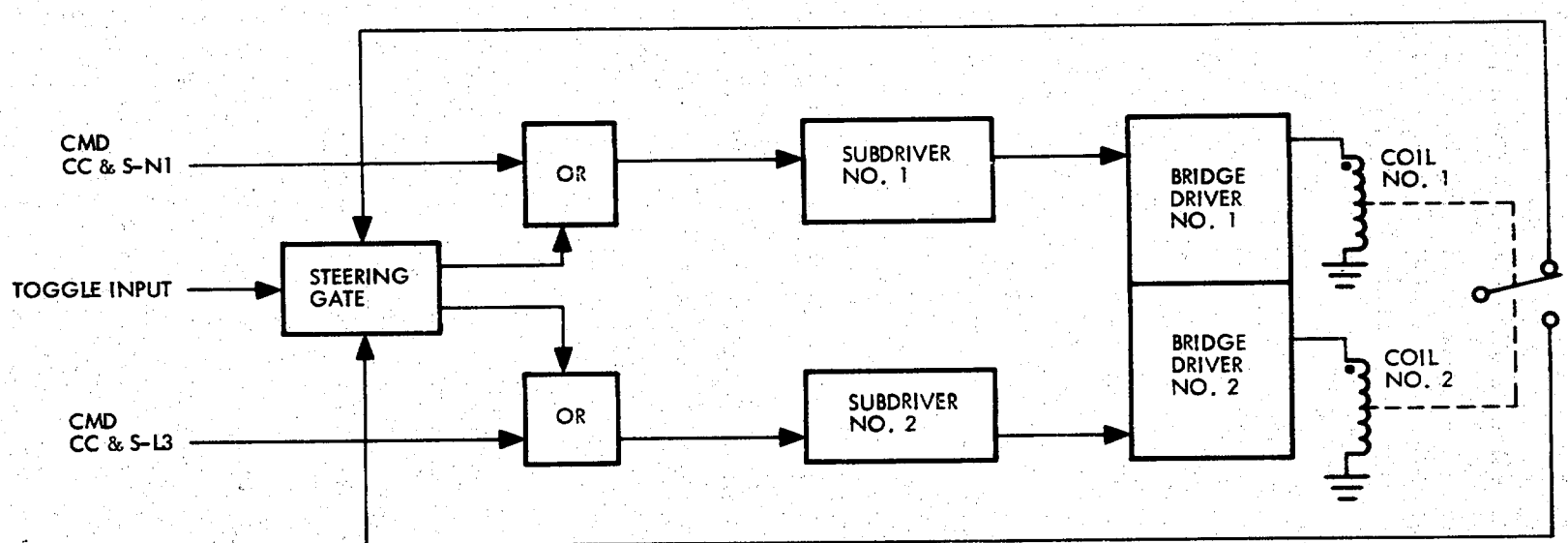


Figure 6-25. Command-Relay Driver Block Diagram

For redundancy purposes there is another identical relay driver and coil (Relay Driver No. 2 and Coil No. 2 in Figure 6-24), so that any single part failure and certain multiple part failures will not inhibit the correct operation of the relay.

Table 6-15. Characteristics of Selected Relay Drives

Item	Advantage	Disadvantage
1. Bridge driver redundant circuit	Reliability: Improved. Redundancy allows normal operation for all single part failures including one of two relay coils, except relay contacts. Many multiple part failures can also be survived.	Size and weight are increased by redundant circuit. Parts increase ≈3X.
2. AC command signal coupling	Reliability: Improved, since normal command operation can continue after a command input fails in the ON state.	Small increase in size and weight. Approximately three additional parts per OR'd command signal.
3. Toggle circuit	Reliability: Improved, since parts are restricted to the toggle command and are not in line for parallel commands. Size and weight: Timing energy storage and logic are performed at a lower level, allowing small parts tc be utilized.	
4. +30 Vdc supply	Reliability: Improved. 1) Supply is eliminated, deleting a single function which is in line with all commands. 2) Through part redundancy to allow normal operation for all single and some multiple part failures, including cable faults.	1) Increased part ratings required for operation at higher voltage. 2) Increased size and weight. Several additional parts are required for the basic supply, plus two parts per relay driver and using function (CC&S, decoder, etc.)

- Subdriver. Each subdriver is composed of four NPN transistors also connected in a bridge configuration and capable of providing input signals to both relay drivers when the subdriver itself receives an input voltage of at least 5 V referred to ground. The input terminal of each subdriver is the anode of diodes CR5 and CR6.

  One of the subdrivers causes the relay to close or set (Subdriver No. 2 in Figure 6-24) and the other will open or reset the relay. The subdrivers, again, are insensitive to any single part failure and to certain multiple part failures.

- Toggle Operation. Transistors Q1 and Q2, capacitors C1, C2, C3, and C4, resistors R1 through R10, and one relay contact constitute the toggle circuit.

  To describe the operating principle, assume that the contact has the position shown in Figure 6-24. This will cause Q1 to be on, and therefore it will not allow the next input signal to reach subdriver No. 2 via diode CR1. Instead, the toggle input will be directed through CR2, since Q2 is open and permitted to reach subdriver No. 1 (reset subdriver), causing the relay to open or reset. Once the relay is open the contact will cause Q1 to turn off the Q2 to turn on with a built-in time delay (see capacitor C1 and resistors R5 and R6) to prevent the toggle command to be directed to both subdrivers simultaneously.

  With Q1 off, the next toggle command will cause the relay to close, completing one full toggling cycle.

- Gate Circuits. The gate circuit associated with the CC&S-N1 command is only capable to close the relay, or, if the relay were already on, the application of the input will not cause the relay to change states. Conversely, the gate circuit associated with the CC&S-L3 command is only capable to open the relay. The apparent lack of redundancy in the individual toggle or gate circuits is obviated by the fact that there is more than one input circuit, whether a toggle or gate, capable of reaching the subdrivers via the OR gates (diodes CR1, CR2, CR3, and CR4).

6.8 BATTERY CHARGER

6.8.1 Description

The battery charger provides the battery charge current at a prescribed limit, if power is available. When a constant voltage limit is reached, this limit is maintained. The charger responds to a ground command to initiate and terminate charge. Charge initiation/termination is also accomplished by two on-board commands. Table 6-16 presents a comparison of charger characteristics for the Mariner '69 and the selected system.

Table 6-16. Characteristics Comparison

Characteristic	Mariner '69	Selected System
Source	Solar array	Regulated bus
Input voltage	34.6 to 50 Vdc	50 Vdc ±1%
Current limit	Less than 1 amp	300 ± 50 ma/battery
Voltage limit	34.6 Vdc	35.4 Vdc
Tolerance	±0.2 Vdc	±0.2 Vdc

6.8.2 Areas for Improvement

The circuit presently utilized incorporates no redundancy, exclusive of input and output filter capacitors. Therefore the failure of any single part disables the regulator in one of two conditions:

Open: Unable to charge the battery.

Short: Unable to voltage-limit; charge termination must be by ground command.

The open failure condition seriously degrades spacecraft capability to perform the mission, particularly since no backup capability exists for battery recharge with the regulator failing open.

PNP power transistors could be utilized to reduce the series drop if operation at input voltages approaching 34.6 Vdc is really a necessity. Additionally the current limit could be implemented resistively with the value chosen to satisfy the 1-amp current limit at the highest solar-array input voltage. This deletes a transistor (Q3) and possibly the need for a diode (CR15).

6.8.3 Approaches Considered

Of the approaches considered, switching regulators were eliminated because the efficiency improvement was not worth the additional complexity. Similarly majority voting or quad regulator circuits were also eliminated because only a small reliability improvement was achieved at a large increase in parts and weight. The three final candidate approaches are:

- Dissipative regulator (active): Present Mariner approach.
- Dissipative regulator (active: With command backup for charging if an open failure occurs.
- Dissipative regulator (inactive): Battery charge current switches to zero at voltage limit; command backup included.

The dissipative regulator considered was basically the same as the Mariner approach with the modifications discussed in Paragraph 6.8.2. A schematic is shown in Figure 6-26.

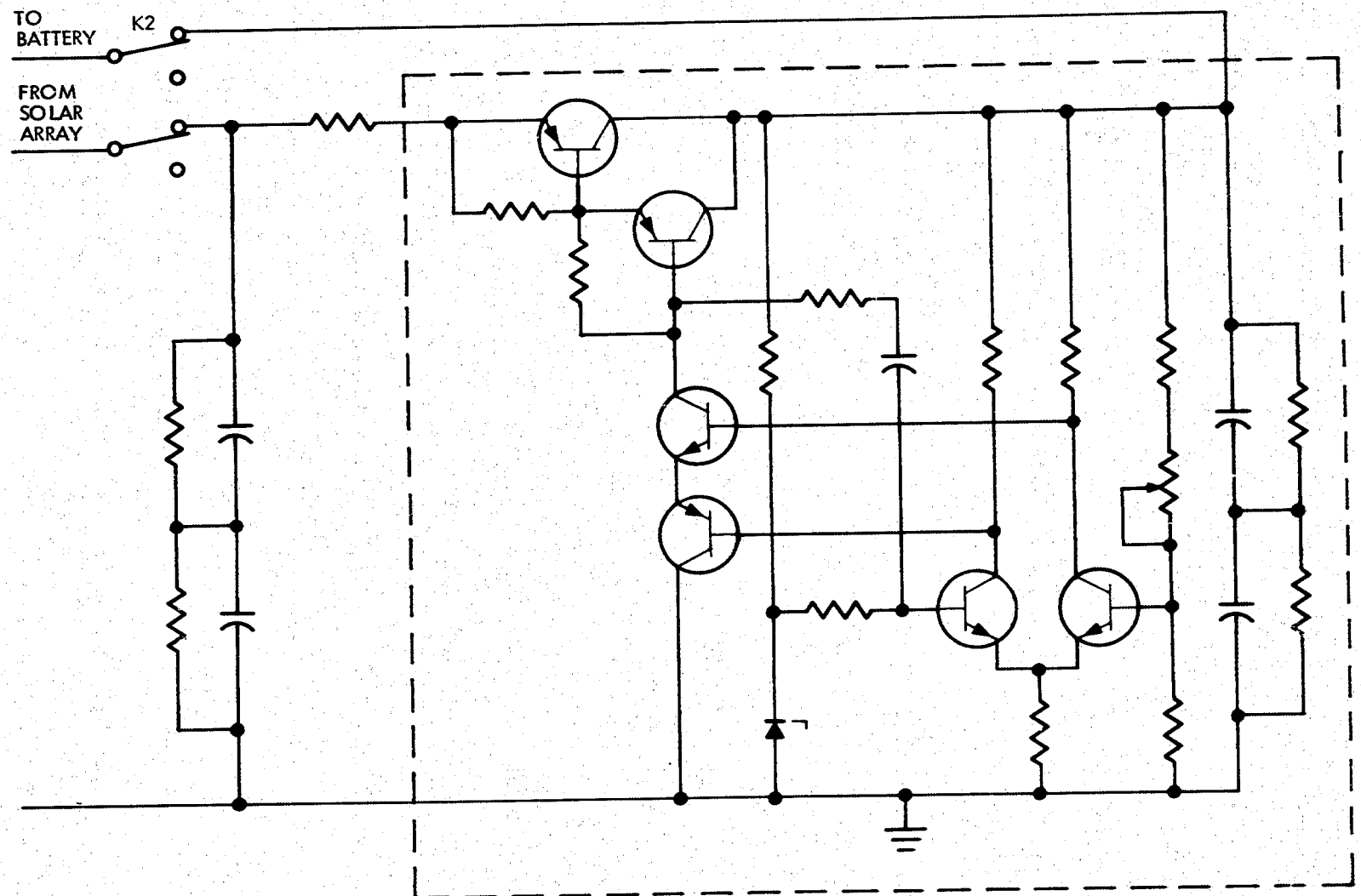


Figure 6-26. Dissipative Regulator (Active) Schematic Diagram

Figure 6-27 shows the same basic regulator with added command relay capability to override any regulator failure. Battery charge occurs through resistor R1 when K_x is commanded closed, after terminating charge through the regulator by opening K2. This same basic approach can be implemented with the existing Mariner charger design.

Since the selected system provides a regulated bus, the current could be implemented through resistors and the charge terminated by opening the series relay at the limiting voltage. Figure 6-28 shows a block diagram and schematic of this approach.

To guard against failure of the voltage sensor, if the voltage limit was sensed at too low a level to effectively charge the battery, a flip-flop plus logic is added to provide command override capability.

In a modification of the last approach, a majority voting voltage sensor can be implemented using existing, available, integrated-circuit flat-packs, (Figure 6-29). No increase in size or weight is expected since the AND gate and override flip-flop would be deleted along with the additional command.

6.8.4 Summary

Of the three basic approaches considered, the dissipative regulator with no ground command override capability was believed to be too unreliable for the orbiting mission.

Table 6-17 summarizes the four approaches using the existing Mariner approach as a base line. From the table it is seen that, for the selected system with a regulated bus, the current-limited charge can be achieved with resistors (dissipative, inactive charger). Charge termination is achieved with a voltage sensor in combination with the charger disconnect relay and driver. The sensor can be implemented in a highly reliable manner with no size or weight penalty. This approach also obviates additional command backup and related circuitry. The recommended system has two separate battery chargers.

6.9 MOMENTARY BOOSTER

6.9.1 Description of Functions

The following are the functions of the momentary booster:

a. Detection of current sharing. This particular function is important since current sharing is a misuse of the energy available at both the solar array and the battery.

b. Boost momentarily the battery voltage via a dc-to-dc converter to minimize the load seen by the solar array to a higher voltage operating point.

c. Limit the duration of boosting action as well as the idling intervals so as to be commensurate with the power capacity of the momentary booster.

6.9.2 Requirements

The following are the requirements of the momentary booster:

a. Booster must be capable of providing a minimum of 150 W power capability for a pulse duration not to exceed 1 sec.

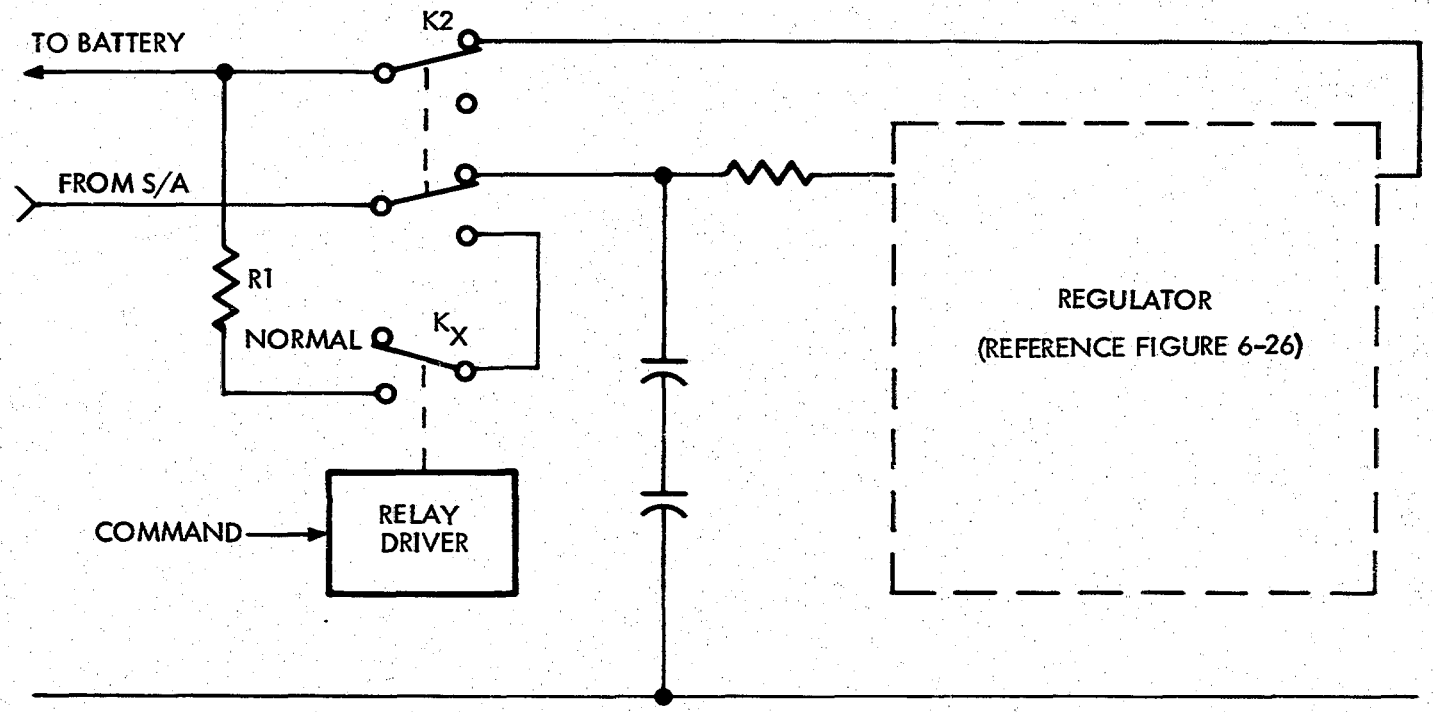
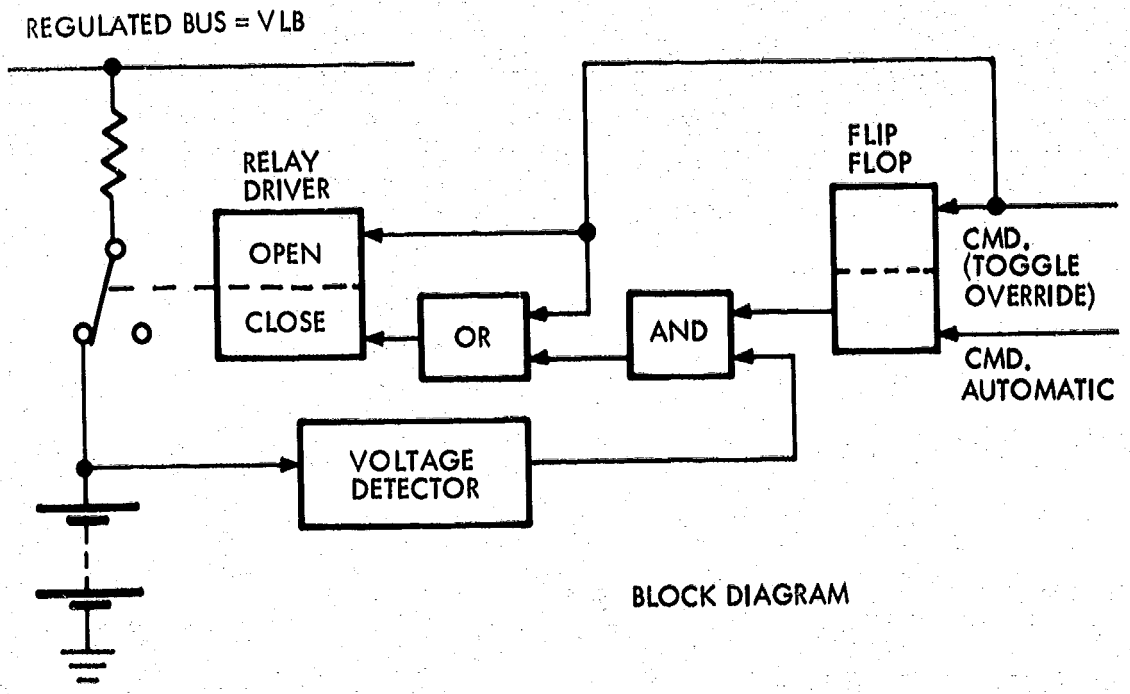


Figure 6-27. Dissipative Regulator (Active) with Command Backup for Charging



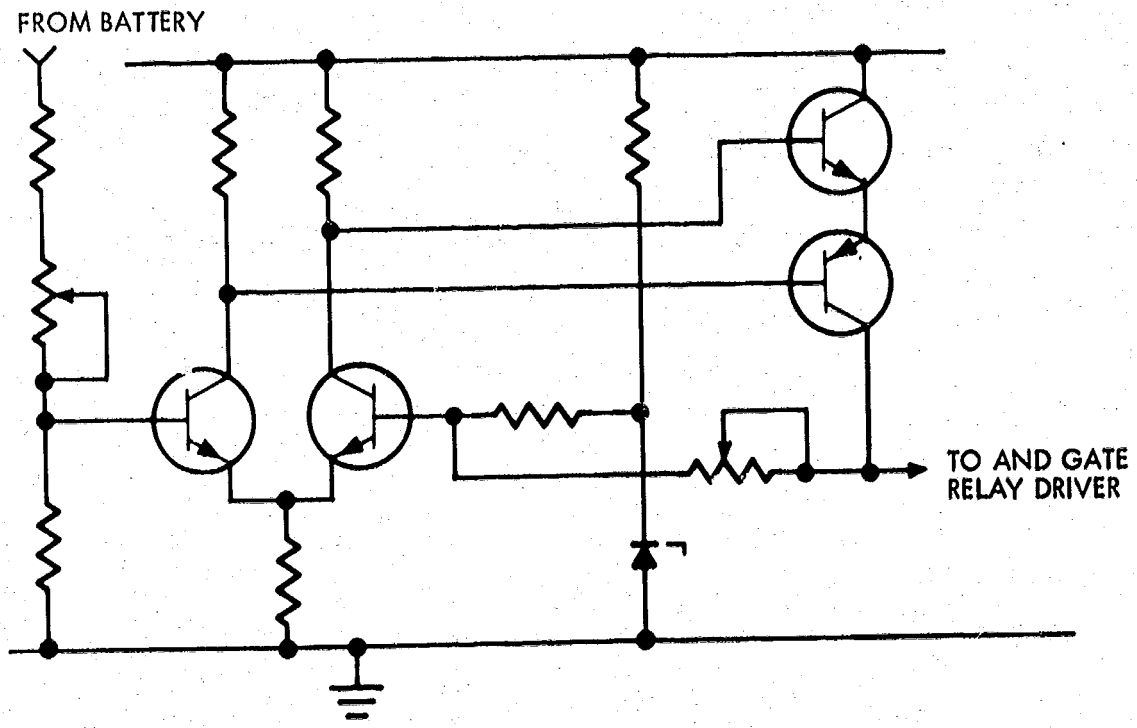


Figure 6-28. Voltage Detector Schematic

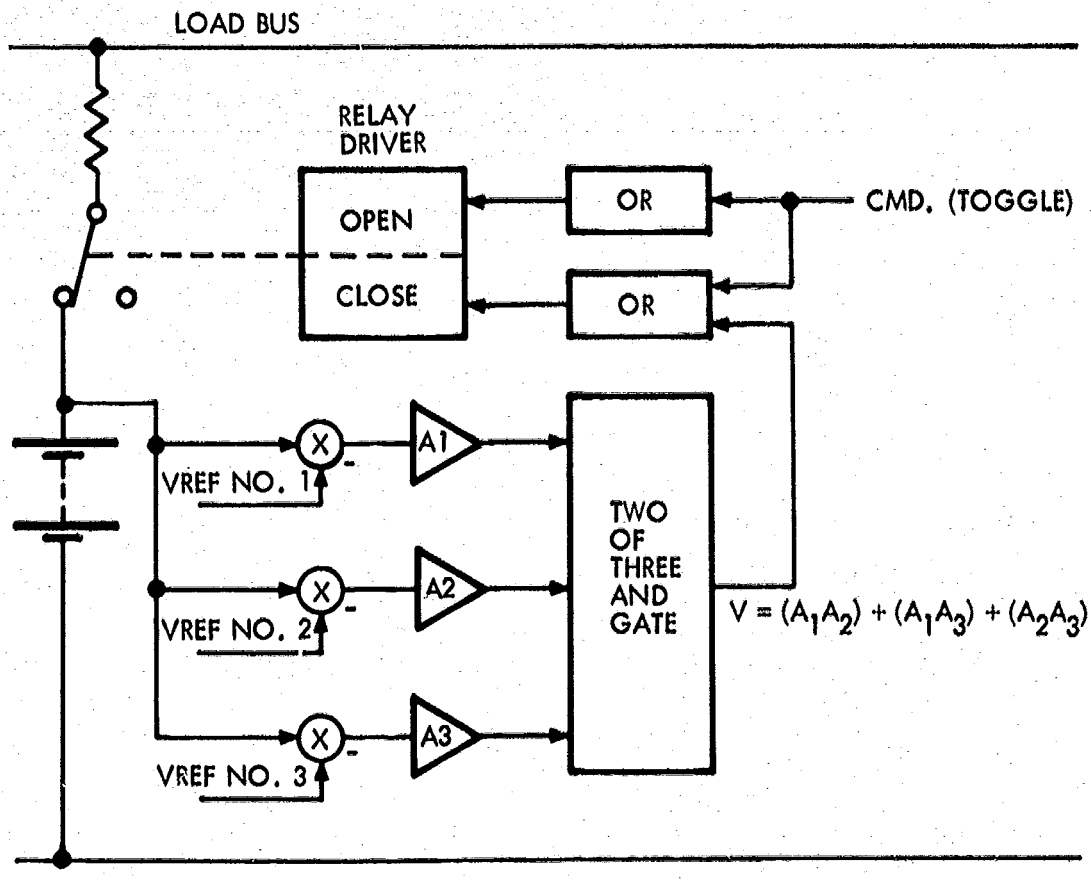


Figure 6-29. Dissipative Regulator – (Inactive) with Majority Voting Level Detector

b. Idling intervals must be within 5 sec minimum and 15 sec maximum.

c. Current-sharing detector to command boosting action whenever the primary voltage drops below 33 V.

d. Means of overriding or fusing the momentary booster must be provided to avoid the possibility of a continuous boosting action.

e. Some form of redundancy or backup must be provided to prevent current-sharing mode after the momentary booster has failed.

f. The input voltage to the boost inverter must be between 22 and 34 Vdc.

g. The output voltage of the boost inverter must be 44 V minimum.

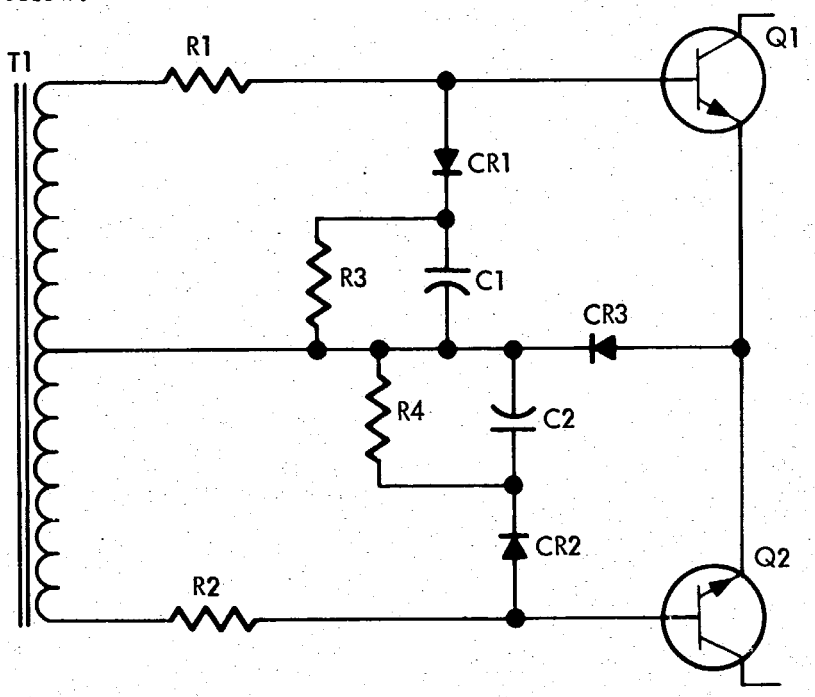
Table 6-17. Summary of Four Approaches

Charger	Advantages	Disadvantages
1. Dissipative (active) Modified	Current limit: Set by passive components (resistors). Active regulator is deleted and reliability is improved. Command backup: No backup charging mode is available if regulator fails OPEN.	No fixed-current limit.
2. Dissipative (active) with command backup	Current limit: Set by passive components (resistors). Active regulator is deleted and reliability is improved. Command backup: Charging mode exists in event regulator fails OPEN.	Addition relay and driver circuitry are required with increased size and weight. Additional command is required.
3. Dissipative (inactive) with command backup	Current limit: Set by passive components (resistors). Active regulator is deleted and reliability is improved. Command backup: Charging mode exists in event regulator fails OPEN. No additional relay or circuitry are required with automatic charge termination at voltage limit. Net weight is reduced.	No continuous voltage limit charging can be achieved. Override command and logic are required.
4. Dissipative (inactive) with command backup and majority voting sensor	Current limit: Set by passive components (resistors). Active regulator is deleted and reliability is improved. Command backup: Not required with highly reliable sensor, achieved at no weight or size penalty.	

6.9.3 Analysis of Existing Mariner Design

The following areas need improvement.

a. Momentary booster. Present Mariner approach does not show any well-defined technique to avoid the overlap of the on-state of both power switches. The reverse bias afforded by capacitor C10 during switching is helpful, but incapable of preventing overlap in the presence of a voltage waveform with a high dv/dt. One technique to avoid overlap is shown below.



where:

T1 = Transformer providing base drive to power transistors

Q1 and Q2 = Power transistors of the inverter or the boost inverter.

b. Current-sharing detector.

1. The right hand side of diff. amp. Q7 has an undesirable floating base mode of operation. A 3.3 Megohm emitter-to-base resistor is recommended.

2. There should be a resistor or a fuse in series with the coil of Q10; otherwise, there is a failure mechanism that may well result in a short across the 50-V bus: either a shorted CR1 or a shorted K1 coil (independently of the position of the K1 contacts) will lead to the failure so described.

6.9.4 Approaches Considered

6.9.4.1 Preliminary Screening

a. Mariner approach (nonredundant)

b. Mariner approach with the incorporation of improvements (see Paragraph 6.9.3.1).

c. Redundant momentary booster (using two Mariner circuits, one main and another standby).

6.9.5 Relative Merits of Individual Approaches

Concept	Approach		
	(a)	(b)	(c)
Weight: 1 = light; 2 = medium	1	1	2
Simplicity of current sharing detector: 1 = simple	1	1	1
Detector detects; c = current, v = voltage	v	v	v
Need of additional failure detector	No	No	Yes
Requires transformer or autotransformer	Yes	Yes	Yes

7. SYSTEM COMPARISON AND SELECTION

7.1 INTRODUCTION

For ac distribution systems, there are a multitude of possible systems to consider. Section 5 "Selection of Model System Configurations" delineates the rationale in arriving at the five model systems depicted in Figure 5-1. For the Mars Orbiter on flyby missions, efficient battery charging is not required for the following reasons:

- Battery charging power is relatively low (25 W)
- Battery charging times are long
- The sizing of the solar array occurs during a nonbattery charging mode (namely TV sequence)

In summary, contrary to low earth orbits where continuous charge/discharge cycling of the battery occurs, battery-charging efficiency is not a primary design criteria for the missions of concern.

The power conditioning elements (2.4 kHz and 1ϕ, 3ϕ 400-Hz inverters) supply regulated ac power to the spacecraft user equipment. There are several ways of supplying the regulated ac power, namely:

- Providing a regulated dc (±1% regulation) to an unregulated inverter (present Mariner scheme).
- Provide separate regulators in the ac conversion units.

Based upon previous studies* centralized (e.g., the use of a single regulator for the entire set of inverters) rather than distributed equipment will result in higher efficiency, lower weight, and fewer number of parts.

Analysis of the power requirements shows that the majority of power (194 W maximum) is required at 2.4-kHz and 116-W unregulated power for TWT converters and dc heaters. The major system tradeoffs involve the various methods of conditioning the power source power (solar array and battery) to provide unregulated power and regulated power. However, it is desirable for reasons of load equipment design simplicity and efficiency to provide all the loads with regulated dc. Power system tradeoffs, on the other hand, will determine the optimum mix of unregulated and regulated power distribution.

Table 7-1 summarizes, in matrix form, the relative advantages and disadvantages of the various system methods to provide conditioned power for both the regulated and unregulated dc loads.

7.2 SOLAR ARRAY POWER UTILIZATION

The solar array utilization factor (SAUF) for solar array power utilization will be defined as the ratio of power delivered to the loads divided by the required solar array maximum power at the critical design point. The definitions are as follows:

- Power to loads: Unregulated dc (heaters), 1ϕ or 3ϕ output, 2.4 kHz output, and output power of the TWT converter.

*"Study and Analysis of Satellite Power System Configurations for Maximum Utilization of Power" Report No. 04894-601-R000, Contract NAS 5-9178, 1966 December 30

Table 7-1. Advantages and Disadvantages of System Methods

Criteria	SYSTEM 1 PWM Array Control and Battery Boost Regulator	SYSTEM 2 Active Shunt and Battery Boost Regulator	SYSTEM 3 Zener Limiter and Boost Line Regulator	SYSTEM 4 Shunt Limiter and Boost Line Regulator	SYSTEM 5 Buck-Boost Regulator
1. Solar array power utilization (%)	84.4	81.1 to 87.3	84.5	85.8	84.4
2. Reliability assessment	≥0.999	≥0.999	0.927	≥0.999	≥0.999
3. Number of power-handling units	2	2	2	2	1
4. Short circuit protection	Current-limiting	Current-limiting	None	None	Current-limiting
5. Weight (lb)	20	19 to 25	16	≥19 to 25	10
6. Isolation between power sources and regulator dc bus	No	No	No	No	Yes
7. Restring of solar array	Yes	Yes	No	No	No
8. Heat dissipation	Moderate	High (in shunt elements)	High transient (zener limiter)	High transient (shunt limiter)	Moderate
9. Number of active control loops	3	3	1	2	1
10. Complexity	Current-sharing	Current-sharing	Low	Low	Low
11. Momentary booster	No	No	Yes	Yes	Yes
12. Battery discharge diode	No	No	Yes	Yes	Yes
13. Testability	No problems	Shunt regulator during power-dissipating mode	No problems	Shunt limiter during power-dissipating mode	No problems
14. Failure detection	More complex with PWM and boost regulator	Battery boost regulator	Boost line regulator	Boost line regulator	No detection parallel operating redundancy
15. Transient response	Same	Same	Same	Same	Same
16. Battery power	0	0	+3.5% (single diode)	+7.0% (quad discharge diode)	-7.0% (quad discharge diodes)
17. Cabling	Moderate	Moderate	Moderate	Moderate	Minimum
18. Test and manufacturing	Moderate	Moderate	Moderate	Moderate	Minimum

- Critical design point: The critical design point is that time in the mission where the solar array power margin (with respect to required load) is a minimum. For the orbiter mission, the critical design point occurs during the TV sequence when all experiments and the high-level TWT are turned on.

The analysis is presented in the following sequence:

- Comparison of existing Mariner power system design with a buck-boost system.
- Solar array power utilization for an active shunt system – Model System No. 2
- Comparison of SAU factors for all five model systems, including efficiency improvements in the TWT converter and 2.4 kHz inverter.

7.2.1 Comparison of Existing Mariner Design with the Improved Buck-Boost System

The following analysis will show how solar array power utilization can be improved by increasing the efficiency of the existing power conditioning elements. The major functional power-handling elements for the existing MM system are shown in Figure 7-1.

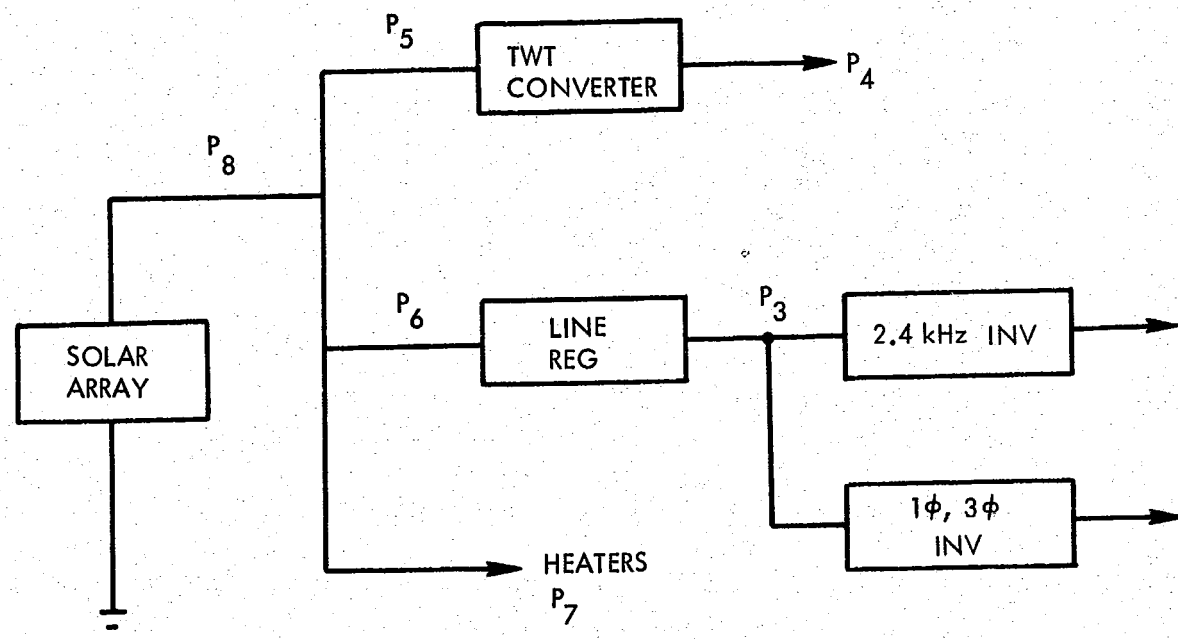


Figure 7-1. Power-Handling Elements

P_1 = output power of 2.4 kHz inverter

P_2 = output power of 1φ or 3φ inverter

P_3 = output power of line regulator

P_4 = output power of TWT converter

P_5 = input power to TWT converter

P_6 = input power to line regulator

P_7 = heaters

P_8 = required solar array power

η_1 = efficiency of 2.4 kHz inverter

η_2 = efficiency of 1ϕ or 3ϕ

η_3 = efficiency of line regulator

η_4 = efficiency of TWT converter

Analysis of the load profile (Table 4-2) shows that the maximum solar array power requirements occur during the TV sequence. The loads for this mode are as follows:

P_1 = 187.15 W $\quad\quad$ η_1 = 0.912

P_2 = 15.5 W $\quad\quad$ η_2 = 0.838

P_5 = 89.0 W $\quad\quad$ η_3 = 0.887

P_6 = 27.0 W $\quad\quad$ η_4 = 0.75

Solar array power (existing MM '69 design)

$$= \frac{\frac{P_1}{\eta_1} + \frac{P_2}{\eta_2}}{\eta_3} + P_5 + P_6 + \text{line losses}^*$$

$$= \frac{\frac{187.15}{0.912} + \frac{15.5}{0.838}}{0.887} + 89 + 27 + \text{line losses}$$

$$= \frac{205 + 15.5}{0.887} + 89 + 27 + \text{line losses}$$

$$= (252 + 89 + 27)\ 1.03 = 368\ (1.03 = 379\ \text{W} \quad (7\text{-}1)$$

The power flow diagram for the recommended buck-boost system is shown in Figure 7-2.

Solar array power requirements for the recommended buck-boost regulated dc system have been computed for the following basis:

Case 1:

a. TWT converter efficiency of 75% (existing design)

b. 2.4 kHz inverter efficiency of 91.2% (existing design)

*Line losses assumed to be 3%.

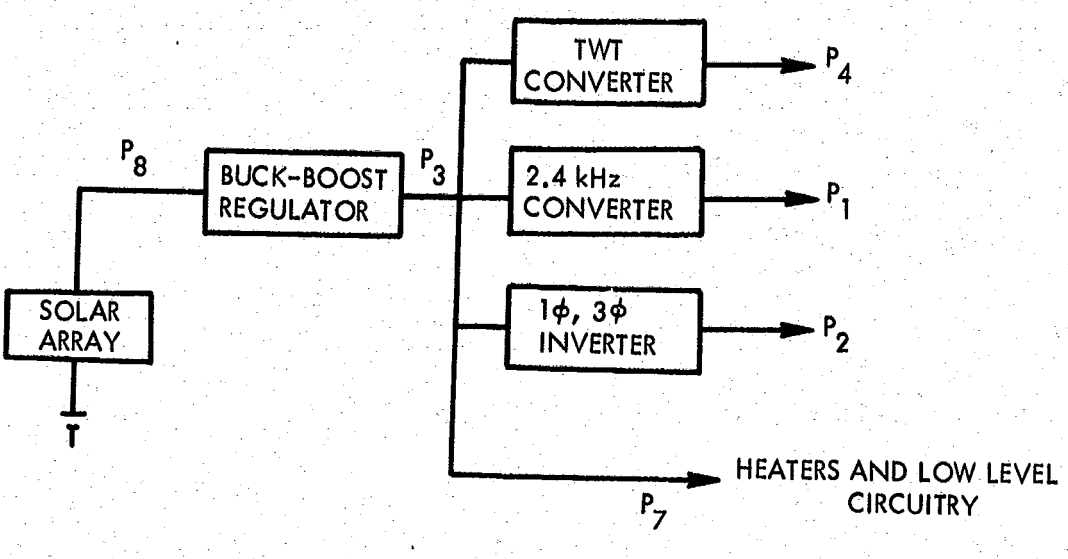


Figure 7-2. Power Flow Diagram

Case 2:

a. TWT converter efficiency of 92% (improved design)

b. 2.4 kHz inverter efficiency of 91.2% (existing design)

Case 3:

a. TWT converter efficiency of 92% (improved design)

b. 2.4 kHz inverter efficiency of 93% (improved design)

The required solar array power for Case 1 is as follows:

$$P_8 = \text{Solar array power} = \frac{\left(\frac{P_1}{\eta_1} + \frac{P_2}{\eta_2} + \frac{P_4}{\eta_4} + P_6\right)\left(1.03\right)}{\eta_3} \qquad (7\text{-}2)$$

where:

$P_1 = 187.15$ W $\quad \eta_1 = 91.2\%$

$P_2 = 15.5$ W $\quad \eta_2 = 83.8\%$

$P_4 = 66.7$ W $\quad \eta_4 = 75.0\%$

$P_7 = 27$ W $\quad \eta_3$ = efficiency of buck-boost regulator

$$= \frac{339.5\,(1.03)}{\eta_3} = \frac{350}{\eta_3} \qquad (7\text{-}3)$$

The required solar array power for Case 2 is as follows:

$$\text{Solar array power} = \frac{323\,(1.03)}{\eta_3} = \frac{333}{\eta_3} \qquad (7\text{-}4)$$

where:

$P_1 = 187.15$ $\quad \eta_1 = 91.2\%$

$P_2 = 15.5$ $\quad \eta_2 = 83.8\%$

$P_4 = 66.7$ $\quad \eta_4 = 92\%$

$P_7 = 27$ $\quad \eta_3$ = efficiency of buck-boost regulator

For Case 3, the required solar array power is

$$\frac{319}{\eta_3}\,(1.03) = \frac{329}{\eta_3} \qquad (7\text{-}5)$$

where:

$P_1 = 187.15$ W $\quad \eta_1 = 93\%$

$P_2 = 15.5$ W $\quad \eta_2 = 83.8\%$

$P_4 = 66.7$ W $\quad \eta_4 = 92\%$

$P_7 = 27$ W $\quad \eta_3$ = efficiency of buck-boost regulator

Equations (7-3), (7-4), and (7-5) are depicted in graphic form in Figure 7-3.

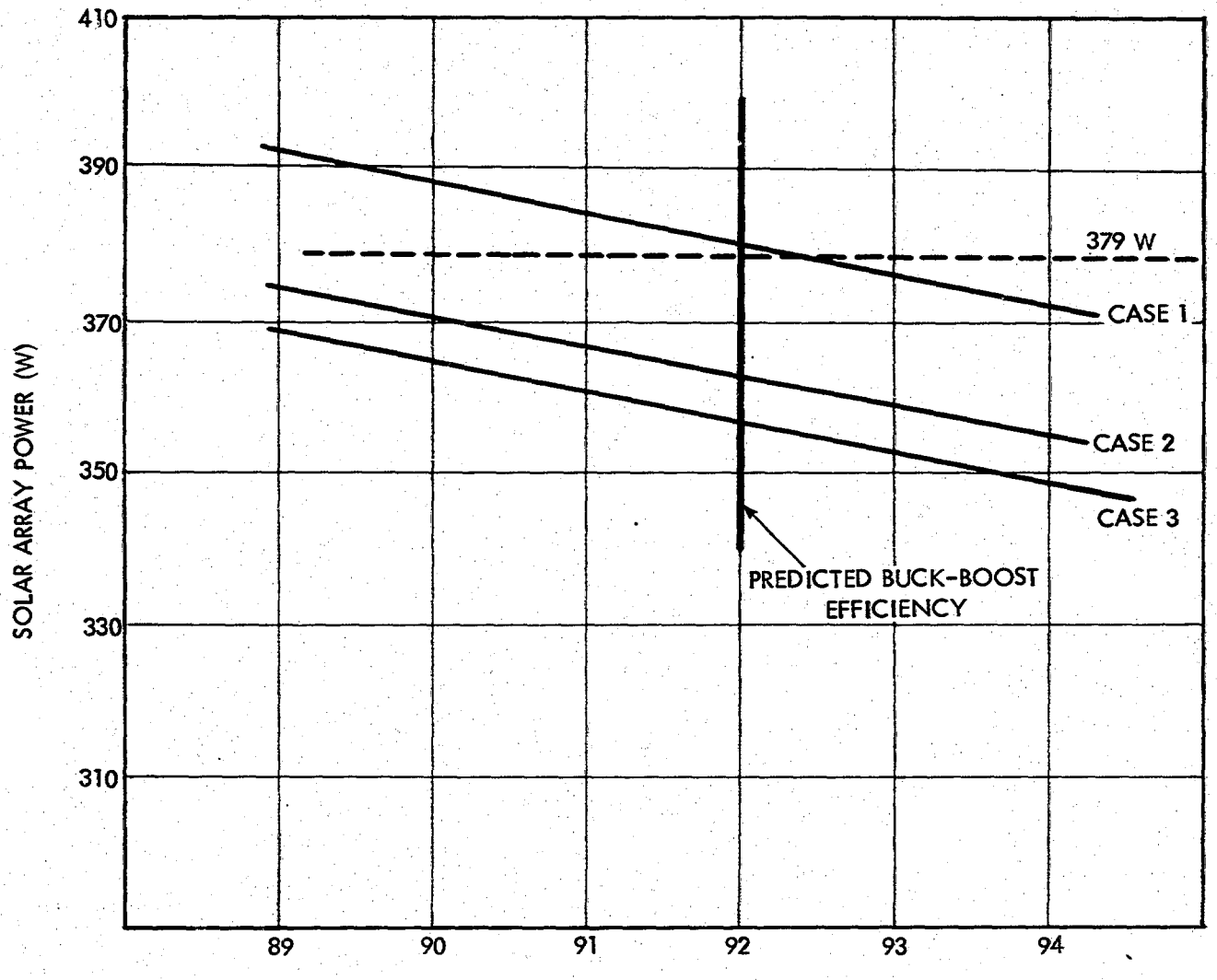


Figure 7-3. Required Solar Array Power versus Buck-Boost Efficiency

7.2.2 Active Shunt System

The active shunt system (regulated dc bus) SAU factor is a direct function of the solar array I-V curve at Earth and the I-V curve at Mars. Figure 7-4 illustrates the relationships between the regulated dc voltage and the solar array power availability. For a given constant power load, P_L, the solar array must satisfy this at Earth as well as at Mars. In Figure 7-4, P_L can be satisfied at Earth (point E) and with a little margin at Mars at point M. For this case the regulated dc voltage (shunt voltage) will be V_R. The power available at the regulated dc (V_R) is P_S while the maximum available power is P_{max}. The tradeoff for shunt systems is as follows:

The shunt system, as shown in Figure 7-4, does not operate at P_{max} at Mars; however, systems which can operate at P_{max} will require some form of a regulator to force the solar array operating point at P_{max}. The additional losses in the regulator must be traded off with the additional load power capability of the system when operating at P_{max}. There are several factors which can affect the regulated dc design center (V_R) and the array utilization for a shunt system, namely:

a. Solar array temperature uncertainties

b. Solar array I-V curve uncertainties

c. Spacecraft-to-Sun distance (AU) variations

Figure 7-5 is a plot of the required solar array maximum power requirements at Mars as a function of AU. The load conditions (TV sequence) are the same as delineated in Paragraph 7.2.1. The bottom curve labeled "No Uncertainty" shows an increasing solar array power requirement as a function of AU. This is directly attributable to the solar array temperature, decreasing with an increase resulting in solar array maximum power at Mars (P_{max}) becoming further removed for the available power (P_S) at the regulated voltage V_R. The top curve is an arithmetic worst-case condition in which the uncertainties in solar array temperature and I-V curve are taken in directions resulting in an upper maximum limit for solar array power required.

7.2.3 Summary of Solar Array Utilization Factors for Model System

Table 7-2 shows in summary form the SAU factors and the required solar array power requirements (TV sequence mode) for the five model systems. Significant improvements can be made by simply improving the TWT converter efficiency from the existing 75% to 92%. The effect of such an improvement is delineated in Table 7-2.

7.3 NUMBER OF POWER-HANDLING UNITS

All the model systems, except the buck-boost, require two power-handling devices, one for the array control (zener or shunt limiter) and a boost line or battery boost regulator. The buck-boost combines the array and battery/line regulation into one single unit.

7.4 SHORT CIRCUIT PROTECTION

Table 7-3 compares the short-circuit capabilities and characteristics of the five model systems. For system No. 1, current-limiting can be provided in the power regulators; however, fault currents will be approximately 2.4 times normal maximum currents (for comparison purposes it is assumed that the current limit is set 20% higher than maximum expected currents).

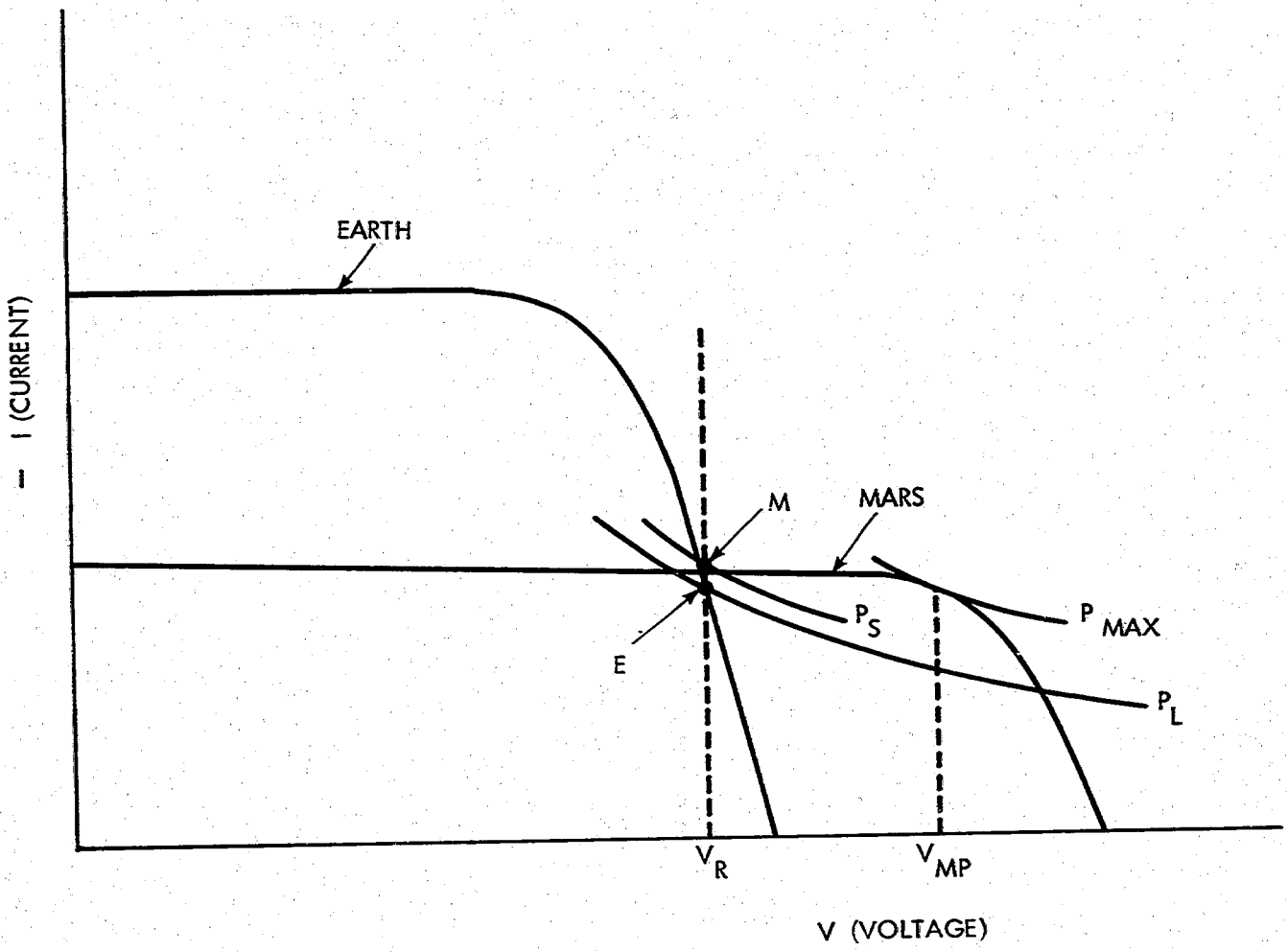


Figure 7-4. Typical Solar Array and Load I-V Characteristics

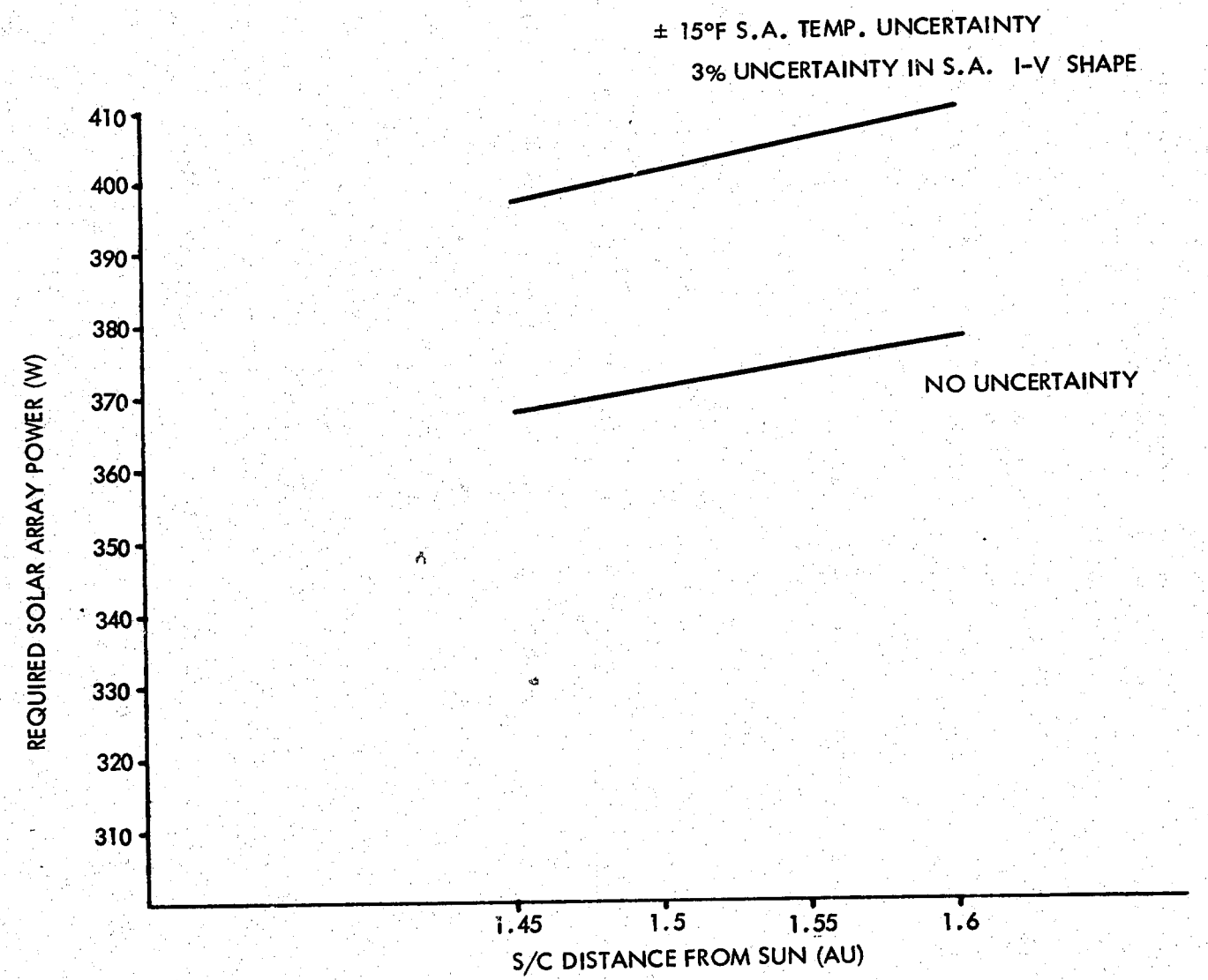


Figure 7-5. Required Solar Array Power versus S/C Distance for a Shunt Regulator System

Table 7-2. Solar Array Power Utilization

System	Solar Array Utilization Factor (%)				Comments
	TWT Converter Efficiency (75%)	Required Solar Array Power	Improved TWT Converter Efficiency (92%)	Required Solar Array Power (W)	
1. Zener limiter and boost line regulator (Mariner)	80.8	379	84.5	363	Boost line regulator efficiency of 88.7%
2. Shunt limiter and boost line regulator (BLR)	80.8	379	84.5/86.2*	363/355*	*η_{BLR} = 94% and all power processed through regulator
3. Shunt limiter and battery boost line regulator	81.1 to 83.5	378 to 368	85 to 87.3	361 to 351	
3a. Same with maximum uncertainties	74.8 to 77.0	410 to 397.5	77.9 to 80.5	393.5 to 381	
4. PWM regulator and battery boost regulator	80.5	380.5	84.4	363	η_{PWM} = 92%
5. Buck-boost (BB) regulator	80.5	380.5	84.4	363	η_{BB} = 92%

Table 7-3. Short-Circuit Capabilities of Model Systems

System No.	Regulators	Current Limit	Maximum Fault Current	Comments
1.	PWM battery boost	1.2 I	2.4 I	Requires isolation transformer to provide current limit
2.	Active shunt	None	≥2.5 to 3.0 I	Depends on array current capability
3.	Zener limiter boost line	None None	≥5	Requires isolation transformer in boost line regulator for current limiting; reduces efficiency
4.	Shunt limiter boost line	None None	≥5	Same as above
5.	Buck-boost	1.2 I	1.2 I	

Current-limiting cannot be incorporated easily or efficiently in zener or shunt limiter systems. Boost-line regulators require an isolation transformer or some additional series current-limiting circuitry. The buck-boost, since it has an isolation transformer and it processes both the solar array and battery power, can limit fault current to a reasonable level above normal load currents. The primary advantages of current-limiting include:

a. Allows additional time for corrective action to be taken in the event of a load fault.

b. Limits maximum current through 2.4-kHz fault sensor relay and assures reliable transfer in the event of a 2.4-kHz inverter short.

c. Limits maximum current through power system units and cabling in the event of ground testing malfunctions.

7.5 WEIGHT

The weight of system No. 1 is composed of a redundant PWM regulator (10 lb) and a redundant battery boost regulator (10 lb). The shunt limiter weights for systems No. 2 and 4 are based on a full dissipative shunt design approach, in which the shunt elements are mounted on the solar array panels. Figure 7-6 shows how the heat dissipation is distributed between the resistor (nichrome wire, for example) and the power transistors. For the Mars Orbiter mission, the shunt would be designed for a maximum of 600 W. Maximum heat dissipation in the transistors will be approximately 156 W. The shunt limiter weights are based on shunt element power/weight ratios of 20 W/lb achieved on past TRW Systems spacecraft programs. The precise weights will require further detailed analysis of the actual thermal interfaces and the proper sizing of the heat sinks.

System No. 3 (existing Mariner design) consists of 12.2 lb (redundant boost regulators) and an estimated weight of 3.8 lb in zeners and associated wiring.

The shunt limiter in system No. 4 dissipates power only during transient solar array temperature conditions (launch and post-orbit insertion). Since the

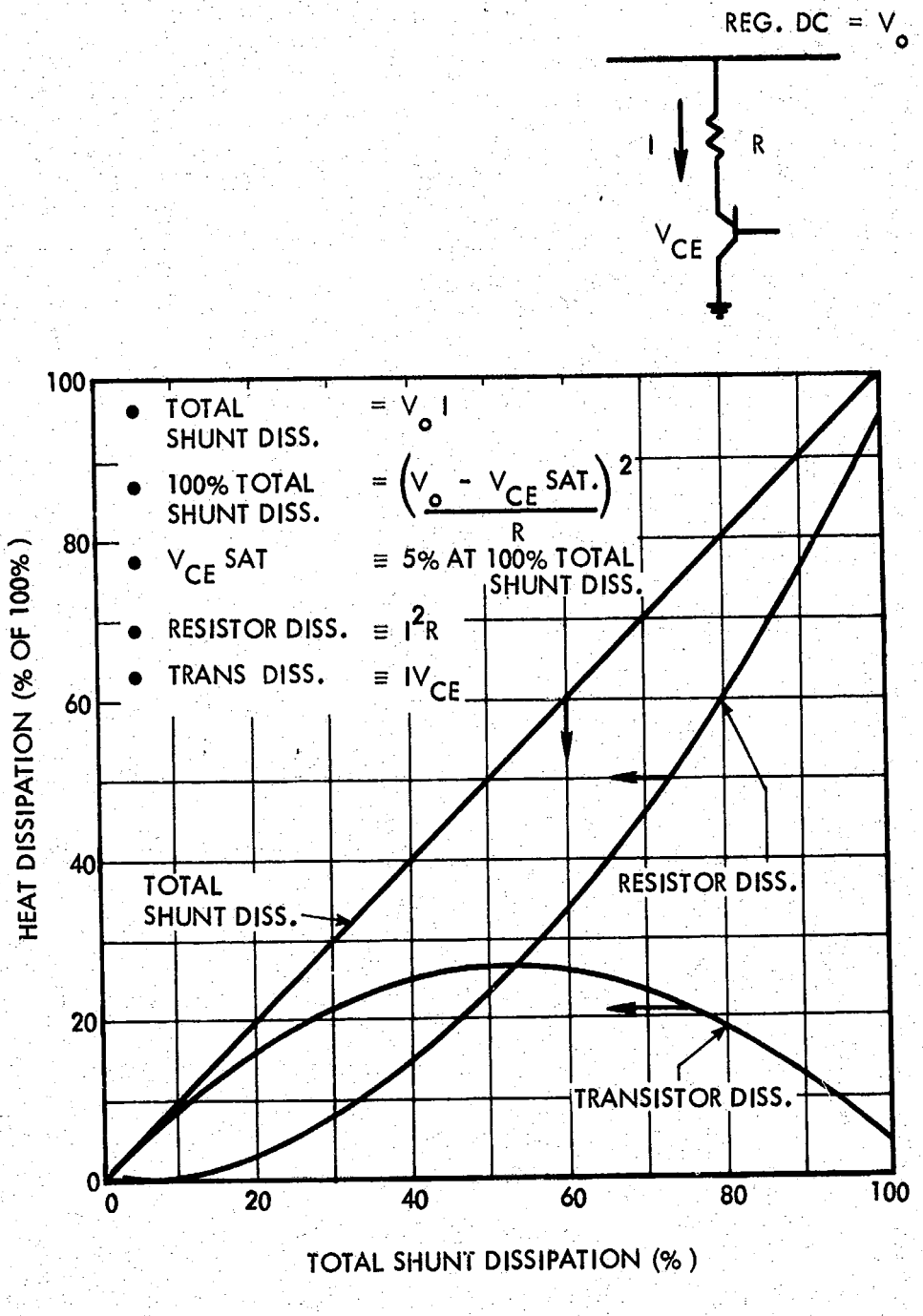


Figure 7-6. Heat Dissipation Characteristics for Full Shunt System

high heat-dissipation duration may be from 5 to 10 min, it may be possible to reduce the shunt heat sink weights. The buck-boost, being a single unit, is estimated to be the lightest of the above-mentioned five forms of power regulation.

7.6 TRANSIENT RESPONSE

The present system design has poor transient response characteristics in the unregulated dc bus. For example, during sunlight operations, any load transients will cause the unregulated bus to drop from the solar-array voltage of 38 to 50 Vdc to battery voltage (28 V nominal). Poor transient response is attributable to a power source (or regulator) having high dynamic source impedance for a given step load change. For the recommended system, all loads will be powered from the regulated dc bus or the ac inverters. The transient response design task is common to all five model systems, requiring detailed knowledge of the transient behavior (current versus time) of the loads. The design task involves incorporating sufficient energy storage in the filters and fast enough dynamic response in the regulator (buck-boost) to prevent either the regulated dc bus or the ac bus from deviating excessively in voltage due to step load change. For improved transient response, voltage sensing should be as close to the source of step load changes as possible to minimize the delay times. Preliminary information on the loads indicates that the TWT converter (inrush of 5 to 6 amps) is the load causing the largest transient step load change. Proper filtering and response must be designed into the buck-boost regulator to maintain good power quality on the dc and ac buses. Because of the impact on the buck-boost design, it is strongly recommended that current-limiting be incorporated into the now existing TWT converter. TRW has incorporated current limiting with TWT converters on the Pioneer and Intelsat III spacecraft with a relatively few number of parts. Current-limiting is also desirable from the TWT standpoint, since it minimizes any voltage overshoot upon turn-on.

In summary, the transient response characteristics are common to all systems, each requiring detailed transient load characteristics and the appropriate design in the regulators.

7.7 SUMMARY

Based on the comparative analysis of the five model systems, the buck-boost approach (system No. 5) offers the greatest advantages in terms of simplicity, reliability, weight, and power utilization. The advantages and disadvantages of the other four competitive model power systems with respect to the recommended buck-boost system are delineated below.

System No. 1 disadvantages are as follows:

a. Requires two power-handling units source

b. Requires additional 10 lb at power-source conditioning

c. Greater complexity in providing current sharing between PWM, battery boost regulator, and battery charging.

d. Current limiting not as effective.

e. Higher number of parts and increased test and manufacturing costs.

System No. 1 advantages are as follows:

a. Slightly better solar array power utilization (1%).

b. Elimination of battery discharge diodes and momentary booster.

System No. 2 disadvantages are as follows:

a. Requires two power-handling units

b. Requires an additional 9 to 15 lb of power source conditioning

c. Heat dissipation is very high

d. Will probably require power transistors and power dissipating resistors to be mounted on panels

e. Testing of shunt elements in high-dissipation mode

f. Current limiting not as effective

g. Higher number of parts and increased test and manufacturing costs

System No. 2 advantages are as follows:

a. Inherent reliability in active shunt through use of component redundance

b. Active shunt regulator performance has been thoroughly demonstrated

c. Low output impedance

d. No electromagnetic interference

System No. 3 disadvantages are as follows:

a. Requires two power-handling units

b. Requires additional weight (6 lb)

c. Higher failure rate due to zener limiter

d. No current limiting

e. Wide tolerance of zener limiting voltage

System No. 3 advantages are as follows:

a. System has been designed and flown on previous Mariner spacecraft

System No. 4 disadvantages are as follows:

a. Requires two power-handling units

b. Requires additional weight ($\geq$9 to 15 lb)

c. No current limiting

d. Higher manufacturing and test costs and more parts

e. Transient heat dissipation in shunt limiter

System No. 4 advantages are as follows:

a. Higher solar array power utilization (1.8%)

b. Demonstrated circuit designs

7.8 SYSTEM RELIABILITY ASSESSMENTS

Reliability assessments have been made on the five model systems, including the existing Mariner system. Detailed assessments, including the assumptions and guidelines, are presented in Appendixes A, B, and C. Table 7-4 presents the system reliabilities for a 1-yr mission with the same degree of redundancy as in the existing system, i.e., redundancy in the main power-handling components. Several conclusions have been derived from the system reliability assessment analysis, namely:

a. For a 1-yr mission, incorporation of redundancy in a regulator (boost, buck-boost, PWM, etc.) will generally result in regulator reliabilities of ~ 0.999 based on the assumed component failure rates.

b. The maximum system reliability is limited by the Ag-Zn battery reliability assessment of 0.9538.

c. The unreliability of the Mariner system is largely attributable to the zener limiter (0.9271). Replacement of the zener with a redundant shunt limiter (0.999) will raise the Mariner system reliability from (0.8544) to 0.922).

d. Since the system reliability of the model system (redundancy in the primary power-handling units only) results in reliability assessments of 0.922 to 0.928 and the upper limit is constrained by the battery (0.9538), any further redundancy in the power conditioning and control circuitry will not result in significant improvements from a reliability assessment viewpoint. However, redundancy can be incorporated in critical low-level control circuitry with low attendant weight and efficiency penalties, thus increasing the overall confidence in achieving successful operation. It also minimizes the chances of a single component failure in a critical circuit to cause a mission failure.

7.8.1 Weight-Reliability Tradeoffs

The major area of reliability improvement (exclusive of the zener limiter) is in the battery configuration. Reliability analysis (reference Appendix C) shows that two parallel batteries will increase the battery (including the charge control) reliability from 0.9538 to 0.9917. This is based on the following assumptions:

a. For the one-battery configuration:

1. 18 cells in series

2. 50 A-H nominal, capacity

3. 300-bit failure rate/cell for maximum depth of discharge of 50%

4. Failure criteria (one cell failure constitutes a battery failure).

Table 7-4. Reliability Assessments

	Reliability (1 Yr)	Comments
Zener and boost line regulator (Mariner system)	0.8554	Unreliability in zener limiter
Shunt limiter and boost line regulator	0.9251	
PWM array control and battery boost regulator	0.928	Eliminates momentary booster
Shunt limiter and battery boost regulator	0.928	Eliminates momentary booster
Buck-boost line regulator	0.925	

b. For the two-battery configuration:

1. Two batteries in parallel, 18 cells/battery
2. Nominal capacity of 25 A-H
3. Each battery has the capability to support the maximum load (refer to Section 3 for battery energy analysis)
4. Assumed 600-bit failure rate/cell since in a failure mode, the remaining battery will be stressed more than a single battery
5. Failure criteria (one cell failure in each battery constitutes a failure)

The additional weight increase for the two-battery configuration is estimated as follows:

a. Cell weight 3.5 lb

b. Chassis weight 0.9 lb

c. Battery charge/discharge control 1.7 lb

For an additional 6.1 lb, the reliability for the recommended system will be increased from 0.925 to 0.964. Table 7-5 shows the effect of reliability and weight for various degrees of redundancy in the Mariner system and for the recommended buck-boost system. A reliability versus weight plot (based on Table 7-5) is depicted in Figure 7-7.

7.9 OPTIMUM INVERTER SWITCHING FREQUENCY

The effect of different squarewave inverter-operating frequencies on power subsystem characteristics (weight and efficiency) was determined to check whether the present frequency of 2.4 kHz represents an optimum choice. In addition, the impact of faster switching times in the inverter power transistors on these same characteristics was also determined. Power conditioning, weight, and efficiency

Table 7-5. Summary of Weight and Reliability--Mariner System and Recommended System

POINT ON CURVE	CONFIGURATION	POWER CONDITIONING WEIGHT (INCLUDING ZENER LIMITER)	RELIABILITY	TOTAL SYSTEM WEIGHT
1	EXISTING DESIGN (NO REDUNDANCY IN POWER CHAIN)	34.67	0.8209	108.67
2	EXISTING DESIGN	43.73	0.8544	117.73
3	EXISTING DESIGN (PLUS REDUNDANT BATTERY)	45.73	0.887	124.13
4	RECOMMENDED DESIGN (LESS REDUNDANCY IN BUCK-BOOST, 2.4 KHz INVERTER AND CONTROL CIRCUITRY)	28	0.88	102
5	RECOMMENDED DESIGN (SINGLE BATTERY)	33.67	0.925	109.67
6	RECOMMENDED DESIGN (REDUNDANT BATTERIES)	35.37	0.9706	113.77

data, generated in the course of a recent NASA study*, were utilized in both these assessments along with a few assumptions regarding inverter operation. These assumption are:

a. Equal transistor ON and OFF switching times

b. Effects of transformer leakage reactance and winding capacitance on inverter transistor switching are neglected

c. Symmetrical overlapping of transistor currents and voltages during switching periods are assumed

d. Resistive load is assumed for inverter

e. Inverter central circuit losses are neglected

*"Analysis of Aerospace Power Conditioning Component Limitations," prepared for NASA Headquarters by TRW Systems under Contract NAS 7-546, 1968 June 30.

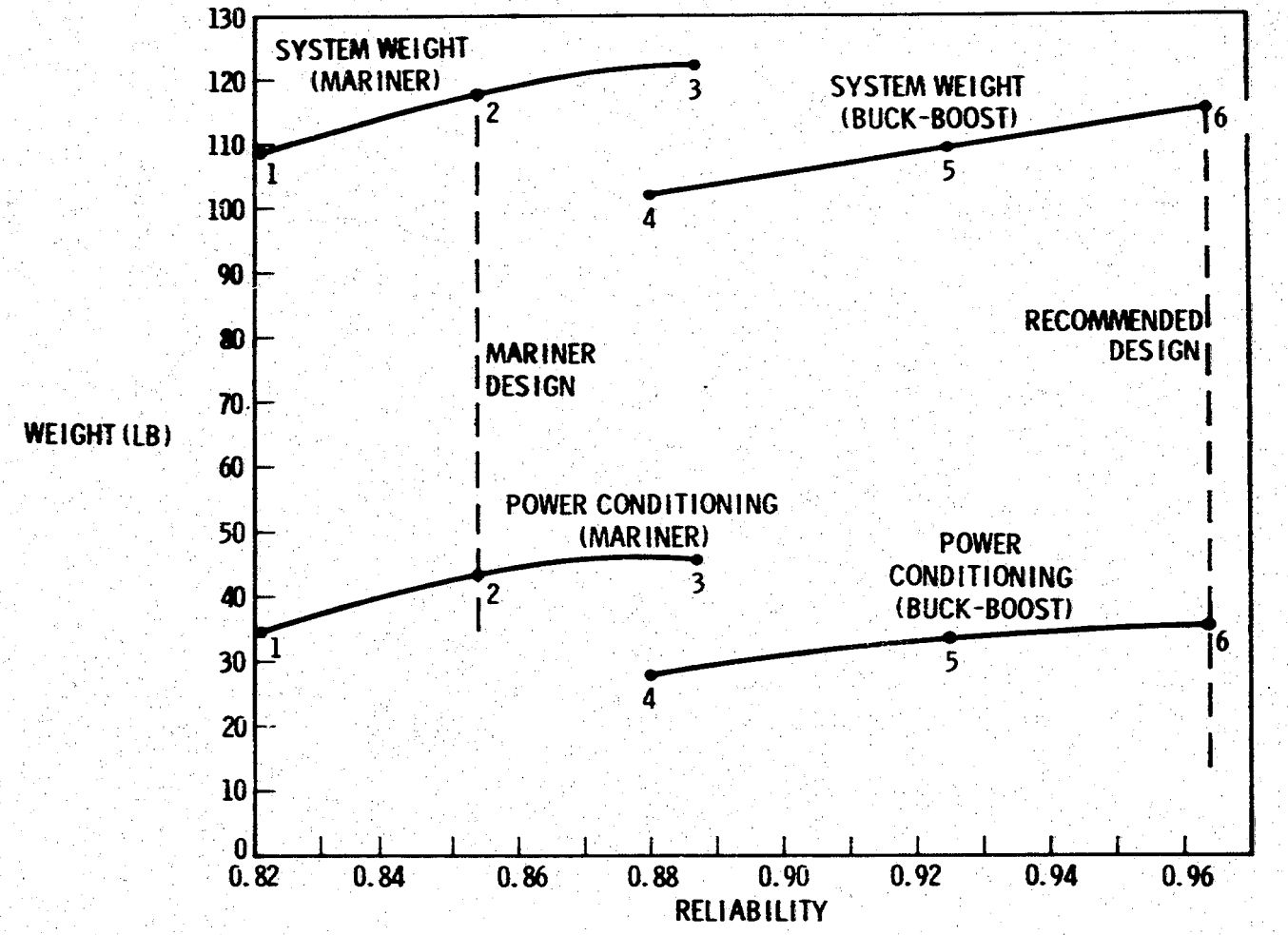


Figure 7-7. Weight-Reliability Characteristics of Mariner and Recommended System Design

The condition for optimum inverter switching frequency is that resulting in a minimum power subsystem weight. For purposes of the following analysis, power subsystem weight, W_o, is specially defined as

$$W_o = W_I + KP_I \tag{7-6}$$

where W_I represents the weight in pounds of major inverter components, including transistor heat sink weight, P_I represents total inverter power loss in watts, and K is the power source (solar array) power density in pounds per watt (assumed here as 0.2 lb/W).

In determining optimum frequency on the basis indicated, the following transistor parameters and circuit operating conditions are selected:

Output power = 200 W

Input voltage = 50 V = E in.

Output voltage = 50 V peak

Maximum collector current = 4 amps = I_c

Collector-emitter saturation voltage = 0.4 V = V_{CES}

Base-emitter saturation voltage = 0.9 V = V_{BES}

Minimum transistor current gain = 10 = β

Transistor ON time (or OFF time) = 1.0 μs = t_{SW}

The following relations for transistor power loss (conduction, drive, and switching) apply:

$$P_{on} = \frac{VCE_S\, I_C}{2} \tag{7-7}$$

$$P_{Drive} = V_{BES} \frac{I_c}{\beta} \tag{7-8}$$

$$P_{SW} = \frac{2E_{in}\, I_C\, t_{SW}}{3T} \tag{7-9}$$

(T = period of switching frequency)

In Table 7-6, both the transistor and transformer losses and weights are indicated for switching frequencies of 1.0, 2.4, 5, and 10 kHz. The transformer weight and loss figures (W_x, P_x) and the transistor (with heat sink) weight figures were taken from the referenced study. Also indicated are the corresponding values of total inverter weight W_I, as previously defined, and W_o, power subsystem weight. As seen, a minimum W_o is obtained at 5 kHz. In terms of the overall or absolute power subsystem weight, the improvement actually realized by designing for 5 kHz rather than 2.4 kHz is slight when considering the inverter only. Additional component weight savings, though, would accrue in downstream equipment operating at a higher frequency.

Table 7-6. Transistor and Transformer Losses and Weights (1 μsec Switching)

Power Loss, (W)						Weight, (lb)			
Frequency (kHz)	P_{on}	P_{Drive}	P_{sw}	P_x	P_{total}	Transistor and Heat Sink	Transformer W_x	W_I	W_o
1.0	0.8	0.36	0.13	13.4	14.7	0.34	0.42	0.76	3.7
2.4	0.8	0.36	0.32	9.4	10.9	0.39	0.25	0.64	2.82
5.0	0.8	0.36	0.67	7.4	9.2	0.495	0.185	0.68	2.53
10.0	0.8	0.36	1.33	6.9	9.4	0.685	0.15	0.835	2.72

The impact of slower transistor switching speeds can be shown both in terms of inverter efficiency and in the effect on power subsystem weight. For an operating frequency of 2.4 kHz, the inverter losses for 1 and 5 μsec switching times, respectively, are 10.9 and 12.2 W. The 1-μsec switching case yields an inverter efficiency improvement of approximately 0.6% as compared with the 5 μsec case. The saving in required power-source weight, as shown by the W_o figures in Table 7-7 amounts to only 0.29 lb.

Table 7-8 shows the effects of loss and weight for a 5-μsec rise/fall time; the 2.4-kHz frequency is shown to be near optimum.

Table 7-7. Required Power-Source Weight

Power Loss, (W)						Weight (lb)			
tsw, μsec	P_{on}	P_{Drive}	P_{sw}	P_x	P_{total}	Transistor and Heat Sink	W_x	W_I	W_o
1.0	0.8	0.36	0.32	9.4	10.9	0.39	0.25	0.64	2.82
5.0	0.8	0.36	1.6	9.4	12.2	0.42	0.25	0.67	3.11

Table 7-8. Transistor and Transformer Losses and Weights (5 μsec Switching)

Power Loss, (W)						Weight (lb)			
Frequency	P_{on}	P_{Drive}	P_{sw}	P_x	P_{total}	Transistor and Heat Sink	Transformer W_x	W_I	W_o
1.0	0.8	0.36	0.65	13.4	15.25	0.48	0.42	0.9	4.3
2.4	0.8	0.36	1.6	9.4	12.2	0.8	0.25	1.05	3.49
5.0	0.8	0.36	3.35	7.4	11.92	1.3	0.185	1.485	3.79
10.0	0.8	0.36	6.65	6.9	14.71	2.0	0.15	2.15	5.1

7.10 CONCLUSIONS

The minimum power subsystem weight occurs at a switching frequency of 5 kHz for 1 μs rise/fall time constraint. The overall weight advantage, however, is relatively small (0.29 lb). Accounting for input filter, weight, and assumed battery power source density (0.1 lb/W), the overall weight advantage compared to the 2.4 kHz frequency is approximately 0.5 lb. Additional weight savings will be accrued in the load transformer-rectifier-filter units.

With no rise/fall time constraints, optimum switching frequencies for the inverter and system are estimated to be about 10 Kc, resulting in further reduction of load transformer-rectifier-filter units.

For rise/fall time of 5 μsec, 2.4 kHz appears to be near optimum.

8. FAILURE MODES AND EFFECTS ANALYSIS

The following subsections report on the element and system failure mode and effects analysis, as well as methods of failure protection and reliability improvement. In general, an element is defined in this report as a major power system function such as a boost line regulator, solar array, battery charger, etc.

8.1 ELEMENT FAILURE AND EFFECTS

Each of the major elements constituting a power system configuration has been analyzed for its failure modes. The possible failure modes of the element and the causes of the failures, as related to internal major parts and circuit functions, have been identified. In general, the component/circuit failure modes are classified as open circuits, short circuits, or degraded performance. The method of detection of these failures and means by which redundancy can be provided have also been defined. Table 8-1 presents in tabular form the element failure analysis for the existing Mariner system. Schematics of key representative circuits which were analyzed are presented in Figures 8-1 through 8-7. Table 8-2 summarizes the results of the analysis.

8.2 SYSTEM FAILURE AND EFFECTS

After the element failure analysis was completed, the functional elements making up a power system were analyzed to determine the failure effects of a given element upon an adjacent functional element. This analysis was then expanded to define the propagation throughout the power system, including the power interface to the spacecraft user equipment.

The functional elements were assumed to have failed in each of the modes presented in the element failure list (Table 8-1). The effects of these failures as manifested at the input and output terminals of that functional element were tabularized. The parameters considered as providing significant information about the failure were: input voltage, input current, input power, percent regulation of the input voltage, and percent ripple on the input voltage. The effect of one element failure within the power system is identified by its effect on the remaining functional elements and total equipment circuit. An example of this detailed failure effects analysis is shown in Table 8-3.

The left-hand column of Table 8-3 (under "No." heading) lists the major elements and the failure modes associated with each element. The failure mode identification is consistent with that delineated in Table 8-1. The effect of the failure on each of these related elements is noted in the body of the table, using six symbols or combinations thereof. The (+) and (-) symbols indicate that the magnitude of that parameter increased or decreased, respectively. The large "C" and "F" and small "f" indicate the degree of the change as noted in the legend. A "0" indicates that the change did not exceed normal operating limits. A combination of symbols, such as "0/+F" was used when the change in that parameter depended upon the operating conditions of the circuit and could fall anywhere within the indicated range.

Since the output parameters of each element are also the input parameters for the following element, only the input parameters (except for solar array and battery where output parameters are tabularized) are shown in the column, "Effect on Related Elements."

The effect on the power system outputs, namely, unregulated dc, regulated 56 Vdc, 2.4 kHz, 10, 30 400 Hz, load capability in sunlight, and load capability during maneuver (battery operation) are delineated in the column, "Effect on System Performance."

Table 8-1. Failure Modes and Effects Analysis – MM '69 Power System

UNIT	NO.	FAILURE MODE	FAILURE CAUSE	METHOD OF DETECTION	REDUNDANCY PROVISION	COMMENTS
Solar Array	1.	String open	Wire or connection open	DC level sensor ($Z \rightarrow \infty$)	Multiple strings	
	2.	String short	Solar cell or diode (anode) to ground short or string + to - short (wire)	DC level sensor ($Z \rightarrow 0$)	Multiple strings with blocking diode	
	3.	Multiple strings open (mom. booster disabled)	Same for string	DC level sensor ($Z \rightarrow \infty$)	Multiple strings	
	4.	Multiple strings short (mom. booster disabled	Same for string	DC level sensor ($Z \rightarrow 0$)	Multiple strings with blocking diode	
	5.	Strings open or short (mom. booster enabled)	Same for string	DC level sensor	Multiple strings	
	6.	Illumination low	Spacecraft misorientation	Sun angle sensor	Attitude control system	
	7.	Array temp. high	Poor prediction	Temp. sensor	Not applicable	
	8.	Array temp. low	Poor prediction	Temp. sensor	Not applicable	
Array Control	1.	Voltage limiting open	Zener(s) open or drift to high voltage	DC level sensor	Multiple strings in parallel to minimize effects of zener(s) open or drift	
	2.	Voltage limiting short	Zener(s) short or mechanical short (e.g. at connector or positive to negative)	DC level sensor	Multiple strings in parallel to minimize effects of shorted zener and multiple series zeners for each string	
	3.	No solar array power	Main bus open (mechanical failure), zeners short, blocking diodes open	Solar array current	Multiple wires, zener, blocking diodes	
	4.	Unreg. bus short	Short (mechanical or cathode to ground short, blocking diode)	Current sensor	Multiple wiring, isolation of blocking diode	

Table 8-1. Failure Modes and Effects Analysis – MM '69 Power System (Cont)

UNIT	NO.	FAILURE MODE	FAILURE CAUSE	METHOD OF DETECTION	REDUNDANCY PROVISION	COMMENTS
Array Control (continued)	5.	Loss of string power	Blocking diode open	String current	Parallel diodes	Same effect as "Solar Array 1,2"
	6.	Loss of string isolation	Blocking diode short	Volt. differential sensor	Series diode	None unless string shorts
Battery	1.	Loss of battery power	Cell open	Battery current sensor	Parallel battery	
	2.	Decrease in battery voltage	Shorted cell	Battery voltage	Additional series cell	
	3.	Battery voltage decrease to 0	Shorted cells or mechanical failure	Battery current	None	Incorporate good mechanical design
Discharge Diode	1.	Loss of blocking function	Shorted diode	Voltage differential sensor	Series	
	2.	Loss of battery discharge power	Open diode	Discharge current	Parallel	
Kinetic Switch	1.	Loss of battery discharge power	Open switch	Discharge current	Parallel	
Filter	1.	Loss of Solar Array Current	L1 open	Solar array current	Parallel	
	2.	Excessive ripple	L1 short	Ripple current	Series	
	3.	Excessive ripple	C10, C11 open	Ripple current	Parallel/quad	
	4.	Zero voltage input	Shorted capacitors	Fuse	Series/quad	
Battery Charger	1.	No output current nor voltage (input current low)	a) Loss of drive power b) Loss of or erroneous error signal from diff. amp c) Open series element (transistor, resistor, diode) d) *K2 relay coil or relay driver failure	Not Practical (NP) NP Current TLM	Quad Majority voting Parallel or standby Quad	*or failed comman

Table 8-1. Failure Modes and Effects Analysis – MM '69 Power System (Cont)

UNIT	NO.	FAILURE MODE	FAILURE CAUSE	METHOD OF DETECTION	REDUNDANCY PROVISION	COMMENTS
Battery Charger (continued)	2.	Output voltage low (input current normal)	a) Inadequate base drive	Not practical (NP)	Quad	
			b) Drift in diff.-amp	NP	Majority voting Series	
	3.	No outut current or voltage (input current excessive)	a) Input capacitor(s) short	Fuse	Quad or use of fuses to clear short	
	4.	Output current high	a) Current limiter open	NP	Parallel	
	5.	Output voltage high	a) Excessive base drive	NP	Quad	
			b) Failure in diff. amp	NP	Majority voting	
	6.	No output, impedance low	Output capacitors short	Fuse	Series or quad	
	7.	Loss of battery charger off	*K2 relay coil or Driver failure	TLM	Quad	*Includes command failure
Momentary Booster	1.	No output	a) *K3 relay coil or driver failure	TLM	Quad	
			b) Share mode detector and logic failure	TLM	Majority voting	
			c) K1 relay coil or driver	TLM	Quad	
			d) Oscillator open	TLM	Standby	
			e) Power stage failure (power transistors short or open, transformer open or short)	TLM	Standby	
			f) Fuse open or output resistor (R35) open	Current	Parallel	
	2.	Input current pulse high	a) Shorted transformer or open or shorted power transistors or output diodes short	Current	Standby	

Table 8-1. Failure Modes and Effects Analysis – MM '69 Power System (Cont)

UNIT	NO.	FAILURE MODE	FAILURE CAUSE	METHOD OF DETECTION	REDUNDANCY PROVISION	COMMENTS
Momentary Pooster	3.	Continuous Output	a) Duty cycle control failure in ON state	Current and TLM	Majority voting	
			b) Relay K1 failure in ON state	TLM	Quad	
Main Boost Regulator	1.	Low Output	a) Loss of drive	NP	Quad/majority voting	
			b) Transformer open/short	Current	Standby	
			c) Transistor open/short	Current	Standby	
			d) K1 relay open	TLM	Quad	
			e) Output capacitor short	Current/fuse	Quad	
			f) Free-wheeling diode short	Current/fuse	Series/quad	
			g) Output inductor open	Current	Parallel	
			h) Diff. amp. failure	N.P.	Majority voting	
			i) Loss of 20 volt regulator	Voltage	Quad	
	2.	High Output	a) Drive excessive	NP	Quad	
			b) Diff. amplifier failure	NP	Majority voting	
	3.	Excessive Input Current	a) Power transistor(s) open/short	Current	Standby	
			b) Power transformer current short	Current	Standby	
			c) Output capacitor short	Fuse	Series	
			d) Input capacitor short	Fuse	Series	
	4.	Excessive Output Ripple Voltage	a) Output inductor short	Current	Series	
			b) Input capacitor open	N.P.	Parallel	
2.4 KHz Inverter	1.	No Output Voltage ($\frac{1}{t} \rightarrow \infty$)	a) Loss of drive	N.P.	Standby	
	2.	No Output Voltage ($\frac{1}{t} \rightarrow 0$)	a) Power inverter stage short	Current	Standby	
			b) Transformer open/short	Current	Standby	
	3.	High Output Voltage	a) High input voltage	Voltage	N.P.	
	4.	Loss of Frequency	a) Failure in crystal oscillator or in any counter	Frequency detector	Standby or operating	

Table 8-1. Failure Modes and Effects Analysis – MM '69 Power System (Cont)

UNIT	NO.	FAILURE MODE	FAILURE CAUSE	METHOD OF DETECTION	REDUNDANCY PROVISION	COMMENTS
Failure Sensor	1.	Fails ON (causes switchover to standby)	a) Failure in frequency, voltage, or time delay circuits	TLM	Quad and majority voting	
			b) K1 relay or relay driver failure	TLM	Quad	
	2.	Fails off (doesn't switch in event of failure)	a) Failure in frequency, voltage, or time delay circuits	TLM	Quad and majority voting	
			b) K1 relay or relay driver failure	TLM	Quad	
1ø, 3ø 400 Hz Inverter	1.	No output (2→00)	a) Loss of sync.	Voltage	Standby	
			b) Loss of internal regulated power	Voltage	Standby	
			c) Open transformer	Current	Quad	
			d) Relay K1 or K2 open	TLM	Series	
	2.	No output (2→0)	a) Input capacitor short	Fuse	Standby	
			b) Power transistors short	Current	Standby	
			c) Output transformer short	Current	Standby	
1ø, 3ø 400 Hz Inverter	3.	Frequency change	a) Failure in binary counter	Frequency detector	Quad or series/ parallel	Refer to schematic "Heater and Power Distributio 4A19"
Power Switching	1.	Failure to set relay	a) R1,R4,C2,Q1,CR1,CR3 open	TLM		
			b) C1,C2,Q1,CR4 short			
			c) +30 vdc low			
			d) Set coil open			
			e) Contact fail in reset position			
			f) Command fails			
	2.	Failure to reset relay	a) R5,R7,C3,Q2,CR6, CR7 open	TLM	Quad or series/ parallel	
			b) C3,C4,Q2,CR5 short			
			c) +30 vdc low			
			d) Reset coil open			
			e) Contact fails in set position			
			f) Command fails			

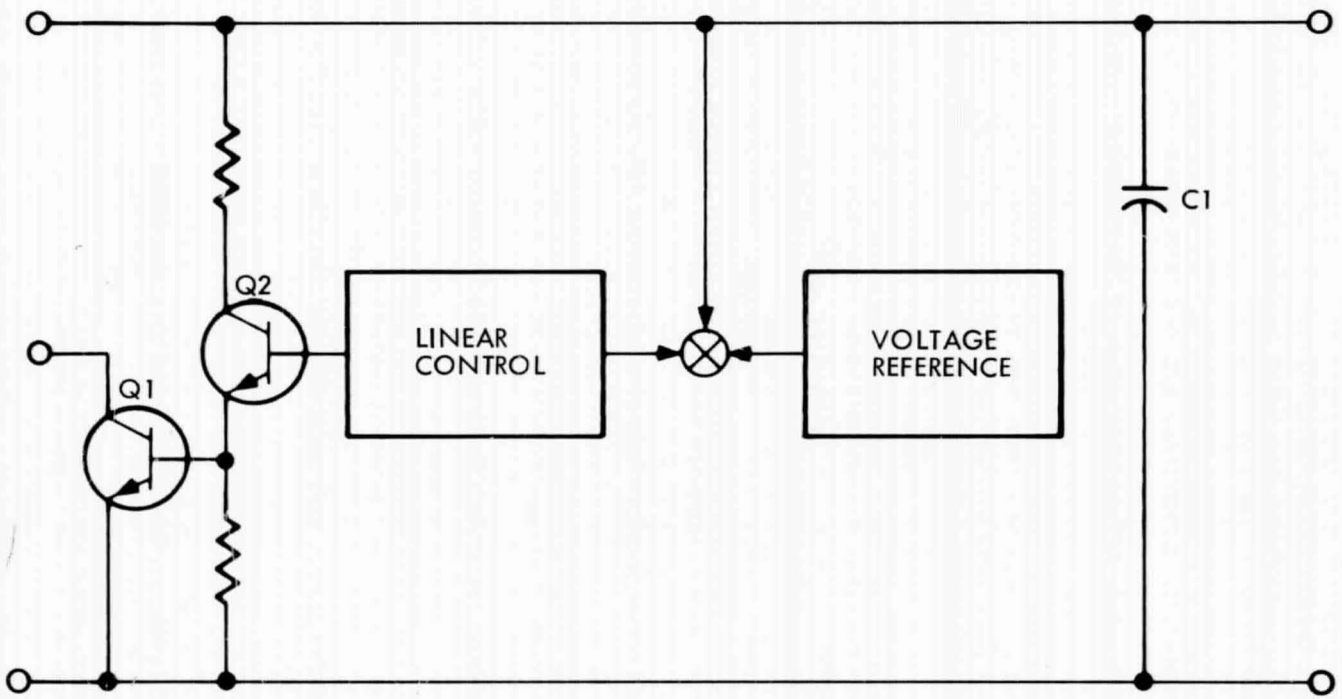


Figure 8-1. Active Shunt Limiter or Regulator, Baseline Schematic

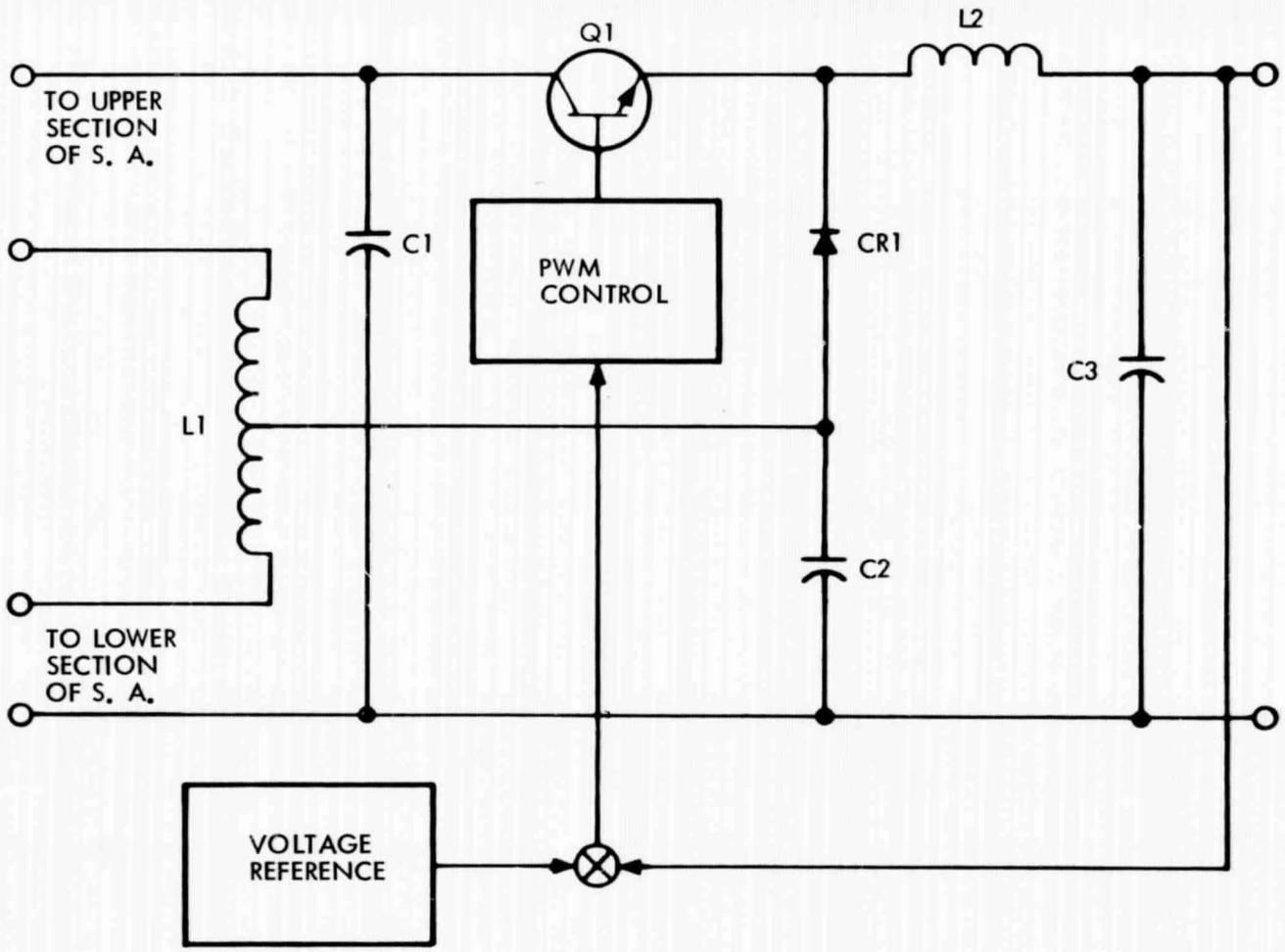


Figure 8-2. PWM Quasi-Buck Series Regulator, Baseline Schematic

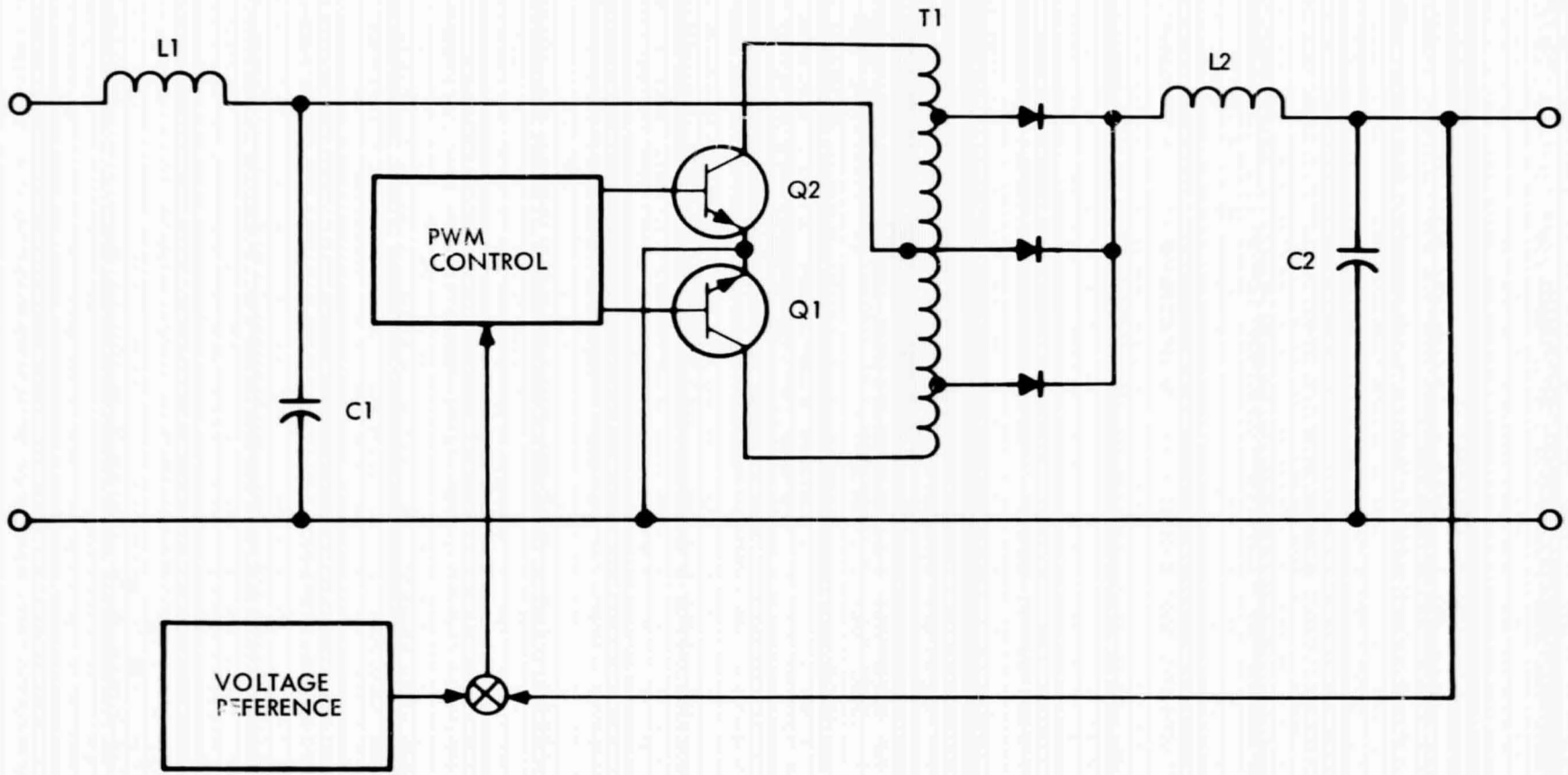


Figure 8-3. Pulse Width Modulated Boost Line Regulator, Baseline Schematic

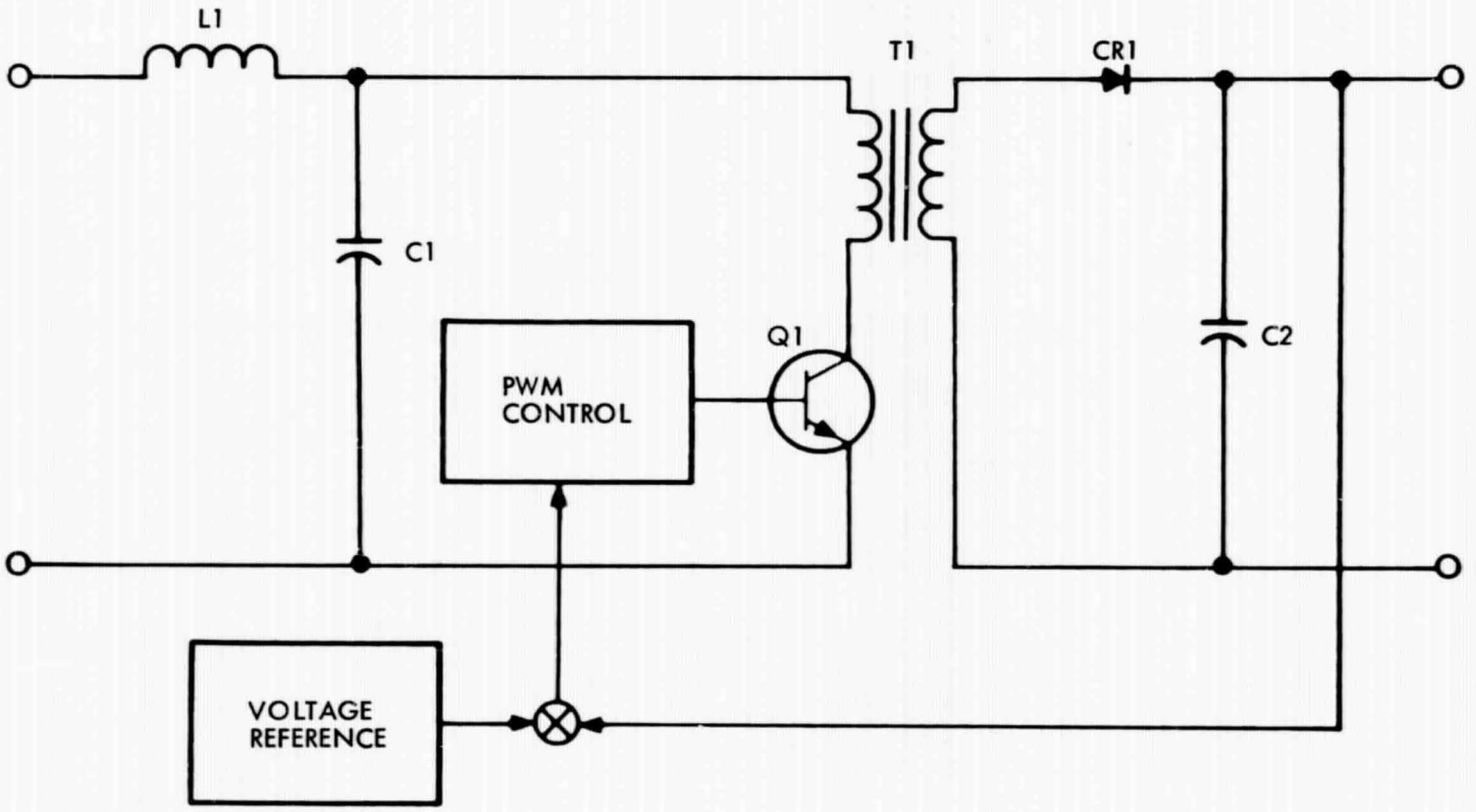


Figure 8-4. Pulse Width Modulated Buck-boost Regulator, Baseline Schematic

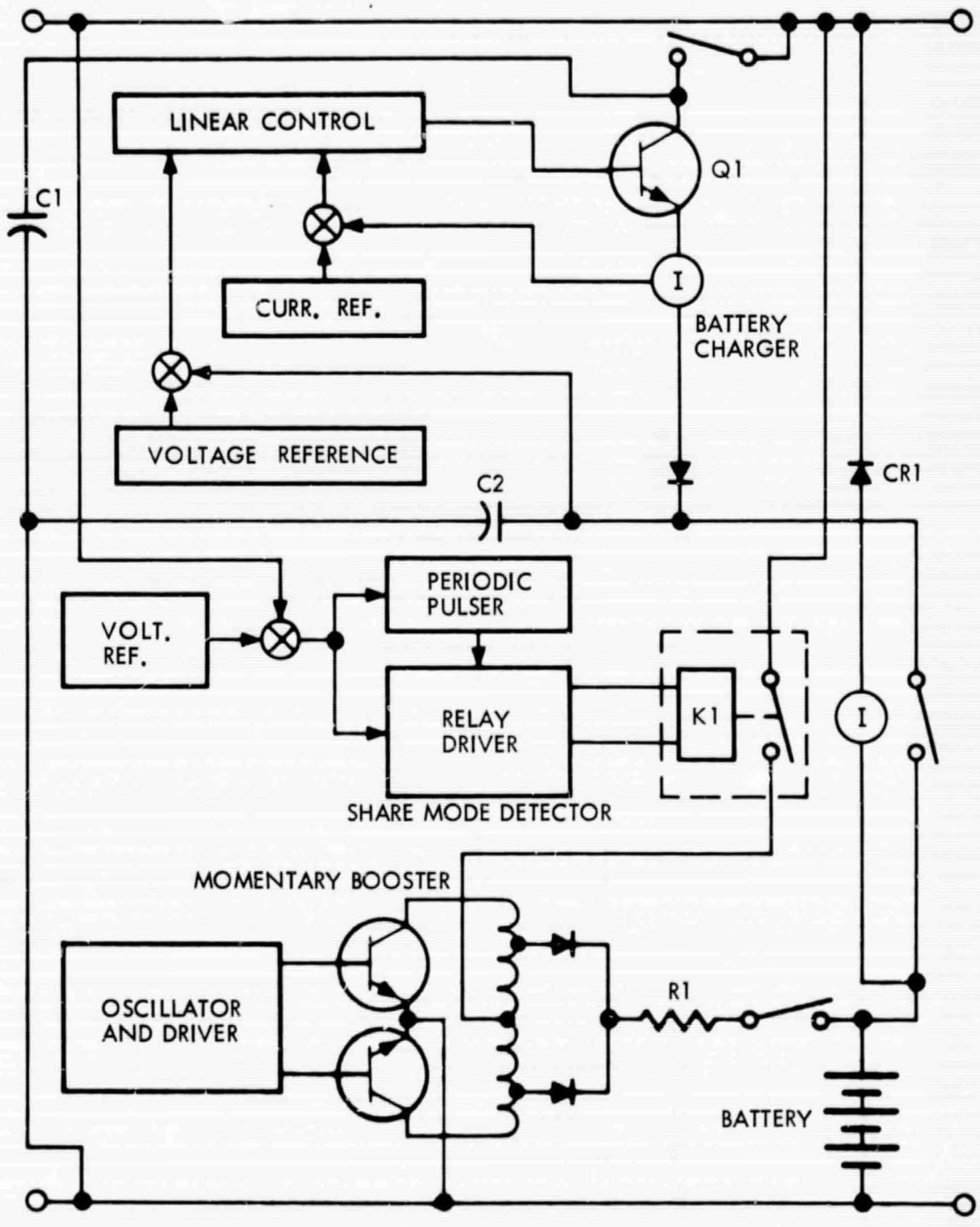


Figure 8-5. Dissipative Battery Charger, Momentary Booster, Baseline Schematic

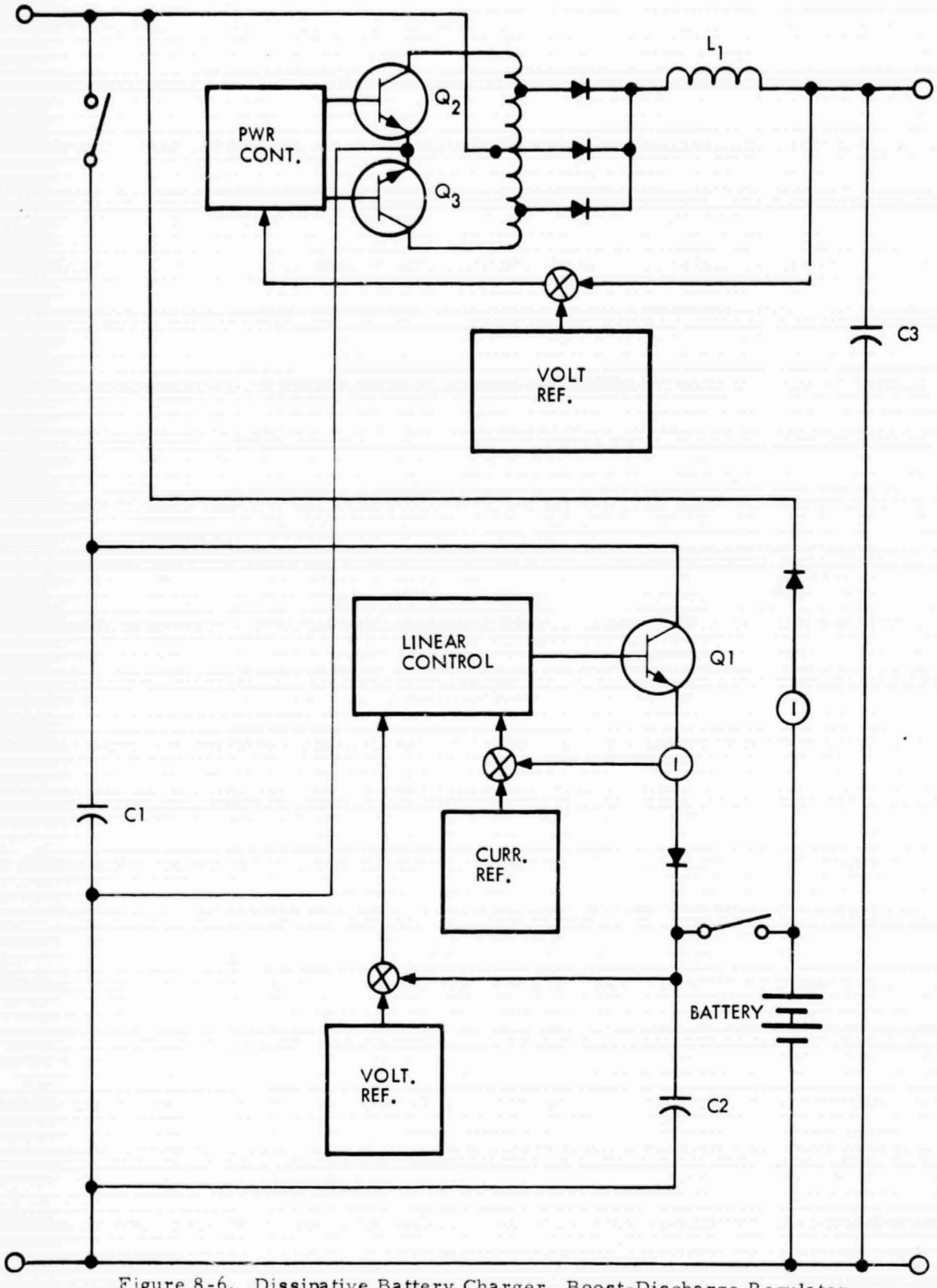


Figure 8-6. Dissipative Battery Charger, Boost-Discharge Regulator Baseline Schematic

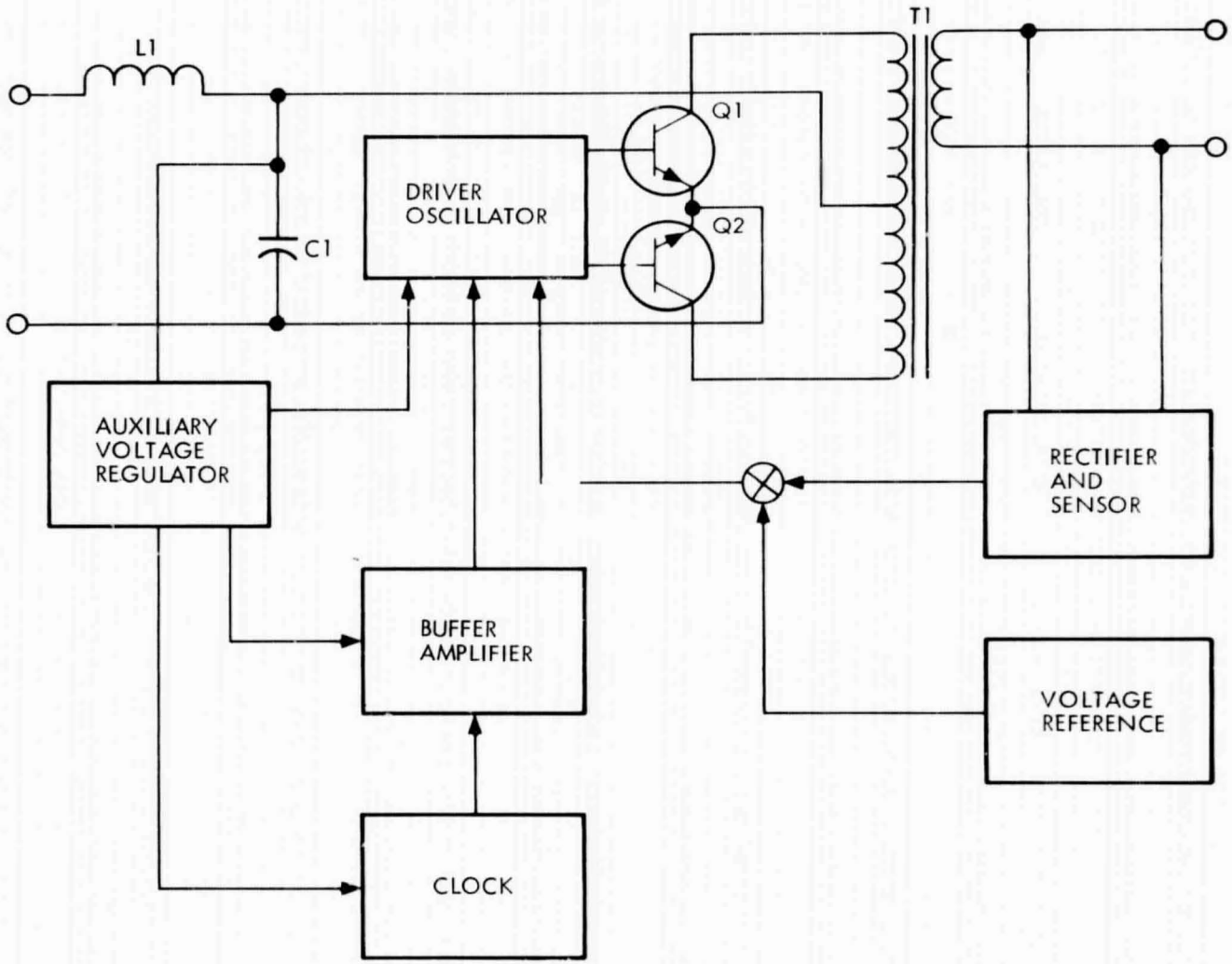


Figure 8-7. 2.4 kHz Inverter, Baseline Schematic

ELEMENT	FAILURE MODE	FAILURE CAUSE	Solar Array Control	None	Zener Limiter	Shunt Limiter or Regulator
Excessive ripple (E or I), instability or inadequate response.						X
Low output signal (E or I).				X	X	
Loss of output signal and Zo → 0.					X	
Loss of output signal and Zo → ∞.						
High output signal (E or I).						
Loss of battery recharge capability.						
Loss of voltage regulation, or variation of the voltage limiting point.						X
Loss of share mode detection, or anomalies in the periodicity of the momentary discharge booster.						
Loss of frequency control.						
Loss of drive power						
Shorted power transistor						
Open input filter inductor						
Shorted input filter capacitor						
Shorted "commutating" diode						
Loss of signal through logic circuit						
Inadequate drive due to preamplifier malfunction						X
Shorted input filter inductor						
Open transformer or autotransformer						
Shorted transformer or autotransformer						
Open input filter capacitor						
Open "commutating" diode						
Shorted auxiliary diode, or limiting zener					X	
Open auxiliary diode, or limiting zener						X
Leakage degradation of limiting zener					X	
Inadequate input power				X		
Open power transistor						
Open output filter inductor						
Open output filter capacitor						
Shorted output filter inductor						

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Table 8-2. Summary of Failure Modes and Effects Analysis

CAUSE												METHOD OF DETECTION					REDUNDANCY PROVISIONS						
Open commutating diode	Shorted auxiliary diode, or limiting zener	Open auxiliary diode, or limiting zener	Leakage degradation of limiting zener	Inadequate input power	Open power transistor	Open output filter inductor	Open output filter capacitor	Shorted output filter inductor	Shorted output filter capacitor	Malfunction in time delay circuit	Malfunction in frequency control mechanism	Not applicable	Fuses	AC level sensor	DC level sensor	Timing mechanism	Derating of parts used in parallel (a)	Majority voting	Quad configuration	Standby redundancy	Building block redundancy with built-in open failure modes (b)	Not applicable	NOTES
				X											X							X	*
			X										X								X		
			X												X					X			
	X												X								X		
															X					X			
		X										X					X						
															X					X			
												X					X						
												X						X					
												X							X				
												X							X				
													X								X		
												X					X						
												X						X					
												X							X				
												X					X						
												X							X				
													X								X		
												X					X						
												X						X					
												X							X				
					X							X							X				
													X								X		

NOTES

(a) Applicable to parts that are expected to fail open.
(b) This assumes that the minimum power capability of the source powering the element is higher than the power capability of the building block.
(c) Certain combinations of methods of detection and redundancy provisions have been discarded. For instance, it would not be advisable to account for a shorted output capacitor by using a dc failure sensor and standby redundancy.
(d) One effective way to minimize the critical effects of a shorted inductor is to have two or three smaller inductors in series. This solution goes hand-in-hand with building block redundancy, and provides a strong incentive to obviate standby redundancy in many instances.
(e) The concept of "quad" has been extended to include capacitor banks configured so that each string has two capacitors in series, and rectifier redundancy (either quad, series, or parallel).
(f) Loss of solar array orientation.
(g) The significance of prescribing fusing-and-building-block redundancy to take care of an "open inductor" failure is that various PWM (or whatever the element might be) are assumed to be in parallel and power sharing is obtained by virtue of:
    1. Synchronized switching
    2. Using LC input and output circuits both as filters and as current equalizing impedances.
(h) Failure in a related element.
(i) Relay redundancy not included in this study.

*Second order malfunction, low illumination

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ELEMENT	FAILURE MODE	FAILURE CAUSE	Solar Array Control	PWM Buck Series Regulator
	Excessive ripple (E or I), instability or inadequate response.			X
	Low output signal (E or I).			
	Loss of output signal and Zo → 0.			
	Loss of output signal and Zo → ∞.			
	High output signal (E or I).			
	Loss of battery recharge capability.			
	Loss of voltage regulation, or variation of the voltage limiting point.			
	Loss of share mode detection, or anomalies in the periodicity of the momentary discharge booster.			
	Loss of frequency control.			
		Loss of drive power		
		Shorted power transistor		
		Open input filter inductor		
		Shorted input filter capacitor		
		Shorted "commutating" diode		
		Loss of signal through logic circuit		
		Inadequate drive due to preamplifier malfunction		
		Shorted input filter inductor		
		Open transformer or autotransformer		
		Shorted transformer or autotransformer		
		Open input filter capacitor		
		Open "commutating" diode		
		Shorted auxiliary diode, or limiting zener		
		Open auxiliary diode, or limiting zener		
		Leakage degradation of limiting zener		
		Inadequate input power		

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Table 8-2. Summary of Failure Modes and Effects Analysis (Cont)

								METHOD OF DETECTION					REDUNDANCY PROVISIONS						
Inadequate input power	Open power transistor	Open output filter inductor	Open output filter capacitor	Shorted output filter inductor	Shorted output filter capacitor	Malfunction in time delay circuit	Malfunction in frequency control mechanism	Not applicable	Fuses	AC level sensor	DC level sensor	Timing mechanism	Derating of parts used in parallel (a)	Majority voting	Quad configuration	Standby redundancy	Building block redundancy with built-in open failure modes (b)	Not applicable	NOTES
								X*					X						
								X						X					
								X							X				
										X						X			
									X								X		
								X							X				
									X								X		
				X						X						X			
									X								X		
			X					X							X				
									X								X		
								X					X						
								X						X					
								X							X				
X											X							X	
								X							X				
X									X								X		
								X							X				
									X								X		
					X			X							X				
									X								X		
								X					X						
								X							X				
									X								X		
											X					X			
									X								X		
	X										X					X			
									X								X		
		X									X					X			
									X								X		

NOTES

(a) Applicable to parts that are expected to fail open.
(b) This assumes that the minimum power capability of the source powering the element is higher than the power capability of the building block.
(c) Certain combinations of methods of detection and redundancy provisions have been discarded. For instance, it would not be advisable to account for a shorted output capacitor by using a dc failure sensor and standby redundancy.
(d) One effective way to minimize the critical effects of a shorted inductor is to have two or three smaller inductors in series. This solution goes hand-in-hand with building block redundancy, and provides a strong incentive to obviate standby redundancy in many instances.
(e) The concept of "quad" has been extended to include capacitor banks configured so that each string has two capacitors in series, and rectifier redundancy (either quad, series, or parallel).
(f) Loss of solar array orientation.
(g) The significance of prescribing fusing-and-building-block redundancy to take care of an "open inductor" failure is that various PWM (or whatever the element might be) are assumed to be in parallel and power sharing is obtained by virtue of:
    1. Synchronized switching
    2. Using LC input and output circuits both as filters and as current equalizing impedances.
(h) Failure in a related element.
(i) Relay redundancy not included in this study.

*Second order malfunction, low, illumination

FAILURE MODE	FAILURE CAUSE	ELEMENT	Solar Array Control	PWM Buck Series Regulator (cont)							PWM Quasi-Buck Series Regulator							
		Excessive ripple (E or I), instability or inadequate response.									X		X	X	X	X		
		Low output signal (E or I).															X	X
		Loss of output signal and Zo → 0.																
		Loss of output signal and Zo → ∞.																
		High output signal (E or I).		X	X													
		Loss of battery recharge capability.																
		Loss of voltage regulation, or variation of the voltage limiting point.				X	X	X										
		Loss of share mode detection, or anomalies in the periodicity of the momentary discharge booster.																
		Loss of frequency control.																
		Loss of drive power																
		Shorted power transistor		X														
		Open input filter inductor																
		Shorted input filter capacitor																
		Shorted "commutating" diode																
		Loss of signal through logic circuit																
		Inadequate drive due to preamplifier malfunction					X	X				X						X
		Shorted input filter inductor											X					
		Open transformer or autotransformer																
		Shorted transformer or autotransformer																
		Open input filter capacitor					X							X				
		Open "commutating" diode																
		Shorted auxiliary diode, or limiting zener																
		Open auxiliary diode, or limiting zener																
		Leakage degradation of limiting zener																

FOLDOUT FRAME 1

Table 8-2. Summary of Failure Modes and Effects Analysis (Cont)

									METHOD OF DETECTION					REDUNDANCY PROVISIONS						
Open power transistor	Open output filter inductor	Open output filter capacitor	Shorted output filter inductor	Shorted output filter capacitor	Malfunction in time delay circuit	Malfunction in frequency control mechanism			Not applicable	Fuses	AC level sensor	DC level sensor	Timing mechanism	Derating of parts used in parallel (a)	Majority voting	Quad configuration	Standby redundancy	Building block redundancy with built-in open failure modes (b)	Not applicable	NOTES
										X		X*					X	X		
									X					X						
									X						X					
										X						X		X		
									X					X						
									X						X					
									X							X		X		
	X								X							X				
										X								X		
									X					X						
									X						X					
									X							X				
											X						X			
										X								X		
									X							X				
										X								X		
			X								X						X			(c)
										X								X		(d)
	X								X							X				(e)
										X								X		
									X					X						
									X						X					
									X							X				
												X							X	(f)

NOTES

(a) Applicable to parts that are expected to fail open.
(b) This assumes that the minimum power capability of the source powering the element is higher than the power capability of the building block.
(c) Certain combinations of methods of detection and redundancy provisions have been discarded. For instance, it would not be advisable to account for a shorted output capacitor by using a dc failure sensor and standby redundancy.
(d) One effective way to minimize the critical effects of a shorted inductor is to have two or three smaller inductors in series. This solution goes hand-in-hand with building block redundancy, and provides a strong incentive to obviate standby redundancy in many instances.
(e) The concept of "quad" has been extended to include capacitor banks configured so that each string has two capacitors in series, and rectifier redundancy (either quad, series, or parallel).
(f) Loss of solar array orientation.
(g) The significance of prescribing fusing-and-building-block redundancy to take care of an "open inductor" failure is that various PWM (or whatever the element might be) are assumed to be in parallel and power sharing is obtained by virtue of:
    1. Synchronized switching
    2. Using LC input and output circuits both as filters and as current equalizing impedances.
(h) Failure in a related element.
(i) Relay redundancy not included in this study.

*Second order malfunction, low, illumination

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ELEMENT: Solar Array Control — PWM Quasi-Buck Series Regulator (cont)

FAILURE MODE	Excessive ripple (E or I), instability or inadequate response.												
FAILURE MODE	Low output signal (E or I).												
FAILURE MODE	Loss of output signal and Zo → 0.										X	X	X
FAILURE MODE	Loss of output signal and Zo → ∞.						X	X	X	X			
FAILURE MODE	High output signal (E or I).				X	X							
FAILURE MODE	Loss of battery recharge capability.												
FAILURE MODE	Loss of voltage regulation, or variation of the voltage limiting point.	X	X	X									
FAILURE MODE	Loss of share mode detection, or anomalies in the periodicity of the momentary discharge booster.												
FAILURE MODE	Loss of frequency control.												
FAILURE CAUSE	Loss of drive power									X			
FAILURE CAUSE	Shorted power transistor					X							
FAILURE CAUSE	Open input filter inductor								X				
FAILURE CAUSE	Shorted input filter capacitor												X
FAILURE CAUSE	Shorted "commutating" diode											X	
FAILURE CAUSE	Loss of signal through logic circuit												
FAILURE CAUSE	Inadequate drive due to preamplifier malfunction			X	X								
FAILURE CAUSE	Shorted input filter inductor												
FAILURE CAUSE	Open transformer or autotransformer												
FAILURE CAUSE	Shorted transformer or autotransformer												
FAILURE CAUSE	Open input filter capacitor		X										
FAILURE CAUSE	Open "commutating" diode												
FAILURE CAUSE	Shorted auxiliary diode, or limiting zener												
FAILURE CAUSE	Open auxiliary diode, or limiting zener												
FAILURE CAUSE	Leakage degradation of limiting zener												
FAILURE CAUSE	Inadequate input power												
FAILURE CAUSE	Open power transistor							X					
FAILURE CAUSE	Open output filter inductor						X						
FAILURE CAUSE	Open output filter capacitor	X											
FAILURE CAUSE	Shorted output filter inductor												

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Table 8-2. Summary of Failure Modes and Effects Analysis (Cont)

E CAUSE															METHOD OF DETECTION					REDUNDANCY PROVISIONS							
Open input [illegible]	Open "commutating" diode	Shorted auxiliary diode, or limiting zener	Open auxiliary diode, or limiting zener	Leakage degradation of limiting zener	Inadequate input power	Open power transistor	Open output filter inductor	Open output filter capacitor	Shorted output filter inductor	Shorted output filter capacitor	Malfunction in time delay circuit	Malfunction in frequency control mechanism	Not applicable	Fuses	AC level sensor	DC level sensor	Timing mechanism	Derating of parts used in parallel (a)	Majority voting	Quad configuration	Standby redundancy	Building block redundancy with built-in open failure modes (b)	Not applicable	NOTES	
													X							X		X			
													X	X								X			
										X			X	X						X		X			
													X	X				X				X			
													X	X						X		X			
														X		X					X	X			(g)
						X								X		X					X	X			
							X							X		X					X	X			
														X		X					X	X			
														X				X							
														X					X						
														X	X					X		X			
													X	X				X				X			
													X	X					X			X			
													X	X						X		X			
X													X	X						X		X			
									X				X	X						X		X			

NOTES

(a) Applicable to parts that are expected to fail open.
(b) This assumes that the minimum power capability of the source powering the element is higher than the power capability of the building block.
(c) Certain combinations of methods of detection and redundancy provisions have been discarded. For instance, it would not be advisable to account for a shorted output capacitor by using a dc failure sensor and standby redundancy.
(d) One effective way to minimize the critical effects of a shorted inductor is to have two or three smaller inductors in series. This solution goes hand-in-hand with building block redundancy, and provides a strong incentive to obviate standby redundancy in many instances.
(e) The concept of "quad" has been extended to include capacitor banks configured so that each string has two capacitors in series, and rectifier redundancy (either quad, series, or parallel).
(f) Loss of solar array orientation.
(g) The significance of prescribing fusing-and-building-block redundancy to take care of an "open inductor" failure is that various PWM (or whatever the element might be) are assumed to be in parallel and power sharing is obtained by virtue of:
    1. Synchronized switching
    2. Using LC input and output circuits both as filters and as current equalizing impedances.
(h) Failure in a related element.
(i) Relay redundancy not included in this study.

*Second order malfunction, low, illumination

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													Line Voltage Regulator Boost Type	ELEMENT	
									X	X	X	X	X	Excessive ripple (E or I), instability or inadequate response.	FAILURE MODE
			X	X	X	X	X	X						Low output signal (E or I).	FAILURE MODE
X	X	X												Loss of output signal and Zo → 0.	FAILURE MODE
														Loss of output signal and Zo → ∞.	FAILURE MODE
														High output signal (E or I).	FAILURE MODE
														Loss of battery recharge capability.	FAILURE MODE
														Loss of voltage regulation, or variation of the voltage limiting point.	FAILURE MODE
														Loss of share mode detection, or anomalies in the periodicity of the momentary discharge booster.	FAILURE MODE
														Loss of frequency control.	FAILURE MODE
														Loss of drive power	FAILURE CAUSE
														Shorted power transistor	FAILURE CAUSE
														Open input filter inductor	FAILURE CAUSE
		X												Shorted input filter capacitor	FAILURE CAUSE
	X													Shorted "commutating" diode	FAILURE CAUSE
														Loss of signal through logic circuit	FAILURE CAUSE
								X					X	Inadequate drive due to preamplifier malfunction	FAILURE CAUSE
												X		Shorted input filter inductor	FAILURE CAUSE
							X							Open transformer or autotransformer	FAILURE CAUSE
						X								Shorted transformer or autotransformer	FAILURE CAUSE
											X			Open input filter capacitor	FAILURE CAUSE
														Open "commutating" diode	FAILURE CAUSE
					X									Shorted auxiliary diode, or limiting zener	FAILURE CAUSE
				X										Open auxiliary diode, or limiting zener	FAILURE CAUSE
														Leakage degradation of limiting zener	FAILURE CAUSE
			X											Inadequate input power	FAILURE CAUSE
														Open power transistor	FAILURE CAUSE

FOLDOUT FRAME 1

Table 8-2. Summary of Failure Modes and Effects Analysis (Cont)

RE CAUSE															METHOD OF DETECTION						REDUNDANCY PROVISIONS						
Open "commutating" diode	Shorted auxiliary diode, or limiting zener	Open auxiliary diode, or limiting zener	Leakage degradation of limiting zener	Inadequate input power	Open power transistor	Open output filter inductor	Open output filter capacitor	Shorted output filter inductor	Shorted output filter capacitor	Malfunction in time delay circuit	Malfunction in frequency control mechanism	Not applicable	Fuses	AC level sensor	DC level sensor	Timing mechanism	Derating of parts used in parallel (a)	Majority voting	Quad configuration	Standby redundancy	Building block redundancy with built-in open failure modes (b)	Not applicable	NOTES	
												X*					X							
												X						X						
												X							X					
													X	X						X	X			
													X	X						X	X			
								X					X	X							X			
							X					X	X						X		X			
												X					X							
												X						X						
												X							X					
													X		X					X	X			
													X		X						X			
	X												X		X						X			
		X											X		X						X			
				X											X								(f) (h)	
													X	X					X		X			
												X	X						X		X			
									X			X	X						X		X			

NOTES

(a) Applicable to parts that are expected to fail open.
(b) This assumes that the minimum power capability of the source powering the element is higher than the power capability of the building block.
(c) Certain combinations of methods of detection and redundancy provisions have been discarded. For instance, it would not be advisable to account for a shorted output capacitor by using a dc failure sensor and standby redundancy.
(d) One effective way to minimize the critical effects of a shorted inductor is to have two or three smaller inductors in series. This solution goes hand-in-hand with building block redundancy, and provides a strong incentive to obviate standby redundancy in many instances.
(e) The concept of "quad" has been extended to include capacitor banks configured so that each string has two capacitors in series, and rectifier redundancy (either quad, series, or parallel).
(f) Loss of solar array orientation.
(g) The significance of prescribing fusing-and-building-block redundancy to take care of an "open inductor" failure is that various PWM (or whatever the element might be) are assumed to be in parallel and power sharing is obtained by virtue of:
    1. Synchronized switching
    2. Using LC input and output circuits both as filters and as current equalizing impedances.
(h) Failure in a related element.
(i) Relay redundancy not included in this study.

*Second order malfunction, low, illumination

FOLDOUT FRAME 2

ELEMENT	FAILURE MODE: Excessive ripple (E or I), instability or inadequate response.	FAILURE MODE: Low output signal (E or I).	FAILURE MODE: Loss of output signal and Zo → 0.	FAILURE MODE: Loss of output signal and Zo → ∞.	FAILURE MODE: High output signal (E or I).	FAILURE MODE: Loss of battery recharge capability.	FAILURE MODE: Loss of voltage regulation, or variation of the voltage limiting point.	FAILURE MODE: Loss of share mode detection, or anomalies in the periodicity of the momentary discharge booster.	FAILURE MODE: Loss of frequency control.	FAILURE CAUSE: Loss of drive power	FAILURE CAUSE: Shorted power transistor	FAILURE CAUSE: Open input filter inductor	FAILURE CAUSE: Shorted input filter capacitor	FAILURE CAUSE: Shorted "commutating" diode	FAILURE CAUSE: Loss of signal through logic circuit	FAILURE CAUSE: Inadequate drive due to preamplifier malfunction	FAILURE CAUSE: Shorted input filter inductor	FAILURE CAUSE: Open transformer or autotransformer	FAILURE CAUSE: Shorted transformer or autotransformer	FAILURE CAUSE: Open input filter capacitor	FAILURE CAUSE: Open "commutating" diode	FAILURE CAUSE: Shorted auxiliary diode, or limiting zener	FAILURE CAUSE: Open auxiliary diode, or limiting zener	FAILURE CAUSE: Leakage degradation of limiting zener	FAILURE CAUSE: Inadequate input power	FAILURE CAUSE: Open power transistor	FAILURE CAUSE: Open output filter inductor	FAILURE CAUSE: Open output filter capacitor	FAILURE CAUSE: Shorted output filter inductor
Line Voltage Regulator																													
Boost Type (cont)				X						X																			
				X								X																	
				X																		X							
					X											X													
							X									X													
							X																					X	
Buck Boost Type	X															X													
	X																X												
	X																			X									
	X																											X	
		X														X													
		X																								X			

Table 8-2. Summary of Failure Modes and Effects Analysis (Cont)

CAUSE												METHOD OF DETECTION					REDUNDANCY PROVISIONS						
Open auxiliary diode, or limiting zener	Leakage degradation of limiting zener	Inadequate input power	Open power transistor	Open output filter inductor	Open output filter capacitor	Shorted output filter inductor	Shorted output filter capacitor	Malfunction in time delay circuit	Malfunction in frequency control mechanism	Not applicable	Fuses	AC level sensor	DC level sensor	Timing mechanism	Derating of parts used in parallel (a)	Majority voting	Quad configuration	Standby redundancy	Building block redundancy with built-in open failure modes (b)	Not applicable	NOTES
										X					X						
										X							X				
											X								X		
											X		X					X	X		
				X							X		X					X	X		
										X					X						
										X						X					
										X							X				
										X					X						
										X						X					
										X							X				
										X					X						
										X						X					
										X							X				
												X						X			
												X						X			
										X							X				
										X					X						
										X						X					
										X							X				
		X											X							X	(f) (h)

NOTES

(a) Applicable to parts that are expected to fail open.
(b) This assumes that the minimum power capability of the source powering the element is higher than the power capability of the building block.
(c) Certain combinations of methods of detection and redundancy provisions have been discarded. For instance, it would not be advisable to account for a shorted output capacitor by using a dc failure sensor and standby redundancy.
(d) One effective way to minimize the critical effects of a shorted inductor is to have two or three smaller inductors in series. This solution goes hand-in-hand with building block redundancy, and provides a strong incentive to obviate standby redundancy in many instances.
(e) The concept of "quad" has been extended to include capacitor banks configured so that each string has two capacitors in series, and rectifier redundancy (either quad, series, or parallel).
(f) Loss of solar array orientation.
(g) The significance of prescribing fusing-and-building-block redundancy to take care of an "open inductor" failure is that various PWM (or whatever the element might be) are assumed to be in parallel and power sharing is obtained by virtue of:
    1. Synchronized switching
    2. Using LC input and output circuits both as filters and as current equalizing impedances.
(h) Failure in a related element.
(i) Relay redundancy not included in this study.

*Second order malfunction, low, illumination

FOLDOUT FRAME 2

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ELEMENT	FAILURE MODE: Excessive ripple (E or D), instability or inadequate response.	Low output signal (E or D).	Loss of output signal and Zo → 0.	Loss of output signal and Zo → ∞.	High output signal (E or D).	Loss of battery recharge capability.	Loss of voltage regulation, or variation of the voltage limiting point.	Loss of share mode detection, or anomalies in the periodicity of the momentary discharge booster.	Loss of frequency control.	FAILURE CAUSE: Loss of drive power	Shorted power transistor	Open input filter inductor	Shorted input filter capacitor	Shorted "commutating" diode	Loss of signal through logic circuit	Inadequate drive due to preamplifier malfunction	Shorted input filter inductor	Open transformer or autotransformer	Shorted transformer or autotransformer	Open input filter capacitor	Open "commutating" diode	Shorted auxiliary diode, or limiting zener	Open auxiliary diode, or limiting zener	Leakage degradation of limiting zener	Inadequate input power	Open power transistor	Open output filter inductor	Open output filter capacitor
Line Voltage Regulator																											
Buck Boost Type (cont)			X										X														
			X											X													
			X															X									
			X																								
				X						X																	
				X								X															
				X													X										
				X																X							
				X																					X		
					X											X											
					X																			X			
							X									X											
							X										X										

FOLDOUT FRAME 1

Table 8-2. Summary of Failure Modes and Effects Analysis (Cont)

CAUSE														METHOD OF DETECTION						REDUNDANCY PROVISIONS							
Open auxiliary diode, or limiting zener	Leakage degradation of limiting zener	Inadequate input power	Open power transistor	Open output filter inductor	Open output filter capacitor	Shorted output filter inductor	Shorted output filter capacitor	Malfunction in time delay circuit	Malfunction in frequency control mechanism	Not applicable	Fuses	AC level sensor	DC level sensor	Timing mechanism	Derating of parts used in parallel (a)	Majority voting	Quad configuration	Standby redundancy	Building block redundancy with built-in open failure modes (b)	Not applicable	NOTES	
										X							X		X			
										X							X		X			
											X		X					X	X			
							X			X							X					
										X					X							
										X							X		X			
											X		X					X	X			
											X		X					X	X			
			X								X		X					X	X			
										X					X							
										X						X						
										X							X					
		X											X							X	(h)	
										X					X							
										X						X						
											X		X					X	X			

NOTES

(a) Applicable to parts that are expected to fail open.
(b) This assumes that the minimum power capability of the source powering the element is higher than the power capability of the building block.
(c) Certain combinations of methods of detection and redundancy provisions have been discarded. For instance, it would not be advisable to account for a shorted output capacitor by using a dc failure sensor and standby redundancy.
(d) One effective way to minimize the critical effects of a shorted inductor is to have two or three smaller inductors in series. This solution goes hand-in-hand with building block redundancy, and provides a strong incentive to obviate standby redundancy in many instances.
(e) The concept of "quad" has been extended to include capacitor banks configured so that each string has two capacitors in series, and rectifier redundancy (either quad, series, or parallel).
(f) Loss of solar array orientation.
(g) The significance of prescribing fusing-and-building-block redundancy to take care of an "open inductor" failure is that various PWM (or whatever the element might be) are assumed to be in parallel and power sharing is obtained by virtue of:
    1. Synchronized switching
    2. Using LC input and output circuits both as filters and as current equalizing impedances.
(h) Failure in a related element.
(i) Relay redundancy not included in this study.

*Second order malfunction, low, illumination

ELEMENT	FAILURE MODE: Excessive ripple (E or I), instability or inadequate response.	Low output signal (E or I).	Loss of output signal and Zo → 0.	Loss of output signal and Zo → ∞.	High output signal (E or I).	Loss of battery recharge capability.	Loss of voltage regulation, or variation of the voltage limiting point.	Loss of share mode detection, or anomalies in the periodicity of the momentary discharge booster.	Loss of frequency control.	FAILURE CAUSE: Loss of drive power	Shorted power transistor	Open input filter inductor	Shorted input filter capacitor	Shorted "commutating" diode	Loss of signal through logic circuit	Inadequate drive due to preamplifier malfunction	Shorted input filter inductor	Open transformer or autotransformer	Shorted transformer or autotransformer	Open input filter capacitor	Open "commutating" diode	Shorted auxiliary diode, or limiting zener	Open auxiliary diode, or limiting zener	Leakage degradation of limiting zener	Inadequate input power	Open power transistor	Open output filter inductor	Open output filter capacitor	Shorted output filter inductor	Shorted output filter capacitor	Malfunction in time delay circuit
Line Voltage Regulator																														
Buck Boost Type (cont)							X													X										
							X																				X			
Battery Control																														
Dissipative Battery Charger, Momentary Booster	X											X																		
	X															X														
	X																										X			
	X																													X
			X										X																	
			X																									X		
				X						X																				
				X											X															
				X																										
				X																					X					
						X				X																				

Table 8-2. Summary of Failure Modes and Effects Analysis (Cont)

			METHOD OF DETECTION						REDUNDANCY PROVISIONS						
Malfunction in time delay circuit	Malfunction in frequency control mechanism		Not applicable	Fuses	AC level sensor	DC level sensor	Timing mechanism		Derating of parts used in parallel (a)	Majority voting	Quad configuration	Standby redundancy	Building block redundancy with built-in open failure modes (b)	Not applicable	NOTES
			X								X				
			X	X							X		X		
				X									X		
			X*								X				
				X									X		
			X						X						
			X							X					
			X								X				
			X	X							X		X		
X			X						X						
			X							X					
			X								X				
			X	X							X		X		
			X						X						
			X							X					
			X								X				
						X								Y	(i)
			X								X				
				X									X		
				Y		Y						X			
				Y									X		
			X						X						
			X							X					
			X								X				

NOTES

(a) Applicable to parts that are expected to fail open.
(b) This assumes that the minimum power capability of the source powering the element is higher than the power capability of the building block.
(c) Certain combinations of methods of detection and redundancy provisions have been discarded. For instance, it would not be advisable to account for a shorted output capacitor by using a dc failure sensor and standby redundancy.
(d) One effective way to minimize the critical effects of a shorted inductor is to have two or three smaller inductors in series. This solution goes hand-in-hand with building block redundancy, and provides a strong incentive to obviate standby redundancy in many instances.
(e) The concept of "quad" has been extended to include capacitor banks configured so that each string has two capacitors in series, and rectifier redundancy (either quad, series, or parallel).
(f) Loss of solar array orientation.
(g) The significance of prescribing fusing-and-building-block redundancy to take care of an "open inductor" failure is that various PWM (or whatever the element might be) are assumed to be in parallel and power sharing is obtained by virtue of:
    1. Synchronized switching
    2. Using LC input and output circuits both as filters and as current equalizing impedances.
(h) Failure in a related element.
(i) Relay redundancy not included in this study.

*Second order malfunction, low, illumination

FOLDOUT FRAME 2

ELEMENT	FAILURE MODE: Excessive ripple (E or D), instability or inadequate response.	Low output signal (E or D).	Loss of output signal and Zo → 0.	Loss of output signal and Zo → ∞.	High output signal (E or D).	Loss of battery recharge capability.	Loss of voltage regulation, or variation of the voltage limiting point.	Loss of share mode detection, or anomalies in the periodicity of the momentary discharge booster.	Loss of frequency control.	FAILURE CAUSE: Loss of drive power	Shorted power transistor	Open input filter inductor	Shorted input filter capacitor	Shorted "commutating" diode	Loss of signal through logic circuit	Inadequate drive due to preamplifier malfunction	Shorted input filter inductor	Open transformer or autotransformer	Shorted transformer or autotransformer	Open input filter capacitor	Open "commutating" diode	Shorted auxiliary diode, or limiting zener	Open auxiliary diode, or limiting zener	Leakage degradation of limiting zener	Inadequate input power	Open power transistor	Open output filter inductor	Open output filter capacitor
Battery Control																											
Dissipative Battery Charger, Momentary Booster (Cont)						X									X												
						X												X									
						X													X								
						X															X						
						X																X					
						X																	X				
						X											X										
							X									X											
							X																	X			
							X																				X
								X								X											
								X																			
Dissipative Battery Charger, Boost Discharge Regulator	X															X											
	X																		X								

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Table 8-2. Summary of Failure Modes and Effects Analysis (Cont)

METHOD OF DETECTION						REDUNDANCY PROVISIONS							
Not applicable	Fuses	AC level sensor	DC level sensor	Timing mechanism		Derating of parts used in parallel (a)	Majority voting	Quad configuration	Standby redundancy	Building block redundancy with built-in open failure modes (b)	Not applicable	NOTES	
			X								X	(i)	
	X		X						X	X			
	X		X						X	X			
	X		X					X		X			
	X		X					X		X			
			X								X	(h)	
	X		X						X	X			
X						X							
X							X						
X								X					
			X								X	(h)	
X									X				
	X									X			
X						X							
X							X						
X								X					
X						X							
X							X						
X								X					
X									X				
	X									X			

NOTES

(a) Applicable to parts that are expected to fail open.
(b) This assumes that the minimum power capability of the source powering the element is higher than the power capability of the building block.
(c) Certain combinations of methods of detection and redundancy provisions have been discarded. For instance, it would not be advisable to account for a shorted output capacitor by using a dc failure sensor and standby redundancy.
(d) One effective way to minimize the critical effects of a shorted inductor is to have two or three smaller inductors in series. This solution goes hand-in-hand with building block redundancy, and provides a strong incentive to obviate standby redundancy in many instances.
(e) The concept of "quad" has been extended to include capacitor banks configured so that each string has two capacitors in series, and rectifier redundancy (either quad, series, or parallel).
(f) Loss of solar array orientation.
(g) The significance of prescribing fusing-and-building-block redundancy to take care of an "open inductor" failure is that various PWM (or whatever the element might be) are assumed to be in parallel and power sharing is obtained by virtue of:
    1. Synchronized switching
    2. Using LC input and output circuits both as filters and as current equalizing impedances.
(h) Failure in a related element.
(i) Relay redundancy not included in this study.

*Second order malfunction, low, illumination

FOLDOUT FRAME 2

ELEMENT	FAILURE MODE: Excessive ripple (E or D), instability or inadequate response.	Low output signal (E or D).	Loss of output signal and Zo → 0.	Loss of output signal and Zo → ∞.	High output signal (E or D).	Loss of battery recharge capability.	Loss of voltage regulation, or variation of the voltage limiting point.	Loss of share mode detection, or anomalies in the periodicity of the momentary discharge booster.	Loss of frequency control.	FAILURE CAUSE: Loss of drive power	Shorted power transistor	Open input filter inductor	Shorted input filter capacitor	Shorted "commutating" diode	Loss of signal through logic circuit	Inadequate drive due to preamplifier malfunction	Shorted input filter inductor	Open transformer or autotransformer	Shorted transformer or autotransformer	Open input filter capacitor	Open "commutating" diode	Shorted auxiliary diode, or limiting zener	Open auxiliary diode, or limiting zener	Leakage degradation of limiting zener	Inadequate input power	Open power transistor	Open output filter inductor	Open output filter capacitor	Shorted output filter inductor
Battery Control																												
Dissipative Battery Charger, Boost Discharge Regulator (Cont)	X																										X	
	X																											X
		X								X																		
		X											X															
		X												X														
		X													X													
		X														X												
		X																X										
		X																	X									
		X																		X								
		X																			X							
		X																				X						
		X																					X					
		X																						X				
		X																							X			

FOLDOUT FRAME /

Table 8-2. Summary of Failure Modes and Effects Analysis (Cont)

									METHOD OF DETECTION					REDUNDANCY PROVISIONS						
Open power transistor	Open output filter inductor	Open output filter capacitor	Shorted output filter inductor	Shorted output filter capacitor	Malfunction in time delay circuit	Malfunction in frequency control mechanism	Not applicable	Fuses	AC level sensor	DC level sensor	Timing mechanism	Derating of parts used in parallel (a)	Majority voting	Quad configuration	Standby redundancy	Building block redundancy with built-in open failure modes (b)	Not applicable	NOTES
		X					X							X				
			X					X		X					X	X		
							X					X						
							X							X				
							X	X								X		
							X			X					X			
										X							X	(h) (i)
							X					X						
							X						X					
							X							X				
								X		X					X	X		
								X		X					X	X		
								X		X					X	X		
								X		X					X	X		
								X		X					X	X		
										X							X	(h)
X								X		X					X	X		

NOTES

(a) Applicable to parts that are expected to fail open.
(b) This assumes that the minimum power capability of the source powering the element is higher than the power capability of the building block.
(c) Certain combinations of methods of detection and redundancy provisions have been discarded. For instance, it would not be advisable to account for a shorted output capacitor by using a dc failure sensor and standby redundancy.
(d) One effective way to minimize the critical effects of a shorted inductor is to have two or three smaller inductors in series. This solution goes hand-in-hand with building block redundancy, and provides a strong incentive to obviate standby redundancy in many instances.
(e) The concept of "quad" has been extended to include capacitor banks configured so that each string has two capacitors in series, and rectifier redundancy (either quad, series, or parallel).
(f) Loss of solar array orientation.
(g) The significance of prescribing fusing-and-building-block redundancy to take care of an "open inductor" failure is that various PWM (or whatever the element might be) are assumed to be in parallel and power sharing is obtained by virtue of:
    1. Synchronized switching
    2. Using LC input and output circuits both as filters and as current equalizing impedances.
(h) Failure in a related element.
(i) Relay redundancy not included in this study.

*Second order malfunction, low, illumination

FOLDOUT FRAME 2

	ELEMENT	Battery Control: Dissipative Battery Charger, Boost Discharge Regulator (Cont)												
FAILURE MODE	Excessive ripple (E or I), instability or inadequate response.													
	Low output signal (E or I).													
	Loss of output signal and Zo → 0.												X	
	Loss of output signal and Zo → ∞.										X	X		
	High output signal (E or I)								X	X				
	Loss of battery recharge capability.	X	X	X	X	X	X	X						
	Loss of voltage regulation, or variation of the voltage limiting point.													
	Loss of share mode detection, or anomalies in the periodicity of the momentary discharge booster.													
	Loss of frequency control.													
FAILURE CAUSE	Loss of drive power							X						
	Shorted power transistor						X			X				
	Open input filter inductor													
	Shorted input filter capacitor					X								
	Shorted "commutating" diode													
	Loss of signal through logic circuit				X									
	Inadequate drive due to preamplifier malfunction			X					X					
	Shorted input filter inductor													
	Open transformer or autotransformer											X		
	Shorted transformer or autotransformer													
	Open input filter capacitor													
	Open "commutating" diod													
	Shorted auxiliary diode, or limiting zener													
	Open auxiliary diode, or limiting zener		X											
	Leakage degradation of limiting zener													
	Inadequate input power	X												
	Open power transistor													
	Open output filter inductor										X			
	Open output filter capacitor													
	Shorted output filter inductor													

Table 8-2. Summary of Failure Modes and Effects Analysis (Cont)

CAUSE														METHOD OF DETECTION						REDUNDANCY PROVISIONS							
[illegible]	Shorted auxiliary diode, or limiting zener	Open auxiliary diode, or limiting zener	Leakage degradation of limiting zener	Inadequate input power	Open power transistor	Open output filter inductor	Open output filter capacitor	Shorted output filter inductor	Shorted output filter capacitor	Malfunction in time delay circuit	Malfunction in frequency control mechanism	Not applicable	Fuses	AC level sensor	DC level sensor	Timing mechanism	Derating of parts used in parallel (a)	Majority voting	Quad configuration	Standby redundancy	Building block redundancy with built-in open failure modes (b)	Not applicable	NOTES	
									X			X							X		X			
													X		X					X	X		
						X							X		X					X	X		
													X		X					X	X		
												X				X					X		
												X				X					X		
												X	X		X				X		X		
												X							X		X		
															X							X	(h) (i)
												X				X							
												X	X					X			X		
		X										X			X				X	X			
				X									X		X						X	(h)	

NOTES

(a) Applicable to parts that are expected to fail open.
(b) This assumes that the minimum power capability of the source powering the element is higher than the power capability of the building block.
(c) Certain combinations of methods of detection and redundancy provisions have been discarded. For instance, it would not be advisable to account for a shorted output capacitor by using a dc failure sensor and standby redundancy.
(d) One effective way to minimize the critical effects of a shorted inductor is to have two or three smaller inductors in series. This solution goes hand-in-hand with building block redundancy, and provides a strong incentive to obviate standby redundancy in many instances.
(e) The concept of "quad" has been extended to include capacitor banks configured so that each string has two capacitors in series, and rectifier redundancy (either quad, series, or parallel).
(f) Loss of solar array orientation.
(g) The significance of prescribing fusing-and-building-block redundancy to take care of an "open inductor" failure is that various PWM (or whatever the element might be) are assumed to be in parallel and power sharing is obtained by virtue of:
    1. Synchronized switching
    2. Using LC input and output circuits both as filters and as current equalizing impedances.
(h) Failure in a related element.
(i) Relay redundancy not included in this study.

*Second order malfunction, low, illumination

FOLDOUT FRAME 2

ELEMENT	FAILURE MODE: Excessive ripple (E or I), instability or inadequate response.	Low output signal (E or I).	Loss of output signal and Zo → 0.	Loss of output signal and Zo → ∞.	High output signal (E or I).	Loss of battery recharge capability.	Loss of voltage regulation, or variation of the voltage limiting point.	Loss of share mode detection, or anomalies in the periodicity of the momentary discharge booster.	Loss of frequency control.	FAILURE CAUSE: Loss of drive power	Shorted power transistor	Open input filter inductor	Shorted input filter capacitor	Shorted "commutating" diode	Loss of signal through logic circuit	Inadequate drive due to preamplifier malfunction	Shorted input filter inductor	Open transformer or autotransformer	Shorted transformer or autotransformer	Open input filter capacitor	Open "commutating" diode	Shorted auxiliary diode, or limiting zener	Open auxiliary diode, or limiting zener	Leakage degradation of limiting zener	Inadequate input power	Open power transistor	Open output filter inductor	Open output filter capacitor	Shorted output filter inductor
Battery Control																												
Dissipative Battery Charger, Boost Discharge Regulator (Cont)						X																			X			
						X																						
							X									X												
							X																					
2.4 kHz Inverter																												
Similar to MM69	X															X												
	X																X											
	X																			X								
		X														X												
		X																						X				
			X								X																	
			X										X															
			X																X									
				X						X																		

FOLDOUT FRAME 1

Table 8-2. Summary of Failure Modes and Effects Analysis

Malfunction in time delay circuit	Malfunction in frequency control mechanism	METHOD OF DETECTION: Not applicable	Fuses	AC level sensor	DC level sensor	Timing mechanism	REDUNDANCY PROVISIONS: Derating of parts used in parallel (a)	Majority voting	Quad configuration	Standby redundancy	Building block redundancy with built-in open failure modes (b)	Not applicable	NOTES
					X					X			
			X								X		
		X							X				
			X								X		
		X					X						
		X						X					
		X							X				
					X							X	
		X*					X						
		X						X					
		X							X				
				X						X			
			X								X		
		X							X				
			X								X		
		X					X						
		X						X					
		X							X				
					X							X	(h)
				X						X			
			X								X		
		X							X				
			X								X		
				X						X			
			X								X		
		X					X						
		X							X				
				X						X			
			X								X		

NOTES

(a) Applicable to parts that are expected to fail open.
(b) This assumes that the minimum power capability of the source powering the element is higher than the power capability of the building block.
(c) Certain combinations of methods of detection and redundancy provisions have been discarded. For instance, it would not be advisable to account for a shorted output capacitor by using a dc failure sensor and standby redundancy.
(d) One effective way to minimize the critical effects of a shorted inductor is to have two or three smaller inductors in series. This solution goes hand-in-hand with building block redundancy, and provides a strong incentive to obviate standby redundancy in many instances.
(e) The concept of "quad" has been extended to include capacitor banks configured so that each string has two capacitors in series, and rectifier redundancy (either quad, series, or parallel).
(f) Loss of solar array orientation.
(g) The significance of prescribing fusing-and-building-block redundancy to take care of an "open inductor" failure is that various PWM (or whatever the element might be) are assumed to be in parallel and power sharing is obtained by virtue of:
    1. Synchronized switching
    2. Using LC input and output circuits both as filters and as current equalizing impedances.
(h) Failure in a related element.
(i) Relay redundancy not included in this study.

*Second order malfunction, low, illumination

FOLDOUT FRAME 2

ELEMENT	FAILURE MODE										FAILURE												
	Excessive ripple (E or I), instability or inadequate response.	Low output signal (E or I).	Loss of output signal and Zo → 0.	Loss of output signal and Zo → ∞.	High output signal (E or I).	Loss of battery recharge capability.	Loss of voltage regulation, or variation of the voltage limiting point.	Loss of share mode detection, or anomalies in the periodicity of the momentary discharge booster.	Loss of frequency control.		Loss of drive power	Shorted power transistor	Open input filter inductor	Shorted input filter capacitor	Shorted "commutating" diode	Loss of signal through logic circuit	Inadequate drive due to preamplifier malfunction	Shorted input filter inductor	Open transformer or autotransformer	Shorted transformer or autotransformer	Open input filter capacitor	Open "commutating" diode	
2.4 kHz Inverter																							
Similar to MM69 (Cont)				X									X										
				X															X				
					X												X						
					X																		
							X										X						
									X														

FOLDOUT FRAME 1

Table 8-2. Summary of Failure Modes and Effects Analysis (Cont)

CAUSE															METHOD OF DETECTION						REDUNDANCY PROVISIONS							
Open "commutating" diode	Shorted auxiliary diode, or limiting zener	Open auxiliary diode, or limiting zener	Leakage degradation of limiting zener	Inadequate input power	Open power transistor	Open output filter inductor	Open output filter capacitor	Shorted output filter inductor	Shorted output filter capacitor	Malfunction in time delay circuit	Malfunction in frequency control mechanism	Not applicable	Fuses	AC level sensor	DC level sensor	Timing mechanism	Derating of parts used in parallel (a)	Majority voting	Quad configuration	Standby redundancy	Building block redundancy with built-in open failure modes (b)	Not applicable	NOTES	
														X						X				
													X								X			
													X							X				
												X					X							
												X						X						
												X							X					
				X								X										X	(h)	
												X*					X							
												X						X						
												X							X					
											X	X					X							
												X						X						
												X							X					
														X						X				
														X										

NOTES

(a) Applicable to parts that are expected to fail open.
(b) This assumes that the minimum power capability of the source powering the element is higher than the power capability of the building block.
(c) Certain combinations of methods of detection and redundancy provisions have been discarded. For instance, it would not be advisable to account for a shorted output capacitor by using a dc failure sensor and standby redundancy.
(d) One effective way to minimize the critical effects of a shorted inductor is to have two or three smaller inductors in series. This solution goes hand-in-hand with building block redundancy, and provides a strong incentive to obviate standby redundancy in many instances.
(e) The concept of "quad" has been extended to include capacitor banks configured so that each string has two capacitors in series, and rectifier redundancy (either quad, series, or parallel).
(f) Loss of solar array orientation.
(g) The significance of prescribing fusing-and-building-block redundancy to take care of an "open inductor" failure is that various PWM (or whatever the element might be) are assumed to be in parallel and power sharing is obtained by virtue of:
    1. Synchronized switching
    2. Using LC input and output circuits both as filters and as current equalizing impedances.
(h) Failure in a related element.
(i) Relay redundancy not included in this study.

*Second order malfunction, low, illumination

FOLDOUT FRAME 2

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ITEM	NUMBER	EFFECT ON RELATED ELEMENTS							
		SOLAR ARRAY	ARRAY CONTROL	BATTERY	BATTERY CHARGER	MOM. BOOSTER	LINE BOOST REG.	2 - 4 kHz	3φ
		V I P	V I P T	V I P E T	V I P RR T	V I P DS T	V I P RR T	V I P RR T	V I P RR T
SOLAR ARRAY	1, 2	-0 -0 -0	-0 -0 -0 0	0 0 0 -0 0	-0 -0 -0 0 0	0 0 0 0 0	-0 +0 +0 0 +0	0 0 0 0 0	0 0 0 0 0
	3, 4, 6	-0 -f -f	-0 -0 -0 -0	0 0 0 -f 0	-0 -f -f 0 0	0 0 0 0 0	-0 +0 +0 0 +0	0 0 0 0 0	0 0 0 0 0
	5	-0 -f -f	-0 -0 -0 -0	0 0 0 -f 0	-0 -f -f 0 0	0 0 0 0 0	-0 +0 +0 0 +0	0 0 0 0 0	0 0 0 0 0
	7	-0 -0 -0	-0 +0 -0 0	0 0 0 0 0	-0 -0 -0 0 0	0 0 0 0 0	-0 +0 +0 0 0	0 0 0 0 0	0 0 0 0 0
	8	+0 -0 +0	+0 -0 +0 0	0 0 0 0 0	+0 0 +0 0 0	0 0 0 0 0	+0 -0 -0 0 0	0 0 0 0 0	0 0 0 0 0
SOLAR ARRAY CONTROL	1	0 0 0	+0 +0 +0 +0	0 0 0 0 0	+f 0 +f 0 +f	0 0 0 0 0	+F/C +0 +0 0 ±0	+F/C +F/C +F/C 0 +F/C	+F/C +F/C +F/C 0 +F/C
	2, 3	0 0 0	-0 +f +f +f	0 0 0 -C 0	-0 -0 -0 0 0	0 0 0 0 0	-0 +0 +0 0 +0	0 0 0 0 0	0 0 0 0 0
	4	0 0 0	-0 -0 -0 -0	-F +F +F -F +F	-0 -0 -0 0 0	-f +F +F ±F +f	-F -F -F 0 +f/F	-F -F -F -F +F	-F -F -F -F +F
	5	SAME AS "SOLAR ARRAY 1, 2"							
	6	NO EFFECT ON SYSTEM, UNLESS STRING IS SHORTED. THEN EFFECTS ARE AS FOR "SOLAR ARRAY CONTROL 4"							
BATTERY	(1)	0 0 0	0 0 0 0	-F -F -F -F 0	0 -0 -0 0 0	-0 -0 -0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0
DARK	(2)	0 0 0	0 0 0 -0	-0 +0 +0 +0 +0	0 +0 +0 0 +0	-0 0 +0 0 0	-0 +0 +0 0 0	0 0 0 0 0	0 0 0 0 0
SUNLIGHT	(2A)	0 0 0	0 0 0 0	+C +C +C -f +f	0 +0 +0 0 +0	0 0 0 0 0	-0 +0 +0 0 0	0 0 0 0 0	0 0 0 0 0
DARK	3	0 0 0	0 0 0 0	-F +F -F -F +F	-f -0 0 0 0	-0 0 0 0 0	-F -F -F 0 -0	-F -F -F 0 -0	-F -F -F 0 0
SUNLIGHT	3A	0 0 0	0 0 0 0	-F +F -F -F +F	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0
DISCHARGE DIODE	(1)*	0 0 0	0 0 0 0	+C +C +C -C +C	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0
KINETIC SW	(1, 2)	0 0 0	0 0 0 0	-F -F -F -F 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0
FILTER	1	0 0 0	+0 +0 +0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0
	(2, 3)	0 0 0	0 0 0 0	0 0 0 0 0	0 0 0 +f 0	0 0 0 0 0	0 0 0 +f 0	0 0 0 0 0	0 0 0 0 0
	4	SAME AS "SOLAR ARRAY CONTROL NO. 4"							
BATTERY CHARGER	1, 2	0 0 0	0 0 0 0	0 0 0 -C 0	0 -0 -0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0
	3	0 0 0	0 0 0 0	0 -F +F -F +F	-F +F +F 0 +f	0 0 0 0 0	-F -F -F 0 0	-F -F -F -F -F	-F -F -F -F -F
	4	0 0 0	0 0 0 0	+C +C +C -C +C	0 +C +C 0 +C	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0
	5	0 0 0	0 0 0 0	+C 0 +C -C +C	0 0 +0 0 +0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0
	6	0 0 0	0 0 0 0	-F +F +F -F +F	0 +0 +0 0 +0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0
	7	0 0 0	0 0 0 0	0 +f +f -0 +f	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0
MOMENTARY BOOSTER	1	0 0 0	0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0
	2	0 0 0	0 0 0 0	-f +f 0 0 0	0 0 0 0 0	-f +F +F 0 +f	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0
	3	0 0 0	0 0 0 0	-0 +0 +0 -C 0	0 0 0 0 0	-0 +F +F 0 +F	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0
BOOST REGULATOR	1	0 0 0	+0 +0 +0 +0	0 0 0 0 0	+0 0 +0 0 0	0 0 0 0 0	+0 -0 -0 0 0	-F -F -F -F 0	-F -F -F -F 0
	1, 3	0 0 0	-0 -0 -0 0	-F +F +F -F +F	-F -F -F -F 0	-F -F -F -F 0	-F +F +F -F +F	-F -F -F -F 0	-F -F -F -F 0
	2	0 0 0	-0 -0 -0 0	0 0 0 0 0	0 -0 0 0 0	0 0 0 0 0	-0 +F/C +F/C 0 +F/C	+F/C +F/C +F/C 0 +F/C	+F/C +F/C +F/C 0 +F/C
	4	0 0 0	0 0 0 0	0 0 0 0 0	0 0 0 +f 0	0 0 0 0 0	-0 +f +f +f +f	+f 0 0 +f 0	+f 0 0 +f 0
2.4 kHz INVERTER	1	0 0 0	+0 +f/0 +f/0 +f/0	0 0 0 0 0	+0 0 +0 0 0	0 0 0 0 0	+0 -f/0 -0 0 0	+f 0 0 +f 0	+f 0 0 +f 0
	2	0 0 0	-0 -0 -0 0	-F +F +F -F +F	0 0 0 0 0	0 0 0 0 0	-F +F +F -F +F	-F +F +F -F +F	-F -F -F -F 0
	3	0 0 0	-0 -0 -0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	-0 +F/f +F/f 0 +F/f	0 +F/f +F/f 0 +F/f	0 0 0 0 0
	4	0 0 0	0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0
1φ, 3φ INVERTER	1	0 0 0	+0 +0 +0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	+0 -0 -0 0 0	0 0 0 0 0	0 0 0 0 0
	2	0 0 0	-0 -0 -0 0	-F +F +F -F +F	0 0 0 0 0	0 0 0 0 0	-F +F +F -F +F	-F -F -F -F -0	-F +F +F -F +F
	3	0 0 0	0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 +f

FOLDOUT FRAME 1

Table 8-3. Failure Modes and Effects Matrix – Mariner Power System

1φ (I P RR T)	COMMENTS	NUMBER	EFFECT ON SYSTEM PERFORMANCE: UNREG. DC (V I P RR)	REG. 56 VDC (V I P R RR)	2.4 kHz (V I P f)	0.4 kHz 3φ (V I P f)	0.4 kHz 1φ (V I P f)	S/C PWR (SUN) P	S/C PWR (SUN) LS	S/C PWR MANEUVER P
0 0 0 0		1, 2	-0 +0 ±0 0	0 C 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	-0		
0 0 0 0	(1) DURING A MANEUVER, THERE WILL BE A COMPLETE LOSS OF POWER.	3, 4, 6	-0 +0 ±0 0	0 0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	-f	Y/N	-f
0 0 0 0	DURING SUNLIGHT, LOAD TRANSIENTS WILL CAUSE	5	-0 +0 ±0 0	0 0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	-f	Y/N	-f
0 0 0 0	SYSTEM "HANG-UP" AT A LOW VOLTAGE (<25 VDC).	7	-0 +0 ±0 0	0 0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0			
0 0 0 0		8	+0 -0 ±0 0	0 0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0			
	(2) MANEUVER OPERATION									
$+\frac{F}{C}$ $+\frac{F}{C}$ 0 $+\frac{F}{C}$	(2A) SUNLIGHT-BATTERY CHARGING MODE	1	+F +0 +0 0	+F +F +F +F 0	+F +F +F $+\frac{F}{f}$	+F +F +F	+F +F +F $+\frac{F}{f}$	-C	Y	-C
0 0 0 0	(1)* BATTERY WILL OVERCHARGE	2	-0 +0 ±0 0	0 0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	-C	Y	-C
-F -F -F +F	AND WILL BE PERMANENTLY DAMAGED IN AN OPEN OR SHORTED CONDITION	4	-F +F -F +F	-F -F -F -F +F	-F -F -F ±F	-F -F -F ±F	-F -F -F ±F	-F	Y	-F
		5								
	(1, 2) SAME AS "BATTERY (NO. 1) – CELL OPEN"	6								
0 0 0 0	(2, 3) MAY CAUSE BOOST REGULATOR INSTABILITY	(1)	0 0 0 0	0 0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	-C	N	-F
0 0 0 0	AND LOSS OF SYSTEM REGULATION – IMMEDIATE	(2)	-0 +0 +0 0	0 0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0			
0 0 0 0	FAILURE	(2A)	-0 +0 +0 0	0 0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0			
-F -F 0 0		3	-F -F -F 0	-F -F -F -F 0	-F -F -F -F	-F -F -F -F	-F -F -F -F	-F		-F
0 0 0 0		3A	0 0 0 0	0 0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	O	N	-F
0 0 0 0		(1)*	-0 -0 0 0	0 0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	-C/-f	Y	-C/-f
0 0 0 0	1. LOAD SHARING WILL OCCUR IF LOAD TRANSIENT	(1, 2)	0 0 0 0	0 0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	O	N	-F
0 0 0 0	OR ORIENTATION MALFUNCTION	1	0 0 0 0	0 0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	-F	Y	-F
0 0 0 0	$Z_0 \to \infty$	(2, 3)								
	$Z_0 \to \infty$									
0 0 0 0		1, 2	0 0 0 0	0 0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	O	N	-F/C
-F -F -F -F	NOTES:	3	-F -F -F -F	-F -F -F -F -F	-F -F -F -F	-F -F -F -F	-F -F -F -F	-F	Y	-F
0 0 0 0	+ = INCREASE	4	0 0 0 0	0 0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	-C	Y	-C
0 0 0 0	- = DECREASE	5	0 0 C 0	0 0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	-C	N	-C
0 0 0 0	0 = WITHIN NORMAL LIMITS	6	0 0 0 0	0 0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	-O	Y/N	-F
0 0 0 0	f = MAXIMUM LIMITS, POTENTIAL DEGRADATION	7	0 0 0 0	0 0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	O	N	-f
0 0 0 0	F = EXTREME LIMITS, IMMEDIATE FAILURE	1	0 0 0 0	0 0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	-C/O	Y/N	-C/O
0 0 0 0	C = EXTREME LIMITS, FAILURE IF NO CORRECTIVE ACTION TAKEN	2	0 0 0 0	0 0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	O	N	-C
0 0 0 0	V = VOLTAGE	3	0 0 0 0	0 0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	O	Y	-C
	I = CURRENT									
-F -F -F 0	P = POWER	1	+0 0 0 0	-F -F -F -F -F	-F -F -F -F	-F -F -F -F	-F -F -F -F	-F	N	-F
-F -F -F 0	R = PERCENT REGULATION	1, 3	-F +F -F -F	-F -F -F -F -F	-F -F -F -F	-F -F -F -F	-F -F -F -F	-F	Y	-F
$+\frac{F}{C}$ $+\frac{F}{C}$ 0 $+\frac{F}{C}$	RR = RIPPLE	2	-0 0 0 0	+F +F +F +F +f	+F +F +F 0	+F +F +F 0	+F +F +F 0	-F/C	Y	-F/C
0 0 +f 0	E = ENERGY	4	-0 0 0 +f	+f 0 0 +f +f	+f 0 0 0	+f 0 0 0	+f 0 0 0	-O	N	O
	T = TEMPERATURE									
0 0 +f 0	DS = DUTY CYCLE	1	+0 0 0 +f	-f 0 0 +f +f	-F -F -F -F	+f 0 0 0	+f 0 0 0	O	N	O
-F -F -F 0	f = FREQUENCY	2	-F -F -F -F	-F -F -F -F -F	-F -F -F -F	-F -F -F -F	-F -F -F -F	-F	Y	-F
0 0 0 0	Y = YES	3	-0 0 0 0	$-\frac{F}{f}$ $-\frac{F}{f}$ $+\frac{F}{f}$ $-\frac{F}{f}$ 0	$+\frac{F}{f}$ $+\frac{F}{f}$ $+\frac{F}{f}$ 0	0 0 0 0	0 0 0 0	-C/F	Y/N	-C/f
0 0 0 0	N = NO	4	0 0 0 0	0 0 0 0 0	0 0 0 +f	0 0 0 +f	0 0 0 +f	O	N	O
	LS = SOLAR ARRAY – BATTERY LOAD SHARING									
-0 -0 0 0		1	0 0 0 0	0 0 -0 -0 0	0 0 0 0	-F -F -F -F	-F -F -F -F	O	N	O
-F +F -F +F		2	-F -F -F 0	-F +F +F -F -F	-F -F -F -F	-F -F -F -F	-F -F -F -F	-F	Y	-F
0 0 0 +f		3	0 0 0 0	0 0 0 0 0	0 0 0 0	0 0 0 $+\frac{F}{f}$	0 0 0 $+\frac{F}{f}$	O	N	O

FOLDOUT FRAME 2

8.3 METHODS OF FAILURE PROTECTION AND RELIABILITY IMPROVEMENT

In analyzing the various power system configurations, the major approaches considered in implementing reliability were as follows:

a. Parallel redundancy
b. Fail-safe components
c. Series redundancy
d. Quad redundancy
e. Majority voting
f. Standby redundancy
g. Fail-safe redundancy
h. Ground command override

Each of these techniques is discussed in detail in the following paragraphs.

8.3.1 Parallel Redundancy

This redundancy method involves two or more similar circuits/parts operating in parallel such that they will share the load. Capability is incorporated to detect their own failures in a manner that their particular failure modes are predicted and conditioned so that they do not impair the performance of the remaining portions of the circuit. Furthermore, the share of power or voltage handled by the remaining segments of the circuit, although higher after the failure has occurred, still is well within their rating. This approach applies only in cases where open-circuit failures predominate (or forced to an open circuit condition) in the circuit or parts under consideration.

From the weight point of view, the additional weight necessary to incorporate redundancy can be expressed as

$$\% \text{ excess of weight} = \frac{m - x}{x} \times 100 \qquad (8\text{-}1)$$

where

m = number of circuit segments built in

x = minimum number of circuit segments that must remain active to ensure continuance of operation.

This would mean, for instance, that if $m = 5$ (as shown in Figure 8-8) and $x = 4$, then the excess weight would be 25%.

If $m = 7$ and $x = 6$, the excess weight would be 17%. Any further increase of m would result in a smaller weight increment, or could lend itself to tolerate more than one failure and yet retain its operational effectiveness.

From the reliability point of view, Figure 8-8 can be viewed as a reliability block diagram whose probability of survival can be expressed by using a binomial as follows:

$$R_s = \sum_{m=x}^{n} \binom{n}{m} \times R^m \left(1 - R\right)^{(n-m)} \qquad (8\text{-}2)$$

where

$x \leq m \leq n$

$$\binom{n}{m} = \frac{n!}{(n - m)!\, m!}$$

R = Reliability of the individual segment

R_s = Reliability of the redundant circuit.

R_s increases as m is increased, or conversely, as the ratio $\frac{n - x}{n}$ is decreased.

Figure 8-8 depicts, in simplified form, parallel redundancy.

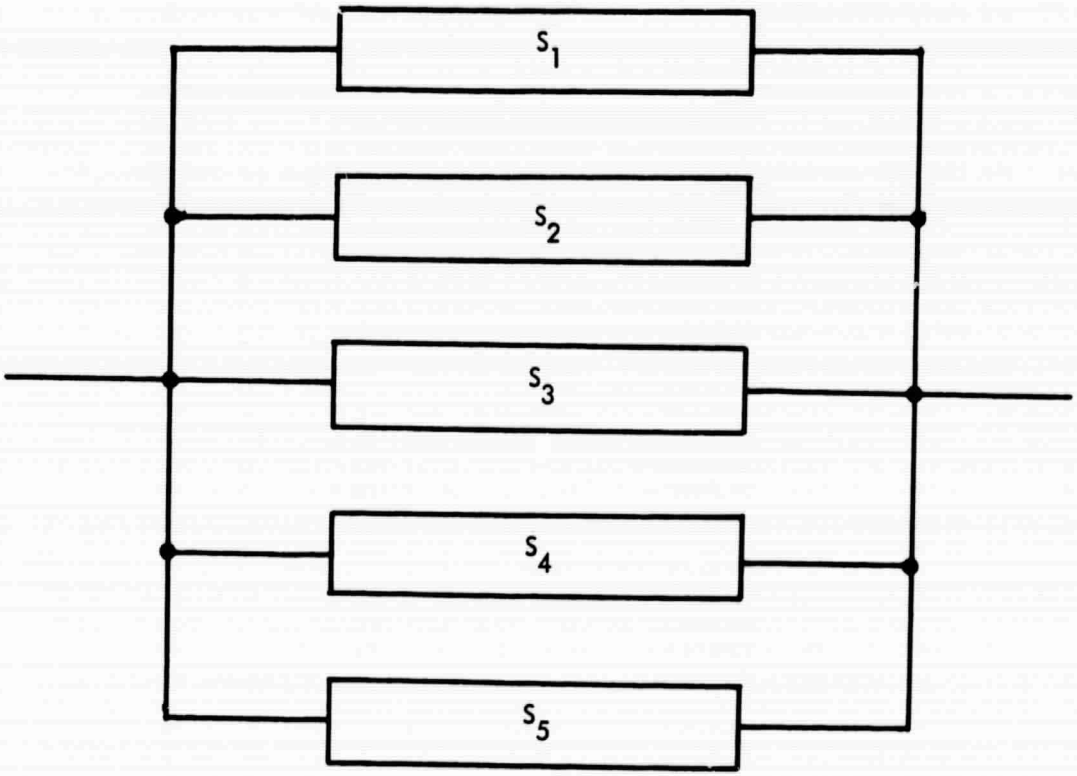


Figure 8-8. Parallel Redundancy

Other properties of the parallel redundancy are covered in the following paragraphs.

8.3.1.1 Current-Sharing

For this type of redundancy to be effective, it is necessary that the various redundant segments of the circuit divide the current among themselves on an equal basis. An efficient way to ensure current-sharing is by means of current-sharing reactors. An example of such is presented in Paragraph 8.3.1.2.

Current-sharing can be provided by dissipative schemes as shown in Figure 8-9. Current-sharing between parallel circuits (e.g., PWM regulator) can also be obtained by taking advantage of the input and output filter characteristics and proper pulse-width control. For example, current-sharing for the proposed buck-boost regulator is obtained in this manner.

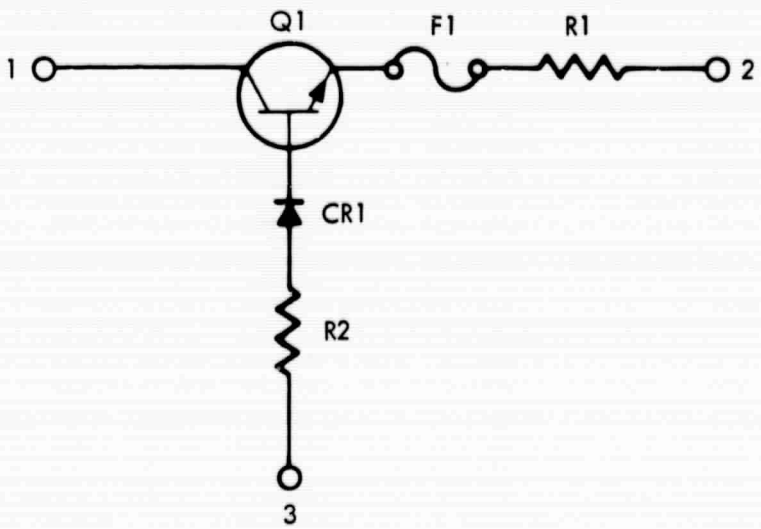


Figure 8-9. Current-Sharing Dissipative Scheme

8.3.1.2 Application of Parallel Redundancy and Current-Sharing to Magnetics

Active redundancy and current-sharing were investigated for converters and inverter power transformers.

Two basic types of single-phase transformer applications are discussed:

a. Transformers for dc-to-dc-converter applications.

b. Transformers for inverter applications.

8.3.1.3 DC-to-DC Converter Applications

In this approach, three single-phase transformers used for dc-to-dc converter application are paralleled as shown in Figure 8-10.

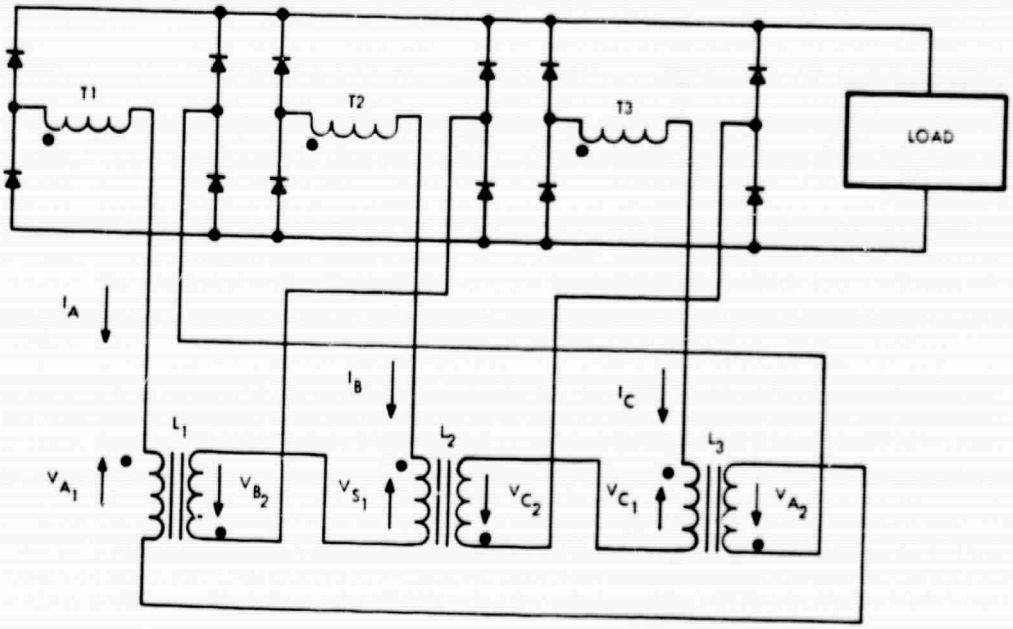


Figure 8-10. DC-to-DC Converter Application Using Paralleled Transformers

Inductors L1, L2, and L3 must have sufficient support voltage to account for the following voltage imbalances:

a. Two silicon rectifiers

b. Maximum voltage imbalance between equally loaded secondary windings.

These imbalances might be between 2 to 3 V.

Reactors L1, L2, and L3 may be small powder core inductors.

In general, the voltage drop across a reactor would be

$$V = L \frac{di}{dt} \qquad (8\text{-}3)$$

where

$$i = I_A - I_B \text{ or } I_B - I_C \text{ etc.} \qquad (8\text{-}4)$$

Parameters can be redesigned to write

$$V_{A_1} = K_1 (I_A - I_B) \quad (8\text{-}5)$$

$$V_{B_1} = K_2 (I_B - I_C) \quad (8\text{-}6)$$

$$V_{C_1} = K_3 (I_C - I_A) \quad (8\text{-}7)$$

for equal conduction in all transformers

$$V_{A_1} = V_{B_1} = V_{C_1} = 0$$

When any transformer coil tends to have a current larger than its own share, the two associated reactors will develop a voltage in opposition to that of the transformer secondary coil. Accordingly, the other two current-equalizing reactors will have an induced voltage, boosting the output of the two remaining transformer coils.

Furthermore, if one secondary coil should open, the two remaining coils will continue to share current.

8.3.1.4 Transformers for Inverter Application

The redundancy technique of paralleling transformers powering ac loads is simpler than that previously described because any failure reflecting a short to the secondary winding of one of the transformers will also reflect the failure to the two remaining transformers.

To account for that critical failure, the following circuit provisions can be included:

a. Using two secondary coils instead of one (one for each current polarity) will increase the size of the transformer by

$$\frac{1 - \frac{1/\sqrt{2}}{0.5}}{2} \times 100 = 20.7\%$$

b. Insertion of one rectifier in series with each coil (6 rectifiers altogether) will preclude any shorted coil from being reflected to the other two coils in phase.

c. The addition of 2 SCR's working synchronously with the AC signal will prevent any shorted coil from being seen by the out-of-phase coils (see Figure 8-11).

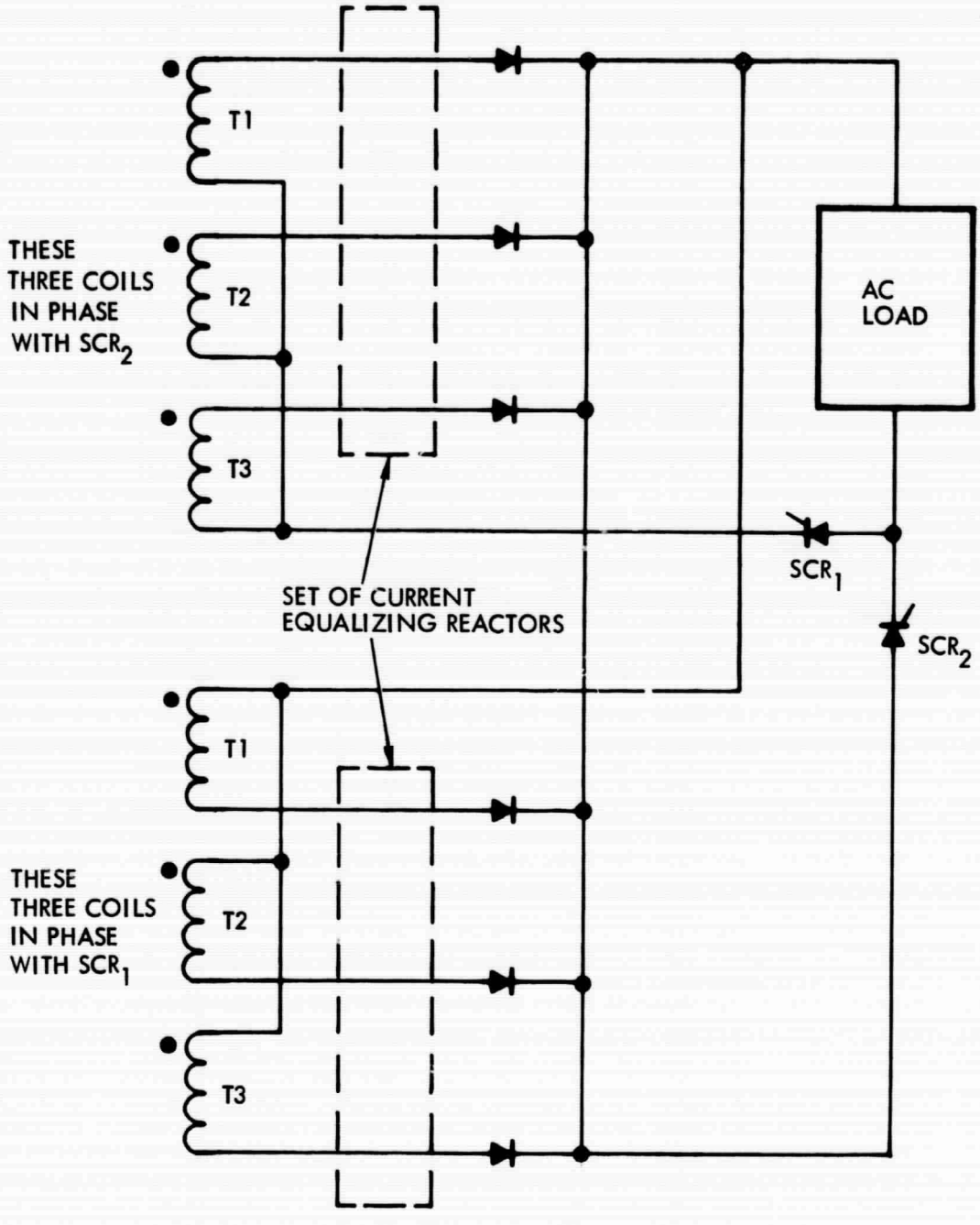


Figure 8-11. Use of Transformers for Inverter Application

8.3.2 Fail-Safe Components

8.3.2.1 Transformers, Inductors, and Magamps

The failure rates of magnetic components can be reduced to extremely low values by careful design and special manufacturing techniques. Therefore, by increasing the spacing between turns and impregnating the coils with adequate compounds and epoxies, it is possible to greatly reduce the probability of failure of the magnet wire insulation (which happens to be the least-reliable characteristic of a magnetic component). Therefore, the possibility of designing and manufacturing fail-safe magnetic components allows the circuit designer and the reliability analyst to disregard open and shorted magnetic components.

8.3.2.2 Relays

a. Coils

The preceding statements can be extended to include relay coils also. Furthermore, the availability of double-coil relays permits an additional increase or reliability by connecting both coils in parallel.

b. Contacts

The avoidance of any current in excess of the safe limits recommended by the manufacturer becomes a necessity to minimize failure rates. A good design practice, therefore, is to protect the contacts against excessive currents by fuses or active current-limiting and to increase reliability, if necessary, by ground command override functions.

8.3.3 Series Redundancy

This technique is applicable to components having a predominant shorted failure mode. The disadvantage of series redundancy is that it increases the losses by a factor of two; this becomes a significant increase in power-handling circuits.

8.3.4 Quad Redundancy

This technique of series and parallel parts may be considered a fail-safe scheme to the extent that at least two failures must occur before its redundant properties are destroyed. There are two types of quad redundancy:

a. Bar: The mid-point of one string is connected to the mid-point of the other.

b. Series: The mid-point of both strings is not connected.

The low efficiency and the considerable parts count make this scheme generally unattractive for power-circuit applications.

8.3.5 Majority Voting

This type of redundancy provides a majority voting function to select the proper output and reject the faulty one. Majority voting is best suited to circuits containing sensing or regulating functions where a relatively high parts count is justifiable.

Applications are:

a. Voltage or current detectors used fail-safe circuits

b. Switching preamplifiers

c. Logic circuits

d. DC amplifiers

e. Feedback amplifiers

8.3.6 Standby Redundancy

This scheme is commonly used in power-circuit applications where efficiency considerations have great importance. It consists of two identical circuits: one normally active, and the other de-energized but ready to be switched in place of the former in the event of a failure.

Different from the schemes discussed earlier, this method requires the addition of a failure-detector circuit in order to sense a malfunction. The failure-detector circuit must be a highly reliable circuit since it has to recognize the malfunction, disconnect the faulty unit, and then connect the standby unit. Its capability of failure recognition must be carefully assessed in terms of all the failure modes that may arise. Therefore, the testability and design considerations for this type of redundancy become a critical requirement.

8.3.7 Fail-Safe Redundancy

Fail-safe redundancy applies to circuits which perform within their prescribed performance limits despite any single component failure whether it be an open or shorted failure. An example of such is the quad and majority voting redundancy.

8.3.8 Ground Command Override

This redundancy scheme is based on ground-command override of automatic functions. This type of redundancy is permissable only when the significant time delays associated with telemetry functions are not objectionable.

The scheme is applicable in four distinct manners:

a. Controlling functions which are not automatically performed

b. Upgrading the reliability of circuits with redundancy provisions.

c. Providing a degraded function capability to a circuit that has lost its normal operation.

d. Increasing efficiency by bypassing dissipative components.

8.4 METHODS OF DETECTION

8.4.1 Fuses

This method is automatic in the sense that it does not require the support of any other special circuit. Its advantages are as follows:

a. The detection function is attended by a protective one.

b. Its protective characteristics are particularly important when heavy fault currents (that could be damaging to relay contacts and semiconductor switches) are expected.

Its disadvantages are as follows:

a. Relatively high failure rates

b. Testability limitations

c. Requirement of a low-impedance, high-current source.

8.4.2 Status TLM

This method has the following advantages:

a. Replacement of complex fail-safe automatic functions

b. Reliability improvement

Its disadvantages are as follows:

a. Additional telemetry requirements

b. Completion of functions may be objectionably delayed.

8.4.3 Voltage or Current Detectors

The advantage of this method is the immediate signal transmission of a fault condition.

9. NEW TECHNOLOGY

Several new concepts developed during this study effort under JPL Contract No. 952151 are reported for the first time below. The concepts are presented in the pages of this report identified below in parentheses:

a. PWM quasi-buck series solar array regulator (page 6-20)

b. Active redundancy and current sharing techniques applicable to converter and inverter transformers (pages 8-46, 8-48)

c. Majority voting time delay circuit (page B-10)

d. Fully redundant emitter follower supply (page B-12).

Innovator: H. E. Gavira

APPENDIX A

RELIABILITY ASSESSMENT OF MARINER-MARS '69 POWER SYSTEM

APPENDIX A

RELIABILITY ASSESSMENT OF MARINER MARS 69 POWER SYSTEM

Introduction

Presented herein are the results of a reliability assessment of the Mariner Mars Power System considering the configuration shown in Figure 1. The reliability assessment was performed for the orbit phase considering a one year (8760 hours) mission time.

Reliability Analysis Ground Rules and Assumptions

(1) The failure rates for the component parts are listed in Table 1. The reliability assessments for the different assemblies are shown in Tables 2 through 17 and are based on parts count from Reference 1.

(2) The following equations were used for calculating the reliability of the system:

(a) Reliability of individual assemblies was calculated by:

$$R = \exp(-\lambda t)$$

where: λ = failure rate of assembly (failures/10^9 hours)

t = mission time (8760 hours)

(b) Reliability of parts or assemblies in series configuration was calculated by:

$$R = \exp(-\Sigma\lambda_i t)$$

where: λ_i = failure rate of each series part or assembly.

(c) For two units (A and B) in active redundancy, when the failure rates of the redundant assemblies are equal, the reliability was calculated by:

$$R = 1 - (1 - \exp(-\lambda_A t))^2$$

where: $\lambda_A = \lambda_B$

(d) For two units (A and B) in active redundancy , when the failure rates of the redundant assemblies are different, the reliability was calculated by:

$$R = 1 - \left[(1 - \exp(-\lambda_A t)\ (1 - \exp(-\lambda_B t)\right]$$

where: $\lambda_A \neq \lambda_B$

(e) For the reliability of a binomial configuration consisting of "n" identical units each having a reliability of R_p, with "m" of "n" units required for success:

$$R = \sum_{X=m}^{n} \binom{n}{X} R_p^X\ (1-R_p)^{n-X}$$

where: $\binom{n}{X} = \dfrac{n!}{(n-X)!\ X!}$

(f) For two units (A and B) with one unit in standby non-operating condition and ideal switching, the reliability was calculated by:

$$R = \exp(-\lambda_A t) + (\lambda_A/(\lambda_A+\lambda_{B2}-\lambda_{B1}))\left[\exp(-\lambda_{B1} t) - \exp(-\lambda_A-\lambda_{B2})t\right]$$

where: λ_A = failure rate of active unit

λ_{B1} = failure rate of standby unit when it is operating

$\lambda_{B2} = 0.1\ \lambda_{B1}$ = failure rate of standby unit when it is inactive

(g) Whenever possible, all reliability calculations were performed on the TYMSHARE Computer System using the REAMX Computer Program.

(h) System Reliability in a series configuration is calculated as the product of the reliabilities of the series units.

(1) It is assumed that the relays will operate not more than 40 cycles a year.

(j) It is assumed that the Reliability of the Solar Array (4A1, 4A3, 4A5, 4A7) is 1.0 per your instructions.

(k) The reliability of an assembly that is ON for 10% of the mission time is calculated by:

$$R = R_{ON} \times R_{OFF}$$

$$R = \exp(-\lambda_{ON} t_{ON}) \times \exp(-\lambda_{OFF} t_{OFF})$$

when: $\lambda_{OFF} = 0.1 \lambda_{ON}$

$t_{ON} = 0.1 t$

$t_{OFF} = 0.9 t$

t = mission time

$$R = \exp(-.19 \lambda_{ON} t)$$

Results

Case (1) With all 24 strings of zeners in 4A20 required for success:

System Reliability = .8544

Case (2) With 23 of 24 strings of zeners in 4A20 assembly required for success:

System Reliability = .9191

Case (3) With 22 of 24 strings of zeners in 4A20 assembly required for success:

System Reliability = .9215

Table 1

Failure Rates for Mariner Mars Power System Study

Part Type	Failure Rate (failures/10^9 hours)
Diode	
Silicon, glass(< 1W)	1.3
Silicon power (> 1W)	14
Zener	60
Transistor	
Silicon (< 1W)	10
Silicon power (> 1W)	56
Integrated Circuits, Digital	50
Resistor	
Carbon Composition, fixed	7
Metal film , fixed	1.4
Wirewound power, fixed	65
Wirewound, variable	120
Capacitor	
Glass	2
Ceramic	15
Mica	3
Paper, mylar, teflon	40
Tantalum solid	14
Tantalum foil, or wet slug	21
Magnetic Devices	
Transformers, inductors, mag amps, Chokes, coils, toroids	15

Table 1 (continued)

Part Type	Failure Rate ($failures/10^9$ hours)
Relay	15($failures/10^9$ cycles)
Transducer	100
Fuse	100
Crystal	20
Connector, per active pin	0.6
Connection, welded or soldered	0.5
Battery cell, silver zinc(per cell)	300

Table 2

Reliability Assessment 4A8 Power Source Logic Assembly

Part Type	Quantity	Total Failure Rate ($failures/10^9$ hours)
Diodes		
Silicon(< 1W)	20	26
Silicon(> 1W)	25	350
Zener	5	300
Transistor		
Silicon(< 1W)	2	20
Resistors		
Metal film	33	46.2
Carbon composition	5	35
Wirewound	2	130
Capacitors		
Tantalum solid	14	196
Glass	1	2
Total		1105.2

Table 3

Reliability Assessment: Either 4A9 or 4A10 Booster Regulator Assembly

Part Type	Quantity	Total Failure Rate (10^{-9} failures/hours)
Diodes		
Silicon(< 1W)	9	11.7
Glass(< 1W)	1	1.3
Silicon(> 1W)	3	42.0
Zener	2	120.0
Transister		
Silicon(< 1W)	2	20.
Silicon(> 1W)	7	392
Resistors		
Metal film, fixed	24	33.6
Carbon composition,fixed	5	35
Wirewound, fixed	3	195
Wirewound, variable	1	120
Capacitors		
Tantalum solid	4	56
Tantalum foil	7	147
Paper	2	80
Transformer	7	105
Coil	1	15
	Total	1374

Table 4

Reliability Assessment 4A11 Power Control Assembly

Part Type	Quantity	Total Failure Rate (10^9 hours)
Diodes		
Glass(< 1W)	4	5.3
Silicon(< 1W)	13	16.9
Silicon(> 1W)	2	28
Zener	8	480
Resistors		
Metal film	26	36.4
Carbon composition	17	119
Capacitors		
Tantalum solid	13	182
Teflon	1	40
Transistors		
Silicon(< 1W)	5	50
Silicon(> 1W)	2	112
Transformer	6	90
Connector, active pins	130	78
	Total	1238

Table 5

Reliability Assessment 4A12 Boost Converter Assembly

Part Type	Quantity	Total Failure Rate (10^9 hours)
Diode		
Silicon(< 1W)	3	3.9
Silicon(> 1W)	2	28.0
Capacitors		
Tantalum foil	1	21.0
Resistors		
Carbon composition, fixed	2	14
Wirewound, fixed	6	390
Transistors		
Silicon(> 1W)	2	112
Transformer	2	30
Fuse	2	200.
Connector, active pins	14	8.4
	Total	807

Table 6

Reliability Assessment 4A12 Charger Assembly

Part Type	Quantity	Total Failure Rate (10^9 hours)
Diode		
Silicon(< 1W)	3	3.9
Zener	1	60
Resistors		
Carbon composition, fixed	8	56
Metal film, fixed	4	5.6
Wirewound, fixed	1	65
Transistors		
Silicon(> 1W)	2	112
Silicon(< 1W)	4	40
Connector, active pins	20	12
	Total	355

Table 7

Reliability Assessment 4A12 Detector Assembly

Part Type	Quantity	Total Failure Rates (10^{-9} Failures/hours)
Diodes		
Silicon(< 1W)	7	9.1
Zener	1	14
Resistor		
Metal film, fixed	7	9.8
Carbon Composition, fixed	8	56
Transistor		
Silicon(< 1W)	3	30
Silicon(> 1W)	1	56
Inductor	1	15
Capacitor, Tantalum solid	2	28
Connectors, active pins	14	8.4
	Total	226.3

Table 8

Reliability Assessment 4A15 Power Distribution Assembly

Part Type	Quantity	Total Failure Rate (10^{-9} Failures/hours)
Diodes		
Silicon(< 1W)	43	55.9
Zener	4	240
Capacitors		
Tantalum solid	9	126
Tantalum foil	12	252
Resistors		
Metal film, fixed	49	68.6
Wirewound, fixed	2	130
Transistors		
Silicon(< 1W)	10	100
Connector, active pins	106	63.6
	Total	1036

Table 9

Reliability Assessment 4A16 Main Inverter Assembly

Part Type	Quantity	Total Failure Rate (10^9 hours)
Resistors		
Metal film, fixed	19	26.6
Wirewound, fixed	6	390.
Carbon composition, fixed	3	21
Transistors		
Silicon(< 1W)	5	50
Silicon(> 1W)	4	224
Inductor	1	15
Capacitor		
Glass	6	12
Tantalum solid	4	56
Tantalum foil	1	21
Paper	1	40
Crystal	1	20
Diodes		
Glass(< 1W)	1	1.3
Silicon(< 1W)	8	10.4
Zener	3	180
Transformers	4	60
Integrated circuit,digital	7	350
Transducer	2	200
Connector, active pins	25	15
	Total	1692

Table 10

Reliability Assessment 4A17 Clock Assembly

Part Type	Quantity	Total Failure Rate (10^{-9} Failures/hours)
Resistors		
Metal film, fixed	13	18.2
Transistors		
Silicon(< 1W)	5	50
Capacitors		
Glass	6	12
Tantalum solid	2	28
Diodes		
Glass(< 1W)	1	1.3
Silicon(< 1W)	2	2.6
Integrated circuit, digital	7	350
Transformer	1	15
Crystal	1	20
	Total	497

Table 11

Reliability Assessment 4A17 Free Run Assembly

Part Type	Quantity	Total Failure Rate (10^{-9} Failures/hours)
Resistors		
Metal film, fixed	6	8.4
Wirewound, fixed	1	65
Transistors		
Silicon(> 1W)	2	112
Transformer	2	30
	Total	215.4

Table 12

Reliability Assessment 4A17 Inverter Assembly

Part Type	Quantity	Total Failure Rate (10^{-9} Failures/hours)
Resistors		
Wirewound, fixed	5	325
Metal film, fixed	2	2.8
Carbon composition, fixed	3	21
Capacitors		
Paper	1	40
Tantalum solid	2	28
Tantalum foil	1	21
Diodes		
Silicon(< 1W)	6	7.8
Zener	3	180
Transducer	1	100
Transistors		
Silicon(> 1W)	2	112
Coil	1	15
Connector, active pins	25	15
	Total	868

Table 13

Reliability Assessment 4A18 Synchronizer Assembly

Part Type	Quantity	Total Failure Rate (10^{-9} Failures/hours)
Diodes		
Glass(< 1W)	6	7.8
Silicon(< 1W)	4	5.2
Zener	3	180
Transistors		
Silicon(< 1W)	2	20
Capacitors		
Ceramic	2	30
Tantalum solid	2	42
Resistors		
Metal film, fixed	3	4.2
Wirewound, fixed	2	130
Transformer	1	15
Integrated circuit,digital	3	150
Connector, active pins	8	4.8
	Total	589

Table 14

Reliability Assessment 4A18 3 ϕ Inverter Assembly

Part Type	Quantity	Total Failure Rate (10^{-9} failures/hours)
Transistor		
Silicon(< 1W)	6	60
Silicon(> 1W)	6	336
Resistors		
Metal film, fixed	12	16.8
Wirewound, fixed	6	390
Carbon composition,fixed	3	21
Capacitors		
Tantalum wet slug	1	21
Paper	1	40
Transformer	1	15
Inductor	1	15
Connector, active pins	18	10.8
	Total	837

Table 15

Reliability Assessment 4A18 1 ϕ Inverter Assembly

Part Type	Quantity	Total Failure Rate (10^{-9} Failures/hours)
Resistors		
Metal film, fixed	4	5.6
Wirewound, fixed	4	260
Carbon composition,fixed	4	28
Transistors		
Silicon(< 1W)	2	20
Silicon(> 1W)	4	224
Transformer	1	15
Coil	1	15
Capacitors		
Tantalum wet slug	1	21
Paper	1	40
Fuse	2	200
Connectors, active pins	14	8.4
	Total	971

Table 16

Reliability Assessment 4A19 Heater & DC Power Assembly

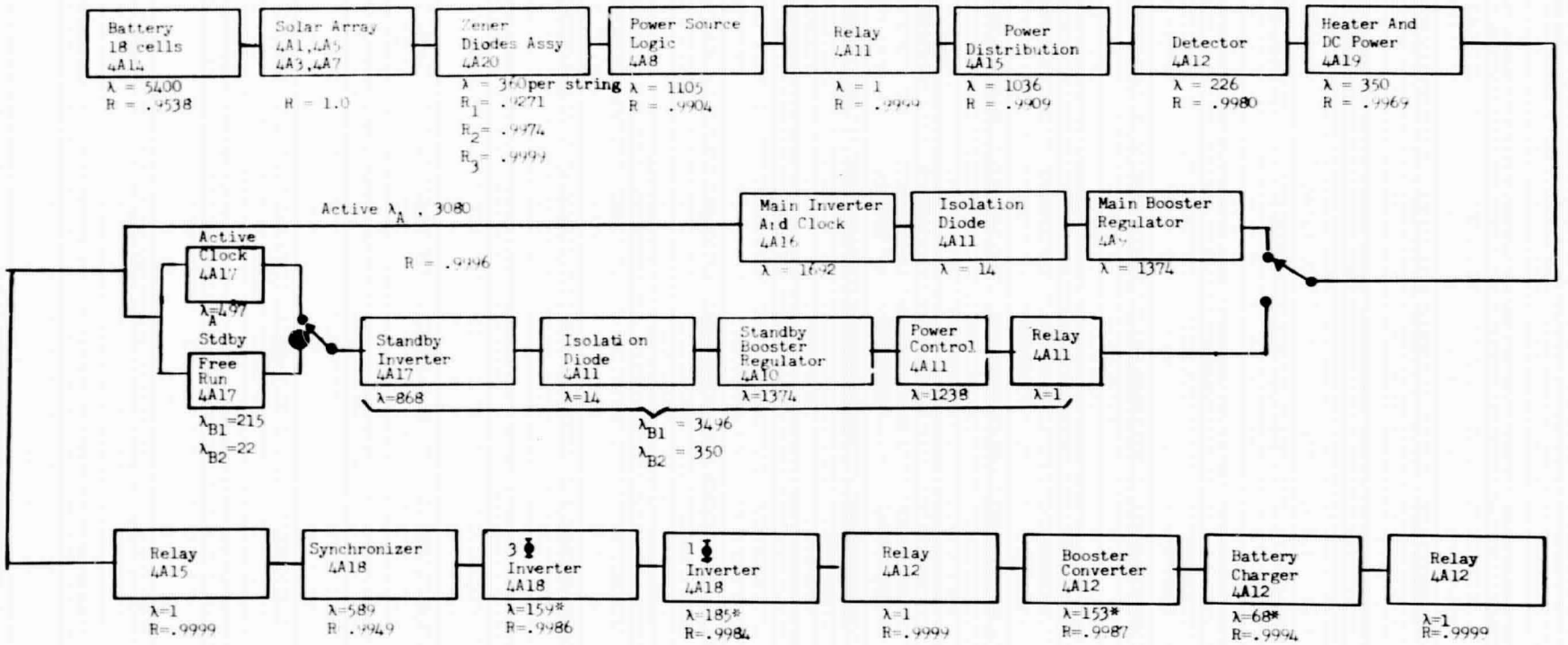
Part Type	Quantity	Total Failure Rate (10^{-9} Failures/hours)
Resistors		
Metal film, fixed	7	9.8
Carbon composition, fixed	2	14
Wirewound, fixed	2	130
Diode		
Silicon(< 1W)	9	11.7
Relay	1	1.0
Transformer	2	30
Capacitors		
Tantalum solid	3	42
Tantalum foil	2	42
Transistors		
Silicon(< 1W)	2	20
Connectors, active pins	84	50.4
	Total	350

Table 17

Reliability Assessment 4A20 Zener Assembly

Part Type	Quantity	Total Failure Rate (10^{-9} Failures/hours)
Diode, Zener	6(per string)	360

Note: There are 6 zener diodes per string and 24 strings in the 4A20 Zener Assembly.



System Reliabilities:

Case 1 R_{S1} = .8544 (with all 24 strings of Zeners in 4A20 required for success)

Case 2 R_{S2} = .9141 (with 23 of 24 strings of Zeners in 4A20 req'd for success)

Case 3 R_{S3} = .9215 (with 22 of 24 strings of Zerers in 4A20 req'd for success)

Notes: 1. λ = failure rate in failures/10^9 hours

2. * for units operating only 10% of mission time. λ = .19 (λ active) see text (k)β

3. The reliability of 4A17 clock and Free Run is assumed ~ 1.0

Figure A-1. Mariner-Mars Power System Reliability Block Diagram

Reference 1

Schematic Diagram	Unit	JPL Drawing No.	Revision	Date
Power source logic	4A8	10013178	F	7-6-67
Booster regulator	4A9/4A10	10013154	F	7-5-67
Power control	4A11	10012971	F	7-7-67
Battery charger	4A12	10013175	F	10-13-67
Power distribution	4A15	10013157	F	7-5-67
Main inverter	4A16	10012721	E	10-16-67
Standby inverter	4A17	10016056	F	7-5-67
400 Hz, 1ϕ and 3ϕ inverter	4A18	10001220	E	7-5-67
Heater and dc power distribution	4A19	10016156	None	7-5-67

APPENDIX B

RELIABILITY ASSESSMENT OF SELECTED CIRCUITS AND SYSTEMS

APPENDIX B

RELIABILITY ASSESSMENT OF SELECTED CIRCUITS AND SYSTEMS

Reliability assessments of key circuits and systems are delineated in this appendix. The reliability analysis ground rules and assumptions utilized are listed in Appendix A.

Tables B-1 through B-19 present in tabular form the part type, quantity, and reliability assessment of various circuits. Selected circuit diagrams corresponding to the aforementioned tables are depicted in Figures B-1 through B-11.

The circuit, reliability, and failure detector block diagrams of the 2.4-kHz inverter are shown in Figures B-12, B-13, and B-14, respectively. Corresponding diagrams for the battery-boost regulator are depicted in Figures B-15, B-16, and B-17. The circuit and reliability block diagrams of the 400-Hz inverters are shown in Figures B-18 and B-19.

Reliability assessments have been made on the existing Mariner power system with no redundancy in the main power chain (i.e., boost-line regulator and 2.4-kHz inverter). The block diagram and resultant system reliability are shown in Figure B-20. Table B-20 summarizes the redundant and nonredundant designs.

Figure B-21 depicts the reliability block diagram for model System No. 2, which incorporates a shunt limiter and a battery-boost regulator. Figure B-22 shows an overall reliability improvement from 0.9251 to 0.9345 via redundancy inclusion in the power distribution and share mode detector circuitry. The reliability assessments for model System No. 1 are virtually identical to model System No. 2, since the PWM buck regulator reliability (0.9996) is nearly the same as the shunt regulator (0.9997).

Figure B-23 depicts the reliability block diagram for the recommended buck-boost regulator system.

Table B-1. Reliability Assessment of Figure B-1 Current Monitor

Part Type	Quantity	Total λ
Transformer	1	15
Mag amplifier	1	15
Diodes (< 1 W)	8	10.4
Total effective λ		40.4
R = 0.9996		

Note: The resistors and capacitors are not included in the parts count because the computed reliability of their circuit configuration is 1.

Table B-2. Reliability Assessment of Figure B-2 Majority Voting Time Delay Circuit

Part Type	Quantity	Total λ
Transistors (<1 W)	15	150.0
Diodes (<1 W)	3	4.2
Resistors, metal film	42	58.8
Capacitors, solid tantalum	6	72.0
Total		285.0
R = 1.0		

Note: The computed reliability of this circuit configuration is 0.999997 and is assumed = 1.0.

Table B-3. Reliability Assessment of Figure B-3 Fully Redundant Relay Driver

Part Type	Quantity	Total λ
Transistors (<1 W)	16	160.0
Diodes (<1 W)	12	15.6
Resistors, metal film	46	64.4
Coils	2	30.0
Total		270.0
R = 1.0		

Note: The computed reliability of this circuit configuration is 0.999997 and is assumed to be 1.0.

Table B-4. Reliability of Three-Level Voltage Detector

Part Type	Quantity	Total λ
Resistors, metal film	26	36.4
Capacitors, solid tantalum	2	28.0
Diodes (<1 W)	7	9.1
Diodes, zener	2	120.0
Transistors (<1 W)	8	80.0
Transistor, dual amplifier	1	20.0
Total		293.5

Note: R = 0.9999 (with two of three voltage detectors required for success).

Table B-5. Reliability Assessment of Figure B-4 Majority Voting Gates

Part Type	Quantity	Total λ
Resistors, metal film	12	16.8
Transistors (< 1 W)	6	60.0
Diodes (< 1 W)	3	3.9
Total		80.7
	R = 1.0	

Note: The computed reliability of this circuit configuration is 1.0.

Table B-6. Reliability Assessment of Figure B-5 Fully Redundant Emitter – Follower Supply

Part Type	Quantity	Total λ
Diodes (< 1 W)	2	2.6
Resistors, metal film	2	2.8
Total effective λ		5.4
	R = 0.9999	

Note: The parallel zeners and quaded transistors circuit are not included in the parts count because their computed reliability is 0.99998 and is assumed = 1.0.

Table B-7. Reliability Assessment of Figure B-6 Low-Level, Fully Redundant Voltage Detector

Part Type	Quantity	Total λ
Transistors (< 1 W)	12	120.0
Diodes (< 1 W)	8	10.4
Resistors, metal film	30	42.0
Capacitors, solid tantalum	6	72.0
Total		244.4
	R = 1.0	

Note: The computed reliability of this configuration is 0.999997 and is assumed = 1.0.

Table B-8. Reliability Assessment of Figure B-7, 3.3 Volt Series Regulator Type Fully Redundant Reference Supply

Part Type	Quantity	Total λ
Resistors, metal film	40	56.0
Capacitors, solid tantalum	7	84.0
Diodes, zener	3	180.0
Diodes (< 1 W)	6	7.8
Transistors (< 1 W)	18	180.0
Total		507.8
R = 1.0		

Note: The computed reliability of this circuit configuration is = 0.99999 and is assumed = 1.0.

Table B-9. Reliability Assessment of Figure B-8 Fail-Safe Rectifier and Filter

Part Type	Quantity	Total λ
Coil	1	15
Total effective λ		15
R = 0.9998		

Note: The diodes and capacitors are in quad configuration whose computed reliability is 1.0.

Table B-10. Reliability Assessment of Figure B-9 Three-Level Current Detector Fully Redundant

Three-Level Current Sensor No. 1		
Part Type	Quantity	Total λ
Transistors (< 1 W)	10	100.0
Diodes (< 1 W)	5	6.5
Diodes, zener	2	120.0
Resistors, metal film	20	28.0
Total for Current Sensor No. 1		254.5

Note: R = 0.9999 (with two of three current sensors required for success).

Table B-11. Reliability Assessment of Figure B-10 Detector of Gross Frequency Variations

Part Type	Quantity	Total λ
Transformer	1	15.0
Resistors, metal film	6	8.4
Diodes (< 1 W)	4	5.2
Total effective λ		21.6
R = 0.9997		

Note: The capacitors are not included in the parts count because the computed reliability is 1.0.

Table B-12. Reliability Assessment Fail-Safe Low-Level Driver Stage

Part Type	Quantity	Total λ
Transformer	1	15.0
Diodes (< 1 W)	4	5.2
Resistors, metal film	8	11.2
Total effective λ		31.4
R = 0.9997		

Note: The resistor and transistors in the push-pull quad circuit configuration are not included in the parts count because the computed reliability is 1.0.

Table B-13. Reliability Assessment of Conjugate Amplifiers and Detectors

Conjugate Amplifier and Detector No. 1		
Part Type	Quantity	Total λ
Diodes (< 1 W)	45	58.5
Resistors, metal film	96	134.4
Capacitors, ceramic	12	180.0
Diodes, zener	6	360.0
Inductors	6	90.0
Transistors (< 1 W)		540.0
Total		1363.0
R = 0.9996 (with two of three conjugate amplifier and detector required for success)		

Note: Parts count of majority voting gates are not inclued because the computed reliability of their circuit configuration is 1.0.

Table B-14. Reliability Assessment Battery Charger

Part Type	Quantity	Total λ
Resistors, metal film	10	14.0
wirewound	2	130.0
Capacitor, solid tantalum	1	14.0
Diode, (> 1 W)	1	14.0
zener	1	60.0
Transistors, (> 1 W)	2	112.0
(< 1 W)	3	30.0
Total		360.0
	R = 0.9994	

Note: This circuit operates only 10 percent of mission time.
λ = 0.19 (active λ) = 68.4 (see Appendix A).

Table B-15. Reliability Assessment of Shunt, Figure B-11

Part Type	Quantity	Total λ
Resistors, metal film	2	2.8
wirewound	4	260.0
Diodes (> 1 W)	3	42.0
Transistors (> 1 W)	2	112.0
Total		416.8

Table B-16. Reliability Assessment of I_1

Part Type	Quantity	Total λ
Resistors, metal film	5	7.0
wirewound	2	130.0
Transistors (> 1 W)	2	112.0
Diodes (> 1 W)	3	42.0
Total		291.0

Table B-17. Reliability Assessment of I_2

Part Type	Quantity	Total λ
Resistors, metal film	1	1.4
wirewound	8	520.0
Transistors (> 1 W)	2	112.0
Diodes (> 1 W)	3	42.0
Total		675.4

Table B-18. Reliability Assessment of Synchronizer

Part Type	Quantity	Total λ
Integrated Circuits, Digital	3	150.0
Diodes (< 1 W)	5	6.5
Transistor (< 1 W)	1	10.0
Resistor, metal film	1	1.4
Total		167.9
R = 0.9985		

Table B-19. Reliability Assessment of Bias Supply and 2.4 kHz Excitation for Synchronizer

Part Type	Quantity	Total λ
Transformer	1	15.0
Diodes (< 1 W)	14	18.2
Resistors, metal film	6	8.4
Total effective λ		31.6
R = 0.9997		

Note: The capacitors, zeners, and transistors are in quad redundant configuration and are not included in the parts count because their computed reliability is 0.999994 and is assumed = 1.0.

Table B-20. Comparison of Reliability Assessments for Redundant and Nonredundant Mariner Power System

Case	Condition	Mariner Systems	
		Redundant	Nonredundant
1	With all 24 strings of zeners in 4A20 required for success	0.8544	0.8316
2	With 23 of 24 strings of zeners in 4A20 required for success	0.9191	0.8947
3	With 22 of 24 strings of zeners in 4A20 required for success	0.9215	0.8969

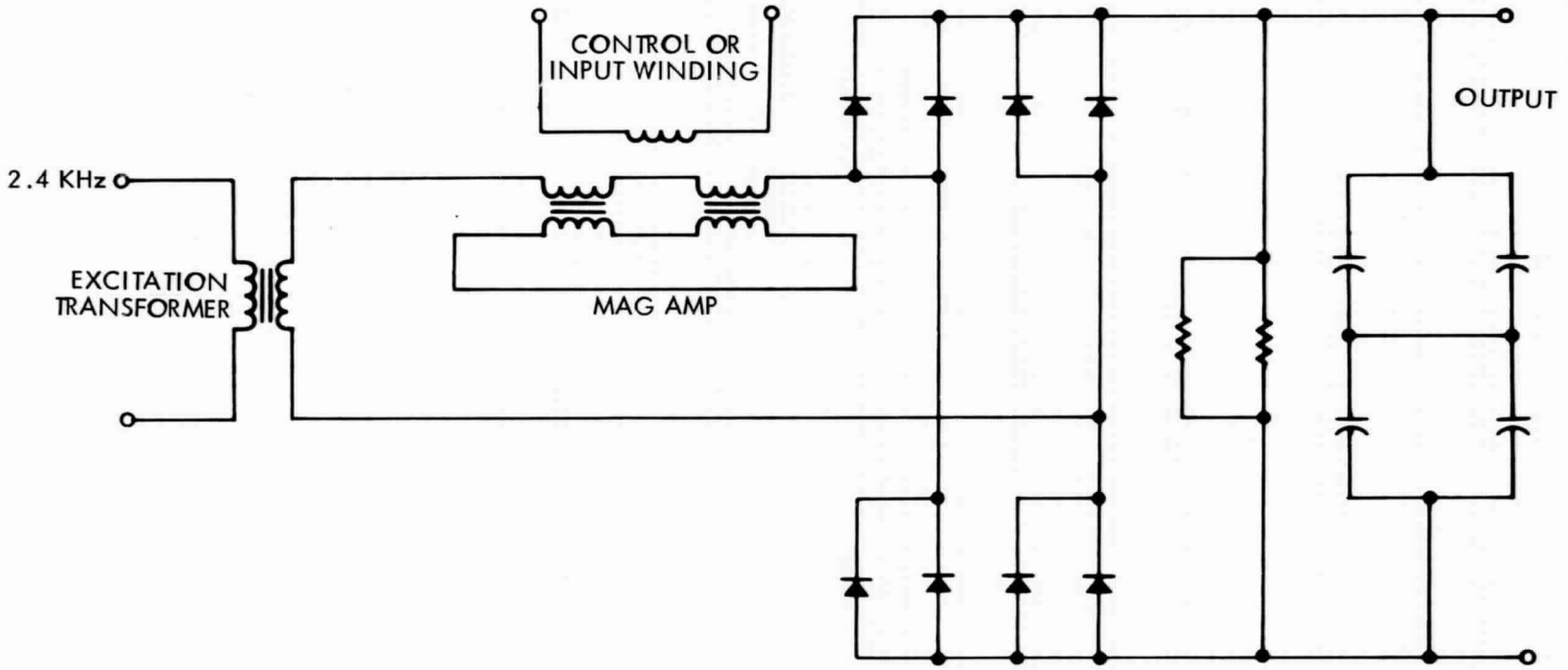


Figure B-1. Current Monitor Partially Redundant

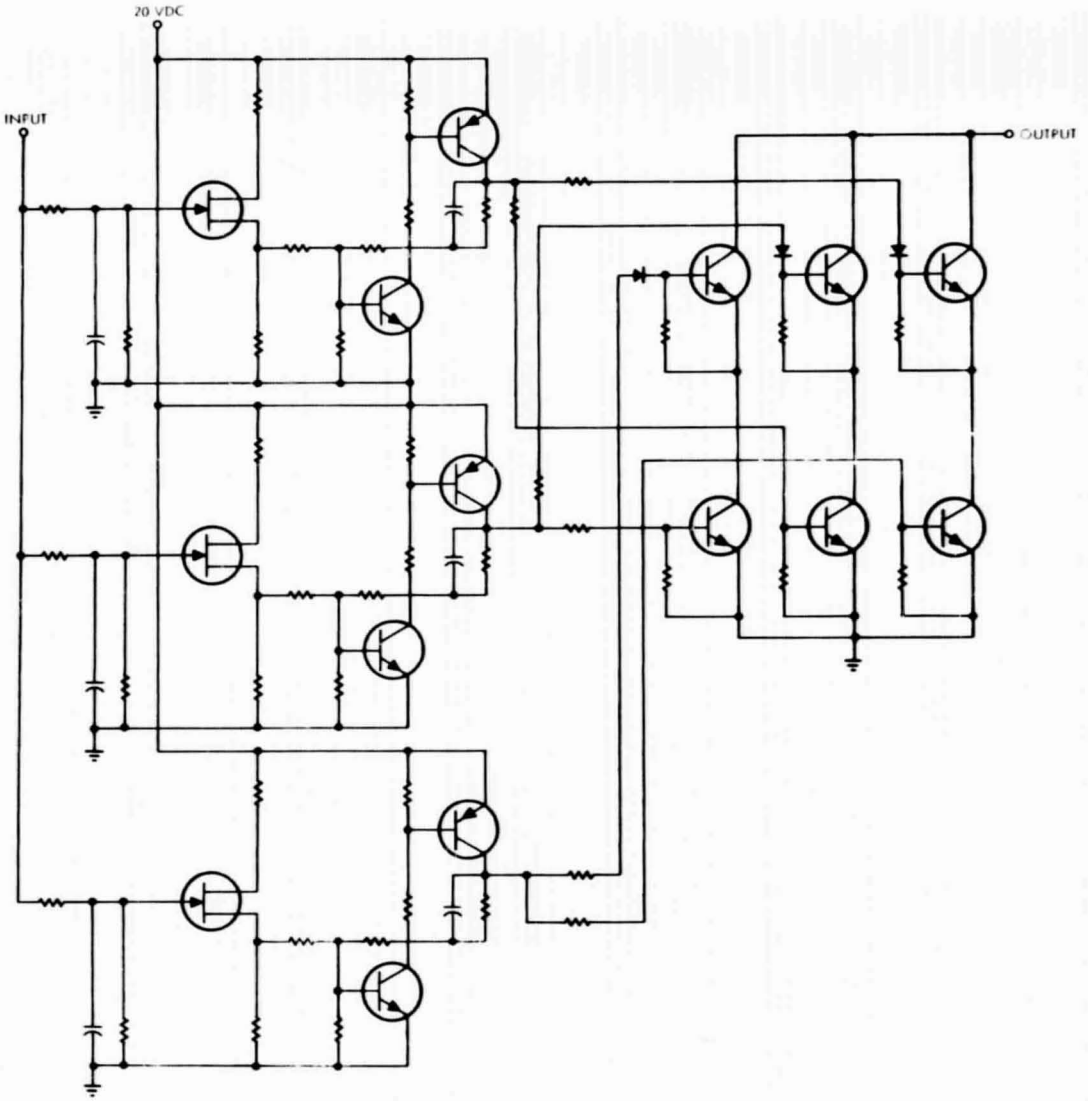


Figure B-2. Majority Voting Time Delay Circuit

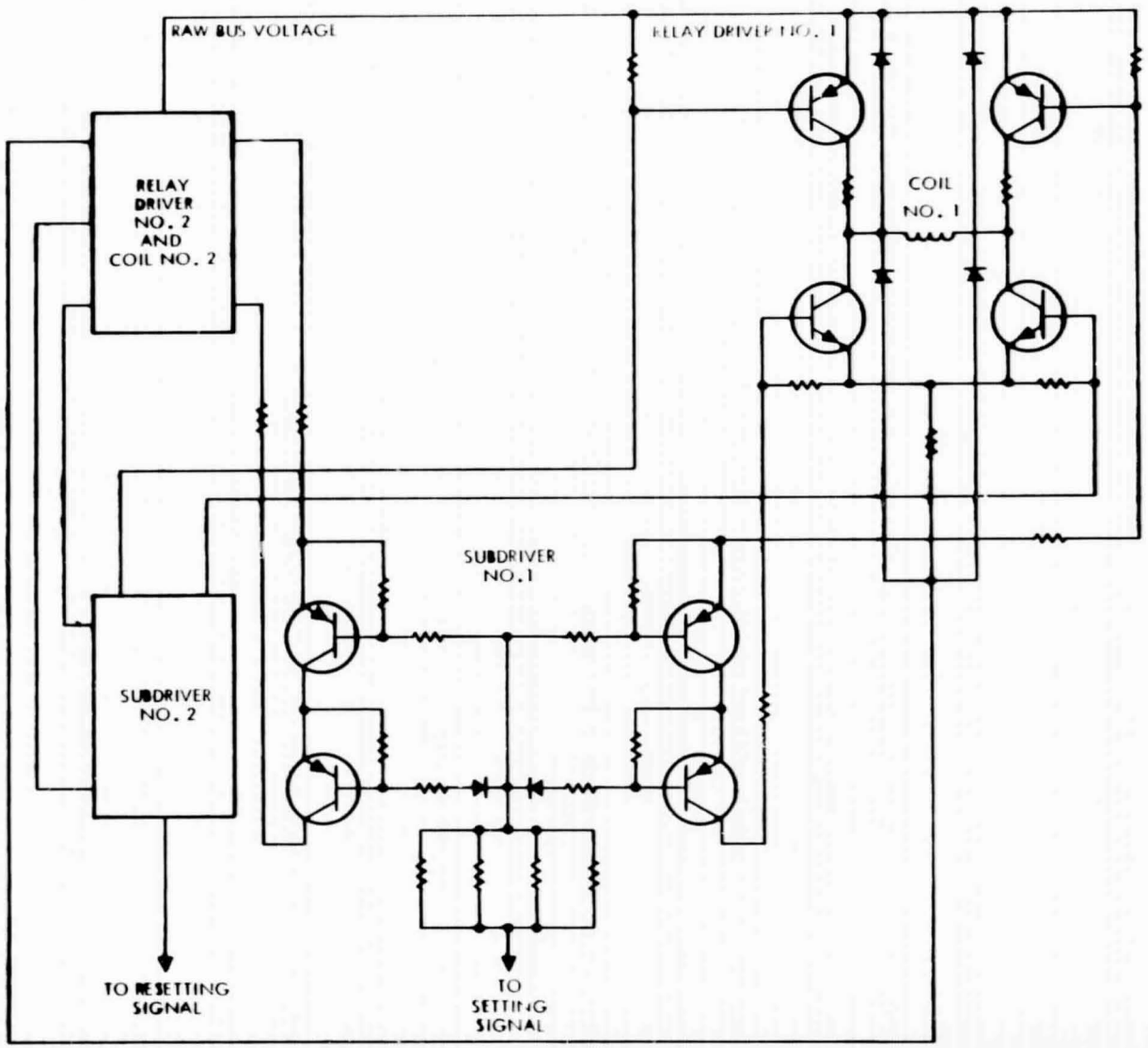


Figure B-3. Fully Redundant Relay Driver

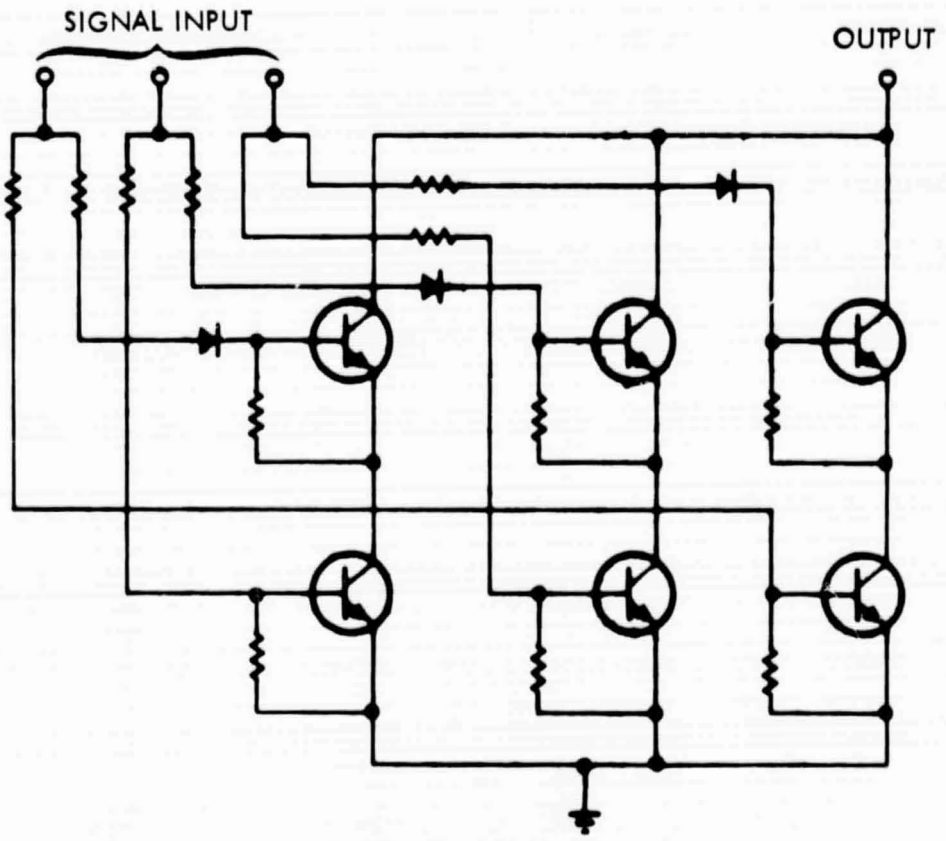


Figure B-4. Majority Voting Gates

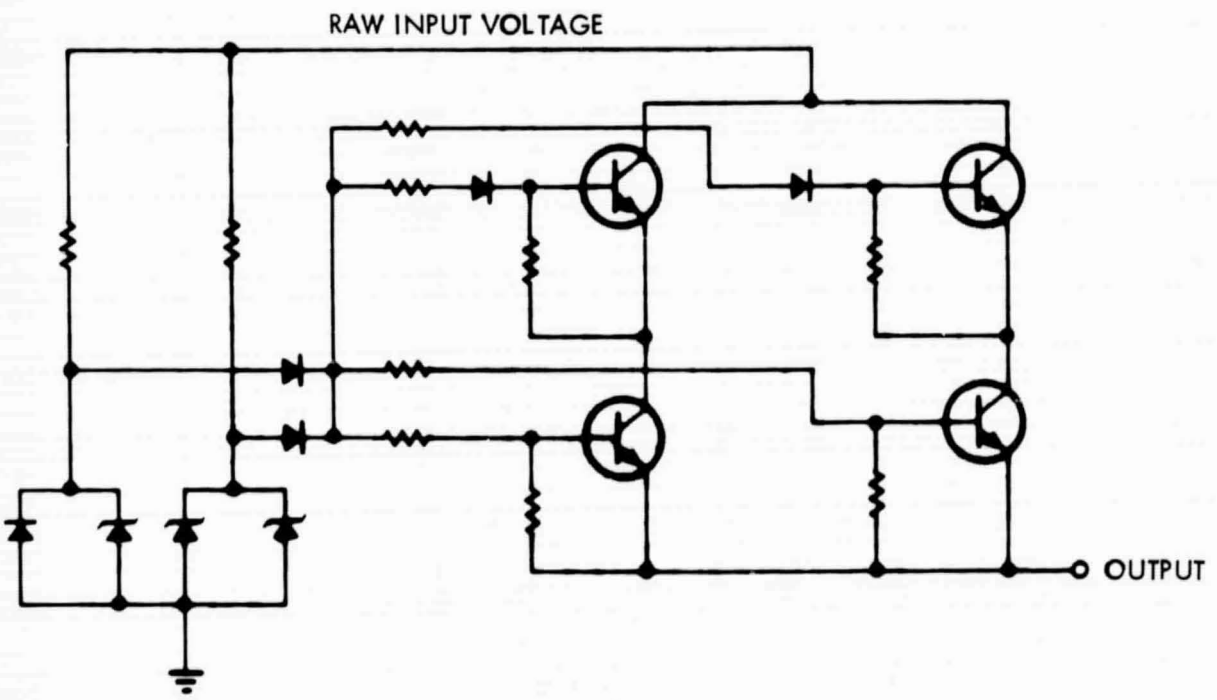


Figure B-5. Fully Redundant Emitter-Follower Supply

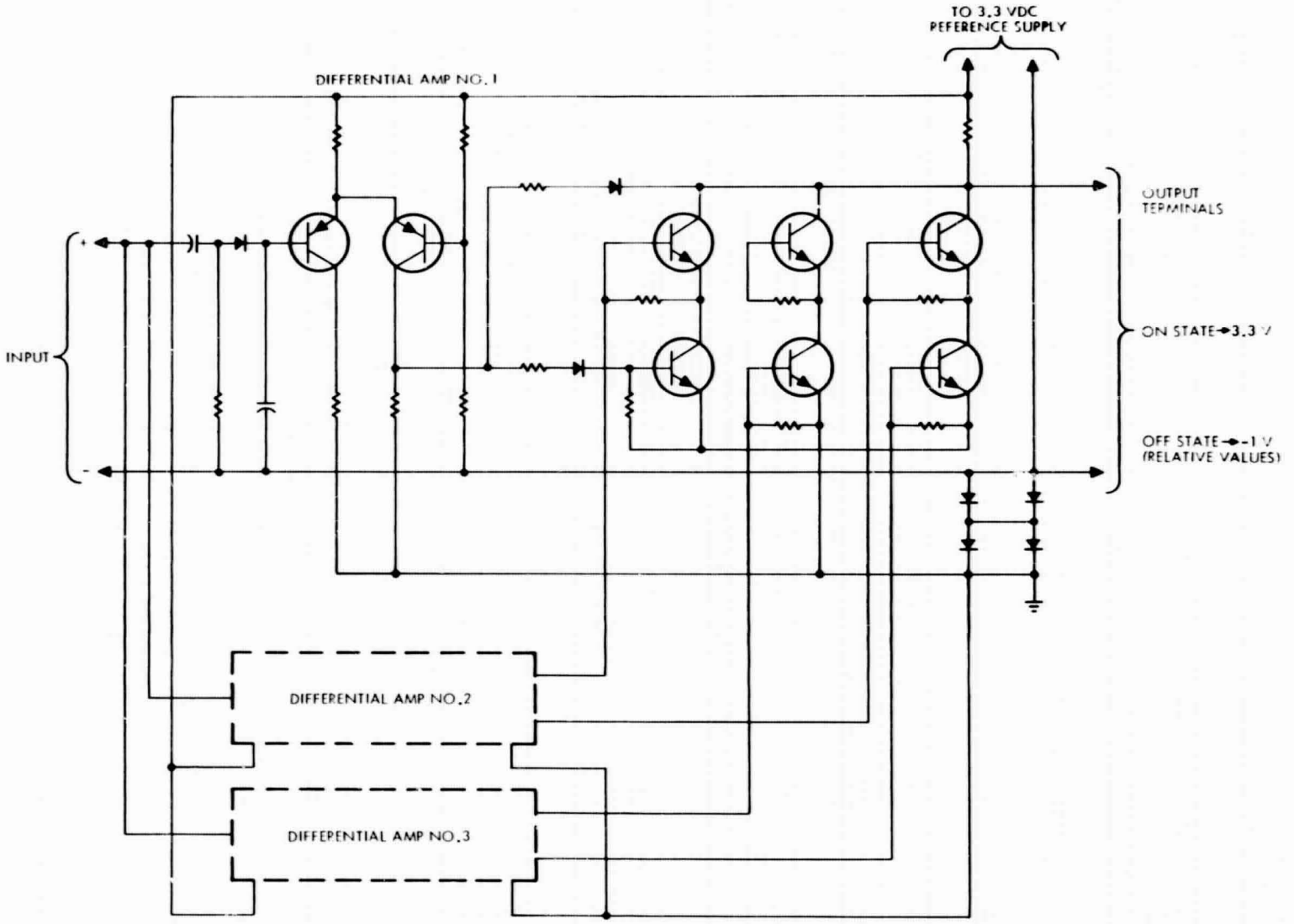


Figure B-6. Low Level Fully Redundant Voltage Detector

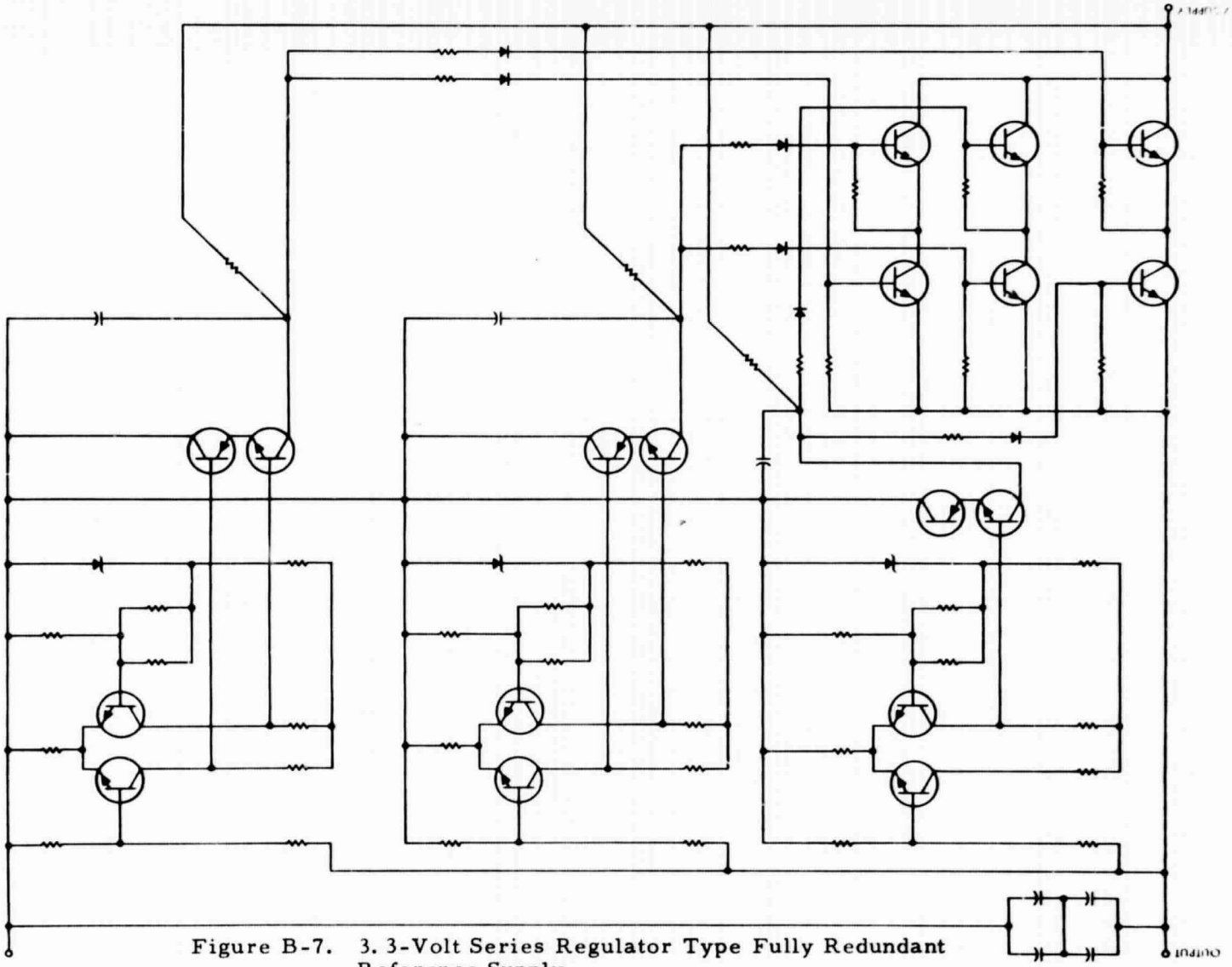


Figure B-7. 3.3-Volt Series Regulator Type Fully Redundant Reference Supply

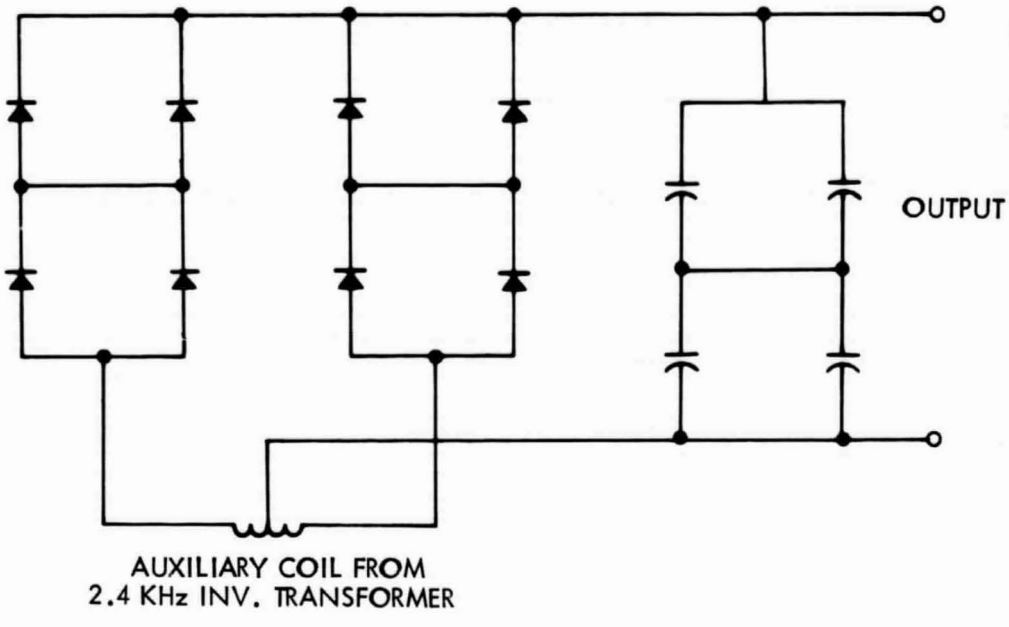


Figure B-8. Fail Safe Rectifier and Filter

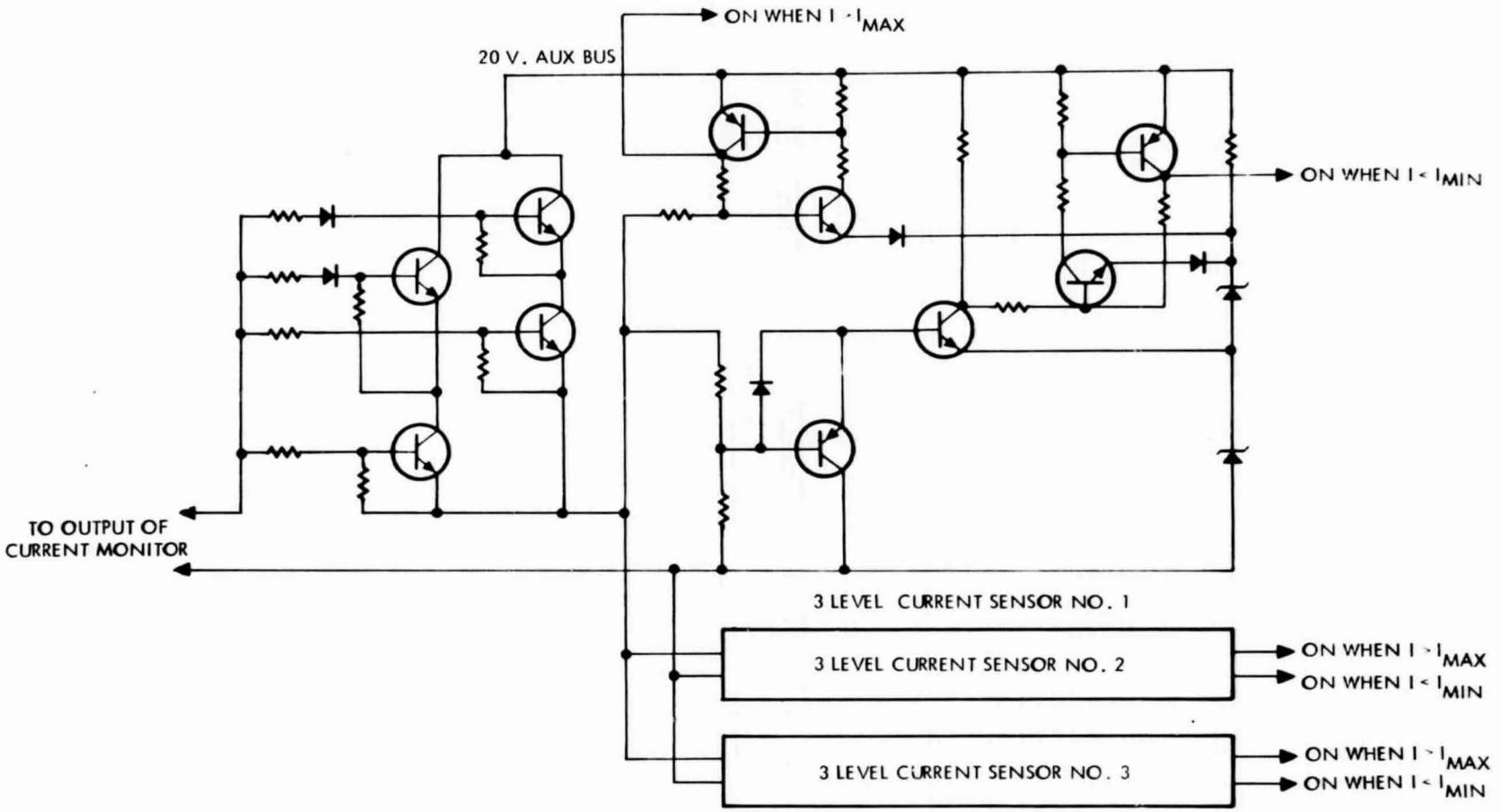


Figure B-9. Three-Level Current Detector Fully Redundant

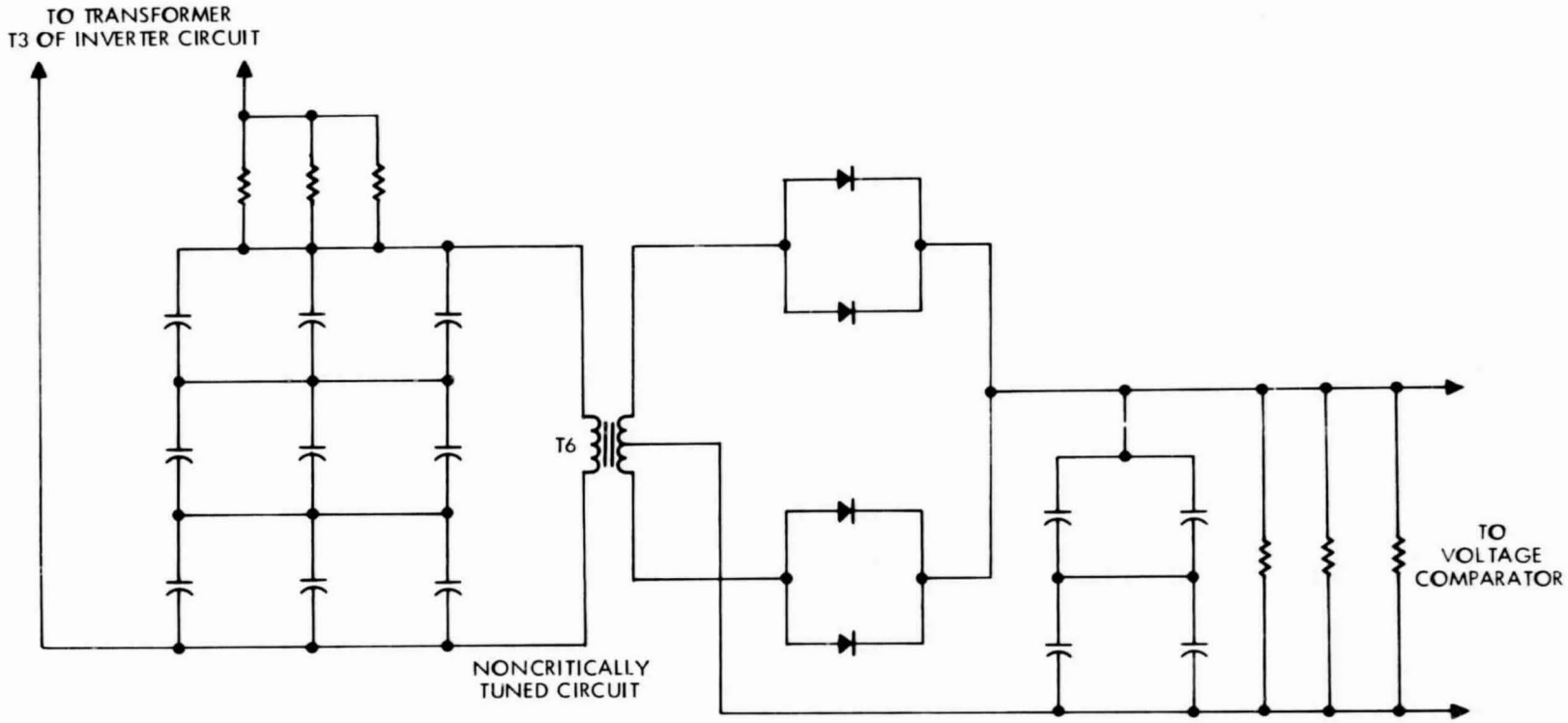


Figure B-10. Detector of Gross Frequency Variations

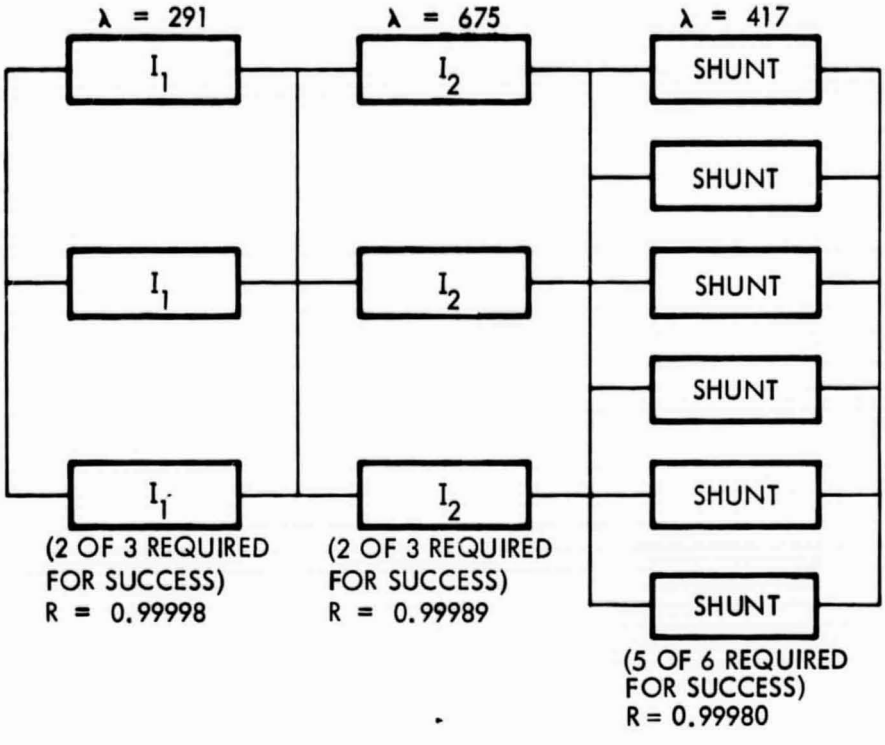


Figure B-12. Reliability Assessment of Shunt Assembly

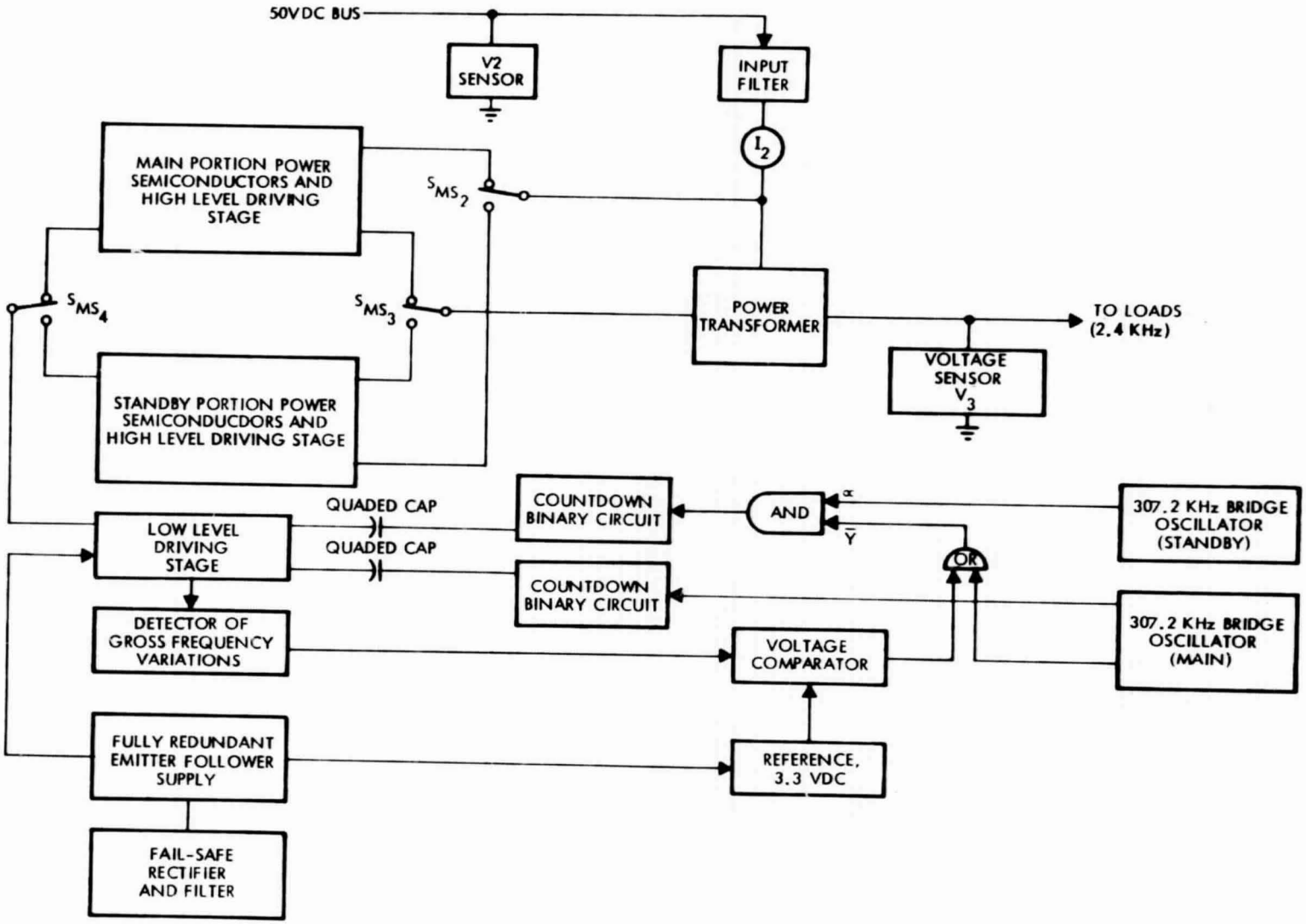
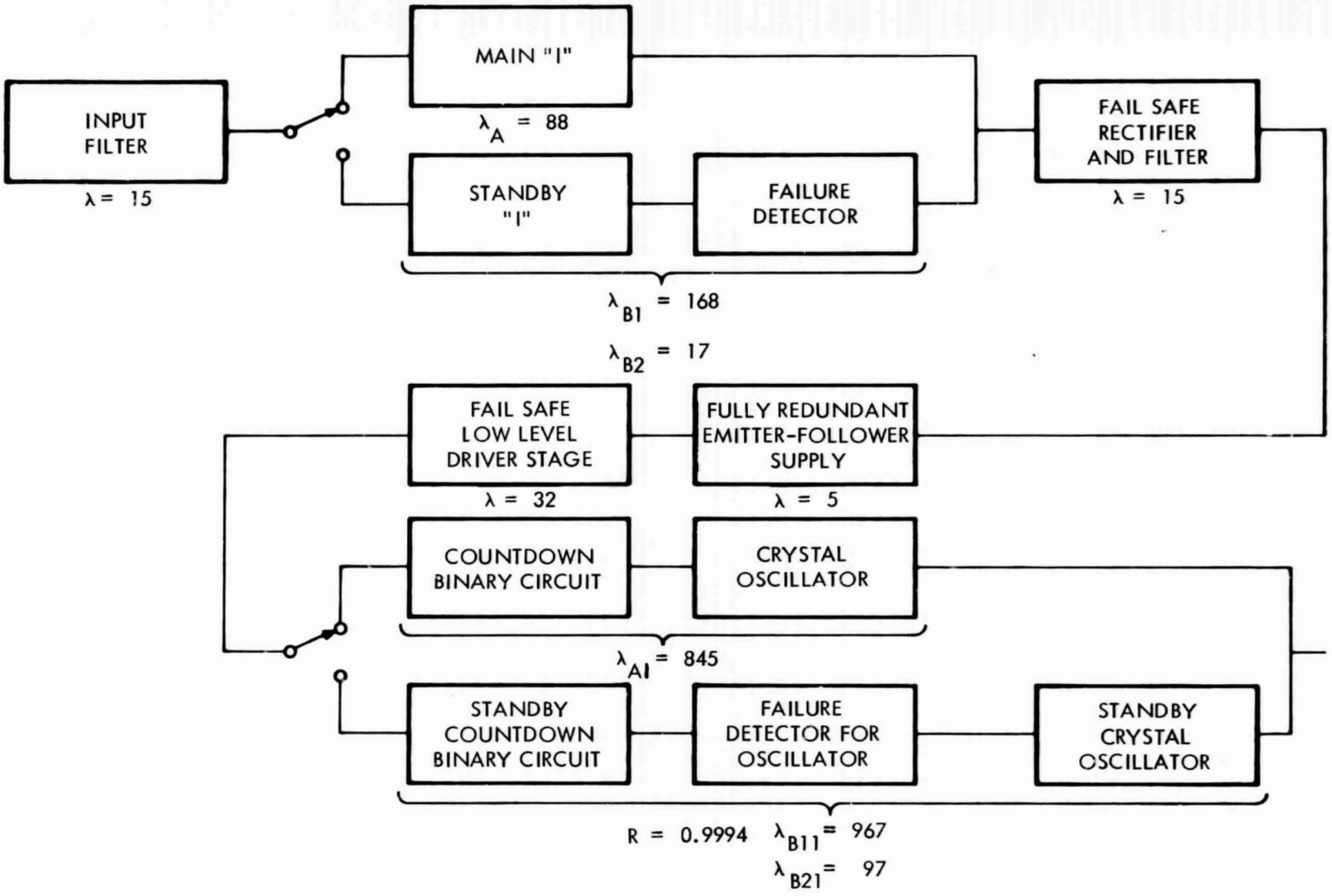
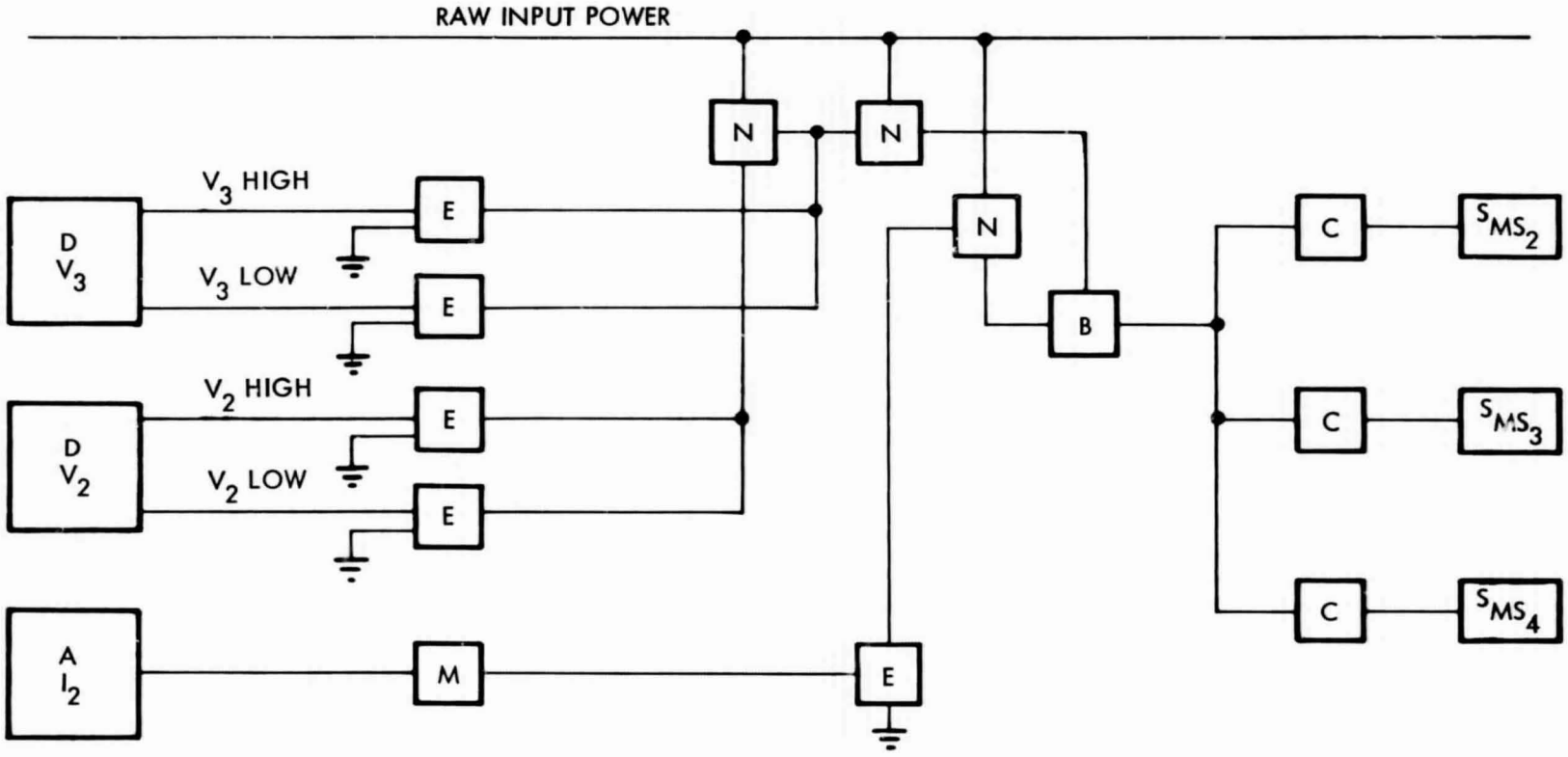


Figure B-13. Block Diagram, 2.4 kHz Inverter



B-14. Reliability Block Diagram of 2.4 kHz Inverter



A CURRENT MONITOR
B MAJORITY VOTING ONE SECOND DELAY
C REDUNDANT RELAY DRIVER
D TWO LEVEL VOLTAGE DETECTOR
E MAJORITY VOTING GATES
N INVERTED MAJORITY VOTING GATES
S RELAY

Figure B-15. Block Diagram, Failure Detector for 2.4 kHz Inverter

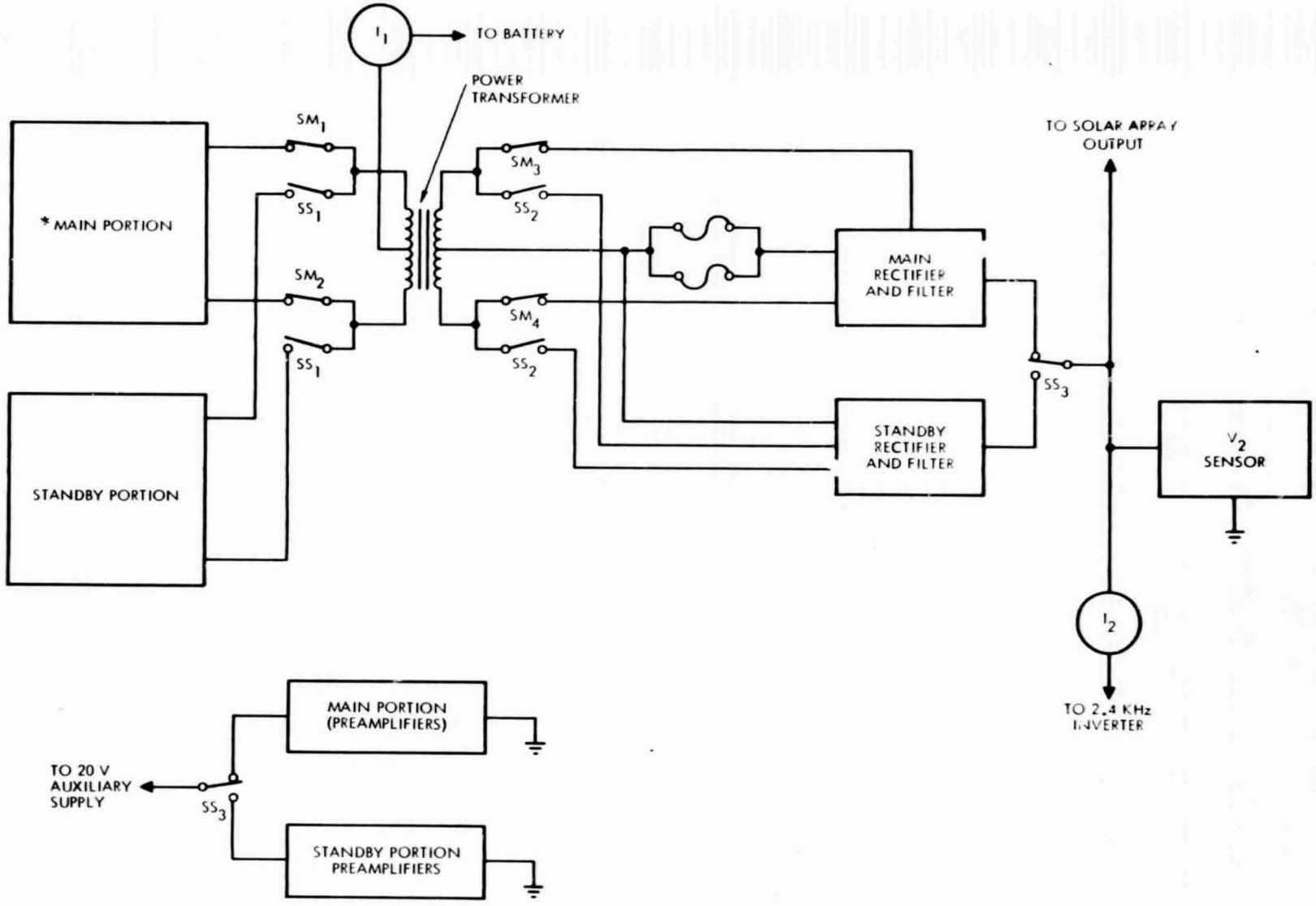


Figure B-16. Block Diagram of Battery Boost Regulator

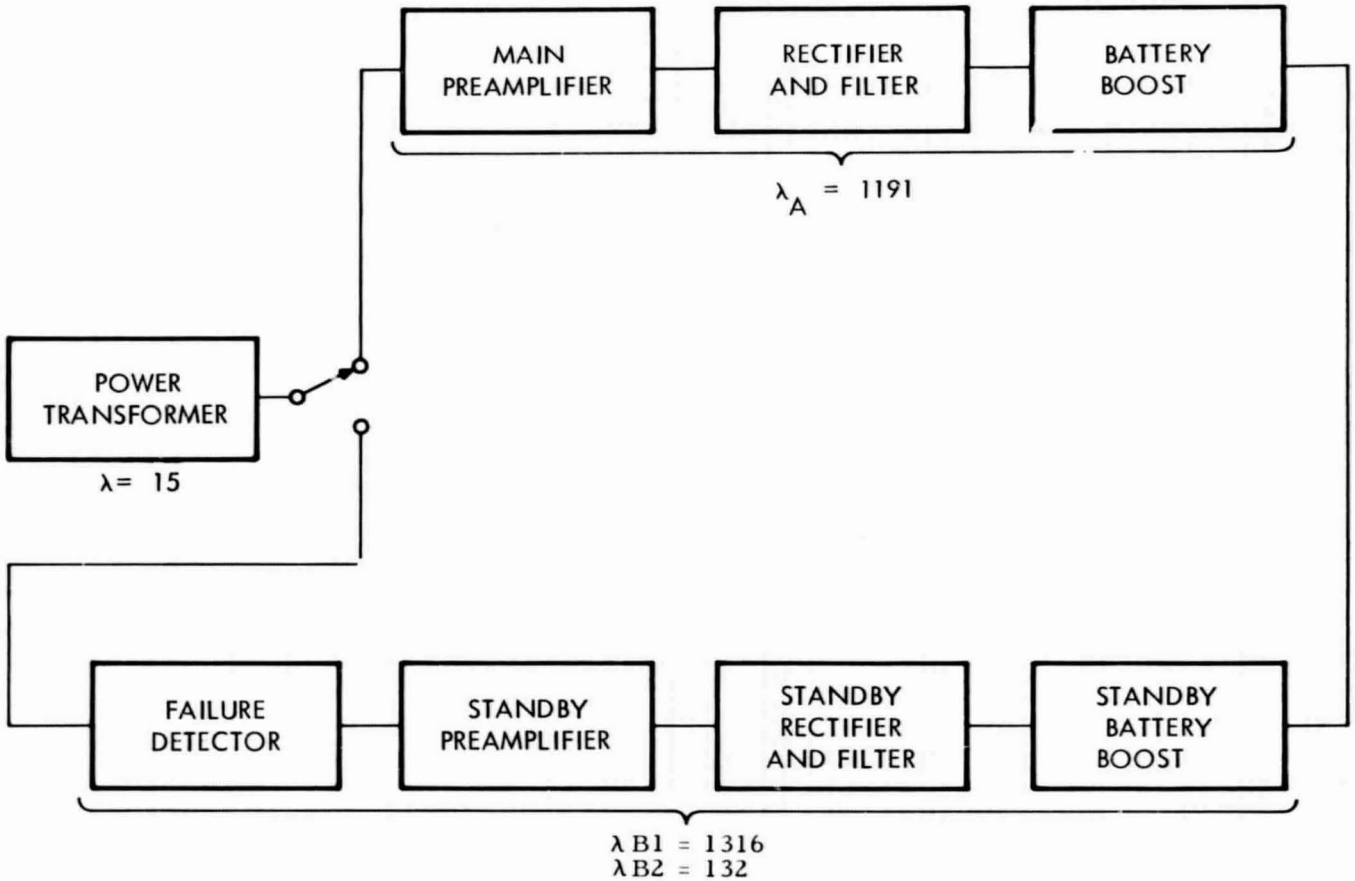
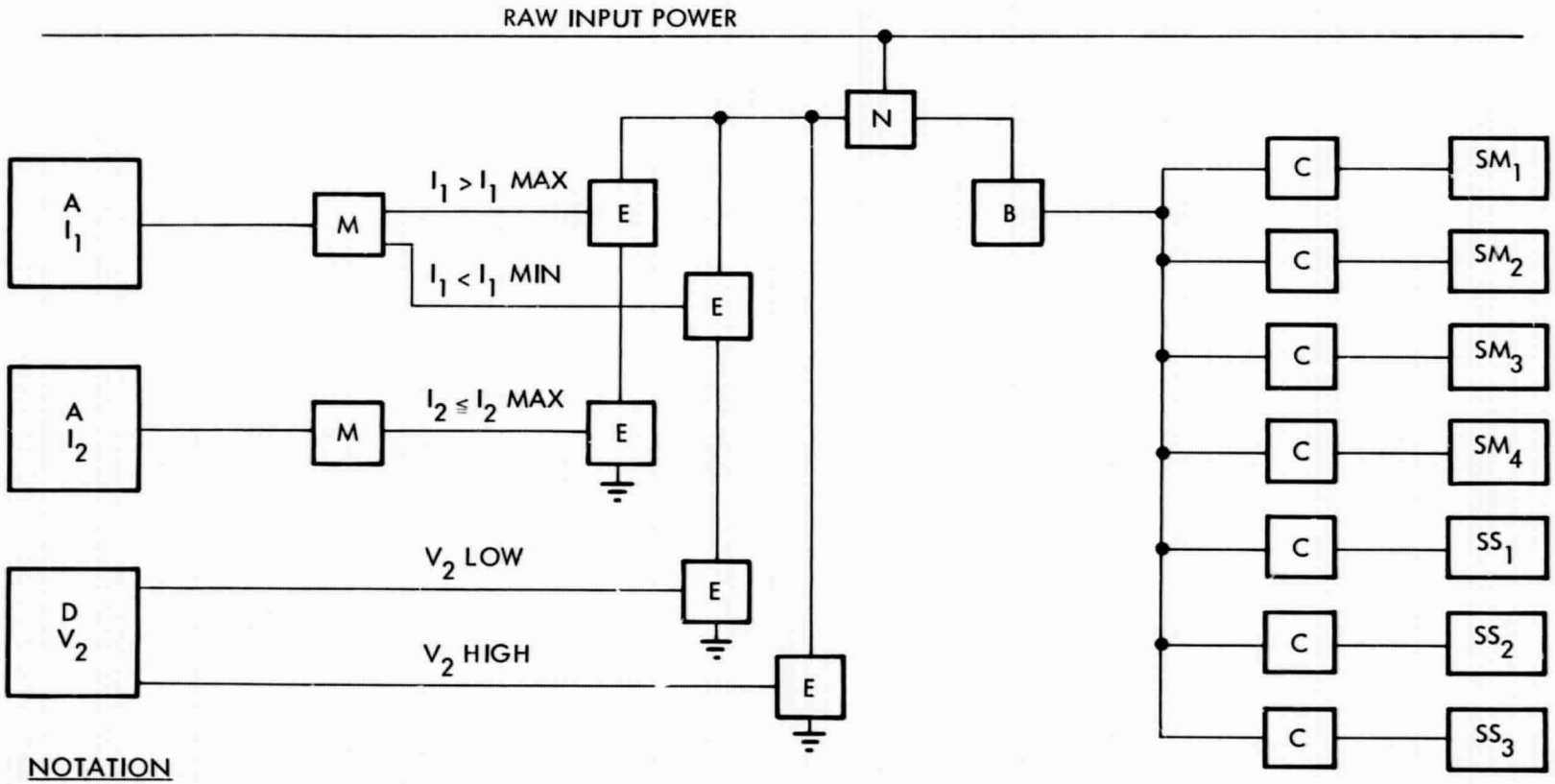


Figure B-17. Reliability Block Diagram of Battery Boost Regulator



NOTATION

A	CURRENT MONITOR
B	MAJORITY VOTING ONE SECOND DELAY
C	REDUNDANT RELAY DRIVER
E	MAJORITY VOTING GATE
M	CURRENT LEVEL DETECTOR
N	INVERTED MAJORITY VOTING GATE
S	RELAY

Figure B-18. Block Diagram, Failure Detector for Battery Boost Regulator

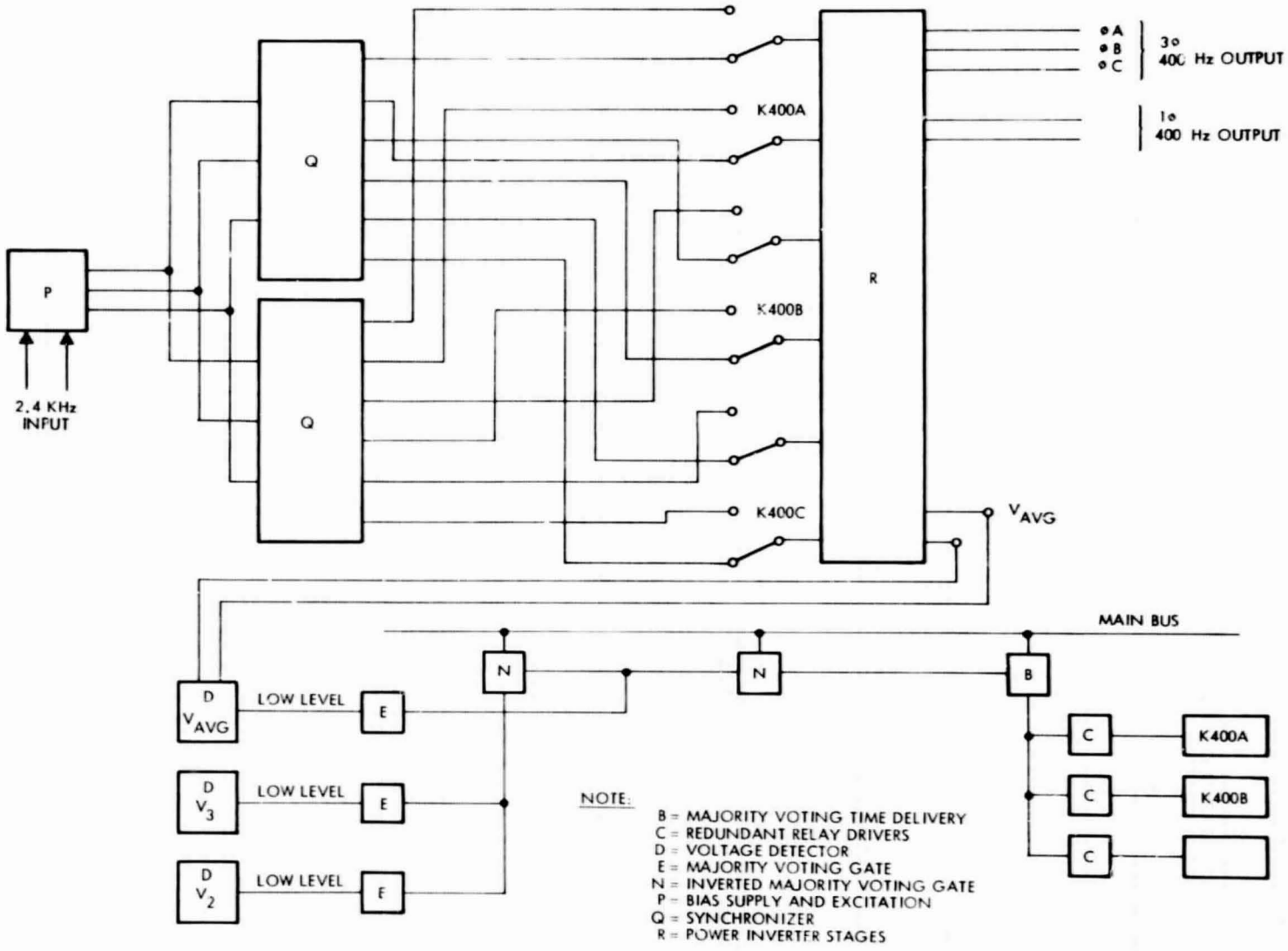
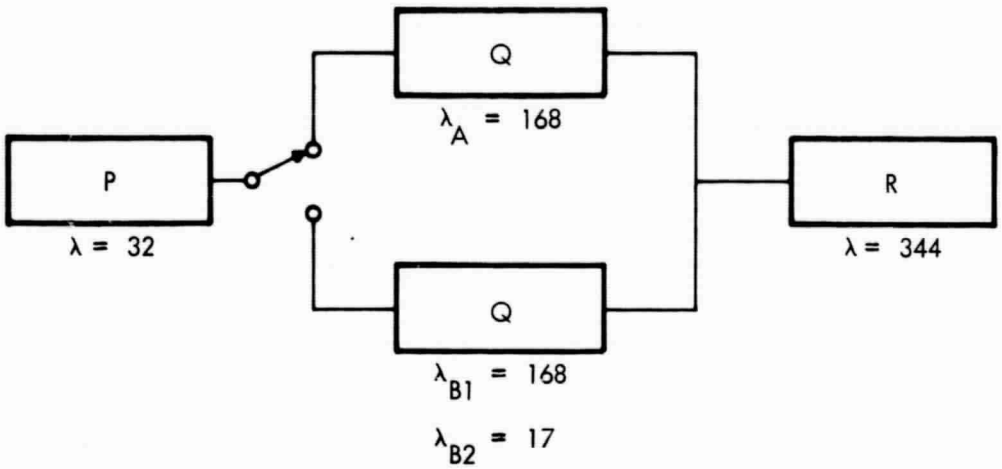


Figure B-19. Block Diagram, 400-Hz Inverters, Including Fail-Safe Excitation and Failure Detector, and Standby Synchronizer



RELIABILITY BLOCK DIAGRAM

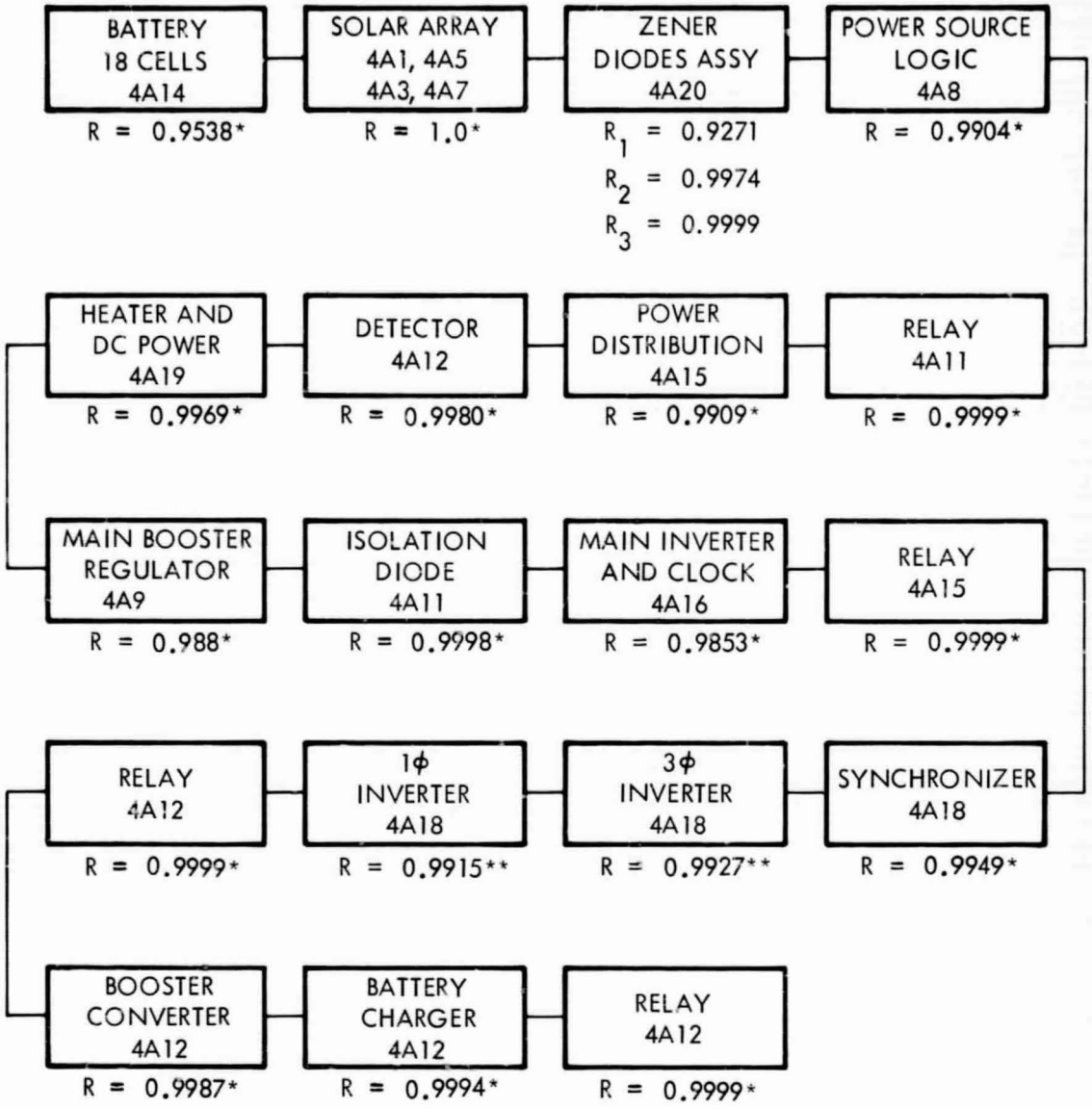
R_S = 0.9967

NOTES:

1) R CONSISTS OF THE 3φ AND 1φ INVERTERS AND OPERATES ONLY 10 PERCENT OF THE MISSION TIME PER YOUR INSTRUCTIONS

2) THE FAILURE DETECTOR IS NOT INCLUDED BECAUSE IT OPERATES ONLY 10 PERCENT OF THE MISSION TIME AND IS ASSUMED = 1.0

Figure B-20. Reliability Block Diagram of 400 Hz Inverters including Fail Safe Excitation and Failure Detector, and Standby Synchronizer



SYSTEM RELIABILITIES: CASE 1 R_{S1} = 0.8316 (WITH ALL 24 STRINGS OF ZENERS IN 4A20 REQUIRED FOR SUCCESS)

CASE 2 R_{S2} = 0.8947 (WITH 23 OF 24 STRINGS OF ZENERS IN 4A20 REQUIRED FOR SUCCESS)

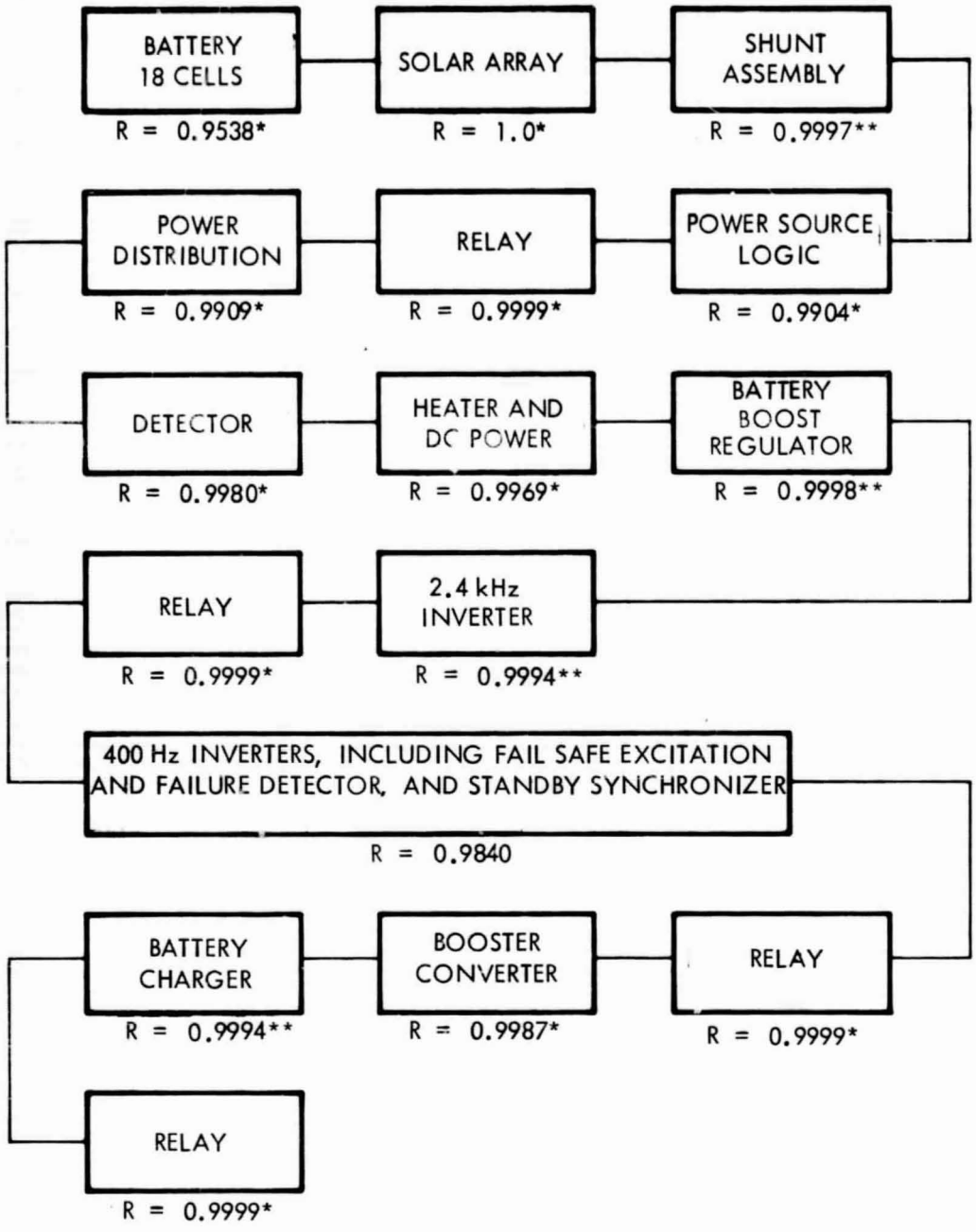
CASE 3 R_{S3} = 0.8969 (WITH 22 OF 24 STRINGS OF ZENERS IN 4A20 REQUIRED FOR SUCCESS)

NOTES:

1) * THE RELIABILITY ASSESSMENTS FOR THE UNITS ARE SHOWN IN APPENDIX A

2) **THESE UNITS OPERATE 100% OF THE MISSION TIME PER YOUR INSTRUCTIONS- FAILURE RATES VALUES ARE IN REFERENCE 1.

Figure B-21. Mariner-Mars Power System (With No Redundancy) Reliability Block Diagram



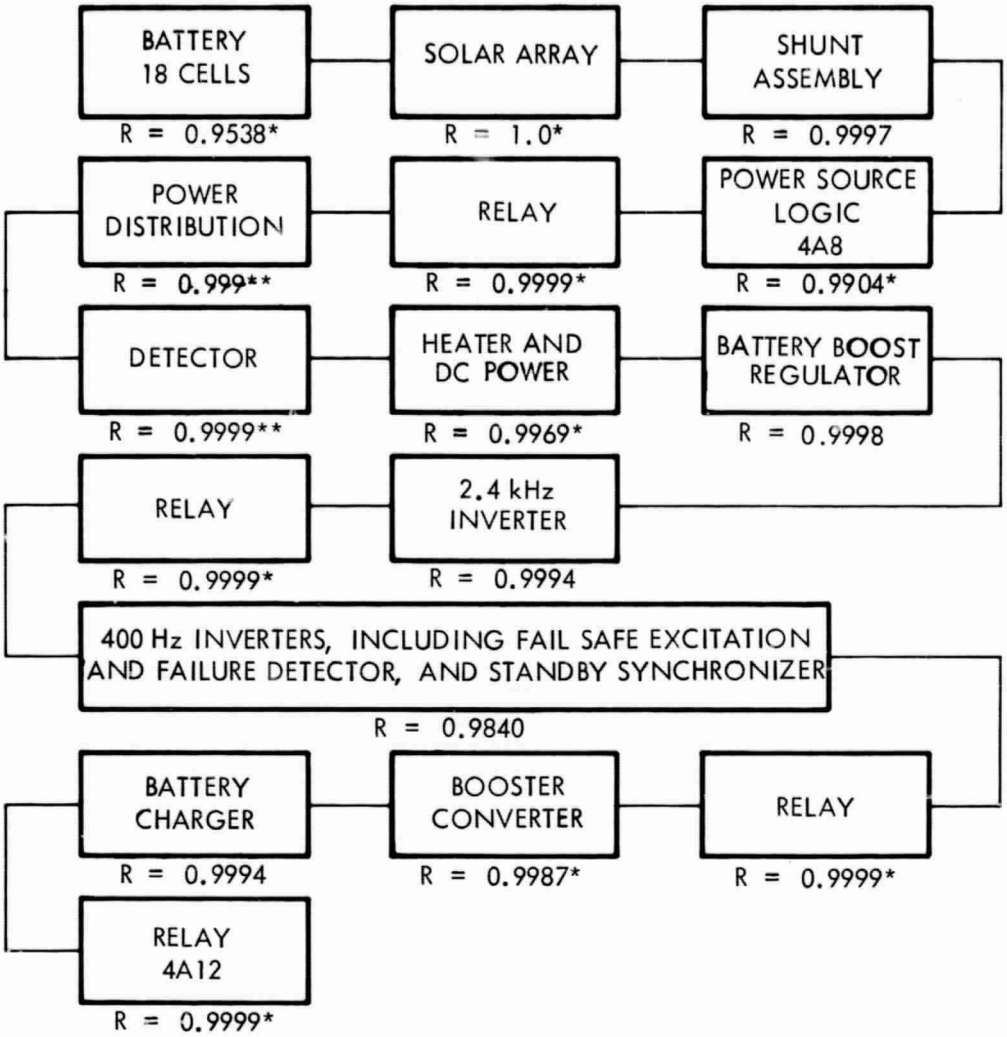
SYSTEM RELIABILITY = 0.9251

NOTES:

1) * RELIABILITIES OF THESE UNITS ARE FROM APPENDIX A

2) **RELIABILITIES OF THESE UNITS ARE FROM REFERENCE 2.

Figure B-22. Regulated Bus System Reliability Block Diagram



SYSTEM RELIABILITY = 0.9345

NOTES:

1) * RELIABILITIES OF THESE UNITS ARE FROM APPENDIX A

2) ** ESTIMATED RELIABILITIES FOR POWER REDUNDANT DISTRIBUTION AND DETECTOR UNITS

Figure B-23. Regulated Bus System Reliability Block Diagram

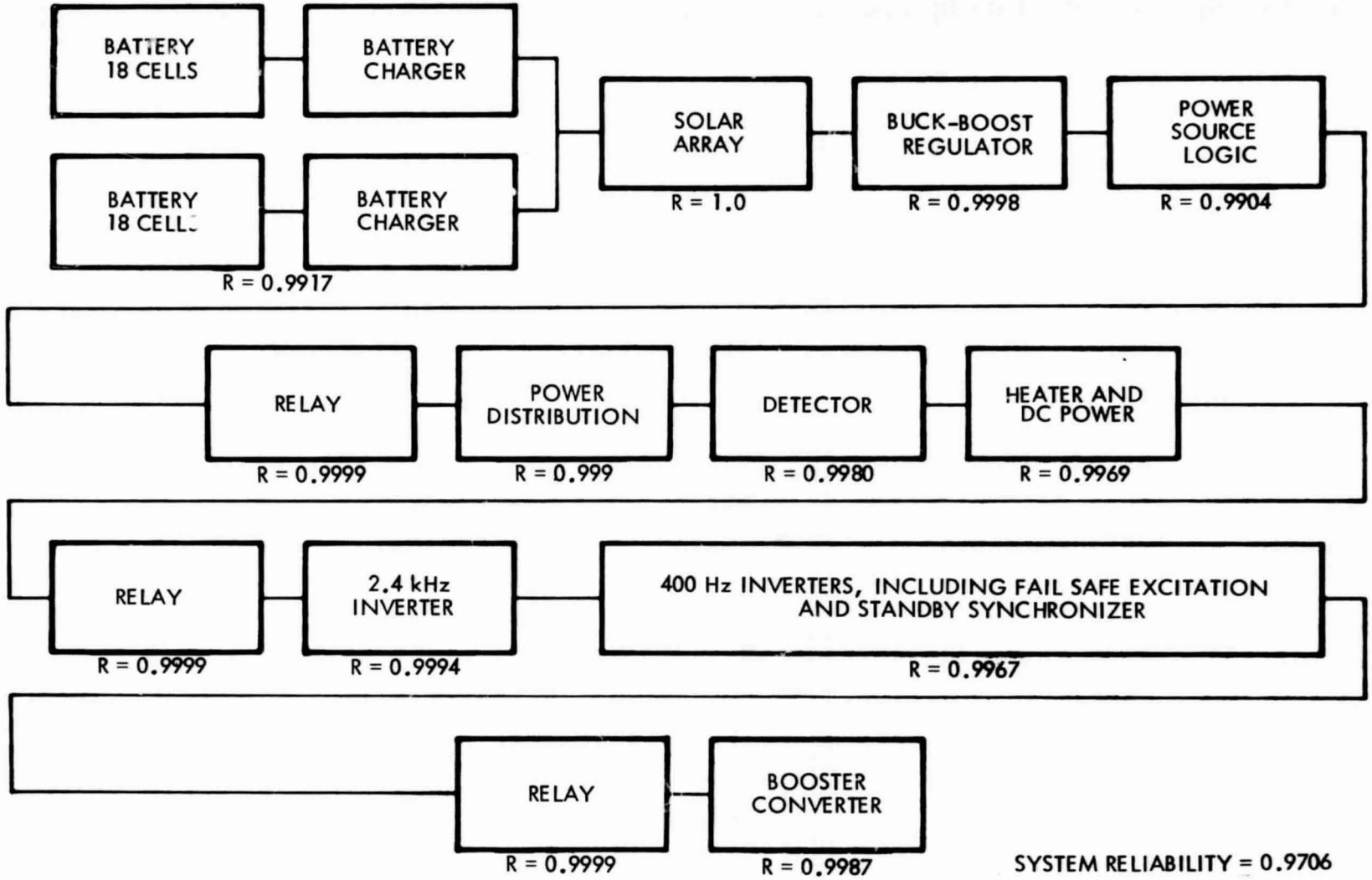


Figure B-24. Recommended System Reliability Block Diagram

APPENDIX C

RELIABILITY ASSESSMENT OF BUCK-BOOST REGULATOR AND BATTERY REDUNDANCY SCHEMES

APPENDIX C

RELIABILITY ASSESSMENT OF BUCK-BOOST REGULATOR AND BATTERY REDUNDANCY SCHEMES

1. INTRODUCTION

Presented herein are the results of the reliability assessment of the buck-boost regulator and battery redundancy schemes considering the configurations shown in Figures C-1 through C-4.

2. RELIABILITY ANALYSIS GROUND RULES AND ASSUMPTIONS

a. The reliability assessments were performed for the orbit phase considering a 1-yr (8760-hr) mission time.

b. The battery charger failure rate is 68 failures/10^9 hr and assumes the unit operates only 10% of the mission time per your instruction. R = 0.9994.

c. Battery A is assumed to have 18 cells with a cell failure rate of 300 failures/10^9 hr. Battery A failure rate = 5400 failures/10^9 hr and reliability R_A = 0.9538.

d. Battery B is assumed to have 18 cells with a cell failure rate of 600 failures/10^9 hr. Battery B failure rate = 10,800 failures/10^9 hr and R_A = 0.9097.

e. The failure rates for the component parts used in this analysis are from Appendix A.

f. The equations used in calculating the reliability of the different redundancy configurations are shown in Appendix A.

g. Whenever possible, all reliability calculations were performed using the REAMX computer program.

h. The results of the analysis are shown in Figures C-1 through C-5 and Tables C-1 through C-3.

Table C-1. Reliability Assessment for One Majority Voting Gate

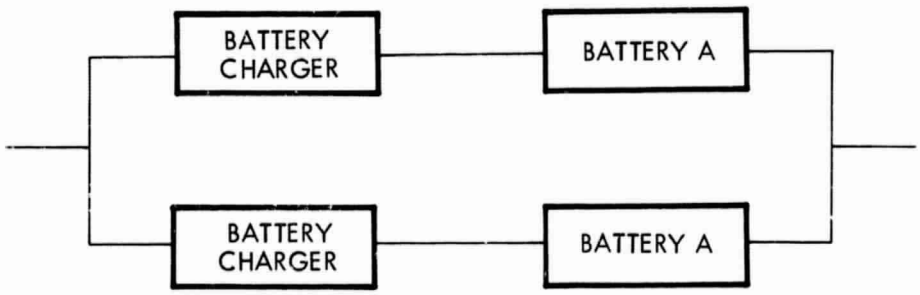
Part Type	n	nλ
Transistor (< 1 W)	2	20.0
Diode (< 1 W)	1	1.3
Resistor, metal film	5	7.0
Total		28.3

Table C-2. Reliability Assessment for One Differential Amplifier

Part Type	n	nλ
Transistor (< 1 W)	2	20.0
Zener	1	60.0
Resistor, metal film	9	12.6
Total		92.6

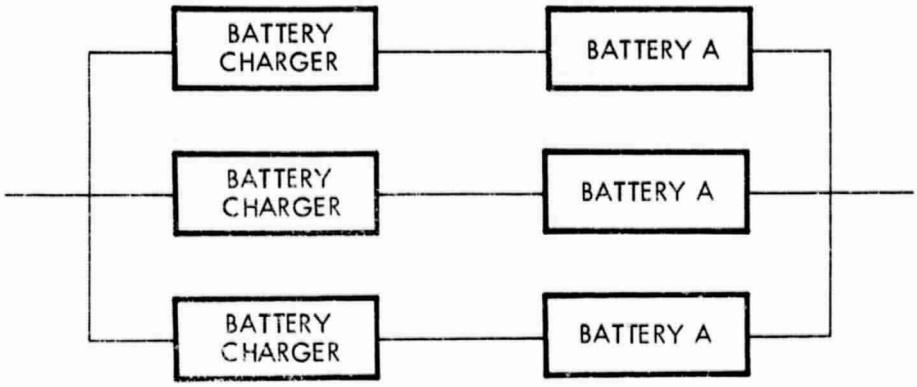
Table C-3. Reliability Assessment for One Power Module

Part Type	n	nλ
Transistor (< 1 W)	1	10.0
(> 1 W)	2	112.0
Diode (< 1 W)	7	9.1
(> 1 W)	2	28.0
Zener	1	60.0
Capacitor, solid tantalum	4	56.0
Resistor, metal film	5	7.0
Transformer	3	45.0
Inductor	2	30.0
Total		357.1



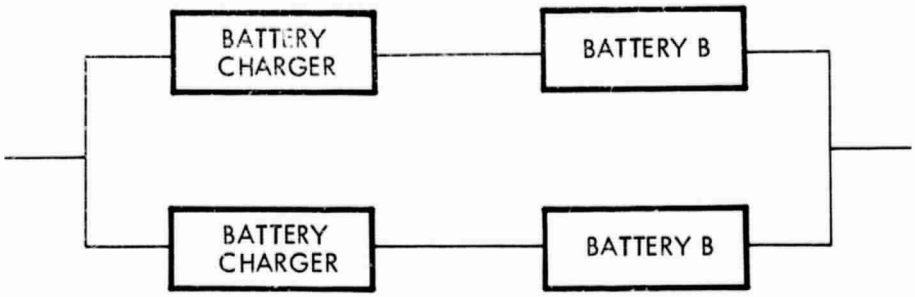
$R_1 = 0.9978$ (WITH ONE OF TWO BATTERY CHARGERS AND BATTERIES REQUIRED FOR SUCCESS)

Figure C-1. Case 1 - Battery Redundancy Configuration No. 1



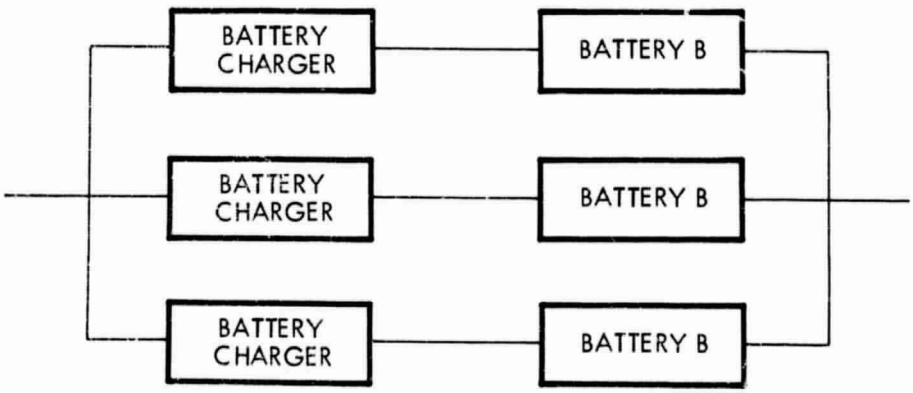
$R_2 = 0.9936$ (WITH TWO OF THREE BATTERY CHARGERS AND BATTERIES REQUIRED FOR SUCCESS)

Figure C-2. Case 2 – Battery Redundancy Configuration No. 2



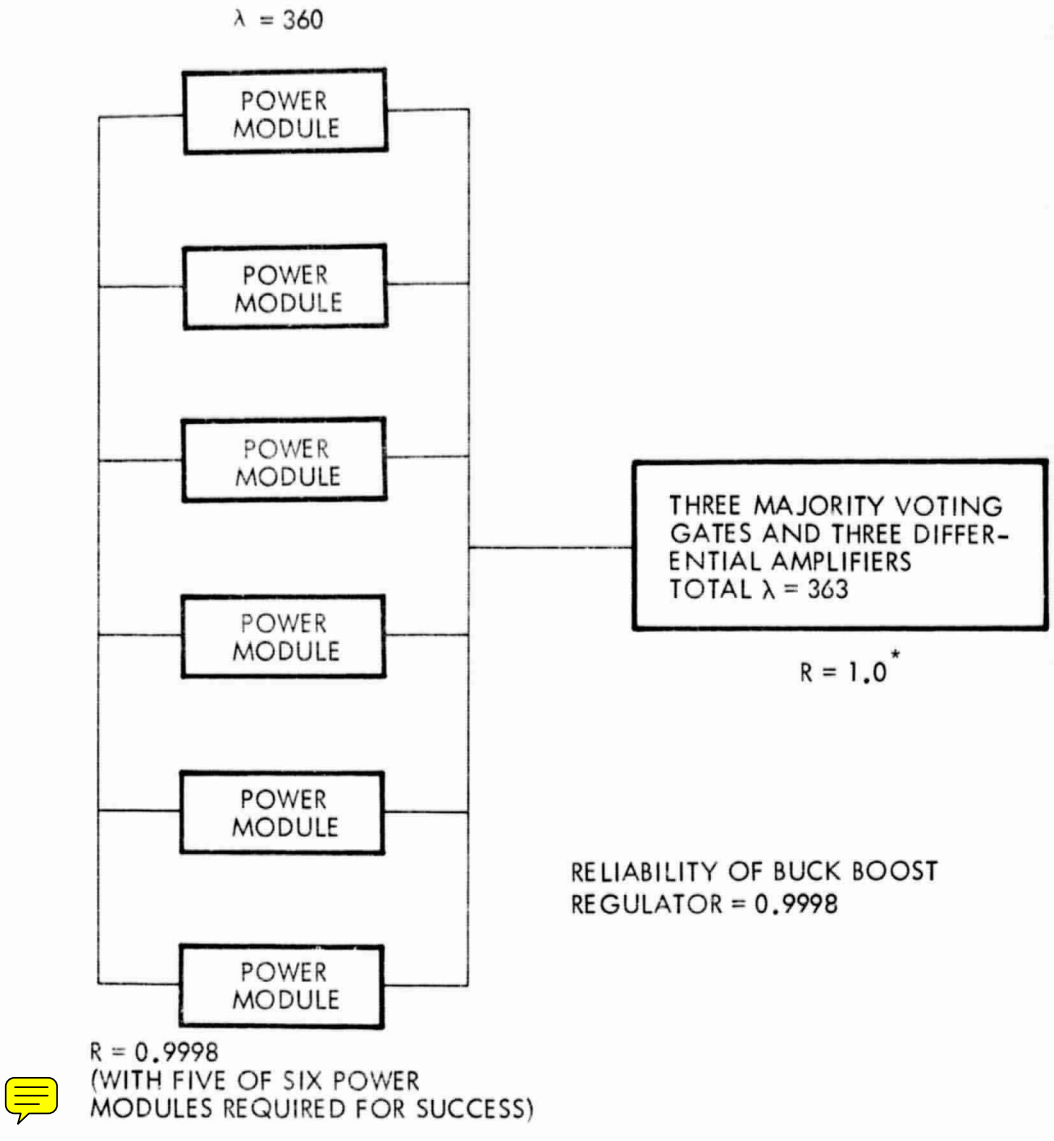
$R_3 = 0.9917$ (WITH ONE OF TWO BATTERY CHARGERS AND BATTERIES REQUIRED FOR SUCCESS)

Figure C-3. Case 3 – Battery Redundancy Configuration No. 3



$R_4 = 0.9767$ (WITH TWO OF THREE BATTERY CHARGERS AND BATTERIES REQUIRED FOR SUCCESS)

Figure C-4. Case 4 – Battery Redundancy Configuration No. 4



NOTES:

1) *THE COMPUTED RELIABILITY OF THIS CIRCUIT CONFIGURATION USING EQUATION (4) OF APPENDIX A IS 0.999995 AND IS ASSUMED = 1.0.
2) THE RELIABILITY OF THE QUADED CAPACITORS AND PARALLEL FUSES WAS NOT CALCULATED AND IS ASSUMED = 1.0.

Figure C-5. Buck-Boost Regulator