Semiannual Report V

March 1968 - August 1968

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Solid State Electronics Laboratory

Engineering Design Center

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I. Abstract

The purpose of this project is to develop a system design and fabrication technique for multi-channel, physiologically implantable, telemetering systems for biological measurements. The design is to be flexible, allowing several channels of information to be handled simultaneously and to be able to telemeter a wide range of physiological signals. This report covers the period from March 1968 to August 1968.

The four-channel discrete component strain-gage transmitter has been functioning satisfactorily since it was implanted in January. Several 24 hour continuous records have been made using this system.

A four-channel integrated circuit strain gage transmitter was constructed and tested. This unit is currently at the NASA Electronic Research Center in Cambridge, Massachusetts.

Improved sample and hold circuitry for the receiver-demodulator system was breadboarded and incorporated into the system. This circuitry uses General Instrument MOS logic circuits for the ring oscillator and for the sampling and holding operations.

A study was started into possible improvements of the transmitter ring oscillator. The current ring oscillator exhibits a slight dependance for proper operation on the storage and delay characteristics of the output transistor which drives the "and" gate and the

associated strain gage amplifier.

Preliminary design and construction of transmitter and receiver-demodulator circuitry to allow subcommutation of one information channel into several lower frequency information channels was completed. This circuitry would allow as many as 10 strain gage information channels to be subcommutated from one channel. The other channels can be used for the higher frequency EKG or EEG signals.

II. Background

A complete explanation of the requirements and guidelines that were used for the design of this system will be found in previous semiannual reports.

During the period of this report, a four-channel integrated circuit strain gage transmitter was assembled from the components which have been under development for this contract. Initial testing and evaluation of the construction techniques and circuitry performance indicated them to be satisfactory.

The four-channel micro-miniature standard component transmitter has continued to function properly following the implant during the last reporting period.

III. Four-Channel, Integrated Circuit Transmitter

The description of the flat pack circuits which were used

in the construction of the four-channel integrated circuit transmitter is given in previous semiannual reports.

A modification of the first ring oscillator stage was found to be necessary to limit the amount of current drawn through the reset transistor when a reset pulse sets this stage to a "1" level. The modified circuit is shown in Figure 1.

It was also found that a 0.1 microfarad capacitor instead of a 0.01 microfarad capacitor improved the reliability of the electronic latching switch. This change was also incorporated into the construction of this transmitter.

The printed circuit board for the four-channel integrated circuit transmitter is 1 1/4" by 1 1/8". The finished unit is 1 1/4" by 1 1/8" by 5/8".

Figure 2 is a partially completed transmitter assembly to show the type of construction used in the transmitter.
There are 16 flat packs mounted on this board for the four-channel strain gage transmitter. The flat pack leads and connecting wires on the board are insulated with Teflon tubing. Assembly of the transmitter was done with the use of a binocular microscope and specially adapted tools for cutting and soldering the leads.

The assembly of the transmitter was completed on August 22, 1968, and this unit was sent to NASA Electronic Research Center

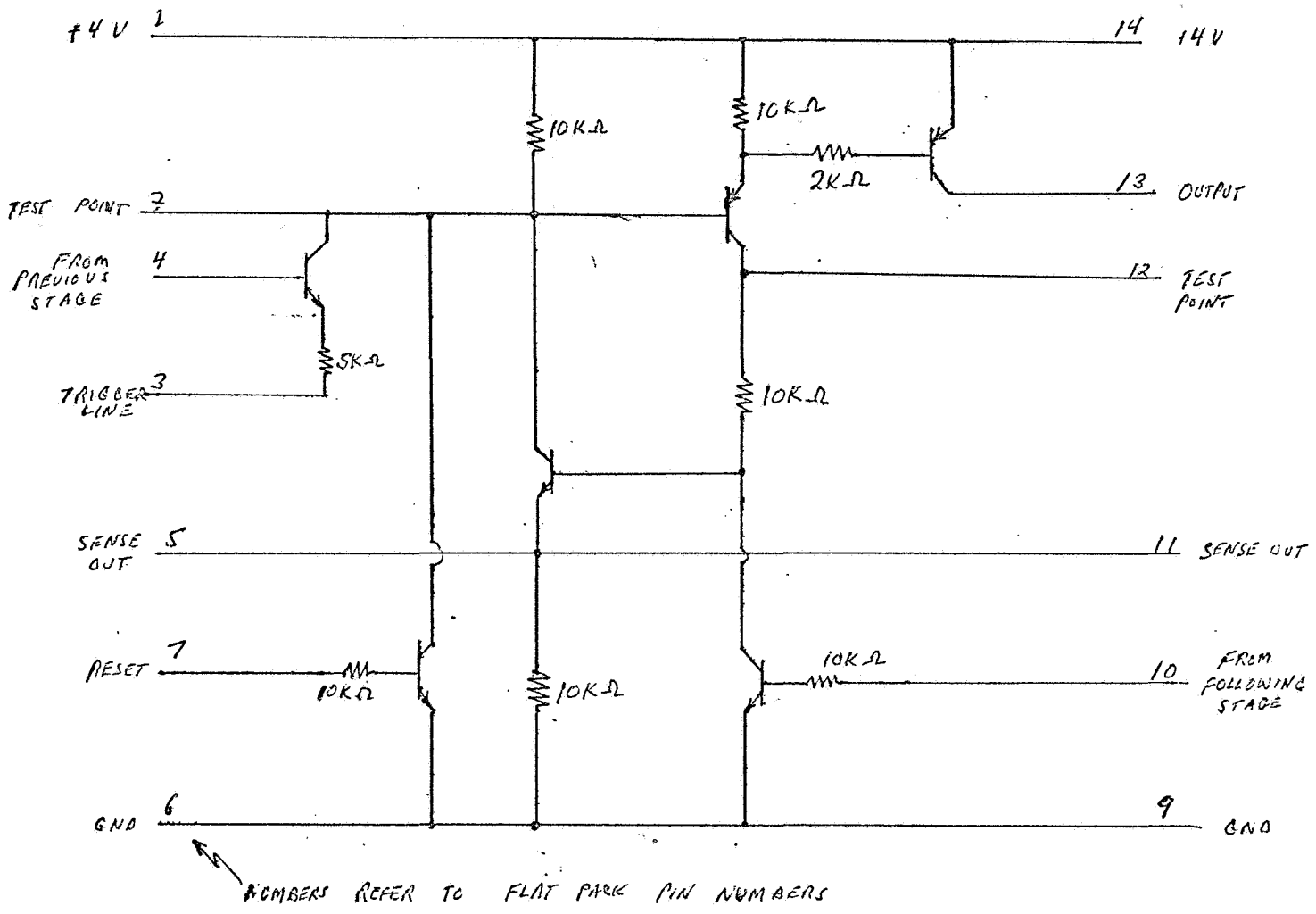

FIGURE 1

FIRST RING OSCILLATOR STAGE

FLAT PACK 202.2

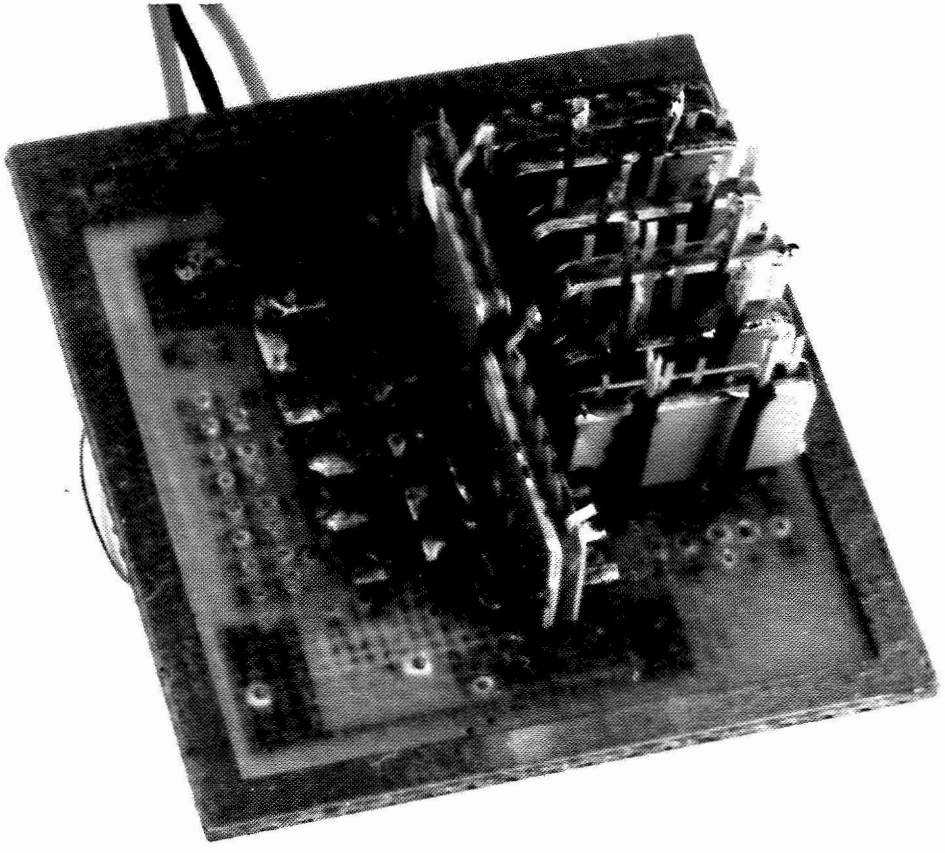

FIGURE 2

Detail of construction of four-channel I.C. transmitter

in Cambridge, Massachusetts for evaluation. Because of an unexpected failure of some strain gages only 2 gages were available to be attached to this unit. The other 2 strain gage channels were tied internally to an intermediate level between the sync and agc levels. The transmitter was not encapsulated since the addition of the other 2 strain gages will require additional connections on the printed circuit board.

IV. Improved Demodulation Circuitry

A block diagram of the multiplex receiver modification is shown in Figure 3. The clock frequency is adjustable, and in operation it is adjusted to the clock frequency in the transmitter. The clock synchronization allows for minor frequency variations and assures a proper phase relationship between the two clocks. Thus, the receiver clock puts out a pulse each time a different channel appears on the incoming signal.

A General Instrument MOS Integrated Circuit, MEM 3012 SP 12-BIT serial in-parallel out shift register, is used to select the proper sample and hold circuit to sample the incoming channel. At the beginning of a cycle of channels coming in (as detected by the sync level detector) a data pulse is fed to the MEM 3012 SP. As each clock pulse comes along, the data pulse is shifted from one output to the next. The pulse appears first in the first output then,

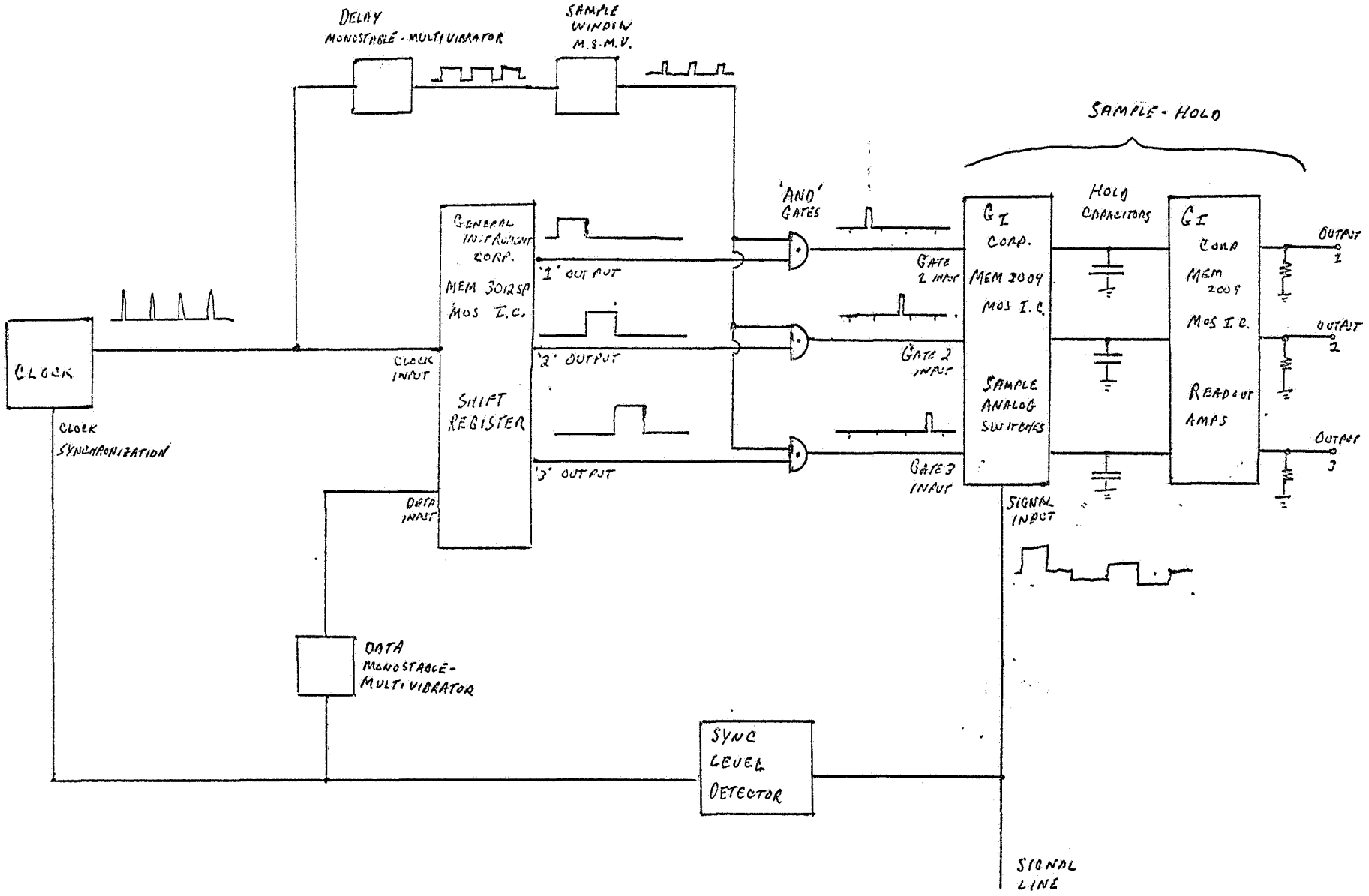

FIGURE 3

BLOCK DIAGRAM

when a clock pulse arrives in the second output and so forth.

Each output of the shift register is fed to an "and" gate. A second input of the "and" gate is connected to a sample window pulse generator. This generator produces a pulse of controlled width in each period between clock pulses. The controlled width pulse is delayed a constant amount from the beginning of the period. The sample window pulse is delayed to allow any switching transients to die down before sampling occurs. The sample window pulse widths may be as short as 1 microsecond.

The output of each "and" gate is fed to the gate of the corresponding sample switch. General Instrument MEM 2009 MOS I.C. multiplex switches are used for the sample switches. The MEM 2009 consists of 6 MOS FET switches. The source connections of all FET's are tied together. The signal line is brought in on this connection. As each gate is turned on, the FET becomes a low resistance and connects the signal line (source) to the hold capacitor (drain). The signal in the line at that time is stored in the hold capacitor. Another MEM 2009 is used to read out the voltage stored on the capacitors. The FET's are used as source-follower (unity gain) amplifiers. The source's of the FET's which are internally tied together are held at -6 volts, the drains are individually fed through load resistors to + 12 volts. The gates are connected to the 'hold' cap-

acitors (Note: The drain and source are reversed from usual source follower connections, but because of the symmetry of an FET, this does not matter). The high input impedance of the MOS FET insures that little charge will leak off the 'hold' capacitor.

Each MEM 2009 flat pack contains six MOS FET's. At least two flat packs must be used together. A total of four flat packs will provide for up to twelve channels of information. The MEM 3012 SP shift register also provides for twelve bits of information. Thus any number of channels up to twelve may be demodulated.

Clock Circuit Description

The clock consists of a simple unijunction transistor relaxation oscillator with a pulse shaper and a synchronization circuit. The pulse shaper is required to obtain adequate pulses for operating the shift register. The synchronization circuit differentiates the sync level pulse, providing a sharp spike. This spike turns on a pnp transistor which shorts the charging resistor and fires the UJT.

The frequency of the clock may be varied by adjusting the 50 K potentiometer. The clock frequency may be varied over an even wider range by changing the timing capacitor. The period must be adjusted such that the synchronization pulse does not cause two clock pulses to appear very close together.

Delay and Sample Window Generation Circuitry

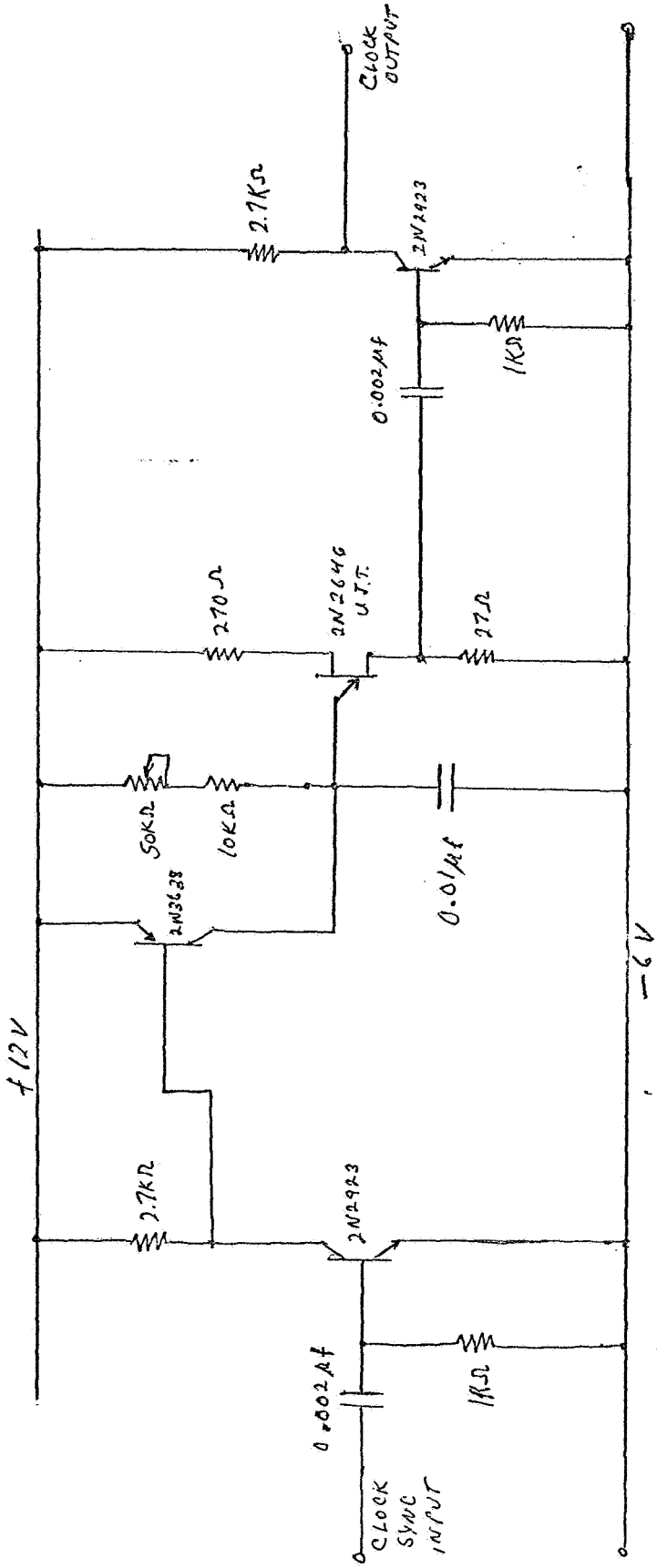

FIGURE 4

REVISED CLOCK CIRCUIT

The delay is generated by an adjustable monostable multivibrator. The delay monostable triggers another adjustable monostable which provides a delayed sample window pulse. The delay is generally set to be one-half of a clock period. The sample window pulse may be as short as 1 microsecond and still allow the sample and hold circuit adequate acquisition time.

Sync Level Detector Circuitry

The sync level detector is the same as used on the original receiver.

Data Monostable Multivibrator

An ordinary adjustable monostable multivibrator is used to provide a data pulse as an input to the shift register when triggered by the sync level detector. The monostable multivibrator must be adjusted to provide a pulse for longer than one clock period, but shorter than two periods.

Shift Register

The shift register is a General Instrument MEM 3012 SP MOS I. C.

"And" Gates Circuitry

. The "and" gates are simple TTL gates. The first pnp transistor from the shift register output provides isolation for and inversion of that output. Speed up capacitors are used to provide fast rise

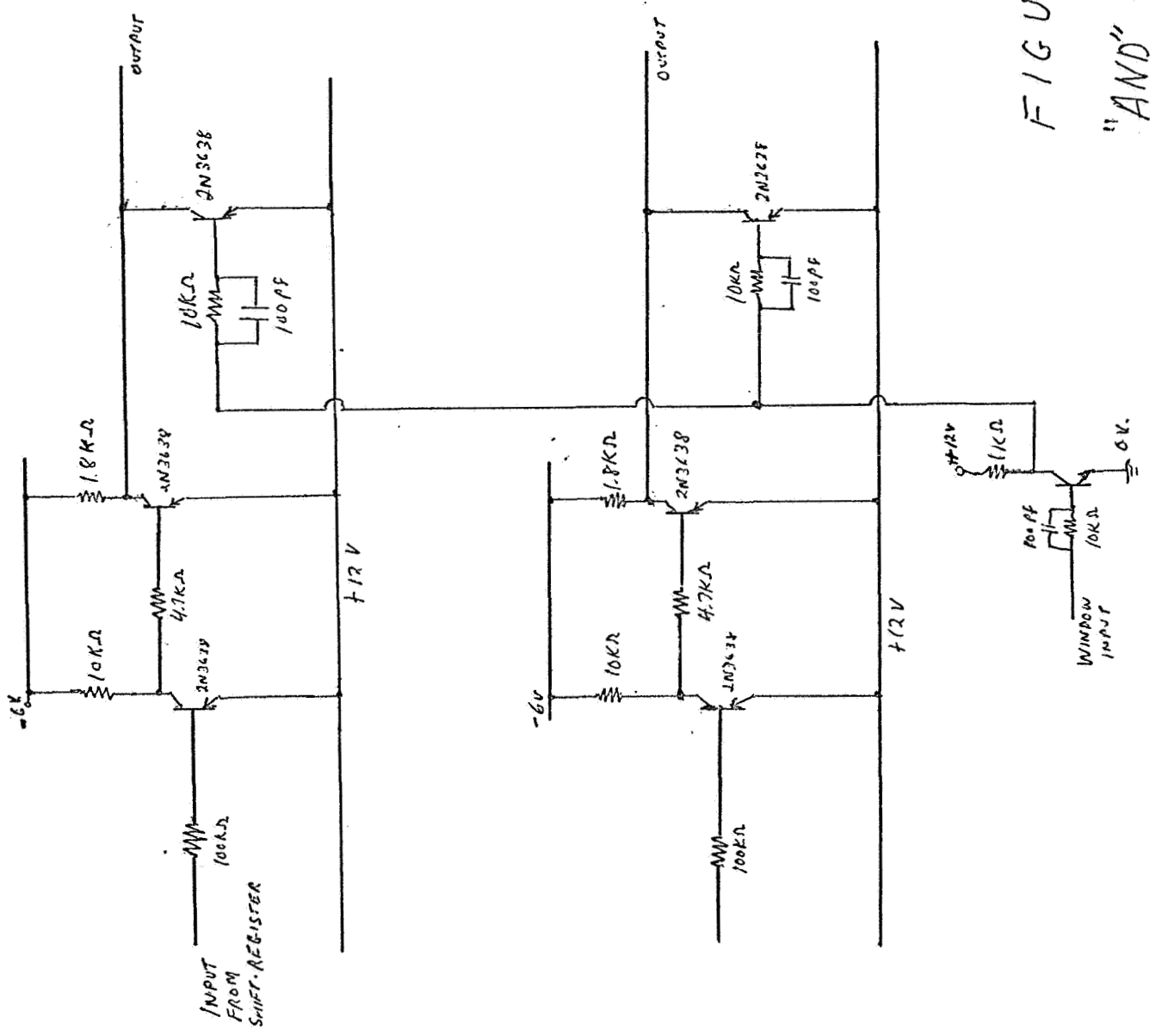

FIGURE 5.

"AND" GATES

times for microsecond sample window pulses.

Sample Hold Circuit

The sample and hold circuit as shown in Figure 6 makes use of two MOS FET's, contained in separate MEM 2009 MOS I. C.'s. The first FET acts as an analog switch connecting the signal line to the hold capacitor upon command from the "and" gates. The hold capacitor stores the signal until it is updated. The second FET acts as unity gain amplifier. It's high input impedance (10^{10} ohms) allows the hold capacitor to maintain its voltage level until the next sample window for that channel. The amplifier FET is operated as source follower (with source and drain levels inverted).

V. Transmitter Ring Oscillator Improvements

It was found that the timing of the ring oscillator driver is directly connected to the overlap time between ring oscillator stages. This overlap time is detected in the "and" circuit which is fed back to the ring oscillator driver to reset the timing circuit. Although the overlap times only vary from one to six microseconds out of a frame width of almost 200 microseconds, this causes the frames to vary from one another by as much as 10%. This large variation is caused by incomplete reset of the timing circuit in the ring oscillator driver when the overlap time is less than five microseconds. Scope traces showing this variation are shown in Figures 7 and 8.

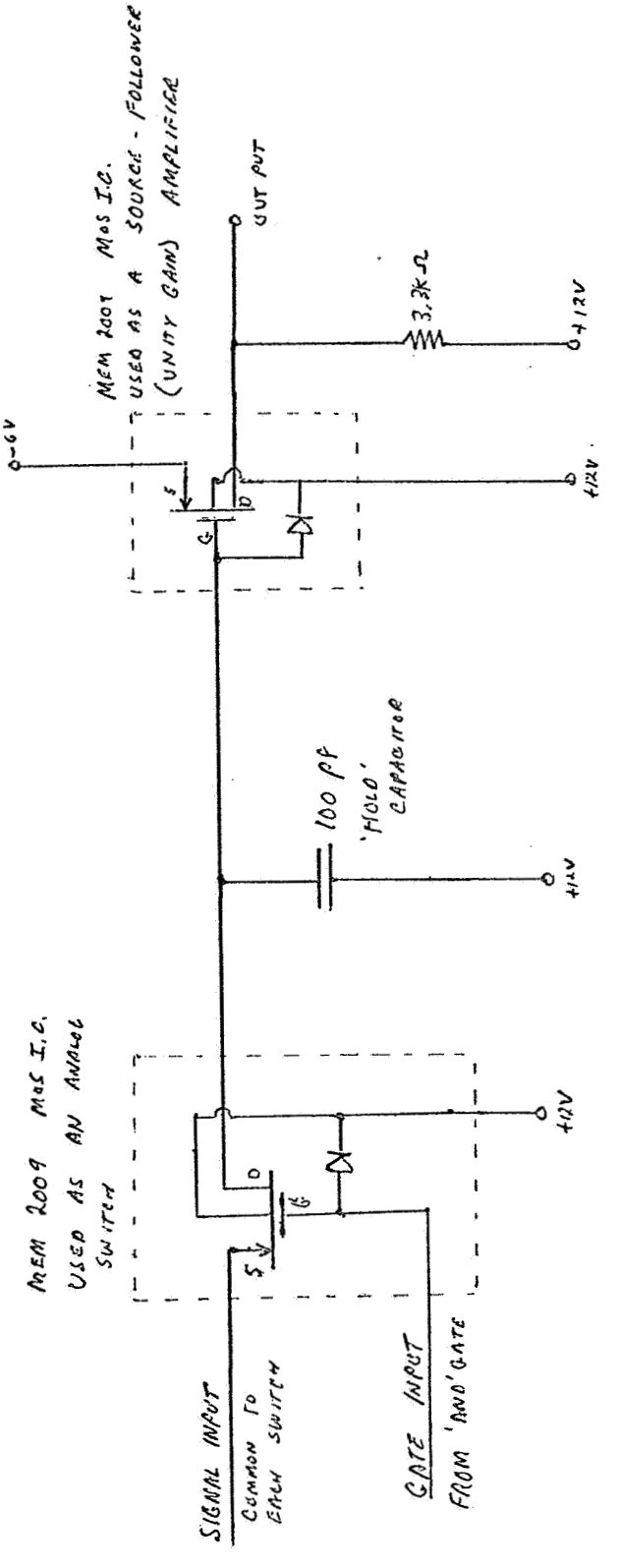

FIGURE 6

A SINGLE SAMPLE-HOLD CIRCUIT.

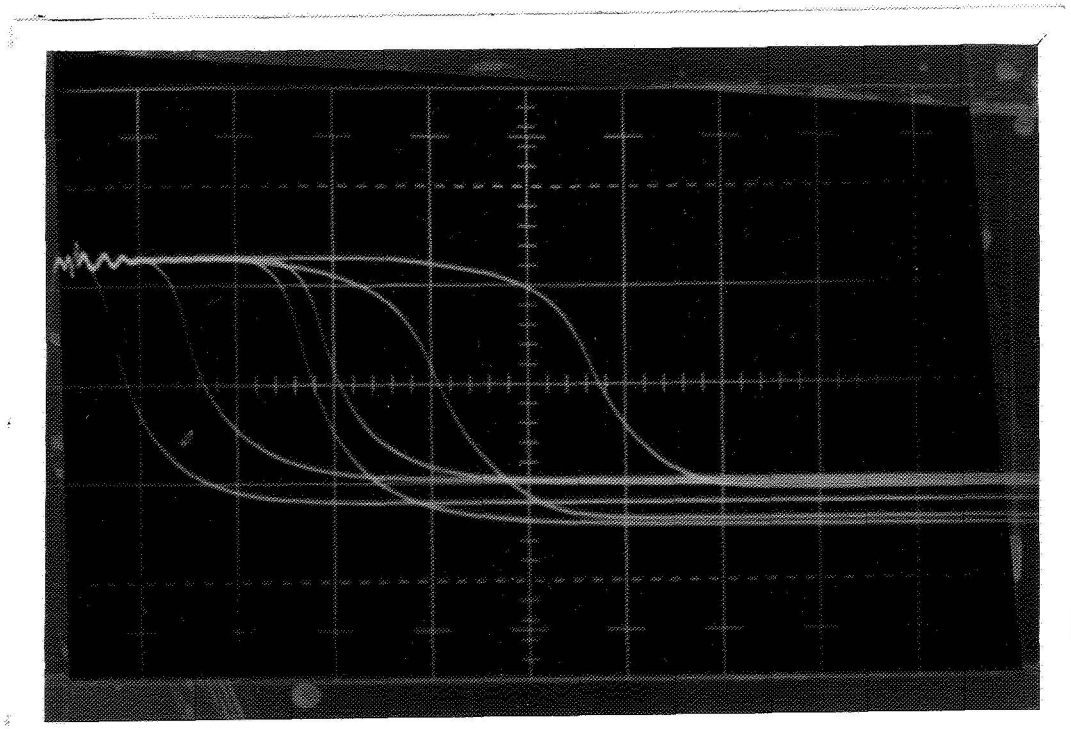

FIGURE 7

Variation of overlap time as seen at the output of the transmitter "and" circuit. 1μ/cm

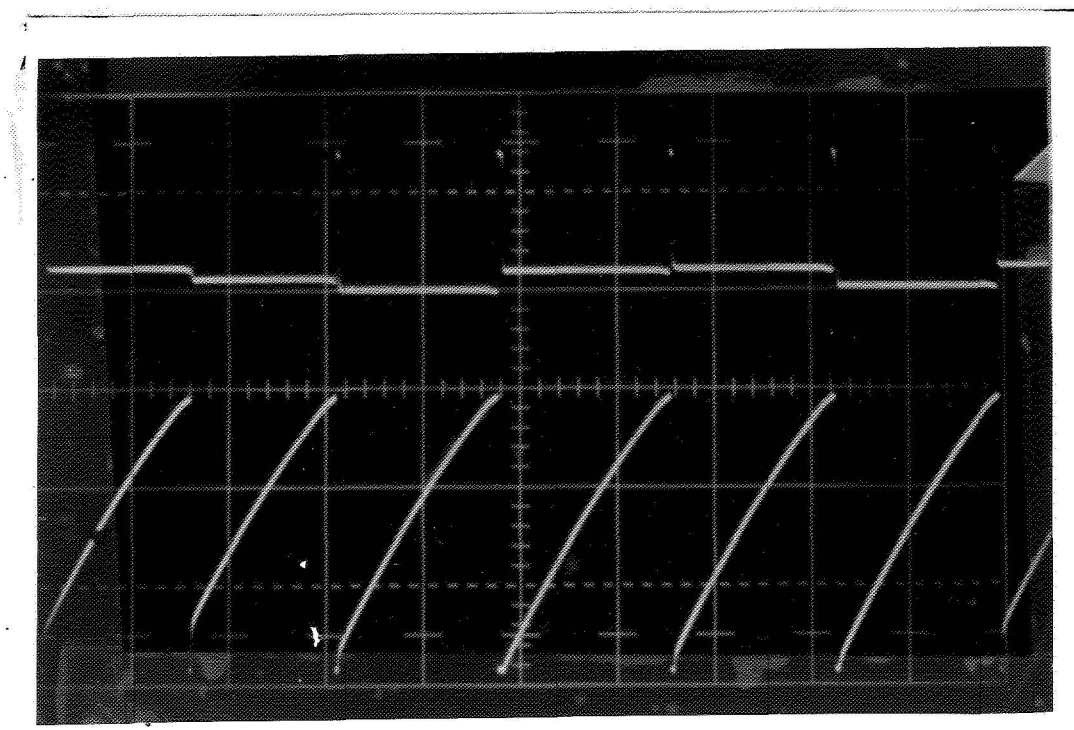

FIGURE 8

Variation of frame period caused by imcomplete reset of Ring Oscillator Driver timing circuit. 100μs/cm

It was found that the variation of overlap time was caused by variations in storage and fall time in the transistor which is used to drive the strain gage amplifiers.

Investigations are currently underway to find ways of improving the reset capabilities of the ring oscillator driver and to minimize the effect of device parameters on the ring oscillator operation.

VI. Subcommutation of Information Channels

Figure 9 shows the circuitry necessary to modify one of the existing strain gage amplifiers for use in a subcommutating system. The actual power for operation is obtained from the lower speed driven ring oscillator stage. The output of the primary ring oscillator stage which is to be subcommutated is used to key the other input so that power is applied only during the frame when it is required. A large resistor is in series with the keying signal to keep this keying signal from applying sufficient power to operate the subcommutated amplifiers. This series resistor also helps prevent loading of the output of that ring oscillator stage.

Figure 10 shows the circuitry used for the ring oscillator driver for the subcommutating ring oscillator. This circuit just differentiates and inverts the output of one of the main ring oscillator stages. This spike is then applied to the shift line of the subcommutating ring oscillator stages, and they operate similarly

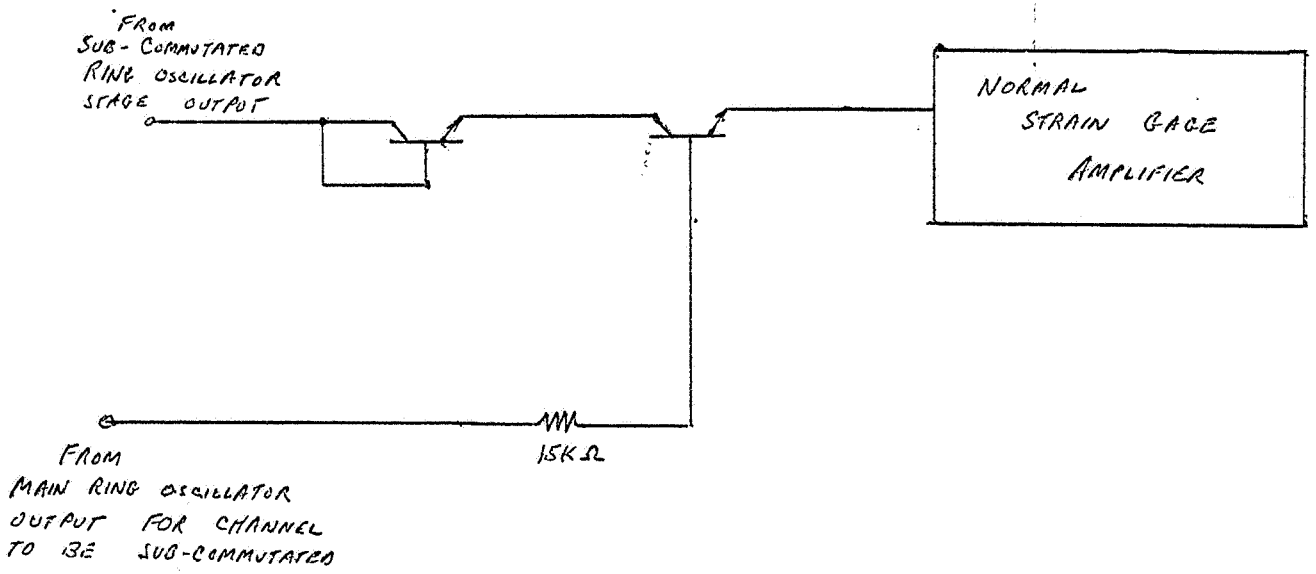

FIGURE 9

MODIFICATION OF PRESENT STRAIN GAGE AMPLIFIER FOR SUB-COMMUTATION

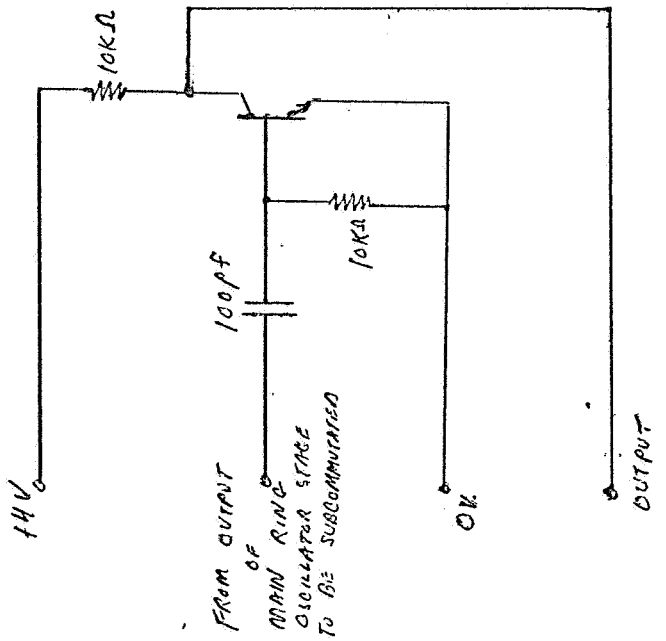

FIGURE 10
SUB COMMUTATING
RING OSCILLATOR
DRIVER

to the main ring oscillator.

The receiver demodulator circuitry for this subcommutating system is basically the same as that for the main system except that no agc function is necessary. A sync level somewhat lower than the main system sync level is used to determine the starting point for the subcommutating receiver ring oscillator. A block diagram of the subcommutating demodulation system is shown in Figure 11.

VII. Eight-Channel System

The eight-channel transmitter system test set up is currently being modified for subcommutation operation as described in the preceding section. It is hoped that subsequent testing of this system will allow the eight channel system to consist of 3 high frequency information channels, one of which is subcommutated into 6 lower frequency information channels. Since most of the transmitter circuitry will remain unchanged for this type of transmitter system, it is felt that a modification of this sort at this time will not slow the progress of the current project.

Work is progressing toward the completion of an eight-channel implantable transmitter. This unit should be completed by the end of the next reporting period.

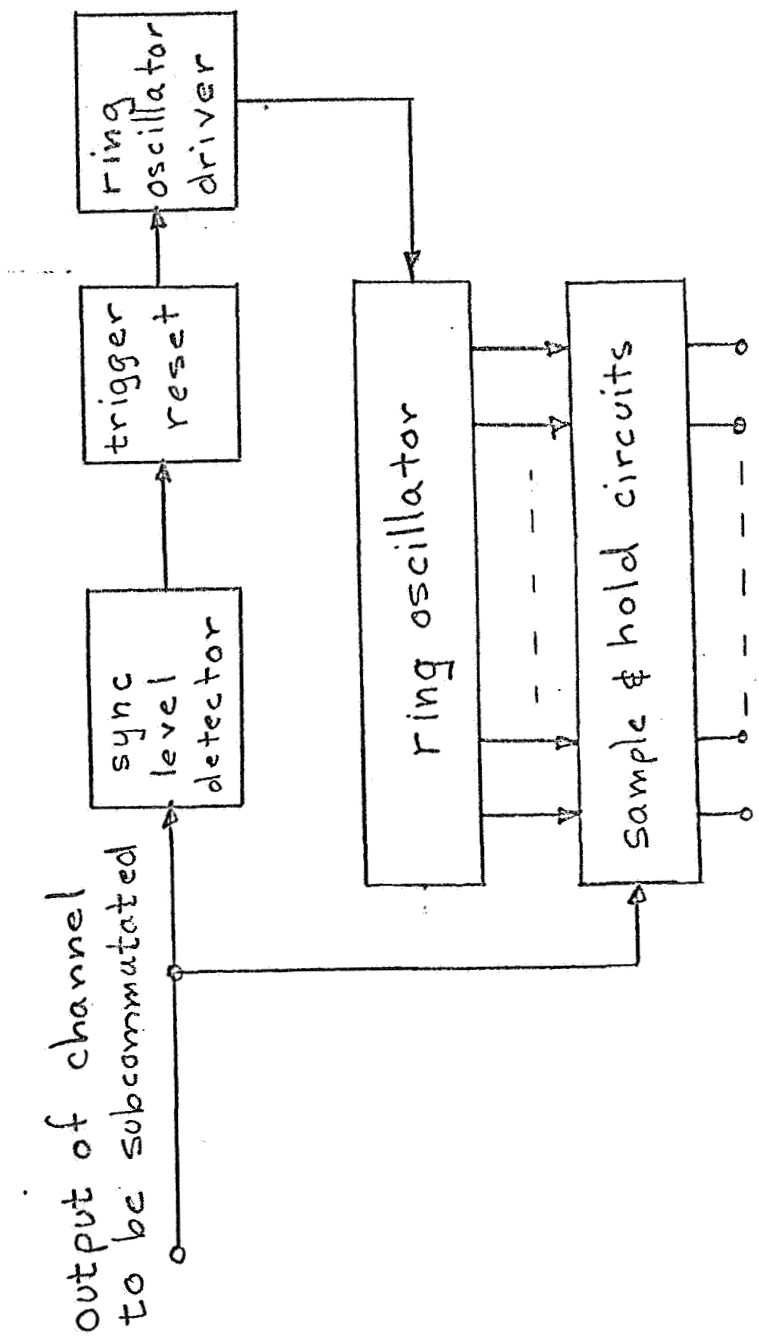

FIGURE 11

BLOCK DIAGRAM OF SUBCOMMUTATING DEMODULATOR