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Report No. 03-68-78

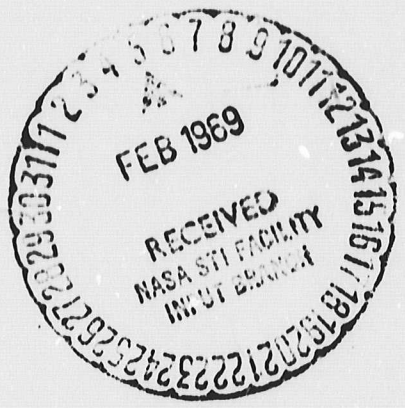
Final Report

for

PHOTON-COUPLED ISOLATION SWITCH

(1 January 1966 through 31 March 1968)

Contract No. 951340



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JET PROPULSION LABORATORY
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This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, sponsored by the National Aeronautics and Space Administration under Contract NAS7-100.

THIS WORK WAS PERFORMED FOR THE JET PROPULSION LABORATORY, CALIFORNIA INSTITUTE OF TECHNOLOGY, SPONSORED BY THE NATIONAL AERONAUTICS AND SPACE ADMINISTRATION UNDER CONTRACT NAS7-100.

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FOREWORD

This report was prepared by the Components Group of Texas Instruments Incorporated, Dallas, Texas, under Jet Propulsion Laboratory Contract No. 951340.

Directing the program at JPL were Raymond Piereson, group supervisor, and Daniel Bergens, cognizant engineer.

The work was performed at Texas Instruments under the direction of Dr. J. R. Biard of the Optoelectronics Department. Chief contributors and their areas of responsibility were E. L. Bonin, project engineer and device development; E. E. Harp, device development; and J. C. Lewis and W. A. Little, Si diffusion.

ABSTRACT

Optoelectronic techniques were used to develop a new type of photon-coupled integrated circuit. This device, called the photon-coupled isolation switch, uses internal photon generation and detection to provide electrical isolation between the driving sources and all other terminals of the switch. The isolation switch combines a monolithic silicon (Si) integrated driver circuit, a gallium arsenide (GaAs) photon-emitting diode, and a Si phototransistor in a single integrated-circuit flat package. The driver circuit delivers bias to the photon-emitting diode and, with DTL circuitry, provides for up to 10 inputs. The emitting diode is optically coupled to the electrically isolated phototransistor which provides the output-switch terminals.

The input-signal requirements for the driver circuit are designed to complement the outputs of conventional digital integrated circuits, with an input of one volt or less ensuring non-conduction between the output terminals and an input of three to six volts producing conduction. The output terminals conduct up to 10 mA with less than 0.6 V drop. Isolation between the output and other terminals is at least 50 V with a capacitive coupling of only three pF typically. Total rise and fall times of the isolation switch are less than 10 and 100 μs respectively. Unlike transformers, the isolation switch can be activated for an indefinite period. The supply requirement is a single 4 ± 0.5 V source, with maximum circuit dissipations of 1 mW and 200 mW in the non-conducting and conducting states respectively. The operating case-temperature range is -20°C to 100°C. The lack of moving parts allows the device to operate in extreme mechanical environments.

As indicated by these characteristics, the solid-state isolation switch is suitable for use in place of mechanical switches, relays, and pulse transformers in advanced-design equipment. The new device can be used to activate power to a number of stages without the introduction of noise due to ground loops in the power circuitry. This development of the isolation switch represents a further step in component miniaturization, as the driving and relay functions are enclosed in a single, small integrated-circuit package.

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SECTION I

INTRODUCTION

Electrical isolation, such as is obtained using a transformer, offers the highly desirable capability to couple signals between circuits operating at different dc potentials and to minimize ground-loop currents produced with direct connections. This four-terminal network operation is not available in most integrated circuits, however, because it cannot be provided effectively with conventional processing techniques. A technique which has successfully provided isolation consists of using photon coupling between a solid-state photon emitter-detector pair.[1,2] The most efficient signal coupling between an optical pair has been obtained using a gallium arsenide (GaAs) PN junction emitting diode with a silicon (Si) PN junction diode, both of which have responses peaking near 0.9 μm at 25°C. The process technologies for these semiconductor materials are also highly advanced. Devices which have been developed[2,3] using photon coupling include an isolated-input transistor, an isolated-gate PNPN-type switch, a multiplex switch requiring no driving transistor, and an isolated-input pulse amplifier.

Under this development program, photon coupling was used in a new type of device consisting of a DTL gate having isolated output terminals. This three-chip isolation switch combines a monolithic Si driver circuit, a GaAs emitting diode, and a Si phototransistor. Inputs (up to 10) are applied to the driver circuit which supplies forward bias to the GaAs diode. The emitting diode is optically coupled to the phototransistor, using a high-refractive-index glass. The output transistor is thereby electrically isolated from the driving sources. This development program was divided into two phases. In Phase I the driver circuit was designed and the emitting diode-phototransistor pair (GaAs switch) was developed. In Phase II the driver circuit was integrated in a monolithic Si wafer, and the complete isolation switch, combining the driver circuit and GaAs switch, was assembled in a miniature integrated circuit flat package.

As described for Phase I in Section II of this report, the basis for the driver circuit design was parameter data measured for another photon-coupled integrated circuit switch, the Texas Instruments type TIXL106, formerly the SNX1304. A number of circuit arrangements were considered for the driver circuit. For the selected circuit a worst-case design was performed to evaluate the available current bias for the emitting diode. A standard type of GaAs emitting diode was employed for the device, namely, the one used in the TIXL106. From the calculated values of diode bias current and known emission-efficiency characteristics, the available photon intensity was derived. This directly indicated the gain required in the phototransistor, and additional calculations were made to select the other parameters. Fabricated phototransistors and GaAs switches satisfied the design goals. Life-test data, as discussed in the section, indicated only small parameter changes in the GaAs switch for almost 12,000 hours of continuous operation. Proton radiation of related devices also indicated that this should have a negligible effect on the isolation switch.

Phase II of the program is described in Section III. The layout and processing steps for the driver circuit and assembly steps for the isolation switch are discussed. Test results showed that the isolation switches met the design specifications.

SECTION II

DESIGN OF ISOLATION SWITCH AND DEVELOPMENT OF GaAs SWITCH

A. ISOLATION-SWITCH DESIGN

1. Functional Description

A black-box representation of the isolation switch is shown in Figure 1. Ten inputs are provided to the driver circuit in the preferred configuration. Application of an input voltage, V_I, above some minimum value to all inputs results in delivery of a significant forward-bias current to the photon-emitting diode. This is denoted the "1" condition. With this bias applied, photons are emitted which are collected by the phototransistor, increasing the conduction between the collector and emitter (output) terminals as would an application of a base current. For some small V_I applied to one or more of the inputs the bias to the emitting diode becomes negligible, and the phototransistor conducts only its leakage current. This low-current mode is considered the "0" condition.

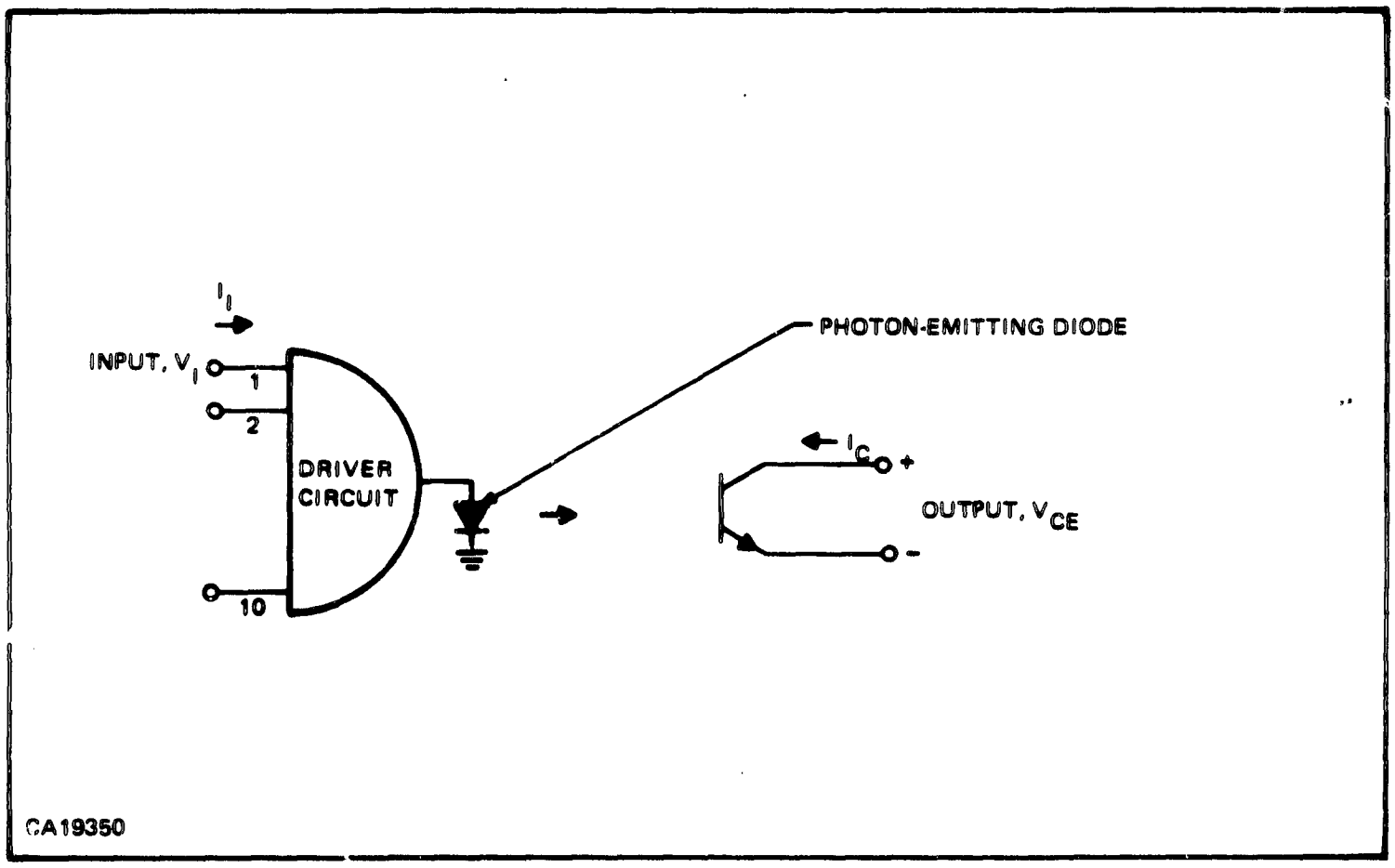


Figure 1. Photon-Coupled Isolation Switch

The current which can be conducted by the transistor is the product of an effective base current and the current gain. As with most diffused transistors, the forward common-emitter current gain is significantly greater than the reverse gain. The transistor is thus substantially a unilateral switch.

2. Specifications and System Considerations

The design-goal specifications for the isolation switch are given in Table I. It can be noted that the input specifications complement the output characteristics of standard RTL-DTL-TTL circuitry. Each of these circuits uses a transistor which saturates to ground in the output; thus they can sink

Table I. Isolation Switch Specifications

Parameter	Symbol	Conditions	Value Min	Value Max	Unit
Input Voltage:					
at "1" level	V_I		3.0	6.0	V
at "0" level	V_I		0	1.0	V
Input Current:					
at "1" level	I_I	V_I = 6 V		50	μA
at "0" level	I_I	V_I = 0.1 V		-1.0	mA
Output Saturation (ON) Voltage	V_{CES}	V_I = 3 V, I_C = 10 mA		0.6	V
Output (ON) Current	I_C	V_I = 3 V, V_{CES} = 0.6 V	10		mA
Output Leakage (OFF) Current	I_{CEO}	V_I = 1 V, V_{CE} = 20 V			
		Temp. = +25°C		0.1	μA
		Temp. = +100°C		20	μA
Output Breakdown Voltage	BV_{CEO}	V_I = 0 V, I_C = 100 μA	35		V
Isolation Capacitance (between output and all other terminals)	C_{ISO}	freq = 1.0 kHz		10	pF
Switching Times:					
Turn ON	t_1	(See Figure 2)		10	μs
Turn OFF	t_2	(See Figure 2)		100	μs
Noise Transmissibility	V_n	(See Figure 3)		2.0	V
Power Dissipation:					
Switch ON	P_{ON}	V_I = 3 V, I_C = 0		200	mW
Switch OFF	P_{OFF}	V_I = 0 V, I_C = 0		1.0	mW

currents for the low-input "0" conditions of the isolation switch. From Table I the "0" input level is specified as 0 to 1 V, for which the prior stages supplying "0" inputs must sink a total of up to 1 mA. The "1" input level of 3 to 6 V requires less than 50 μA from the prior stages. The output saturation voltage of the phototransistor is a maximum of 0.6 V while conducting up to 10 mA. With this output-switch characteristic the device could be used to activate power to a number of circuits. The phototransistor leakage current is a maximum of 20 μA at 20 V, with a breakdown voltage of 35 V or greater. Capacitive coupling between the output leads and all other terminals of the switch must not exceed 10 pF. In addition, it is intended that the device be designed to withstand isolation voltages of up to 50 V. The switching times are specified as a maximum turn-on time of 10 μs and turn-off time of 100 μs, measured with the circuit in Figure 2. A parameter which measures the effectiveness of the phototransistor in the "0" (off) state in isolating noise signals from the output circuitry is called the noise transmissibility, measured with the circuit in Figure 3. The isolation circuit operates with a power-supply potential of 4 ± 0.5 V and over the case-temperature range of -20°C to +100°C. Power dissipation must not exceed 200 mW in the "1" state and 1 mW in the "0" state.

3. Design Considerations

Some preliminary design observations can be made from the specifications. The multi-diode gates used in the inputs of DTL circuits or multi-transistor gates of TTL, might satisfy the input specifications of the isolation switch. The generally greater leakage current of the transistor gates, due to inverse current gain, could preclude the use of this arrangement.

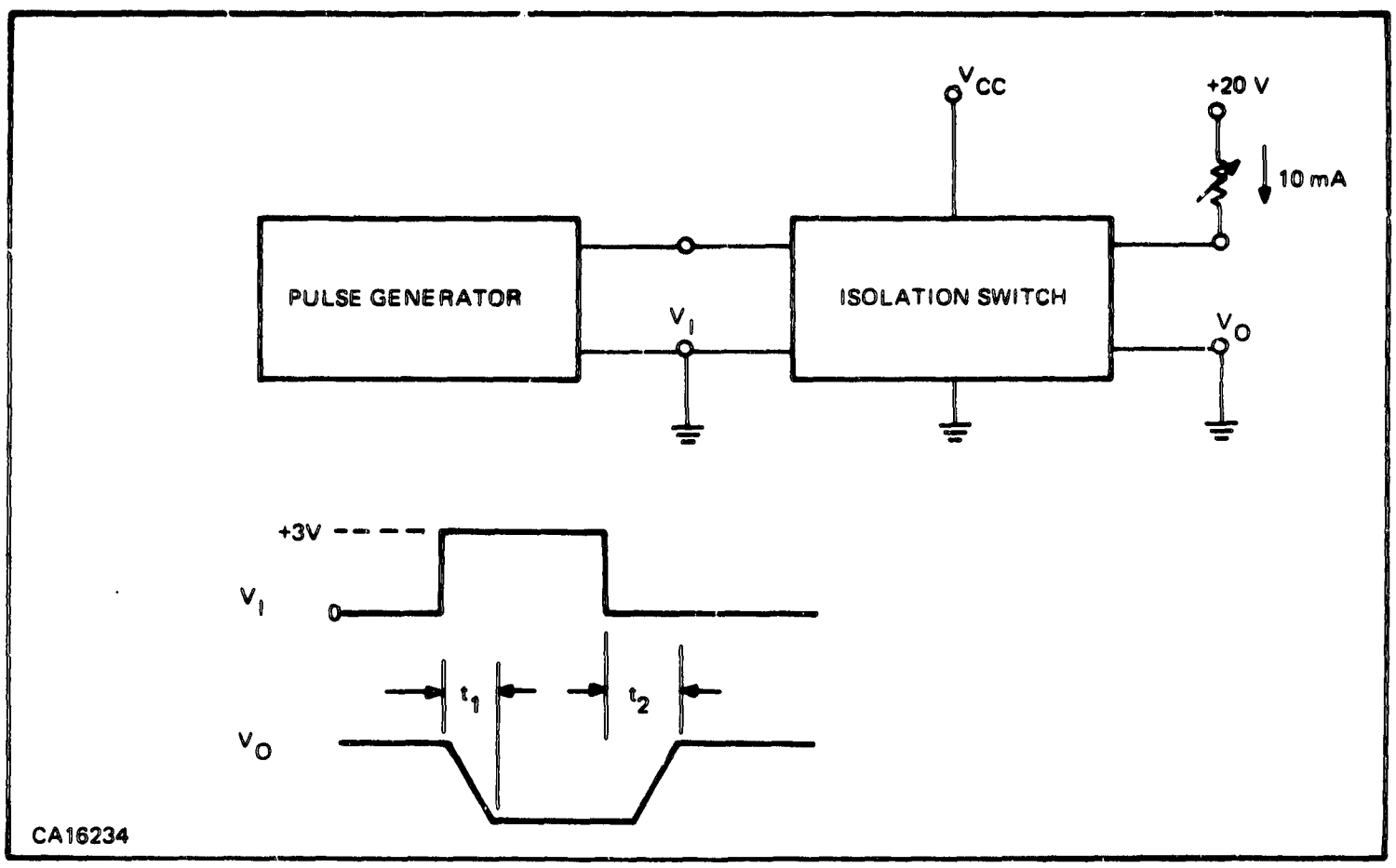


Figure 2. Switching Time Test

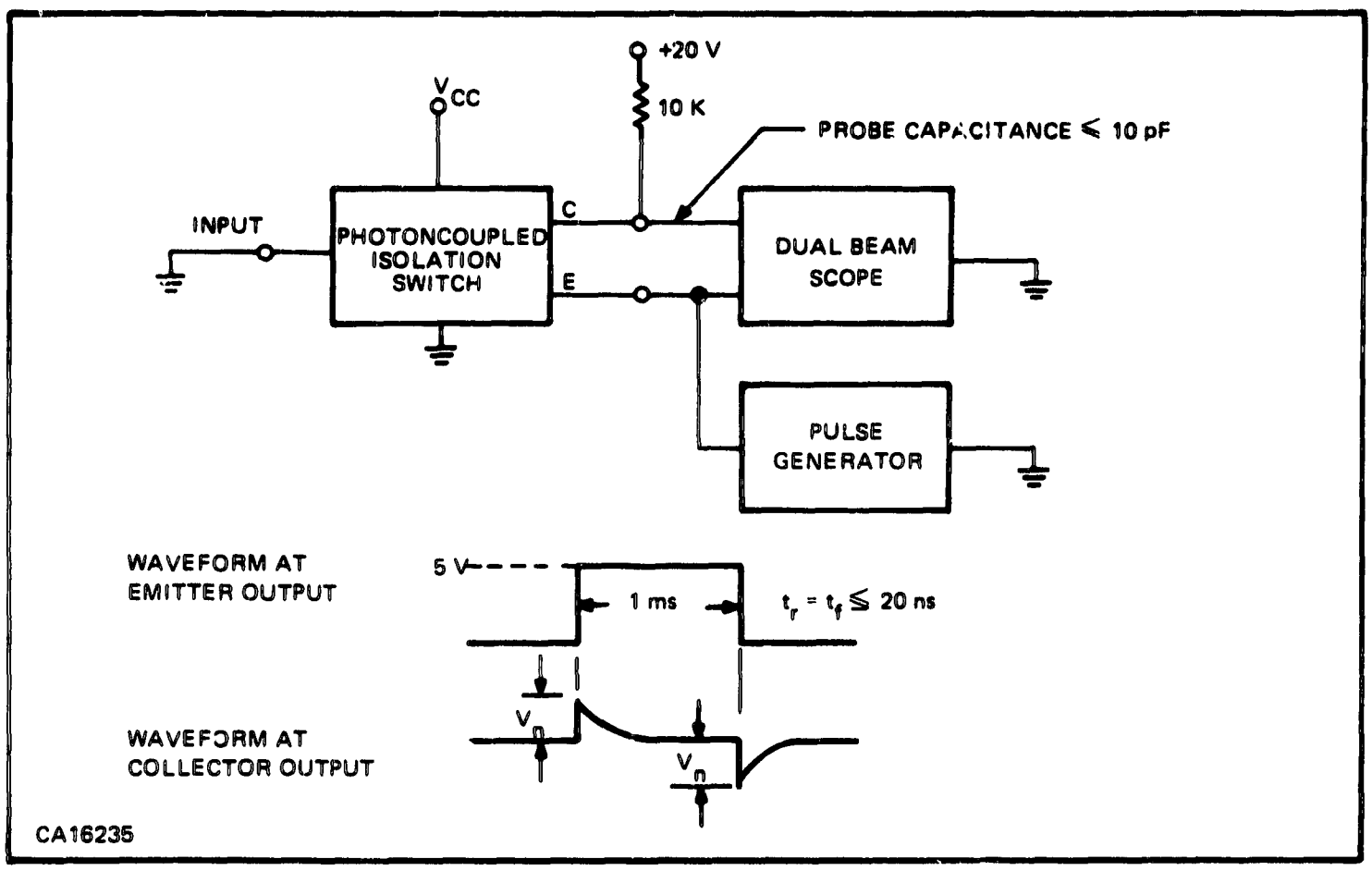


Figure 3. Noise Transmissibility Test

Considering the small available supply voltage, a single saturable transistor should be used in series with the emitting diode. The sum of their voltage drops is likely to be a significant part of the available voltage. The ±12.5 percent supply-voltage range could result in a significantly greater emitting diode current tolerance.

Diffused resistors have a generally positive temperature coefficient, their values increasing with increasing temperature. Conversely, the emitting efficiency of GaAs diodes has a negative coefficient. Use of this resistor for current limiting produces less current for the emitting diode in the face of a falling efficiency with increasing temperature. Thus the worst case for photon emission is at the greatest operating temperature. This situation is offset somewhat by the positive temperature coefficient of the current gain of typical Si transistors. The positive temperature coefficient of diffused resistors also produce the worst case for power dissipation in the "1" condition at the lowest operating temperature.

4. Driver Parameter Data

a. General

Evaluation of various potential circuit arrangements can be conducted from a thorough characterization of the driver circuit components and emitting diode. It is intended that a triple-diffused IC technique be used for fabrication of the driver circuit. Parameter evaluation of this type of IC processing was conducted on the IC of the optically coupled isolator, TI-type

TIXL106. The IC of this device has emitter-, base-, and collector-type diffused resistors and enlarged (NPN) transistors as required for the current levels of the isolation switch. The emitting diode characterized is also that used in the TIXL106. This diode is appropriate for use in the isolation switch.

b. Resistor Characteristics

Preliminary data for resistors made simultaneously with the emitter, base, and collector diffusions are shown in Table II. Evaluation of the data indicated preference for the base-type diffused resistors if a single type were chosen for all resistors in the driver circuit, provided the area required on the IC wafer for any large-value resistors would not be excessively large. The base-type resistor has the smallest temperature coefficient of resistance of the three types, which would permit a greater tolerance for all other important parameters in the circuit. In addition the base sheet resistance can generally be controlled to a closer tolerance. A more thorough evaluation of base-type diffused resistors is given in Table III. This consists of 10 base-type resistors measured at 11 temperatures covering the range of from - 30°C to +125°C. The typical resistance-temperature characteristic for the base-type resistors is shown in Figure 4. For the values of each of the resistors in Table III normalized to 25°C values, the maximum range for all resistors at - 20°C and at +100°C was only ±0.7 percent. Smaller ranges are indicated at the temperature points between - 20°C and +100°C. This indicates the good uniformity obtained with the base-type resistors. From the data,

Table II. Resistance at Several Temperatures for Diffused Resistors in the TIXL106

	Emitter Type			Base Type			Collector Type		
Unit	T = -20°C	25°C	100°C	-20°C	25°C	100°C	-20°C	25°C	100°C
A1	16.4	18.0	19.9	4.36 K	4.50 K	4.98 K	12.7 K	16.6 K	24.6 K
A2	15.3	16.6	18.7	3.34 K	4.52 K	5.04 K	14.2 K	18.5 K	27.8 K
A3	16.0	17.4	19.5	4.80 K	4.96 K	5.62 K	13.0 K	16.9 K	25.3 K
A4	15.6	16.9	19.1						
A5	15.9	17.3	19.4						
A6	15.9	17.1	19.4						
A7	15.6	16.8	18.7						
A8	15.7	16.7	19.1						
B1	24.5	26.4	30.5						
B2	22.5	24.5	28.2						
B3	24.0	26.1	29.8						
B4	23.0	25.1	28.7						
B5	23.5	25.6	29.3						
B6	23.6	25.9	29.2						
B7	22.6	24.7	28.1						
B8	23.0	24.6	28.4						

Values in Ohms

Table III. Resistance in Ohms of Base-Type Diffused Resistors as Function of Temperature

	Temperature										
Unit	-30°C	-25°C	-20°C	-10°C	0°C	25°C	40°C	60°C	80°C	100°C	125°C
1	1952	1956	1961	1974	1993	2059	2112	2188	2272	2364	2488
2	1828	1830	1833	1846	1864	1919	1963	2030	2106	2188	2301
3	2012	2014	2019	2031	2044	2099	2144	2215	2295	2377	2500
4	1968	1971	1976	1990	2008	2073	2121	2193	2277	2268	2386
5	1886	1888	1892	1907	1924	1985	2033	2102	2177	2268	2386
6	1955	1957	1960	1973	1991	2052	2099	2172	2252	2341	2462
7	1782	1785	1791	1808	1827	1888	1936	2004	2081	2165	2278
8	2038	2039	2042	2054	2073	2136	2182	2255	2337	2426	2548
9	1969	1972	1976	1988	2003	2058	2102	2171	2250	2337	2451
10	1978	1982	1986	2002	2023	2090	2138	2212	2297	2385	2507

the temperature-coefficient limits for design of the driver-circuit (base-type) resistors can be expressed in terms of the resistances at -20°C and +100°C, relative to that at 25°C, as follows:

$$0.948 \leqslant R(-20°C)/R(25°C) \leqslant 0.962$$
$$1.132 \leqslant R(100°C)/R(25°C) \leqslant 1.149$$

where R(T) is the resistance at temperature T.

Other approaches, such as the use of low-temperature-coefficient thin-film resistors, could provide improvements in future modifications of the driver circuit.

c. IC Transistor Characteristics

Current Gain. Forward, common-emitter current gains for the IC transistors at collector currents of 1, 7, and 30 mA at -20, 25, and 100°C are given in Table IV. Current gains are substantially greater at the highest temperature. This is of importance for the driver circuit, since the minimum base current also occurs at the highest temperature, due to the positive-temperature coefficients of the diffused resistors.

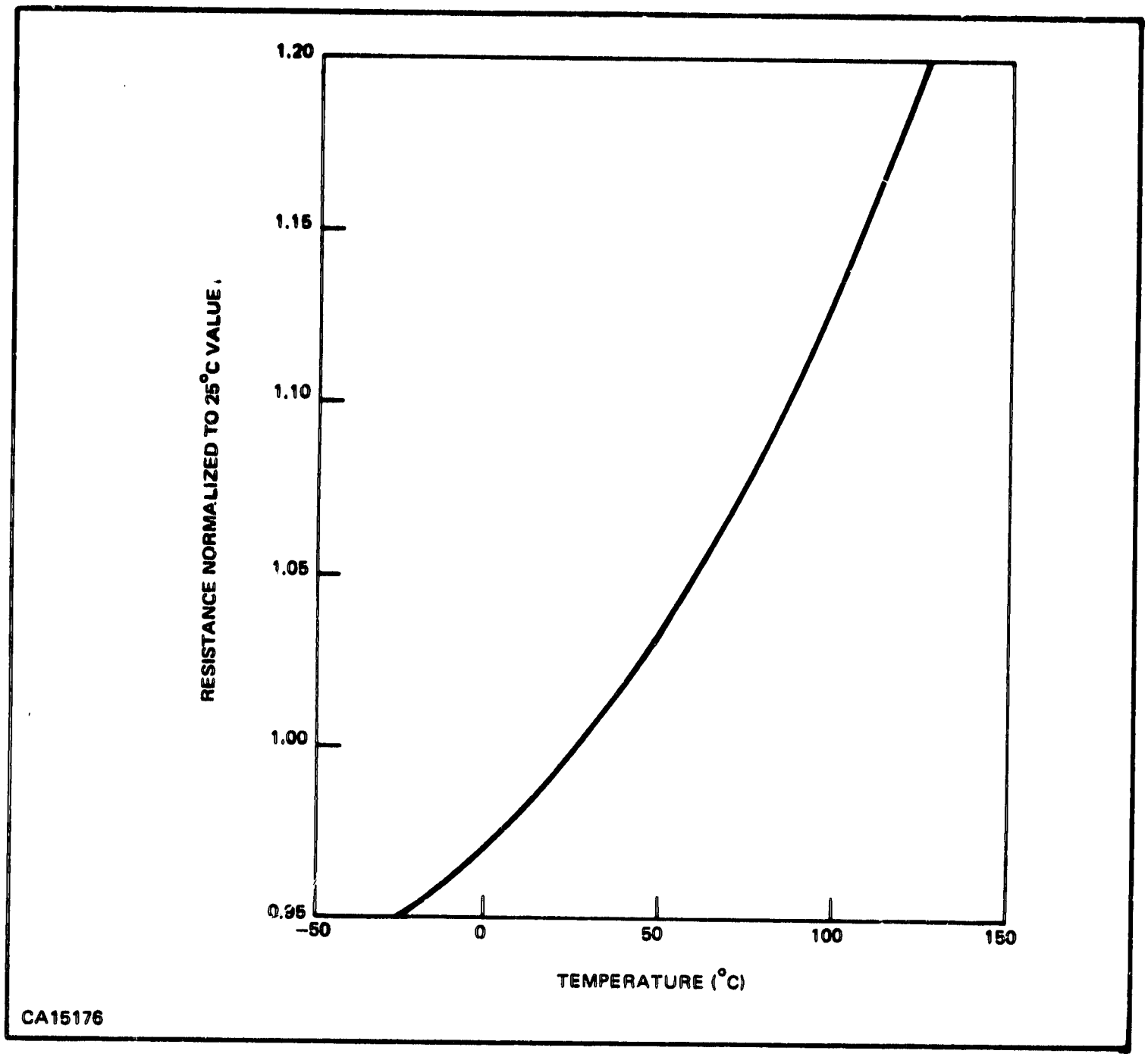


Figure 4. Typical Resistance-Temperature Characteristic

Base-Emitter and Collector-Emitter Voltages. Precise evaluation of the base-emitter forward-diode voltage-drop, V_{BE}, and the collector-emitter saturation voltage, V_{CE}, characteristics requires consideration of the effects of all three (base, emitter, and collector) transistor currents. Analysis indicates that a convenient form for the data would be measurements at specific emitter currents for multiple ratios of collector-to-base currents, due to the fact that V_{BE} and V_{CES} are relatively slowly varying functions of these variables.

The test circuit used to characterize the voltage characteristics of driver-circuit transistors is shown in Figure 5. In this test circuit, common-base connections of PNP transistors are used as constant-current sources for the base and collector currents of the transistor under test. Emitter

Table IV. Forward Current Gain Characteristics for Transistors on the TIXL106

Unit	T = −20°C			25°C			100°C		
	h_{FE} I_C = 1 mA	h_{FE} 7 mA	h_{FE} 30 mA	h_{FE} I_C = 1 mA	h_{FE} 7 mA	h_{FE} 30 mA	h_{FE} I_C = 1 mA	h_{FE} 7 mA	h_{FE} 30 mA
Q1	118	118	79	152	159	114	204	222	162
Q2	36	44	35	60	70	57	119	108	102
Q3	133	133	86	173	175	126	212	250	178
Q4	75	80	58	100	109	81	147	156	119
Q5	70	78	55	91	103	77	141	150	113
Q6	80	77	54	102	103	76	133	142	106
Q7	105	93	75	143	152	109	222	222	158

V_{CE} = 2 V

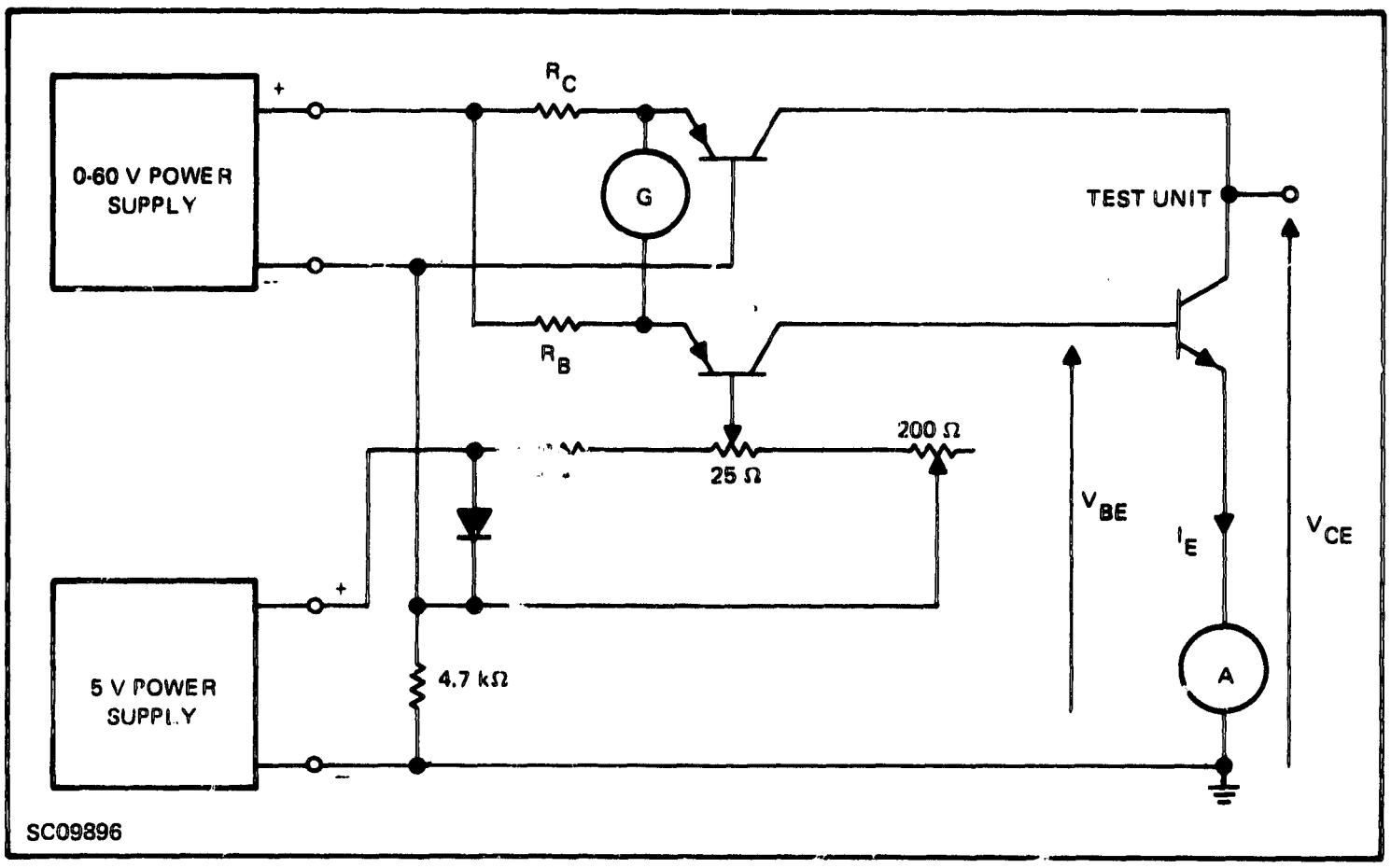


Figure 5. Test Circuit for Characterization of Driver Circuit Transistors

current is measured with meter A. Meter G is an electronic null meter. Resistors R_B and R_C are precision decade resistance units. Voltages V_{CE} and V_{BE} are measured using a voltmeter with an input impedance of 200 megohms. These voltages are measured as functions of the ratio of collector to base currents I_C/I_B and emitter current I_E.

The measurement procedure begins with the selection of I_C/I_B. Resistors R_B and R_C are set so that R_B/R_C is equal to I_C/I_B. Then the variable power supply is adjusted to set the desired emitter current I_E. The 200-ohm and 25-ohm variable resistors are adjusted to null meter G. Usually, after the power-supply and nulling-resistor settings are touched up, a group of similar transistors may be tested with no further adjustments. In practice the test units, in an environmental test chamber, are switch-selected for connection to the external test circuits. Tables V, VI, VII, VIII, and IX give transistor V_{CES} and V_{BE} results. The particular I_E and I_C/I_B values are appropriate to the circuit analyses for lower- and higher-current transistors. Included are data for very-low-current conditions, as for the transistor-input gate of the TTL-type circuit.

For a diode-input gate it would be appropriate, for uniform results, to produce the diode from a similar NPN transistor having the base and collector terminals in common. Leakage data for such a connection are shown in Table X.

d. Emitting-Diode V-I Characteristics

The forward-voltage-current, V_D-I_D, characteristics of typical planar-diffused GaAs photon-emitting diodes, as used in the TIXL106, are given in Table XI. The diodes were evaluated at 6 current levels at - 20, 25, and 100°C.

As will be described in the worst case analysis, the photon emission can be closely related to the voltage applied to the emitting diode. Shunt impedance effects cause variations in the diode V_D - I_D characteristics in the low current region but do not affect the V_D-photon emission relation. Tests on GaAs switches indicate negligible photon emission in the off-condition, and thereby negligible increase in phototransistor leakage current (compared to the 10 μA maximum leakage specified), for diode forward voltages of no more than 0.89, 0.80, 0.70 V at - 20, 25, and 100°C, respectively.

5. Circuit Design

a. General

There are a multitude of potential driver-circuit arrangements. Many of these are eliminated with the conclusion, in the following section, that a diode-gate input circuit should be used. Elimination of additional potential circuits of various arrangements is based on analyses with the characterization data and confirming measurements with breadboard circuits. No satisfactory arrangement for a type of constant-current circuit, for biasing of the emitting diode, could be derived which would operate with the minimum supply voltage of 3.5 V without a significantly greater power dissipation in the off-condition than the specified 1 mW. Thus the biasing current is resistor limited, with a transistor switch in series with the emitting diode which is driven into saturation, as discussed previously.

Table V. Base-Emitter Voltages for Lower-Current Driver-Circuit Transistors

Parameter		V_{BE}											
Units		V											
Conditions		I_E = 0.5 mA			I_E = 1 mA			I_E = 2 mA			I_E = 5.5 mA		
T_A(°C)		−20°C	25°C	100°C	−20°C	25°C	100°C	−20°C	25°C	100°C	−20°C	25°C	100°C
Device No.	I_C/I_B												
1	30	0.790	0.706	0.560	0.810	0.730	0.592	0.832	0.750	0.622	0.880	0.800	0.690
	35	0.790	0.705	0.560	0.810	0.726	0.590	0.830	0.746	0.620	0.880	0.798	0.685
	40	0.786	0.704	0.560	0.808	0.725	0.588	0.830	0.746	0.620	0.875	0.796	0.682
2	30	0.775	0.690	0.542	0.796	0.716	0.574	0.822	0.738	0.610	0.878	0.799	0.685
	35	0.774	0.690	0.540	0.796	0.715	0.570	0.820	0.736	0.606	0.875	0.796	0.682
	40	0.775	0.688	0.540	0.795	0.714	0.570	0.820	0.736	0.605	0.874	0.794	0.678
3	30	0.782	0.700	0.555	0.802	0.722	0.582	0.825	0.740	0.616	0.870	0.794	0.682
	35	0.782	0.700	0.552	0.800	0.720	0.580	0.824	0.740	0.615	0.870	0.790	0.678
	40	0.782	0.698	0.552	0.800	0.720	0.580	0.822	0.740	0.612	0.866	0.786	0.674
4	30	0.761	0.672	0.525	0.785	0.700	0.558	0.815	0.728	0.595	0.860	0.785	0.668
	35	0.762	0.672	0.523	0.785	0.698	0.555	0.810	0.723	0.592	0.855	0.780	0.662
	40	0.761	0.671	0.521	0.783	0.695	0.554	0.810	0.722	0.590	0.850	0.778	0.658
5	30	0.770	0.681	0.535	0.790	0.708	0.565	0.820	0.735	0.600	0.860	0.790	0.673
	35	0.770	0.681	0.531	0.790	0.705	0.563	0.815	0.731	0.599	0.860	0.787	0.670
	40	0.770	0.680	0.531	0.790	0.703	0.562	0.815	0.730	0.596	0.860	0.783	0.665
6	30	0.778	0.689	0.541	0.795	0.711	0.570	0.820	0.739	0.605	0.862	0.791	0.673
	35	0.775	0.688	0.541	0.795	0.710	0.570	0.815	0.735	0.602	0.861	0.789	0.670
	40	0.775	0.688	0.540	0.793	0.710	0.568	0.815	0.733	0.601	0.860	0.785	0.665
7	30	0.770	0.681	0.533	0.792	0.708	0.565	0.820	0.737	0.601	0.870	0.800	0.680
	35	0.770	0.681	0.531	0.792	0.706	0.562	0.820	0.735	0.600	0.870	0.797	0.675
	40	0.770	0.680	0.531	0.790	0.705	0.561	0.820	0.732	0.599	0.870	0.792	0.671

Table VI. Collector-Emitter Voltages for Lower-Current Driver-Circuit Transistors

Parameter		V_{CE}											
Units		V											
Conditions		I_E = 0.5 mA			I_E = 1 mA			I_E = 2 mA			I_E = 5.5 mA		
T_A(°C)		−20°C	25°C	100°C	−25°C	25°C	100°C	−25°C	25°C	100°C	−25°C	25°C	100°C
Device No.	I_C/I_B												
1	30	0.082	0.088	0.103	0.088	0.096	0.113	0.104	0.112	0.136	0.160	0.178	0.216
	35	0.092	0.096	0.112	0.097	0.102	0.122	0.112	0.126	0.143	0.168	0.183	0.225
	40	0.102	0.104	0.118	0.108	0.112	0.127	0.120	0.126	0.150	0.178	0.202	0.233
2	30	0.074	0.074	0.081	0.078	0.083	0.096	0.095	0.106	0.128	0.168	0.192	0.238
	35	0.082	0.080	0.087	0.084	0.088	0.103	0.100	0.110	0.133	0.174	0.195	0.247
	40	0.092	0.086	0.097	0.090	0.092	0.107	0.105	0.113	0.137	0.178	0.205	0.251
3	30	0.078	0.086	0.102	0.087	0.097	0.119	0.110	0.120	0.152	0.178	0.202	0.253
	35	0.082	0.092	0.110	0.093	0.102	0.124	0.114	0.126	0.157	0.187	0.208	0.263
	40	0.090	0.097	0.115	0.098	0.108	0.130	0.120	0.132	0.162	0.194	0.220	0.272
4	30	0.045	0.049	0.058	0.053	0.059	0.073	0.069	0.080	0.100	0.122	0.147	0.183
	35	0.049	0.053	0.062	0.056	0.063	0.076	0.072	0.082	0.102	0.125	0.151	0.191
	40	0.053	0.056	0.065	0.059	0.066	0.079	0.074	0.085	0.107	0.131	0.153	0.197
5	30	0.058	0.064	0.076	0.066	0.075	0.092	0.092	0.097	0.121	0.142	0.170	0.215
	35	0.063	0.068	0.081	0.070	0.079	0.096	0.088	0.100	0.126	0.149	0.173	0.221
	40	0.067	0.072	0.085	0.074	0.082	0.100	0.091	0.105	0.130	0.153	0.180	0.229
6	30	0.065	0.073	0.088	0.073	0.084	0.103	0.089	0.108	0.132	0.151	0.180	0.230
	35	0.070	0.078	0.095	0.078	0.089	0.110	0.096	0.111	0.139	0.158	0.188	0.239
	40	0.075	0.083	0.099	0.082	0.093	0.112	0.099	0.115	0.142	0.165	0.192	0.246
7	30	0.059	0.064	0.076	0.069	0.077	0.093	0.090	0.100	0.125	0.161	0.190	0.243
	35	0.063	0.069	0.081	0.073	0.080	0.097	0 094	0.105	0.130	0.167	0.195	0.249
	40	0.068	0.073	0.086	0.077	0.084	0.101	0.098	0.109	0.132	0.173	0.199	0.251

Table VII. Base-Emitter Voltages for Higher-Current Driver-Circuit Transistors

Parameter		V_{BE}								
Units		V								
Conditions		I_E = 5.5 mA			I_E = 7.75 mA			I_E = 11 mA		
T_A(°C)		−20°C	25°C	100°C	−25°C	25°C	100°C	−20°C	25°C	100°C
Device No.	I_C/I_B									
1	15	0.895	0.818	0.708	0.920	0.840	0.740	0.945	0.875	0.780
	20	0.890	0.810	0.700	0.910	0.838	0.735	0.940	0.870	0.770
	25	0.885	0.804	0.695	0.905	0.830	0.726	0.934	0.860	0.760
2	15	0.890	0.815	0.705	0.920	0.845	0.742	0.950	0.880	0.782
	20	0.886	0.808	0.698	0.915	0.838	0.735	0.944	0.875	0.775
	25	0.882	0.800	0.692	0.910	0.833	0.725	0.940	0.870	0.765
3	15	0.882	0.806	0.700	0.905	0.830	0.734	0.930	0.860	0.766
	20	0.878	0.800	0.694	0.900	0.825	0.724	0.922	0.855	0.758
	25	0.875	0.797	0.686	0.896	0.820	0.718	0.918	0.850	0.750
4	20	0.865	0.792	0.680	0.889	0.820	0.711	0.910	0.848	0.742
	25	0.861	0.790	0.671	0.885	0.811	0.705	0.905	0.840	0.745
5	20	0.870	0.800	0.688	0.895	0.825	0.718	0.920	0.855	0.751
	25	0.865	0.795	0.679	0.890	0.820	0.710	0.915	0.848	0.743
6	20	0.872	0.801	0.688	0.895	0.825	0.719	0.920	0.855	0.752
	25	0.868	0.796	0.680	0.890	0.821	0.710	0.915	0.849	0.743
7	20	0.871	0.810	0 690	0.910	0.840	0.729	0.940	0.872	0.769
	25	0.871	0.805	0.685	0.905	0.833	0.720	0.935	0.866	0.760

Table VIII. Collector-Emitter Voltages for Higher-Current Driver-Circuit Transistors

Parameter		V_{CE}								
Units		V								
Conditions		I_E = 5.5 mA			I_E = 7.75 mA			I_E = 11 mA		
T_A(°C)		−20°C	25°C	100°C	−20°C	25°C	100°C	−25°C	25°C	100°C
Device No.	I_C/I_B									
1	15	0.136	0.152	0.183	0.167	0.190	0.225	0.208	0.230	0.282
	20	0.144	0.160	0.197	0.178	0.198	0.242	0.224	0.245	0.301
	25	0.153	0.170	0.207	0.188	0.208	0.254	0.238	0.260	0.320
2	15	0.152	0.167	0.201	0.192	0.213	0.253	0.246	0.268	0.330
	20	0.158	0.180	0.217	0.205	0.227	0.272	0.265	0.290	0.350
	25	0.164	0.186	0.228	0.212	0.240	0.288	0.280	0.310	0.370
3	15	0.153	0.173	0.213	0.192	0.216	0.267	0.242	0.270	0.340
	20	0.163	0.185	0.230	0.203	0.230	0.287	0.262	0.290	0.370
	25	0.172	0.193	0.243	0.215	0.243	0.303	0.277	0.310	0.400
4	20	0.115	0.135	0.172	0.146	0.171	0.219	0.189	0.220	0.279
	25	0.120	0.141	0.179	0.152	0.179	0.226	0.199	0.230	0.290
5	20	0.131	0.154	0.198	0.165	0.192	0.247	0.211	0.248	0.310
	25	0.139	0.161	0.205	0.175	0.201	0.258	0.225	0.260	0.330
6	20	0.140	0.162	0.208	0.172	0.201	0.259	0.221	0.259	0.330
	25	0.148	0.172	0.219	0.182	0.212	0.271	0.238	0.275	0.350
7	20	0.152	0.179	0.229	0.200	0.232	0.299	0.269	0.310	0.390
	25	0.158	0.185	0.235	0.208	0.241	0.301	0.278	0.320	0.410

Table IX. Base-Emitter and Collector-Emitter Voltages for Characterization of Transistor Input Devices

Parameter		V_{BE}						V_{CE}					
Units		V						V					
Conditions		V_{BE} for I_E = 0.1 mA			V_{BE} for I_E = 0.2 mA			V_{CE} for I_E = 0.1 mA			V_{CE} for I_E = 0.2 mA		
T_A(°C)		−20°C	25°C	100°C	−20°C	25°C	100°C	−20°C	25°C	100°C	−25°C	25°C	100°C
Device No.	I_C/I_B												
1	30	0.750	0.660	0.502	0.765	0.680	0.528	0.084	0.087	0.098	0.082	0.086	0.098
	35	0.750	0.660	0.502	0.765	0.680	0.526	0.100	0.097	0.108	0.093	0.095	0.108
	40	0.750	0.660	0.502	0.765	0.680	0.528	0.345	0.110	0.117	0.110	0.104	0.116
2	30	0.730	0.642	0.484	0.750	0.660	0.508	0.125	0.084	0.075	0.089	0.076	0.075
	35	0.734	0.642	0.484	0.750	0.660	0.506	0.157	0.096	0.082	0.107	0.084	0.081
	40	0.734	0.644	0.482	0.750	0.660	0.505	0.233	0.107	0.088	0.130	0.092	0.087
3	30	0.744	0.656	0.498	0.760	0.675	0.520	0.076	0.081	0.093	0.074	0.086	0.094
	35	0.744	0.656	0.498	0.760	0.674	0.520	0.084	0.088	0.100	0.082	0.088	0.101
	40	0.744	0.656	0.496	0.760	0.672	0.520	0.094	0.095	0.108	0.089	0.094	0.108
4	30	0.720	0.622	0.468	0.740	0.645	0.492	0.049	0.046	0.048	0.045	0.046	0.050
	35	0.720	0.622	0.468	0.740	0.645	0.491	0.054	0.051	0.052	0.049	0.050	0.054
	40	0.720	0.622	0.465	0.738	0.642	0.490	0.060	0.055	0.056	0.054	0.054	0.058
5	30	0.730	0.632	0.479	0.748	0.655	0.501	0.063	0.060	0.066	0.058	0.059	0.068
	35	0.728	0.632	0.479	0.747	0.653	0.501	0.070	0.065	0.071	0.063	0.064	0.073
	40	0.728	0.632	0.478	0.745	0.652	0.500	0.078	0.071	0.076	0.069	0.069	0.077
6	30	0.738	0.642	0.488	0.752	0.661	0.510	0.064	0.069	0.080	0.063	0.069	0.082
	35	0.735	0.642	0.487	0.752	0.661	0.510	0.071	0.075	0.087	0.068	0.075	0.088
	40	0.735	0.642	0.485	0.752	0.660	0.509	0.077	0.081	0.093	0.073	0.080	0.093
7	30	0.732	0.635	0.478	0.748	0.655	0.500	0.054	0.057	0.066	0.054	0.058	0.068
	35	0.730	0.632	0.478	0.747	0.655	0.500	0.060	0.062	0.072	0.059	0.063	0.073
	40	0.730	0.632	0.476	0.746	0.652	0.500	0.065	0.067	0.076	0.064	0.068	0.077

Table X. Leakage Currents for Diode-Connected NPN Transistors*

Device	I_R (nA)
1	1.0
2	8.5
3	9.3
4	11.1
5	11.0
6	11.5

*Emitter as cathode and common base and collector as anode, V_R = 6 V, T = 100°C.

Table XI. Forward Voltage–Current Characteristics of GaAs Photon-Emitting Diodes

Device No.	V_D (V) at I_D (mA) shown						T(°C)
	0.1	0.5	1	5	10	40	
1	1.00	1.09	1.12	1.18	1.20	1.25	-20
2	1.03	1.12	1.15	1.20	1.22	1.26	-20
3	1.02	1.10	1.13	1.18	1.20	1.24	-20
1	0.91	1.4	1.4	1.11	1.14	1.19	25
2	0.94	1.04	1.06	1.11	1.14	1.18	25
3	0.94	1.04	1.07	1.12	1.14	1.20	25
1	0.77	0.88	0.93	1.01	1.03	1.11	100
2	0.80	0.91	0.95	1.02	1.06	1.13	100
3	0.78	0.89	0.94	1.02	1.04	1.11	100

Examples of circuit arrangements considered for the driver circuit are shown in Figure 6. Circuits 1 through 5 indicate various positions of the GaAs diode and current-limiting resistors with two transistors, and 6 through 8 indicate three-transistor arrangements. All have the diode-gate input circuit. Examination of the data taken on the variation in the parameters and their temperature characteristics eliminated consideration of all but one of the circuits. As illustrated in the worst-case design of the selected circuit, a complete analysis is fairly complex and lengthy. for brevity the results of analyses for the circuits in Figure 6 are summarized as follows:

1) Two transistor configurations without the GaAs diode in the ground section of the circuits are not cut off at any temperature with a 1-V input (specified as maximum in the off-condition). These include circuits 1, 2, and 3. Resistors in the emitter-base string, as in circuits 2 and 3, are ineffective for assisting cut-off at the low-current levels.

2) The inadequate cut-off is also characteristic of both of the three-transistor circuits at the higher temperatures.

3) Of the remaining circuits, 4 and 5, circuit 5 requires greater transistor current gains. The base voltage of the first transistor can be at a greater voltage level in the on-condition, and thus less base current can be available through the base resistor.

4) Circuit 4 is marginally on with a 1-V input. Slight modifications available to ensure cut-off include the addition of resistors from each emitter to ground, as shown in Figure 7. A resistor on the emitter of the input transistor increases by a small amount the current in that emitter in the off-condition, increasing the emitter-base voltage slightly. The resistor to the second emitter shunts the emitting diode for the low currents. At the high currents of the on-condition, the logarithmic characteristic of the diode results in most of the current being delivered to the diode. The circuit in Figure 7 is that selected for the driver circuit and analyzed in a subsequent section.

b. Input Configuration

Connections for the ten inputs are detailed in Figure 8. Figure 8a shows a diode-connected-transistor input device; Figure 8b, an active transistor input device. By connecting each transistor as shown in Figure 8b, the voltage at the base terminal of the following transistor, Q_1, can be made smaller than for connection (a) by proper selection of R_A and R_B. The object of this connection is to make certain that the photon-emitting diode current will be small when V_I = 1 V. The lower limit for R_A is set by the requirement $(I_{RA})\ (V_{CC\ max}) \leq 1$ mW when $V_I = 0$. This requirement gives $I_{RA} \leq 0.222$ mA for $V_{CC} = 4.0 \pm 0.5$ V. Because the base-emitter voltages for the input devices are nearly the same for connections (a) and (b), R_A and R_1 are equal. For the "1" state the total resistance between supply and the base terminal of Q_1 is R_1 for connection (a), and $R_1 + R_B$ for connection (b). At the lower limits of supply voltage, less base current is available in connection (b), requiring a larger minimum gain for Q_1.

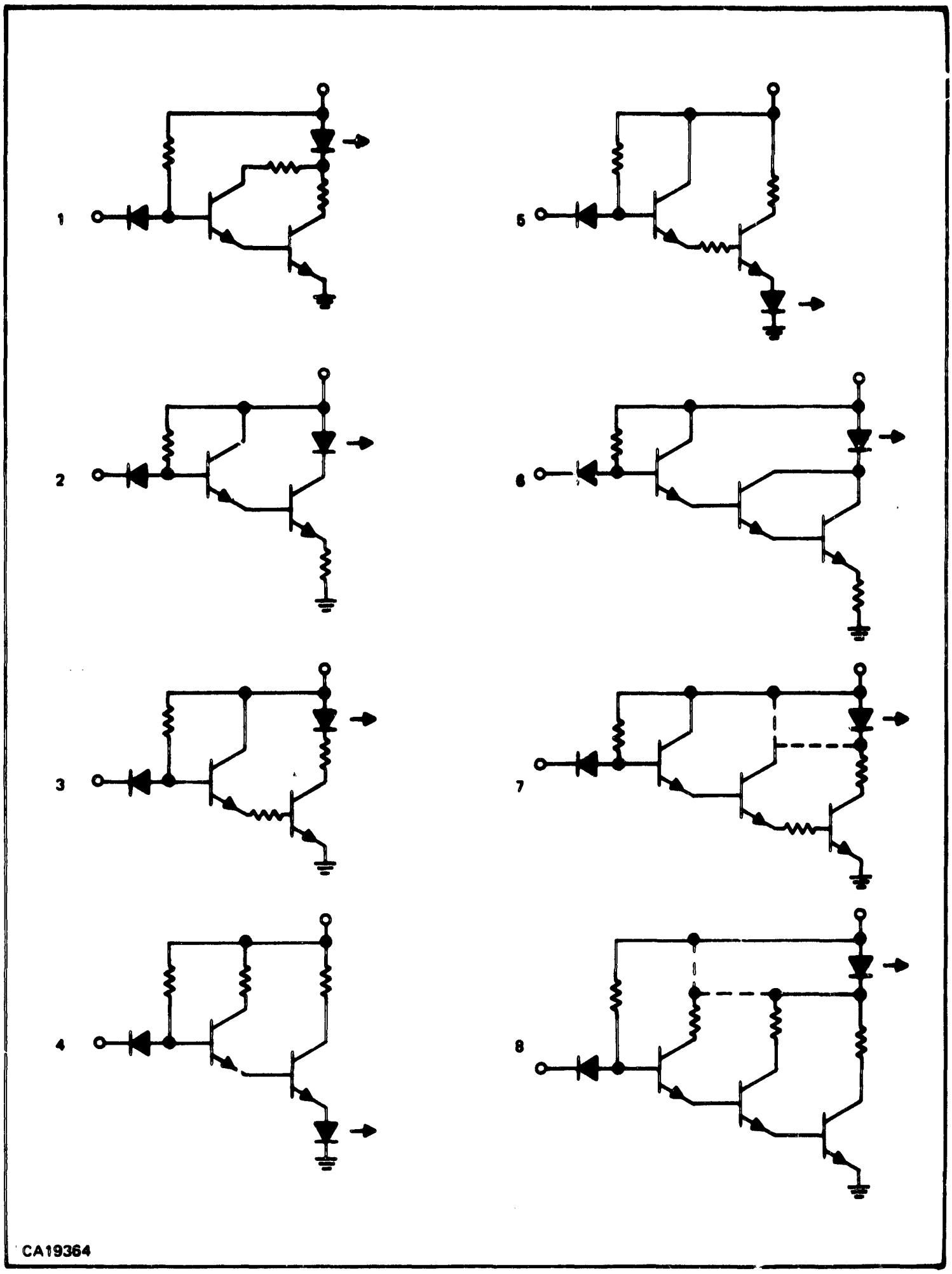


Figure 6. Circuit Arrangements Considered for the Driver Circuit

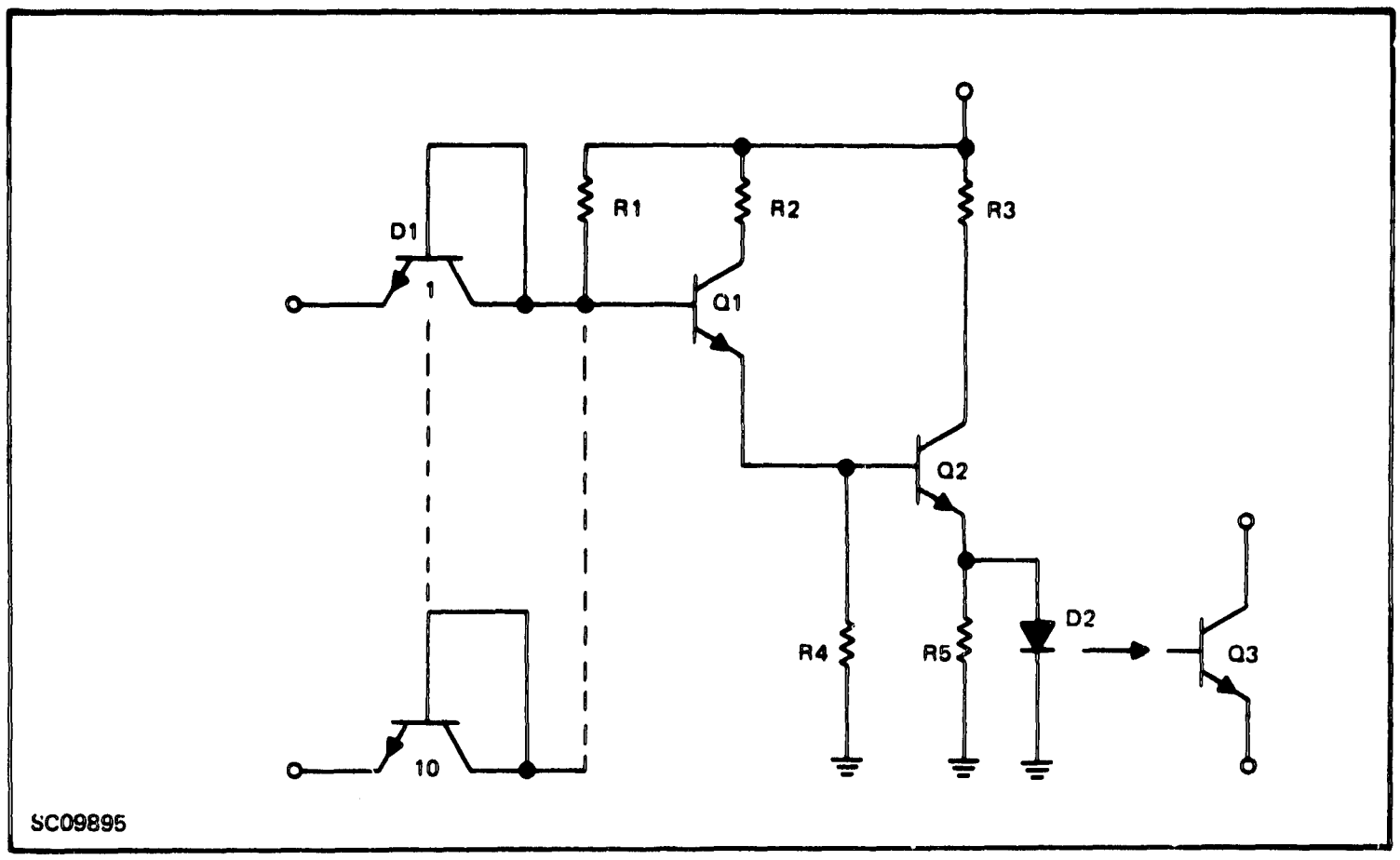


Figure 7. Isolation Switch Schematic Showing Driver Circuit Selected for Design

In connection (a) the inputs are isolated from each other by a reverse-biased junction when one input is on and another off. For connection (b) interaction between inputs is possible, as indicated in Figure 8c. With zero input voltage for transistor Q_A and transistor Q_A in saturation, the base collector junction of transistor Q_B is forward biased while the base-emitter junction is reverse biased. Transistor Q_B is thus biased for inverse operation. In contrast to connection (a), where input currents are limited to junction leakages, input currents for connection (c) can be large if V_{BC} is large. Note that V_{BC} is the difference between V_{BE} and V_{CE} of transistor Q_A. At 100°C and $I_C/I_B \leq 30$, $V_{BC} \leq 0.43$ V. For $V_{BC} = 0.43$ V, I_E for transistor Q_B can be 60 μA. A worst-case analysis for this input connection would require $V_{BC\ max} = 0.68$ V at - 20°C. Again, about 60-μA input current could result.

Because of the interaction between inputs and because less base drive is available for Q_1, the transistor input connection is not desirable.

The leakage characteristics of diode-connected transistors were described in Table X. These data were taken for a diode reverse voltage of 6 V, actually greater than that experienced by the diode-connected transistor in Figure 8a by the amount of the base voltage of Q_1. The leakages were all less than 12 nA at 100°C for the six measured diodes, compared to the specification of 50 μA.

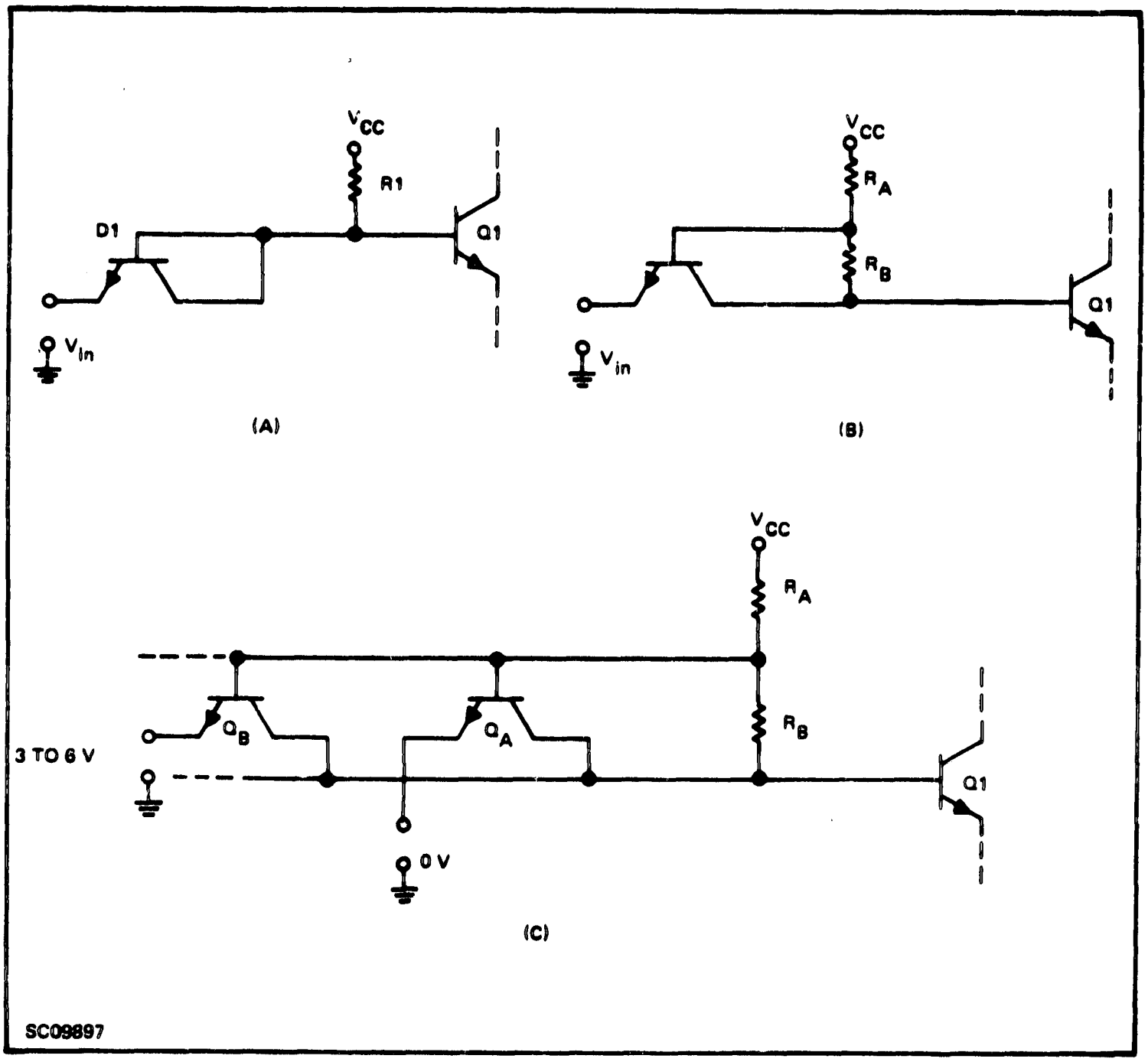


Figure 8. Alternate Driver Circuit Input Connections

c. Worst-Case Analysis

The design of the driver-circuit resistors depends on the assignment of worst-case resistor tolerances based on the resistor sheet resistance and geometry variances. The most critical resistor is R3. For each of two metallization patterns used, the tolerance factor for R3 is 1.06, which will be taken to mean that the upper limiting value of R3 is 1.06 times its nominal value, and that the lower limit is the nominal value divided by 1.06. On this basis the tolerance factors for the remaining resistors are 1.11 for R2, 1.15 for R1, and 1.24 for R4 and R5.

The measurements taken to characterize representative transistors and diodes demonstrated that saturation voltages and base-emitter voltages are well-behaved functions of emitter current and the ratio of collector-to-base current. A list of worst-case voltages for extreme values of supply voltage at -20°C, +25°C, and +100°C is given in Table XII, with the resulting worst-case voltages

Table XII. Worst-Case Voltages Assumed for Driver-Circuit Design

		Temperature					
		-20°C		25°C		100°C	
V_{CC}	(V)	3.5	4.5	3.5	4.5	3.5	4.5
V_{CE2}	(V)	0.19	0.20	0.22	0.22	0.25	0.28
V_{BE2}	(V)	0.88	0.89	0.80	0.84	0.69	0.74
V_{CE1}	(V)	0.11	0.06	0.11	0.08	0.13	0.10
V_{BE1}	(V)	0.81	0.80	0.73	0.72	0.59	0.59
V_{D2}	(V)	1.32	1.20	1.25	1.14	1.14	1.05
V_{R1}	(V)	0.49	1.61	0.72	1.80	1.08	2.12
V_{R2}	(V)	1.19	2.35	1.34	2.44	1.54	2.61
V_{R3}	(V)	1.99	3.10	2.03	3.14	2.11	3.17
V_{R4}	(V)	2.20	2.09	2.15	1.98	1.73	1.79
V_{R5}	(V)	1.32	1.20	1.25	1.14	1.14	1.05

across resistors R1 through R5. Included are worst-case allowable values of GaAs photon-emitting diode voltages. Combinations of these worst-case voltages with the resistor temperature coefficients and circuit specifications were used to design the resistors.

Resistors R1, R4, and R5 depend on conditions when the GaAs diode is off or non-conducting. Resistor R1 controls the circuit power dissipation, P_{OFF}, with V_{CC} = 4.5 V and V_I = 0. The worst case occurs at - 20°C, for which R_1 is minimum (see Figure 4).

$$P_{OFF_{MAX}} = 4.5\ V\ (4.5\ V - 0.7\ V)/R1_{MIN} \qquad (1)$$

$$= 17.1\ V^2/R1_{MIN}$$

For the expression above, the voltage across R1 is 4.5 V less the minimum voltage across an input diode, 0.7 V. Applying worst-case tolerance and temperature-coefficient factors, the nominal 25°C design value of R1 is given by

$$R1 = (1.15)\ (17.1)/(0.948)P_{OFF},\ \text{in k}\Omega \quad \text{for} \qquad (2)$$

P_{OFF} in mW

Resistors R4 and R5 are designed to limit the maximum voltage across D2, the GaAs diode, for the off-condition when the input voltage is one volt. The photon emission from the diode is approximately proportional to exp (qV_D/kT).[4] At 100°C a diode voltage of 0.7 V can be tolerated. For an input voltage of 1 V, an input-diode voltage drop of 0.51 V, V_{BE1} of 0.41 V for I_{E1} = 0.036 mA, and V_{BE2} of 0.40 V for I_{E2} = 0.10 mA, the voltage across D2 will not exceed 0.7 V, which corresponds to a minimum diode current of 0.01 mA. The room-temperature values of R4 and R5 are given by

$$R4 = (1.1V)/(1.149)\ (1.24)\ (0.036\ \text{mA}),\ \text{in k}\Omega, \qquad (3)$$

$$R5 = (0.7\ V)/(1.149)\ (1.24)\ (0.10\ \text{mA} - 0.01\ \text{mA}), \qquad (4)$$

The design values to be used for R4 and R5 are

$$R4 = 21.4\ \text{k}\Omega,$$
$$R5 = 5.46\ \text{k}\Omega$$

The values of R4 and R5 are constrained to track the values of R1, R2, and R3 because all the resistors are diffused simultaneously, and only geometrical errors contribute to errors in the ratios of these resistors.

Table XIII gives the calculated worst-case values of R4 and R5 and the worst-case currents I_{R4} and I_{R5} for the conditions of Table XII.

The critical conditions when the input voltage is high (on-condition) are:

1) The maximum values of the ratios I_{C1}/I_{B1} and I_{C2}/I_{B2} for V_{CC} = 3.5 V and T = - 20°C, which specify the minimum allowable transistor gains.
2) The maximum circuit power dissipation for V_{CC} = 4.5 V and T = - 20°C.
3) The minimum GaAs diode current, I_{D2}, for V_{CC} = 3.5 V and T = 100°C.

Table XIII. Worst-Case Values of Resistors R4 and R5 and of Currents I_{R4} and I_{R5}

		Temperature					
		-20°C		25°C		100°C	
V_{CC}	(V)	3.5	4.5	3.5	4.5	3.5	4.5
R_4	(kΩ)	18.865	22.14	19.90	23.01	22.53	26.44
R_5	(kΩ)	4.81	5.65	5.08	5.87	5.75	6.75
I_{R4}	(mA)	0.117	0.0944	0.108	0.086	0.0768	0.0677
I_{R5}	(mA)	0.274	0.212	0.246	0.1942	0.1982	0.1556

The design equations which relate these factors will be developed with the following notation:

For T = -20°C

A = (I_{C1}/I_{B1}) MAX

B = (I_{C2}/I_{B2}) MAX

C = (17.1) (1.15)/0.948

D = $V_{R1\ MIN}/1.15$ = 0.49/1.15

E = $V_{R2\ MIN}/1.11$ = 1.19/1.11

F = $V_{R3\ MIN}/$ 1.06 = 1.99/1.06

G = 0.962 $I_{R4\ MAX}$ = (0.962) (2.20)/18.865

H = 0.948

I = 1.15 $V_{R1\ MAX}$ = (1.15) (1.61)

J = 1.11 $V_{R2\ MAX}$ = (1.11) (2.35)

K = 1.06 $V_{R3\ MAX}$ = (1.06) (3.10)

For T = +100°C

$$L = I_{R4\ MAX} + I_{R5\ MAX} = 0.275$$

$$I_D = I_{D2\ MIN} \text{ at } 100°C$$

$$M = V_{R1\ MIN}/(1.149)\ (1.15) = (1.08)/(1.149)\ (1.15)$$

$$N = V_{R2\ MIN}/\ (1.149)\ (1.11) = (1.54)/(1.149)\ (1.11)$$

$$P = V_{R3\ MIN}/(1.149)\ (1.06) = (2.11)/(1.149)\ (1.06)$$

The expression for R1, Equation (2), becomes

$$R1 = C/P_{OFF} \tag{5}$$

The collector-to-base current ratio, I_{C1}/I_{B1}, is given by

$$A = ER1/DR2 \tag{6}$$

which is solved for R2.

$$R2 = CE/ADP_{OFF} \tag{7}$$

Similarly, the ratio I_{C2}/I_{B2} is given by

$$B = \frac{F/R3}{D/R1 + E/R2 - G} \tag{8}$$

The maximum power dissipation at -20°C, P_{ON}, is given by

$$P_{ON} = (V_{CC}/H)(I/R1 + J/R2 + K/R3) \tag{9}$$

Either equation (8 or 9) can be solved for R3.

$$R3 = \frac{F/B}{DP_{OFF}/C + ADP_{OFF}/C - G} \tag{10}$$

$$R3 = \frac{K}{H\ P_{ON}/V_{CC} - I\ P_{OFF}/C - J\ ADP_{OFF}/CE} \tag{11}$$

R3 is eliminated by equating (10) and (11). The minimum transistor gain relation is obtained by letting B = A (equal transistor gains).

$$A^2 - (CG/DP_{OFF} - 1 - JF/KE)\ A \tag{12}$$

$$- (FI/KD)\ (CH\ P_{ON}/I\ V_{CC}\ P_{OFF} - 1) = 0$$

This quadratic equation in A is solved, and the minimum gain at 25°C is assumed to be

$$h_{FE\ MIN} = 2\ A \tag{13}$$

The minimum I_{D2} at 100°C is given by the sum of the currents in R1, R2, and R3, less the currents in R4 and R5. The expression is

$$I_D = M/R1 + N/R2 + P/R3 - L \tag{14}$$

Equations (5), (7), (10) and (14) give

$$I_D = \frac{M}{C}\left[P_{OFF}\left(1 + \frac{ND}{ME}A + \frac{PD}{MF}B + \frac{PD}{MF}AB\right)\right. \tag{15}$$

$$\left. - \frac{PCG}{MF}\right]B - L$$

The final forms of the design equations with B = A given below are Equations (12) and (15) with the appropriate worst-case values applied.

$$A^2 - \left(\frac{5.4617}{P_{OFF}} - 2.3901\right) A - 2.4826 \left(2.3602 \frac{P_{ON}}{P_{OFF}} - 1\right) = 0, \qquad (16)$$

$$I_D = 0.03940 \left[P_{OFF} (1 + 1.0682A + 0.4811A^2) - 2.6274A \right] - 0.275 \qquad (17)$$

This form of these equations allows the circuit design to be performed with selection of any two of the parameters P_{ON}, P_{OFF}, I_D, or A. For P_{ON} = 200 mW and P_{OFF} = 1 mW,

$$A = 35.77$$

$$I_D = 21.82 \text{ mA}$$

Applying equations (5), (7), (10), and (13):

$$h_{FE_{MIN}} = 72$$

$$R1 = 20.74 \text{ k}\Omega$$

$$R2 = 1.459 \text{ k}\Omega$$

$$R3 = 81.61 \ \Omega$$

The circuit layout is designed to give the required resistor values for nominal base-type diffusion sheet resistances of 97.5 and 109.5 ohms per square. The widths of the resistors are 10.75 mils for $R3_M$, 2 mils for R2 and $R3_P$, 1 mil for R1, and 0.5 mil for R4 and R5. The design lengths of these resistors are given in Table XIV. Based on these design values, specified parameter worst-case values are given in Table XV. The emitting diode worst-case minimum currents are calculated as 24.3, 24 and 21.8 mA at - 20, 25, and 100°C. Tests described in following sections use values of 24.5, 24, and 22 mA, respectively, with the values being rounded-off to the nearest, greater half-mA.

Table XIV. Design Lengths of Diffused Driver-Circuit Resistors

	Sheet Resistance		
Resistor	97.5 Ω/□	109.5 Ω/□	Unit
R1	213	198.5	mils
R2	30	26.5	mils
$R3_M$	9	9	mils
$R3_P$	---	14	mils
R4	110	98	mils
R5	28	25	mils

Table XV. Worst-Case Values of Circuit Characteristics Calculated for Designed Diffused Resistors

	Sheet Resistance		
Characteristic	97.5 Ω/□	109.5 Ω/□	Unit
P_{ON}	199.98	199.45	mW
P_{OFF}	0.999	0.9997	mW
$ID2_{MIN}(100°C)$	21.84	21.75	mA
$(I_{C1}/I_{B1})_{MAX}$	35.72	35.98	
$(I_{C2}/I_{B2})_{MAX}$	36.84	35.41	

B. GaAs-SWITCH DEVELOPMENT

1. General Construction

The optical coupling technique to be used for the emitting diode-phototransistor pair, or GaAs switch, is similar to that for the TIXL106, pictured in Figure 9. The emitting diode is to be bonded to the transistor with a thin layer of an Se-S-As glass. This glass, on melting at higher temperatures, wets both the GaAs and Si surfaces, this being important for good optical coupling and mechanical rigidity. Thus the functions of the glass are a non-conductive cement and a good optical coupling medium. The requirements for the glass are as follows:

- Good mechanical adhesion to GaAs and Si
- Relatively transparent for 0.9-μm photons of GaAs
- Good thermal expansion match to GaAs and Si
- Bonding temperature compatible with fabrication and reliability
- High refractive index (~2.5) compared to those of GaAs (3.3) and Si (3.5).[5]

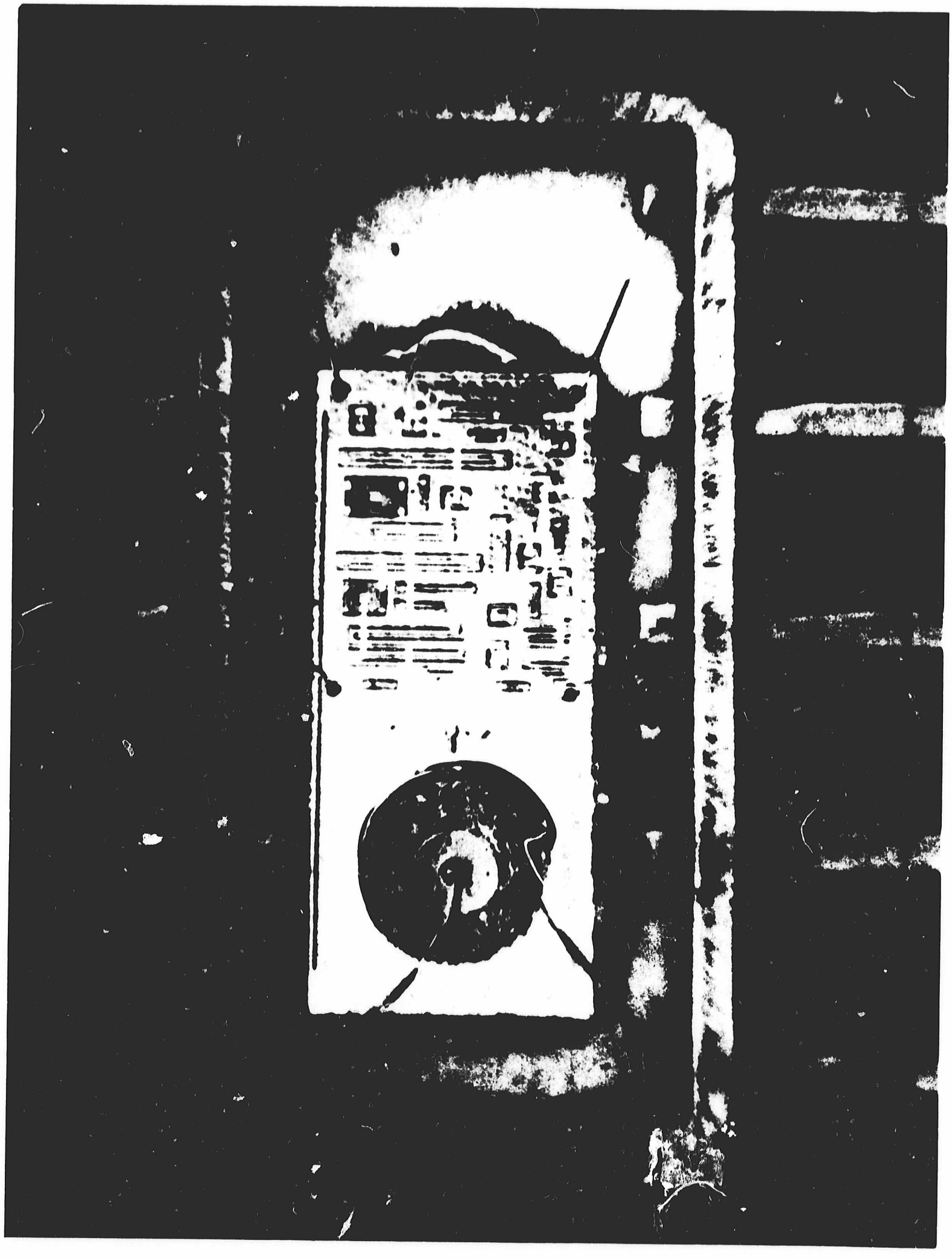


Figure 9. Uncanned TIXL 106

These are highly restrictive requirements. Only a few types of glasses can be considered. Two glasses which to date best satisfy the requirements are in the Se-S-As family. The bonding operation is performed at approximately 210°C. Tests have been made to evaluate softening within the operating and storage temperature extremes of the GaAs switch. At 100°C the glasses are moderately soft, demonstrating no tendency to flow. However, there is some question whether this would be sufficient at this temperature in a highly vibrating environment. For this reason encapsulation is desirable. At 150°C the glasses are fairly soft with some tendency to flow. The good wetting characteristics and surface tension of the glasses tend to hold the wafers in stable positions at 150°C. Encapsulation can also ensure structural integrity at this temperature.

The coupling glasses tested tend to have about the same temperature range (Δ T) for satisfactory operation. The above glasses previously exhibited highly stable low-temperature coupling characteristics to below - 55°C and are presently used in the TIXL106. Other glasses have shown tendencies to fracture at the low-temperature extremes, causing some variance in the coupling on temperature cycling. Additional testing is described in a subsequent section.

The encapsulation used in the TIXL106 is a proprietary epoxy compound which wets the wafers, coupling glass and glass in the bottom of the header. The epoxy is cured to a very rigid state. It is quite firm at 100°C; at 150°C, when deformed under high pressure, it is elastic. Tests show that application of this epoxy directly on the entire surface of the phototransitor results in no increase in high-temperature leakage.

Photons are emitted from the P-N junction region of the diode, which is approximately 10 mils in diameter. The size of the sensitive region of the transistor must be selected accordingly, with allowances made for the extreme paths of photons through the materials and an additional small amount for alignment tolerance. A sensitive region of about 20 mils in diameter is appropriate.

The transistor emitter region is covered with a contacting metal and thus should be outside the photon path. Portions of the base and collector form the photosensitive regions. The GaAs switch construction is illustrated in Figure 10. Details are discussed in following sections. The package used for Phase I GaAs switches is the JEDEC type TO-89, 1/8 × 1/4-inch integrated circuit flat-pack.

The thin-glass coupling medium provides an isolation voltage of over 100 volts in the TIXL106, which is greater than the design goal of 50 V previously indicated. Also, the isolation coupling capacitance is typically only about 3 pF, compared to the 10-pF maximum specification.

2. GaAs Photon-Emitting Diode

The construction of a GaAs photon-emitting diode such as used in the TIXL106 is shown in Figure 11. The diode is formed with a planar, oxide-passivated, P-type diffusion made into an N-type slice. Metal contacts to both the anode and cathode are formed on the same side of the GaAs wafer, with photons exiting from the opposite side. For the GaAs switch (and isolation switch), diodes are selected by screening visually under a high-magnification microscope for a pinhole-free passivation oxide over the planar-diffused PN junction; and for good contact metallization and also screening electrically for a low-leakage reverse characteristic and a sharp "knee" in the forward-voltage current characteristic.

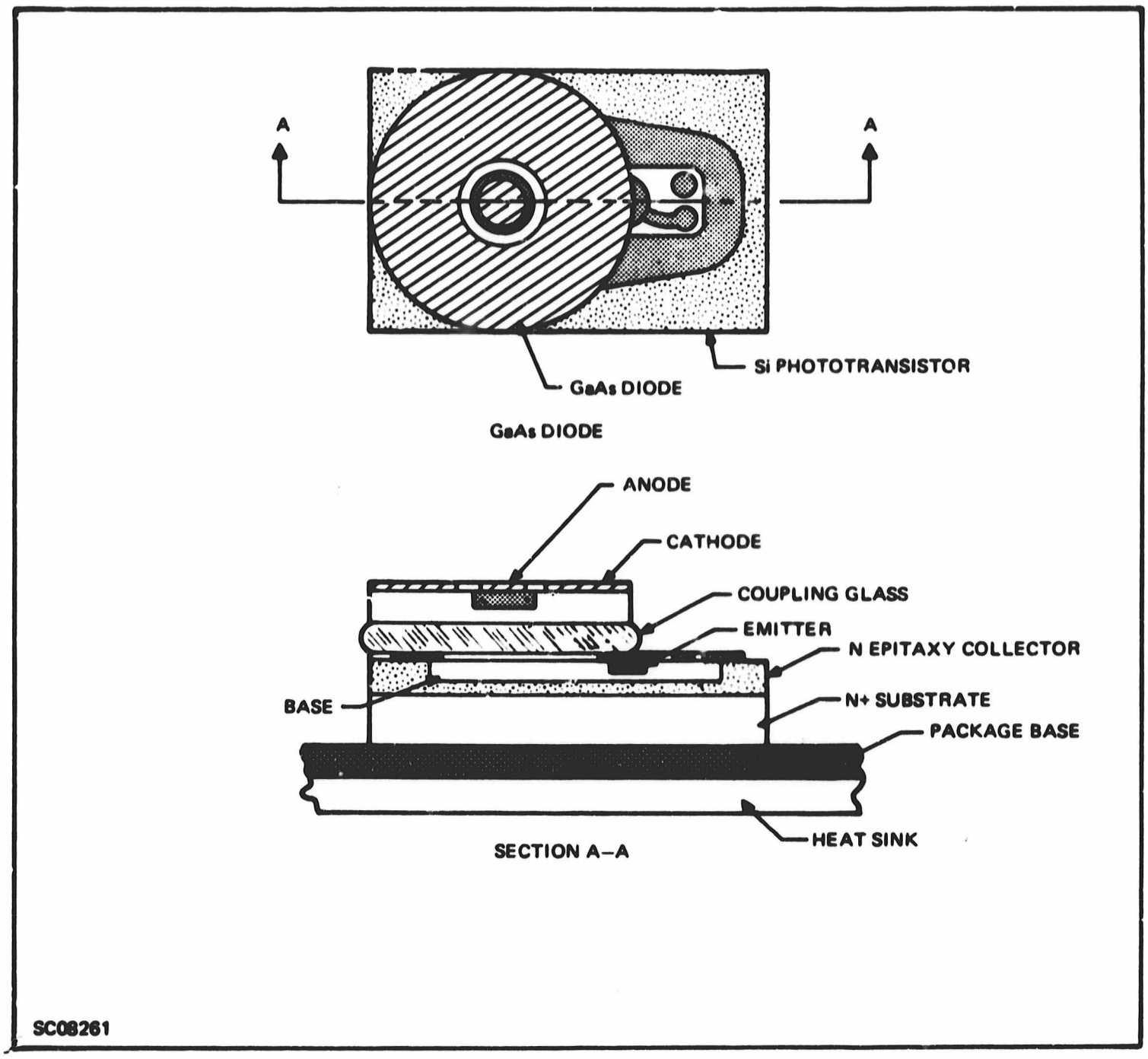


Figure 10. GaAs Switch Construction

The diameter of the junction is typically 10 mils, and the outside dimensions of the diode wafer vary from a 40-mil diameter, as shown in Figure 11, down to about 26 mils square. Although all devices delivered in the program used the 40-mil-diameter wafer, the thermal results described later indicate that the small wafer would be equally satisfactory. Photons are generated predominatly in an area near the junction in the P-region. No development was required for the diodes, as they are generally available for fabrication as discrete emitting diodes or for assembly in other photon-coupled devices.

Pertinent photo-emission characteristics for the emitting diode are considered in the designs of the phototransistor.

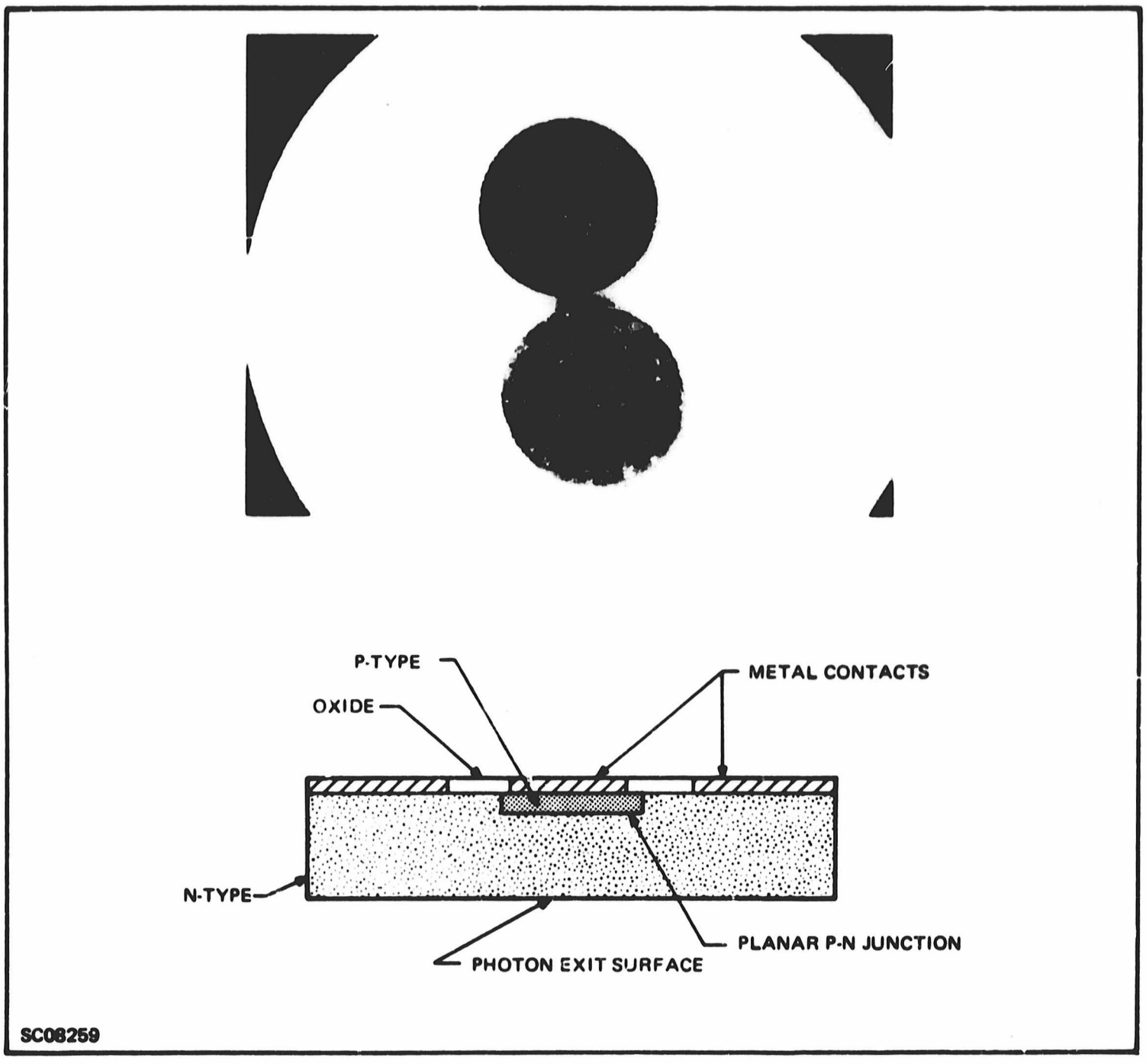


Figure 11. GaAs Photon Emitting Diode

3. Phototransistor Layout

The concept of the phototransistor design is illustrated in Figure 12. The starting material consists of an N^+ substrate with about 1 mil of high-resistivity N-type epitaxy. This epitaxial-layer thickness is of the order of an absorption length[6] for the 0.9-μm emission of the GaAs diode for adequate optical absorption (considering also the minority carrier diffusion lengths), suitably low saturation voltage, and good material availability.

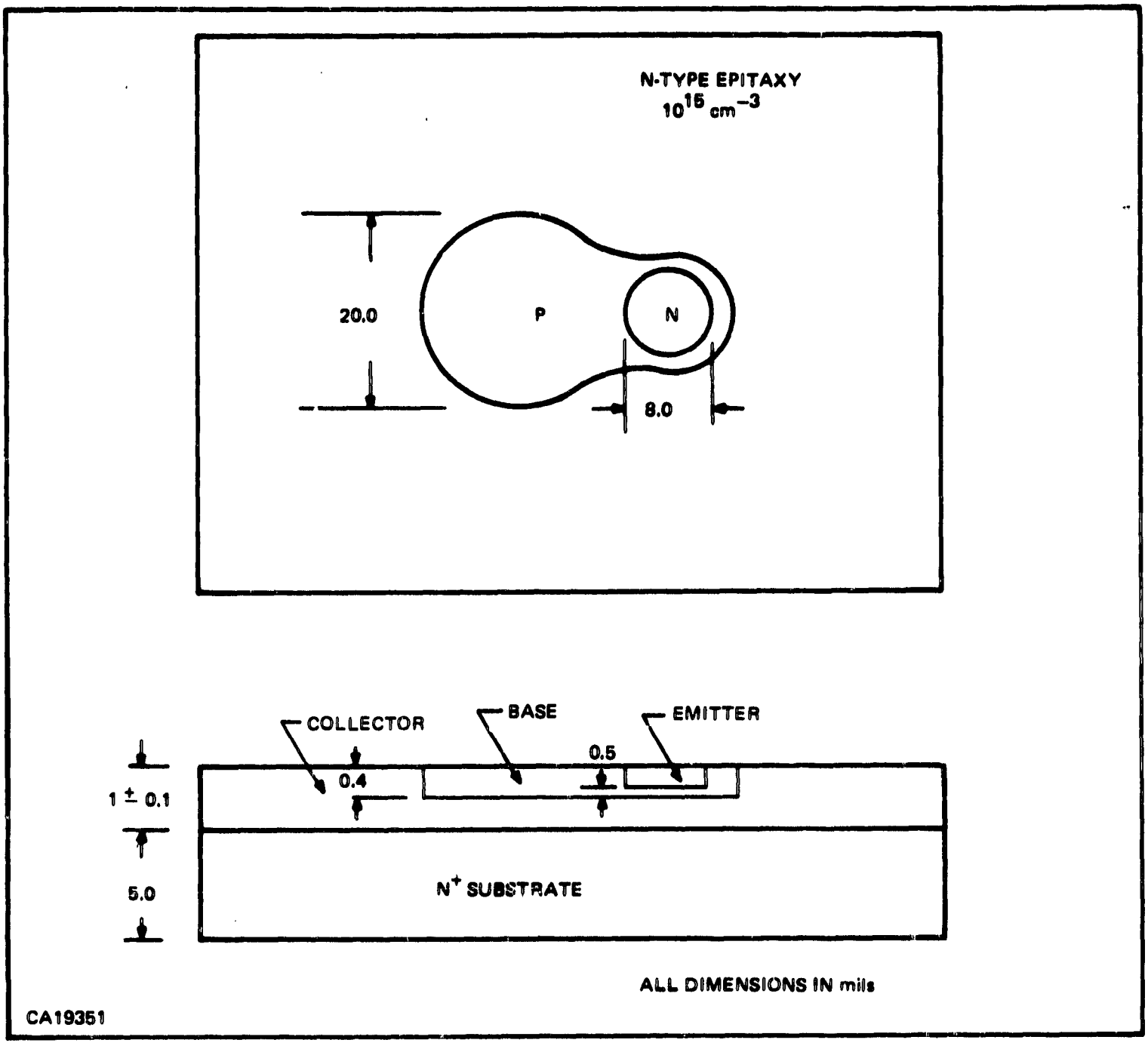


Figure 12. Basic Phototransistor-Diffusion Outline

Basic considerations for the phototransistor layout are as follows:

a) The base should be of sufficient size to serve as the photosensitive area and, of course, enclose the emitter.

b) The base and emitter should have small areas for low capacitance as related to speed and noise transmissibility.

c) The emitter should have sufficient size to satisfy the saturation-voltage requirement.

The photosensitive region required for the base can be determined with reference to the physical dimensions of the emitting diode and the glass layer and to the respective refractive indices. This type of analysis indicates the size of the sensitive area onto which a significant fraction of the available photons would impinge. In the limit, an infinitely large base would be required in collecting all available photons. A diameter for the base sensitive area of about twice the diameter of the emitting junction (nominally 10 mils) has been found to be practical for structures of this size for good photo-collection without excessive collection areas. This size also allows for normal tolerances when placing the diode over the sensitive area.

Based on parameter calculations, such as in the following sections, a phototransistor layout was made as shown in Figure 13. This layout utilized a 22-mil-diameter photosensitive area (window in the base oxide) and an 11-mil-diameter emitter (after diffusion). As is discussed in a following section, high-leakage currents were exhibited by devices made with this structure in the GaAs switch. Analysis indicated the need for modifications, consisting of a guardring surrounding the base (see Figure 14) and a field relief electrode (see Figure 15). These are later discussed in detail. Devices made with the second structure satisfied the design goals. For both structures, calculations of collector-base and emitter-base junction capacitances indicated that the base and emitter areas were appropriate for both the required speed and the immunity to noise transmission. In addition, the emitter in the second structure was reduced to 10 mils and the base sensitive area to 20 mils to obtain smaller junction capacitances. These changes were based on data for devices using the first structure which indicated the need for an additional margin for speed. The compromises were made considering the highly conservative results obtained for saturation voltage and photon coupling. Photographs of the modified phototransistor with and without the emitting diode are shown in Figure 16.

4. Design and Results

a. General

In this section the considerations made for the various design parameters are discussed. Following the analysis of each parameter are the test results. Considerable compromising was required among the various parameters to meet the design specifications. Expressions are described which can be used to examine the trade-offs involved and extrapolate the results for other design conditions. Both the calculations and test results refer to the use of the modified phototransistor structure unless otherwise indicated. The Phase I GaAs switches were subjected to a 100-hour burn-in period prior to final testing, in which 50 mA of forward bias was applied to the GaAs diode in a 25°C air ambient. For Phase I, ten GaAs switches were fabricated with and ten without the epoxy encapsulation.

b. Current-Gain Requirements

The transistor is so designed that the photons are absorbed in the base and collector regions. Photons absorbed within a diffusion length from the collector-base junction diffuse toward the junction, thereby creating bias current. This can be measured as a conduction current between the

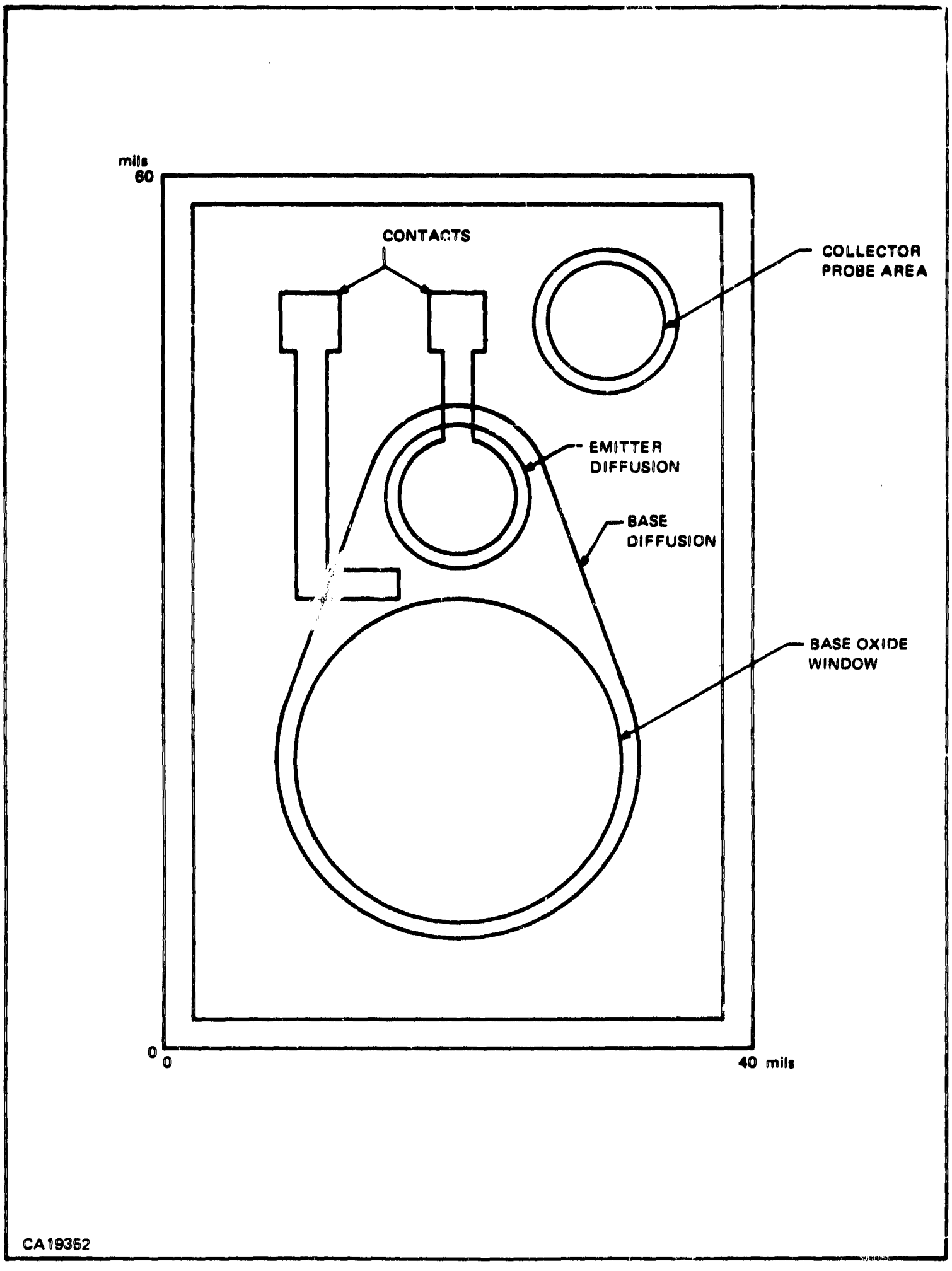


Figure 13. Preliminary Photo Transistor Layout

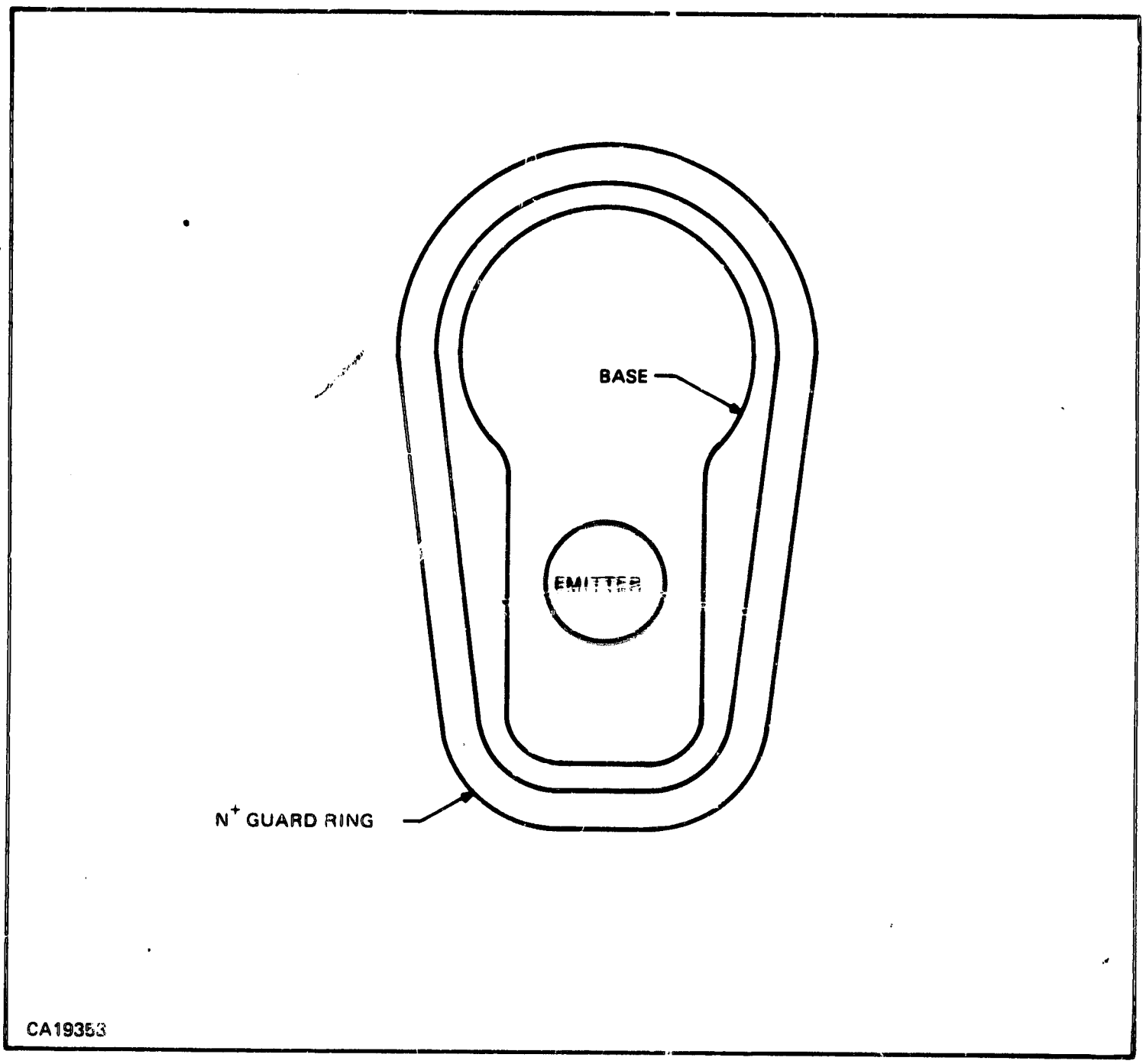


Figure 14. Phototransistor Diffusion Layout

collector and base leads. The photocurrent is effectively produced by a current generator across these terminals and thus can be considered a collector-base bias current. The current available from the collector and emitter terminals is the product of the effective base current and the transistor common-emitter current gain.

The current gain required can be represented as the ratio of the required collector current to the available base current. The collector current in the on-condition is specified to be a minimum of 10 mA at 0.6 V collector-to-emitter voltage, which may be near the saturated bias condition for the transistor. Using a conservative increase of 20 percent in the equivalent base current as sufficient for the out-of-saturation condition for GaAs switches having the least overall current gain, the minimum collector current out-of-saturation at 100°C is 12 mA. Allowing an additional 20 percent

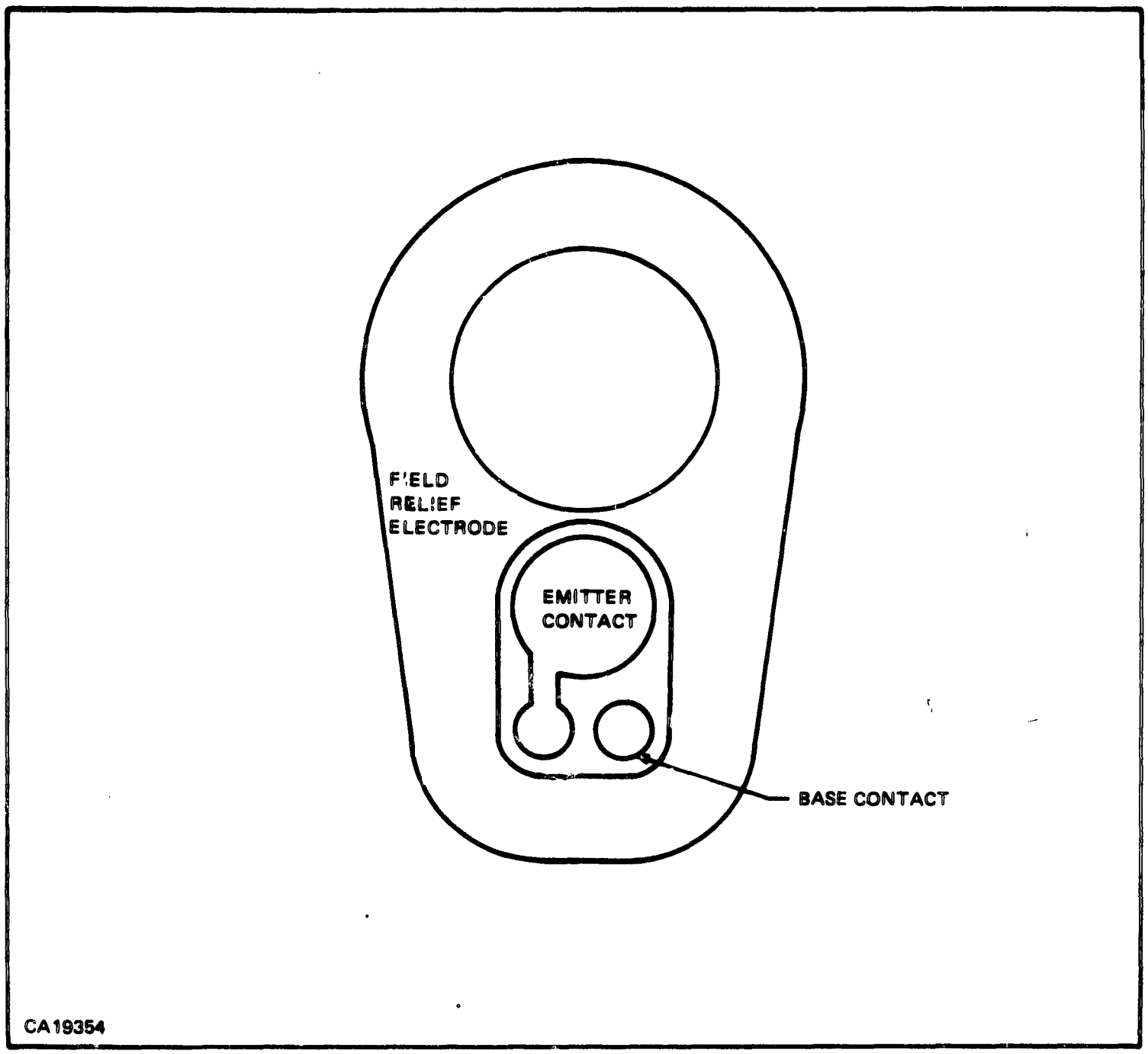


Figure 15. Metallization Layout

factor for both ageing effects in the GaAs diode which might reduce its light emission and in the Si transistor which might decrease its current gain, the minimum acceptable initial collector current out of saturation at 100°C is:

$$I_{C_{\substack{\text{Unsat.}\\ \text{Initial}\\ 100°C}}} \geq \frac{12.0\ \text{mA}}{0.80} = 15\ \text{mA}$$

A temperature of 100°C is specified because this is the worst-case temperature for current gain. Both the photon-emitting efficiency of the GaAs diode and the bias current for the diode decrease with increasing temperature.

Figure 16. Si Phototransistor and GaAs Switch

From past experience with the TIXL106, which uses basically the same type of photon coupling, the equivalent base current was estimated to be in the range of 20 to 40 μA at 100°C for GaAs diodes having "average" photon emission and operated at the worst-case bias of 22 mA. The current gain required for 20-μA base current is

$$h_{FE_{100°C}} = \frac{15 \text{ mA}}{20 \ \mu\text{A}} = 750$$

and for 40-μA base current, 375. Allowing an additional 20% margin in gain for high utilization of emitting diodes, the required gain range is 450 to 900. The forward-current gain characteristics of three high-gain transistors previously fabricated for coupling with an emitting diode are shown in Table XVI. For a collector current of 10 mA the current gains increased an average of about a factor of 1.3 for a temperature increasing from 25°C to 100°C. Using this figure, the required current gain at 25°C should be in the range of 350 to 700. Choosing a design objective for h_{FE} of 500, gains ranging from about 200 to 700 should be produced. An arbitrarily narrow range can be provided by probing of the individual wafers.

Substantiating data for the available equivalent base current were taken for transistors made with the initial structure. For a number of units the photo-induced current in the phototransistor was measured by shorting the collector and emitter terminals, and measuring the short-circuit

Table XVI. Forward Current Gains of Phototransistors

Unit No.	h_{FE} at I_C = 1 mA	h_{FE} at 5 mA	h_{FE} at 10 mA	T (°C)
1	417	495	488	−20
2	400	467	465	−20
3	200	296	320	−20
1	527	641	625	25
2	500	618	599	25
3	263	368	396	25
1	769	894	820	100
2	769	862	787	100
3	385	513	549	100

V_{CE} = 6 V

current between this connection and the base lead (brought out for Phase I devices). Initial results for two batches of emitting diodes are shown in Table XVII. The first group (units 2 through 13) used GaAs diodes having outputs judged as ranging from "average" to "excellent." The second group used GaAs diodes with "poor" outputs. The latter GaAs diodes were not considered sufficiently good for Phase I devices, but were tested to obtain reference values. The data shown were measured at 25°C. A good estimate for the efficiency of the GaAs diodes at 100°C is 1/2 the 25°C value. For the first group of GaAs emitters the half-values range from 40 to 75 μA, and, for the second group, 16 to 20 μA. These values are in agreement with the range of 20 to 40 μA described previously for average GaAs diodes.

Table XVII. Photo-Induced Current in Phototransistor

I_D = 22 mA, T = 25°C		
Unit No.	I_X (μA)	1/2 I_X (μA)
2	143	71
3	85	42
7	87	43
8	80	40
10	118	59
11	108	54
13	150	75
A1	32	16
A2	32	16
A3	40	20
A4	34	16

For a GaAs diode current of 22 mA (100°C worst-case minimum value), the relationships between the phototransistor collector currents at 25°C and 100°C are shown in Figure 17 for 18 GaAs switches. Included are devices having high and low values of I_{CEO}. No clear-cut correlation was observed between the change in I_C with temperature and I_{CEO}, indicating that the change in h_{FE} with temperature is approximately the same for both high- and low-leakage devices. The h_{FE} characteristics at 25°C and 100°C are given as a function of I_C in Figure 18 for representative low leakage (Unit 23) and high leakage (Unit 19) devices. The fact that Unit 19 has nominally higher h_{FE} is of no particular consequence. Applying the 25°C and 100°C values of I_C for each device given in Figure 17, the ratio of h_{FE} at 100°C to that at 25°C is about 1.50 for both devices. Also from Figure 17, the average ratio of I_C at 100°C to that at 25°C is 0.85. The ratio of these values.

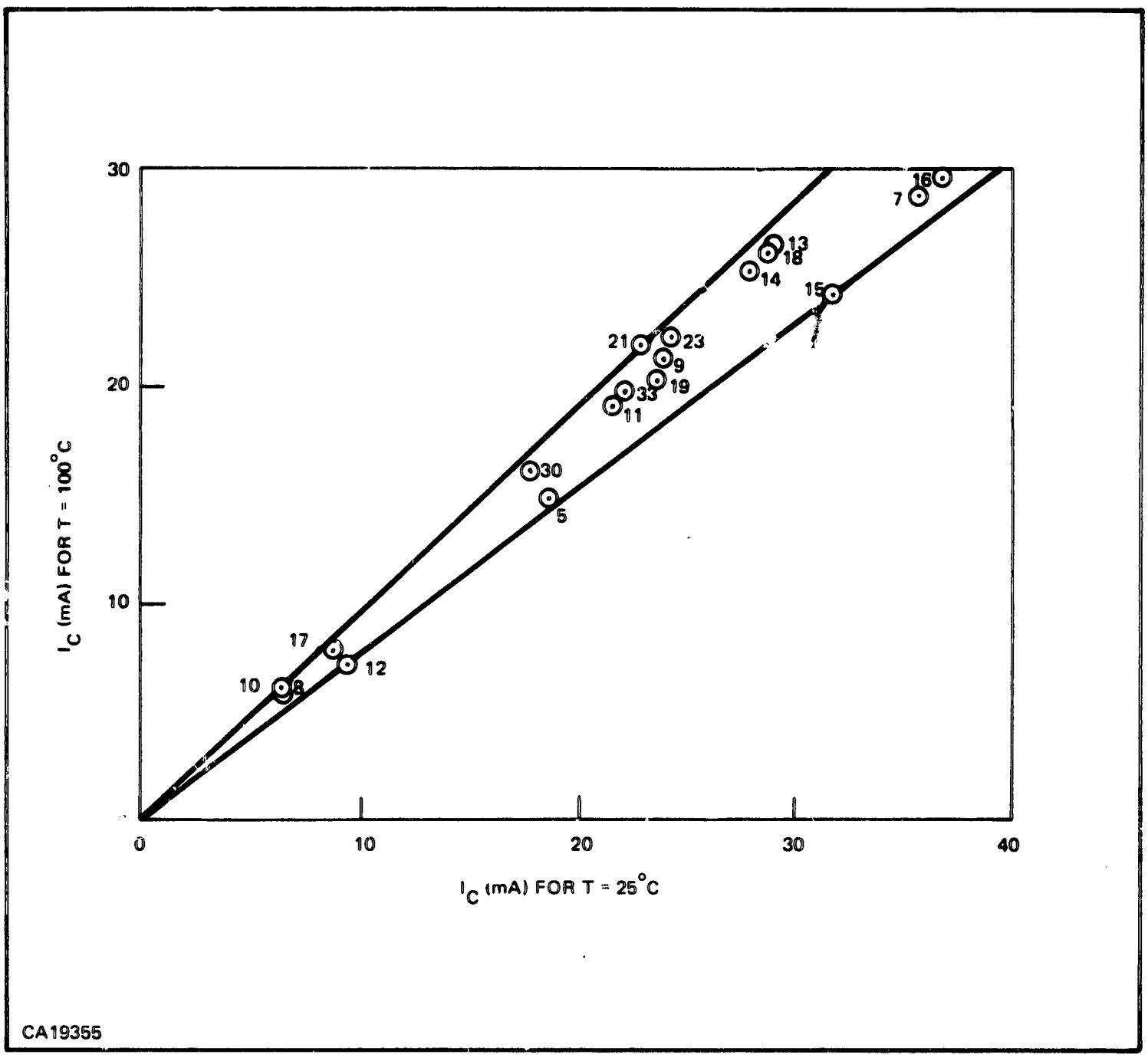


Figure 17. Phototransistor Collector Current, I_C, at 25°C and 100°C for GaAs Diode Current I_F = 22 mA, V_{CE} = 1 V

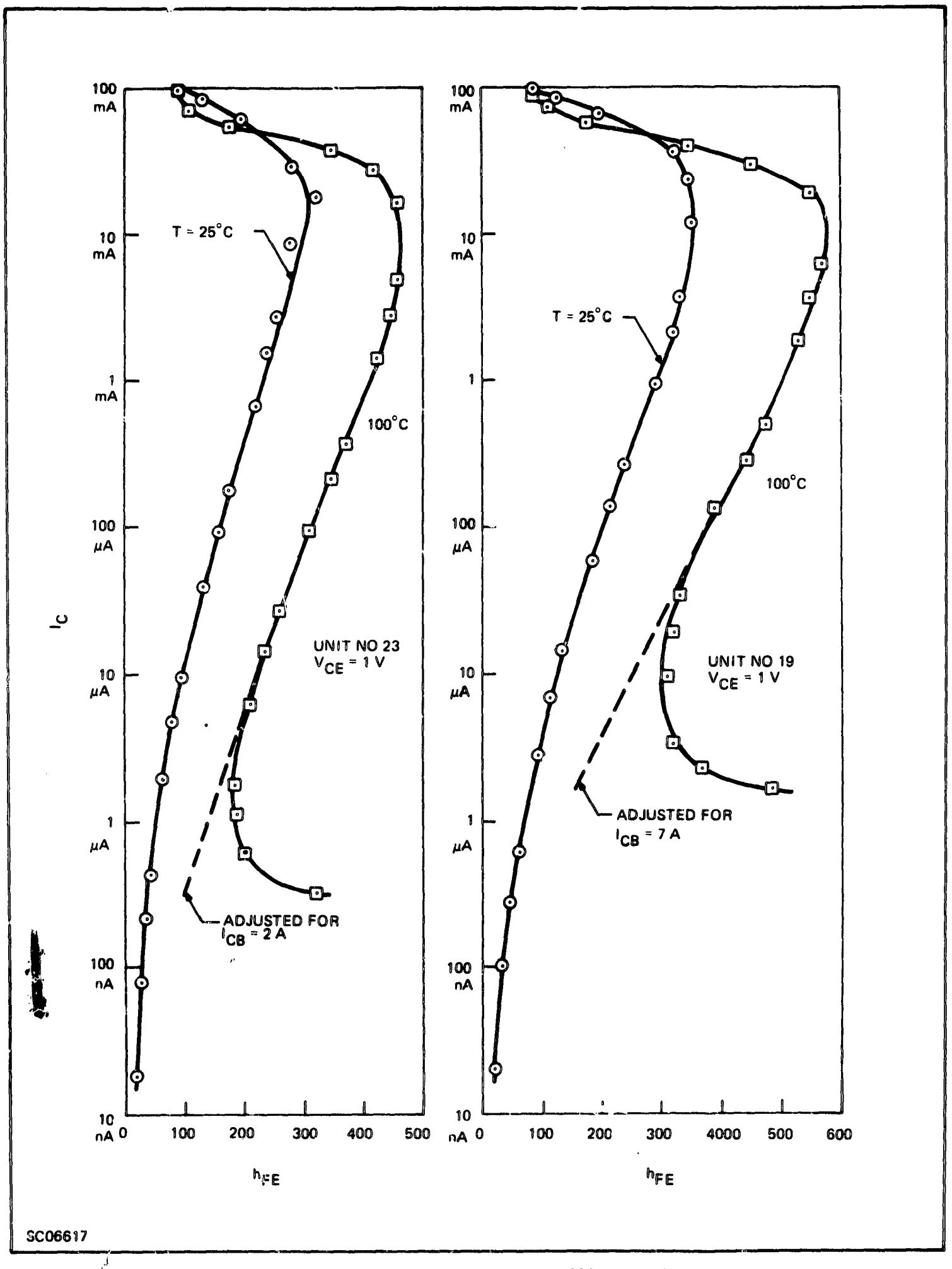


Figure 18. Current Gain Characteristics of Phototransistors

0.85÷1.5 = 0.57, is the ratio of the effective base current at 100°C to that at 25°C. This is close to the nominal value of 1/2 used previously for the effect of temperature on the emitting-diode efficiency. No allowance was made for the change in the detection efficiency of the phototransistor.

Of the 18 devices in Figure 17, 13 have collector currents of over 15 mA at 100°C out of saturation for the worst case biasing of the emitting diode. Four of the other devices were built with transistors having low gains ($200<h_{FE}<400$) to provide additional points for the low current portion of the figure. Thus the 15-mA minimum value appears quite satisfactory for the GaAs switches on the basis of yield.

Final test data for Phase I GaAs switches are shown in Table XVIII. The collector current I_C for the worst-case biasing of the emitting diode at -20, 25, and 100°C is typically well above the 15-mA minimum specification. Values at 100°C range from 16 to 26 mA and, at -20°C, 18 to 45 mA.

c. Leakage Current

For good Si planar small-signal transistors the collector-emitter leakage current I_{CEO} is primarily the collector-base leakage I_{CBO} times the current gain at that current level. For state-of-the-art transistors having a collector resistivity of nominally 6 Ω-cm (at 25°C) and a base area approximately that described, I_{CBO} generally ranges from 1 to 50 nA at 100°C (worst-case temperature). Life test data with high-temperature storage, high-humidity storage, and full-power operating tests over several thousand hours indicate for most of the state-of-the-art transistors that any increase in I_{CBO} is less than a factor of 2. In a few cases the increase is by as much as a factor of 4. Again, the current gain at the leakage level could be less than the value at high current ($450\leqslant h_{FE}\leqslant 900$ at 100°C). Choosing an initial measurement specification $I_{CEO}\leqslant 10\mu A$ would allow, for I_{CBO} = 50 nA, $h_{FE}\leqslant 200$ at this current level. This gain is probably somewhat low; thus only units having lower I_{CBO} would be acceptable.

As mentioned previously, a major problem was experienced with the leakage-current characteristics of transistors made with the initial transistor layout. An unstable collector-emitter leakage characteristic was found which was associated with the coupling glass, high temperature and bias. This effect was only demonstrated by transistors having the GaAs emitter diode and coupling glass. This also was independent of the epoxy. This leakage effect was initially observed as follows: typically, if a collector-to-emitter bias current of 100 μA was applied for a few minutes in a 100°C ambient, the voltage drop of the unit slowly decreased from about 50 volts to about 20 volts. The time required for the total change varied greatly, and some units did not demonstrate the effect until after a few temperature cyclings. Both Ge-P-Se and Se-S-As coupling glasses were used with the same results.

Table XVIII. Data for Phase I GaAs Switches

Parameter	V_{CES}			I_C			I_{CEO}		BV_{CEO}		C_{iso}	t_1	t_2	V_{n1}	V_{n2}
Units	V			mA			μA		V		pF	μs	μs	V	V
Conditions	I_F = W.C.* I_C = 10 mA			I_F = W.C.* V_{CE} = 0.6 V			V_{CE} = 20 V		I_C = 100 μA		f = 1 kHz	—	—	v_i = 5 V	v_i = −5 V
T_A(°C)	−20°C	25°C	100°C	−20°C	25°C	100°C	25°C	100°C	25°C	100°C	25°C	25°C	25°C	25°C	25°C
Device No.	With No Epoxy														
5	0.09	0.16	0.18	40	35	25	0.0012	4.1	71	66	2.3	3.1	59	1.7	1.6
8	0.11	0.13	0.20	35	32	22	0.00013	1.5	75	72	2.1	3.5	52	1.8	1.5
10	0.08	0 11	0.16	42	37	26	0.9014	5.6	64	61	2.8	3.6	20	1.8	1.5
12	0.10	0.12	0.18	34	32	24	0.0009	3.1	64	60	2.3	3.6	56	1.7	1.6
13	0.08	0.10	0.16	45	39	28	0.0005	2.4	70	66	2.0	2.7	64	1.8	1.6
14	0.10	0.12	0.17	40	36	26	0.0038	8.4	61	55	2.3	3.1	68	1.7	1.6
29	0.09	0.11	0.16	39	37	26	0.0005	2.4	65	62	2.5	2.7	56	1.7	1.6
31	0.09	0.11	0.16	38	37	26	0.0002	2.4	55	53	2.3	2.9	63	1.7	1.6
32	0.10	0.12	0.17	35	35	25	0.0011	4.4	84	68	1.8	2.5	49	1.8	1.7
34	0.10	0.14	0.17	34	25	25	0.0003	2.8	77	69	2.0	3.3	46	1.8	1.7
	With Epoxy														
18	0.11	0.14	0.20	32	31	23	0.0013	3.4	78	67	3.0	2.7	29	1.7	1.6
19	0.09	0.11	0.17	37	35	25	0.0006	4.8	57	54	2.0	3.0	62	1.7	1.6
21	0.09	0.11	0.17	39	36	26	0.0005	6.2	60	57	2.3	2.9	70	1.7	1.5
22	0.09	0.11	0.16	39	36	26	0.0002	1.7	64	61	2.6	2.9	52	1.7	1.6
23	0.09	0.12	0.17	37	34	25	0.0001	0.07	65	63	1.8	2.8	54	1.7	1.6
24	0.09	0.11	0.16	42	37	26	0.0009	3.6	54	52	1.9	2.8	74	1.7	1.6
25	0.09	0.11	0.17	41	37	25	0.0013	4.7	58	55	2.1	2.7	62	1.7	1.5
39	0.10	0.12	0.18	32	32	24	0.0039	10.6	64	59	3.4	5.1	56	1.7	1.5
41	0.11	0.14	0.20	29	29	22	0.0050	10.0	71	62	6.4	4.0	33	1.6	1.4
46	0.14	0.16	0.24	18	20	16	0.0051	12.2	85	66	2.0	6.6	30	1.9	1.7

* Worst Case Values: T_A = −20°C 25°C 100°C
I_F = 24.5 mA 24 mA 22 mA

In ordinary applications the design of the transistor should have been addquate; tests indicated no instability for the discrete transistor at 100°C. For the GaAs switch (the coupled pair), characterizations of the leakage effect were made to evaluate its cause. During the leakage tests above, no external potential was applied to the GaAs diodes and therefore there was no applied potential across the glass bond. It was suspected that the leakage effects were due to inversion layers on the surface of the transistor which were related to the characteristics of the coupling glass. The effects of changing the field on the glass, by varying the potential between the GaAs and Si wafers, were studied. The following results for a representative GaAs switch were typical:

In Figure 19, the collector-emitter breakdown voltage for the phototransistor at 100°C is given as a function of V_G, the voltage across the coupling glass. Sufficient time (1 to 10 minutes) was

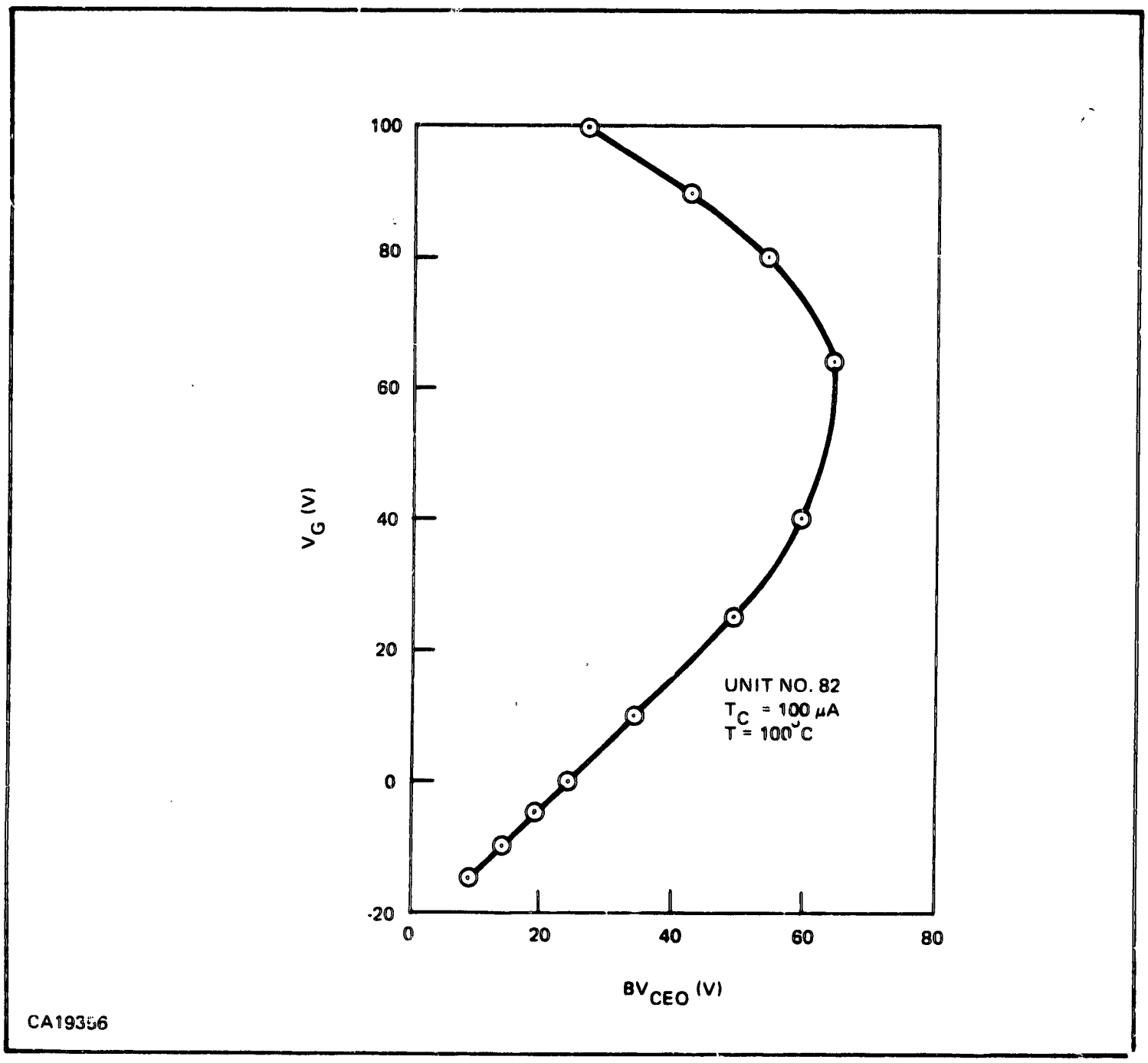


Figure 19. Collector-Emitter Breakdown Voltage versus V_G

allowed for each value to stabilize. A pronounced effect is evident. From these results it can be deduced that, with no connection to the GaAs wafer, the potential on the wafer initially follows that on the collector (since this covers most of the area under the GaAs diode), so that the breakdown voltage is initially high. As the potential on the GaAs wafer slowly drops due to package leakage paths, the breakdown voltage falls (as shown in Figure 19).

The leakage currents for the collector-base junction I_{CBO}, for the collector-emitter junction with open base I_{CEO}, and for the collector-emitter junction with base and emitter shorted I_{CES} are given as a function of V_G in Figures 20 and 21. Transistor supply voltages of 3 and 35 volts respectively are used. In both figures, for $V_G \approx 30$ V, $I_{CEO} \approx h_{FE} I_{CBO}$ and $I_{CES} \approx I_{CBO}$, as expected. For $V_G > 50$ V, V_G has only a small effect on I_{CBO}, but both I_{CEO} and I_{CES} experience rapid increases. The value of V_G for which this occurs is not dependent on the transistor supply voltage V_C. This is characteristic of an inversion layer which bridges the base, supplying a conductive path between collector and emitter.

Also in both cases, for $V_G < V_C - 20$ V all three currents increase greatly. In this region $I_{CEO} \approx h_{FE} I_{CBO}$ and $I_{CES} \approx I_{CBO}$. This indicates a leakage of the collector-base junction due to an inversion layer across the collector.

To eliminate the inversion layers, a redesign of the phototransistor was required. Diffusion outlines for the new design were shown in Figure 14; and the metallization pattern, in Figure 15. Remedies employed to eliminate the leakage effects include the addition of an N^+ diffusion (guardring) surrounding the base as shown in Figure 14, and a contact to the ring which completely covers the collector-base junction over the oxide field-relief electrode in Figure 15. These modifications prevent contact to the base of a collector inversion layer. The base surface concentration was also increased to reduce the probability of formation of an inversion layer on the base.

Initial testing, to determine whether these modifications were sufficient to eliminate the effects of the inversion layers on the leakage characteristics, was conducted on standard, commercially available Si transistors. The Texas Instruments type 2N2484 Si transistor is fabricated with surface-passivation techniques similar to those above. Three of the 2N2484 transistors were fabricated with standard ball-bond connections, and GaAs emitting diodes were then bonded to the transistors using a Se-S-As coupling glass. These transistors are much smaller than the phototransistor. To prevent shorting of the GaAs wafer to the ball-bonded leads on the Si wafer, a glass thickness of about 3 mils was used, compared to the thickness 1 to 2 mils used for the phototransistor. Testing conditions were the same as those used for studying the leakage characteristics of the phototransistor: 0 to 100 V applied between the GaAs and Si wafers, a collector-emitter voltage between 3 and 35 V, and an ambient temperature of 100°C. Collector-emitter leakage currents I_{CEO} were the same as before the GaAs diodes were mounted. This indicated that inversion-free leakage characteristics should also be obtained with the modified design of the phototransistor.

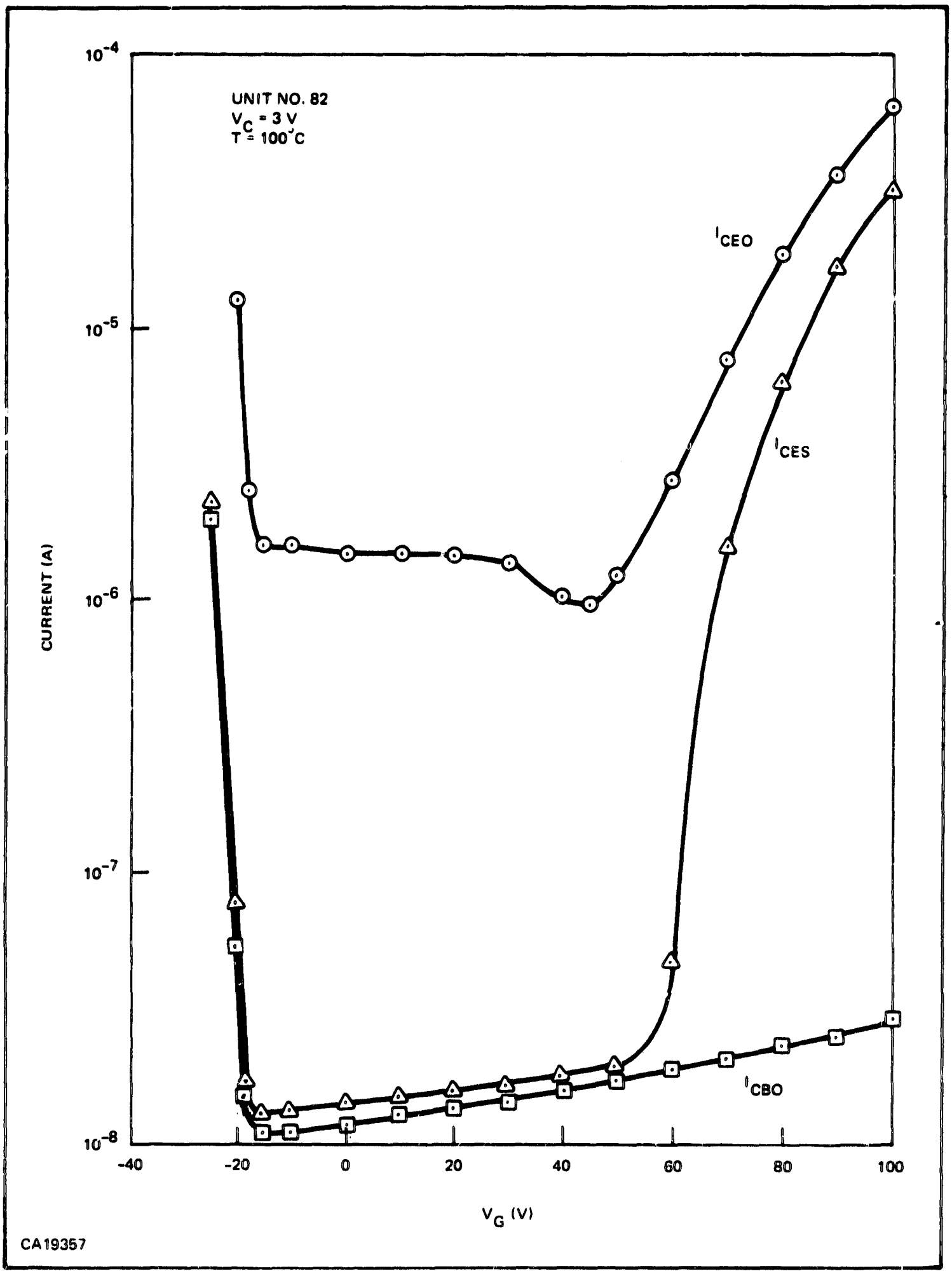


Figure 20. Transistor Leakage Currents versus V_G (V_C = 3 Volts)

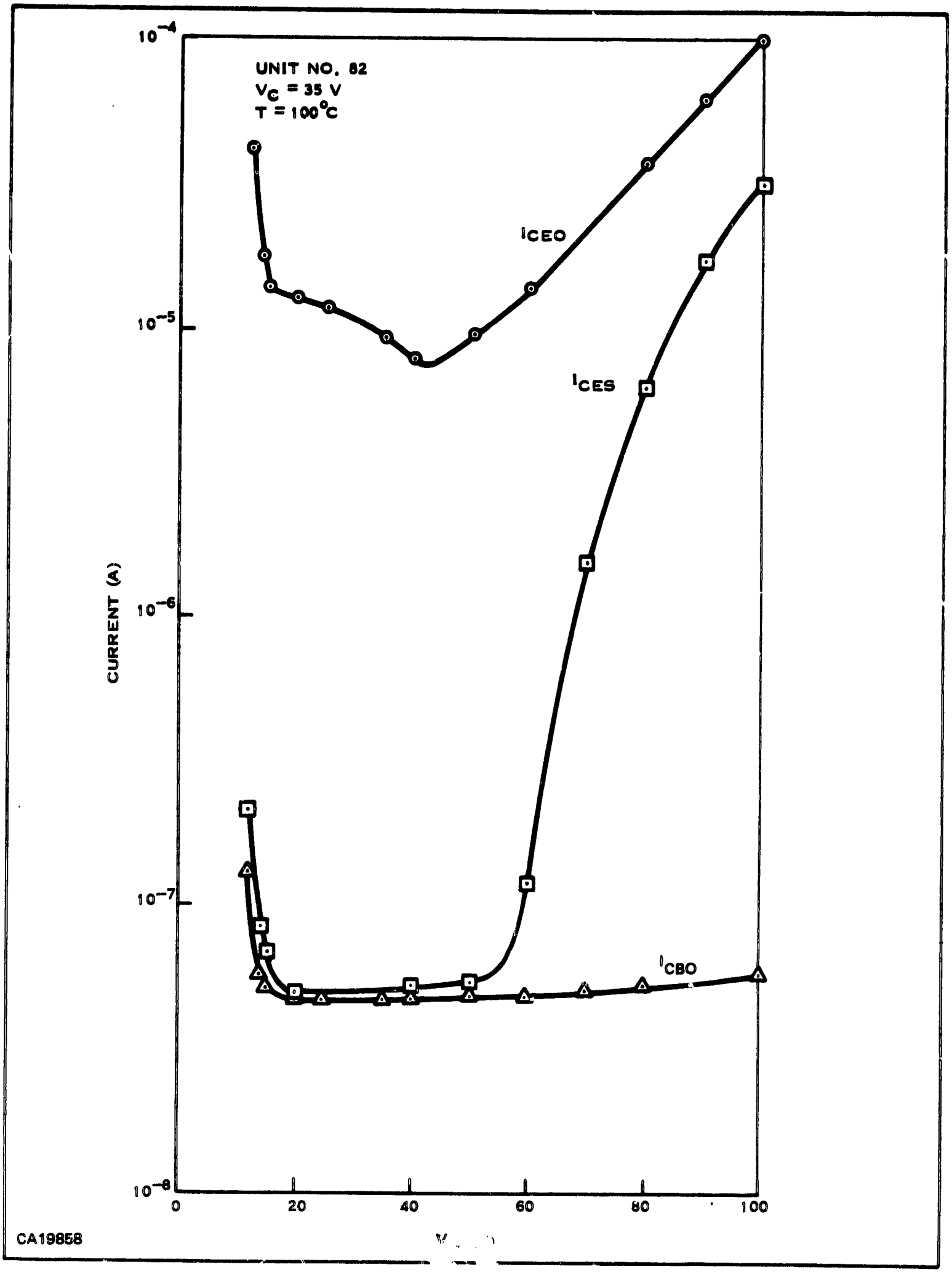


Figure 21. Transistor Leakage Currents as a Function of V_G (V_C = 35 Volts)

Diffusion masks for the new phototransistor were then developed and new transistors processed. Leakage tests, as described above, were made for the new phototransistor. Low-valued leakage currents were obtained, without the instabilities demonstrated previously with inversion layers.

Distributions of I_{CEO} at 20 V and 100°C are shown in Figure 22. These include results for two batches of phototransistors having the original geometry, type A, and for four batches having the new geometry, type B. Each device had an I_{CEO} within the incremental current range indicated. Prior to these leakage measurements, devices were screened on the slice for a collector-emitter breakdown voltage greater than 40 V, and, after separation of the transistor dice, the transistors were sorted for common-emitter forward current gain, h_{FE}. There was no prior test for leakage. For the tests, type A devices did not have GaAs diodes mounted, since this results in the inversion layers at higher temperatures.

The effect of supply voltage on I_{CEO} and collector-base leakage, I_{CBO}, at 100°C is shown in Figure 23 for representative types A and B devices. For the type A devices shown, h_{FE} ranged between 400 and 500, as measured at V_{CE} =1 V, I_B = 0.1 mA, and T = 25°C. For the type B devices, h_{FE} ranged between 300 and 400. A study of the results in Figure 23 indicates that I_{CEO} at the specified bias of 20 V is largely independent of h_{FE} as defined above. Rather, I_{CEO} depends on I_{CBO} and the particular influence of supply voltage. As discussed previously for state-of-the-art silicon small-signal planar transistors, I_{CBO} leakage typically ranges between 1 to 50 nA at 100°C. This closely agrees with the results obtained for the phototransistors, as shown in Figure 23. In the Phase I data in Table XVIII, the I_{CEO} of almost all devices can be noted to be less than 10 μA. The maximum value of 12.2 μA is well below the 20-μA value specified.

d. Breakdown Voltage

For a high current gain transistor the effect of current gain on the collector-base breakdown voltage must be considered. A useful design expression[7,8] for an NPN Si transistor is

$$BV_{CBO} = BV_{CEO} (h_{FE})^{\frac{1}{4}} \qquad (18)$$

where

BV_{CBO} is the collector-base breakdown voltage

BV_{CEO} is the collector-emitter breakdown with the base open-circuited

In this case, BV_{CEO} refers to the bulk breakdown, not necessarily to the measured terminal value, which might be limited by surface effects. Using this expression and data from J. Shields[9], the graph in Figure 24 of current gain as a function of collector impurity concentration, for several values of BV_{CEO}, was obtained. The shaded region corresponds to a collector resistivity range at 25°C of 6±2 ohm-cm (concentration of 6.5×10^{14} cm^{-3} to 1.3×10^{15} cm^{-3}) and gain ranging

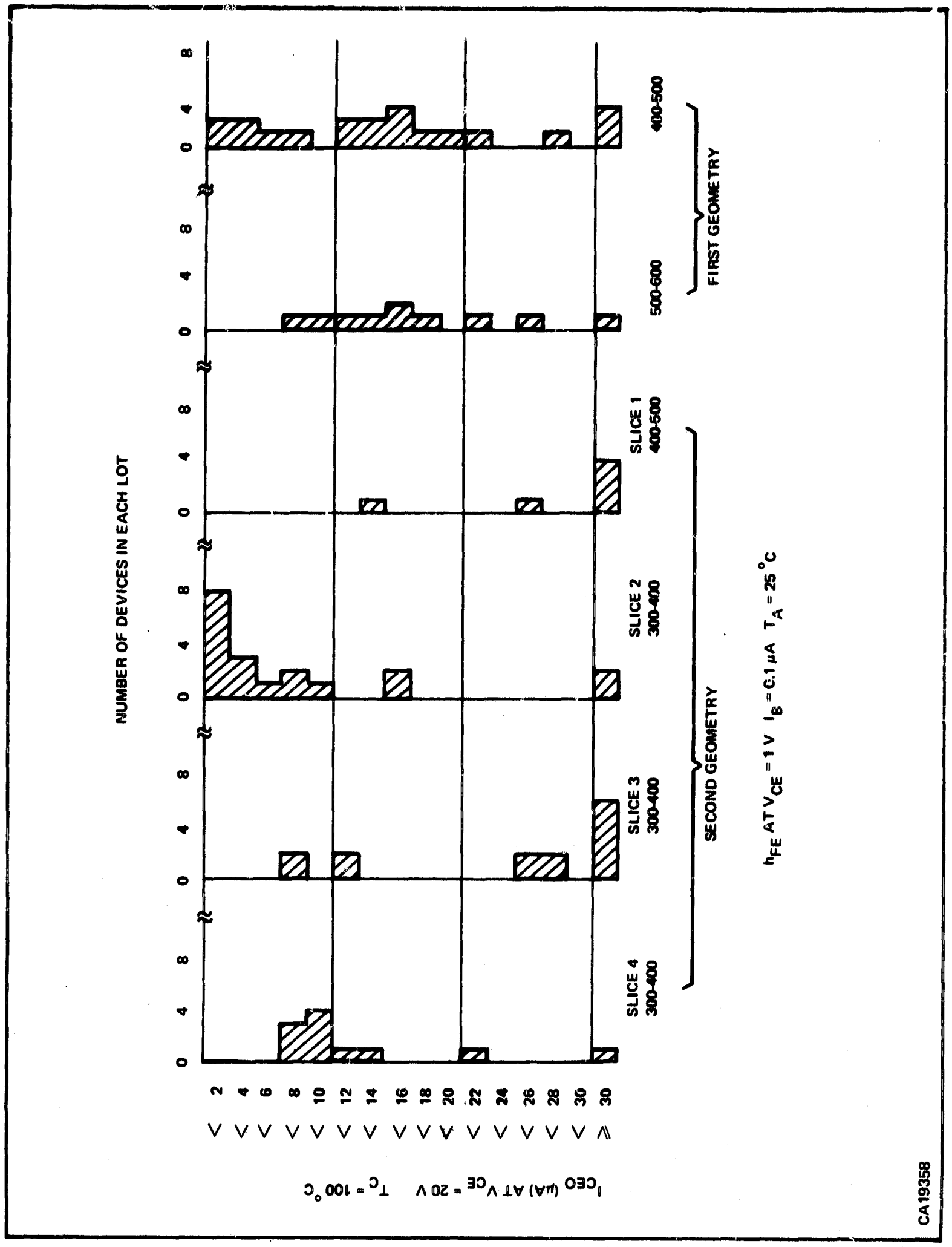


Figure 22. Distribution of I_{CEO} for Phototransistor

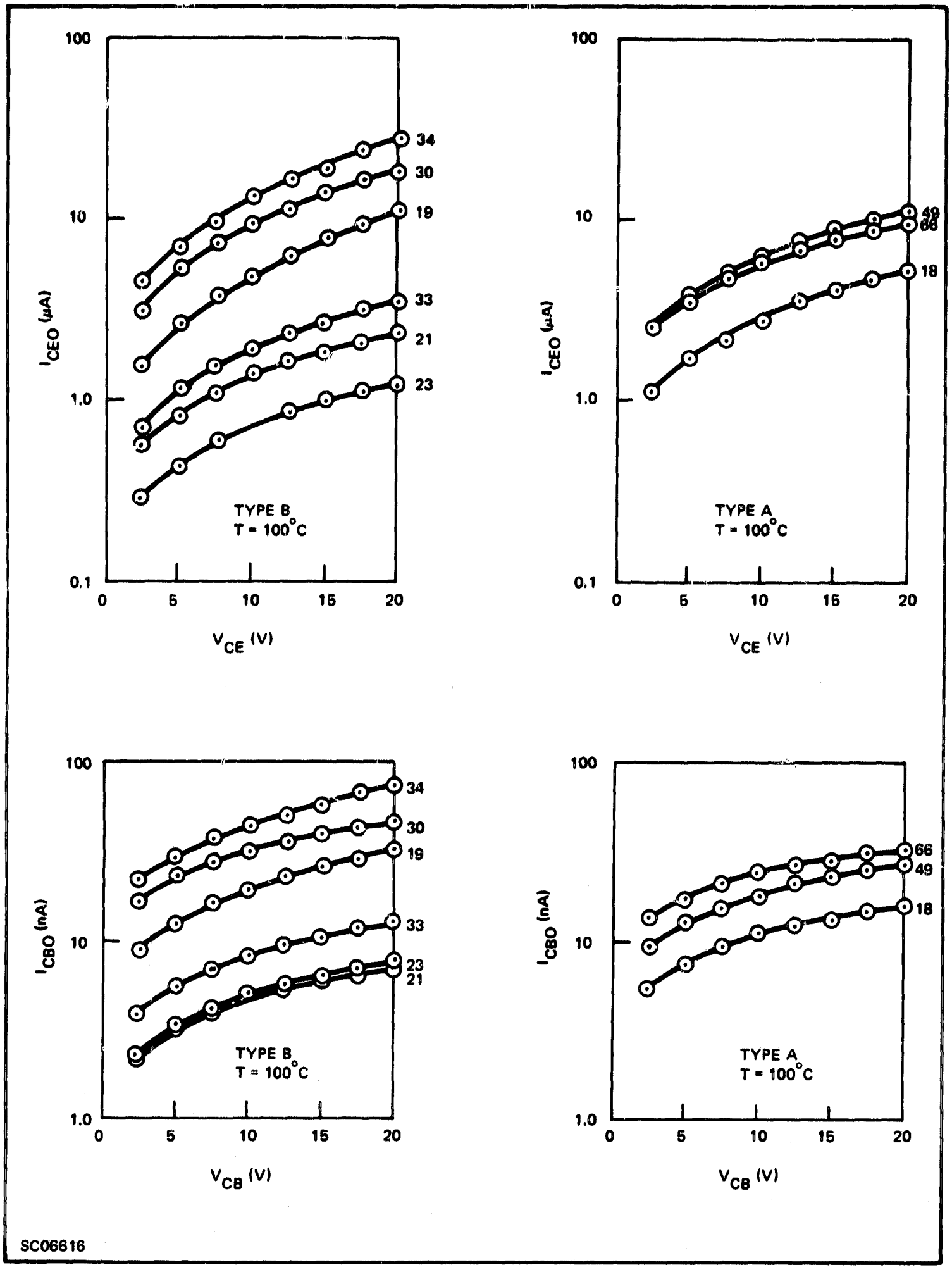


Figure 23. Leakage Characteristics of New (B) and Original (A) Geometry Phototransistors

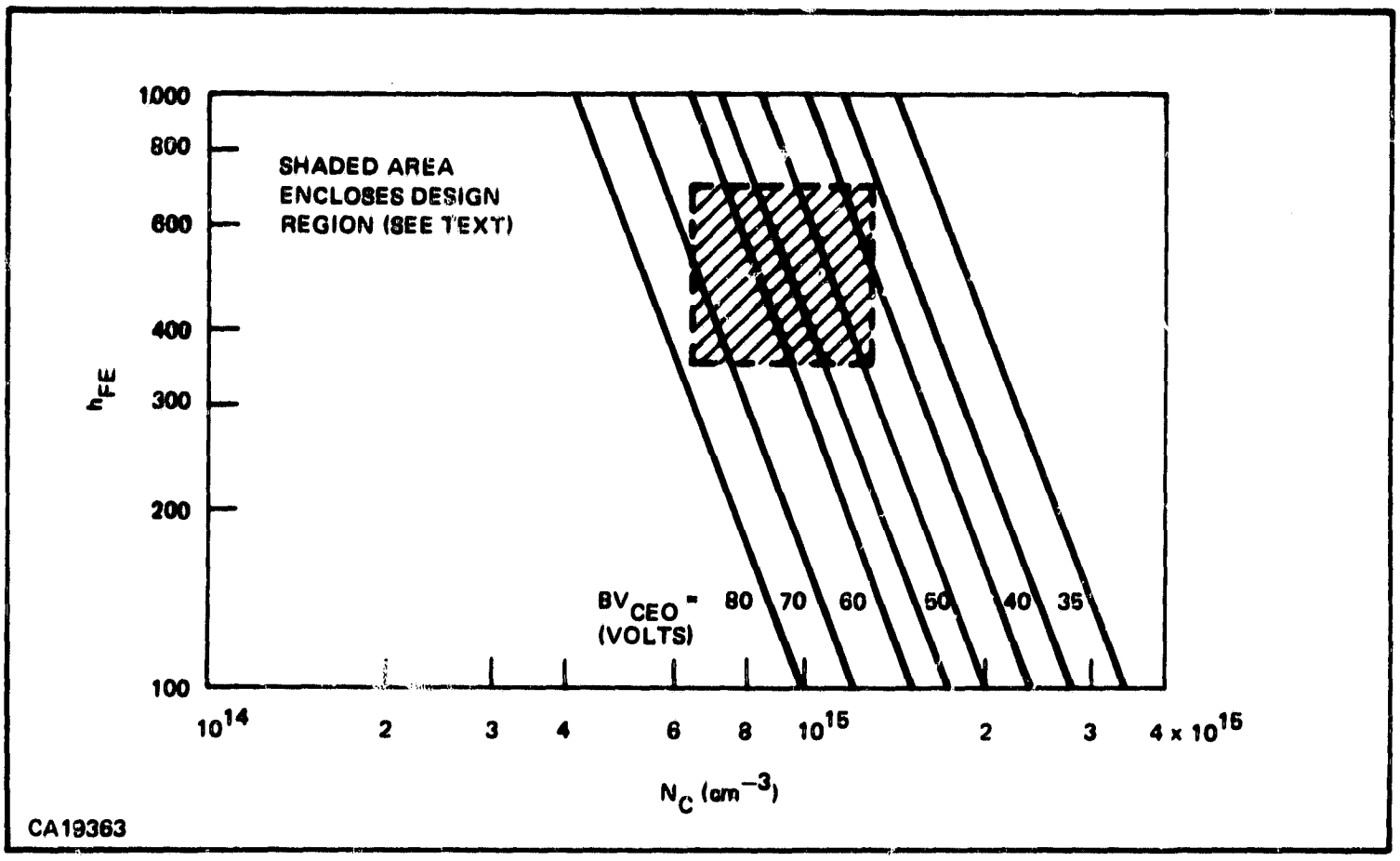


Figure 24. Phototransistor Current Gain as a Function of Collector Impurity Concentration and Collector-Emitter Breakdown Voltage

between 350 and 700. This resistivity is practical from consideration of material tolerance specifications and also of the effect on the several device parameters. The breakdown voltage at 100°C should be slightly less than at 25°C, as gain increases with increasing temperature. It is reasonable that the current gain should be less for the collector current of 100 μA specified at breakdown than at the 10-μA level. Thus, the breakdown voltage was expected to be considerably greater than the 35-V minimum.

As indicated by the Phase I results in Table XVIII, the breakdown results were highly favorable, ranging from 52 to 72 V compared to the 35 V minimum specification.

e. Collector Saturation Voltage

With the isolation switch in the "1" condition, the phototransistor is to be in saturation. The design specification limits the collector-emitter saturation voltage to a maximum of 0.6 V for a collector current of 10 mA. The equivalent collector series resistance R_{CS} for the saturation case, as derived on the basis of the Ebers and Moll[10] small-signal analysis of junction transistors, and including the bulk and contact resistances, can be expressed as

$$R_{CS} = \frac{kT}{q\, I_B} \left[\frac{1}{1 + h_{FE} + \frac{I_E}{I_B}} + \frac{1}{h_{IE} + \frac{I_E}{I_B}} \right] + R_C \qquad (19)$$

where

k = Boltzmann's constant

T = absolute temperature

q = electron charge

h_{IE} = common-emitter inverse-current gain

I_E, I_B = emitter and base currents respectively

R_C = collector region series resistance

As discussed previously, for the current requirements in saturation

$$I_B \geq 1.2 \frac{I_C}{h_{FE}} \tag{20}$$

Thus

$$\frac{I_E}{I_B} = \frac{I_C + I_B}{I_B} < \frac{h_{FE}}{1.2} + 1 \tag{21}$$

At 25°C,

$$\frac{kT}{q} \approx 0.026 \text{ V}$$

Also, $h_{FE} \geq 350$, as previously described. Thus,

$$\frac{I_E}{I_B} \leq 293,$$

and a conservatively low minimum value is 50. It is reasonable that h_{IE} could be very small, so that

$$\frac{I_E}{I_B} \approx 50 \gg h_{IE}$$

A conservative assumption includes a negligible h_{IE}, for which the maximum indicated value for the series resistance at 25°C is

$$R_{CS} < 0.026V \left(\frac{50}{10\ mA}\right) \left(\frac{1}{401} + \frac{1}{50}\right) + R_C \qquad (22)$$

$$R_{CS} < 2.9\ \Omega + R_C \qquad (23)$$

The bulk-resistance portion of R_C is that contributed by the high-resistivity collector region under the emitter. Neglecting spreading resistance effects, the bulk resistance R'_C is given by

$$R'_C = \frac{\rho_C\ t_C}{A_E} \qquad (24)$$

where

ρ_C = collector resistivity

t_C = collector material thickness

A_E = emitter area

As described, the phototransistor design utilizes a 10-mil-diameter emitter with an 0.7-mil maximum collector thickness under the emitter. For the maximum ρ_C = 16 Ω-cm at 100°C the resistivity is approximately double the 25°C value for the antimony-doped epitaxial material.[11]

$$R'_C = \frac{16\ \Omega\ cm\ (0.7\ mil)}{\pi\ (5\ mil)^2\ (2.54 \times 10^{-3}\ cm/mil)} = 56.1\ \Omega \qquad (25)$$

Resistance contributions by the contacts and other regions total less than one ohm. Thus R_{CS}<60 Ω. For the collector-emitter saturation voltage,

$$V_{CE(SAT)} = I_C\ R_{CS} < 10\ mA\ (60\ \Omega) \qquad (26)$$

$$V_{CE(SAT)} < 0.6\ V$$

Conductivity modulation effects[12], which result in lower saturation voltages for transistors having a thick, high-resistivity collector region were, conservatively, not accounted for in this analysis.

Data for saturation voltage in Table XVIII were well below the 0.6 V maximum specified. Worst-case maximum values were obtained at 100°C as expected. For the worst-case minimum bias to the GaAs diode of 22 mA at 100°C, $V_{CE(SAT)}$ ranged from 0.16 to 0.24 V. These small values indicate the possibility of benefit from conductivity modulation effects.

f. Noise Transmissibility

In the off-condition, one requirement for the isolation switch is an insensitivity of the voltage at the collector of the phototransistor to noise pulses at the emitter. In order to establish an appropriate equivalent circuit for the phototransistor under these conditions, the collector transient voltages of a number of transistors were measured, using the circuit in Figure 25.

If no transistor action were involved, the expected transistor equivalent circuit would consist simply of the collector-base and emitter-base P-N junction capacitances (C_{CB} and C_{EB} respectively). Table XIX lists the measured C_{CB} (at 20 V reverse bias), C_{EB} (at zero bias), and h_{FE}

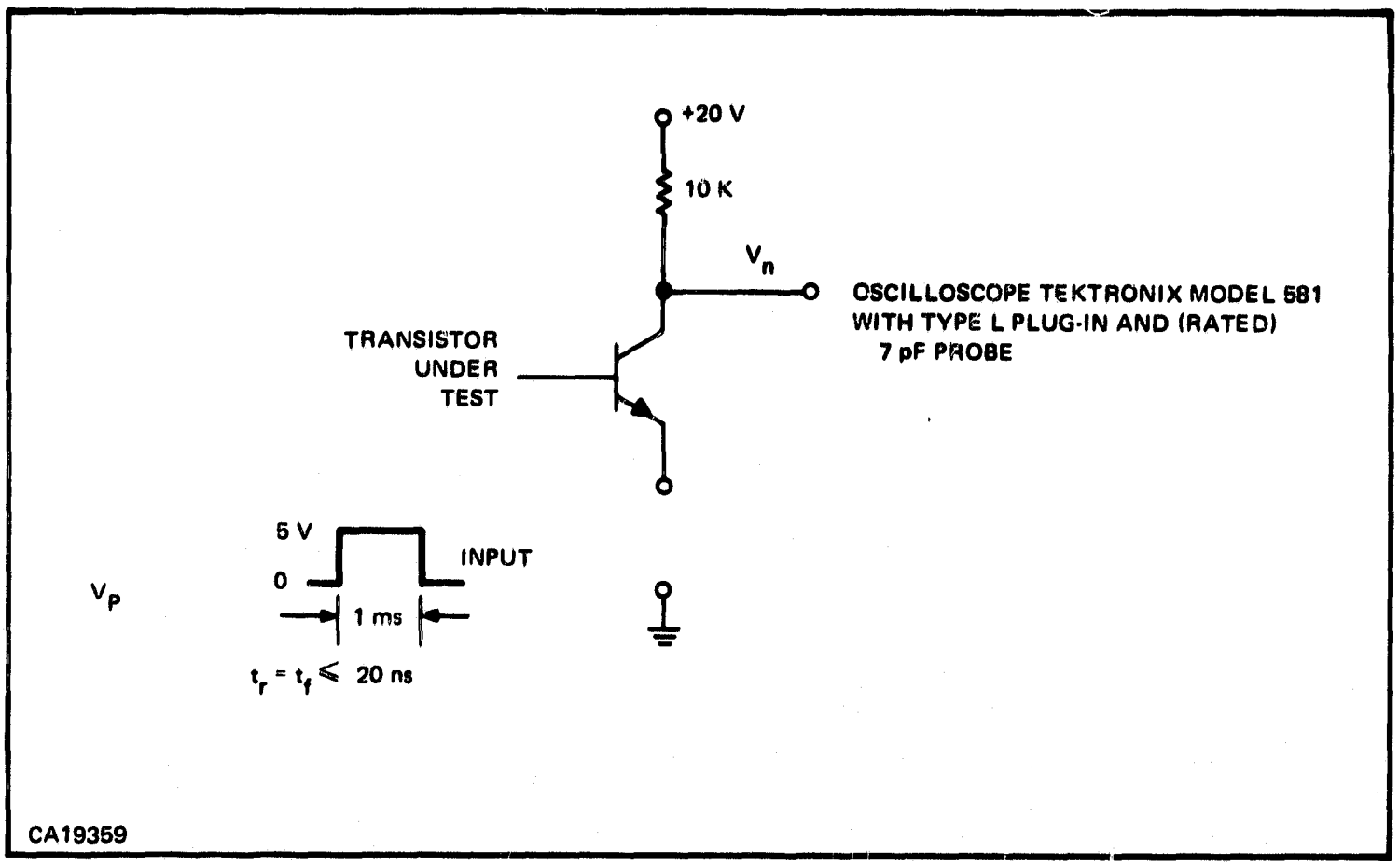


Figure 25. Circuit for Measuring Noise Transmissibility

Table XIX. Data for Noise Transmissibility Study

Transistor	V = 0 CEB (pF)	V = 20 V C_{CB} (pF)	I_C = 10 mA V_{CE} = 5 V H_{FE}	Meas V_n (V)	Calc V_n (V)
2N656(1)	125.0	28.0	26	2.8	3.0
2N656(2)	94.0	35.0	18	3.0	3.2
2N1507(1)	64.2	12.5	116	2.2	2.2
2N1507(2)	62.0	14.5	167	2.2	2.3
2N1507(3)	53.7	12.1	238	2.1	2.1
2N1711	62.1	12.8	141	2.15	2.2
2N3420(1)	860.0	92.0	47	4.2	4.2
2N3420(2)	886.0	87.5	46	4.2	4.2
PCT No. 13	7.2	8.0	308	1.2	1.2
OPEN				0.33	
10 pF				2.0	

(at I_C = 10 mA, V_{CE} = 5 V) for several transistors. Also indicated are the measured collector peak transient voltages, V_n. Practically identical values of V_n were obtained for positive and negative pulses at the emitter. The values for positive pulses were slightly greater, due to a greater net C_{CB} for the reduced average collector-base voltage, and these values are given in Table XIX.

Measured V_n for an open-jig and for a 10 pF capacitor inserted between the collector and emitter terminals of the jig are also indicated in Table XIX. The latter were used in determining the jig parasitic capacitances. The equivalent circuit used in calculating V_n is shown in Figure 26. In the figure, C_1 is a jig capacitance and C_2 combines jig shunt capacitance and oscilloscope probe capacitance. These are given by the simultaneous equations

$$v_{n(o)} = v_p\left(\frac{C_1}{C_1 + C_2}\right) \tag{27}$$

$$v_n(10\ pF) = v_p\left(\frac{C_1 + 10\ pF}{C_1 + C_2 + 10\ pF}\right) \qquad (28)$$

where

$v_{n(o)}$ = the collector peak transient voltage for an open jig socket

$v_{n(10\ pF)}$ = the transient with the 10-pF capacitor in the jig

v_p = the 5-V pulse input

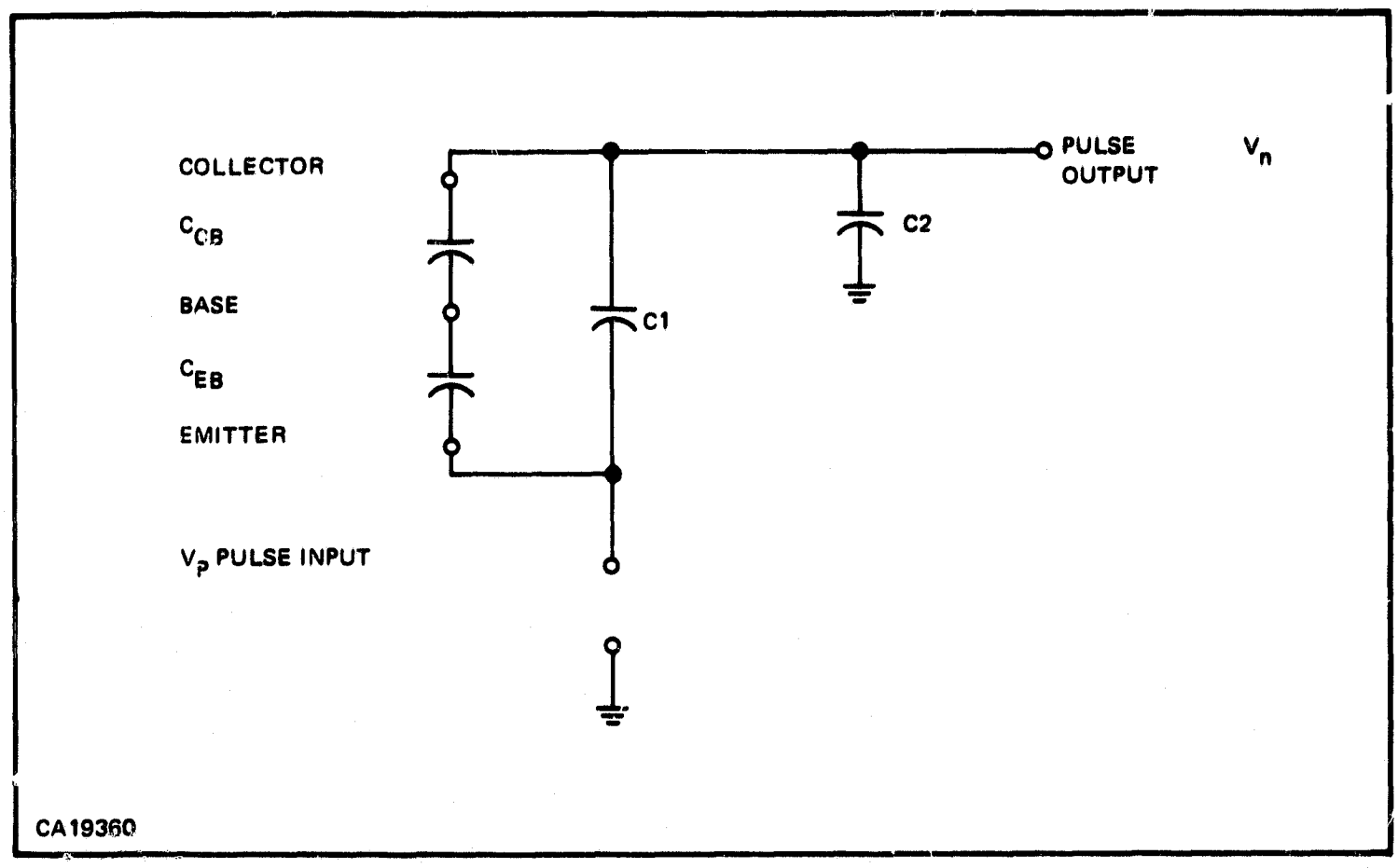


Figure 26. Equivalent Circuit Used in Calculating V_{n}

at the emitter. Using the measured values we obtain, on substitution in Equations (25) and (26), C_1 = 1.2 pF and C_2 = 16.8 pF.

A general formula for calculating the peak transient voltage for a transistor, derived from Figure 26, is

$$V_n = \frac{V_P \left[C_1 \left(C_{CB} + C_{EB} \right) + C_{CB}\, C_{EB} \right]}{\left(C_1 + C_2 \right) \left(C_{CB} + C_{EB} \right) + C_{CB}\, C_{EB}} \qquad (29)$$

Calculated values of V_n for each transistor are given in Table XIX. In Figure 27, measured V_n is plotted against calculated V_n. The good agreement indicates that the equivalent circuit used is adequate; therefore, only the junction and circuit capacitances need be considered in noise transmissibility.

For the GaAs switch, there also is a capacitance between the emitting diode and the phototransistor. A test of the effect of this capacitance was made using PCT No. 13, a high-gain, low-capacitance phototransistor. For this transistor additional capacitances up to 30 pF were connected into the circuit between the transitor base and ground. Effects of transistor action were not observed for either positive or negative pulses. Stray capacitances in the photon-coupled isolation switch to the base should be only about 1 pF, based on measurements on the TIXL106. The effect of the capacitance between the emitting diode and the collector is to reduce the noise transmissibility, as the surface facing the transistor is connected to the ground plane. Because C_2 is small, the capacitance to the GaAs can have considerable effect in reducing V_n.

Calculations of the transistor capacitances can be used to estimate the noise transmitted. As indicated by Equation (29), the worst-case condition is for maximum transistor capacitances. Using a collector potential of 20 volts (for which noise transmissibility is measured), the collector region depletes[13] about 0.17 mil for a collector resistivity (ρ_C) of 4 Ω-cm. The collector-base junction area in Figure 14 is about 700 mils^2. The collector-base junction capacitance $C_{C'B}$ is given by

$$C'_{CB} = \frac{\epsilon_o \epsilon \ (700 \text{ mil}^2)}{0.17 \text{ mil}} = 10.8 \text{ pF} \qquad (30)$$

where

$\epsilon_o \epsilon$ = the permittivity of silicon.

Base capacitance contributed by the expanded collector contact over the base area can be calculated for the approximately 145 mils^2 area, 9000 Å of oxide and typical 230 pF-Å/mil^2. For these values the additional capacitance C''_{CB} = 3.7 pF. Thus the calculated total C_{CB} = 14.5 pF. Measured values averaged 16.4 pF, including package capacitances of a few tenths of a pF.

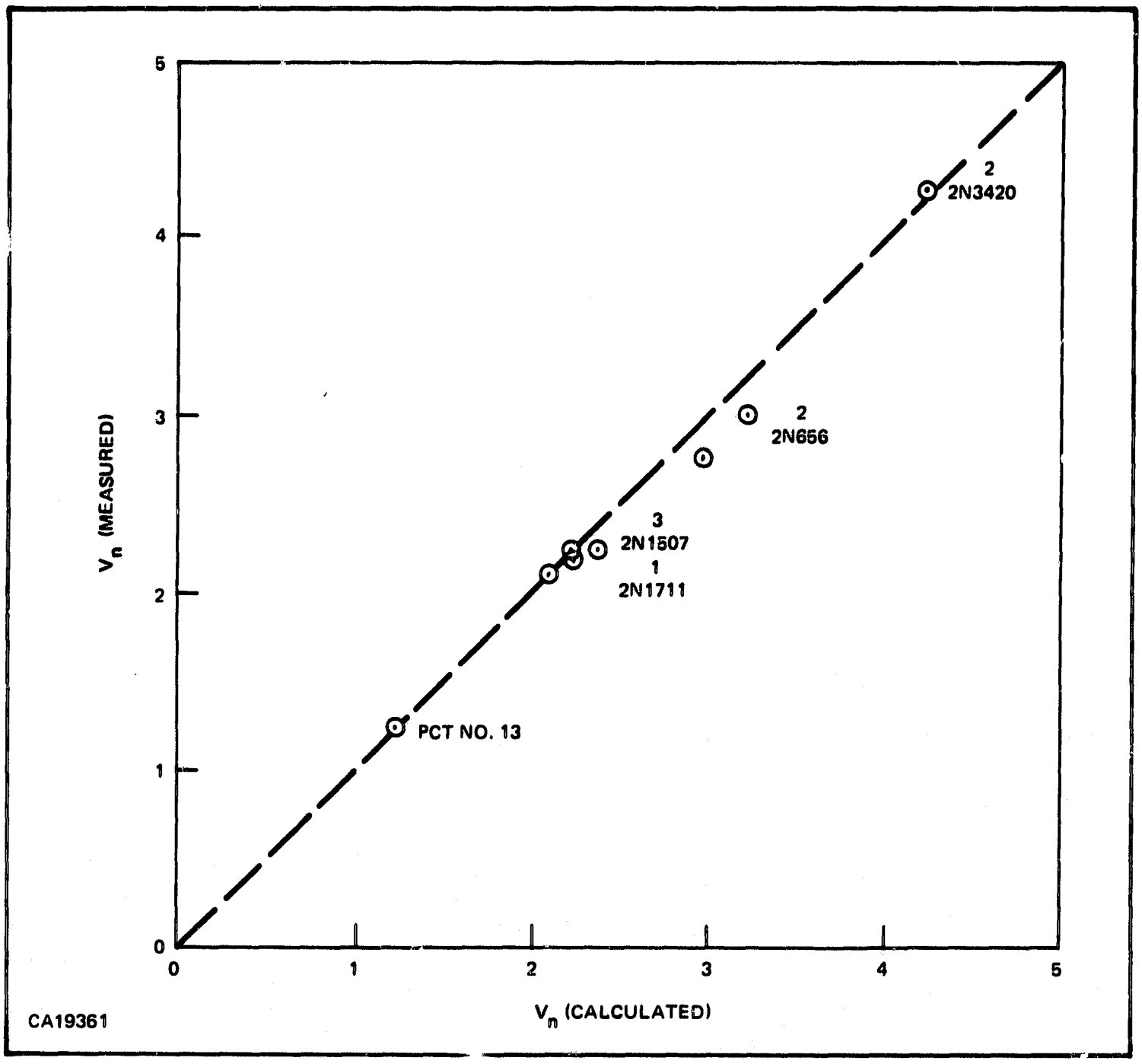


Figure 27. Comparison of Measured and Calculated Noise Transmissibility

The jig made for measuring the noise transmissibility of the flat-packaged Phase I devices had parasitic capacitances different from those of the jig used in the analysis. The changes were required to meet the circuit specifications. The equivalent circuit of this jig is shown in Figure 28. Included in the figure are the component, oscilloscope (CRO), and jig capacitances, as determined from direct capacitance measurements and transmissibility measurements, using known capacitances in place of the phototransistor. For this jig, C_1 = 1.8 pF, and C_2 = 10.7 pF. The 1.8 pF capacitance shunting the collector-emitter terminals tends to increase the noise transmissibility slightly. Because of the complex nature of the parasitic capacitances, no correction was made for this shunt capacitance in the data. This tends to make the data somewhat conservative. Complicating a correction for the shunt capacitance is the capacitance between the GaAs light-emitting diode and the phototransistor. Nominally about 3 pF, this capacitance represents the total coupling to the collector and base areas. Values to each of these areas cannot be separated easily. Because the GaAs diode is grounded in the measurement, both capacitances are shunted to ground. This grounded connection of the GaAs diode simulates the connection of the diode in the driver circuit. The oscilloscope capacitance of 8.4 pF is less than the specified maximum of 10 pF. This capacitance substantially influences the results. The total jig and oscilloscope capacitance shunting the collector to ac ground (which includes the 0.3 pF load resistor capacitance) of 10.7 pF is representative of that with the GaAs switch or isolation switch assembled in a circuit.

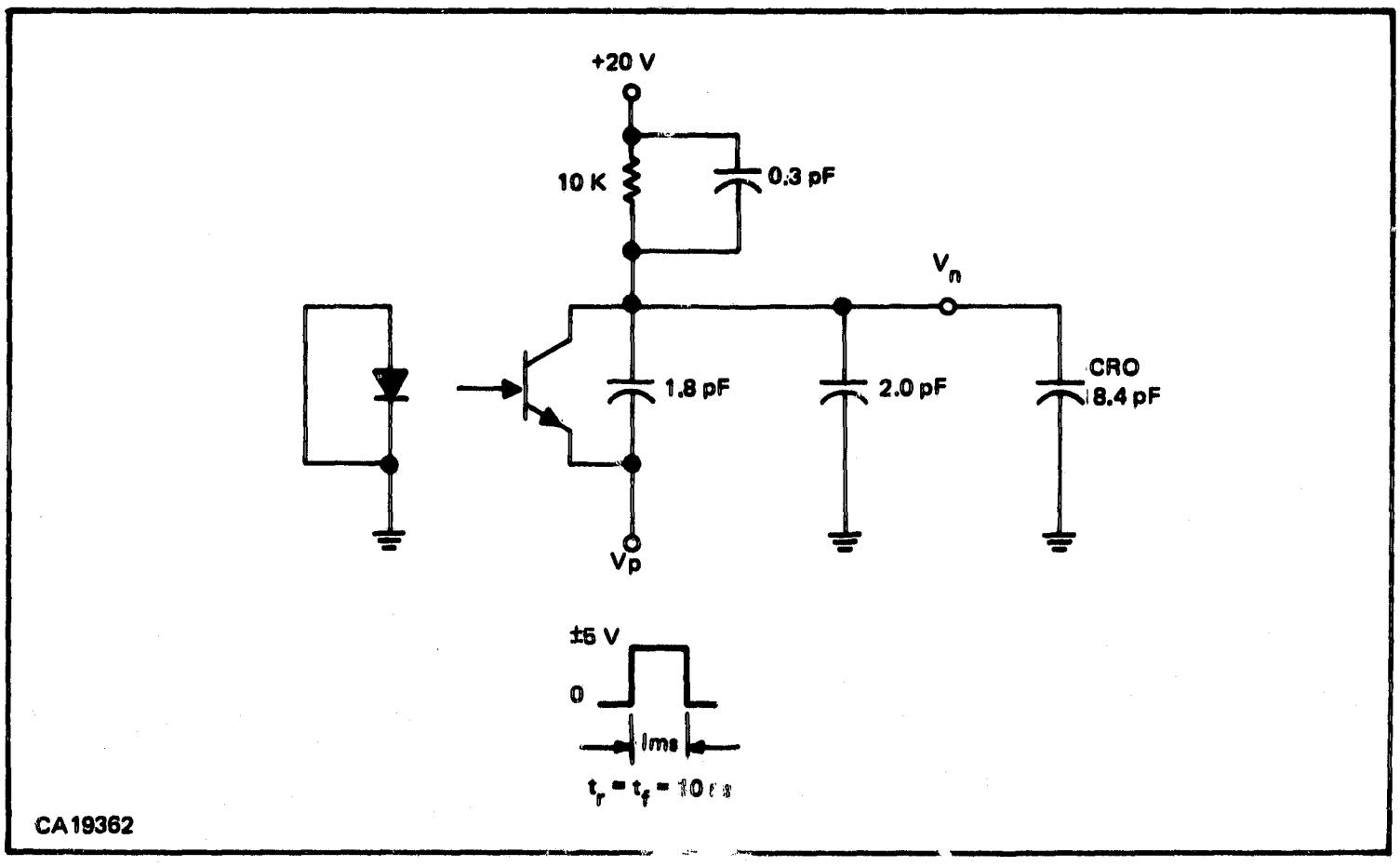


Figure 28. Noise Transmissibility Test Jig with Parasitic Capacitances

A rough design value for C_{EB} is 1/4 pF/mil^2, and, for the 9-mil diameter, the calculated C_{EB} = 16 pF. Coincidentally, the measured C_{EB} = 16.3 pF, typically. For these parasitics and the measured transistor capacitances of C_{CB} = 16.4 pF and C_{EB} = 16.3 pF, in Equation (27), we obtain V_n = 2.4 V, greater than the 2 V maximum specification. However, the capacitance to the GaAs diode results in a reduction. In Table XVIII, V_n ranges from 1.6 to 1.9 V for the Phase I devices for positive input pulses. The calculated and measured values are conservative, since the measuring-jig capacitances tended to increase the values.

Another factor which had to be considered in all the measurements was the effect of the rise time of the input pulse on the measured transient signal at the collector. The time constant of the circuit, composed of the 10 k-Ω load resistor and the capacitances, is not insignificant compared to the rise time of the input pulse, specified to be 10 ns or less. For this reason, highly reproducible results require the use of a single pulse rise time. Reproducibility between two different types of high-speed pulse generators may not be better than 10 percent, with greater transient values being measured with the generator having the faster rise time. An input pulse having a 10 ns rise time was used for the tests.

g. Switching Times

The rise time of the phototransistor can be given approximately by the expression

$$t_R = \frac{0.8\ \overline{C_{CB}}\ (V_{CC})}{I_B} + \frac{\overline{h_{FE}}}{\overline{\omega_T}} \qquad (31)$$

where

$\overline{C_{CB}}$ = the effective collector-base capacitance during the turn-on transient

V_{CC} = the supply voltage

I_B = the equivalent base current

$\overline{h_{FE}}$ = the effective current gain during the transient

$\overline{\omega_T}$ = the effective angular cutoff frequency of the transistor during the transient.

Effective values are given for several parameters, as their values are expected to change considerably during the transient. The expression describes the time required for the base photocurrent to charge C_{CB} so that the change in the voltage across the capacitor is 0.8 V_{CC} (10 to 90 percent points). This is approximately true for large values of V_{CC}. The second factor in the expression allows for the effect of the intrinsic speed limitation of the transistor. An order-of-magnitude value can be calculated for $h_{FE} \approx 500$ and $\omega_T = 2\pi(200\ \text{MHz})$, or about 0.4 μs; small compared to the total rise time of 10μs maximum as specified. An additional factor in total rise time is the delay time. This represents the time required for the photocurrent to increase the emitter-base voltage sufficiently to

produce a high level of collector current. The emitter-base voltage is usually only a few tenths of a volt below this conduction point, due to the collector-base leakage. For the GaAs switch the delay was expected to be only a fraction of a microsecond.

The fall time of the phototransistor can be given approximately by

$$t_F = 2.2\ \overline{h_{FE}'}\ R_L\ \overline{C_{CB}'} + \frac{\overline{h_{FE}'}}{\overline{\omega_T'}} \tag{32}$$

where

R_L = the collector load resistance

$\overline{C_{CB}'}$ = the effective C_{CB} during the turn-off transient.

This expression describes an R-C type (simple exponential) response in which 2.2 R-C time constants are required between the 10 and 90 percent response points. The effective collector capacitance which is discharged through the load resistor is the current gain times the collector-base capacitance. The additional factor in total fall time is the "storage time." As the base overdrive is not excessive, probably less then a factor of three, storage should not be a very considerable portion of the maximum turn-off of 100 μs specified.

Switching-speed characteristics were studied for the breadboarded driver circuit and a GaAs switch (initial transistor structure). The supply voltage and the peak input voltage used were 4.0 V. For the phototransistor (of the original design), a supply voltage of 20 V and a load of 2 kΩ were used. Delay (0 to 10 percent), rise (10 to 90 percent), storage (100 to 90 percent), and fall (90 to 10 percent) times were measured as a function of capacitance added to what will be the common junction of the input diodes. Typically, the input-diode capacitance is about 3 pF, or about 27 pF for 9 diodes having inputs at a constant potential. Measurements were made for capacitances of up to 200 pF.

Figure 29 describes the switching times for the voltage across the final collector resistor, which is approximately that for the current in the GaAs diode. Figure 30 describes the switching times at the collector of the phototransistor. The total rise ($t_D + t_R$) and total fall ($t_S + t_F$) times for the circuit and GaAs switch of 3.6 μs and 39.6 μs respectively at C = 27 pF are well within the maximum specifications of 10 μs and 100 μs.

For the particular peak current in the GaAs diode of 31.7 mA, I_B was measured as 127 μA. The measurement consisted of shorting the collector and emitter leads and determining the short-circuit current between this point and the base lead. The collector-base capacitance at 20 V was measured as 11 pF, but $\overline{C_{CB}}$ is greater due to the fact that the collector voltage varies between 20 V and about 0 V during the switching transient, and capacitance increases with decreasing voltage. Analysis[14] of the effective capacitances for the rise and fall transients, with the assumption of a cube-law C-V relationship, indicates $\overline{C_{CB}} = 1.31\ C_{CB}$, where C_{CB} is the value at 20 V. Thus $\overline{C_{CB}} = 1.31$ (11 pF) = 14.4 pF. Similarly $\overline{C_{CB}'} = 1.55\ C_{CB} = 17$ pF. Calculations of the switching times from the initial terms of Equations (31) and (32) using these values of the effective capacitances, produce

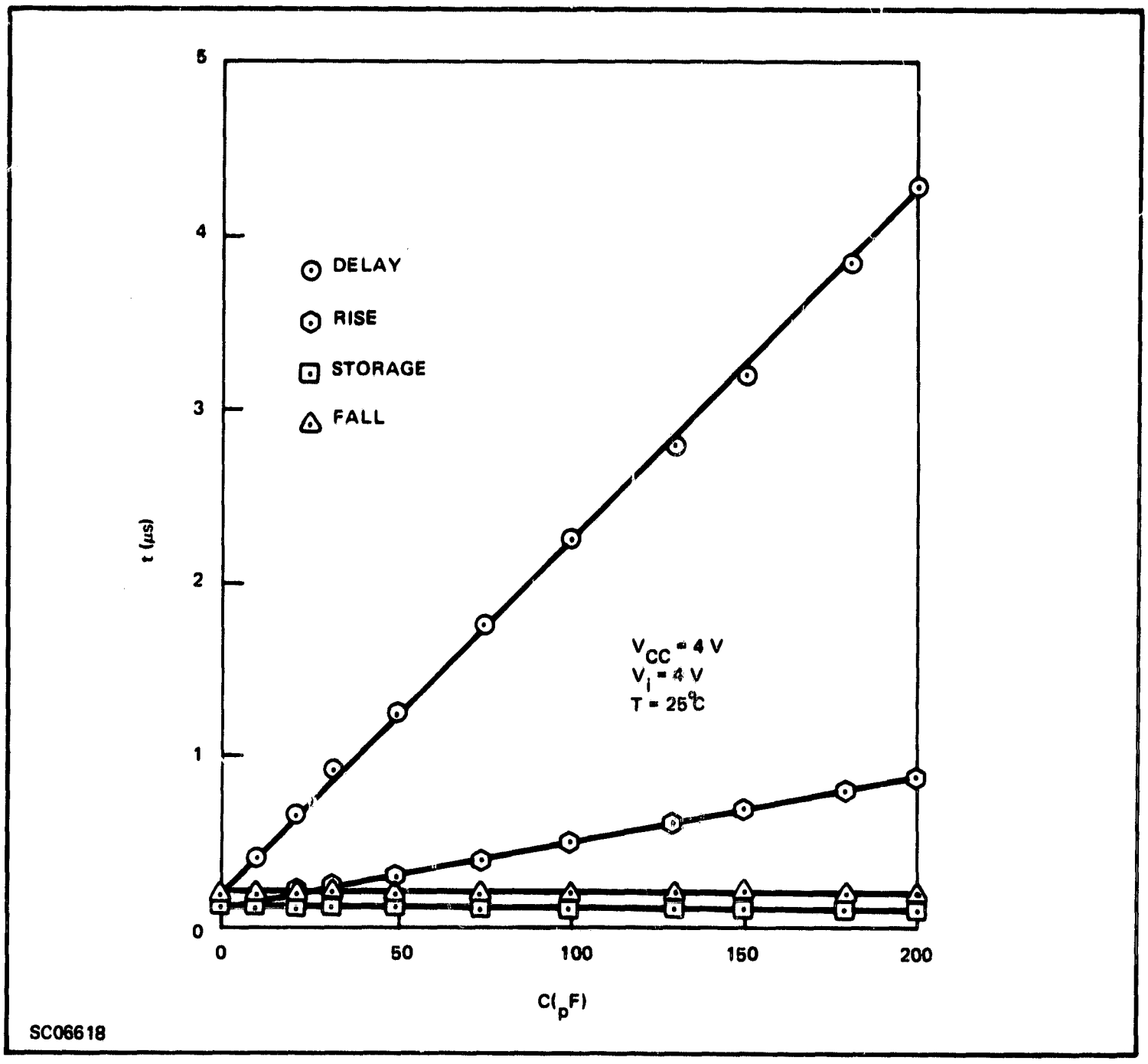


Figure 29. Switching Times at Driver Circuit Final Collector Resistor versus Loading Capacitance

t_R = 1.8 μs

t_F = 36.2 μs

which are reasonably close to the measured values of 2.2 and 32.0 μs respectively at the transistor terminals. The driver circuit contributed about 0.2 μs to each of the measured values. For the new structure, applying the increased factor of 1.5 for C_{CB}, the calculated

t_R = 2.7 μs

t_F = 54 μs

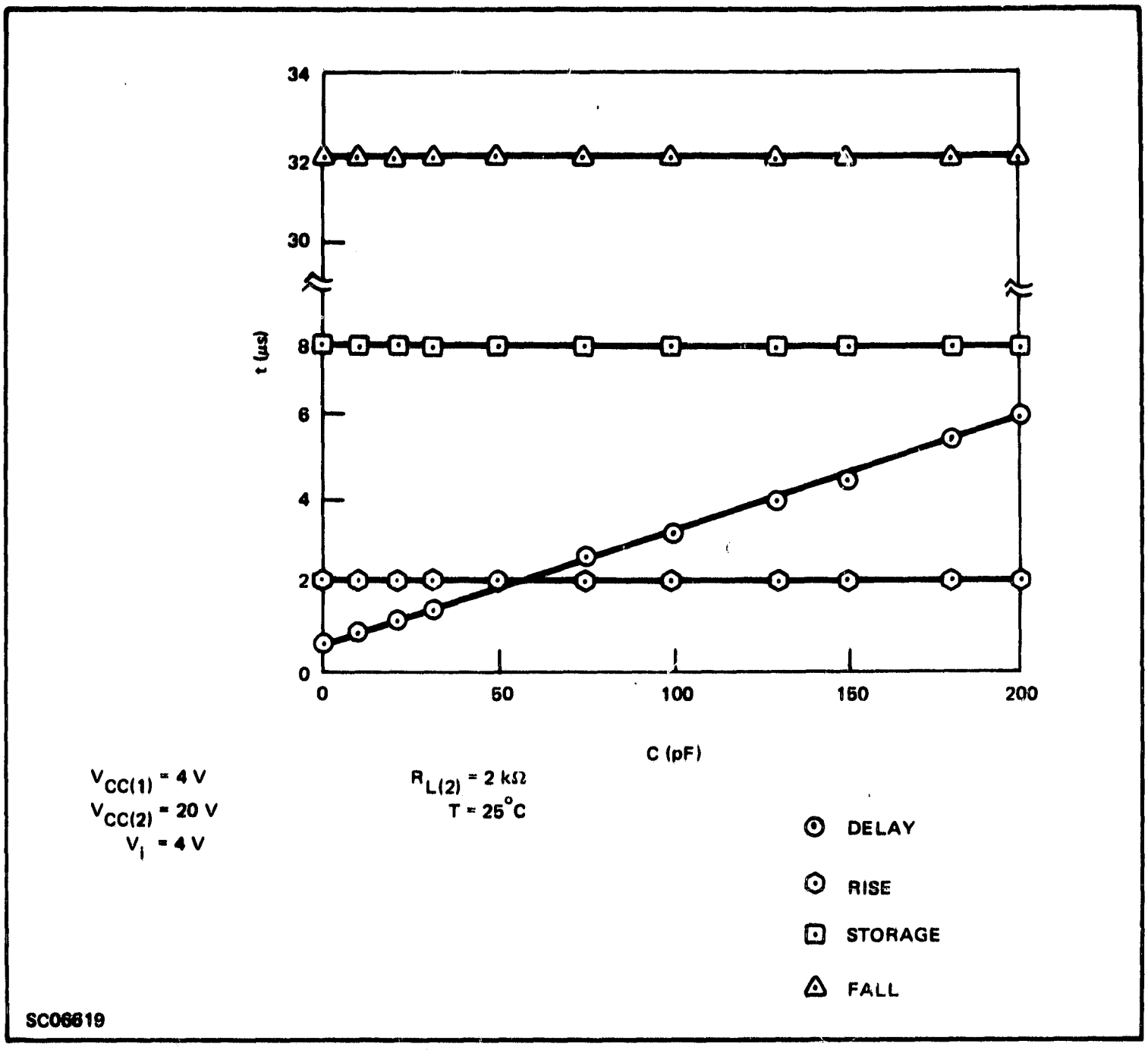


Figure 30. Phototransistor Switching Times versus Driver Circuit Loading Capacitance

For comparison, the typical values for the Phase I devices in Table XVIII are

$$t_R = 3.3\ \mu s$$

$$t_F = 52\ \mu s$$

compared to the maximum specifications of 10 and 100 μs respectively.

Additional speed measurements were made on the driver-circuit breadboard, using a diffused resistor between the power supply and base of the first transistor. The resistor consisted of one 17-kΩ or 2 series-connected 17-kΩ resistors from the TIXL106. Effects for other (diffused) driver-circuit resistors are expected to be negligible.

For large additional capacitance applied to what will be the common junction of the input diodes, the delay and rise times of collector current in the driver-circuit final transistor were found to be proportional to the resistance, regardless of whether the resistor was a diffused or a carbon-composition type. For small additional capacitance, delay and rise times at the transistor collector were slightly larger, which can be accounted for simply by the capacitance of the diffused resistors. Time values were proportional to the resistance (and capacitance) value of the diffused resistors. Indicated delay and rise times with a 27-kΩ diffused resistor are 360 and 180 ns respectively, compared to 180 and 120 ns for the 27-kΩ carbon resistor. Storage and fall times were the same for both resistance types.

For the switching times at the collector of the phototransistor, the delay time for the diffused resistor was about 600 ns and 900 ns for the 17-kΩ and 34-kΩ values, compared to 700 ns for the 27-kΩ carbon resistor. Rise, storage, and fall times were identical for both types.

In conclusion, the distributed capacitance of the large-value resistor in the driver circuit should have only a small effect on the switching-time characteristics of the complete isolation switch.

h. Isolation Characteristics

For the Phase I devices the capacitance between the phototransistor collector-emitter terminals and the other terminals C_{iso} ranged from 1.8 to 6.4 pF, compared to the 10 pF maximum specification. The average value was 2.5 pF.

All devices were also required to meet a 50 V isolation.

i. Environmental Testing

Preliminary devices were subjected to mechanical tests for evaluation. Of the two Se-S-As optical coupling glasses described previously, the one having the higher softening temperature was used. Nineteen GaAs switches having epoxy encapsulation, and eleven without epoxy, were subjected to vibration consisting of 35 g's of rms vibration swept sinusoidally from 20 to 2000 Hz and then returned to 20 Hz during a 15-minute period. The devices were hard mounted in each of three mutually perpendicular planes. All of the devices passed the test without lead rupture or significant change in the optical coupling. The relative optical coupling was determined by measuring the collector-base current with forward bias applied to the light-emitting diode.

The devices were then subjected to temperature cycling. Each of 10 cycles consisted of 15 minutes at -65°C, 5 minutes at +25°C, 15 minutes at +200°C, and 5 minutes at +25°C in immediate succession. The results, for cycling to +200°C, were not satisfactory. Of the 19 epoxied devices, 7 passed without lead rupture or change in optical coupling. Of the 12 others, one or more leads were ruptured. Of the 11 devices without epoxy, no lead ruptures were exhibited. However, only one had no change in optical coupling. The other ten exhibited an optical-coupling reduction of over 90 percent. For the unepoxied devices, these results are in agreement with observations of the softness of the coupling glass at high temperatures.

Additional temperature-cycling tests were performed using both glasses to determine the reasonable operating-temperature limits for each. All devices tested had epoxy encapsulation. Three temperature-cycling tests were used: units were cycled ten times between -65°C and +150°C, -65°C and +175°C, and -65°C and +200°C. After each fifteen-minute exposure to a high or low temperature the units were placed in the laboratory ambient for five minutes. After each complete cycling the units were tested electrically to determine whether any leads had opened or there was any significant change in the optical coupling. Designating the glass having the higher softening temperature as Glass No. 1, Table XX summarizes the results for 20 units, ten made with each type of glass, and successively cycled between the temperature limits shown. Failures include those which experienced emitter or base lead breakage on the phototransistor or a significant change in the optical coupling. Optical coupling was measured in terms of the collector-base current resulting for a fixed forward-bias current applied to the light-emitting diode.

Table XX. Temperature - Cycling Results for GaAs Switch

Temperature Limits	Cumulative Percentage of Failures	
	Glass No. 1	Glass No. 2
-65°C to +150°C	0	0
-65°C to +175°C	10	30
-65°C to +200°C	10	70

Using the criteria of no failures in the above tests, it can be concluded that the upper temperature limit for both glasses is 150°C. Considering this and previous poor results with devices fabricated without the epoxy encapsulation, it is considered that the best design uses Glass 1 and the epoxy encapsulation.

Of the 20 GaAs switches delivered under Phase I, ten were internally encapsulated with the epoxy for added structural rigidity. After lids were welded on each package, hermetic sealing was tested using Radiflo, which indicated leakage rates of less than 10^{-8} cc/s air, and also using a bubble test in 65°C alcohol which indicated no gross leakages.

j. Thermal Characteristics

The basic construction of the GaAs switch shown in Figure 10 is identical to that for this coupled pair in the isolation switch. For both, the thermal path for heat dissipated in the GaAs diode is through the coupling glass, the transistor, and the package base material to the heat sink.

For a number of Phase I GaAs switches, tests were made to evaluate the temperature rise of the diode under dissipation conditions. The base ceramic of these devices was larger than will be described for the isolation switch, but this should not have a significant effect on the results, as thermal spreading effects in the ceramic should be small. The measuring technique consisted of using the voltage drop of the GaAs diode at a forward current of 5 mA as the temperature-indicating parameter. The voltage drop at 5 mA was first measured over the temperature range of 25°C to 100°C. Because there is little temperature rise at a 5 mA bias level, these calibration curves provide an accurate measure of the junction temperature of the GaAs wafers. The GaAs switch integrated-circuit flat packages were then mounted in pressure contact with a 25°C heat sink, and power was applied to the GaAs diodes. The power was repetitively interrupted for a brief time for application of 5 mA, and the corresponding forward drop was measured with an oscilloscope. The GaAs wafer temperature was then determined using the calibration curves. The thermal resistance was calculated by dividing the rise in the GaAs wafer temperature above that of the heat sink by the average power dissipation.

The forward-voltage calibration curves for three GaAs switches are shown in Figure 31. These devices used 40-mil-diameter GaAs diodes as pictured in Figure 11. For these devices the measured thermal resistances were 0.31, 0.39, and 0.40°C/mW. Overall accuracy of the measurements was about ± 20 percent. For maximum GaAs diode biasing for the isolation switch of 44 mA at 1.46 V at -20°C and 34 mA at 1.25 V at 100°C, as given by worst-case analyses, the maximum dissipations are 64 mW at -20°C and 42 mW at 100°C. For the largest value of thermal resistance measured at 0.4°C/mW, the indicated maximum temperature rise for the GaAs diode above that of the heat sink at -20°C and 100°C is only about 25°C and 17°C respectively, or a 117°C maximum diode temperature at 100°C (for no transistor dissipation).

Additional tests were made to evaluate the temperature rise of the GaAs diode for GaAs switches which use the smaller, 26 × 26-mil GaAs wafer. For these tests, GaAs switches with larger and smaller GaAs wafers were evaluated which were assembled on TO-5 headers. Thus it is the additional thermal resistance exhibited with the smaller wafer which is of interest. For two larger wafer devices tested, the thermal resistances measured 0.23 and 0.33°C/mW, or an average of 0.28°C/mW. For two GaAs switches having the smaller GaAs wafers the thermal resistances measured 0.33 and 0.43°C/mW, or an average of 0.38°C/W. Thus the smaller emitting-diode wafers result in a thermal resistance between the diode and case which is 0.1°C/mW greater than that with the larger wafers. The increase is only 27 percent (compared to the average 0.37°C/mW for the larger wafer devices), much less than the factor of 90 percent indicated on a wafer-area basis. This indicates that the heat flow is not transmitted uniformly through the glass layer. Accurate calculations could not be made because of lack of a value for the thermal conductivity of the glass. However, order-of-magnitude calculations suggested that the 27 percent increase is reasonable on the basis of thermal spreading effects; that is, the GaAs wafer has a thermal gradient which results in a major portion of the heat flow being through the central region. Addition of the 0.1°C/mW increase to the maximum previous value of 0.4°C/mW indicates a maximum value of 0.5°C/mW for the smaller GaAs wafer, or a maximum wafer temperature at 100°C of 121°C. This is insignificantly greater than the 117°C value for the larger GaAs wafer.

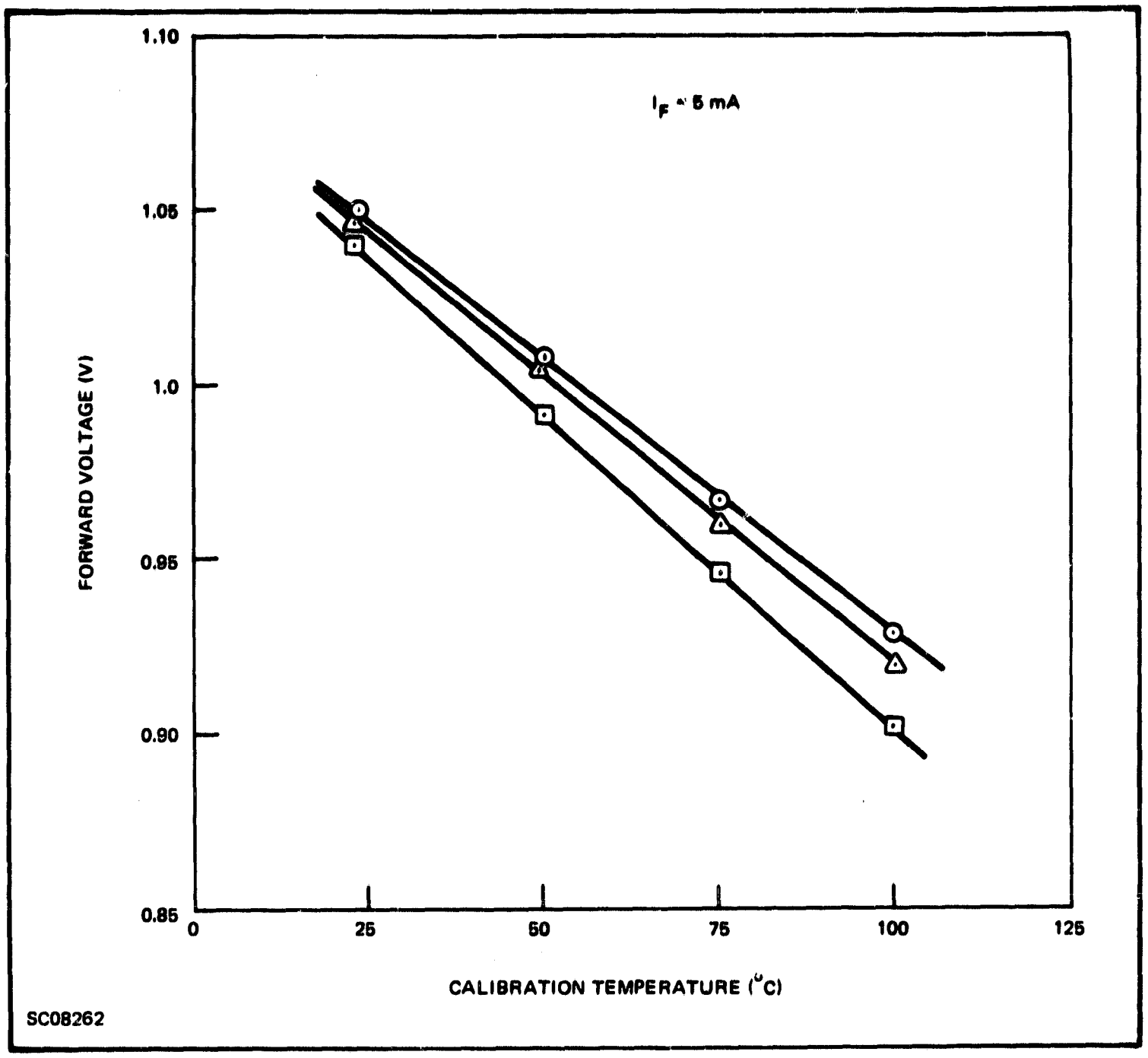


Figure 31. GaAs Diode Forward Voltage - Temperature Characteristics

Preliminary data for thermal resistance between phototransistor and case gave a value of about 0.1°C/mW or less. The maximum dissipation in the phototransistor for the conditions in the test specifications (V_{CC}= 20 V and $I_{C(SAT)}$ = 10 mA) is 50 mW, for which the preliminary indicated maximum temperature for a 100°C heat-sink temperature would be 105°C. A dissipation of 50 mW would be experienced in the phototransistor only in the intermediate switching range (10 V drop across the transistor), and the 5°C rise could occur only if this bias point were held for a significant period (~0.1 sec). Normally the maximum temperature rise in the transistor would occur in the "1" state, for which the specifications would allow only 6 mW dissipation ($V_{CE(SAT)} \leq 0.6$ V, I_C = 10 mA); the preliminary indicated maximum temperature would be only 100.6°C. In either case the temperature rise should be added to that of the GaAs diode for an indication of its maximum temperature. Additional data for the isolation switch are presented in a subsequent section.

k. Life Test Studies

Life tests conducted on the Phase I GaAs switches totaled 11,843 hours. These tests evaluated several important design parameters of the isolation switch: the phototransistor saturation voltage $V_{CE(SAT)}$ conduction current out of saturation, I_C, and the emitting-diode forward voltage drop, V_D. The life test conditions consisted of a GaAs diode forward current I_D = 30 mA at 25°C.

For $V_{CE(SAT)}$ the test results are presented in Table XXI for 31 measurement points for each of 12 GaAs switches. The test conditions consisted of I_{CE} = 10 mA and I_D = 30 mA. The average change in $V_{CE(SAT)}$, between initial and final readings, was an increase of 6 percent; greatest increase was 14 percent.

The test results for I_C of the same devices are given in Table XXII for 26 measurement points. The test conditions were V_{CE} = 0.6 V and I_D = 24 mA. The average change in I_C was a drop of 7 percent. The worst case was a drop of 22 percent.

Results for V_D are given in Table XXIII. The test condition was I_D = 30 mA. The average drop was 3.5 mV; the worst case, 8 mV.

Most of the changes are sufficiently small to make the measuring uncertainty significant. However, some conclusions can be reached. From a previous analysis the major contributor for $V_{CE(SAT)}$ was given as the bulk resistance. Changes, as indicated, would substantiate the benefit of conductivity modulation effects. These would make the ageing effects more sensitive to other parameters. The changes in V_D are of sufficient magnitude, because V_D related to photon-emitting efficiency, to account for the decrease in I_C.

In conclusion, these results indicate a significant operating lifetime for the isolation switch. The devices operated satisfactorily for almost 12,000 hours of continuous biasing. In application some reduced duty cycle would be used. For a 50 percent duty cycle these ageing effects might correspond to twice the period of operation, or almost 24,000 hours.

C. RADIATION TESTING OF RELATED DEVICES

Measurements were made on numerous devices submitted for proton radiation. The devices included 15 discrete GaAs light-emitting diodes (5 each of types TIXL02, TIXL06, and TIXL08), 3 GaAs diode-Si phototransistor pairs (type PEX4001), and 5 diode-transistor integrated-circuit logic gates (type SNX1503). The devices were numbered as follows:

Unit Nos.	Type
1-3	GaAs-Si Pair
4-8	TIXL06
9-13	TIXL08
14-18	TIXL02
19-23	SNX1503

Table XXI. Life-Test Data for $V_{CE(SAT)}$ of GaAs Switches

Device No.	$V_{CE(SAT)}$ at I_{CE} = 10 mA, I_D = 30 mA Elapsed Time (Hrs.)																														
	0	70	160	282	456	765	961	1196	1369	1530	1698	2034	2537	2705	2928	3260	3542	3939	4277	4678	5192	5670	6312	6821	7582	8028	8738	9300	10050	11000	11843
5	0.100	0.101	0.100	0.102	0.100	0.101	0.101	0.102	0.102	0.101	0.101	0.101	0.101	0.101	0.102	0.102	0.102	0.101	0.102	0.102	0.102	0.102	0.103	0.104	0.102	0.103	0.104	0.105	0.104	0.105	0.104
8	0.102	0.104	0.103	0.103	0.103	0.102	0.103	0.103	0.103	0.103	0.103	0.103	0.103	0.103	0.103	0.103	0.103	0.102	0.103	0.103	0.102	0.102	0.103	0.104	0.102	0.103	0.103	0.104	0.103	0.103	0.103
10	0.093	0.095	0.094	0.094	0.094	0.094	0.094	0.095	0.095	0.094	0.095	0.095	0.094	0.095	0.095	0.096	0.095	0.095	0.095	0.096	0.095	0.095	0.096	0.097	0.096	0.097	0.097	0.098	0.100	0.097	0.097
12	0.109	0.106	0.015	0.015	0.105	0.105	0.105	0.106	0.106	0.105	0.106	0.106	0.105	0.106	0.106	0.016	0.106	0.105	0.106	0.106	0.106	0.105	0.106	0.108	0.106	0.107	0.107	0.108	0.109	0.107	0.106
13	0.092	0.094	0.093	0.090	0.091	0.091	0.091	0.091	0.093	0.091	0.093	0.092	0.091	0.091	0.092	0.093	0.091	0.091	0.092	0.091	0.091	0.092	0.092	0.093	0.092	0.092	0.092	0.093	0.092	0.093	0.094
14	0.109	0.107	0.106	0.105	0.106	0.106	0.106	0.106	0.107	0.106	0.107	0.107	0.106	0.017	0.107	0.107	0.107	0.107	0.107	0.108	0.107	0.106	0.108	0.107	0.105	0.107	0.107	0.109	0.107	0.109	0.108
25	0.100	0.100	0.099	0.099	0.099	0.099	0.099	0.099	0.099	0.098	0.099	0.099	0.098	0.099	0.099	0.099	0.099	0.098	0.100	0.099	0.099	0.099	0.100	0.101	0.100	0.101	0.100	0.102	0.101	0.101	0.101
36	0.089	0.089	0.089	0.089	0.089	0.090	0.090	0.091	0.091	0.091	0.092	0.092	0.092	0.093	0.093	0.094	0.094	0.093	0.095	0.095	0.095	0.095	0.097	0.098	0.097	0.099	0.099	0.100	0.100	0.101	0.101
37	0.099	0.096	0.095	0.095	0.095	0.096	0.096	0.096	0.097	0.097	0.097	0.097	0.098	0.098	0.100	0.099	0.099	0.099	0.100	0.101	0.101	0.101	0.103	0.104	0.103	0.105	0.104	0.107	0.107	0.108	0.109
39	0.121	0.113	0.112	0.112	0.113	0.114	0.114	0.115	0.115	0.115	0.116	0.116	0.116	0.117	0.119	0.119	0.119	0.119	0.120	0.120	0.120	0.121	0.123	0.124	0.123	0.125	0.126	0.128	1.12	0.129	0.130
41	0.121	0.123	0.121	0.121	0.122	0.122	0.123	0.123	0.124	0.124	0.124	0.125	0.125	0.125	0.126	0.127	0.127	0.126	0.128	0.128	0.128	0.129	0.130	0.131	0.131	0.132	0.133	0.135	0.134	0.135	0.136
46	0.145	0.146	0.145	0.145	0.146	0.146	0.146	0.147	0.147	0.147	0.148	0.148	0.149	0.149	0.150	0.150	0.151	0.150	0.151	0.152	0.152	0.152	0.154	0.155	0.155	0.157	0.158	0.160	0.160	0.162	0.164

Table XXII. Life-Test Data for I_C of GaAs Switches

Device No.	I_C (mA) at V_{CE} = 0.6 V, I_D = 24 mA Elapsed Time (Hrs.)																								
	0	504	961	1361	1530	1864	2034	2255	2537	2705	2927	3260	3548	3039	4277	4678	5142	5670	6312	6821	7582	8028	8738	10050	11000	11843
5	35	36	36	36	36	38	36	36	36	36	36	36	36	36	36	36	36	36	36	35	36	35.5	35.5	35	35	35
8	32	33	33	33	33	33.5	33.5	33.5	33.5	33.5	33.5	33.5	33.5	33	33.5	33.5	33.5	33.5	33.5	33	33.5	33.5	33.5	33	33	33
10	37	38	38	38	38	38	38	38	38	38	38	38	38	38	38	38	38	38	38	38	38	37.5	37.5	37	37.5	37.5
12	32	33	33	33	33	33	33	33	33	33	33	33	33	32.5	33	33	33	33	32.5	32	32	32.5	32.5	32	32.5	32.5
13	38	40	40	40	40	40	40	40	40	40	40	39	40	40	40	40	40	39	40	40	39.5	39.5	39.5	39.5	39	38.5
14	36	37	37	37	37	37	37	37	37	37	37	37	37	37	37	37	37	37	37	37	38	37	37	37	37	36.5
25	37	38	38	38	38	38	38	38	38	38	38	37.5	38	38	38	38	38	37	37.5	37	37.5	37	37	37	37	37
36	45	44	44	44	44	44	44	44	43.5	43.5	43.5	43	43	43	43	43	43	42.5	42.5	42	42	41.5	41	41	40.5	40
37	40	41	41	41	41	41	41	41	41	41	40.5	40	40.5	40	40	40	40	39.5	39.5	39	39	38.5	38	37.5	37	36.5
39	32	31	31	30	30	30	30	30	30	30	30	29.5	29.5	29.5	29	29	29	28.5	28.5	28	27.5	27	27	26	25.5	25
41	29	29	28	28	28	28	28	28	28	28	27.5	27.5	27.5	27.5	27	27	27	26.5	26	26	25.5	25	25	24	23.5	23.5
46	20	20	20	20	20	20	20	20	20	20	19	19	19	19	19	19	19	18.5	18.5	18.5	18	17.5	17.5	17	16.5	16

Life Conditions: I_D = 30 mA, T_A = 25°C

Table XXIII. Life-Test Data for V_D of GaAs Switches

Device No.	V_D (V) at I_D = 30 mA Elapsed Time (Hrs)																														
	0	70	160	282	456	765	961	1196	1361	1530	1698	2034	2537	2705	2923	3260	3542	3839	4277	4578	5192	5670	6312	6821	7582	8028	8738	9300	10050	11000	11843
5	1.249	1.249	1.250	1.247	1.249	1.249	1.249	1.247	1.249	1.249	1.249	1.247	1.248	1.249	1.247	1.246	1.247	1.249	1.246	1.247	1.247	1.247	1.245	1.245	1.247	1.245	1.246	1.244	1.242	1.244	1.245
8	1.232	1.231	1.231	1.230	1.230	1.230	1.230	1.229	1.231	1.231	1.231	1.230	1.231	1.231	1.229	1.229	1.230	1.232	1.230	1.231	1.231	1.231	1.229	1.229	1.231	1.229	1.230	1.229	1.229	1.229	1.230
10	1.225	1.229	1.224	1.223	1.223	1.223	1.223	1.223	1.224	1.224	1.225	1.223	1.224	1.225	1.223	1.223	1.224	1.226	1.223	1.224	1.224	1.225	1.222	1.223	1.224	1223	1.224	1.222	1.219	1.222	1223
12	1.203	1.203	1.203	1.202	1.202	1.202	1.202	1.201	1.203	1.203	1.203	1.202	1.203	1.203	1.202	1.201	1.202	1.205	1.202	1.203	1.203	1.203	1.201	1.201	1.203	1.201	1.201	1.201	1.200	1.201	1.202
13	1.221	1.220	1.221	1.219	1.220	1.219	1.220	1.219	1.221	1.221	1.221	1.220	1.221	1.221	1.220	1.219	1.220	1.222	1.219	1.221	1.221	1.221	1.218	1.219	1.221	1.219	1.220	1.218	1.219	1.218	1.219
14	1.231	1.230	1.230	1.229	1.229	1.230	1.229	1.229	1.230	1.230	1.231	1.229	1.230	1.231	1.229	1.229	1.229	1.232	1.229	1.230	1.230	1.231	1.228	1.229	1.231	1.229	1.230	1.228	1.226	1.228	1.229
25	1.230	1.229	1.230	1.229	1.229	1.229	1.228	1.227	1.229	1.229	1.229	1.228	1.229	1.229	1.227	1.227	1.228	1.231	1.227	1.229	1.229	1.229	1.227	1.227	1.229	1.227	1.228	1.226	1.224	1.227	1.227
36	1.225	1.224	1.224	1.223	1.224	1.223	1.224	1.223	1.224	1.224	1.225	1.223	1.224	1.225	1.223	1.223	1.223	1.226	1.223	1.224	1.224	1.224	1.222	1.222	1.223	1.222	1.222	1.221	1.220	1.220	1.221
37	1.209	1.208	1.209	1.208	1.208	1.208	1.208	1.207	1.209	1.209	1.209	1.208	1.209	1.209	1.208	1.207	1.208	1.211	1.207	1.208	1.208	1.209	1.206	1.206	1.208	1.205	1.206	1.204	1.201	1.204	1.204
39	1.239	1.237	1.239	1.236	1.236	1.236	1.236	1.235	1.237	1.237	1.237	1.236	1.236	1.237	1.235	1.235	1.235	1.238	1.234	1.236	1.236	1.236	1.233	1.233	1.235	1.233	1.233	1.232	1.229	1.231	1.231
41	1.216	1.215	1.216	1.215	1.215	1.215	1.215	1.214	1.216	1.216	1.216	1.215	1.216	1.216	1.214	1.214	1.215	1.217	1.214	1.215	1.215	1.215	1.213	1.215	1.215	1.213	1.214	1.212	1.209	1.211	1.212
46	1.256	1.255	1.256	1.254	1.255	1.254	1.255	1.254	1.255	1.255	1.255	1.254	1.255	1.255	1.254	1.253	1.254	1.256	1.253	1.254	1.254	1.254	1.252	1.252	1.254	1.252	1.253	1.251	1.250	1.250	1.250

The proton radiation consisted of the following:

Unit Nos	Radiation Dosage
1,5,8,10,11 14,18,19,20	1.2×10^{10} protons/cm^2 at 30 MeV
2,4,12,17,21	1.1×10^{10} protons/cm^2 60 MeV
3,6,9,15,22	1.1×10^{10} protons/cm^2 at 100 MeV
7,13,16,23	1.6×10^{10} protons/cm^2 at 140 MeV

Table XXIV describes the data for the GaAs emitters, which consist of light-output data, forward voltage, and reverse breakdown voltage. In each case little or no change occurred.

In Table XXV, data for the emitter-detector pairs include transistor current gains and overall current gains for several collector currents and saturation voltages. Small decreases in the transistor current gains are indicated only for the lower current. Transistor saturation voltage data unfortunately included 2 pre-radiation values which were in error and were excluded. The one other set of saturation data (for Unit No. 1) is in close agreement.

Data in Table XXVI for SNX1503 logic gates indicate practically identical results before and after radiation.

In conclusion, no significant changes in the important device parameters are indicated for proton radiation.

Table XXIV. Characteristics of GaAs Light Emitter Diodes Before and After Proton Radiation

	Pre-Radiation Tests					Post Radiation Tests				
Unit No.	I_λ at I_F=0.1A	I_λ at 0.5A	V_F at 10 μA	V_F at 0.5A	V_R at 10 μA	I_λ at I_F=0.1A	I_λ at 0.5A	V_F at 10 μA	V_F at 0.5A	V_R at 10 μA
4	0.055	0.54	0.78	1.86	14	0.054	0.54	0.77	1.86	14
5	0.115	0.92	0.73	2.40	17	0.102	0.91	0.73	2.22	17
6	0.021	0.20	0.80	1.80	8	0.020	0.19	0.79	1.80	8
7	0.033	0.34	0.78	1.82	7	0.033	0.35	0.74	1.83	7
8	0.048	0.48	0.75	2.15	8	0.047	0.49	0.78	2.14	8
	I_λ at 50 mA	I_λ at 0.1A	V_F at 10 μA	V_F at 0.1A	V_R at 10 μA	I_λ at 50 mA	I_λ at 0.1A	V_F at 10 μA	V_F at 0.1A	V_R at 10 μA
9	0.115	0.32	0.80	1.30	13	0.12	0.32	0.78	1.30	13
10	0.066	0.195	0.78	1.37	10	0.070	0.196	0.76	1.37	10.4
11	0.110	0.275	0.80	1.30	9	0.111	0.273	0.78	1.31	9
12	0.093	0.225	0.80	1.33	11	0.096	0.230	0.79	1.31	11
13	0.180	0.46	0.82	1.33	13	0.182	0.445	0.80	1.32	12.6
	I_λ at 50 mA	I_λ at 0.1A	V_F at 10 μA	V_F at 0.1A	V_R at 10 μA	I_λ at 50 mA	I_λ at 0.1A	V_F at 10 μA	V_F at 0.1A	V_R at 10 μA
14	0.016	0.42	0.62	1.10	5	0.016	0.041	0.62	1.13	4.4
15	0.033	0.074	0.74	1.12	7	0.033	0.073	0.73	1.13	7.3
16	0.032	0.072	0.70	1.13	6	0.033	0.072	0.68	1.13	5.0
17	0.032	0.074	0.70	1.13	7	0.030	0.071	0.55	1.14	2.1
18	0.039	0.086	0.70	1.13	7.7	0.038	0.086	0.70	1.13	7.5

I_λ – solar cell photodetector, short-circuit current in mA

Table XXV. Characteristics of GaAs Emitter Diode–Si Transistor Pairs Before and After Proton Radiation

Unit No.	I_B (μA) I_C = 0.1 mA	I_B (μA) at 1 mA	I_B (μA) at 10 mA	I_D (mA) at 0.1 mA	I_D (mA) at 1 mA	I_D (mA) at 10 mA	$V_{CE(sat)}$ (V) at I_D = 20 mA I_C = 10 mA
Pre-radiation Tests							
1	0.20	1.68	15.9	0.675	2.34	10.7	2.23
2	0.19	1.66	17.0	1.13	4.6	23.8	
3	0.63	3.75	26.1	5.2	9.1	22.8	
Post-radiation Tests							
1	0.23	1.80	16.2	0.69	2.43	10.8	2.26
2	0.25	1.75	17.2	1.18	4.8	24.0	16.0
3	0.60	3.80	26.1	5.2	9.1	23.0	14.0

I_B = transistor base current
I_D = GaAs emitter current
V_{CE} = 6 V T = 25°C

Table XXVI. Characteristics of Diode-transistor Logic Gates-type SNX1503, Before and After Proton Radiation

Device	Input Lead	Output Lead	Pre-radiation			Post-radiation		
			V1 (V)	V2 (V)	V3 (V)	V1 (V)	V2 (V)	V3 (V)
19	9	8	1.22	1.58	0.054	1.18	1.60	0.052
	10	8	1.21	1.59	0.054	1.18	1.59	0.052
	12	11	1.21	1.59	0.056	1.20	1.60	0.055
	13	11	1.21	1.59	0.056	1.20	1.60	0.055
20	9	8	1.22	1.59	0.066	1.21	1.61	0.066
	10	8	1.22	1.60	0.066	1.20	1.61	0.065
	12	11	1.21	1.59	0.071	1.20	1.60	0.069
	13	11	1.22	1.59	0.071	1.21	1.60	0.069
21	9	8	1.24	1.61	0.070	1.22	1.62	0.070
	10	8	1.24	1.60	0.070	1.22	1.61	0.070
	12	11	1.24	1.63	0.069	1.22	1.62	0.066
	13	11	1.24	1.62	0.069	1.22	1.62	0.066
22	9	8	1.22	1.60	0.063	1.21	1.60	0.060
	10	8	1.22	1.60	0.063	1.21	1.60	0.060
	12	11	1.23	1.60	0.074	1.22	1.60	0.071
	13	11	1.23	1.60	0.074	1.22	1.60	0.071
23	9	8	1.21	1.60	0.057	1.21	1.60	0.055
	10	8	1.20	1.61	0.057	1.24	1.60	0.054
	12	11	1.21	1.76	0.055	1.20	1.61	0.052
	13	11	1.21	1.74	0.055	1.20	1.62	0.052

V_{CC} = 4.75 V

V_2 - Input turn-on threshold, output = V3 = 0.002 V above full-on output

V1 - Input turn-off threshold, output = 4.70 V.

SECTION III

ISOLATION-SWITCH DEVELOPMENT

A. INTEGRATED-DRIVER CIRCUIT

1. Layout

Seven photolithographic masks were designed for fabrication of the integrated-driver circuit. These consist of the following:

a) one for diffusion of transistor collectors;

b) one for diffusion of transistor bases and all resistors;

c) one for emitter diffusion;

d) one for removing oxide on wafer where metal contacts are to be made;

e) one for preliminary metal pattern for probe measurements;

f) two for interconnection metal pattern selected according to tap required on resistors as described in a following section.

A preliminary composite scale drawing of these patterns is shown in Figure 32, with 14 diode-connected transistors provided on three sides of the wafer. The 4 additional diodes were included to allow for the possibility that the yield for the input diodes for the first fabrication runs of the driver circuit may not be high. In that case there would still be the probability that 10 of the 14 would be satisfactory as determined from individual probing. The 4 additional diodes, accounting for little area on the driver wafer, also allow for future expansion of the number of input diodes or for future major modifications of the interior lead arrangement.

Each of resistors R1 through R5 is surrounded by a separate N-type (collector-diffused) tank which provides electrical isolation between the P-type resistors and substrate. An appropriate point on each tank is electrically connected to the point of greatest potential of the associated resistor. This establishes a reversed-bias condition on the isolating PN junction between the substrate and tank. Continuity between the resistor and tank also prevents transistor action between the substrate and resistor which could result in "latch-up" at high temperatures. This condition is characterized by a high-dissipation, inoperative mode of the integrated circuit. Three of the metal pads provided on each resistor allow for two alternate resistor connections as required to establish resistor tolerances less than standard manufacturing tolerances. Additional pads on R1, R2, and R3 were included to increase the versatility of the driver circuit, allowing operation for a power-supply-potential design range of 5.0 to 6.0 volts within the present power-dissipation

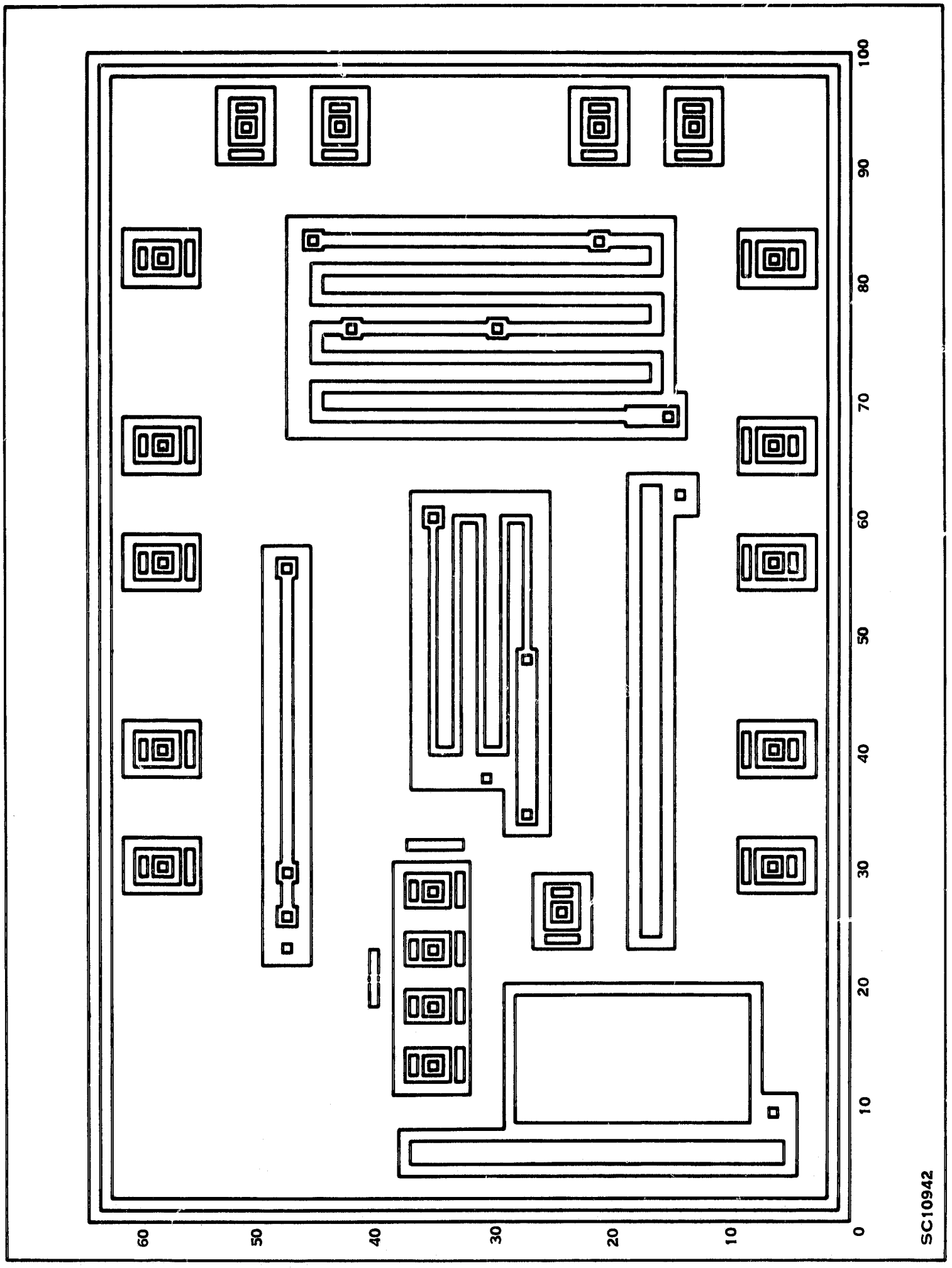


Figure 32. Driver Circuit Component Layout

specifications. The interconnection patterns as now designed allow for the present specified design range of 3.5 to 4.5 volts for the power-supply potential. Resistor R3, the most important component for establishing the current in the light-emitting diode, consists of two separate sections connected in parallel by the interconnection pattern, depending on the required resistor value. The width of the larger-area section of R3 was chosen to minimize the effects of mechanical tolerances, and the area was selected with consideration for the maximum density of power dissipation. Transistor Q_2 (Figure 32) consists of one collector region and four separate base-emitter regions. This design provides the same type of transistor saturation voltage characteristics as for the devices evaluated for the design data. Two small emitter-diffused regions near Q_2 allow for the single interconnection crossover in the base and emitter lead paths, providing the same base drive conditions for the two base paths.

Metal pads are appropriately positioned for lead connections between the driver-circuit wafer and package, as will be discussed in a following section.

2. Processing

Major processing steps are shown in Figure 33. The processing procedure is as follows:

a) Oxidize the slice. Use KMER with mask 1. Perform oxide removal and N-type diffusion into the P-type substrate. This forms the transistor collectors and resistor-isolation tanks.

b) Reoxidize the slice. Use KMER with mask 2. Perform oxide removal and P-type diffusions into the previous N-diffusions. This forms the transistor bases and the resistors.

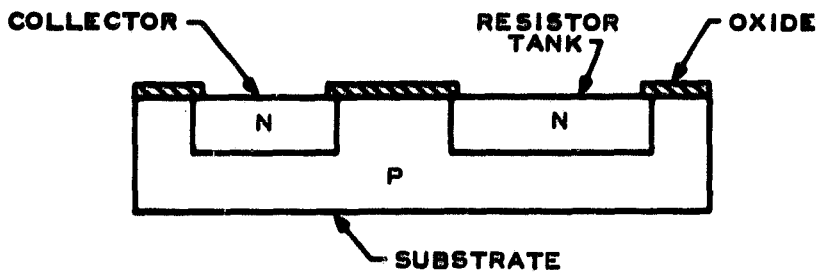
c) Reoxidize the slice, and use KMER with mask 3. Perform oxide removal and N-type diffusion into the P-diffusions of the transistors. This forms the transistor emitters.

d) Reoxidize the slice, and use KMER with mask 4. Perform oxide removal, revealing the silicon areas to be metallized.

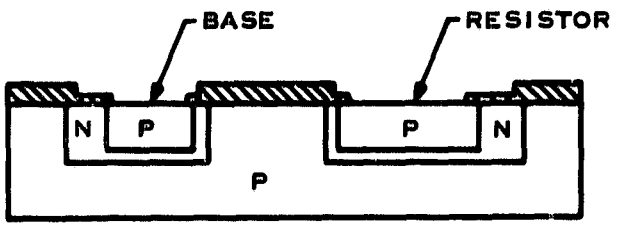
e) Evaporate metal over the slice. Use KMER with mask 5, leaving only metal within the oxide windows of step 4, with pads for each for probing. At this point measurements can be made of the circuit parameters in slice form.

f) Measure the circuit resistors to establish which of two resistance ranges has been produced within the manufacturing tolerance. Remetallize the slices and apply KMER. Use either mask 6 or 7 as appropriate for forming the interconnection pattern and selecting the proper resistor taps.

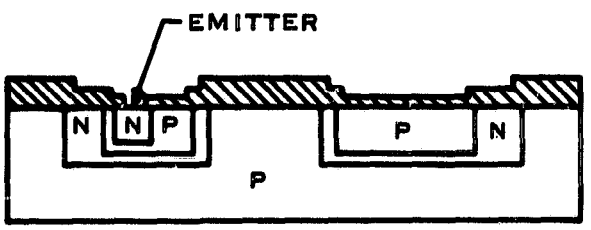
Many evaluations are made during processing. One important test is concerned with the forward current gains of the transistors. Following step c a portion of a slice is taken from the lot, and all oxide is removed. Transistor current gains are measured by probing directly to the diffused regions. As indicated in step f, measurements of the resistors are needed to set the values within the range used in the worst-case analysis. The values of most corresponding resistors in an entire diffusion run fall within a narrow range. A wider production tolerance is obtained when a



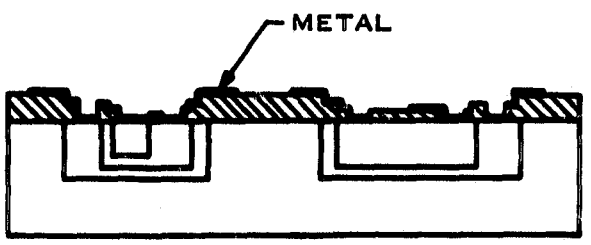
a. DIFFUSE TRANSISTOR COLLECTORS AND RESISTOR TANKS



b. DIFFUSE BASES AND RESISTORS



c. DIFFUSE EMITTERS



d. APPLY METALLIZATION

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Figure 33. Major Processing Steps for Driver Circuit

significant number of runs is involved. Establishing the particular resistivity range for a given lot permits a choice between two metallization patterns. This determines the taps employed and the resistor limits for the lot.

3. Device Results

A completed driver-circuit wafer is shown in Figure 34. Individual components on the wafer can be identified with reference to the composite drawing of the diffusion masks in Figure 32 and the circuit schematic in Figure 7.

For the first lot of driver circuits the resistor values were in the proper range, but transistor collection-emitter breakdown voltages were low. Processing of these devices was continued through fabrication of sample complete isolation switches. For the second lot of circuits the parameters were within design limits.

Individual driver circuits were probed on the slice for overall evaluation. A circuit terminal characteristic in the on-condition, the voltage between the supply voltage terminal and the emitter of Q_2, was measured for values of current of 24 mA and 40 mA. These values corresponded to the worst-case limits of GaAs photon-emitting diode current for the minimum and maximum values of supply voltage. The yield of driver-circuit wafers from this and subsequent lots was good.

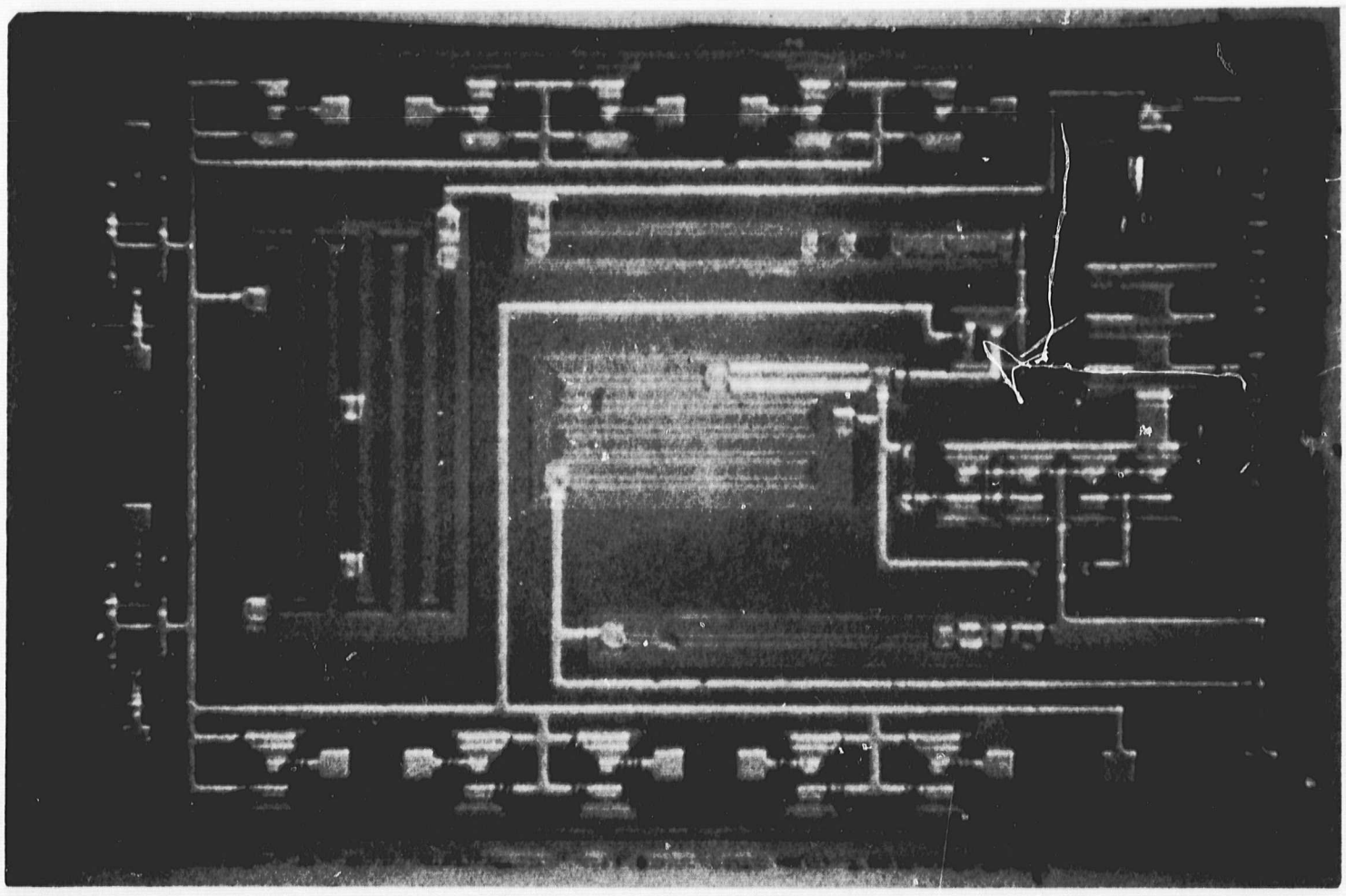


Figure 34. Driver Circuit Wafer

B. ISOLATION SWITCH

1. Packaging and Assembly

Figure 35 illustrates the positioning of the parts in the integrated-circuit flat package. These parts, shown in Figure 36, include the wafers for the driver circuits, phototransistor, and light-emitting diode, two ceramic mounts, and a 14-lead TO-84 integrated-circuit header. Other parts not shown include the high-refractive index glass which bonds the phototransistor and GaAs diode, bonding leads, and solder preforms. The two metallized ceramic mounts are used for isolating the driver circuit and phototransistor. The ceramics chosen have different heights to allow abutting of the ceramics without shorting the metallizations. This allows sufficient clearance for the bonding wires which pass near or over the phototransistor wafer, and minimizes the lead lengths for bonds in this part of the package.

Bonding-lead connections are also illustrated in Figure 35. The arrangement shown provides for the ten inputs. An alternate connection of one of the leads provides connection to the base of Q_1. The metal pads on the driver-circuit wafer were positioned to minimize, insofar as possible, the lengths of the bonding leads to the package leads. Use of 10 of the 14 leads of the package for input leads to the driver wafer limit to some extent the flexibility for positioning wafers and locating metal pads for minimum bonding-lead lengths.

An assembled isolation switch is shown in Figure 37. The driver-circuit wafer was from the first run described. The major assembly steps of the isolation switch are seen in Figure 38. The assembly procedure is as follows:

a) Solder the phototransistor and and driver-circuit wafers to the ceramic submounts.

b) Solder the two metallized ceramic submounts into the header. The positions of the ceramics correspond to the location of the phototransistor and driver-circuit wafers in Figure 37.

c) Bond leads between appropriate pads on the phototransistor and driver-circuit wafers and the header pads.

d) Bond leads to the unmounted emitting diode wafer.

e) Mount the emitting diode to the sensitive region of the phototransistor with the high-refractive-index glass.

f) Bond the appropriate leads of the emitting diode to the header and driver circuit.

g) Cover the periphery of the emitting diode with epoxy.

h) Hermetically can the package.

Preliminary evaluation of this assembly procedure was conducted with isolation switches built with electrically inferior semiconductor wafers. The most important result of this procedure was a change in the choice of the integrated-circuit flat package. The first type of package was selected for its large glass-free wafer-mounting area. There was also a region in the center of the bottom where

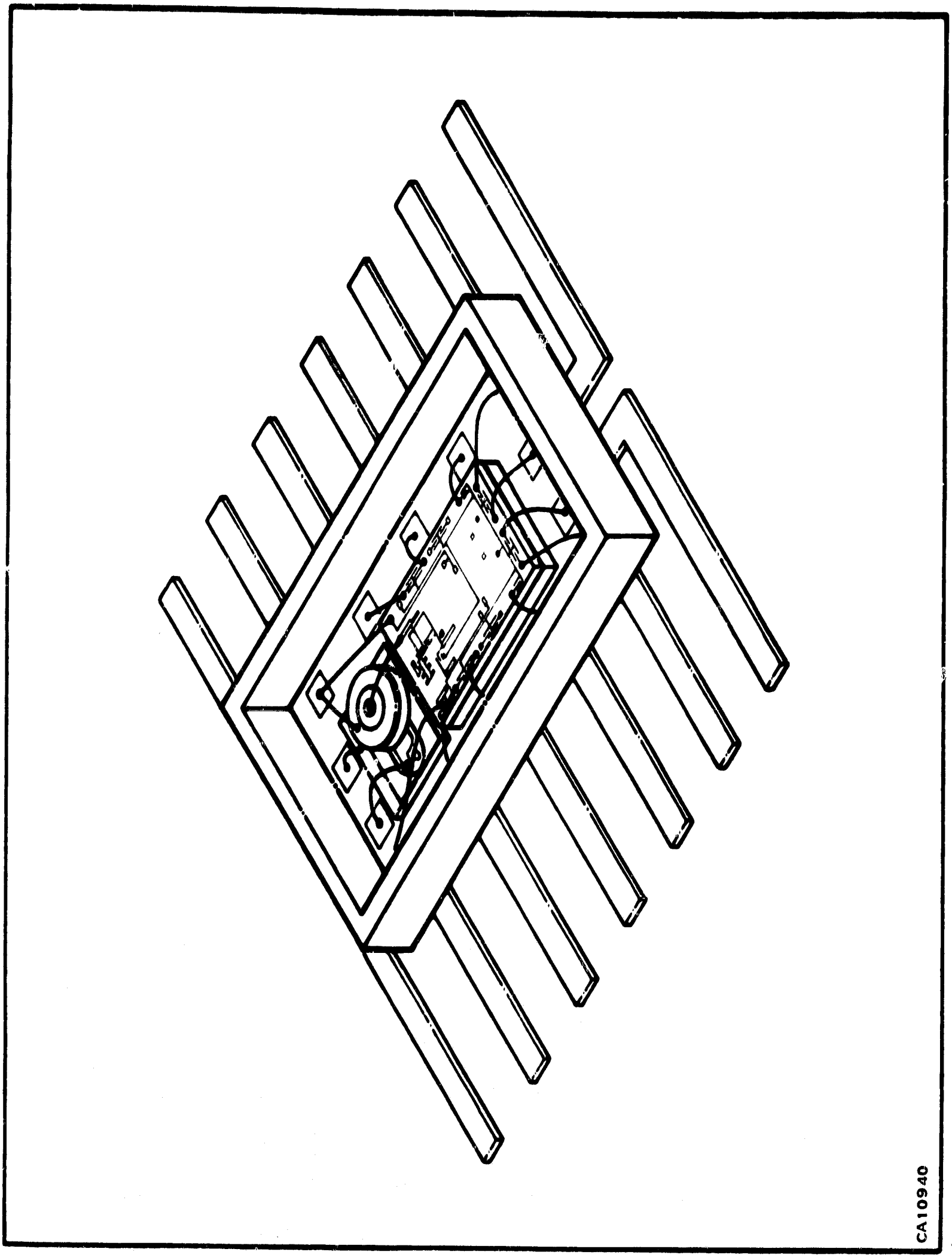


Figure 35. Isolation Switch Layout

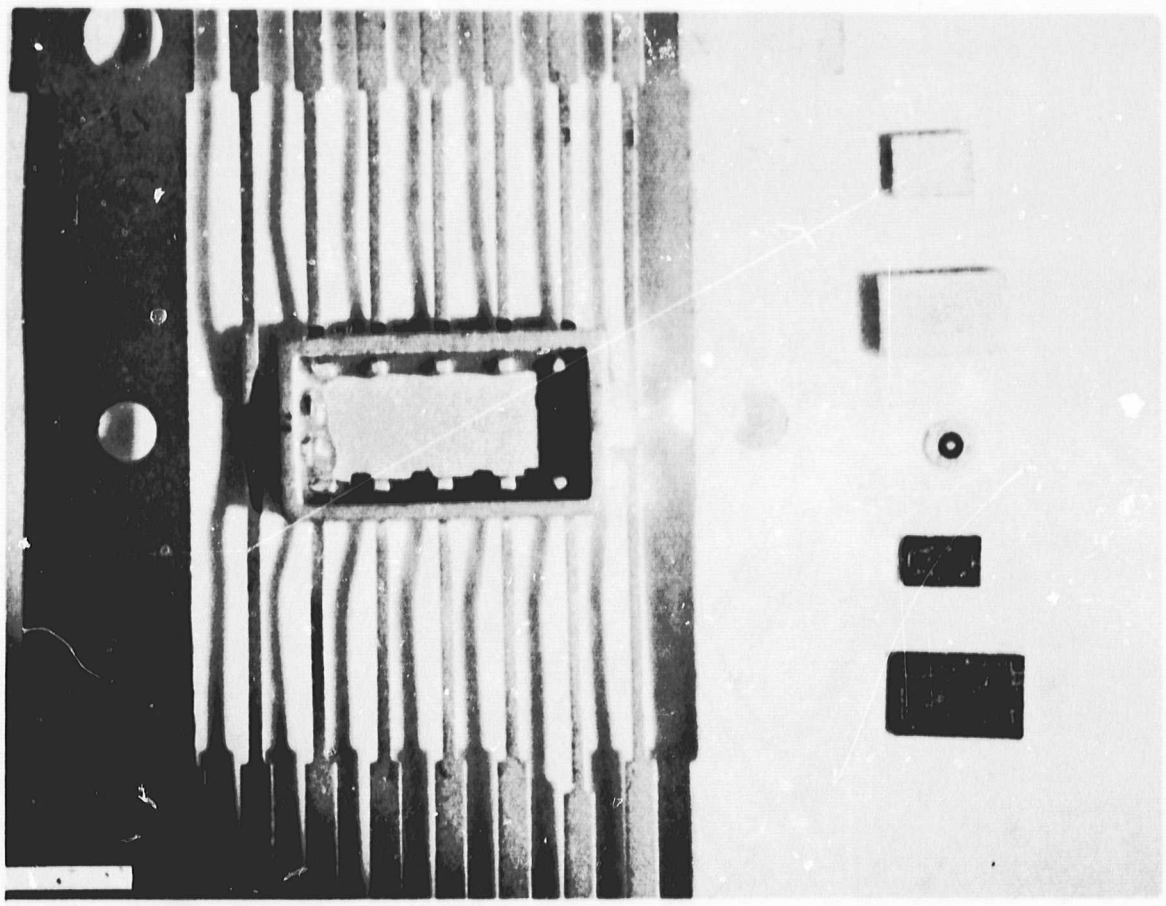


Figure 36. Isolation Switch Parts

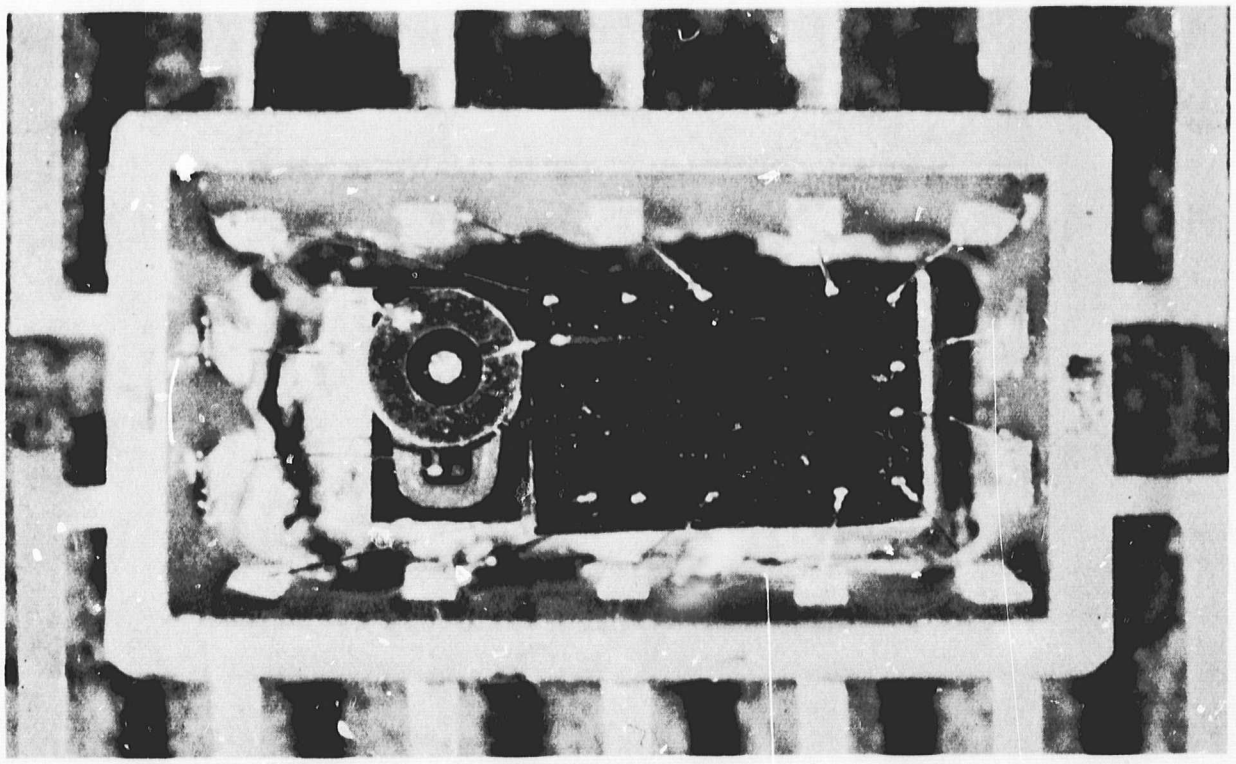
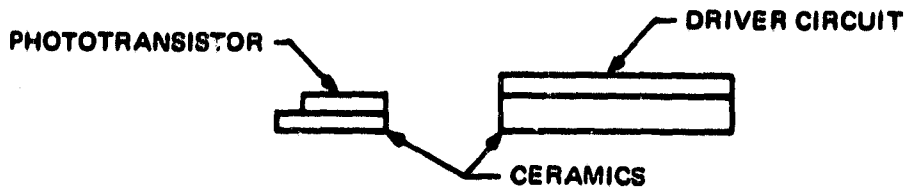
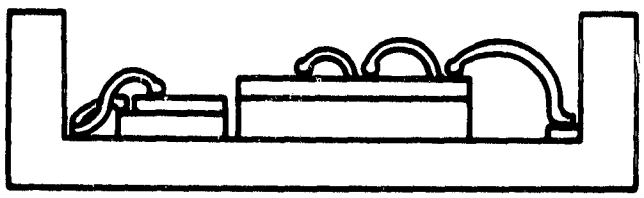


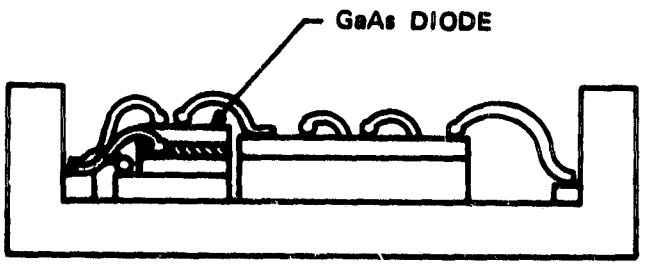
Figure 37. Internal View of Assembled Isolation Switch



a. a) MOUNT SI WAFERS ON CERAMICS



b) MOUNT CERAMICS IN HEADER AND BOND LEADS



c) MOUNT GaAs DIODE AND BOND LEADS

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Figure 38. Major Assembly Steps for Isolation Switch

gold plating was missing. As this package is usually used with silicon chips mounted with glass frit, the gold-free area is usually unimportant. For the isolation switch, however, metallized ceramic wafers are mounted to the package bottom using alloy performs. In the first package the alloy tended to flow to the plated portion of the package bottom, resulting in lumps of excess alloy around the bottom of the ceramic wafers. The new package was dimensionally identical with the former package, but the bottom was completely plated. Isolation switches mounted in the new packages showed no gold lumps.

No significant problems developed in wafer mounting or lead bonding, thus verifying that the assembly procedure was adequate.

Bonding in the isolation switch is considerated a monometallic system. Although aluminum and gold are used for metallization on the phototransistor and driver circuit, respectively, the corresponding type of bonding lead is used to each wafer. Actually all bonding leads are gold except for one aluminum lead required for the phototransistor emitter contact. Aluminum metallization is now employed for the phototransistor because it requires a less complex technique of metal application for low surface-leakage current.

2. Device Results

a. Preliminary Testing

Preliminary electrical evaluation was performed on five isolation switches built with good semiconductor wafers. Circuit parameters, measured at - 20°C, 25°C, and 100°C, are given in Tables XXVII and XXVIII along with the design specifications and measurement conditions. The ten input-diode terminals were connected to give worst-case values of the power dissipation in the off-condition, P_{OFF}, the input diode current in the on- and off-conditions, and the input-diode-breakdown voltage. For these tests the diode breakdown was determined as the difference between the input voltage and the supply voltage, less 0.2 V for the drop across the resistor in series with the input diodes and the power supply, R_1.

Table XXVII. Preliminary Isolation-Switch Characteristics

Parameter	Specification		Device					Conditions				
	Value	Unit	1	2	3	4	5	T (°C)	V_{CC} (V)	V_I (V)	V_{CE} (V)	I_C (mA)
P_{ON}	⩽200	mW	164	160	165	158	166	25	4.5	6	–	–
P_{ON}	⩽200	mW	171	170	172	167	171	-20	4.5	6	–	–
P_{ON}	⩽200	mW	144	143	145	139	142	100	4.5	6	–	–
P_{OFF}	⩽1	mW	0.86	0.90	0.90	0.90	0.90	25	4.5	0	–	–
P_{OFF}	⩽1	mW	0.86	0.90	0.90	0.90	0.91	-20	4.5	0	–	–
P_{OFF}	⩽1	mW	0.81	0.83	0.83	0.86	0.84	100	4.5	0	–	–
I_I	$\leqslant 5 \times 10^4$	nA	≪1	≪1	≪1	≪1	≪1	25	4.5	6	–	–
I_I	$\leqslant 5 \times 10^4$	nA	≪1	≪1	≪1	≪1	≪1	-20	4.5	6	–	–
I_I	$\leqslant 5 \times 10^4$	nA	24.8	28.0	23.0	42.0	36.0	100	4.5	6	–	–
I_I	⩽-1	mA	-0.189	-0.197	-0.197	-0.195	-0.198	25	4.5	0	–	–
I_I	⩽-1	mA	-0.190	-0.200	-0.200	-0.200	-0.200	-20	4.5	0	–	–
I_I	⩽-1	mA	-0.174	-0.178	-0.179	-0.178	-0.180	100	4.5	0	–	–
BV_{DI}	⩾6.5	V	7.9	8.0	7.9	8.0	7.9	25	–	–	–	–
BV_{CEO}	⩾35	V	72	84	75	70	86	25	–	–	–	1
I_{CEO}	⩽100	nA	1	1.3	1	1.2	1.1	25	–	–	20	–

Table XXVIII. Preliminary Isolation-Switch Output Characteristics

Parameter	Specification		Device					Conditions				
	Value	Unit	1	2	3	4	5	T (°C)	V_{CC} (V)	V_I (V)	V_{CE} (V)	I_C (mA)
I_{CEO}	100	nA	1.4	1.9	1.4	1.8	1.3	25	4.5	1	20	–
I_{CEO}	100	nA	<1	<1	<1	<1	<1	-20	4.5	1	20	–
I_{CEO}	10	μA	5.95	4.8	6.3	9.4	3.0	100	4.5	1	20	–
V_{CES}	0.6	V	0.14	0.17	0.14	0.17	0.17	+25	3.5	3	–	10
V_{CES}	0.6	V	0.14	0.14	0.11	0.14	0.14	-20	3.5	3	–	10
V_{CES}	0.6	V	0.36	0.31	0.23	0.31	0.38	100	3.5	3	–	10
V_{CES}	0.6	V	0.4	0.26	0.24	0.30	0.27	25	3.5	3	–	15
V_{CES}	0.6	V	0.22	0.20	0.15	0.23	0.23	-20	3.5	3	–	15
V_{CES}	0.6	V	–	–	0.39	–	–	100	3.5	3	–	15
I_C	15	mA	18.5	19.2	27.5	18.5	19.2	25	3.5	3	0.6	–
I_C	15	mA	23.0	17.0	31.0	18.2	18.6	-20	3.5	3	0.6	–
I_C	15	mA	12.5	13.2	18.5	13.4	12.5	100	3.5	3	0.6	–

Switching Times										V_I = Pulse (V)	V_{CE} (V)	I_C (mA)
										Pulse	OFF	ON
t_1	10	μs	10	7.4	6.3	11.6	7.4	25	3.5	3	20	10
t_1	10	μs	6	4.6	4.0	6.6	4.2	25	4.5	3	20	10
t_2	100	μs	40	24	42	41	23	25	3.5	3	20	10
t_2	100	μs	43	27	43	45	25	25	4.5	3	20	10

The data show that only one isolation switch met all design specifications. Four devices failed to satisfy the specification for the phototransistor current, I_C at V_{CE} = 0.6 V, V_{CC} = 3.5 V. These parameters are related to the light emission of the GaAs diode, the optical coupling and phototransistor gain. As indicated by the satisfactory performance of Phase I GaAs switches, these results were not typical of those expected for the isolation switches. Selection techniques used for the GaAs diodes and phototransistors ensure sufficient optical coupling to meet the specifications for I_C and t_1.

Additional tests of the isolation switch were made at 25°C, using a breadboard connection of various driver circuit wafers and a representative GaAs photon-emitting diode. The data for six units, shown in Table XXIX, consist of:

Table XXIX. Characteristics of Several Isolation Switches

Device	$I_{D2(ON)}$ (mA) V_{CC} = 3.5 V V_I = 6 V	$I_{D2(OFF)}$ (nA) V_{CC} = 4.5 V V_I = 1 V	P_{ON} (mW) V_{CC} = 4.5 V V_I = 6 V	BV_{D1} (V) I_I = 10 A	I_I (mA) V_{CC} = 4.5 V V_I = 0
1	23.8	48	160	8.3	-0.192
2	24.3	43	167	8.2	-0.196
3	24.4	44	164	8.2	-0.190
4	24.8	43	166	8.2	-0.198
5	24.3	45	162	8.2	-0.192
6	24.6	43	164	8.2	-0.196

- The emitting-diode current, I_{D2}, for a worst-case on-condition (with the supply voltage V_{CC} = 3.5 V and the input voltage V_I = 6 V) and off-condition (with V_{CC} = 4.5 V and V_I = 1 V)
- The power dissipation P_{ON}, in a worst-case on-condition (with V_{CC} = 4.5 V and V_I = 6 V)
- The breakdown voltage of the input diode, BV_{D1}
- The input-diode current, I_I, in a worst-case on-condition (with V_{CC} = 4.5 V and V_I = 0).

Values obtained for P_{ON}, BV_{D1}, and I_I agree closely with those in Table XXVII. From the worst-case design, the calculated minimum value for I_{D2} at 25°C in the on-condition, $I_{D2(ON)}$, is 24.0 mA. In Table XXVI five devices have values of $I_{D2(ON)}$ between 24.3 and 24.6 mA. For one device $I_{D2(ON)}$ was 23.8 mA, which is within the measuring accuracy of the worst-case value. Values in Table XXIX for I_{D2} in the off-condition, $I_{D2(OFF)}$, range from 43 to 48 nA; this current level results in negligible photo emission and, thereby, photo-induced leakage in the phototransistor.

A primary relationship in the design of the driver circuit for the off-condition is that between the input voltage and the voltage applied to the emitting diode. A detailed measurement of this characteristic was made for a representative driver circuit and emitting diode. The results are described in Figure 39. The relationship between input voltage and emitting-diode current for the same devices is shown in Figure 40. These results are within the design tolerances.

The isolation switches mounted in the new package for evaluation of the device assembly techniques were continued through final processing. Preliminary environmental tests were conducted to examine the units for gross defects. A process lot of 16 units was separated into three groups, submitted for environmental testing, and tested electrically for open or short-circuited leads and for isolation of chips from each other and the package. The tests performed were:

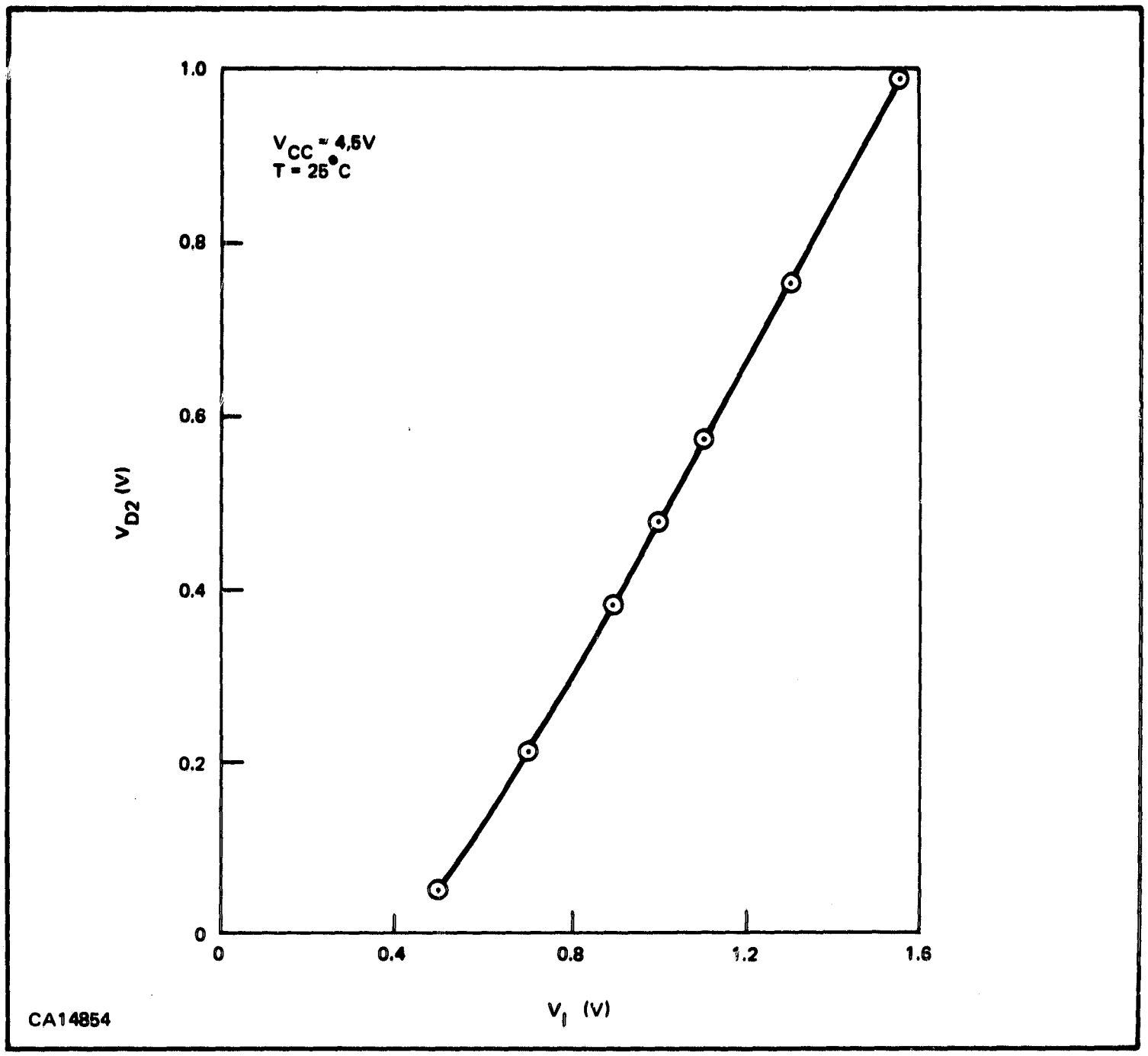

Figure 39. Input Voltage - Emitting Diode Voltage Characteristic for Representative Isolation Switch

- Variable Frequency Vibration: 20 to 2000 to 20 Hz at 50 g, three perpendicular planes, 15 minutes per plane.
- Mechanical Shock: 10,000 g, 0.2 ms onset time, all six planes, five blows per plane.
- Temperature Cycling: 10 cycles consisting of 15 minutes at -65°C, 5 minutes at 25°C, 15 minutes at 150°C, and 5 minutes at 25°C.

No failures were noted. These tests support the recommendation based on tests with GaAs switches, made earlier, that temperature cycling should be limited to -65°C and 150°C.

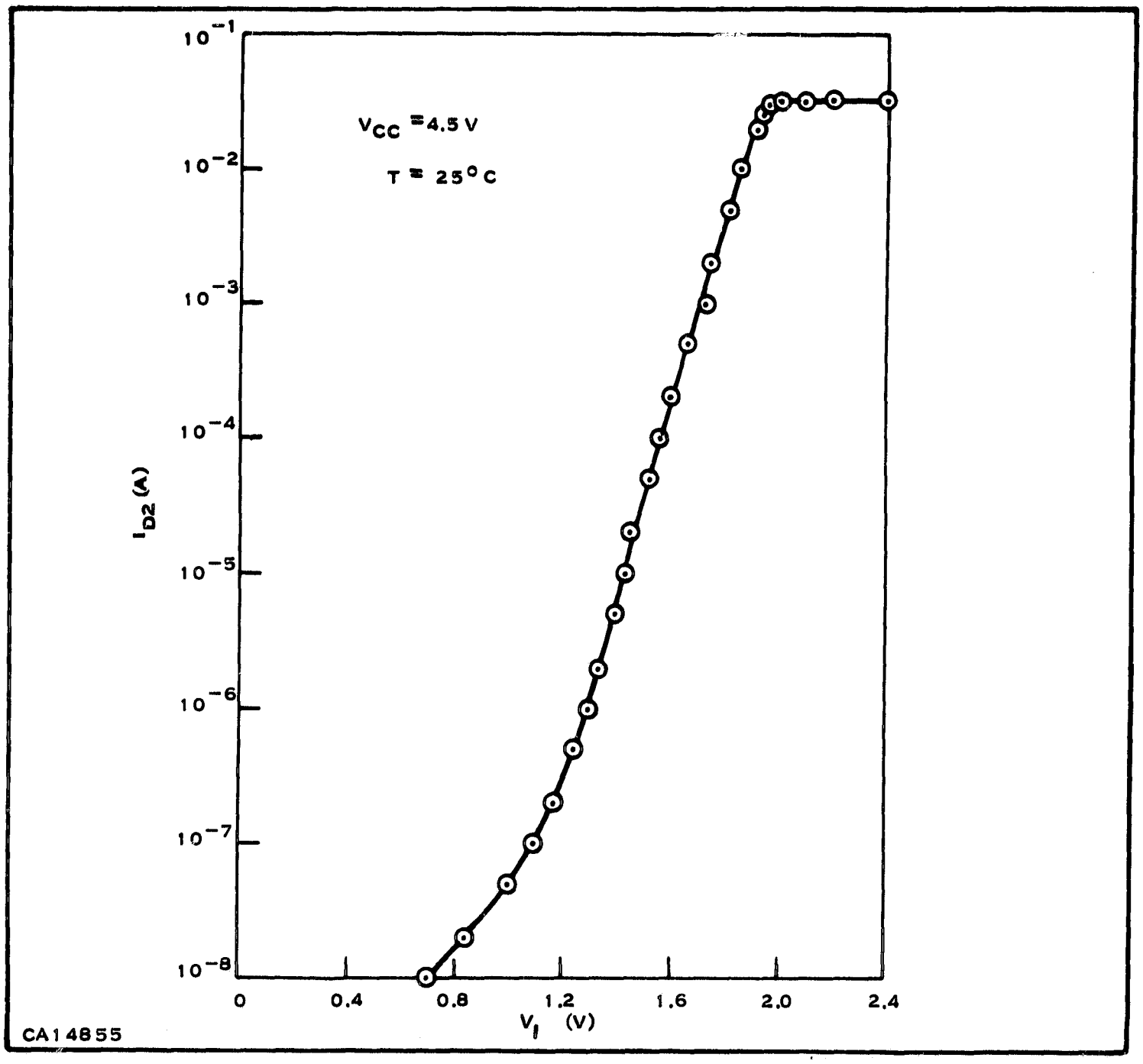

Figure 40. Input Voltage - Emitting Diodes Current Characteristic for Representative Isolation Switch

Following these tests, four electrically good isolation switches (Nos. 1, 2, 4, and 5, described in Table XXVII) were subjected to the previously described environmental tests and to acceleration of 20,000 g's for a period of one minute, with units mounted in each of three mutually perpendicular planes. The evaluation tests consisted of operational measurements and tests for isolation. None of the devices exhibited lead or bond fracture, or change in the isolation or the optical coupling.

b. Final-Test Results

Isolation switches to be tested to the design specifications were first subjected to a 100-hour burn-in consisting of V_{CC} = 4.5 V and V_I = 3 V ("1" condition). Before final testing was started, preliminary sorting was done to eliminate faulty units. The checks made during this sorting include:

1) Checking to see that each of the ten input diodes is connected, and that none have obviously low breakdowns or high leakage.

2) Connecting V_{CC} = 3.5 V to the driver circuit, and checking the phototransistor collector current to ensure that the collector current is in excess of 20 mA when the input circuit is open, and that the collector current drops to a low value when the input circuit is grounded.

Data for thirty isolation switches are given in Tables XXX and XXXI, including the specification limits. All units meet the specifications. The results are in agreement with the characteristics discussed in the previous sections.

Measurements were made of the thermal resistances of the isolation switch for comparison with the previously described results. For the representative isolation switch selected, the thermal resistance of the GaAs diode (larger-type wafer) to the heat sink measured 0.32°C/mW. Measurements were also made of the thermal resistance between the phototransistor and the case. For these tests the collector-base junction was operated in the manner of the GaAs diode described previously. Calibration curves were obtained of the forward-biased V-I characteristic, V_{CB}, as a function of temperature at a constant current of 5 mA. Higher forward-bias currents were applied to heat the diode, and these currents were interrupted to measure V_{CB} at 5 mA. This means dissipating power in the phototransistor with the collector-base forward biased is appropriate, as under normal biasing conditions the dissipation also is primarily in the collector-base junction. For this isolation switch the thermal resistance of the phototransistor to the case measured only 0.07°C/mW. These results are in agreement with results described for the Phase I devices.

Measurements were also made for this device to evaluate the temperature rise of the driver-circuit wafer. In this case a diode-connected transistor near the prominent heat-dissipating element, R_3, was used in the measurement. The forward voltage of this diode was calibrated as a function of temperature. The driver circuit was turned on and the corresponding temperature rise in the nearby diode was evaluated. For the worst-case power dissipation in the driver circuit at 100°C of 144 mW, the temperature rise was measured as only 6.3°C above the heat-sink temperature for a driver circuit mounted on the ceramic wafer in the flat package, as previously described.

In conclusion, the operating temperatures of the semiconductor wafers in the isolation switch can be expected to be only nominally greater than the case temperature.

Table XXX. Performance Characteristics of Isolation Switches for V_{CC} = 4.5 V

	P_{ON} (mW)			P_{OFF} (mW)			I_I (nA)			I_I (mA)			I_{CEO}			BV_{CEO} (V)	BV_I (V)
	V_{CC} = 4.5 V, V_I = 6.0 V			V_{CC} = 4.5 V, V_I = 0 V			V_{CC} = 4.5 V, V_I = 6.0 V			V_{CC} = 4.5 V, V_I = 0 V			V_{CC} = 4.5 V, V_I = 1.0 V, V_{CE} = 20 V			I_{CE} = 0.1 mA	I_D = −0.1 mA
Temp.	−20°C	25°C	100°C	−20°C	25°C	100°C	−20°C	25°C	100°C	−20°C	25°C	100°C	−20°C (nA)	25°C (nA)	100°C (μA)	25°C	25°C
Spec.	200	200	200	1	1	1	5×10^4	5×10^4	5×10^4	−1	−1	−1	100	100	10	35	6.5
Unit																	
1	163	154	141	0.90	0.90	0.84	<1	<1	57	−0.192	−0.192	−0.179	<1	0.82	2.2	81	8.1
2	156	152	137	0.84	0.84	0.80	<1	<1	84	−0.180	−0.179	−0.164	<1	0.71	2.0	70	7.2
3	162	157	140	0.88	0.87	0.81	<1	<1	29	−0.189	−0.188	−0.171	<1	1.6	2.4	67	8.1
4	163	158	144	0.87	0.87	0.81	<1	<1	37	−0.188	−0.188	−0.172	<1	0.80	2.2	71	8.0
5	162	158	142	0.87	0.86	0.81	<1	<1	50	−0.188	−0.187	−0.171	<1	4.3	4.8	66	7.3
6	158	154	137	0.88	0.88	0.83	<1	<1	36	−0.190	−0.190	−0.172	<1	0.25	2.4	69	8.1
7	160	154	137	0.87	0.87	0.82	<1	<1	48	−0.188	−0.187	−0.170	<1	0.48	2.4	72	8.1
8	162	157	140	0.87	0.86	0.81	<1	<1	49	−0.188	−0.187	−0.170	<1	0.48	1.7	70	8.1
9	163	157	140	0.88	0.87	0.81	<1	<1	37	−0.189	−0.188	−0.170	<1	1.3	2.5	68	8.1
10	158	153	137	0.85	0.84	0.79	<1	2.2	100	−0.180	−0.180	−0.168	<1	1.1	2.4	69	7.2
11	158	148	140	0.85	0.85	0.79	<1	<1	45	−0.182	−0.182	−0.169	<1	0.05	2.2	70	8.1
12	159	153	138	0.87	0.86	0.81	<1	<1	38	−0.188	−0.188	−0.171	<1	2.3	4.4	67	8.1
13	160	154	140	0.86	0.86	0.80	<1	<1	46	−0.188	−0.187	−0.171	<1	0.05	1.1	67	8.0
14	157	150	136	0.84	0.84	0.80	<1	<1	34	−0.182	−0.180	−0.168	<1	2.5	2.8	63	8.1
15	155	149	136	0.85	0.85	0.79	<1	<1	37	−0.182	−0.181	−0.168	<1	0.9	2.8	69	8.0
16	157	153	138	0.82	0.83	0.77	<1	<1	32	−0.180	−0.179	−0.165	<1	4.2	9.9	69	8.1
18	171	164	146	0.95	0.92	0.81	<1	<1	12.4	−0.202	−0.205	−0.182	<1	3.6	6.0	68	8.1
19	171	163	144	0.97	0.95	0.88	<1	<1	26.5	−0.209	−0.209	−0.187	<1	0.1	0.91	67	8.1
20	167	157	141	0.91	0.92	0.86	<1	<1	30.0	−0.198	−0.203	−0.181	<1	1.1	2.3	69	8.1
21	167	161	144	0.93	0.92	0.85	<1	<1	17.9	−0.206	−0.202	−0.185	<1	1.7	1.85	69	8.0
22	172	164	148	0.92	0.91	0.86	<1	<1	13.2	−0.203	−0.201	−0.183	<1	3.9	3.0	61	8.1
23	166	160	144	0.91	0.89	0.83	<1	<1	10.5	−0.199	−0.197	−0.179	<1	0.8	1.55	61	8.1
24	158	157	140	0.91	0.90	0.83	<1	<1	13.9	−0.201	−0.198	−0.180	<1	0.9	1.72	67	8.1
25	167	161	144	0.94	0.92	0.86	<1	<1	18.3	−0.208	−0.203	−0.185	<1	0.8	1.40	67	8.1
27	166	158	142	0.92	0.91	0.85	<1	<1	8.5	−0.205	−0.201	−0.183	<1	2.8	2.91	69	8.1
28	167	158	148	0.91	0.91	0.84	<1	<1	19.3	−0.200	−0.200	−0.182	<1	0.8	1.9	69	8.1
29	180	172	153	0.97	0.96	0.89	<1	<1	11.4	−0.212	−0.211	−0.193	<1	3.0	2.2	60	7.9
31	168	161	144	0.96	0.94	0.87	<1	<1	19.0	−0.209	−0.207	−0.189	<1	0.06	0.72	63	8.1
32	169	163	145	0.94	0.93	0.86	<1	<1	9.3	−0.204	−0.202	−0.183	<1	0.6	4.2	78	8.1
33	172	166	147	0.92	0.90	0.84	<1	<1	13.8	−0.202	−0.199	−0.182	<1	0.05	1.36	68	8.1

Table XXXI. Phototransistor Characteristics for Isolation Switches

	V_{CE} (V)			V_{CE} (V)			I_C (mA)			t_1 (µs)	t_2 (µs)	t_1 (µs)	t_2 (µs)	V_{nRise} (V)	V_{nFall} (V)	C_{ISO} (pF)
	V_{CC} = 3.5 V V_I = 3.0 V I_C = 10.0 mA			V_{CC} = 3.5 V V_I = 3.0 V I_C = 15.0 mA			V_{CC} = 3.5 V V_I = 3.0 V V_{CE} = 0.6 V			V_{CC} = 3.5 V V_I = 3.0 V $V_{CE(OFF)}$ = 20 V $I_{C(ON)}$ = 10 mA		V_{CC} = 4.5 V V_I = 3.0 V $V_{CE(OFF)}$ = 20 V $I_{C(ON)}$ = 10 mA		V_{CC} = 4.5 V V_P = 5.0 V		f = 1 MHz
Temp.	−20°C	25°C	100°C	−20°C	25°C	100°C	−20°C	25°C	100°C	25°C	25°C	25°C	25°C	25°C	25°C	25°C
Spec.	0.6	0.6	0.6	0.6	0.6	0.6	15	15	15	10	100	10	100	2	2	10
Unit																
1	0.09	0.12	0.20	0.12	0.15	0.280	42	33	20.1	5.7	44	3.6	58	1.40	1.35	2.038
2	0.09	0.12	0.19	0.11	0.14	0.270	43	35	21.0	6.1	60	3.8	64	1.40	1.35	2.179
3	0.09	0.11	0.20	0.11	0.14	0.290	46	35	20.0	6.7	69	4.1	74	1.40	1.35	1.912
4	0.11	0.13	0.24	0.13	0.16	0.490	33	26	15.6	7.9	58	4.8	64	1.40	1.35	1.990
5	0.10	0.13	0.21	0.13	0.16	0.340	37	30	17.8	7.7	70	4.9	75	1.40	1.30	1.925
6	0.09	0.11	0.20	0.12	0.14	0.270	46	37	20.9	6.1	68	3.8	73	1.40	1.35	1.944
7	0.10	0.12	0.21	0.13	0.15	0.350	38	31	17.7	6.6	59	4.0	63	1.40	1.35	2.205
8	0.10	0.12	0.22	0.12	0.16	0.380	38	30	17.1	6.7	58	4.1	62	1.40	1.32	2.376
9	0.09	0.11	0.20	0.11	0.14	0.280	47	36	20.6	5.8	72	3.7	76	1.40	1.30	2.179
10	0.11	0.13	0.22	0.13	0.16	0.390	37	29	17.3	7.3	62	4.6	67	1.40	1.35	2.189
11	0.11	0.15	0.24	0.13	0.18	0.260	29	26	16.0	8.2	64	5.1	69	1.35	1.30	2.104
12	0.10	0.13	0.20	0.12	0.17	0.280	43	34	20.0	6.9	75	4.3	79	1.40	1.30	1.908
13	0.09	0.12	0.19	0.12	0.16	0.260	45	36	22.0	6.2	64	3.9	67	1.55	1.45	2.116
14	0.08	0.11	0.17	0.11	0.13	0.230	54	43	26.0	5.6	68	3.5	71	1.40	1.35	2.148
15	0.09	0.12	0.19	0.12	0.15	0.250	47	32	22.0	5.9	67	3.7	72	1.35	1.30	2.270
16	0.110	0.140	0.220	0.130	0.180	0.430	33	27	17.0	8.1	56	4.8	63	1.40	1.35	2.042
18	0.085	0.110	0.190	0.105	0.135	0.190	56	42	23.0	4.8	65	3.0	68	1.40	1.30	2.038
19	0.085	0.120	0.210	0.115	0.150	0.210	50	37	19.0	5.3	64	3.3	68	1.40	1.33	2.177
20	0.085	0.110	0.190	0.105	0.140	0.190	57	43	23.0	4.5	71	2.8	75	1.32	1.27	2.549
21	0.105	0.135	0.220	0.125	0.170	0.220	43	32	17.0	6.3	69	3.8	75	1.35	1.30	2.076
22	0.105	0.140	0.240	0.130	0.180	0.240	38	28	15.2	9.6	87	5.8	96	1.32	1.26	2.371
23	0.100	0.130	0.230	0.125	0.165	0.230	43	32	16.5	8.4	89	5.3	96	1.33	1.28	2.239
24	0.090	0.125	0.210	0.115	0.155	0.210	48	36	19.0	5.5	66	3.4	70	1.37	1.30	2.062
25	0.100	0.135	0.240	0.120	0.170	0.240	40	31	15.6	6.4	58	3.8	62	1.35	1.30	2.296
27	0.105	0.135	0.230	0.125	0.170	0.230	44	32	17.0	5.1	65	3.4	69	1.35	1.30	2.056
28	0.085	0.125	0.190	0.110	0.160	0.300	51	37	20.0	4.8	65	3.0	78	1.35	1.30	1.864
29	0.085	0.120	0.190	0.105	0.160	0.350	43	32	17.0	7.7	91	4.7	98	1.35	1.30	2.073
31	0.085	0.125	0.180	0.110	0.155	0.250	51	38	21.0	5.1	60	3.2	62	1.40	1.35	2.038
32	0.115	0.130	0.230	0.150	0.180	0.370	28	28	19.0	6.3	42	4.0	43	1.35	1.30	1.992
33	0.080	0.120	0.220	0.105	0.155	0.340	47	34	18.0	6.1	71	3.6	75	1.35	1.30	2.224

SECTION IV

CONCLUSIONS

The design goals for the isolation switch were met. The successful development of this device demonstrates the ability to combine the present integrated circuit, transistor, and photon-emission-detection technologies to perform functions not realizable in conventional integrated circuits. The isolation switch can be used in place of relays, switches, and signal transformers for better performance in more demanding applications.

The fabrication techniques used were particularly selected to be suitable for practical production of the devices. Commercial availability is planned for a number of device versions. The GaAs emitting-diode phototransistor pair (GaAs switch) is now offered in a six-lead TO-5-type package as the TIXL102 and TIXL103. Plans are being made to offer the isolation switch and also the Si integrated circuit of the switch as an emitting-diode driver.

SECTION V

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