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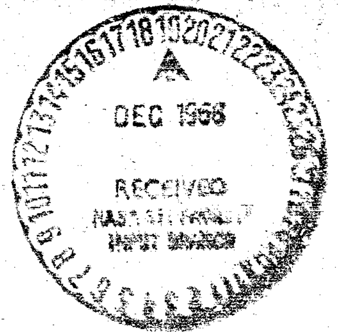

MICROELECTRONICS DIVISION

GENERAL INSTRUMENT CORPORATION • 600 WEST JOHN STREET, HICKSVILLE, L. I. NEW YORK

PHASE I

FINAL REPORT

ESTABLISHMENT OF QUALITY AND RELIABILITY STANDARDS AND DEVELOPMENT OF SCREENING TECHNIQUES FOR MOS MICROELECTRONIC DEVICES

CONTRACT NO. NAS 8-20707

NOVEMBER, 1968

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PHASE I

FINAL REPORT

ESTABLISHMENT OF QUALITY AND
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CONTRACT NO. NAS 8-20767

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FINAL REPORT NAS-8-20767

I. TITLE

Establish Quality and Reliability Standards and Develop Screening Techniques for Metal Oxide Semiconductors (MOS) Microelectronic Devices.

II. PROGRAM OBJECTIVES

To identify and understand the causes of failures in MOS Microcircuits and develop standards and controls to prevent the occurrence of failures in devices used in high reliability applications.

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III. STATEMENT OF WORK

General Instrument has developed and conducted a program to collect, generate and evaluate data and information necessary to establish Quality and Reliability Standards and Reliability Screening Techniques for MOS Microcircuits. After review of the test outline with the MSFC Technical Coordinator, necessary changes were incorporated and the tasks performed.

The test program was later ammended in June of 1968 by contract modification to include a Gas Chromatograph Study and a Temperature/Bias Matrix Test.

The intent of this document is to report on the testing completed in the first phase of the contract, which includes Failure Mechanisms Summary, Temperature Storage Step Stress, Temp. Cycle Evaluation, Static Voltage Study and Gross Leak Evaluation.

The Gas Chromatograph Study and Temperature/Bias Matrix will be reported on at the completion of work covered by the contract modification. The Q and RA Specification will be completed at that time and will incorporate provisions dictated by the results of the Gas Chromatograph Study and Temperature/Bias Matrix.

A. Identification of Failure Mechanisms in MOS Microcircuits

In addition to the normal package related defects which occur in bi-polar semiconductors the MTOS device has several surface related problems which can result In poor yield or eventual failure. These surface problems are reasonably well defined in that solutions for them are known and, for the most part their effect on long term reliability has been minimized.

1. The most common defect in MTOS devices has been internal shorting of metallization patterns, causing degradation of device performance and intermittent operation. This problem has been greatly amplified by the use of very small geometry transistors in very high density designs. This combination has resulted in an average metallization width and line separation of about 0.4 mils (.0004 inches). This gives us an extremely high sensitivity to very small particles many of which cannot be detected by normal visual or x-ray examinations.

This problem has been resolved by the application of a pyrolytic glass overlay (pyro) on the surface of the device after all metallization patterns have been established. Since this glass protective layer is in place prior to die separation and assembly it also affords protection from handling damage and has a favorable effect on yield.

2. The next most common defect is electrical shorts which have been induced as the result of electrostatic discharge. This phenomena is particularly troublesome to the MOS structure. The very thing which makes the device so versatile is the reason for its extreme sensitivity to voltage transients. This is the very thin (1000 to 2000 Å) layer of silicon dioxide (SiO_2) in the gate area. This very small dimension allows a destructive build up of a voltage gradient and at relatively low voltages results in a gradient in excess of the dielectric breakdown of the material.

The most obvious solution to this problem is to protect the input leads with appropriate zener networks thereby limiting the transient voltage which will appear at the gate. This technique has been found most useful and is only limited by a) the maximum input leakage and b) speed considerations.

At present much work is being done on a "sandwich" type construction for the dielectric. Although the major benefit of these new materials has been their resistance to "fast ion" migration a pleasant side effect of some of them has been to increase the dielectric breakdown voltage. This work is being pursued by many people and is reported on in the various technical journals.

A second area for attention is the handling of the device. All devices, when they are shipped from General Instrument have all of the external leads shorted together either by a spring in the case of a transistor can or by the use of conductive foam in the package in the case of flat packs and dual-in-line packages. In addition all of the testing done at G.I. is on equipment that has been grounded and the operators are grounded while handling devices. It is never adviseable to touch any of the leads. Experience has shown that charges of up to 500 V can be supported on the human body without apparent discomfort. A charge of between 50 and 200V is quite common and even at low current densities can cause device failure.

3. The next most prevalent defect is an apparent mechanism whereby a device is out of tolerance and does not meet specification. The causes for this could be test equipment, test procedures or device degradation. The majority of the devices fail because of test equipment design or faulty test procedures. Since many of the MTOS deavices are actually performing the function of sub-systems their proper testing is no small task. In many cases the manufacturer and user both both have had to resort to a "Test Box" approach and are sometimes at the mercy of a very rough go - no/go test. In other cases the test procedure is so vaguely written that consistent test results are almost impossible to obtain.

Device degradation is exhibited in MTOS device much the same as in bi-polar devices and for much the same reasons. There is, however, fewer failures because the MTOS circuitry is more adaptive to degradation than is bi-polar circuitry. The leakage currents are usually in the pico-amp regions on an internal device and in most cases would have to go to the high nano-amps before device operation is affected and to micro-amps before the device failed catastrophically. There is no current gain per-se and slight changes in surface charge, is completely covered by aluminum and therefore is well protected.

One proven means of device stabilization is a high temperature burn-in for a short period of time. Although this is expensive many times the improved stability and resultant reliability improvement are worth the cost.

4. Another defect is poor hermeticity and is very package dependent. One problem which can have a "Time Bomb" effect is where a device is leaking in the "gray area" that is it is too leaky to be detected by Helium but not bad enough to be detected by hot oil. These have been opened after several weeks of use and found to have open aluminum and large areas of corrosion evident under the "pyro". It is apparent that the "pyro" kept the defect from being detected until the device was in equipment. The use of MIL-STD 883 test methods will completely eliminate this problem as the Gross and Fine Leak overlap in sensitivity.

NOTE: Table I contains a summary of Failure Mechanisms on devices returned from customers.

TABLE I

FAILURE MECHANISM SUMMARY

	FAILURE MECHANISM	CAUSE	EFFECT	% OF TOTAL	CORRECTIVE MEASURE
1.	Blown Gates or Protective Zener Networks	Over voltage possibly static	Inoperative Inputs	35.7	See Para. IV, 1
2.	None - Device met in-house spec. when retested	Improper Test Procedure		29.7	Test Procedure Correlation
3.	Melted Leads or Metallization	Excessive Current From Improper Bias	Inoperative Devices	10.9	Proper Handling
4.	Bad Bonds	Intermetalics, Improper Bonding	Open Circuits	8.5	100% Centrifuge
5.	Intermittent Shorts	Foreign Material	Intermittent Operation	6.5	Glass Deposition over entire device surface
6.	Miscellaneous			2.5	As Required
7.	Non-Hermetic	Poor Sealing or Mishandling	Device Degradation	1.5	100% leak test and careful handling
8.	Out of Spec.	Possible Parametric Drift or test equipment problems	Unsatisfactory Operation	1.0	Burn-In for Parameter Stability and Guard Band on Parameter Measurements

B. Temperature Storage Step Stress

A sample of 40 MEM 511's [20 each glassed (pyro) and un-glassed (non-pyro)] were subjected to a Temperature Storage Step Stress which started at 150°C and continued in 10°C steps until at least 50% of each group had failed. The time of storage at each step was 48 hours with no bias applied. Two other groups, one with 120 MEM 511's (60 each pyro and non-pyro) and 120 MEM 3020's (60 each pyro and non-pyro) were then stored for 1000 hours at 10°C less than the first failure in their respective sample. [ie: the glassed MEM 511's and MEM 3020's were stored at 10°C less than the first failure in the glassed step stress sample and the un-glassed MEM 511's and MEM 3020's were stored at 10°C less than the first failure in the unglassed step stress sample.]

The MEM 511 is a "P" Channel Enhancement Mode single transistor in a 4 lead TO-5 Package. The MEM 3020 is a 20 Bit Static Shift Register in an 8 lead TO-5 Package.

Results

Table II and III contain a summary of the results of the Temperature Storage Step Stress. The Raw Data is contained in Appendix I. The unglassed devices experienced their first failure at the 170°C step and all of the unglassed devices have completed a 1000 hour storage life test at 160°C. The first failure on the glassed devices occurred at 230°C and all of the glassed devices have completed a 1000 hour storage life test at 220°C. In order that this data will be more comparable with other testing performed in-house the storage life testing is being extended to 2000 hours at which time a full report of this phase will be made.

In order to better identify the failure cause, several samples which failed because of open bonds have been sent to the Electronic Research Center at Boston for Microprobe Analysis. Preliminary results of this analysis indicate a gold rich aluminum compound resulting from a thin ($\leq$ 2500Å) aluminum deposition.

Conclusions

The temperature storage step stress test indicates strongly that the devices with glass (pyro) on the surface are much more resistant to failure as the result of testing than are the devices without glass (non-pyro). Since all of the devices came from the same period of production and the only difference was the pyro then it can be said conclusively that the pyro, instead of being a detriment to the device, has the opposite effect. The exact reasons for this are not known at this time but this conclusion is upheld throughout all of the testing performed on this contract.

The results of the ERC Microprobe analysis have verified our own analysis and the minimum aluminum thickness has been raised to 16,000Å on all MTOS product. This was done in early spring 1968 and testing performed since has verified that this greatly minimized the bond problem.

TABLE II

SUMMARY OF FAILURES ON TEMPERATURE STORAGE STEP STRESS

DEVICE TYPE: MEM 511 (Single "P" Channel Enhancement Mode)

PACKAGE TYPE: 4 Leak, TO-5

TEMPERATURE OF STEP	NO. OF SAMPLES	NO. OF FAILURES		FAILURE REPORT NO.	FAILURE CAUSE
		Pyro	Non-Pyro		
150	40				
160	40				
170	40		1	918	Open Ball Bond (Note: 1)
180	39				
190	39		1	922	Open Ball Bond (Note: 1)
200	38		1	925	Punch Through Caused by Static
210	37				
220					
230	37	1	1	932	Open Ball Bond
240	36		1	937	Open Ball Bond
250	35				
275					
300			1	1074	Shorted Gate Caused by Static
325			1	1076	Open Ball Bond
350		1		1077	Open Ball Bond
355					
365			1	1081	Open Zener Diode Caused By Open Aluminum (Note: 2)
375			1	1081	Open Zener Diode Caused By Open Aluminum (Note :2)
400		2	6	1083	Die Lifted From Header(Note:3)
425		6		1085	Die Lifted From Header(Note:3)

NOTE: 1. These early bond failures were sent to the Electronic Research Lab at Boston for analysis.
2. The aluminum over the oxide step had opened as the result of prolonged exposure to high temperature.
3. The gold/silicon utectic temperature is ≤ 400°C

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TABLE III

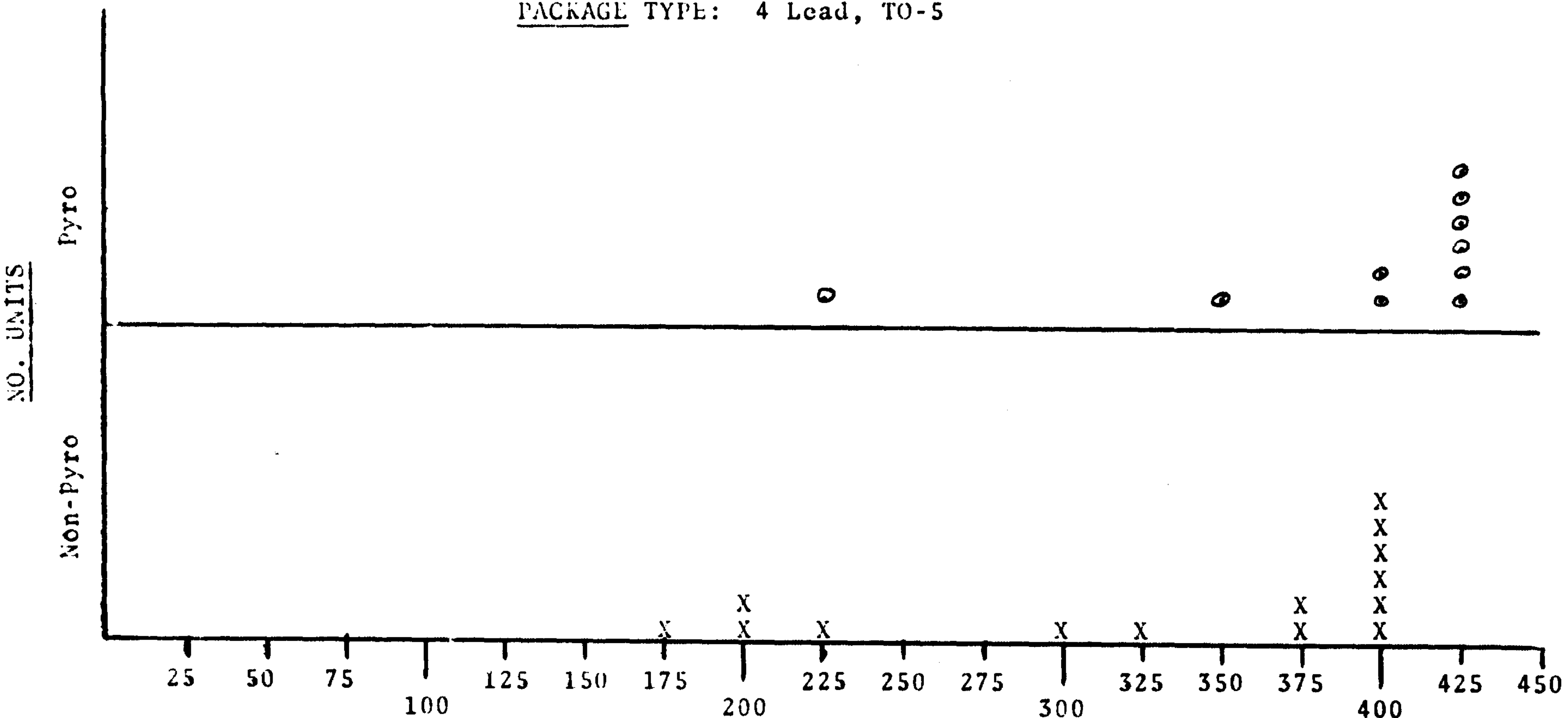
TEMPERATURE STORAGE STEP STRESS

EVALUATION NO. 1086

DEVICE FAILURES AT INDICATED TEMPERATURES

DEVICE TYPE: MEM 511

PACKAGE TYPE: 4 Lead, TO-5



C. Temperature Cycle Program

This program was conducted on two types of packages 1) 14 lead flat pack with 14 internal ball bond connections and 2) 10 lead TO-5 packages with 9 internal ball bonds. The test outline is contained in Figure I.

Results

Table IV and V contain a tabulation of the results of the Temperature Cycle Program. The raw data is contained in appendix II.

A total of 1195 devices were subjected to two series of temperature cycle with only 6 devices failing. There were no failures in the group which had previously been subjected to centrifuge.

Conclusion

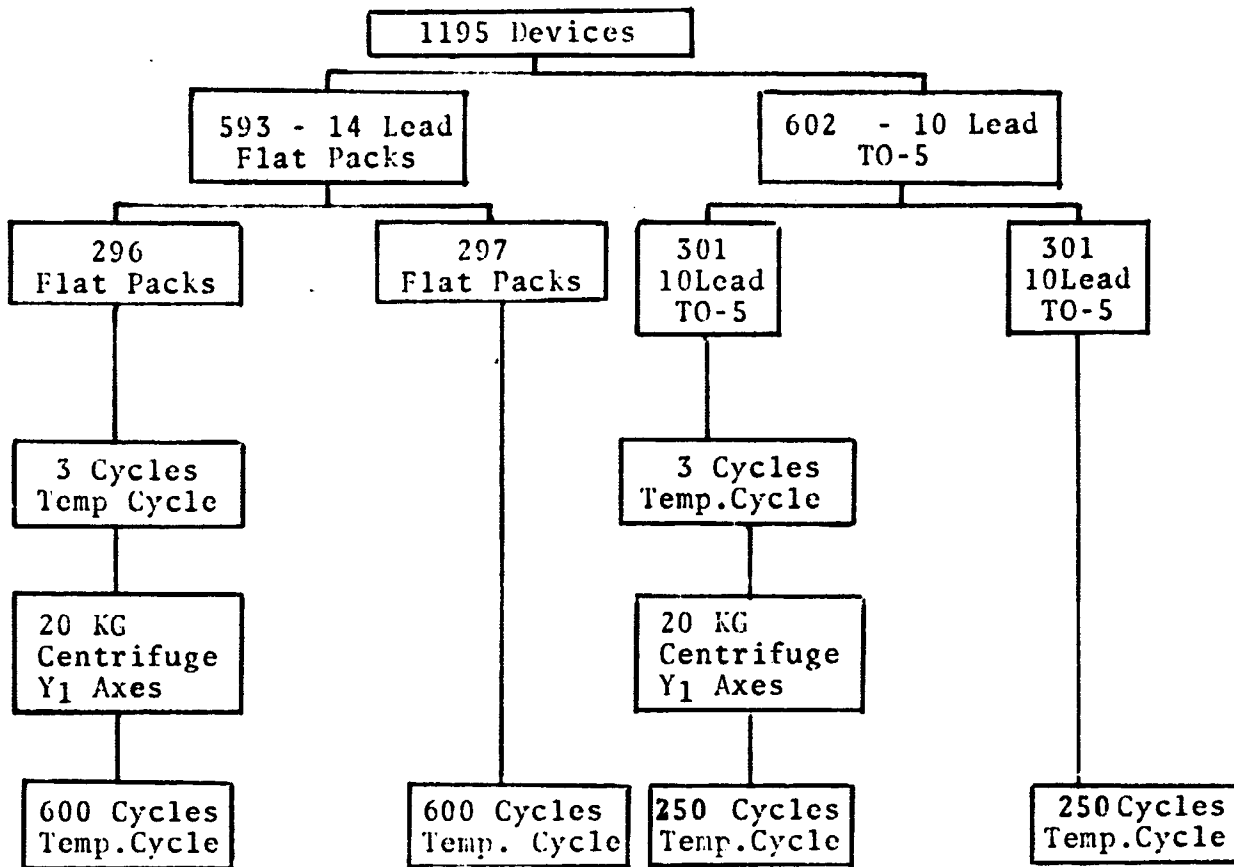
1. The 20K G centrifuge is a useful screen for culling weak bonds which may show up later as the result of a lesser stress.

2. The gold aluminum bond system is quite stable as a function of temperature cycle.

3. Centrifuge would seem to be a much faster means of detecting bad bonds than temperature cycling.

4. There was no significant difference between the performance of the flat pack and the TO header except that the flat pack took more temperature cycles to induce failure. (250 vs. 600)

FIGURE I



TEMPERATURE CYCLE PROGRAM OUTLINE

TABLE IV

SUMMARY OF TEMPERATURE CYCLE PROGRAM

PACKAGE TYPE: 14 Lead Flat Pack (Electrical Rejects MEM 2009)

NO. OF SAMPLES: 593 (296 were subjected to a 20K G centrifuge)

CUMULATIVE NO. OF CYCLES	TOTAL NO. OF SAMPLES	NO. OF FAILURES		FAILURE REPORT NO.	FAILURE CAUSE
		Cent.	No-Cent.		
3	593	1	0	824	Open Ball Bond -This device failed when subjected to 20K G stress
6	592	0	0	-	-
12	592	0	0	-	-
24	592	0	0	-	-
48	592	0	0	-	-
96	592	0	0	-	-
150	592	0	0	-	-
200	592	0	0	-	-
250	592	0	0	-	-
300	592	0	0	-	-
350	592	0	0	-	-
400	592	0	0	-	-
500	592	0	1	884	Open Ball Bond
600	591	0	1	896	Open Ball Bond

All devices failed because of ball bond lifting from the aluminum bonding pad.

TABLE V

SUMMARY OF TEMPERATURE CYCLE EVALUATION

DEVICE NO. MEM 3050

PACKAGE TYPE: 10 lead, TO-5 (9 internal ball bonds)

NO. OF SAMPLES: 602 (301 were subjected to a 20K G centrifuge)

CUMULATIVE NO. OF CYCLES	NO. OF SAMPLES	NO. OF FAILURES		FAILURE REPORT NO.	FAILURE CAUSE
		Cent.	No-Cent		
3	602	4	*	747	Open Ball Bonds
6	598	0	1	748	Open Ball Bond
9	597	0	0	-	-
18	597	0	0	-	-
24	597	0	0	-	-
48	597	0	0	-	-
96	597	0	0	-	-
150	597	0	0	-	-
200	597	0	1	761	Open Ball Bond
250	596	0	1	778	Open Ball Bond

* These were the only open bonds in the group subjected to Centrifuge and were the result of the centrifuge screen. All other failures were from the group that was not subjected to centrifuge and were caused by the ball bond lifting from the aluminum bonding pad.

D. Static Voltage Study

The purpose of this study was to investigate the feasibility of screening out those units which are particularly susceptible to damage by static voltage. This was accomplished by the charging and subsequent discharge of a small (10ps) capacitor into the device terminals.

Most of the evaluations were run on devices without the protective pyrolytic glass layer on the surface of the chip. On these devices a "healing" phenomenon was noted; that is, after a gate oxide rupture had occurred as a result of a static voltage discharge, the next such discharge would frequently burn the short open, leaving an electrically good device.

This did not occur with units covered by pyrolytic glass so that once a gate to substrate short had occurred the aluminum could not be burned open. Therefore, the use of static voltage gate stressing as a screen for "pyrolytic" devices became far more meaningful as it permitted only undamaged units to pass.

1. It appears from the results of evaluation 1048 that static discharge no only screens the weakest units, but may also damage units which survive, as evidenced by the five failures at 50 hours high temperature bias.

2. However, there is evidence that static discharge, followed by high temperature bias, will constitute a valid screen. It was observed that all the failures on the Evaluation 1048 Life Test occurred within the first 50 hours, with no failures beyond this point.

It would be worthwhile exploring the validity of this screen using much larger sample sizes and should be performed on the specific devices to be screened.

Results

The information listed below shows the results recorded from our evaluations. A block diagram of the test circuit used is shown in Figure I.

Evaluation 1041 - Fifty (50)"non-pyro" MEM 511 single devices received 100, 100 volts positive pulses. Seven (7) failed either catastrophically or the leakage readings were extremely high. The forty-three (43) remaining units were put on operating life @ 225mw/ 25°C for 1000 hours with interim data readouts with no further rejects.

Evaluation 1046 - Several "non-pyro" MEM 511 devices were stressed in the following manner. One group received negative pulses exclusively while the second group received positive pulses. The units in both groups were pulsed by discharging 100pF capacitor charged to ± 100 volts. The voltage was increased 10 volts after each pulse until the first gate to substrate short was noted. It was found that negative voltage pulses between 150 - 200 volts or positive voltage pulses between 250 - 300 volts were required to

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Evaluation 1046-Continued

initiate the dialectric breakdown between the gate metallization and the substrate.

Evaluation 1048 - Thirty-nine (39) "non-pyro" devices were stressed in the following manner. Nineteen (19) devices received 100, +150 volt pulses and twenty (20) devices received 100, -75 volt pulses. None of these devices failed and were placed on 1000 hours life test, reversed biased at Vgss = -20V/T = 125°C. Of these thirty-nine, five (5) failed at 50 hours with the remainder being still good at 1000 hours.

Evaluation 1057 - Twenty-five (25) open "non-pyro" MEM 511 devices were stressed under a microscope as follows. Twelve (12) units received negative pulses and thirteen (13) units received positive pulses. The intent was to correlate observed damage with electrical damage and amount of static charge.

It was observed that damage occurred in the gate region only where the voltage spike ruptured the thin oxide shorting the gate metallization to either source or drain.

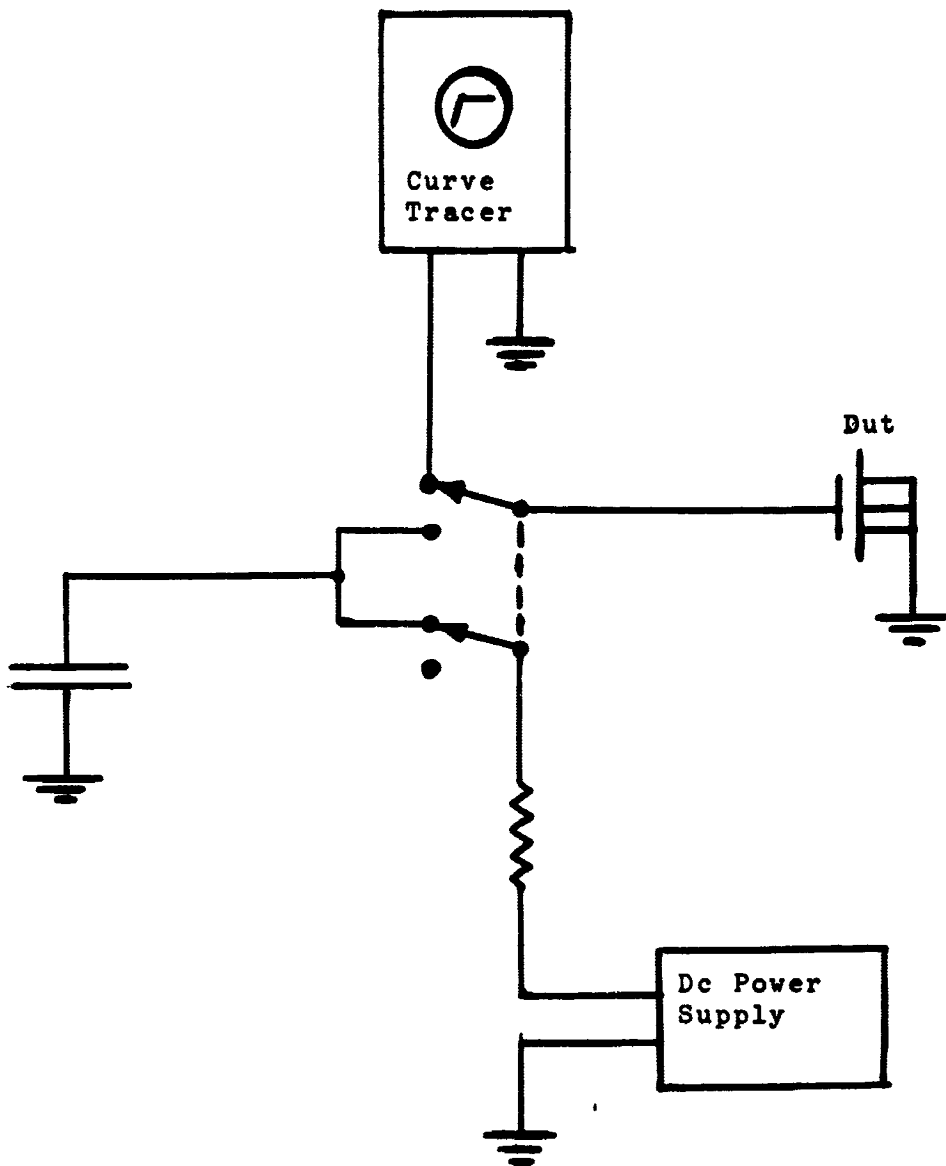
An electrical short was accompanied by a black spot on the gate metallization at the point of rupture and almost always occurred at the gate oxide step.

The physical cause of "healing" electrical shorts was noted to be the vaporization of gate metallization surrounding a shorted region.

Evaluation No. 1102 - Seventy-five (75) "pyrolytic glass process" MEM 511 devices were subjected to the same step stress tests described in Evaluation No. 1046 essentially the same results were noted; negative voltage pulses between 150 - 200 volts or positive voltage pulses between 250 - 300 volts are required to short the gate.

Conclusions

The conclusions are that there is no conclusion. That is no conclusion that would lead us to an effective screen. Instead we have embarked on an intensive study of gate input protective networks to limit the amount of a given charge that is seen by the gate.



STATIC VOLTAGE TEST SET

FIGURE NO. 2

E. Gross Leak Evaluation

An attempt was made to evaluate devices with leak rates between 1×10^{-5} cc/sec. and 1×10^{-8} cc/sec. with the hope that a more effective leak test method could be developed for detecting leak rates in this range.

Results

The study was started by the selection of devices in this leak rate range. However when these same devices were re-checked one month later the results were surprising. The leak rates of those devices with the highest rate of leakage (1×10^{-3} cc/sec.) had degraded drastically thus raising a question of the mechanical integrity of this type of device. Further review of this problem with other people in the industry and a study of available literature indicates that this is not an isolated problem and that it should be made the object of some further study.

Conclusions

1. As indicated in the Seal Integrity Conference, held at MSFC, in September, this is a Universal Problem. It is quite clouded by the fact that "Measured Leak Rate" is not always the true leak rate. Some of the papers presented at this seminar explain methods for measuring more reliably the true leak rate of devices in this range.

2. The methods described in MIL-STD 883 for Gross and Fine Leak rate measurement should cull out devices in the range of 1×10^{-3} to 1×10^{-10} cc/sec.