RESEARCH ON VARIABLE THRESHOLD TRANSISTOR STORAGE SYSTEMS

by

A. J. Lincoln, R. E. Oleksiak and T. R. Williams

FINAL REPORT – PHASE I
Contract No. NAS 12–686
October 1968

Prepared for
ELECTRONICS RESEARCH CENTER
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
CAMBRIDGE, MASSACHUSETTS

SPERRY RAND RESEARCH CENTER
SUDBURY, MASSACHUSETTS 01776

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SECTION I

SUMMARY

The metal-nitride-semiconductor variable threshold transistor (MNS-VTT) is a field effect transistor whose gate turn-on threshold can be shifted semipermanently but reversibly by application of a suitable setting potential. As such it offers promise as the storage element in an electrically alterable, nonvolatile integrated semiconductor memory array.

A number of tests were performed to allow characterization of the MNS-VTT as a memory circuit element. These tests demonstrated parameters such as permanence of storage, writing speed and voltage requirements, gain, temperature behavior, and interrogation delay.

Different memory systems' organization techniques and circuits were studied and evaluated to determine the most effective method of constructing integrated memories from the MNS-VTT's. Several experimental systems were constructed. One of these, the "channel shielded memory," was selected as the best prospect for future development.

SECTION II

INTRODUCTION

Activities under this program were centered on the use of the metal-nitride-silicon variable threshold transistor (MNS-VTT) as a digital storage element. The MNS-VTT is a field effect transistor developed at the Sperry Rand Research Center (SRRC) that is capable of nonvolatile information storage by means of reversible alteration of its gate turn-on threshold voltage.

Before and during the course of the contractual period a number of tests were carried out to qualify and quantify the behavior of the MNS-VTT as a memory device. These tests were designed to promote greater understanding of MNS-VTT performance during both writing and storage phases as a function of applied voltages, pulse duration, temperature, and elapsed time. One objective of these tests was to facilitate the development of testing procedures for future integrated memory arrays which will use the MNS-VTT as the storage element. Another objective of the testing was to provide information to allow more optimum design of the reading and writing procedures to be used in these future memories. The results of the testing program to date are described in Sec. III of this report.

A number of different configurations for organizing a digital memory based on the MNS-VTT have been considered. The objective of this work was to allow development of integrated memories that are consistent with overall system requirements, semiconductor production technology, and the particular characteristics of the MNS-VTT's themselves. Among the specific constraints affecting this development were the necessity for developing relatively high positive and negative potentials at points within a p-channel field effect transistor circuit and the requirements for high speeds in certain systems in spite of longer time constants associated with the turn-on of field effect transistors.

The two general classes of memory organization described both lead to electrically alterable nonvolatile storage systems. One class utilizes only field effect devices, both fixed and variable threshold, for ease in array integration, and the other utilizes MNS-VTT's as memory elements and bipolar transistors as drive and sense elements, to provide high speed readout. A particular system, the "3-D channel shielding technique," is described. This is the method suggested as the best candidate for further development as a fully integrated memory system. Discussion of memory organization forms is carried out in Sec. IV of this report.

SECTION III

MNS-VTT CHARACTERISTICS

The MNS-VTT is a p-channel enhancement mode insulated-gate field-effect transistor with an electrically alterable threshold. The threshold, which is roughly the gate voltage at which a channel is formed, is shifted by applying potentials across the gate insulator structure.

The effort here is to characterize the discrete MNS-VTT by means of electrical measurements made on the four leads, with the emphasis on binary memory applications. Except where noted, the substrate and source are at ground potential.

A. EFFECTS OF GATE VOLTAGE, BIAS, AND TEMPERATURE ON MNS-VTT THRESHOLD VOLTAGE

Figure 1 shows the drain-current/drain-voltage relationship in an MNS-VTT. It will be noted that a rather large gate voltage is necessary to allow current to flow from source to drain. This particular device has been forced to this condition by means of the previously mentioned ability to alter the gate threshold voltage, V_T .

The definition of V_T used in the ensuing discussion is "that gate voltage which will permit minus 100 μA to flow in the drain when the drain is biased at -5 V." This gate voltage is applied as a pulse 20 μs wide, with 0 V for 20 μs before the pulse and 0 V for 10 μs after the pulse. This pulse occurs with a period of 40 ms or longer.

Reference to Fig. 2 shows a waveform typical of those applied to the gate to obtain the threshold switching characteristic. The 20 μsec pulse is moved throughout the period of the wave and its amplitude is adjusted such as to produce 100 μA in the drain with the drain at -5 V. A plot of the pulse amplitude vs time will then result in the lower figure, which shows the typical threshold behavior throughout the period of the applied wave at the ±50 V setting amplitude.

In Fig. 3 the threshold behavior of an MNS-VTT is shown for various setting voltages, using the waveform of Fig. 2. To produce 20 V shifts in the threshold, gate voltages range from 40 to 60 V with pulse widths from 1 sec to 1 ms. Ten units from the same wafer were switched with 55 V, 10 ms pulses. Their thresholds 100 μs after the +55 V pulse ranged from +0.4 to -5.3 V with a mean of -1.58 V. The thresholds ranged from -20.8 to -25 V, with a mean of -23 V, 100 μs after the -55 V pulse.

Figure 4 shows that there will be a few volts of uncertainty in the threshold after a single +55 V, 100 ms wide pulse is applied to a device under differing initial conditions.

Several units were tested with +50 V, 100 ms pulses occurring every 200 ms. These pulses were applied for about 15 minutes. The thresholds ranged from +0.9 V to +1.8 V. Under the same conditions, but with a pulse of negative polarity, the thresholds had a range from -27.5 to -31 V (K85 - 1 batch).

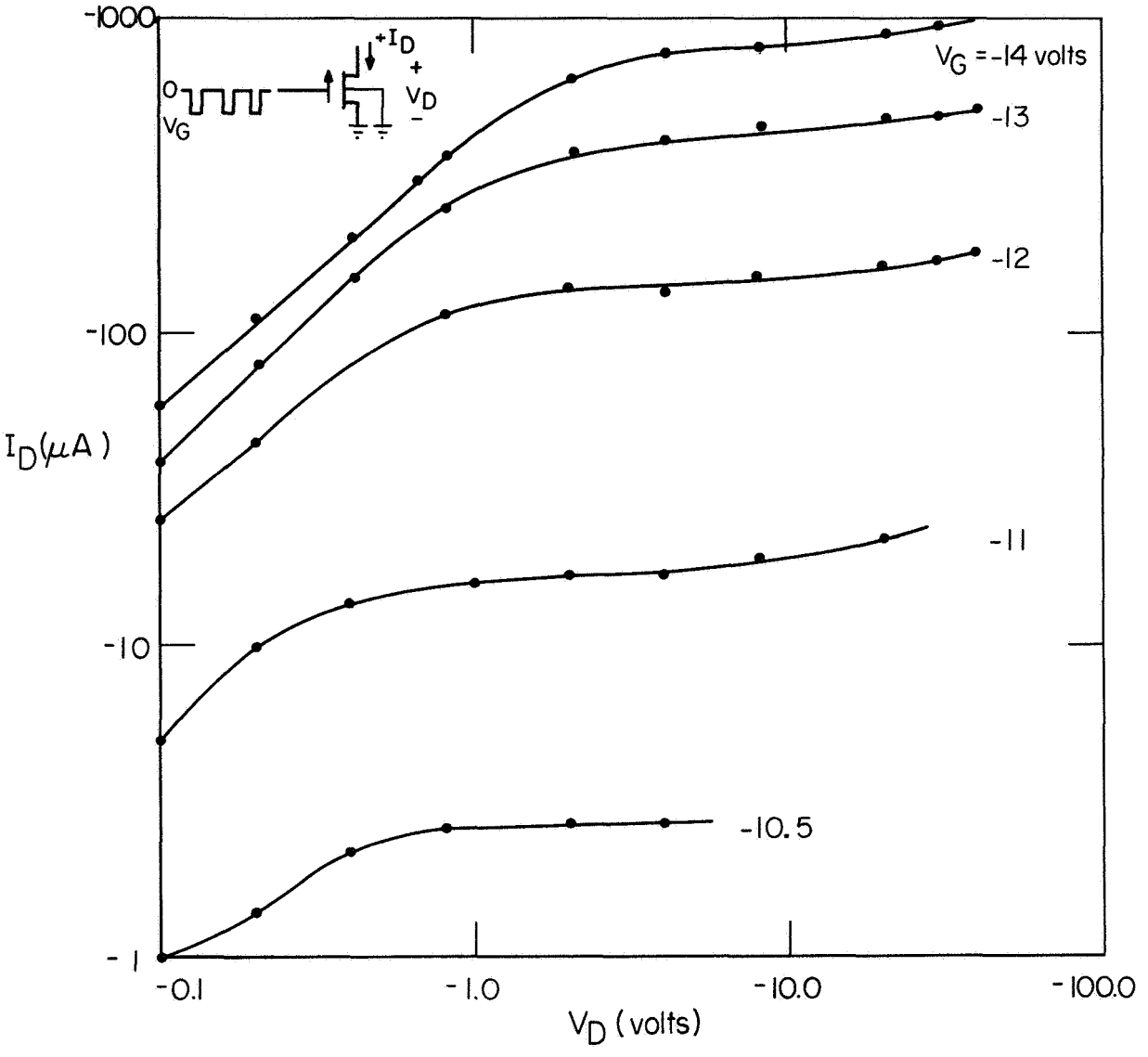

FIG. 1 Drain current-voltage characteristic of an MNS-VTT device (L18-1275).

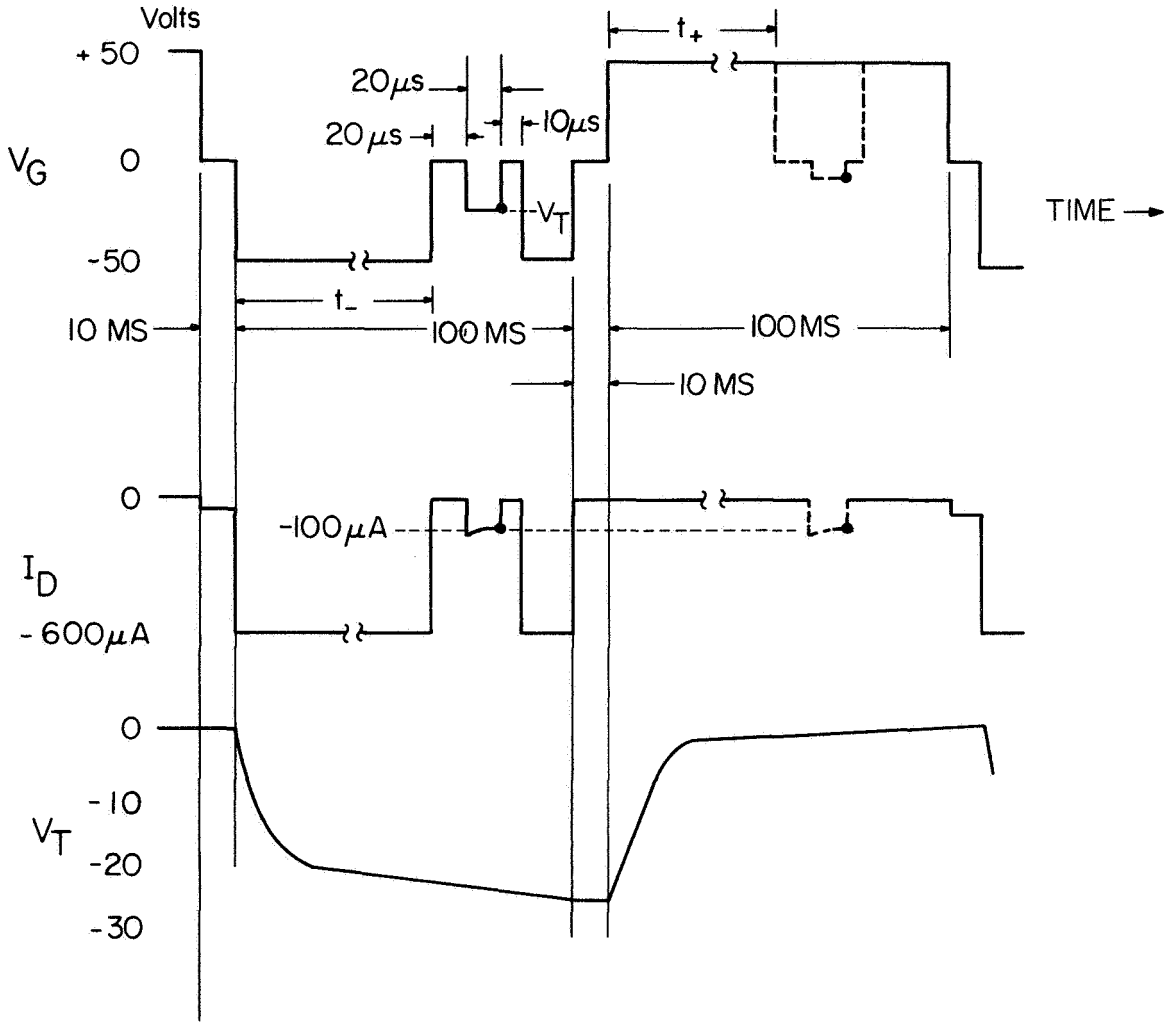

FIG. 2 Typical MNS-VTT test waveform and switching characteristic.

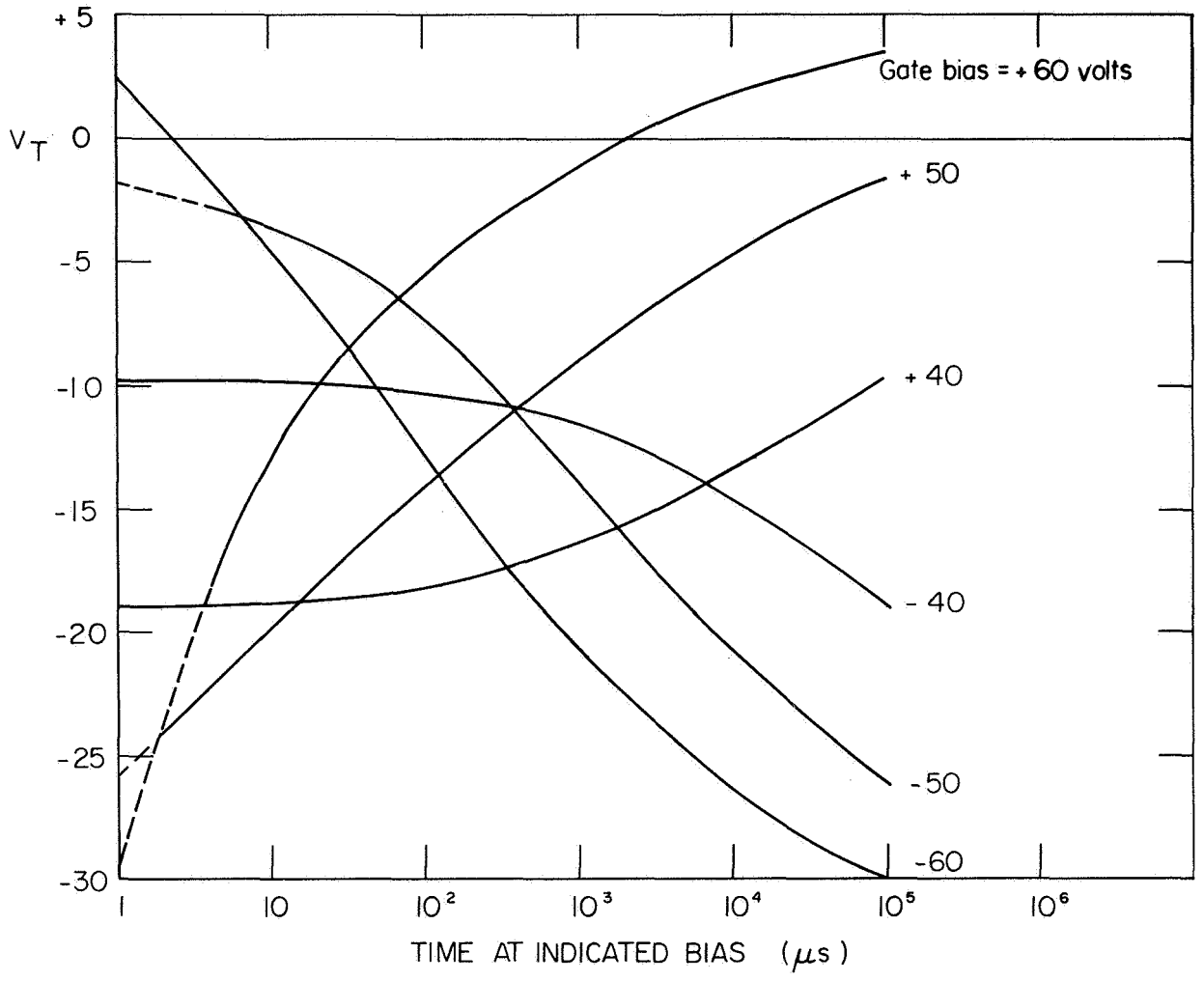

FIG. 3 Write characteristic of an MNS-VTT device (K85-1-3498).

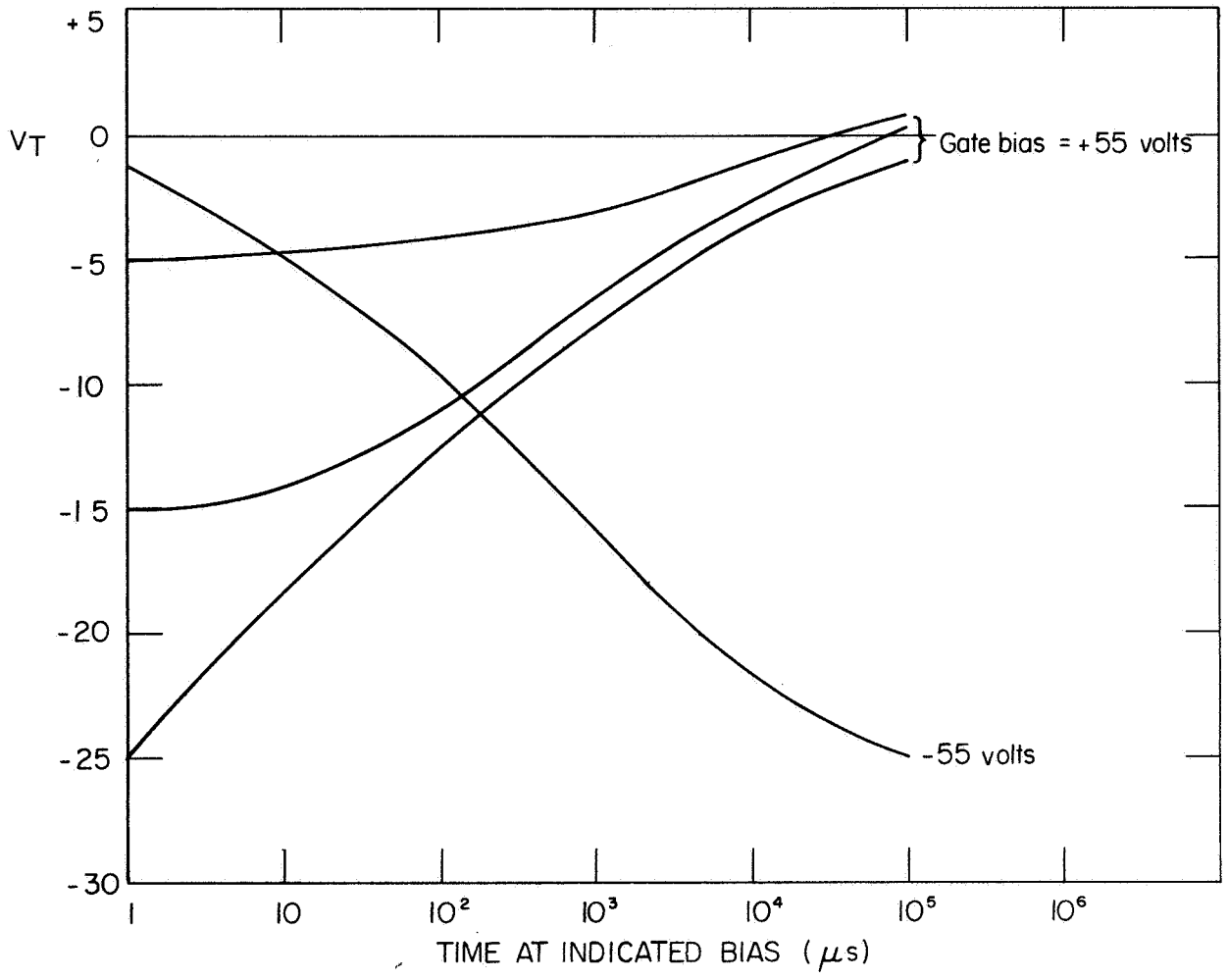

FIG. 4 Effect of initial condition on +55 V set (K85-1-3478).

In Fig. 5 a device has had its threshold shifted by 50 V, 10 ms pulses. Note that under zero bias conditions a detectable shift may remain for many orders of magnitude longer than the setting time. Also, at elevated temperatures both the write characteristic and the read characteristic are substantially unchanged. Figures 6 and 7 examine the effect of other bias voltages in the same way. Note that even under low voltages the rate at which the threshold moves is strongly voltage dependent.

Figure 8 shows how temperature affects the threshold. This temperature effect is substantially independent of the storage phenomena.

Figures 9 and 10 show the effect of temperature on devices which have been set to opposite states. The rate of change of the threshold is basically the same at 125°C as it is at 25°C. All threshold readings were made at 25°C.

It is clear that one of the problems which will flavor the performance of these devices when used as memory elements is their sensitivity to gate voltages of about 10 V. This is the voltage that will be used in many memory organizations to sample the state of the device. Figure 11 shows five different bias conditions on the gate. In all cases the device was set positively in the same way. For gate biases other than zero the device was held at zero bias until it reached a threshold of -4.3 V. It took about 15 minutes after the +55 pulse for this to occur. This is the zero of time for gate voltage conditions other than zero volts. At this time the nonzero bias conditions shown were applied to the gate. When -10 V dc is first applied to the gate, the current in the drain would be several milliamperes if the drain bias were held at -5 V (see Fig. 1). Note that after several hours the threshold has reached -9 V. This means that the current available in the drain has dropped to about 0.5 mA.

A 20 μs pulse of -10 V amplitude occurring every 100 μs is gate voltage condition "A". Note that under these conditions several days must elapse after the set pulse for the threshold to reach -9 V.

A 20 μs pulse of -10 V followed 40 μs later by a +10 V, 20 μs pulse with both pulses occurring at a 100 μs rate, is bias condition "B". Note that under these conditions it may take as long as three years to reach a threshold of -9 V. Condition "B" applied to the same device set with a -55 V, 10 ms pulse resulted in a decay rate only 10% greater than that which occurs under zero bias.

B. LONG TERM STATIC AND DYNAMIC TESTING OF MNS-VTT MEMORY DEVICES

A set of long-term static and dynamic tests has been underway on selected discrete memory devices. These will be described next. In the static tests, groups of memory transistors were set, using standard signals, to either the more positive or more negative threshold state. Their gates were then held at ground potential except during the periods when their thresholds were being measured. Threshold measurement was accomplished by monitoring source current during the application of a variable negative potential to the gate of the transistor being surveyed. The gate voltage which caused a source current of exactly 100 μA was taken to be the threshold voltage. The value of gate threshold voltage as a function of time was plotted. Typical curves for this test are shown in Figs. 12 and

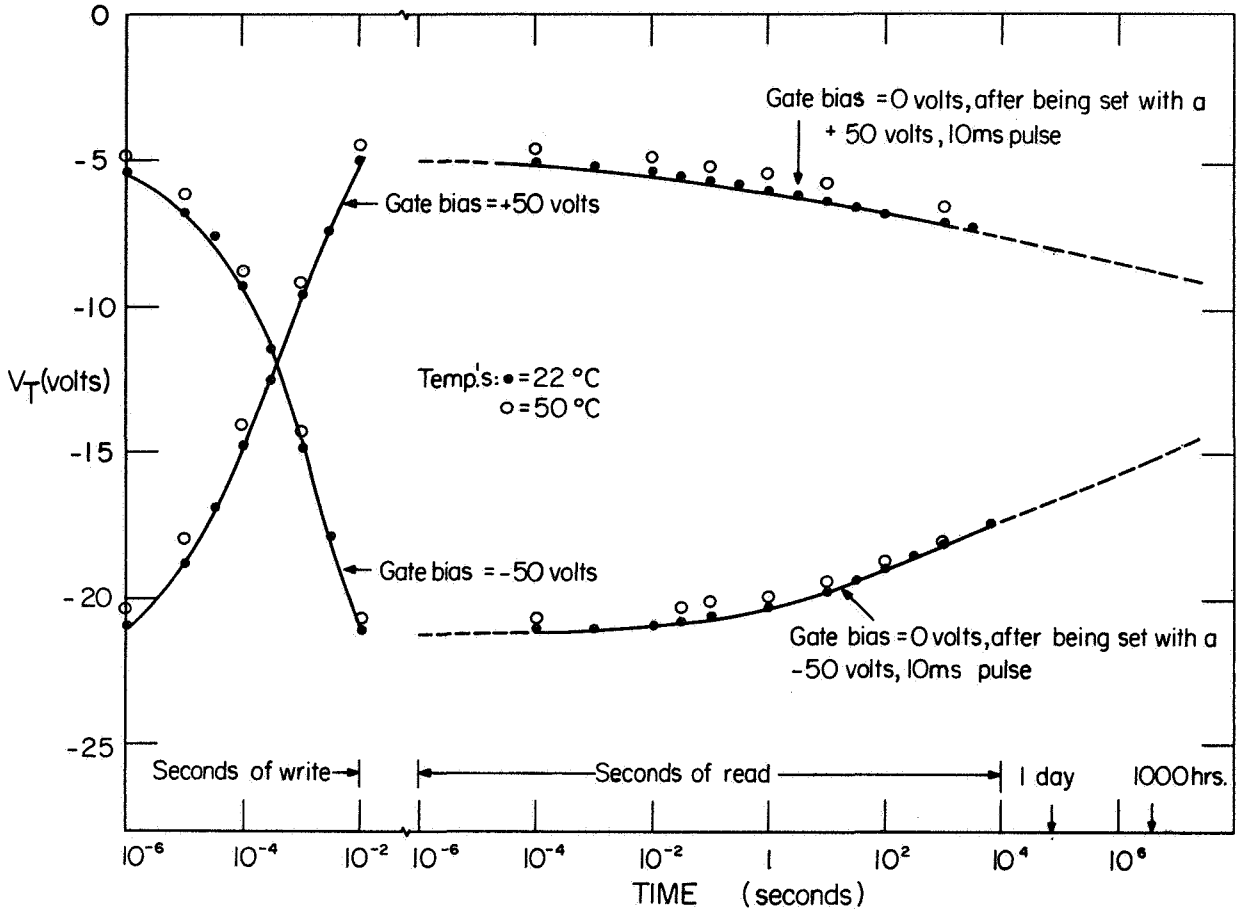

FIG. 5 Write-read characteristic for an MNS-VTT device (K126-1-4112).

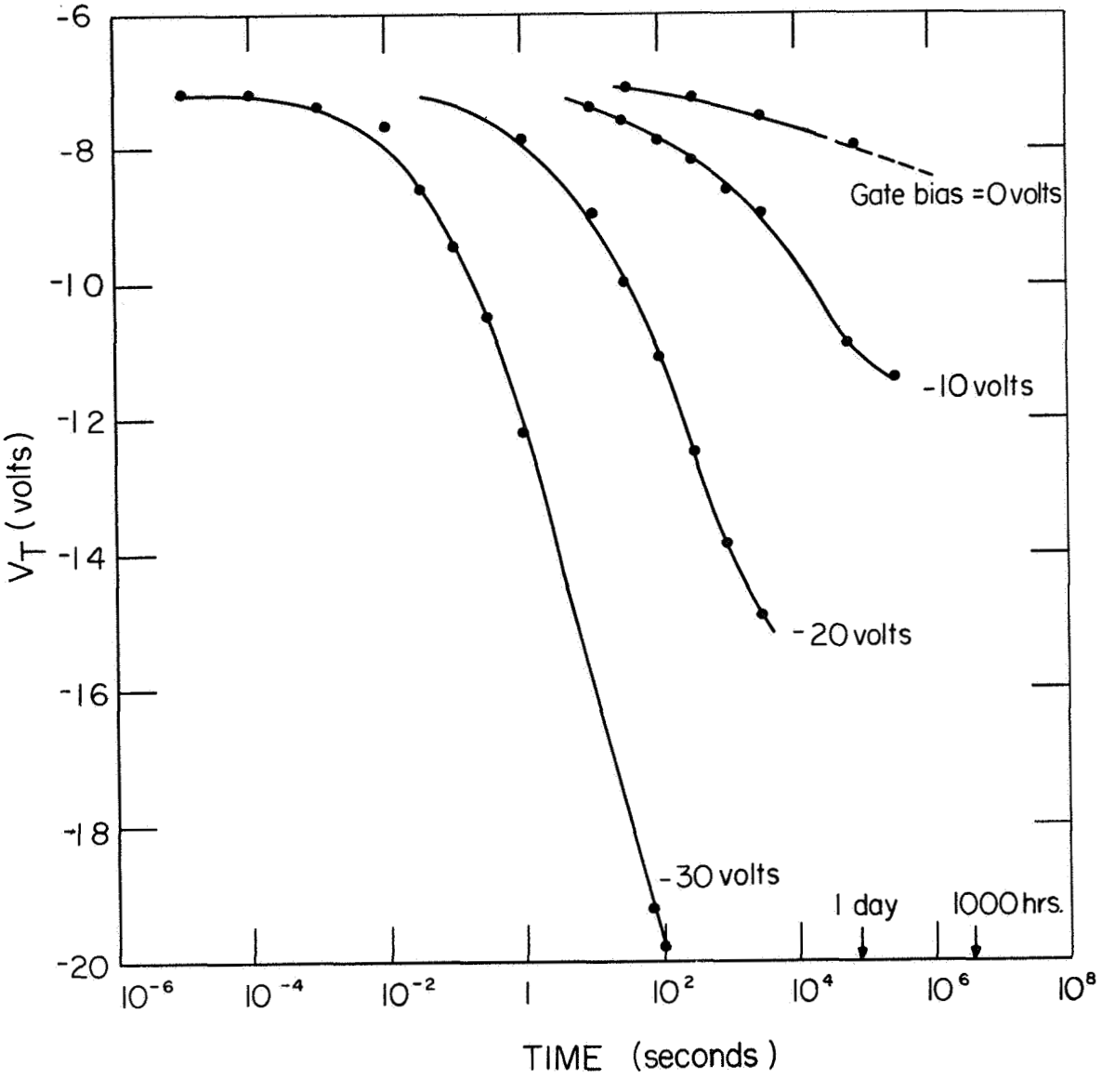

FIG. 6 Effect of gate bias on the positively set threshold of an MNS-VTT device (K85-1-3478).

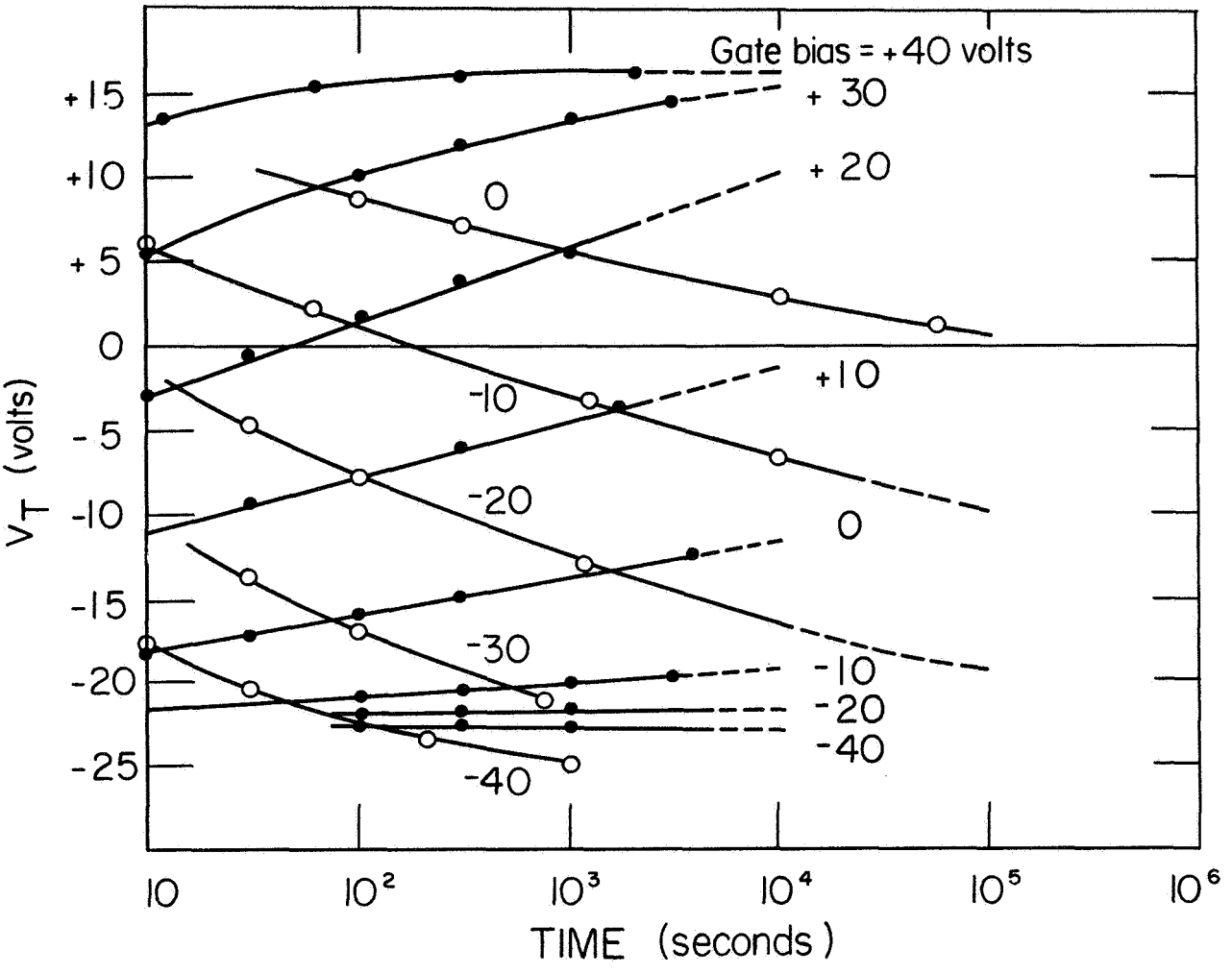

FIG. 7 Effect of gate bias on the positively set and the negatively set MNS-VTT device (L18-1-1275).

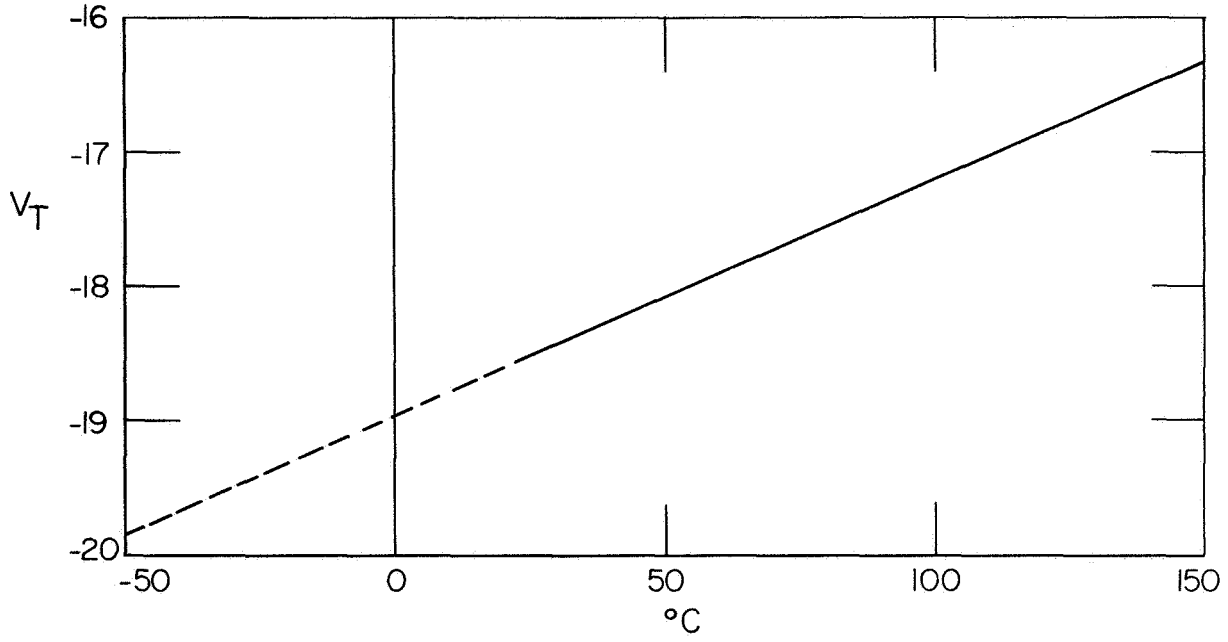

FIG. 8 Effect of temperature on the threshold (V_T) of an MNS-VTT device (K126-1-4112).

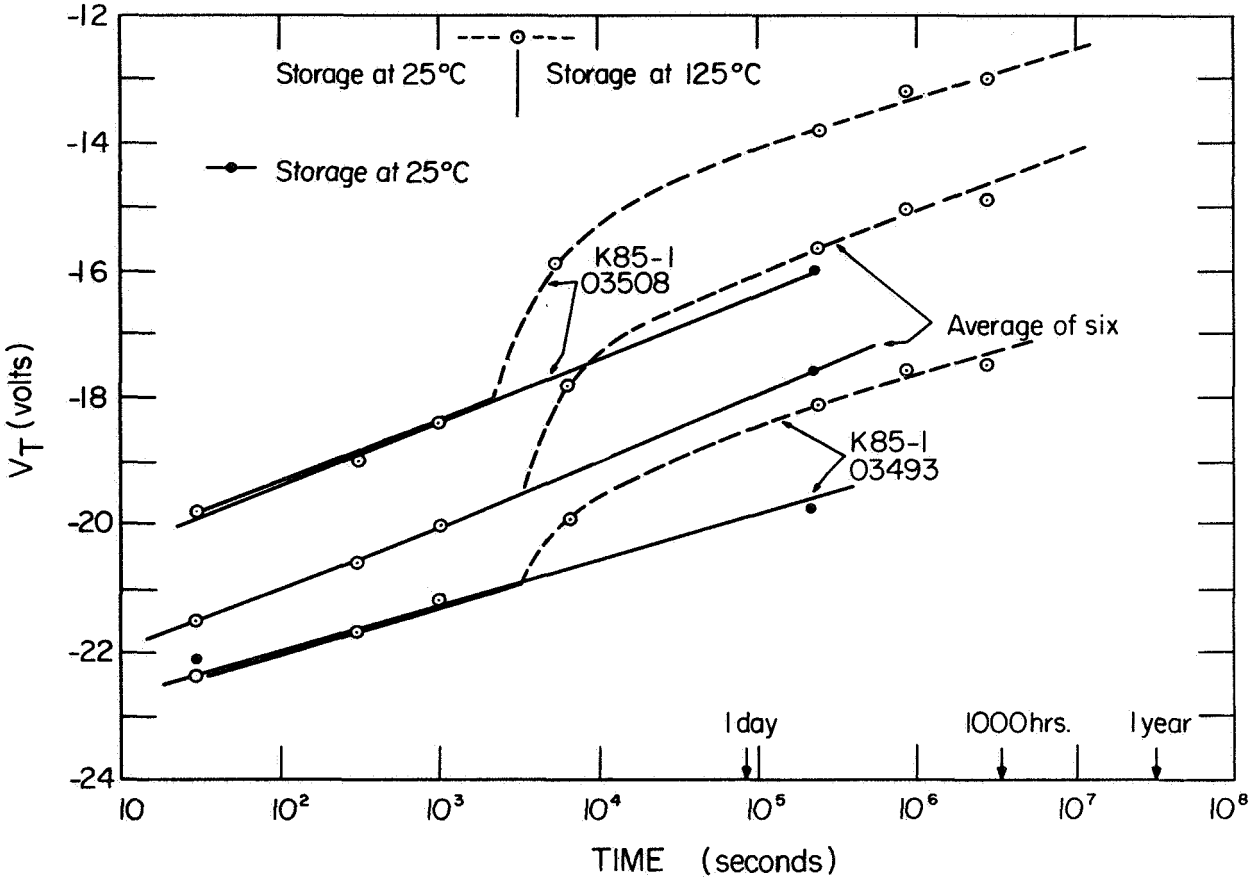

FIG. 9 Temperature effect on MNS devices set negative. All threshold readings at 25°C.

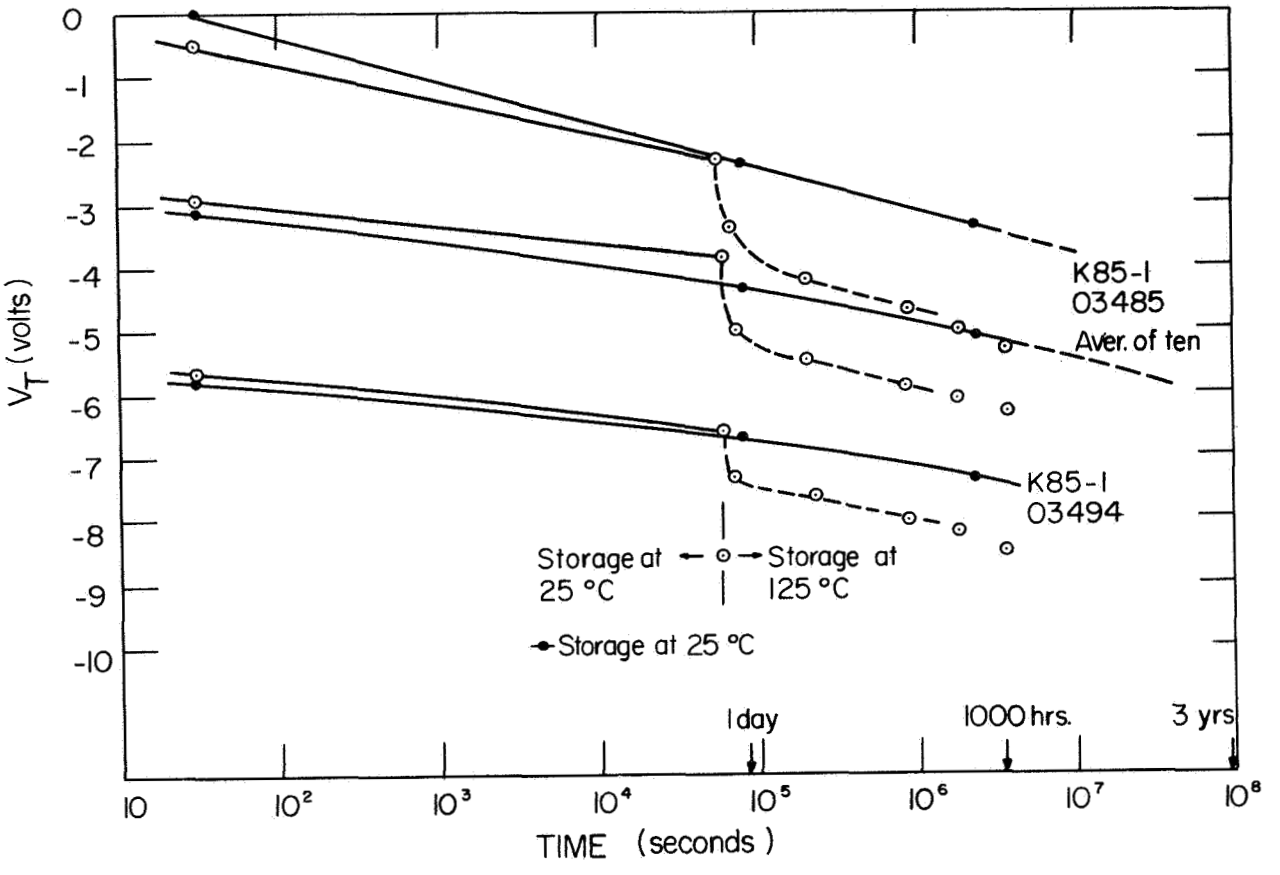

FIG. 10 Temperature effect on MNS devices set positive. All threshold readings at 25°C.

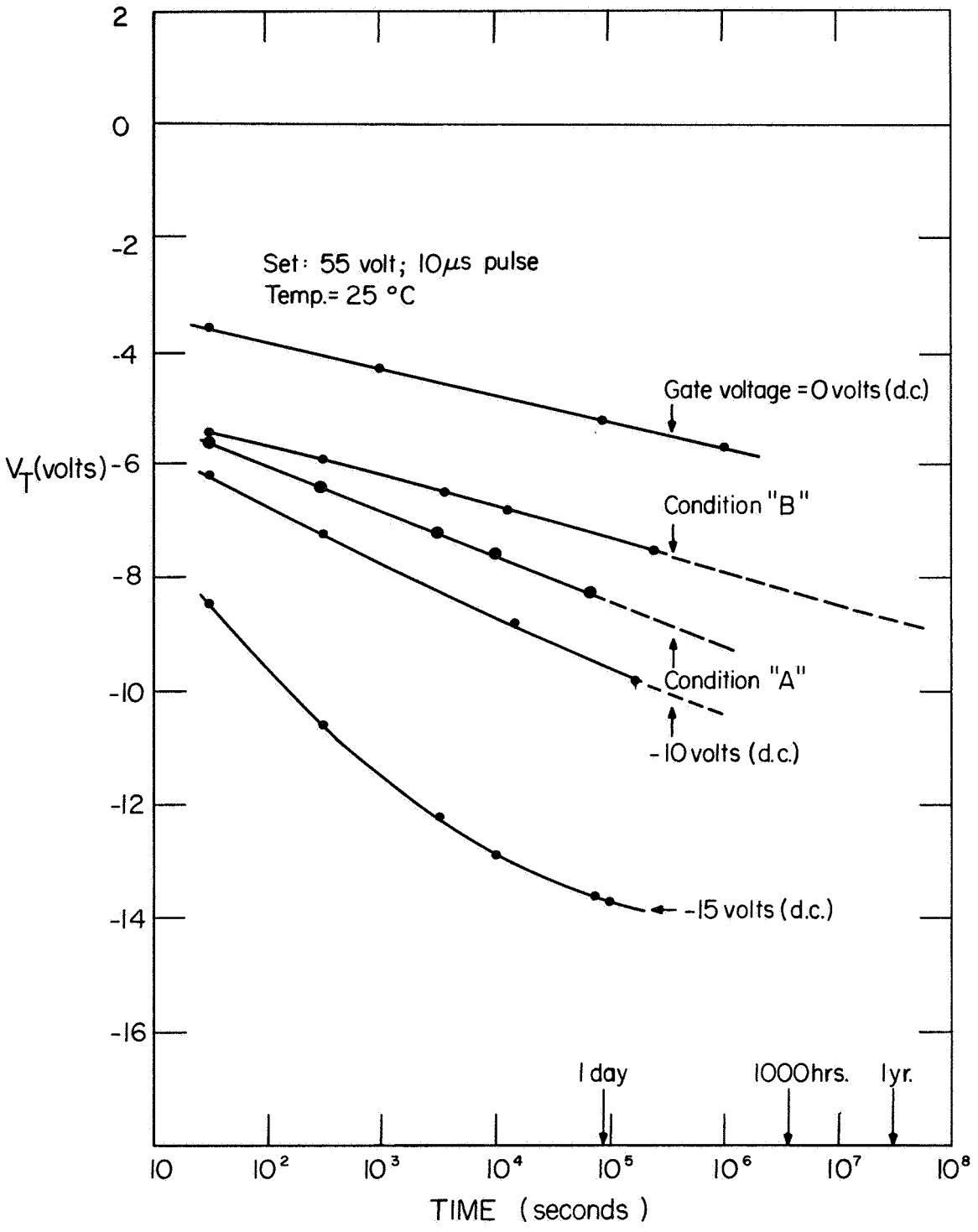

FIG. 11 Effect of gate voltage on threshold (V_T) of an MNS-VTT device (K126-1-4105).

13. It may be seen that thresholds vary approximately linearly with the logarithm of time.

In the pulsed operation tests, the memory transistors were set as in the static tests, but were stored under conditions of constant interrogation. The interrogating pulse was rectangular, with an amplitude of -10 V, a period of 10 μs and an on time of 2.5 μs. The threshold was measured by disconnecting the transistor from the constant amplitude pulse source and supplying a variable amplitude pulse to its gate. The pulse amplitude which caused 100 μA to flow in the drain was taken to be the turn-on threshold. Curves for this test are shown in Figs. 14 and 15. The behavior of transistors during pulsed testing was similar to that during the static tests, except that threshold decay was generally more rapid.

The results of the static and pulsed tests are summarized in Table I below. The values of $V(T_0)$ are the extrapolated initial voltages at 0.1 hr after setting. The extrapolation is based on the intersection of a best-fit straight line with the 0.1 hr ordinate. The values of λ are the slopes of the best-fit straight lines given in volts/decade. The static-reversed test was one in which the transistors were initially set to one state and observed for the period given, and then set to the opposite state and measured.

TABLE I

Long Term Static and Dynamic Test Results for MNS-VTT's

Test	Device Number	State	Duration Hours	$V(T_0)$ (volts)	λ (volts/decade)
Static	K65-1 2379	-	2500	-33.4	1.16
	K65-1 2335	+	2500	- 3.9	-0.62
	K85-1 3488	-	2500	-29.8	1.24
	K85-1 3511	+	2500	- 2.8	-0.60
	K85-1 3496	-	2500	-30.7	1.10
	K85-1 3505	+	2500	- 6.2	-0.44
Static, Reversed	K65-1 2362	-	2500	-27.0	1.00
	K65-1 2362	+	600	- 3.6	-0.72
	K65-1 2357	-	600	-29.6	1.08
	K65-1 2357	+	2500	- 3.4	-0.82
Pulsed	K86-1 3100	+	2500	- 2.2	-0.92
	K86-1 3102	-	2500	-22.4	1.34
	K86-1 3101	-	2500	-22.8	1.64
	K85-1 2336	+	2500	- 5.8	-0.38
	K65-1 2330	-	2500	-25.8	1.72
	K65-2 2576	+	2500	- 3.6	-0.76
	K65-2 2528	-	2500	-16.7	1.00
	K54-4 3115	+	2500	- 7.3	-0.44
	K54-4 3120	-	2500	-25.6	1.20

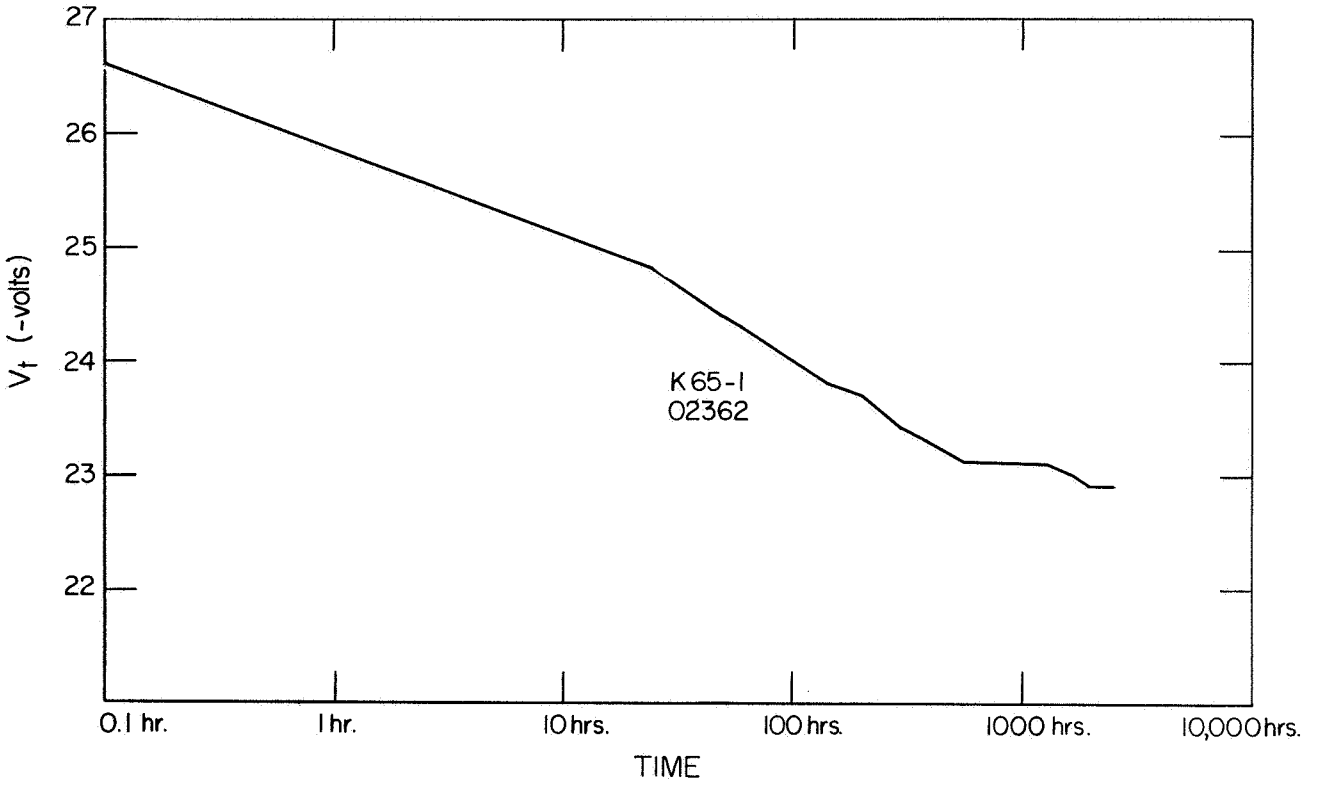

FIG. 12 Long-term static test, negative set condition (device No. K65-1-2362).

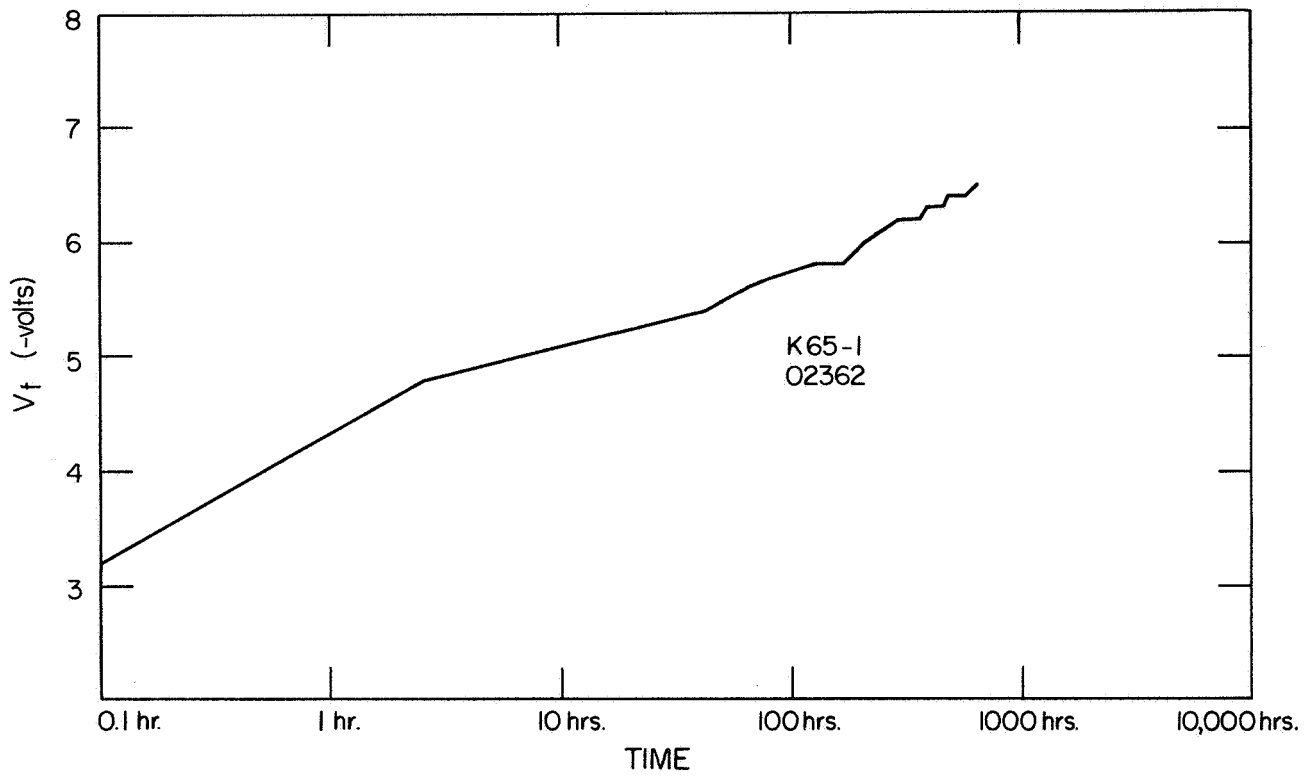

FIG. 13 Long-term static test, positive set condition (device No. K65-1-2362).

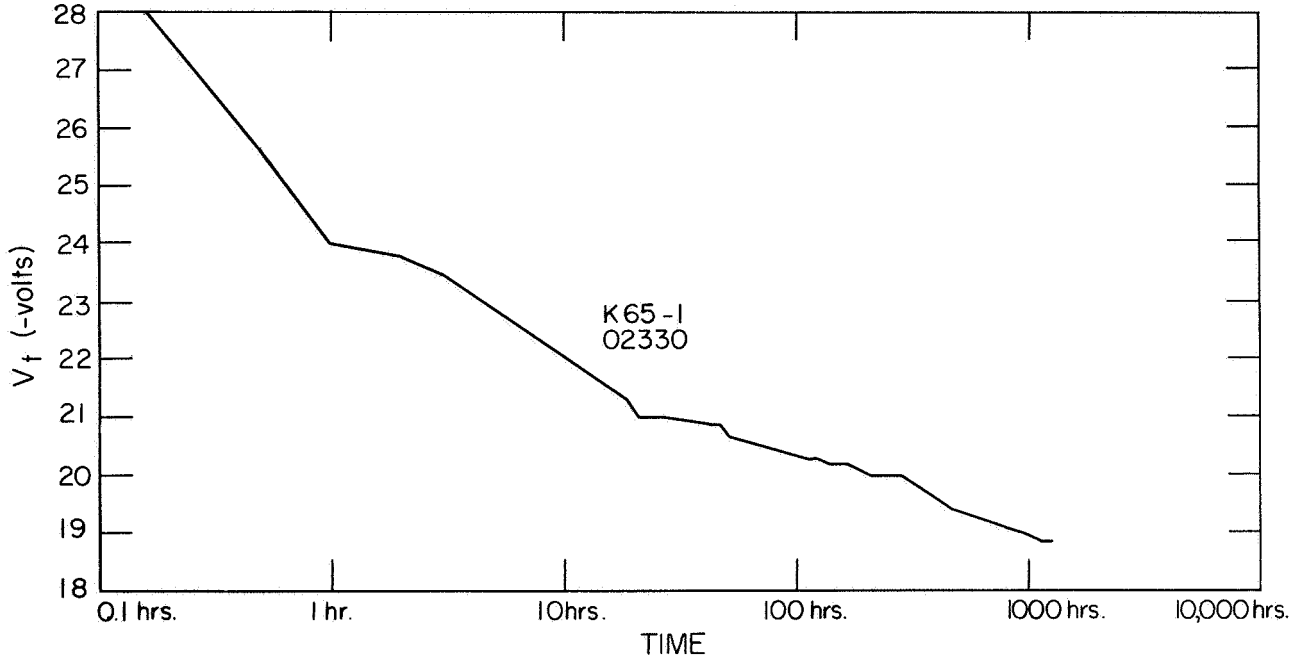

FIG. 14 Long-term pulsed test, negative set condition (device No. K65-1-2330).

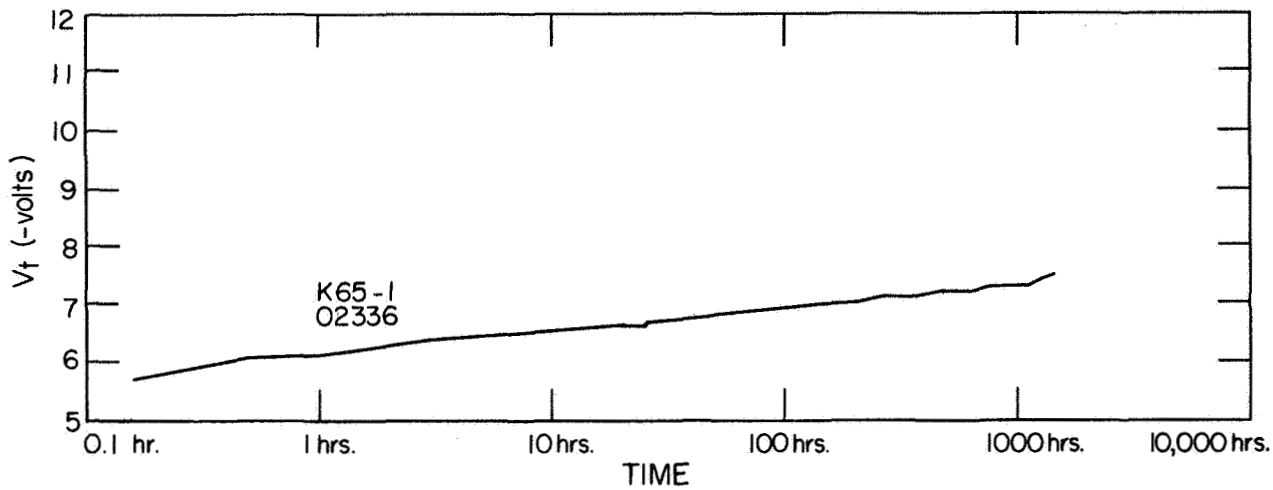

FIG. 15 Long-term pulsed test, positive set condition (device No. K65-1-2336).

It is possible to use the threshold decay curves of Figs. 12 and 13 to make a rough estimate of storage persistence. These curves indicate that the threshold voltage in both the positive and negative set conditions varies approximately linearly with the logarithm of time. Thus, for the negative set condition

$$V_0(t) = V_0(T_0) + \lambda_0 \log \left(\frac{t}{T_0}\right) \qquad \lambda_0 > 0 \tag{1}$$

and for the positive condition

$$V_1(t) = V_1(T_0) + \lambda_1 \log \left(\frac{t}{T_0}\right) \qquad \lambda_1 < 0 \tag{2}$$

Let the gate threshold be $V_0(t)$ when the transistor is set to the ZERO state and $V_1(t)$ when it is set to the ONE state. An appropriate gate interrogation voltage is one which will allow suitable ONE-ZERO discrimination throughout the useful storage lifetime. If the condition of more positive threshold voltage is considered to be equivalent to a stored ONE, then sensing of a ONE implies the larger current flow through the storage transistor. The necessary magnitude of this current is determined by other circuit requirements such as speed, output loading, and allowable power dissipation. Let the drain current, I_d, be given by the approximate equation

$$I_d = g_m\left(V_g - V_t\right) \tag{3}$$

where g_m is the transconductance, V_g is the gate-to-source interrogation voltage, and V_t is the gate threshold voltage. If I_0 is the maximum allowable drain current with V_g applied to the gate when the transistor has been set to the ZERO state and, similarly, I_1 is the minimum allowable drain current when the transistor has been set to the ONE state, the condition for suitable ONE-ZERO discrimination at the output may be expressed by

$$I_0 = kI_1 \tag{4}$$

for some k, $0 < k < 1$.

The discussion so far has made no allowance for deviations in device parameters or supply voltages. The general effect of such deviations is to cause a shortening of storage life. The most serious deviations, namely those of V_g and temperature, may be approximately accounted for by the analysis which follows.

Consider the worst condition of g_m and V_g variation. This is when current flowing in an interrogated transistor storing ZERO is at its maximum value and the current flowing in an interrogated transistor storing ONE is at its minimum. Let these two conditions be denoted by the following equations.

$$I_0 = g_{m,max}\left(V_{g,max} - V_0(t)\right) \tag{5}$$

$$I_1 = g_{m,min}\left(V_{g,min} - V_1(t)\right) \tag{6}$$

Let the tolerance of g_m be σ and that of V_g be δ. Then

$$g_{m,min} = (1 - \sigma)g_m \tag{7}$$

$$g_{m,max} = (1 + \sigma)g_m \tag{8}$$

$$V_{g,min} = (1 - \delta)V_g \tag{9}$$

$$V_{g,max} = (1 + \delta)V_g \tag{10}$$

Also, let the value of time at end of storage be T_ℓ. Then from Eqs. (5) and (6),

$$V_0(T_\ell) = (1 + \delta)V_g - \frac{I_0}{(1 + \sigma)g_m} \tag{11}$$

$$V_1(T_\ell) = (1 - \delta)V_g - \frac{I_1}{(1 - \sigma)g_m} \tag{12}$$

and from Eqs. (1) and (2)

$$V_0(T_\ell) = V_0(T_0) + \lambda_0 \log \frac{T_\ell}{T_0} \tag{13}$$

$$V_1(T_\ell) = V_1(T_0) + \lambda_1 \log \frac{T_\ell}{T_0} \tag{14}$$

Equating Eq. (11) with Eq. (13) and Eq. (12) with Eq. (14), and then solving for T_ℓ and V_g, we obtain

$$T_\ell = T_0 \log^{-1} \left\{ \left[V_1(T_0) - V_0(T_0) + \left(\frac{1}{1-\sigma} - \frac{k}{1+\sigma} \right) \frac{I_1}{g_m} + \delta \left(V_1(T_0) + V_0(T_0) \right. \right. \right.$$

$$\left. \left. \left. + \left(\frac{1}{1-\sigma} + \frac{k}{1+\sigma} \right) \frac{I_1}{g_m} \right) \right] D \right\} \qquad (15)$$

and

$$V_g = \left[\lambda_0 V_1(T_0) - \lambda_1 V_0(T_0) + \left(\frac{\lambda_0}{1-\sigma} - \frac{\lambda_1 k}{1+\sigma} \right) \frac{I_1}{g_m} \right] D \qquad (16)$$

where

$$D = \left[\lambda_0 - \lambda_1 - \delta \left(\lambda_0 + \lambda_1 \right) \right]^{-1} \qquad (17)$$

For the case where the tolerances assigned to V_g and g_m are zero,

$$T_\ell = T_0 \log^{-1} \left\{ \left[V_1(T_0) - V_0(T_0) + (1 - k) \frac{I_1}{g_m} \right] \left[\lambda_0 - \lambda_1 \right]^{-1} \right\} \qquad (18)$$

and

$$V_g = \left[\lambda_0 V_1(T_0) - \lambda_1 V_0(T_0) + \left(\lambda_0 - \lambda_1 k \right) \frac{I_1}{g_m} \right] \left[\lambda_0 - \lambda_1 \right]^{-1} \qquad (19)$$

An example of storage persistence will be shown using data from Table I for device K65-1 2357 under zero gate bias conditions. The parameters used are:

$$I_1 = -1.0 \times 10^{-3} \text{ A}$$

$$g_m = 500 \times 10^{-6} \text{ mho}$$

$$k = 0.1$$

$$T_0 = 0.1 \text{ hr}$$

$$\lambda_0 = 1.08 \text{ V/decade}$$

$$\lambda_1 = -0.82 \text{ V/decade}$$

$$V_0(T_0) = -29.6 \text{ V}$$

$$V_1(T_0) = -3.4 \text{ V}$$

Inserting these values into Eq. (18), the value of T_ℓ with no parameter variations is found to be 7.1×10^{11} hr. If 10% tolerances are allowed for V_g and g_m, then $\delta = \sigma = 0.1$ and the value of T_ℓ is found to be 1.0×10^{10} hr. Figures 9 and 10 show that temperature variations may be accounted for approximately by adding fixed values to $V_0(T_0)$ and $V_1(T_0)$. These values, in the worst case observed, are $V_0 = 2.2$ V and $V_1 = -1.6$ V. Using these new values of initial voltage, T_ℓ is found to be 1.1×10^8 hr.

The example shown here is for the static storage case in which very low interrogation duty cycles are used. If higher duty cycles are analyzed, then curves such as Figs. 14 and 15 should be used for device parameters. Clearly, under single polarity interrogation, storage persistence is reduced. It should also be noted that these calculations are the result of approximate and sometimes extreme extrapolations and should merely be used to give some sense of the expected behavior rather than precise evaluations. A number of factors were not taken into account here. Among the two most important ones omitted are the statistical variations of threshold characteristics from device to device and the behavior of g_m with temperature. A more exact analysis would include these factors (although the device-to-device variations within an array are not capable of being estimated at this time).

SECTION IV

STUDY OF METHODS OF ORGANIZATION OF MNS MEMORIES

A number of alternative forms of organization have been considered for MNS electrically alterable nondestructive read-out (EANDRO) memories. Each of these forms has different implications with respect to interrogation, data insertion, or memory partitioning. The main requirements of any interrogation technique are that the access to stored information be suitably rapid and that the particular interrogation technique give rise to minimal degradation of the stored information. The task of data insertion is complicated by the fact that storage of binary information requires that both positive and negative potentials of moderately high amplitudes be appliable across the gate insulation region of the MNS storage devices. The goal in the design of each of the different data insertion techniques was to develop the necessary signals with the simplest circuitry and with minimal voltage stress applied throughout the memory. The results of the study of different memory organization forms will be discussed in this section.

A. COINCIDENT VOLTAGE WRITE SELECTION MEMORY

The coincident voltage write selection memory shown in Figs. 16, 17, 18, and 19 employs VTT's as memory elements and fixed threshold IGFET for all other functions. In this unit, writing is accomplished by means of a two-phase coincident voltage technique which makes use of the fact that the voltage applied between gate and substrate must exceed a threshold level before any significant change of V_T can take place within the time of the write pulse. The ZERO's are written during the first phase and the ONE's during the second. To write ZERO's, a negative voltage slightly lower than the threshold amplitude is placed on the common gate lead of the selected word. Gates of unselected words are held at ground potential, and the substrate of each bit which is to be driven to ZERO is connected to a positive voltage slightly lower in amplitude than the setting threshold. Bits which are not to be driven to ZERO have their substrates held at ground. In this way, a positive potential of about twice the setting threshold appears across the gate-to-substrate region in all memory cells of the selected word which are to be driven to ZERO, but in all unselected cells or cells that are to be driven to ONE, the maximum voltage appearing across the gate-substrate region is less than the setting threshold. During the second phase, ONE's are written by a similar procedure except that now positive voltages are applied to the selected gates and negative voltages to the substrates, causing a negative gate-to-substrate voltage of twice the setting threshold.

Interrogation is obtained by applying a negative pulse having an amplitude between the ONE and ZERO turn-on threshold to the common gate line of the selected word. All devices in the selected word which store ONE's will conduct, causing a positive voltage change on the bit output lines,

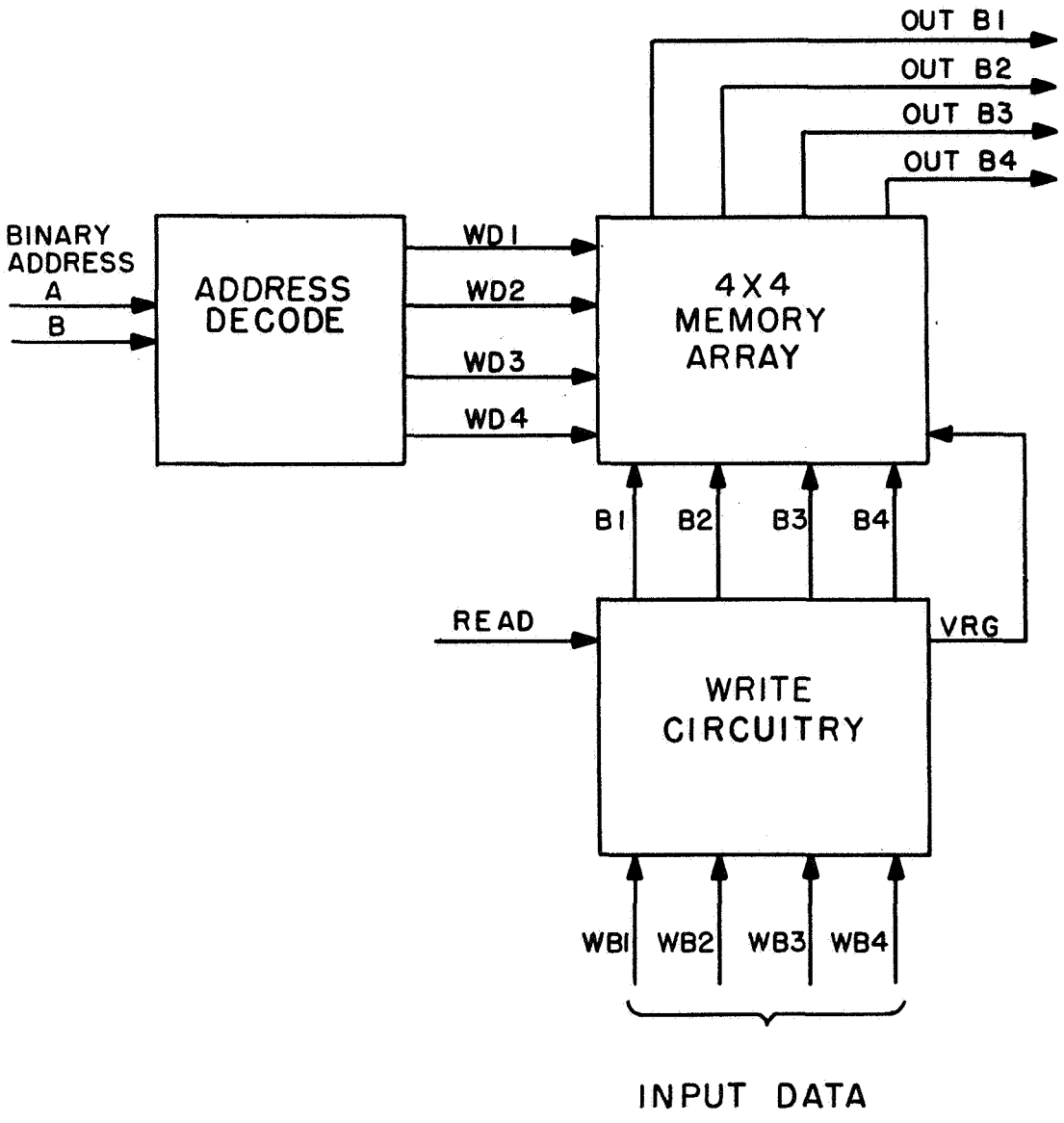

FIG. 16 Block diagram of 4 x 4 coincident select memory.

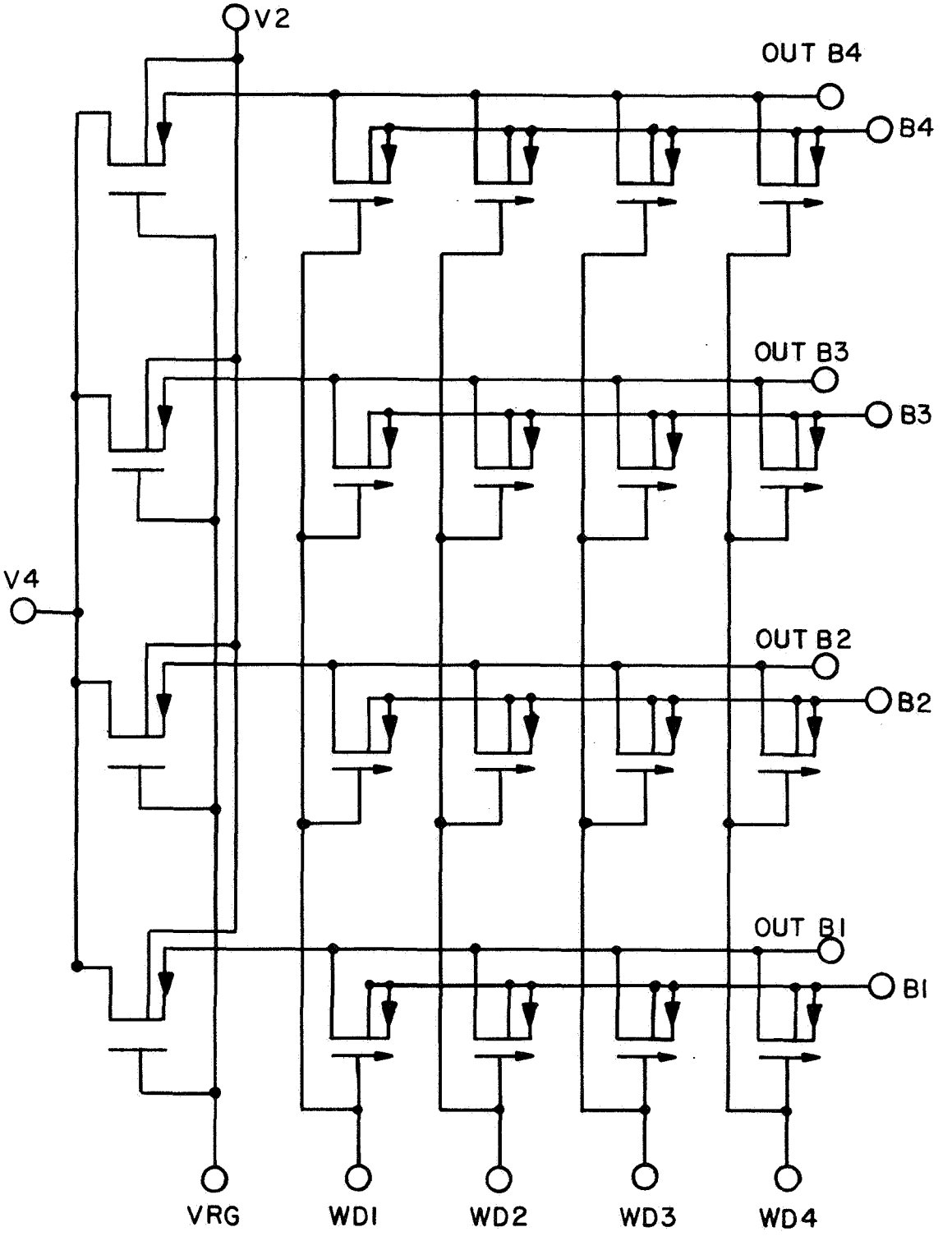

FIG. 17 4 x 4 coincident select memory array.

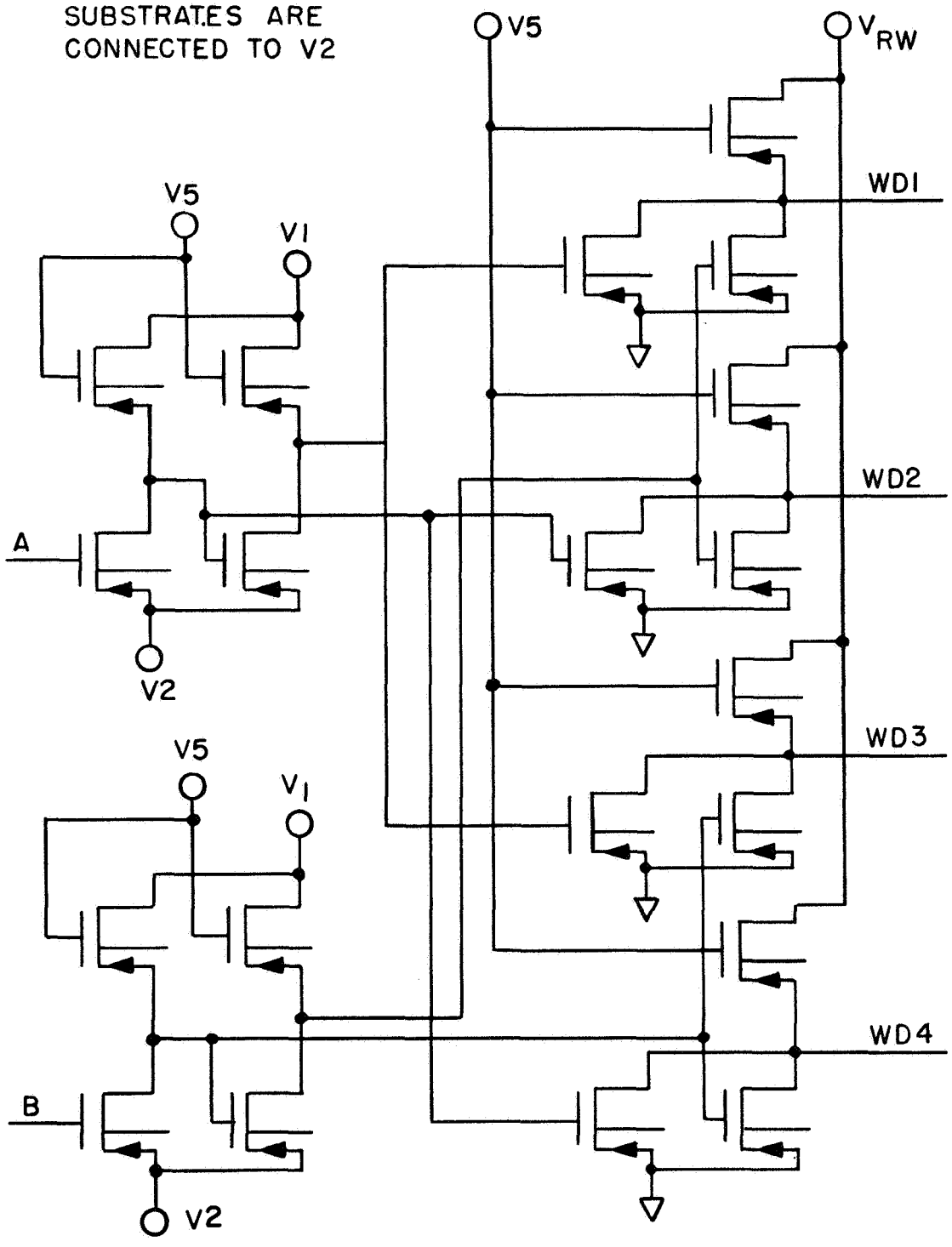

FIG. 18 Address decode.

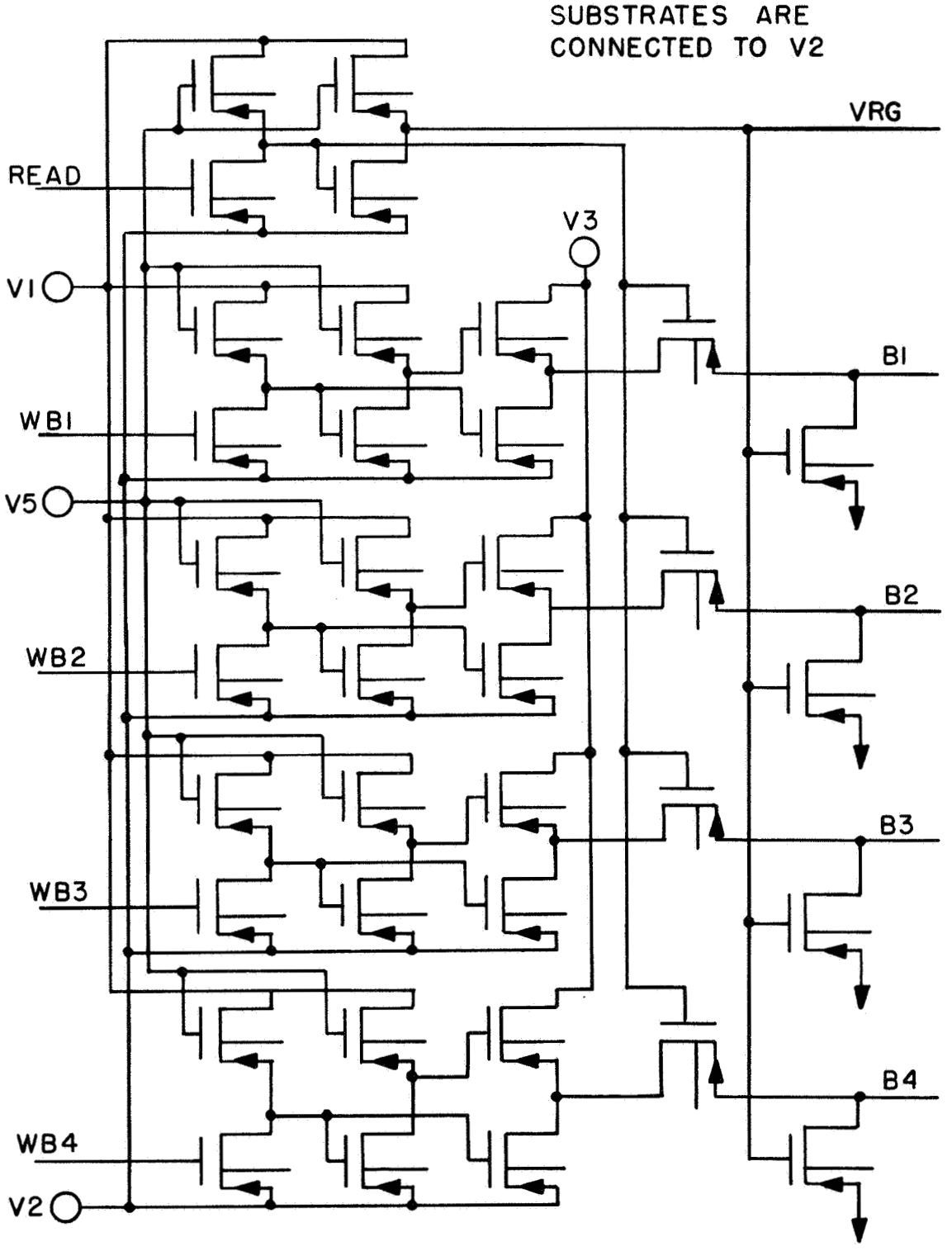

FIG. 19 Write circuitry.

whereas devices storing ZERO's will remain unconducting, with no resultant change in level on their output lines.

A 4 x 4 discrete version of this memory was constructed and capacitance was added to simulate conditions which would exist in a 16 x 16 array. A 10 ms setting pulse duration was used, and read-cycle times were about 1 μs. Tests were run on this memory to determine the effect of repeated application of half-select voltage pulses of polarity chosen to erase the stored information. It was found that after a slight initial alteration of stored threshold in the direction of the disturbing pulse, a constant level was reached which retained a 7 V difference between ONE and ZERO thresholds. This difference was more than that required for adequate ONE-ZERO output discrimination.

Although the coincident voltage selection circuit possesses many features required for a fully integrated EANDRO memory, it has one characteristic that makes it unsatisfactory at this time. This is the requirement that the substrate of each bit column of MNS-VTT's be electrically isolated from the substrates of bit columns of all other MNS-VTT's. This isolation requires an additional diffusion step to be added to the production process and uses up a significant proportion of the chip area. Furthermore, the large diffusions required to withstand relatively high reverse voltages result in an appreciable decrease in device yield. For this reason, data insertion circuits which eliminated or greatly reduced the isolation requirements were investigated. The channel-shielding technique, described next, is one such circuit.

B. CHANNEL-SHIELDING WRITE TECHNIQUE

The channel-shielding write technique is a method to store data in integrated arrays of MNS-VTT's. The main advantage of this technique is that it requires only one deep isolation diffusion to separate the addressing section from the memory section, whereas the coincident voltage technique requires that each bit line be separated from the other bit lines by isolation diffusions. This allows greater component densities, thereby increasing the number of circuits that may be processed on a silicon slice. The second advantage of the channel-shielding write technique is that it does not require the square hysteresis writing characteristic of the MNS-VTT that is required by the coincident voltage writing technique. This easing of the write characteristic requirements, coupled with the smaller number of isolation diffusions, should result in a significant yield improvement. The transistor count of the circuit approaches the lower limit of one transistor per bit in large arrays.

The basic channel shield writing technique can be explained with the aid of Fig. 20, which shows potentials existing in an MNS-VTT under different setting conditions. The MNS-VTT is set to the ZERO state (positive threshold setting) by the application of + 50 V to the gate while the substrate is at 0 V. The transistor is set to the ONE state (negative threshold setting) by a -50 V pulse on the gate while the substrate, source and drain

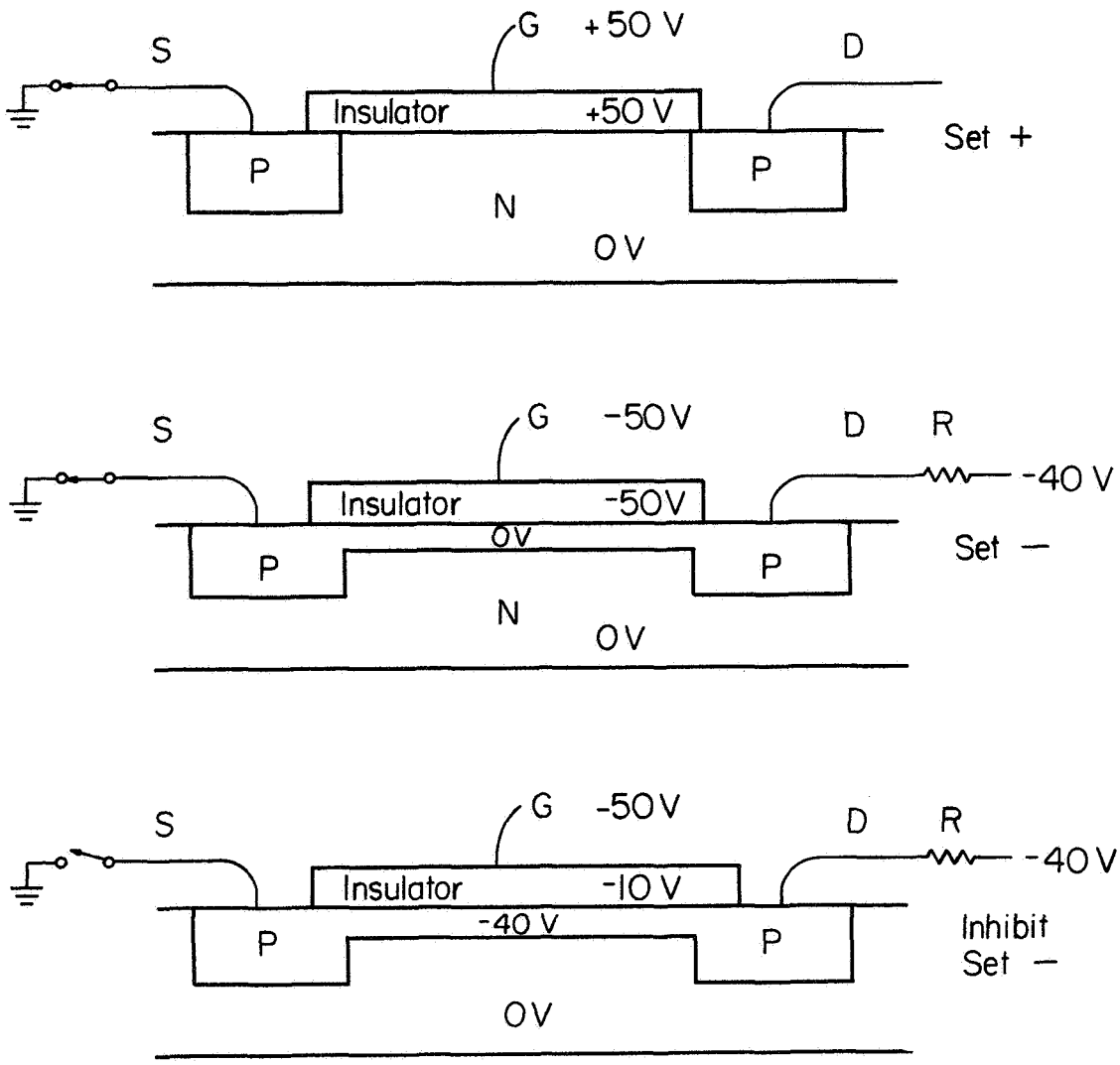

FIG. 20 Cross section of MNS-VTT during different setting conditions.

are held at 0 V. Note that a conducting channel is formed between source and drain when the negative voltage is applied to the gate. If this channel is held at ground potential, the -50 V is applied across the insulator, and the transistor is set to the negative threshold. If the channel is brought to a -40 V potential, the insulator will receive only a net -10 V potential, and the positive threshold setting will not be disturbed. The channel is used as a shield to prevent the -50 V from appearing across the insulator.

The circuit diagram of a 4-word x 4-bit integrated memory array which uses this writing method is shown in Fig. 21. The silicon chip is divided into substrate regions S_1 and S_2, separated by an isolation region. The address decoding and selection consists of four two-input NOR gates on substrate region S_1. The 16 memory transistors (M_{11} to M_{44}), the 4 load transistors (L_1 to L_4) and the 4 gating transistors (G_1 to G_4) are located on substrate region S_2.

The memory transistors are set to the positive threshold with S_1 and V_{ID} at ground potential and S_2 and V_{DD} at -50 V. The word lines, W_1 to W_4, are at ground potential and the substrates of the memory transistors are at -50 V. Each memory transistor has a net +50 V potential across the gate insulator and is therefore set to the positive threshold state.

The memory transistors are selectively set to the negative threshold with V_{DD} at -40 V, V_{ID} at -50 V and S_1 and S_2 at ground potential. Word 1 (W_1) can be selected by grounding the gates of NOR transistors X_{11} and X_{21}. Memory transistors M_{11}, M_{12}, M_{13} and M_{14} will then have channels formed under the gate area due to the -50 V V_{ID} on line 1. If the gates of transistors G_1 to G_4 are grounded so that these transistors do not conduct, their channels will be at V_{DD} (-40 V). The gate insulator is subjected to a net -10 V potential which does not change the positive threshold setting. The thresholds of the memory transistors can be selectively set negative by causing their respective gating transistors to conduct. G_1 to G_4 are relatively high conductance transistors and are able to clamp the channels near ground. With the channel near ground, the gate insulator of the memory transistor is subjected to -50 V and is set to the negative threshold.

A breadboard of the 4-word x 4-bit memory array was built using discrete components. The thresholds of the memory transistors were set to the positive state with a net +50 V applied for a 100 ms. The thresholds were selectively set negative with V_{ID} at -50 V and V_{DD} at -40 V for a period of 100 ms duration. The contents of the memory were read with V_{ID} set at -12 V; a read cycle of 1 μs and an access time of 0.6 μs were obtained.

Write-disturb tests were run using 2-bit x 4-word integrated memory arrays. The integrated arrays which were available required higher write voltages; therefore a V_{ID} of -65 V and a V_{DD} of -50 V were used. The memory was set to a given bit configuration and then one of the 4 words was subjected to 10^6 write cycles. There was no observable effect on the threshold settings of the memory transistors in the three other words.

The channel-shielded memory organization shown in Fig. 21 suffers when it is necessary to place the selection and storage circuits on separate

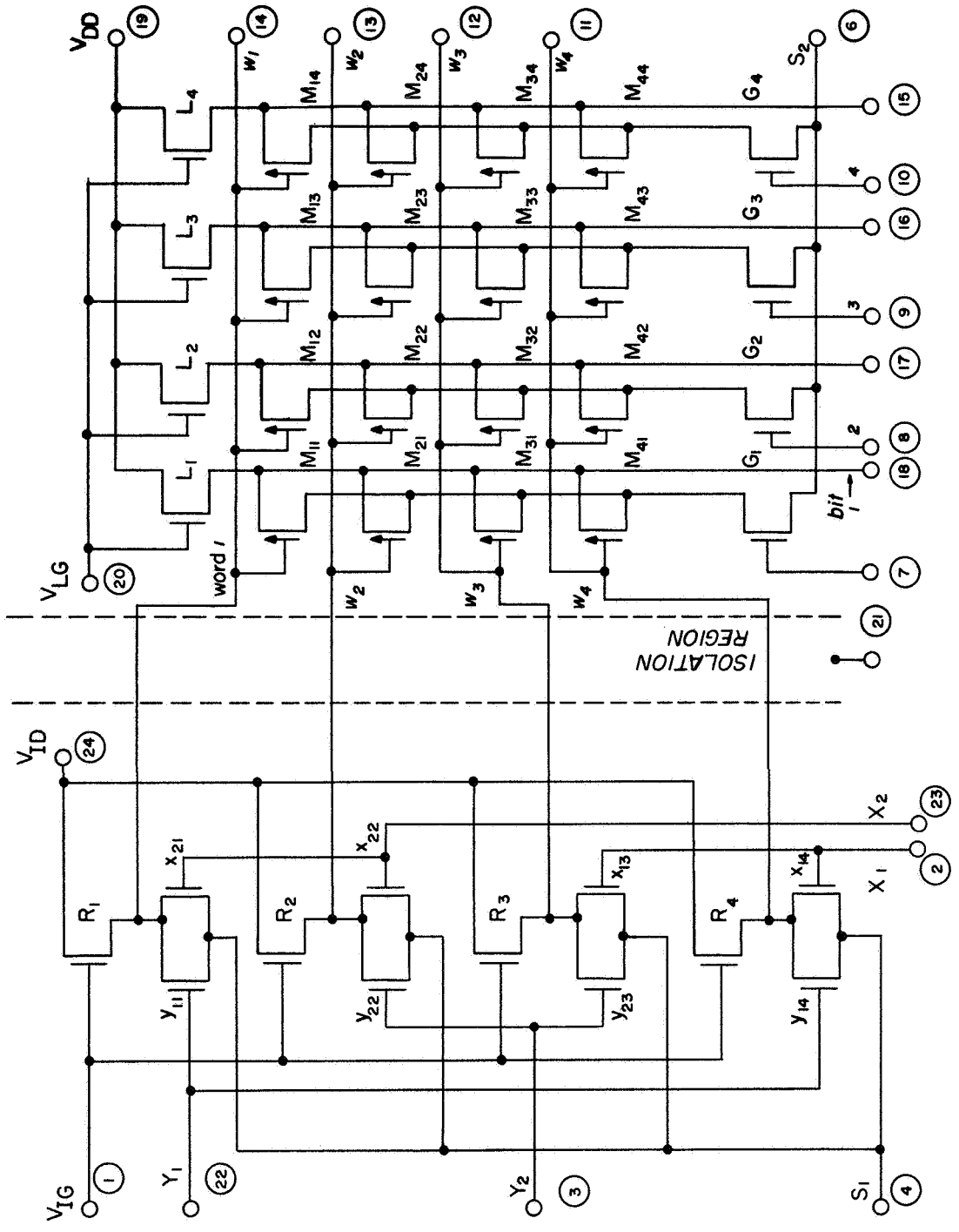

FIG. 21 Channel shielded 4 x 4 memory.

chips, because of the large number of connections which must be made from the selection chip to the storage chip. Another selection method which overcomes this disadvantage, the "3D" techniques is described next.

C. 3D SELECTION TECHNIQUE

The 3D selection technique yields a memory organization which allows the memory array and address selection circuits to be fabricated on separate chips without requiring an excessive number of interconnections between chips. A 128-word by 8-bit memory would require only 16 connections between the separate chips. The deep isolation diffusion required for writing is replaced by "air" isolation between chips. The two-chip approach simplifies fabrication if bipolar transistors are used for address decoding.

An 8-word by 1-bit memory circuit which uses the 3 D selection technique is shown in Fig. 22. The first level of addressing uses lines L_1 and L_2. When L_1 is made negative and L_2 is grounded, the left half of the memory is selected. The next level of selection uses lines G_1 and G_2. A negative voltage applied to G_1 and ground applied to G_2 selects the upper half of the memory. The final level of selection uses lines I_1 and I_2. A negative voltage applied to I_1 and a ground applied to I_2 selects columns 1 and 3. Memory transistor M_{111} is then uniquely selected. Input S is at ground potential during read operation. The state of the threshold setting of M_{111} is determined by the existence of a conductive path between D and S. If M_{111} is set to the positive threshold and G_1 is at the interrogate voltage, there is a conductive path between D and S. If M_{111} is set to the negative threshold, M_{111} does not conduct and the path is broken.

The memory transistors are set to the positive threshold by the application of +50 V to G_1 and G_2. Data is then stored by selectively setting individual transistors to negative thresholds. Data is entered at point D by driving that point either to ground or to -40 V. S is held at -40 V during write. To write a negative threshold in transistor M_{111}, inputs L_1, G_1 and I_2 are driven to -50 V and D, L_2, G_2 and I_1 are held at ground. The role of I_1 and I_2 is reversed during the write mode, where they perform an inhibit function rather than a selection function. The transconductances of transistors gated by I_1 and I_2 are designed to be a minimum of ten times greater than those of the transistors gated by L_1 and L_2. The channel of M_{111} is held at ground by the conductive path to D and the -50 V applied to G_1 is able to set the threshold to the negative state. Note that if D were at -40 V, the channel would be at -40 V and the positive threshold setting would not be disturbed. The channels of M_{112} and M_{212} are held at -40 V due to the greater conductance of the transistors gated by I_2. The channel of M_{211} is not connected to points D or S through a conducting L or I transistor. This channel is returned to -40 V through a transistor gated by W, whose transconductance is less than 1/10 that of the L-gated transistors. These transistors could be eliminated if a negative, low duty-cycle pulse train were applied to I_1 (or I_2 when appropriate) and stored charge were used to maintain the -40 V channel potential of M_{211}. The thresholds of M_{112}, M_{211} and M_{212} are not disturbed by the -50 V on G_1 because they are only subjected to a net -10 V gate-to-channel voltage.

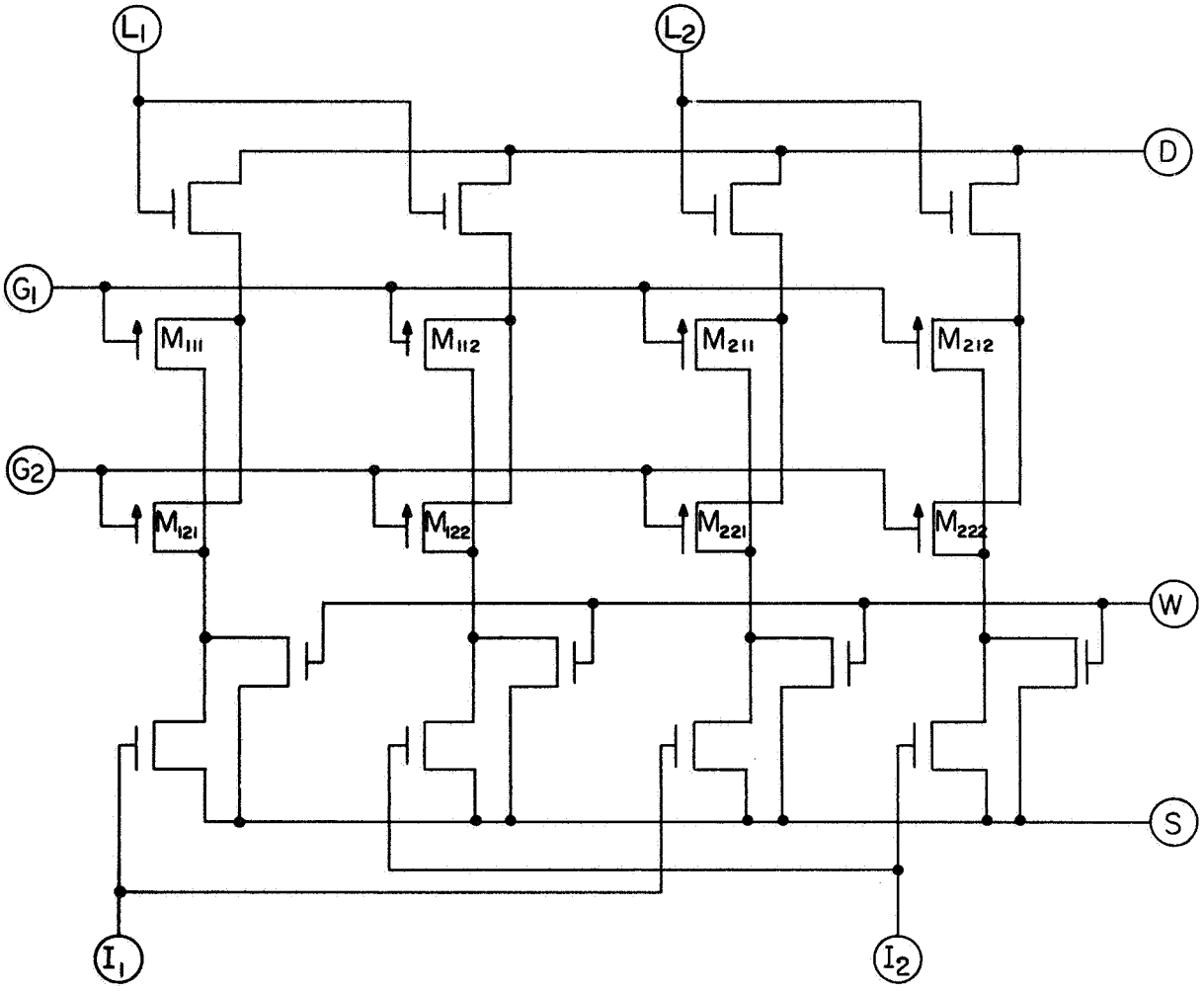

FIG. 22 3D selected channel shielded memory.

The memory can be expanded by increasing the number of L, G, I and D inputs. A 64-word by 4-bit (256 bit total) memory would require 4L, 4G, 4I and 4D inputs plus S, W and a substrate connection. Twelve of these inputs come from the address selection chip and represent the connection penalty incurred by the 2-chip approach.

D. AC COUPLED 2 x 2 ARRAY

In Fig. 23 the schematic of a two word memory is shown. Each word contains 2-bits. The structural diagram of the integrated memory (transistors T_{11}, T_{12}, T_{21}, and T_{22}) is shown in Fig. 24. AC coupling requires only three contacts in the memory portion of the array and also prevents dc current flow when writing.

Data is inserted into the memory in the following way (the waveforms are shown in Fig. 25). The chip is cleared by switching the substrate (V_{sub}) and bit lines (V_{B1} and V_{B2}) to -60 V while holding the word lines (V_{W1} and V_{W2}) at ground. The capacitors will block dc current flow in the word lines. This places +60 V across the insulator (the substrate side of the insulator is taken as the reference) and forces the threshold to assume its positive value. The bit pattern is entered in word one by placing -60 V (V_{W1}) on word line one, holding the potentials of word line two (V_{W2}) and the substrate (V_{sub}) at ground and selectively placing ground on bit lines (e.g., V_{B2}) in which it is desired to force the threshold to a negative value (e.g., transistor T_{12}). This places -60 V across the T_{12} insulator and causes the threshold to move negative. The potential of the other bit line (V_{B1}) is switched to -50 V. At this time T_{11} has the following potentials: the source is at -50 V, the substrate is at ground, and the gate is at -60 V. These potentials are such as to form a channel in T_{11} (since it had previously been set positive); the channel and drain will adopt the source potential (-50 V). The potential across the insulator in T_{11} will be -10 V, which is not large enough to move the positive threshold to a negative value (see Fig. 6). The voltage across the insulators in word two, which is not being written will be 0 V. Word two is written in similar fashion. Note that with careful attention to transient behavior it is possible to make the memory word alterable by selectively placing ground on a word line (e.g., V_{W1}) which is to be cleared and -60 V on the word which is not to be cleared, (e.g., V_{W2}).

The readout cycle is composed of two parts. During the first part the selected word is sampled by driving the word line (e.g., V_{W1}) to -15 V. Bit lines (V_{B1} and V_{B2}) are placed at -5 V and the substrate (V_{sub}) is grounded. In the accessed word these potentials are such that devices in which thresholds have been moved positively will conduct and deliver current to the bit lines. Those set negatively will not conduct. The current in the bit lines will then establish the bit value (ONE or ZERO). The word which is not selected will have its word line (e.g., V_{W2}) grounded. As such, T_{21} and T_{22} will not have a conducting channel and will only contribute capacitive loading of the bit lines.

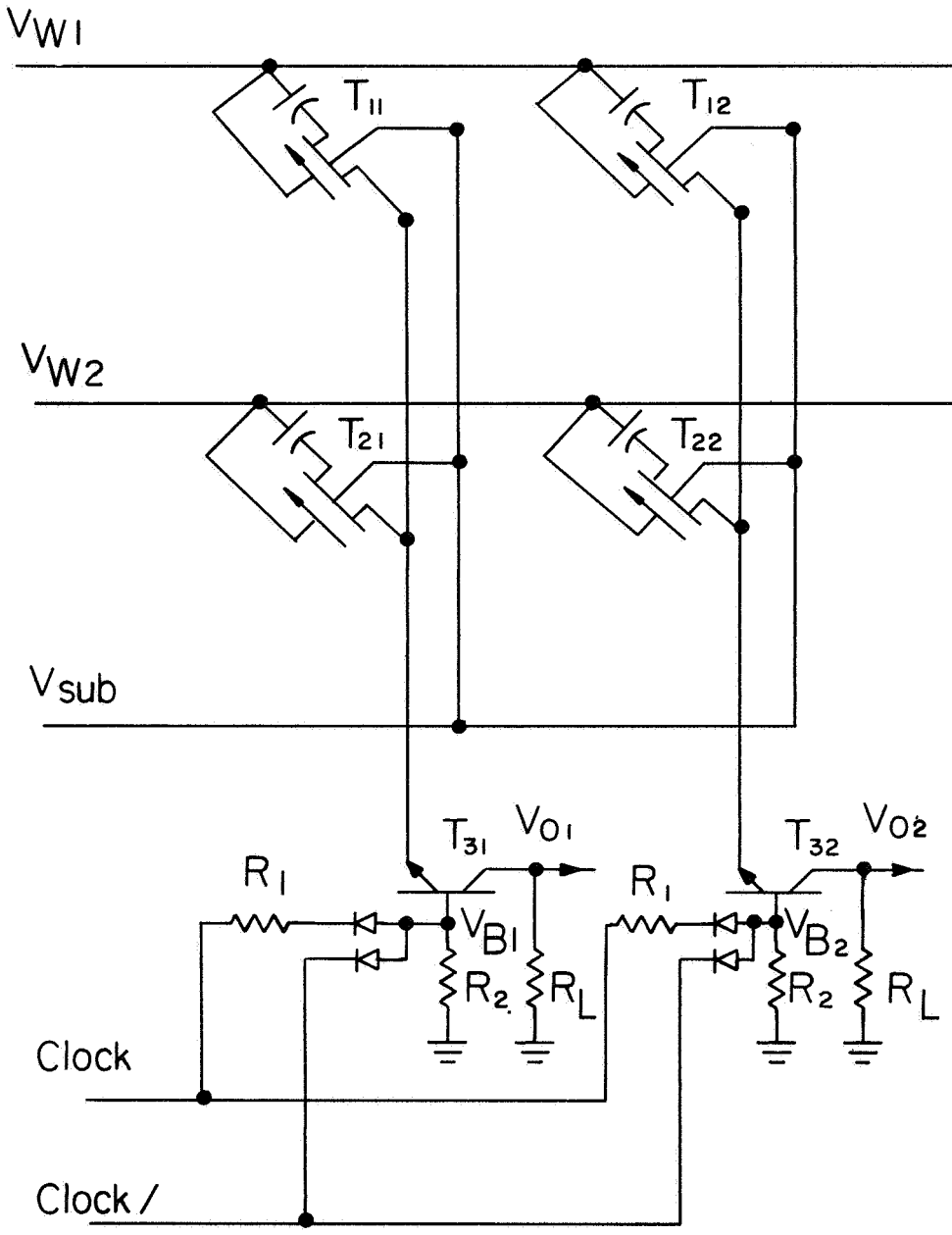

FIG. 23 Schematic of an ac coupled 2 x 2 array using the MNS-VTT device.

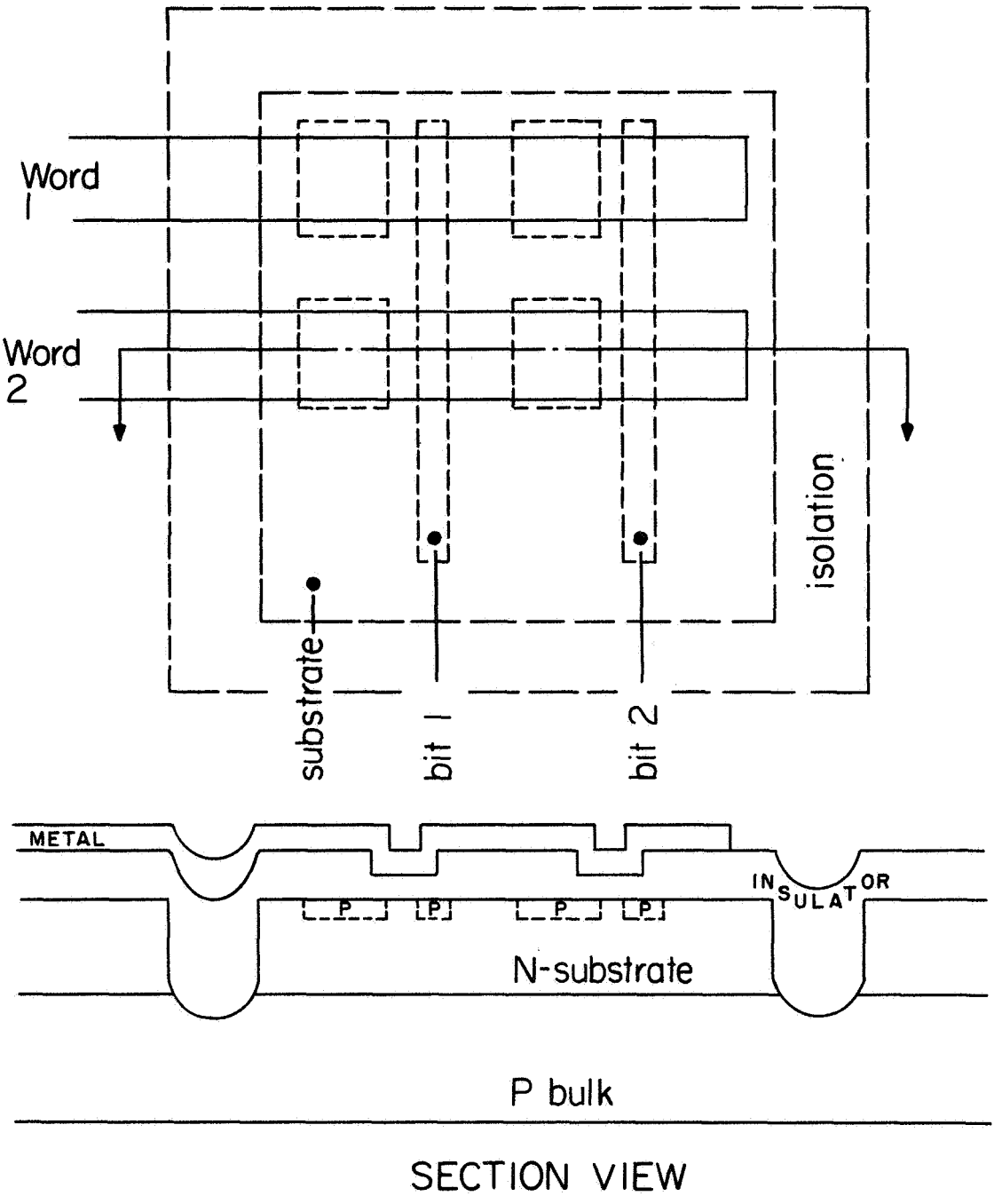

FIG. 24 Structural diagram of an ac coupled 2 x 2 array.

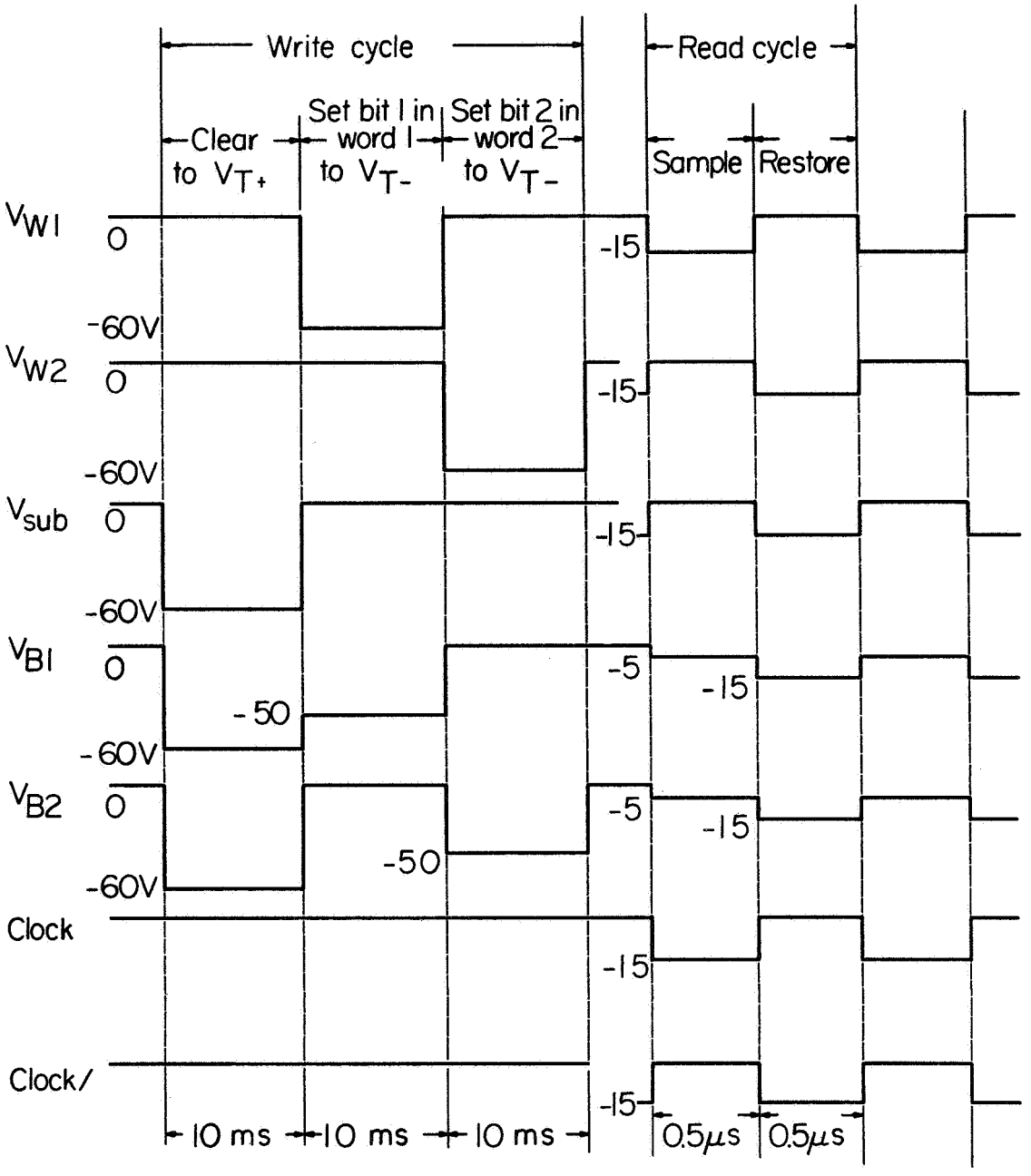

FIG. 25 Timing diagram of an ac coupled 2 x 2 array using the MNS-VTT device.

During the second (restore) part of the cycle, the selected word line goes to ground and the bit lines, the substrate, and the other word lines go to -15 V. The potential across the insulator in the accessed word is then opposite to that which was across the insulator during the sample part of the read cycle. Note that word two, which is not addressed, will have 0 V across its insulator during the entire read cycle. Note that word two, which is not addressed, will have 0 V across its insulator during the entire read cycle.

The reasoning for this type of read cycle may be inferred from data presented in Fig. 11; inparticular, pulse condition "B".

Data from the discrete version of the 2 x 2 array is presented in Figs. 26 and 27. Word one (Fig. 26) has been interrogated continuously (except for measurement of threshold shift) with T_{11} set positively and T_{12} set negatively. The decay of T_{11} is unexpectedly large, but even at that storage of about six months may be expected under these conditions. Word two (Fig. 27) shows decay which is about the same as that under zero bias. As such, if a straight line approximation is valid, there should be about 9 V difference between the unit set positively and the unit set negatively.

E. MNS BIPOLAR MEMORY

Memory systems using IGFETs not only for the storage elements but for the interrogation and selection circuits, as well, are limited in access speed due to inherent delays of IGFET circuits. For this reason, a configuration was investigated which employed MNS-VTT's as the basic storage elements, but use high speed bipolar transistors for driving and sensing elements. A diagram of an experimental 2 x 2 model of this circuit is shown in Fig. 28. During interrogation the gates of all the MNS-VTT's are held at a negative reference voltage. The amplitude of this voltage is chosen such that memory cells which have been set to their most positive gate threshold voltages (ONE's) will be maintained in the conductive state, whereas cells which have been set to their most negative gate threshold voltages (ZERO's) will be maintained in the cutoff state. In this way, the conducting channels of devices storing ONE's are pre-established and the delays required to establish such channels are avoided. Interrogation of a particular word is accomplished by pulsing the base of the bipolar p-n-p word driver associated with the selected word. The word drivers are emitter followers, so that pulses applied to bases appear at the common source node of all memory cells in the selected word. All memory cells storing ONE's will conduct, causing current flow from the emitters of the common-base-connected n-p-n sense amplifiers in their respective bit columns. This current flow will cause negative output pulses to appear across the output load resistors. Memory cells storing ZERO's will not conduct, so that no voltage pulses will appear at their respective bit output points.

Data insertion in the experimental memory was accomplished by mechanically switching the gates of the memory cells to the setting voltages. In an integrated system, techniques such as the coincident voltage method described previously may be employed.

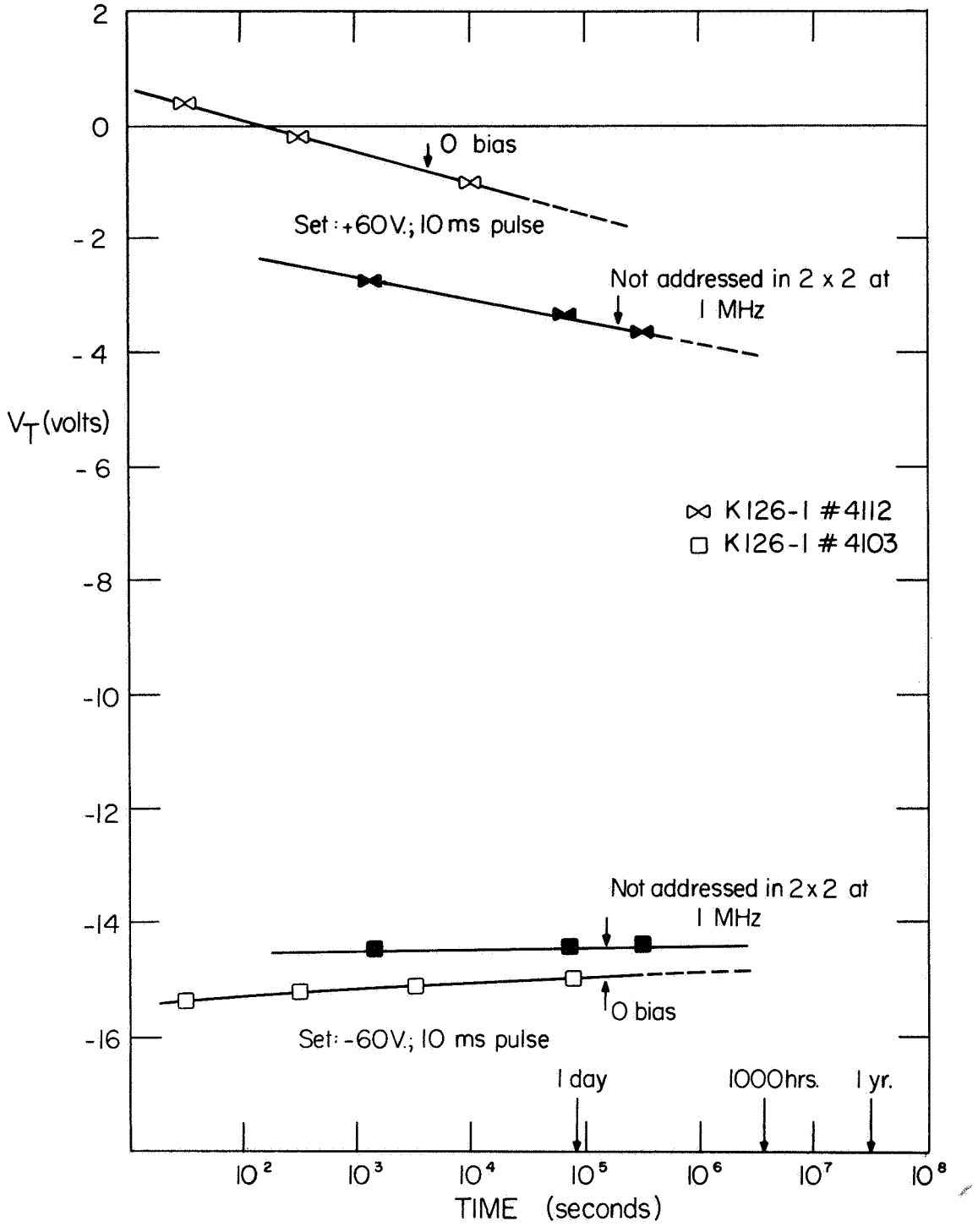

FIG. 26 2 x 2 memory storage characteristics—nonaddressed elements.

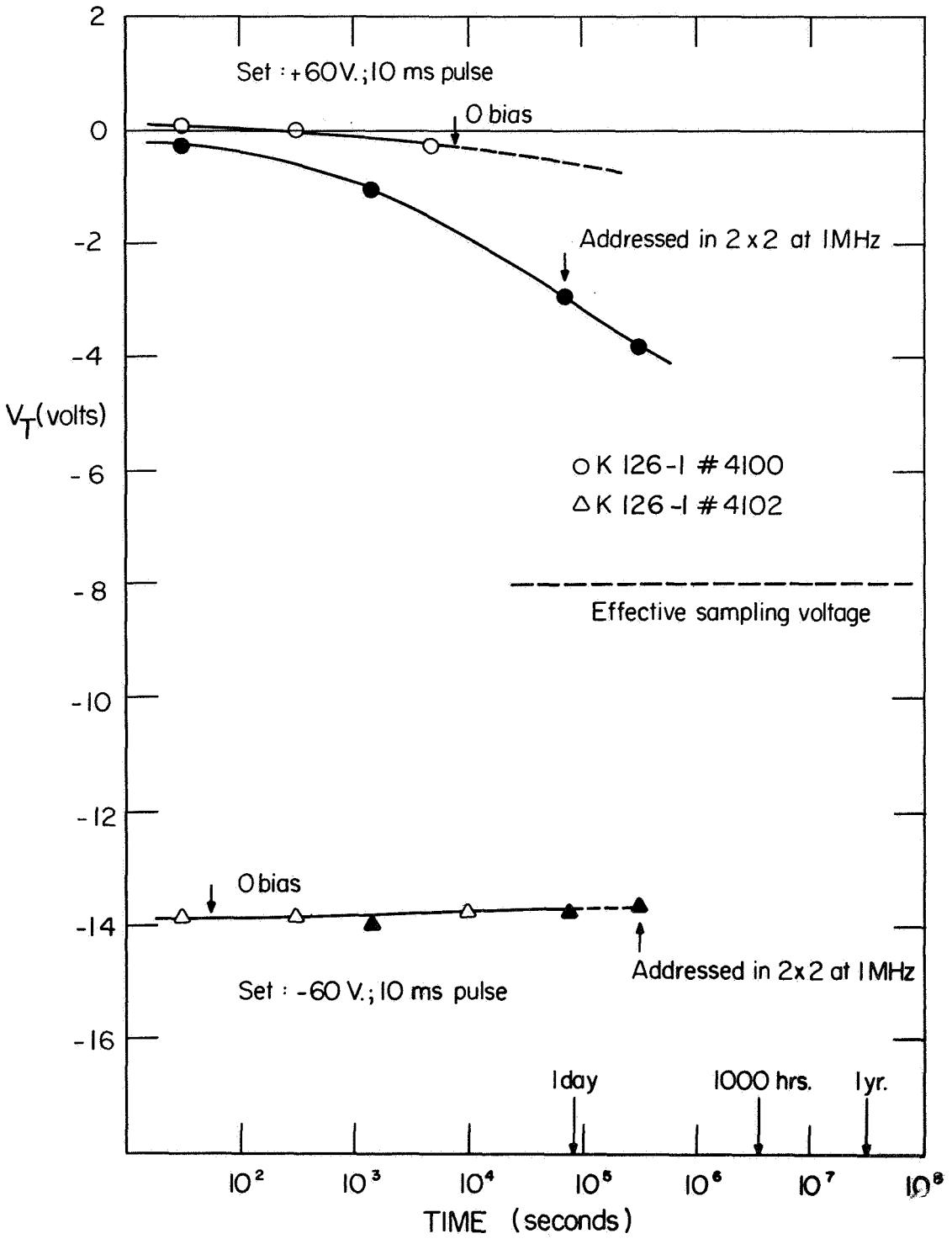

FIG. 27 2 x 2 memory storage characteristics—addressed elements.

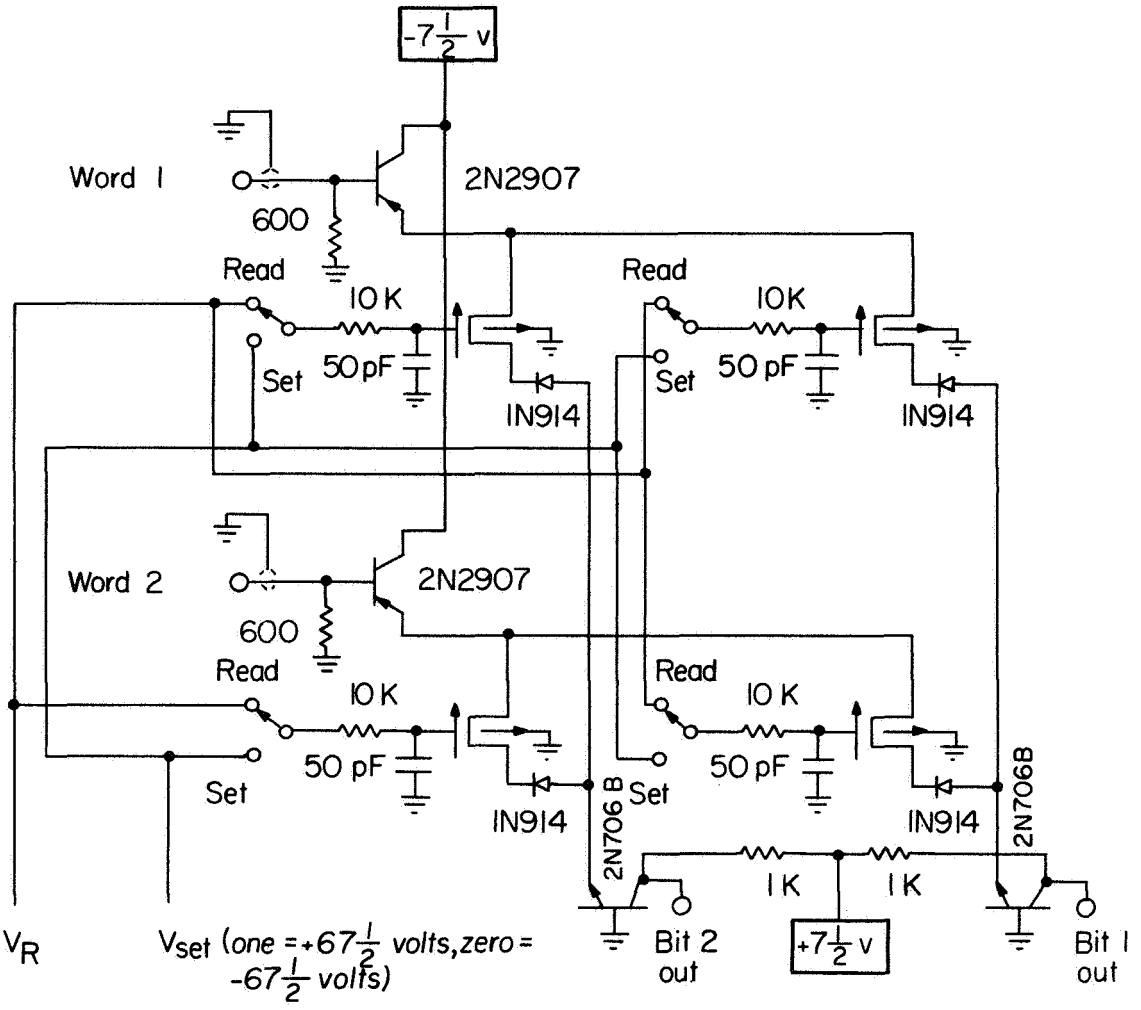

FIG. 28 MNS-VTT/bipolar-transistor 2 x 2 memory.

The operation of the experimental memory was tested by connecting one of the word selection inputs to the output of a GR 1217-C pulse generator. The pulse amplitude was 7 V. A reference voltage of 5 V was applied to the memory cell gates. A set of oscilloscope photographs showing the transfer characteristics of the experimental memory is shown in Fig. 29. In each case, the upper trace shows the input to the word driver and the lower trace shows the output at the collector of the sense amplifier. The first four photographs show the output at successive intervals after setting, when the cell was storing a ONE. The last photograph shows the output when the cell was storing a ZERO. The output delays are seen to be approximately 10 ns in each case.

The decay in output amplitude observed illustrates one of the drawbacks of this memory circuit, namely that the continuous application of nonzero potentials to the memory gates serves to hasten the decay of storage. This may be overcome to some extent by using a block selection technique in which the gates of memory cells in unselected blocks of memory are held at ground potential and only those gates in block of memory being interrogated are driven to the reference voltage. If operations are organized so that a single block is interrogated many times before moving on to another block, then the potential speedup afforded by this type of memory circuit can be obtained.

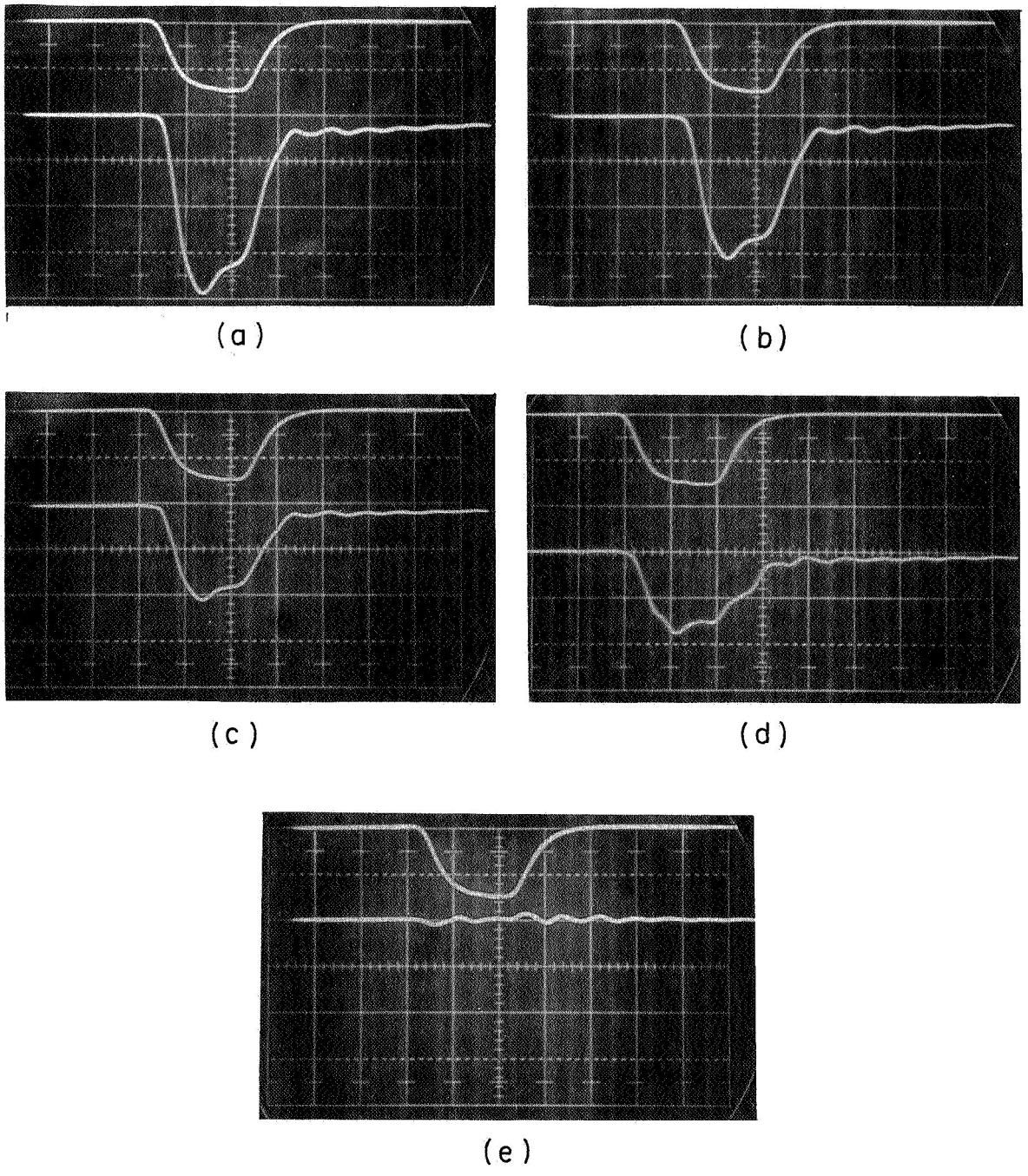

FIG. 29 Oscilloscope traces of VTT/bipolar memory response (upper trace is input, lower is output). Horizontal scale: 50 ns/cm; vertical scale: upper trace - 5 V/cm, lower trace - 0.5 V/cm. The traces are: (a) at positive set time, (b) 30 sec after positive set, (c) 15 min. after positive set, (d) 30 min. after positive set, and (e) 1 min. after negative set.

SECTION V

CONCLUSION

It has been shown that the MNS-VTT provides the basis for an electrically-alterable, nonvolatile memory with storage capabilities in the thousands of hours even when subjected to the standard military temperature range. Writing speeds at present appear to be in the range of several milliseconds per word, but can be increased with the application of higher voltages. Interrogation delays of 10 ns or less have been exhibited.

Since the MNS-VTT is an amplifier, simple read circuitry is possible. Writing techniques, however, are somewhat complex due to the necessity of applying, selectively, both positive and negative gate voltages. The 3-D selection channel-shielded write circuit provides a degree of simplicity in writing circuitry at the expense of a greater number of connections to the memory chip. In view of the reduction in the number of semiconductor processing steps engendered by this system, it is recommended as the best candidate for use in the development of future integrated semiconductor memory arrays based on the MNS-VTT technology.

APPENDIX A

NEW TECHNOLOGY

After a diligent review of the work performed under this contract, no new innovation, discovery, improvement or invention was made.