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IMPLEMENTATION OF A DIGITAL CONTROL UNIT FOR A SPACE PROBE USING MOSFETs

by H. Hauck

Deutsche Versuchsanstalt für Luft- und Raumfahrt

Oberpfaffenhofen, Federal Republic of Germany

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This report describes the use of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) in spacecraft electronic sub-systems. The fundamentals of MOSFETs and rules for their application are presented with emphasis on the application rather than on the theory of operation. Several types of logic systems are compared with respect to their power consumption.- A simple but typical digital control unit for a small spacecraft is described. For this unit the implementation is shown using a special family of integrated MOSFET logic blocks.

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EUROPEAN SPACE RESEARCH ORGANISATION
114, avenue de Neuilly, 92 Neuilly-sur-Seine (France)

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SUMMARY

This report describes the use of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) in spacecraft electronic sub-systems. The fundamentals of MOSFETs and rules for their application are presented with emphasis on the application rather than on the theory of operation. Several types of logic systems are compared with respect to their power consumption.

A simple but typical digital control unit for a small spacecraft is described. For this unit the implementation is shown using a special family of integrated MOSFET logic blocks.

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IMPLEMENTATION OF A DIGITAL CONTROL UNIT FOR A SMALL SPACE PROBE USING METAL-OXIDE-SEMICONDUCTOR FIELD-EFFECT TRANSISTORS (MOSFETs)

H. Hauck
Massachusetts Institute of Technology
Cambridge, Mass.

I. INTRODUCTION

The transmission of information free of errors over interplanetary distances is limited mainly by the spacecraft power systems available. Present systems within a permissible weight range do not supply signals at a high transmission rate with signal-to-noise ratios, which are sufficiently high for the very noisy transmission channel. There are three methods by which these difficulties can be overcome : One solution is the use of high-power pulses [1], but these reduce the bit rate. A second method is the use of transmission codes, as has been suggested by Lumb and Hofman[2], but a low bit rate coding implies increased complexity of the system, in the space craft. A third method, which is able to handle a high complexity and which reduces the power consumption is the implementation of the electronic sub-systems with Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs). Their property of using very little power together with very attractive integration properties increases the effective transmitter power and the number of elements for the space available.

MOSFETs were used in the IMP satellite programme with much success [3] and are being used for the sunprobe "Sunblazer" of MIT [4].

This report describes the implementation of a digital control unit with MOSFETs. To be of general value and interest, the control unit is composed of typical elements used generally in satellite electronics. Although the chosen example would be for a small scientific space probe, its implementation can easily be expanded and changed into any desired size and configuration.

II. SYSTEM ELEMENTS

Basically the control unit of a space probe has the following duties :

a) Timing scientific and engineering measurements.
b) Storing data, whose measurement time occur out of transmission sequence.
c) Converting analogue signals to digital form.
d) Multiplexing (commutating) the data according to a chosen "frame" configuration.
e) Converting parallel words to a serial bit stream.
f) Commanding various operations of the R-F unit (modulation, frequency or phase switches etc.).
g) Generating a code (synchronization).

All this can be done with basic processing elements, such as multiplexers, frequency dividers, storage (buffer), A-D converters (analogue to digital), shift registers, counters, adders and switches.

In Figure 1 these elements are used to form the control unit, which will be the basis of this discussion.

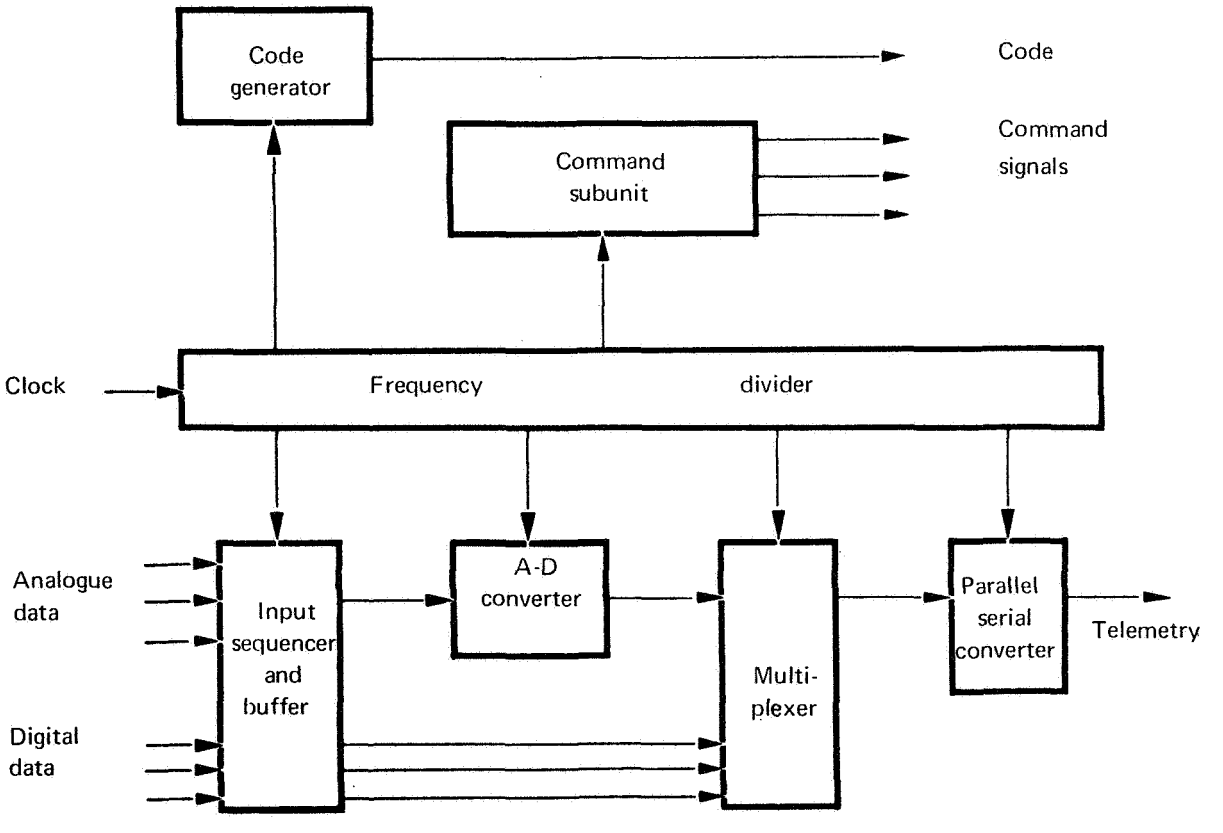

Figure 1. - Block diagram of the control unit.

The signal from the *central clock* is subdivided several times in the *frequency divider* (count down chain) to supply various timing signals to the other elements. The *command sub-unit* encodes these signals in a matrix into complex command signals of different length and period. The *code generator* supplies at the appropriate time a pulse sequence, which is used for synchronization. In this example a double folded 11-bit Barker Code is used. Scientific and engineering measurements in digital and analogue form are enabled by the *input sequencer* and switched at the proper time either to the *A-D converter* or directly to the Multiplexer. If a measurement must be made at a time which does not coincide with its sequencing time, it is stored in the *buffer.* The *multiplexer* switches all words into the proper sequence, which is determined by the "frame" arrangement. Each word then is converted into a series of bits in the *parallel-serial converter.* These bits then modulate the carrier or sub-carrier according to their binary value.

III. MOSFET TECHNOLOGY*

Space electronic systems include digital elements, which usually operate with very low duty factors (1% to 10%) on the average. This means that active switching devices should have very low stand-by power dissipation in both stable states.

The many definite advantages of MOSFETs over bipolar transistors in this respect include :

a) Very high *input resistance* (around 10^{14} ohms), which is unaffected by the polarity of any bias voltage.

b) High *fan out.*

c) Capacitive input, permitting *direct coupled circuitry.*

d) *Low temperature coefficient.*

e) Extremely *low power dissipation* (10^{12} watt) in the "off" state, for complementary circuits in both stable states.

f) Requirement of only *one power supply.*

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* This chapter is partially a repetition of chapter 3 of Hauck[4], except section III.1. Section III.4 gives only a short account of the electrical characteristics, which are treated in much more detail in Hauck[4].

g) *Small geometry* (area only 5% of an integrated bipolar transistor).

h) *Simple production* (single diffusion requiring 38 steps compared with 130 steps for double-diffused circuits).

At this point no discussion will be made on the theory and fabrication techniques of MOSFETs, as this has been treated widely in the literature [5-6]

Only the basic rules of their use and the considerations which lead to the choice of a particular set of MOS logic blocks will be presented here.

III. 1 Basic Rules for MOSFET Logic

The MOSFET is a sandwich-like structure of a metal plate, an insulating layer of oxide (SiO_2) and a substrate of silicon. Two regions are diffused into the substrate, which are of opposite conductivity to it. They are situated directly under the metal plate plus insulation as shown in Figure 2 for both a N-type substrate with P-type regions and vice versa.

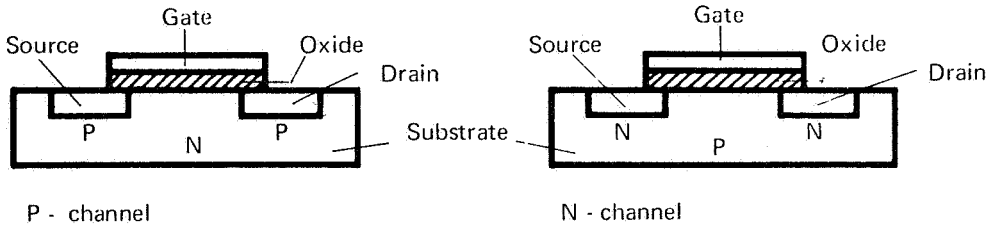


Figure 2. - MOSFET structure.

The metal plate is called "gate", the diffused regions "source" and "drain"; the substrate area between the two regions forms the "channel". The gate and substrate form a parallel plate capacitor. When no charge is on the gate, the channel is just silicon of the conductivity opposite to the drain and the source. In this condition, if a potential difference is applied between source and drain, no current will flow because one PN junction will have reverse bias regardless of the polarity.

If however a charge is applied to the gate, which is sufficient to draw holes into the channel region (PNP-case) or electrons (NPN-case), the conduction type of the channel changes to that of the source and drain regions.

The gate voltage at which this inversion occurs is called threshold voltage. A voltage in excess of this value allows ohmic conduction from source to drain.

This type of channel forming is called *enhancement mode* compared to the *depletion mode*, where a channel always exists, unless a gate voltage produces a type of silicon with opposite conductivity between source and drain. In the following only the enhancement type will be discussed.

In Figure 3 the symbols for P-channel and N-channel MOSFETs are shown together with the basic inverter circuit.

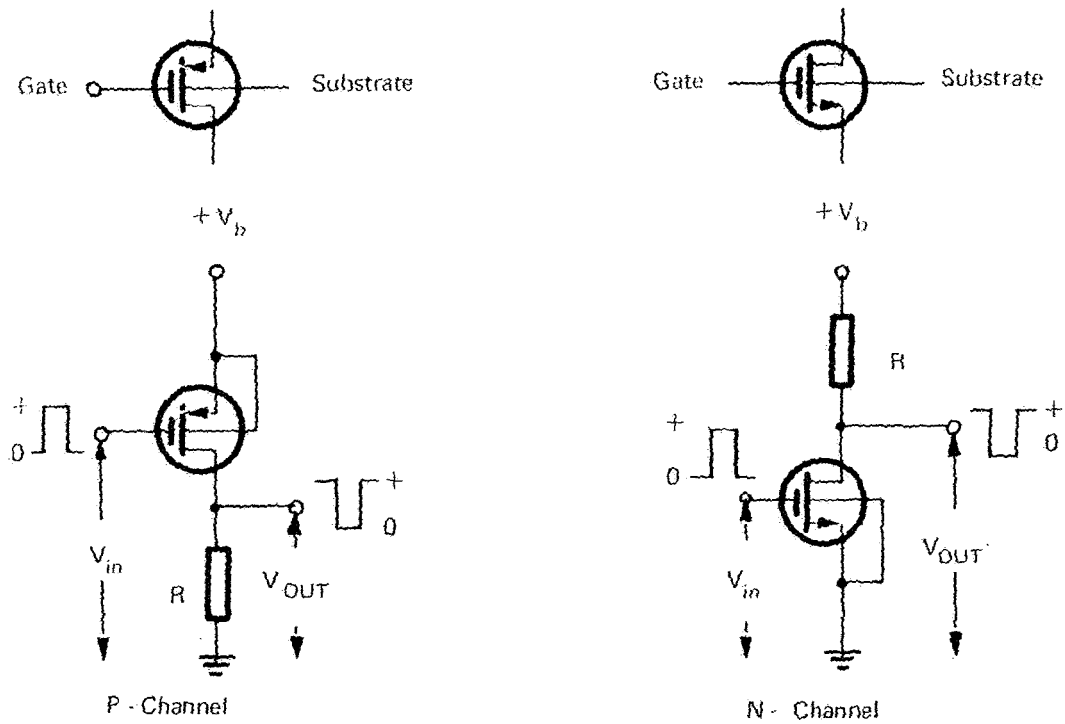


Figure 3.- Symbols and inverter circuits for P-channel and N-channel devices.

The device is completely symmetrical as long as the substrate is not connected to one of the two nodes : in such cases the designations "source" and "drain" will be

omitted. In general the substrate is connected to the highest positive voltage (P-channel) or the most negative voltage (N-channel), because the voltage difference between gate and substrate affects strongly the transconductance of the channel in the conducting ("on") state. This influence increases as the voltage difference increases.

The P-channel device is conducting with a negative gate-voltage with respect to the substrate, the N-channel device with a positive gate-voltage.

The high input resistance (low gate leakage current) and capacitive input property allow *direct coupling* of a high number of stages. This is shown for one P-channel device driving three direct coupled devices in Figure 4.

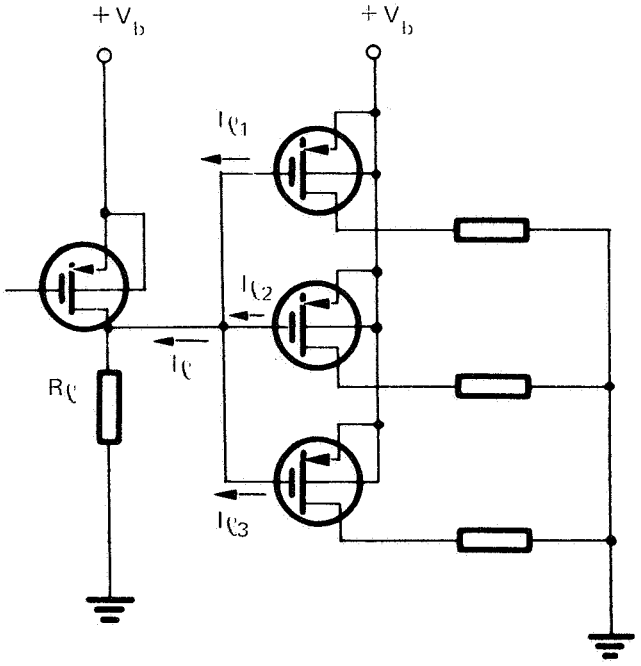
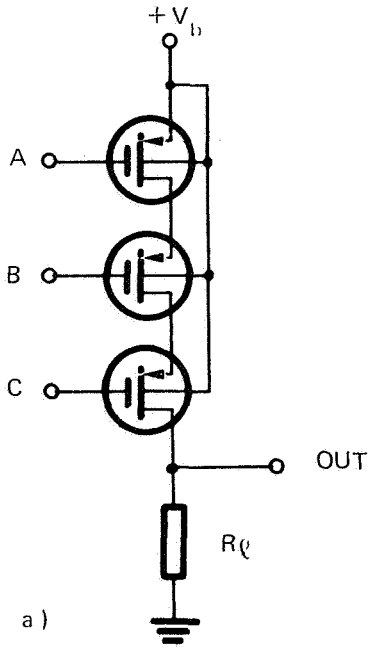


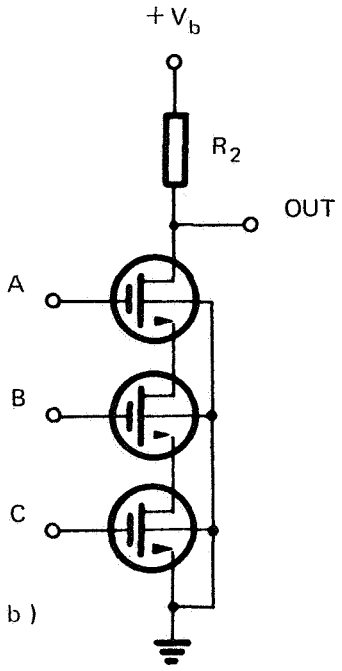
Figure 4.- Direct coupled stages.

The fan-out of the driving stage is only limited by the sum of all gate leakage currents I_1, which produces a voltage level shift in the load resistor R_1 of the driving stage. This shift should stay well below the threshold voltage.

The high channel resistance in the "off" state (10^{14} ohm) and a comparatively low resistance in the "on" state (200-800 ohm) also allows the *direct connection in series* as shown in Figure 5



A	B	C	OUT
0	0	0	+
0	0	+	0
0	+	0	0
0	+	+	0
+	0	0	0
+	0	+	0
+	+	0	0
+	+	+	0



A	B	C	OUT
0	0	0	+
0	0	+	+
0	+	0	+
0	+	+	+
+	0	0	+
+	0	+	+
+	+	0	+
+	+	+	0

Figure 5.- Serial connection and truth tables for, a : P-channel; b : N-channel MOSFETs.

This serial configuration of P-channel devices can be used as NAND - gate for negative signal direction (where 0 volt = "1", + volt = "0") or as NOR - gate for positive signal direction (where 0 volt = "0", and + volt = "1").

With N-channel devices this property is completely reversed.

The number of devices connected in series is limited by the "voltage drop", which is related to the ratio of the sum of channel resistances R_{on} in the conducting state to the load resistor R_l.

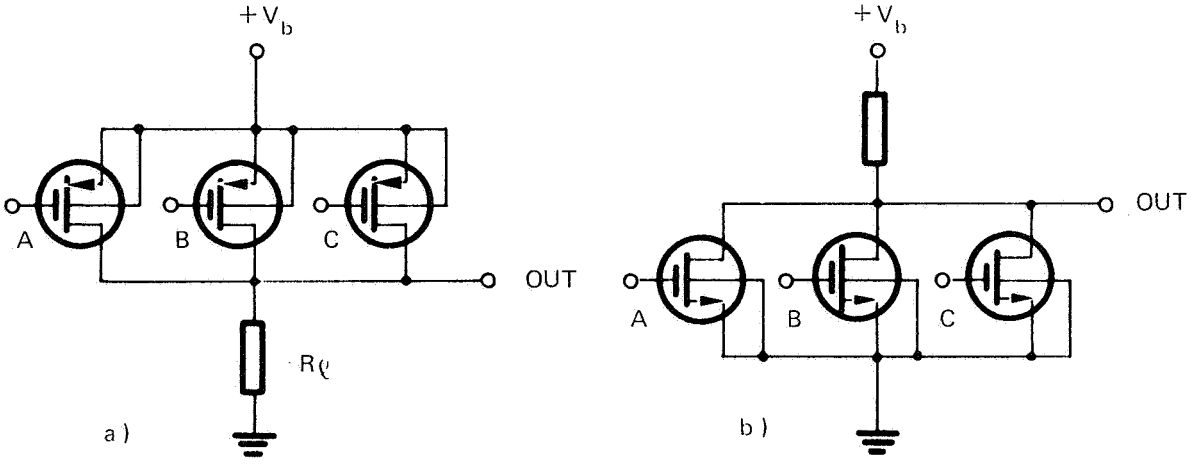
This can be expressed with the equation for the voltage divider :

$$\frac{V_{out}}{V_b} = \frac{R_l}{R_l + R_{on}} \qquad (1)$$

For example, if the sum of the individual channel resistances of the circuit $R_{on} = R_l$, the output voltage V_{out} is only half of the supply voltage V_b.

As this voltage drop, $(V_b - V_{out})$ depends also on the value of the load resistor R_l, which in turn affects also the power consumption and the switching speed of the circuit, a compromise must be found between the number of stages, power and speed as will be shown later in section III.2.

The effect of connecting the devices *in parallel,* shown in Figure 6, is less critical. It is limited only by the sum of channel leakage currents in the "off" state, and is similar to the case of the direct coupled inverter stages (see Figure 4).



A	B	C	OUT
0	0	0	+
0	0	+	+
0	+	0	+
0	+	+	+
+	0	0	+
+	0	+	+
+	+	0	+
+	+	+	0

A	B	C	OUT
0	0	0	+
0	0	+	0
0	+	0	0
0	+	+	0
+	0	0	0
+	0	+	0
+	+	0	0
+	+	+	0

Figure 6.- Parallel connection and truth tables for, a : P-channel; b : N-channel MOSFETs.

The parallel configuration of P-channel devices can be used as NOR - gates for negative signal direction and as NAND - gates for positive signal direction. With N-channel devices the properties are inverted.

This demonstrates clearly, that it is not necessary to use both P-channel and N-channel devices together in one digital system, as one group is already sufficient to produce all Boolean functions.

The only major application in which both N-channel and P-channel devices are used together is in *complementary circuits* : Figure 7 shows the basic inverter.

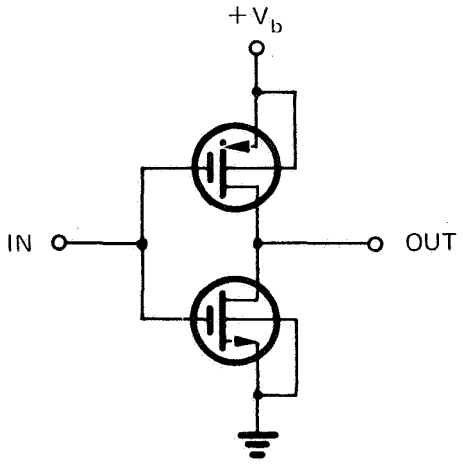


Figure 7.- Basic complementary inverter.

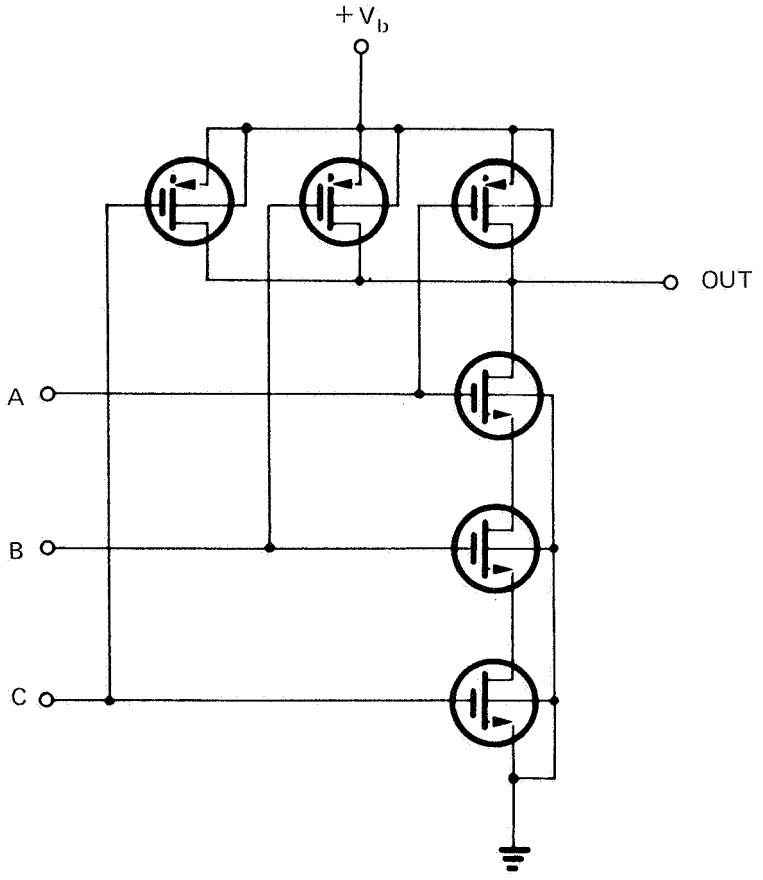
With 0 volt at the input (both gates) the upper P-channel device is fully conducting, whereas the lower N-channel device is cut off. The output voltage is $V_h - V_1$, where V_1 is the voltage drop across the P-channel resistance. V_1 is of the order of 10^{-9} volt as the current flow through the whole circuit is equal to the channel leakage current of the non-conducting device (in the vicinity of 5 nA).

If the voltage at the input is positive the P-channel device is cut off and the N-channel device conducts. The current again is the same as above, the output voltage is 0 volt $+ V_2$, where V_2 is the voltage drop across the N-channel resistance ($V_1 = V_2$).

The huge advantage of complementary MOSFET circuits lies in the extremely low power consumption, which is determined mainly by the transient power dissipated during

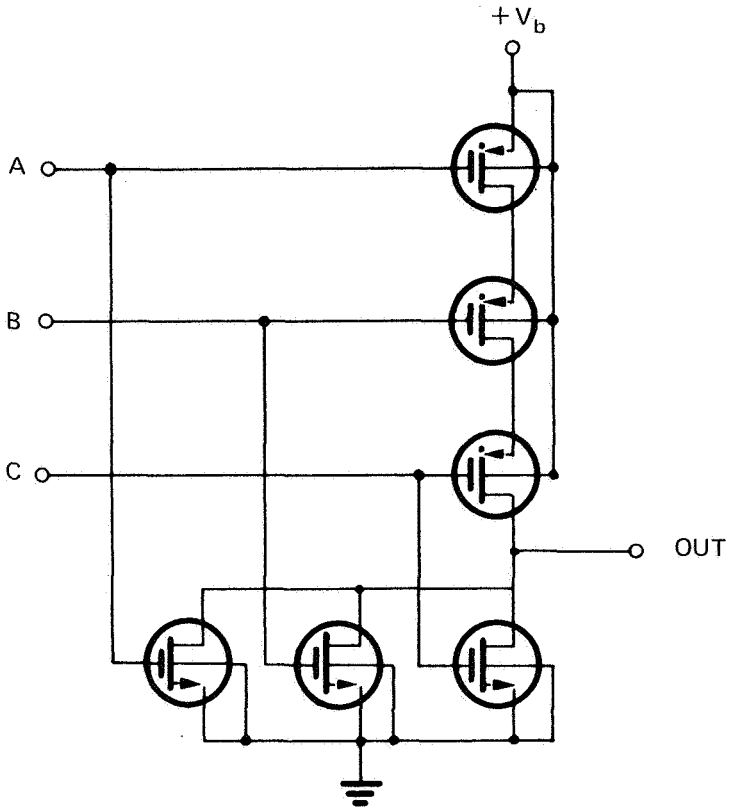
the switching time. This will be discussed and compared with single channel circuits in section III. 2.

The 3-input gates corresponding to those shown in Figure 5 and Figure 6 are shown in Figure 8 and Figure 9.



A	B	C	OUT
0	0	0	+
0	0	+	+
0	+	0	+
0	+	+	+
+	0	0	+
+	0	+	+
+	+	0	+
+	+	+	0

Figure 8. - Complementary 3-input gate (Type A).



A	B	C	OUT
0	0	0	+
0	0	+	0
0	+	0	0
0	+	+	0
+	0	0	0
+	0	+	0
+	+	0	0
+	+	+	0

Figure 9. - Complementary 3-input gate (Type B).

The type A gate is a combination of Figure 5b and Figure 6a and can be used as NOR-gate for negative signal direction and as NAND-gate for positive signal direction.

The type B gate is a combination of Figure 5a and Figure 6b and can be used

as NAND-gate for negative signal direction and as NOR-gate for positive signal direction.

The big advantage of MOSFET logic is the possibility of obtaining more complex logic functions by using the NAND- and NOR-gates described so far.

As an example the implementation of the function F

$$F = (A \cdot \overline{B} \cdot C) + (\overline{A} \cdot B \cdot C) + D$$

where :

$A \cdot B$	means	A AND B
$A + B$	means	A OR B
$\overline{A}$	means	Complement (or Inversion) of A

This is shown in Figure 10 for P-channel devices and negative signal direction.

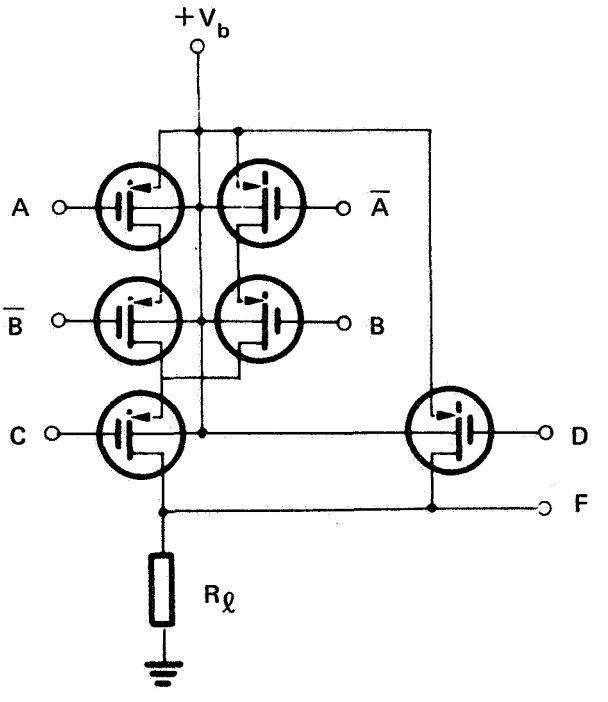


Figure 10.- Implementation of several-input logic function with P-channel MOSFETs.

The same circuit implemented with complementary logic is shown in Figure 11.

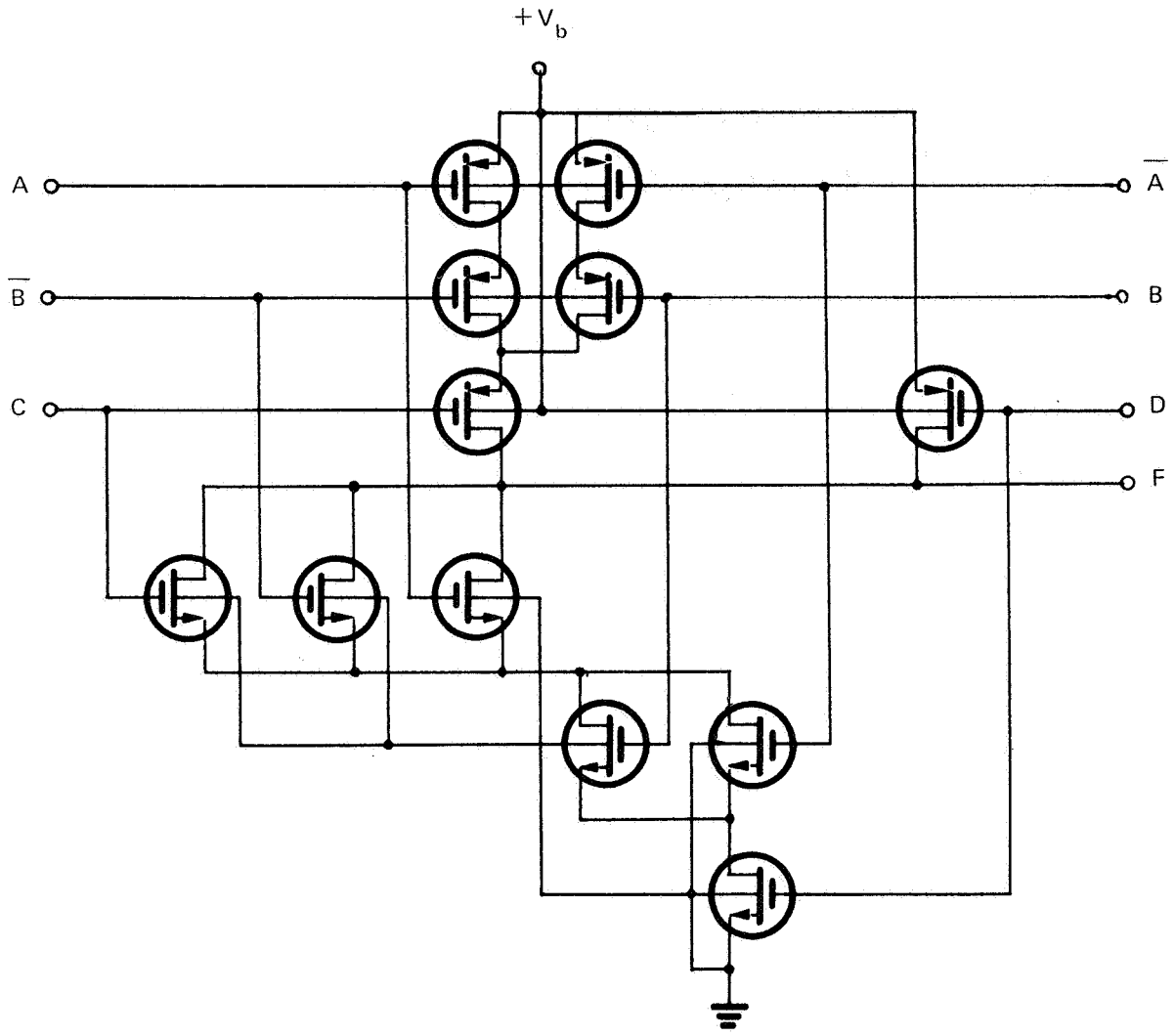


Figure 11.- Implementation of the function F with complementary MOSFETs.

A R-S-flip-flop can be implemented in two ways. Figure 12a shows it for negative signal direction (active input is 0 volt), Figure 12b for positive signal direction (active input is + V). In Figure 12c a D-type flip-flop is shown, where, after preparation of the inputs "IN" and "$\overline{\text{IN}}$", the information is transferred into the flip-flop with the signal Φ.

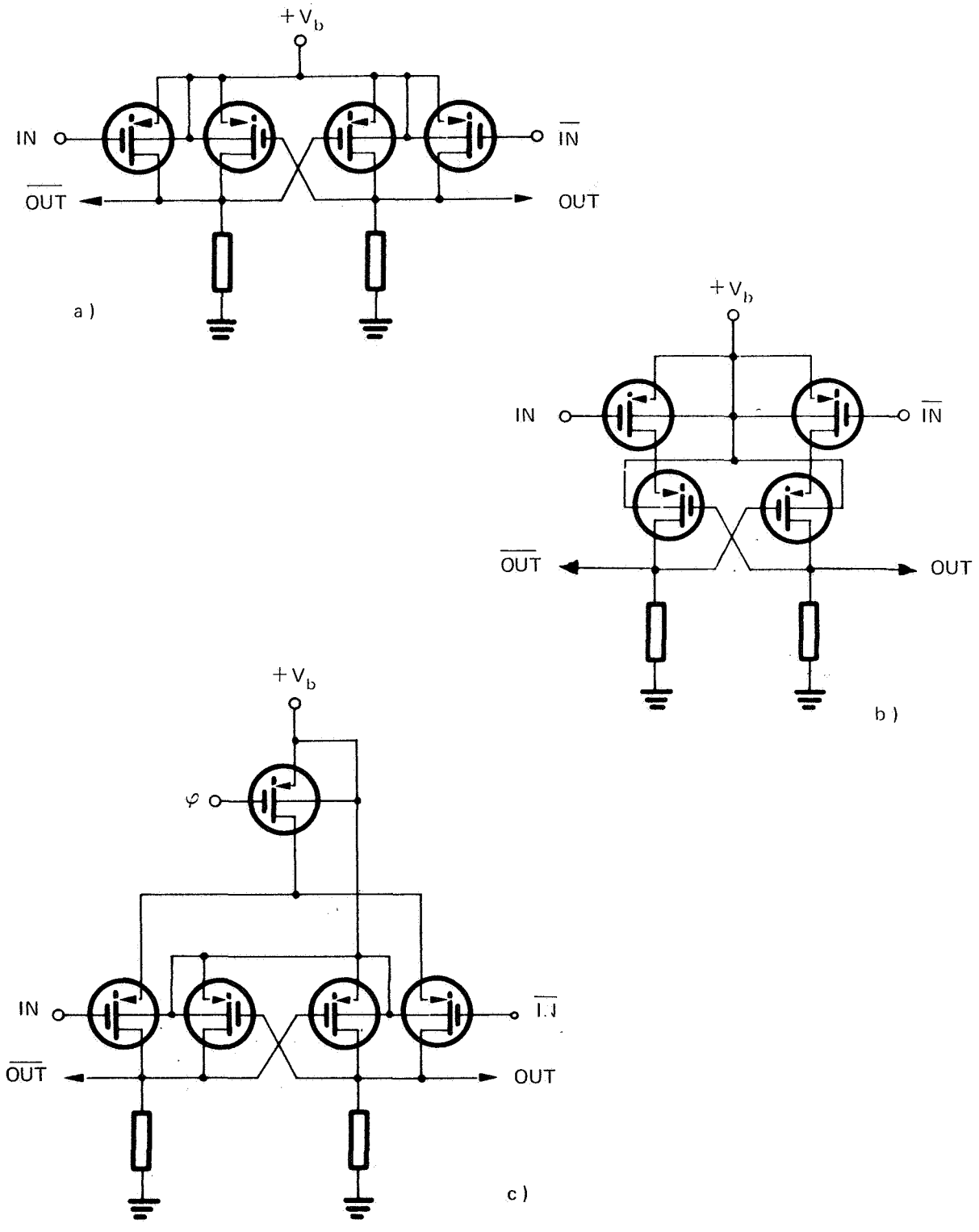


Figure 12.- a and b : R-S-flip-flop; c : D-Type flip-flop.

Two versions of another important logic circuit are shown in Figure 13, namely the half adder or modulo 2 adder.

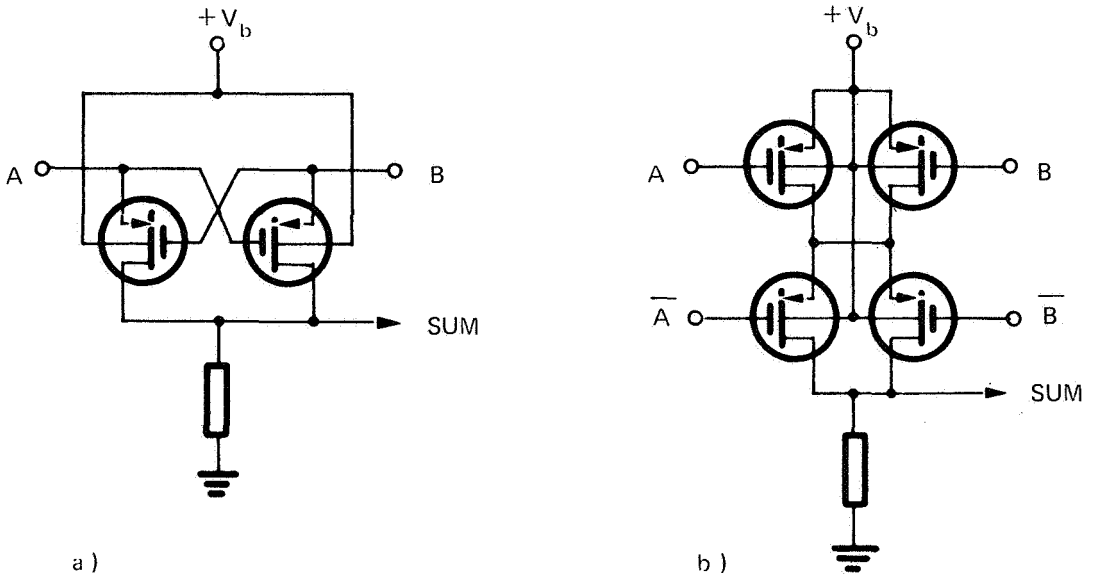


Figure 13.- a : half adder with 2 inputs ; b : half adder with 2 inputs and their complements.

The absence of a fixed supply voltage makes the adder of Figure 13 a rather critical if used in a complex configuration because a "voltage drop" strongly influences the inputs A and B.

Several other possible configurations for the half adder and full adder are shown in Farina and Trotter [7].

III. 2 Speed versus Power Consumption

III. 2. 1 Single-channel devices

The power consumption is different for the "on" and "off" state and can be expressed in the following equations :

$$P_{off} = \frac{V_b^2}{R_l + R_{off}} \quad (2)$$

$$P_{on} = \frac{V_b^2}{R_l + R_{on}} \quad (3)$$

where : P_{off} is the power in the off-state

P_{on} is the power in the on-state

V_b is the supply voltage

R_l is the load resistor

R_{on} is the channel resistance in the on-state

R_{off} is the channel resistance in the off-state

P_{off} is extremely low because $R_{off} = 10^{14}$ ohm.

P_{on} is dependent on V_b and the load resistor R_l with R_{on} as a device constant (usually from 100 ohm to 600 ohm).

i) According to (3), R_l should be made *as high as possible for low power consumption.*

The load which must be driven by each inverter is basically capacitive (see page 3 point c). The switching time therefore is mainly dependent on the product of the load resistor R_l and the load capacity. This influence is shown in Figure 14.

ii) According to the behaviour of the fall time in Figure 14, R_l should be made *as low as possible for high switching speeds.*

A compromise must be found between i) and ii).

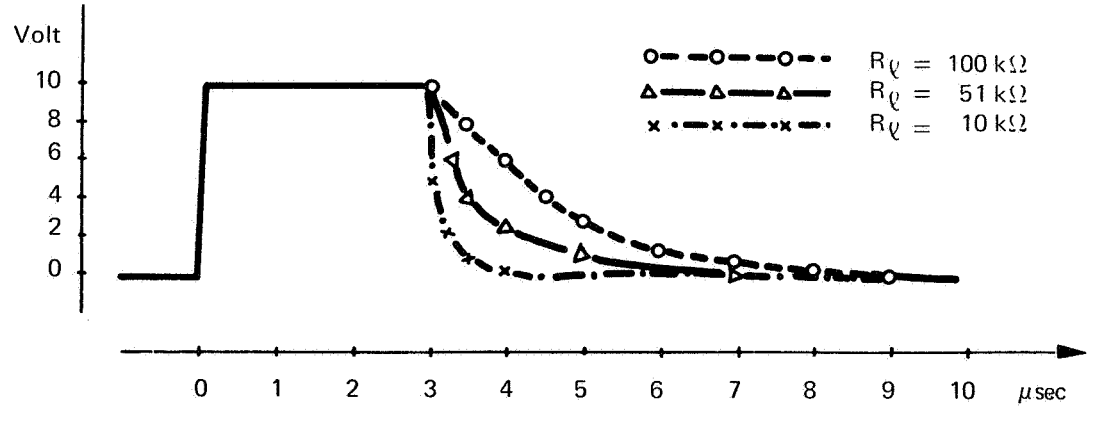


Figure 14.- Influence of load resistor R_l on the switching time of a P-channel device (curves are from Ref. 4 for the SC 1173 micro-circuit)

However, two effects which limit both the lowest and highest possible value of the load resistor R_l facilitate the choice.

a) *The lowest possible value of R_l* is determined by the "voltage drop" across the channel resistance of the device (see page 8, equation (1) .

If the maximal drop allowed in the output voltage V_{out} is k% of the supply voltage V_b then the minimum load resistor $R_{l\,min}$ can be derived from equation (1) :

Voltage drop = $V_b - V_{out} = V_b . k$

$$1 - \frac{V_{out}}{V_b} = k \tag{4}$$

$$\frac{V_{out}}{V_b} = 1 - k = \frac{R_{l\,min}}{R_{l\,min} + R_{on}} \tag{5}$$

From this : $$R_{l\,min} = (\frac{1}{k} - 1) . R_{on} \tag{6}$$

Example : V_b = 10 volt
max. allowable voltage drop = 1 volt
k = 10 %
R_{on} = 500 ohm

From (6) :

$$R_{l\,min} = 9 \cdot R_{on} = 4.5\ k\Omega$$

This result has been verified by experiment for the MOSFET SC 1173 (with R_{on} = 400 to 600 ohm) and has been published by Hauck [4] (see p. 30 of his report).

b) *The highest possible value of R_l* is determined by the "error output voltage" owing to leakage current in the off-state, which is influenced by heat, radiation and the connection of devices in parallel (as in page 8).

If it is assumed that the error output voltage is k% of the supply voltage V_b, the following is obtained :

error voltage = $V_b \cdot k = R_{l\,max} \cdot I_l$ (7)

where I_l is the sum of all leakage currents through R_l

From (7) :

$$R_{l_{max}} = k \frac{V_b}{I_l} \tag{8}$$

Example : V_b = 10 volt
max. allowable error voltage = 1 volt
k = 10 %
I_l = 5 μA

From (8) : $R_{l_{max}}$ = 200 kΩ

III.2.2. Complementary devices

The power consumption of complementary circuits is different from that of single channel devices. For both states one channel is always "off", i.e. non-conducting and the power is :

$$P_1 = \frac{V_b^2}{R_{off}} \tag{9}$$

The amount is extremely low because of the very high values of R_{off} (10^{14} ohm).

The only appreciable amount of power is used during the switching time for which :

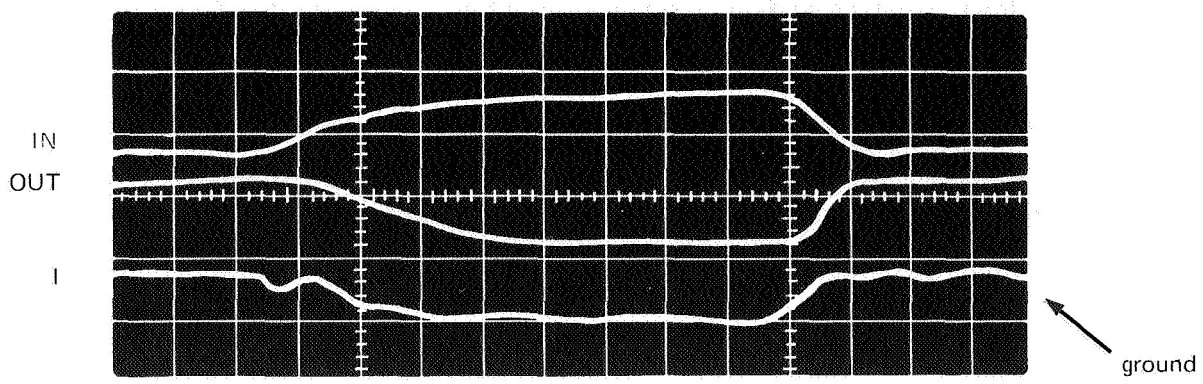
$$P_2 = V_b^2 \cdot C \cdot f \tag{10}$$

where : C is the sum of capacities to be loaded by the output during the transient switching time
f is the switching frequency (duty cycle).

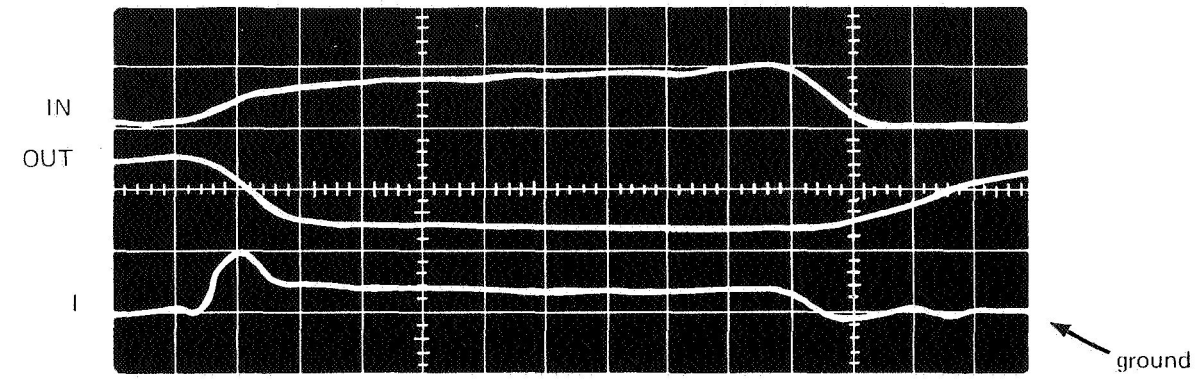
In Figure 15 the input(same for all three), output and current through the load resistor of three inverters are compared.

Figure 15a shows a P-channel inverter (2N 4352 from Motorola) with typical slow fall time and a current through the load resistor in the on-state of approximately 3 mA.

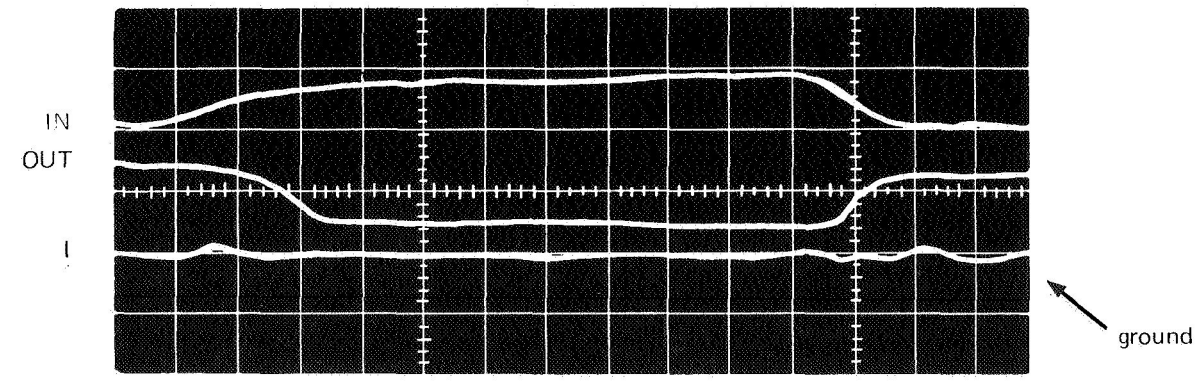
Figure 15b shows the inverse situation with a N-channel inverter (2N 4351 from Motorola) with a slow rise time and a current of approximately 2 mA through the load resistor in the on-state.



2N 4352 P-channel



2N 4351 N-channel



Complementary Circuit

Figure 15. - Power consumption of, a : P-channel ; b : N-channel and c : complementary inverter. (Scale : Horizontal 50 ns/cm - Vertical 10 volt/cm for "IN" and "OUT", 4 mA/cm for current I).

a : 2N 4352 P-channel. b : 2N 4351 N-channel. c : Complementary circuit.

The load resistors of both inverters are chosen to match the faster edge of the pulses to that of the complementary inverter.

This is shown in Figure 15c and is built from both devices shown above. The circuit has the rise-time of the P-channel inverter and the fall-time of the N-channel inverter, thus showing a better speed property. The current through the inverter is not measurable except for a few oscillations during the transient time.

To show this better a complementary R-S-flip-flop was built which is shown in Figure 16.

The current used by eight devices, has a maximum during the switching time of approximately 6 mA, but in the quiescent states is practically zero.

This shows clearly the huge advantage of complementary MOSFET logic over single channel MOSFET logic, when speed and power consumption are considered.

III. 3 Selection Considerations

Because no usable complementary integrated MOSFET system was on the market at the time of this report, single channel devices were used instead.

To minimize the leakage current, P-channel devices were used because at the time of the study their leakage properties were better than those of N-channel devices.

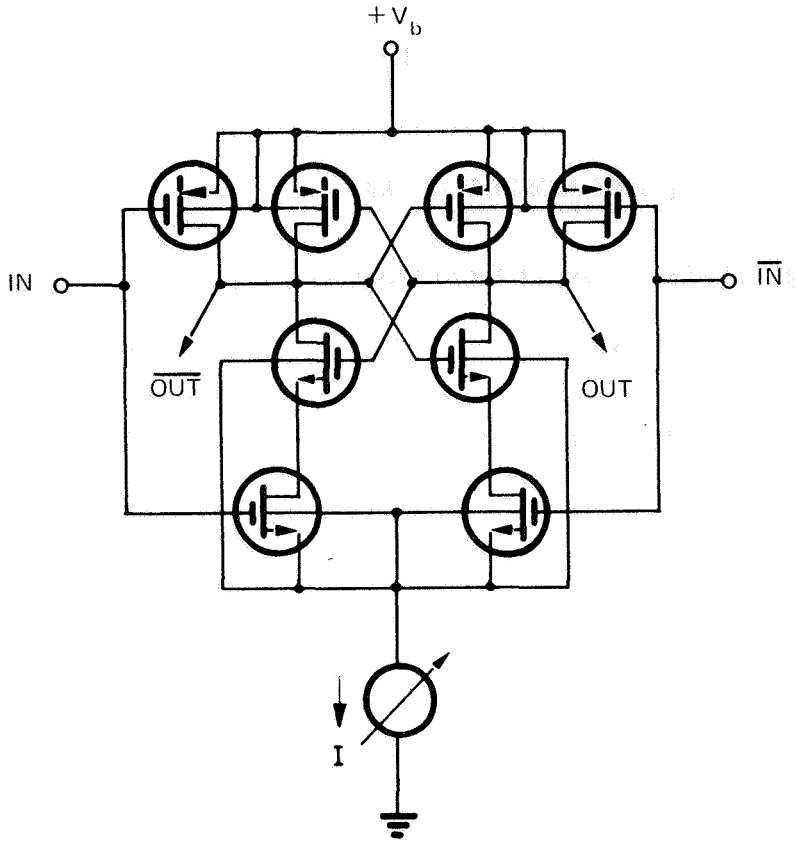
The "enhancement mode" of channel forming (see page 5) is particularly advantageous for integrated circuits, because this type does not conduct until the appropriate gate voltage is applied. Therefore several enhancement mode MOSFETs can be put on a common substrate without interaction.

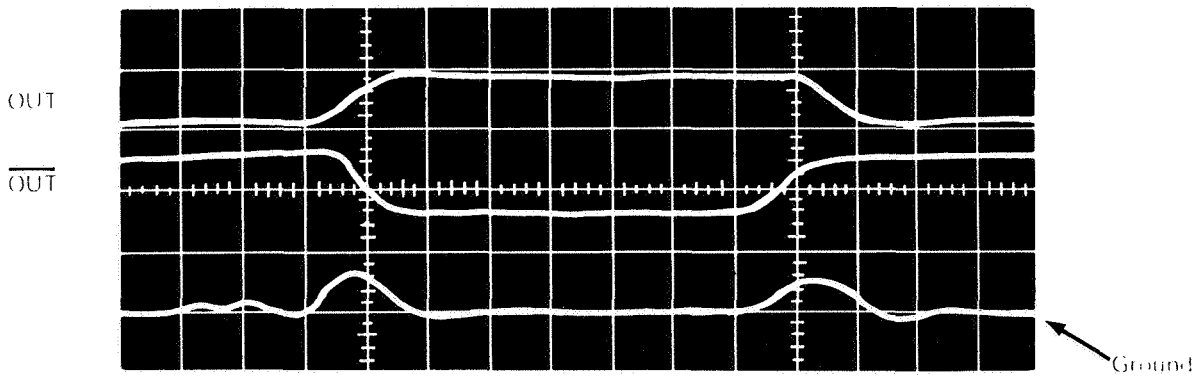
The MOSFET devices should be integrated into larger functional blocks such as counters, flip-flops, shift registers and multi-input gates for both signal directions.

The gate of each device should be protected against high voltage damages, due to excess charges built up by static charges in the environment. This is usually done with a zener diode from gate to substrate.

The devices should be operated with only one power supply.

The reliability of the devices should be established by either a sufficiently long test programme or by a "flight history" if possible.





Horizontal : 50 ns/cm

Vertical : 10 V/cm for OUT and $\overline{OUT}$

10 mA/cm for I

Figure 16. - Diagram and waveforms of complementary R-S-flip-flop.

These facts led to the decision to use the following MOSFET integrated blocks, produced by Philco-Ford Microelectronics Division and by American Micro-Systems Inc.

III. 4 Description of Integrated MOSFET Blocks

The logic blocks consist of three types :

Binary Counter	SC 1149
Three-Input Parallel Gate	SC 1173
Three-Input Serial Gate	SC 1128

They are formed with P-channel devices including protecting zener diodes from gate to substrate.

III. 4. 1 The binary counter SC 1149

The counter consists of two flip-flops in "master-slave" configuration, each consisting of 5 transistors.

One additional transistor for each flip-flop is used to "reset" it into the quiescent state. Both outputs and their complements are connected to external connection pins. The load resistors R_l are supplied externally. Their value determines the speed and power consumption according to section III. 2.

All gates are protected with a zener diode. The substrate is connected internally with the power supply input.

The internal configuration of the SC 1149 is shown in Figure 17, the wave-forms of the counter in Figure 18. Being a master-slave flip-flop, both inputs "IN" and "$\overline{\text{IN}}$" must be exclusive with respect to the 0 volt level (as shown in Figure 18). The circuit oscillates if both inputs are at ground at the same time.

The two outputs "OUT" and "$\overline{\text{OUT}}$" are always exclusive due to internal connections. It is therefore possible to use the outputs of one SC 1149 as inputs to another. It is also possible to complement a single inverter output via another inverter and use them as exclusive inputs, provided the fall time of the second inverter is slower than its rise time.

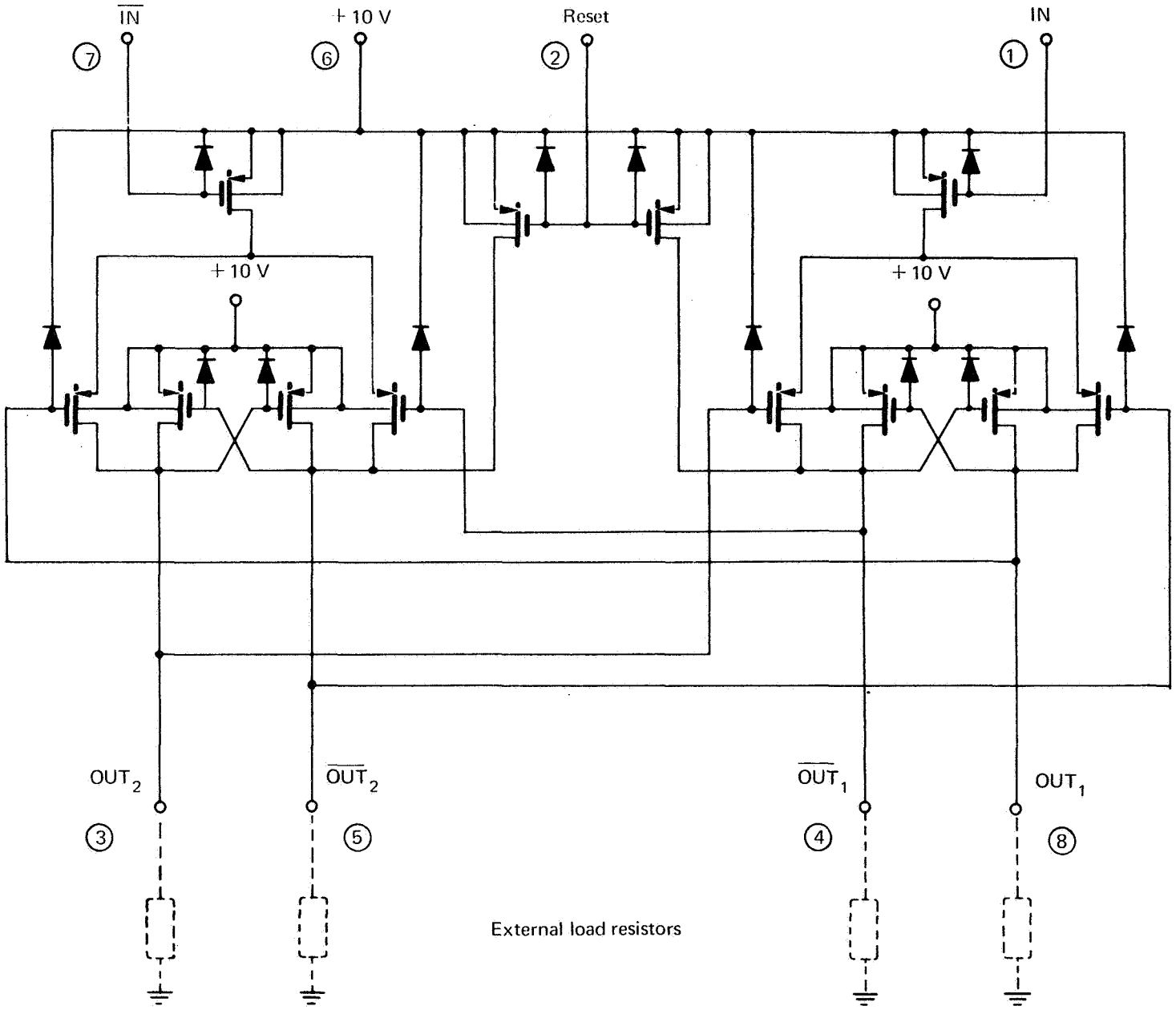


Figure 17.- Internal configuration of the SC 1149. (Numbers in circles are external connection pins).

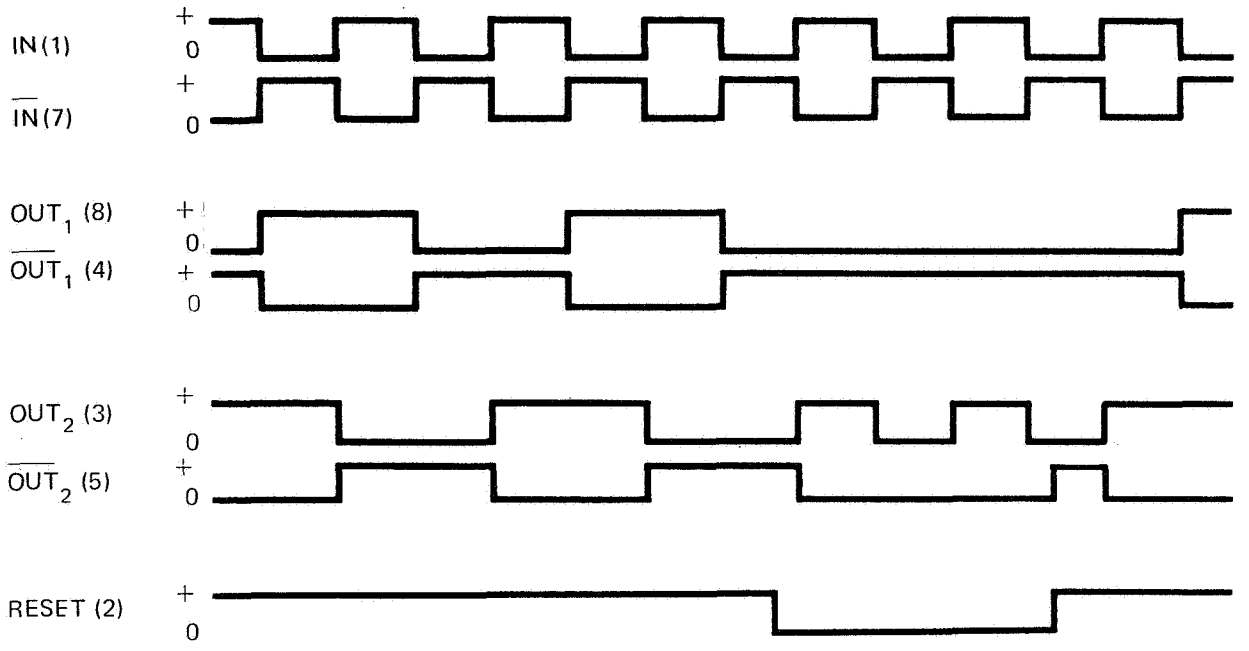


Figure 18. - Waveforms of the counter SC 1149.

It has been found, that the extreme values for the load resistor R_1 are between 50 kΩ and 200 kΩ (see Hauck [4]).

In the following, the symbol of Figure 19 shall be used for the SC 1149.

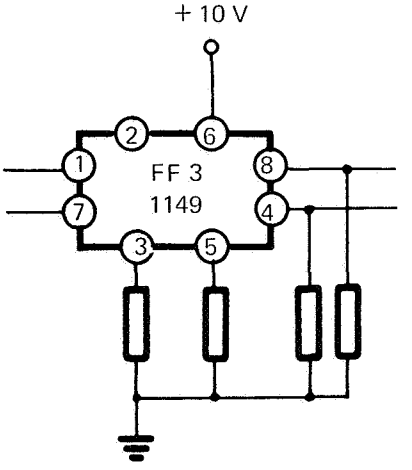


Figure 19. - Symbol for the SC 1149.

III. 4. 2 Three-input parallel gate SC 1173

This block is equivalent to the one shown in Figure 6 a. Its configuration and symbol is shown in Figure 20.

As R_{on} for one device is approximately 500 kΩ ,

$R_{l\,max}$ = 200 kΩ

$R_{l\,min}$ = 10 kΩ

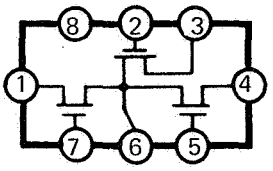


Figure 20. - Symbol for the SC 1173.

III. 4. 3 Three-input serial gate SC 1128

This logic block is equivalent to the one shown in Figure 5 a.

Its configuration and symbol are shown in Figure 21. The values of R_l are the same as for the SC 1173 above, as each individual transistor is basically the same for both blocks.

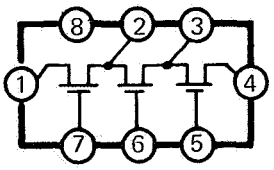


Figure 21. - Symbol for the SC 1128.

Combinations of several of these blocks require a new calculation for R_l as the values given above are valid for one single gate only.

All three logic blocks are mounted on TO-5 headers with eight pins. Additional information on switching times, temperature influence, etc. can be found in Hauck [4].

These 3-input configurations are very versatile when used to construct flip-flops, matrices, adders, NAND-gates and NOR-gates, as will be shown in the following section.

IV. SYSTEM REALIZATION

In this section a realization of the individual sub-units shown in Figure 1 will be described in terms of logic diagrams, pulse diagrams, transistor schematics and interconnection diagrams.

Throughout the whole system *trailing edge logic* will be used, because pulsed dynamic logic presents a certain noise danger to the capacitive inputs of the MOSFET circuits.

IV.1 Frequency Divider

Basically the frequency divider consists of SC 1149 binary counting blocks, connected in cascade as shown in Figure 22.

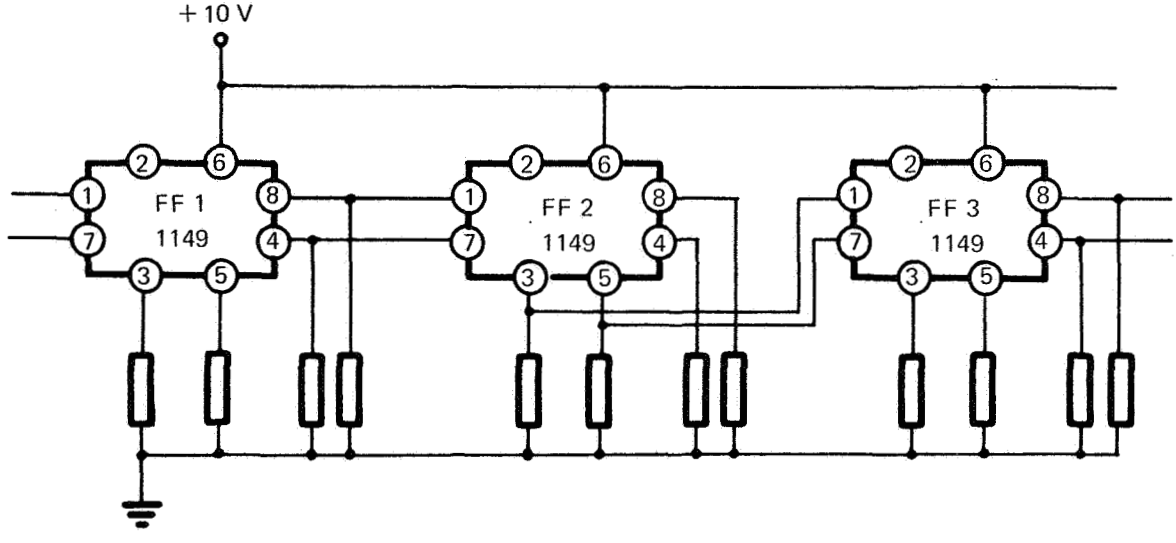


Figure 22.- Three stages of the frequency divider.

Two versions of cascading are shown. If outputs 1/8 and 1/4 (read : output 8 and output 4 of flip-flop FF1) are used as inputs to FF2 the pulse diagram corresponds to that shown in Figure 18.

However if outputs 3 and 5 are used as inputs to the next flip-flop (2/3 and 2/5 in Figure 22) the output waveforms of FF3 are shifted by a half period of FF2.

In the following both outputs OUT_1 (8 and 4) and OUT_2 (3 and 5) will be used as timing signals for various sub-units.

VI. 2 Code Generator

The code generator produces a pulse sequence with very good autocorrelation properties for synchronization purposes. Such sequences are described in Pettit [8]. For our example a double-folded 11-bit Barker Code is chosen. Each fold has as pulse sequence :

1 1 1 0 0 0 1 0 0 1 0

The pulse diagram of each fold (BC 1 and BC 2) and the double-folded result (BC) are shown in Figure 23.

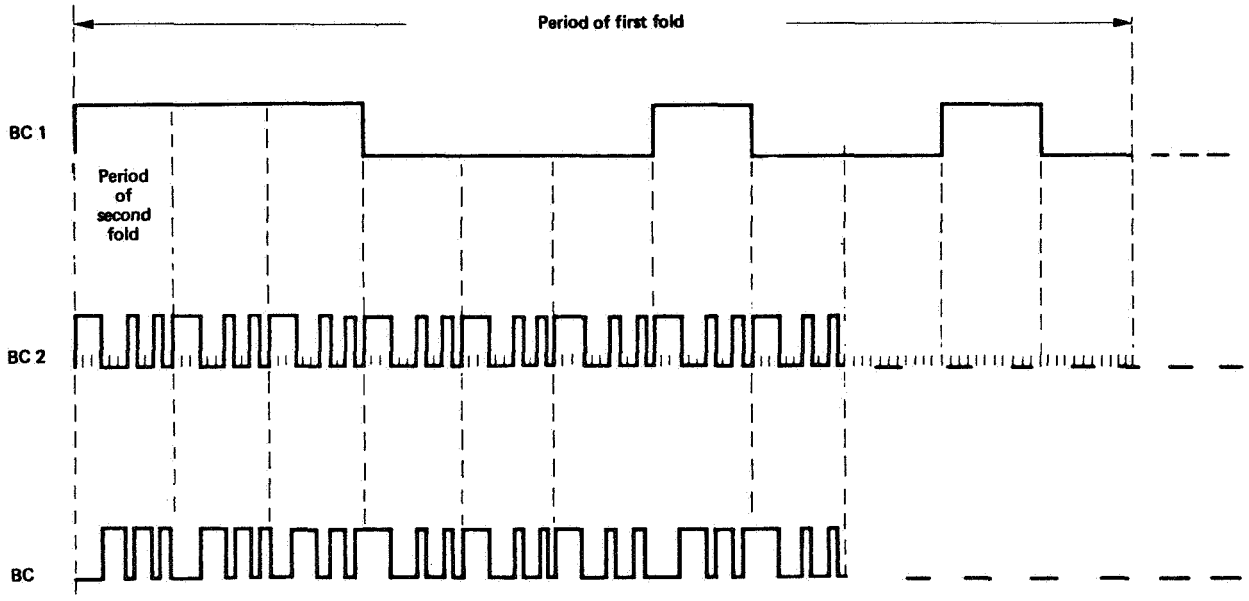


Figure 23.- Double-folded 11-bit Barker Code.

According to an evaluation of several methods for the generation of Barker Codes[9] binary counters are used together with decoding matrices for each fold. Their outputs then are added modulo 2 to achieve the resultant pulse pattern BC of Figure 22.

IV. 2. 1 11-Bit counter

It has been assumed that the input frequency of the generator lies in the same order of magnitude of the stage delay of the SC 1149 blocks (which is around 1.5 μs) or is even smaller.

Therefore the simple implementation with a ripple-counter is not possible.

A parallel (synchronized) counter would eliminate the delay effects but only with a huge complexity.

Therefore a mixed "parellel-ripple" counter will be used with delays, which are present but halve the value of the frequency of the input signal. It will be shown that the resulting erroneous signals can be suppressed after the modulo 2 addition.

Figure 24 shows the schematic of the parallel-ripple counter where four stages form a ripple counter, but in which the inputs of the first stage of the second ripple block are synchronized to the first block.

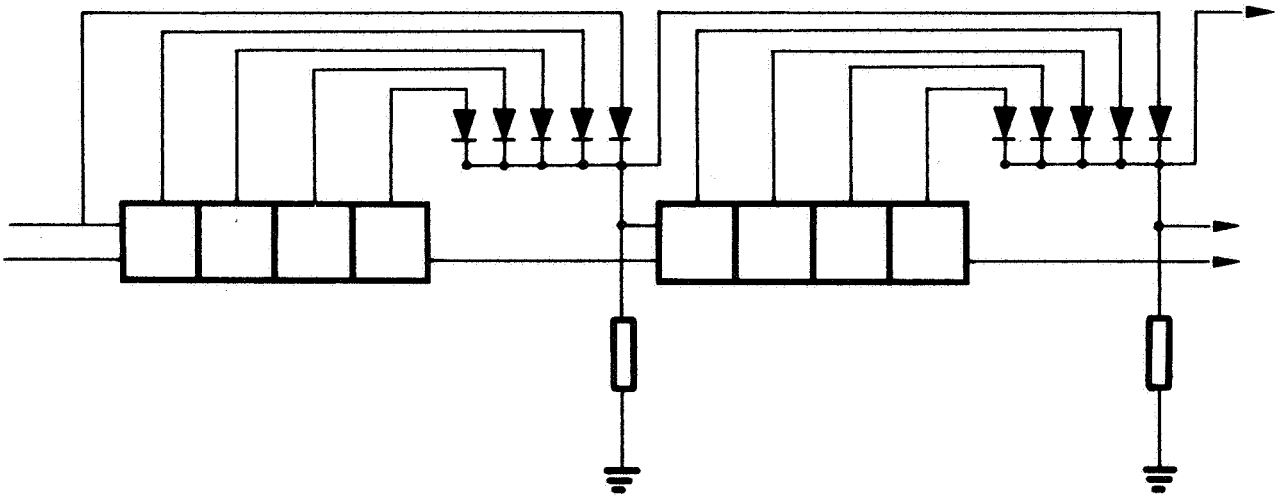


Figure 24. - Schematic of parallel-ripple counter.

Each counter (which would count to 16) must be *reset* to zero after having counted to 11 (length of Barker Code). This is shown in the pulse diagram of Figure 25.

The reset conditions, shown as crosses in the diagram, are :

$\text{Reset}_1 = (1/7) \cdot (1/3) \cdot (2/8) \cdot (4/8)$

where ( ) · ( ) = AND function.

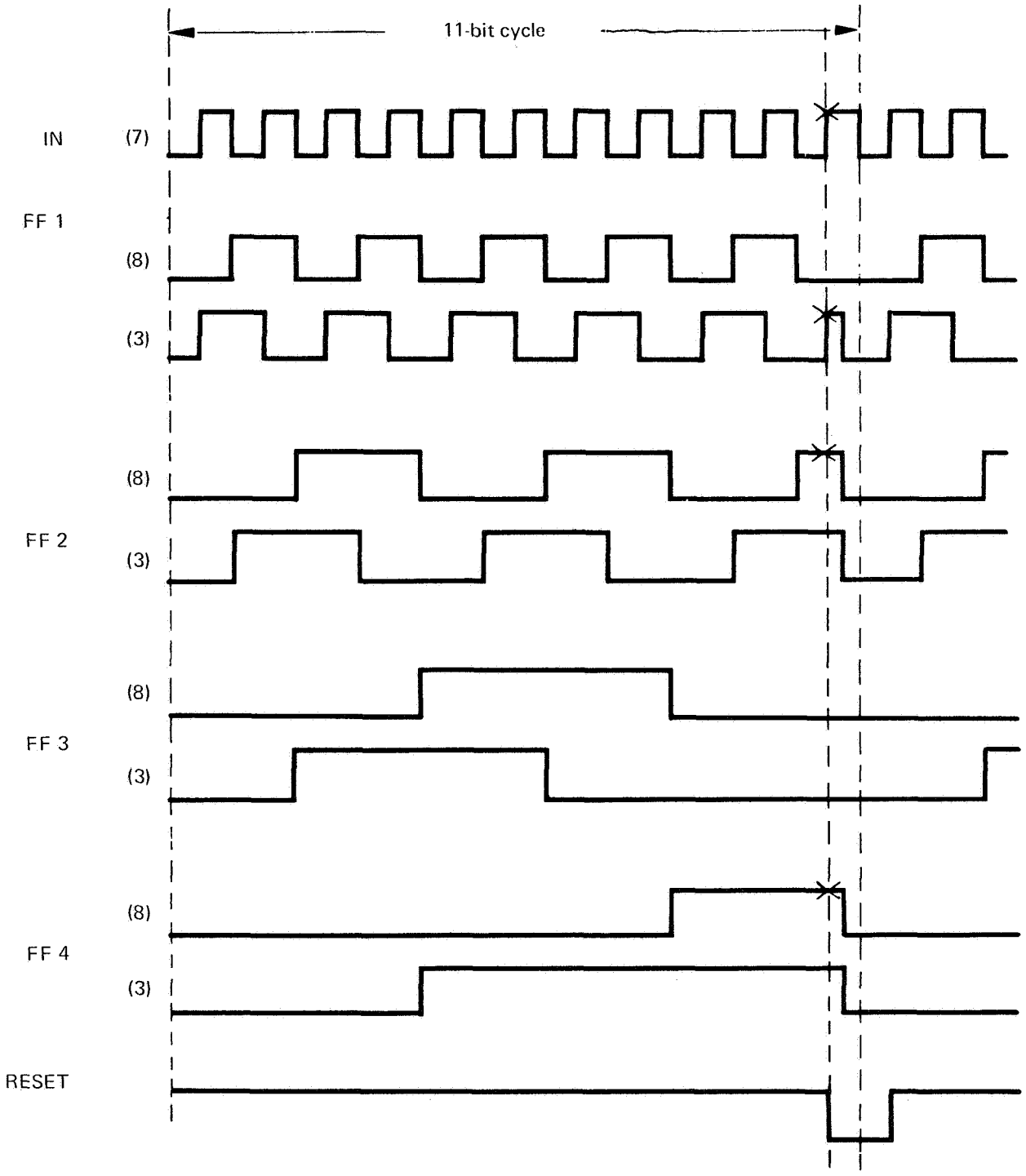


Figure 25. - Pulse diagram of 11-bit counter with reset.

To avoid any hazard, the reset conditions are used to set a flip-flop, which must be in a stable state before it resets the counter. This reset flip-flop is set back to its original state by the slave output$_2$ (pin 5) of the stage driving the input of FF1, which appears between the two dotted lines in Figure 25.

This reset can be used as synchronization of the next 11-bit block, if the reset pulse is used as input to the next group.

The reset condition for the second block corresponds to reset$_1$:

$$Reset_2 = (Reset_1) \cdot (5/3) \cdot (6/8) \cdot (8/8)$$

The whole counter with reset matrices and flip-flops is shown in Figure 26.

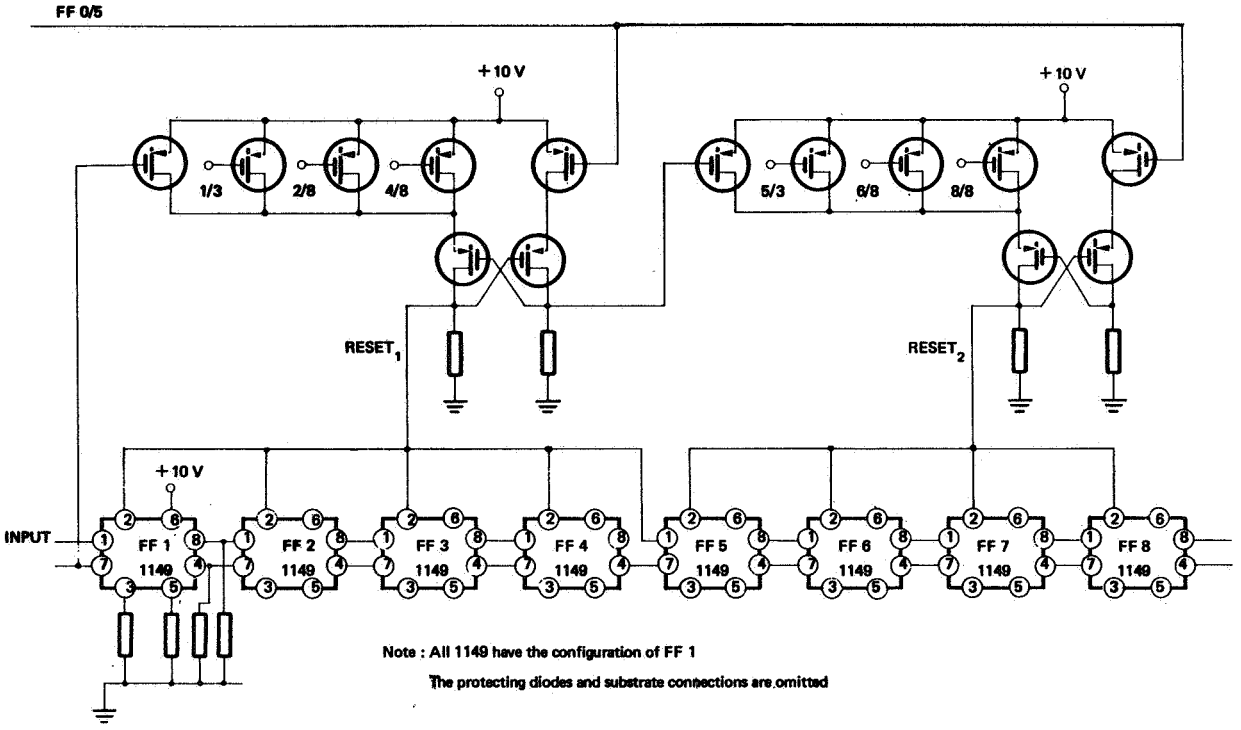


Figure 26. - 11-bit counters with synchronization.

In Figure 27 the interconnection diagram is shown for the reset-matrices and flip-flops.

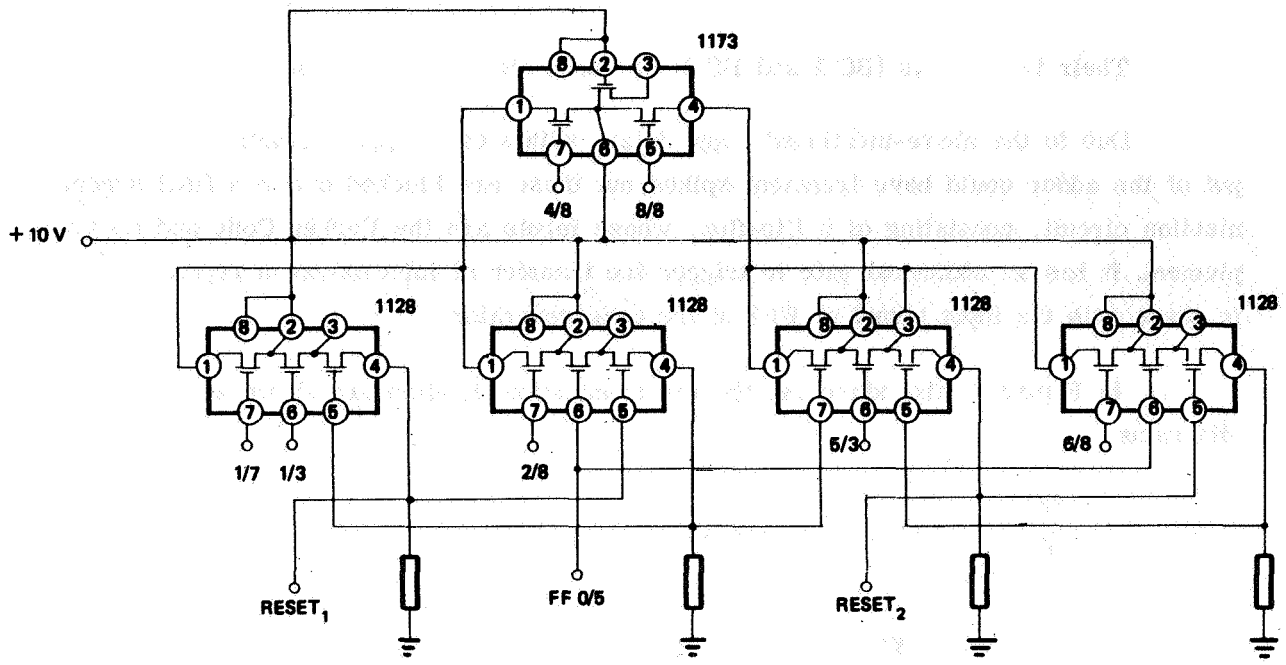


Figure 27. - Interconnection diagram for reset circuits.

IV. 2. 2 Barker Code matrix

Out of the 11 different states of each counter group whose pulse forms are given in Figure 25, the 11-bit Barker Code (11100010010) is decoded.

Both sequences have to start, when the counters are reset. The matrices are shown in Figure 28.

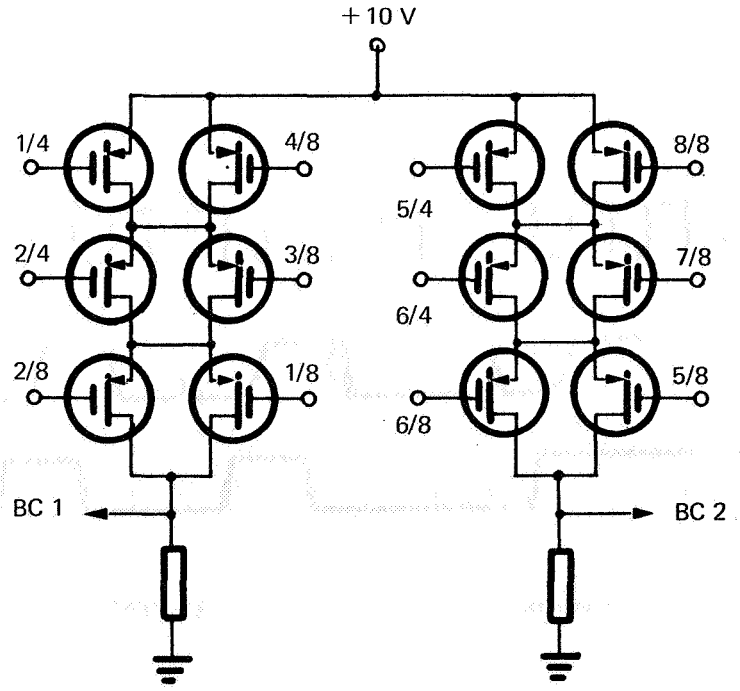


Figure 28. - Barker Code matrices

Their two outputs (BC 1 and BC 2) are used as inputs to a modulo 2 adder.

Due to the above-mentioned stage delays within each ripple counter block, the output of the adder could have transient spikes but these are blocked out in a final synchronization circuit, consisting of a flip-flop, whose inputs are the Barker Code and its complement. It has an additional gate to trigger the transfer of information at regular intervals in phase with the input signal of FF1 of the code generator.

In Figure 29 the adder and the synchronization flip-flop are shown with their pulse diagrams.

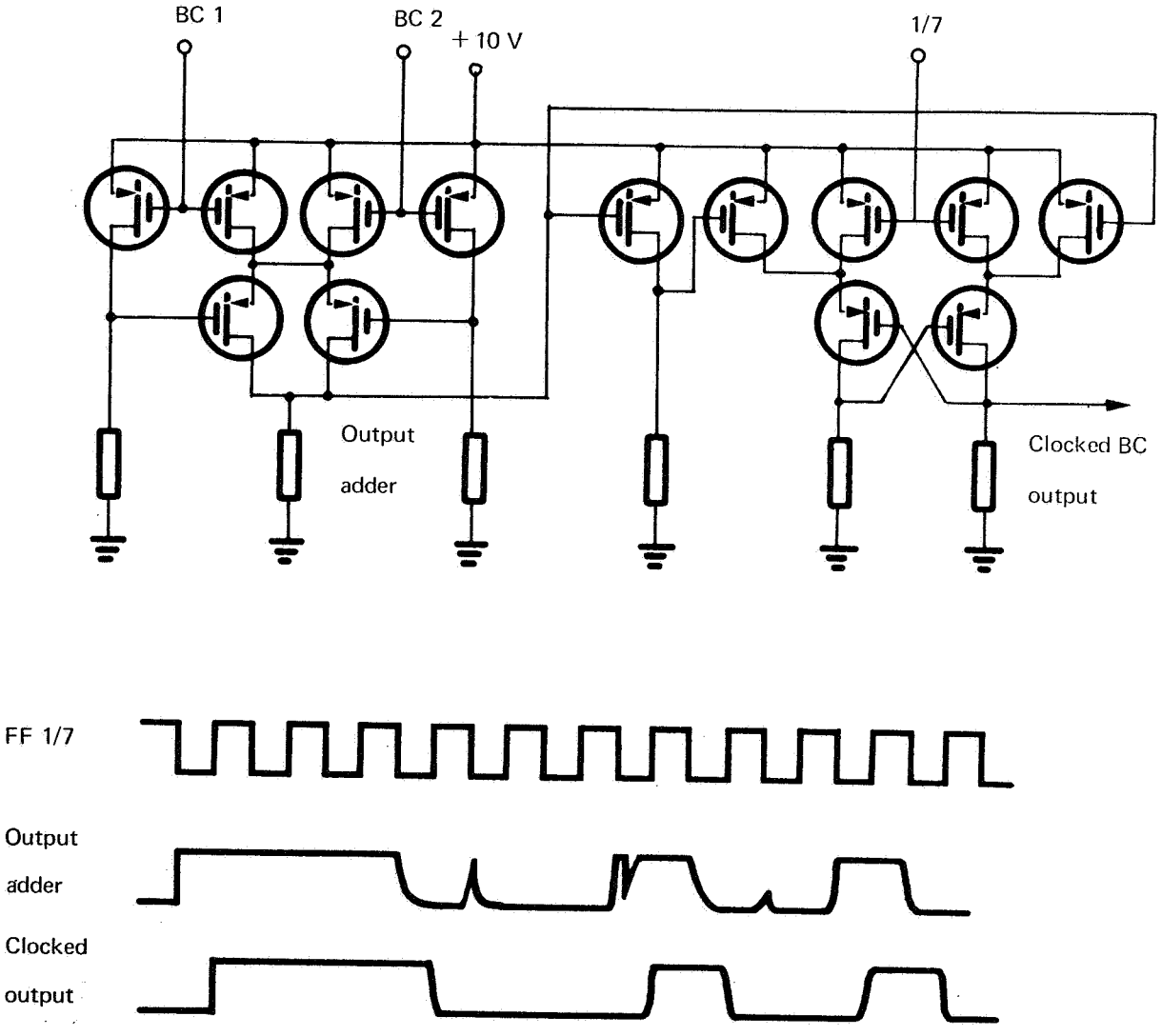


Figure 29.- Transistor schematic and pulse pattern of adder and synchronization flip-flop.

IV.3 Command Sub-unit

This sub-unit gives at specified times a certain number of signals, which can be used for commanding and controlling several operations in the whole system.

The unit consists basically of a part of the frequency divider as time reference and of a decoding matrix.

The matrix itself consists of MOSFET blocks in special serial and parallel configuration, similar to those shown for the Barker Code generator.

The exact configuration depends on the pulse pattern required.

IV.4 Input Sequencer and Buffer

This sub-unit, according to Figure 1, provides analogue and digital data at the appropriate time to the multiplexer (commutator), and could therefore be described as being a part of the multiplexer.

However in a spacecraft there are generally many scientific and house-keeping data to be transmitted, where especially the latter quite often have to be measured at specific times, out of phase of the multiplexer.

Therefore this sub-unit will be considered as an independent unit.

Analogue data are transferred to the A-D converter and kept there after the conversion to be multiplexed. This is done with due consideration of the converting time.

Digital data are transferred into buffer registers and kept there till they are multiplexed.

Data without specific restrictions concerning the measurement time are transferred directly into the multiplexer.

In Figure 30 the transistor schematic and two possible versions of interconnection are shown for one stage of a buffer register.

A signal at the input "t" transfers the data, which are present at the inputs "in" of all stages of the register, into the register.

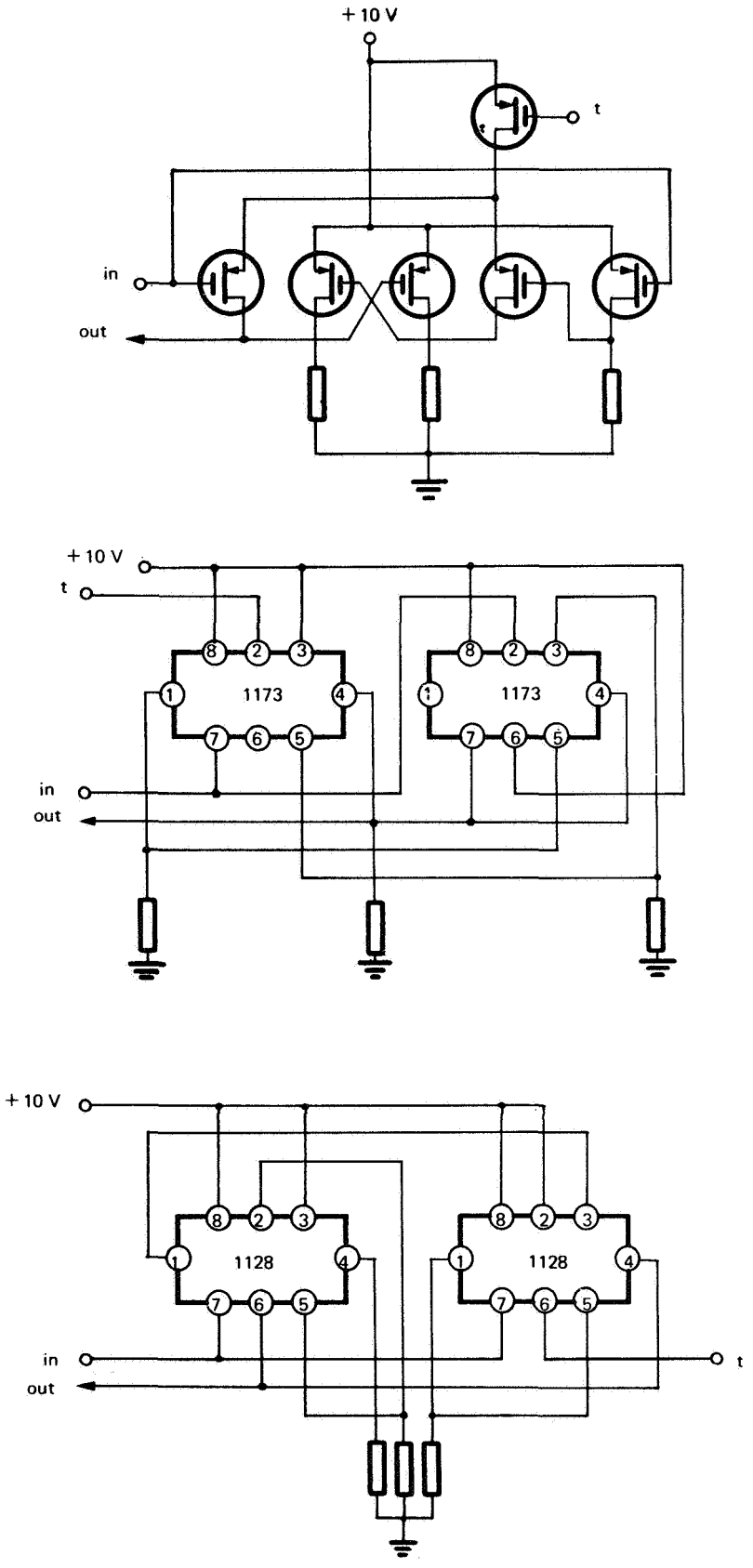


Figure 30.- Transistor schematic and interconnection diagram of register stage.

The contents can be read out by the multiplexer at any time without destroying it.

In Figure 31 the sequencer is shown for analogue data.

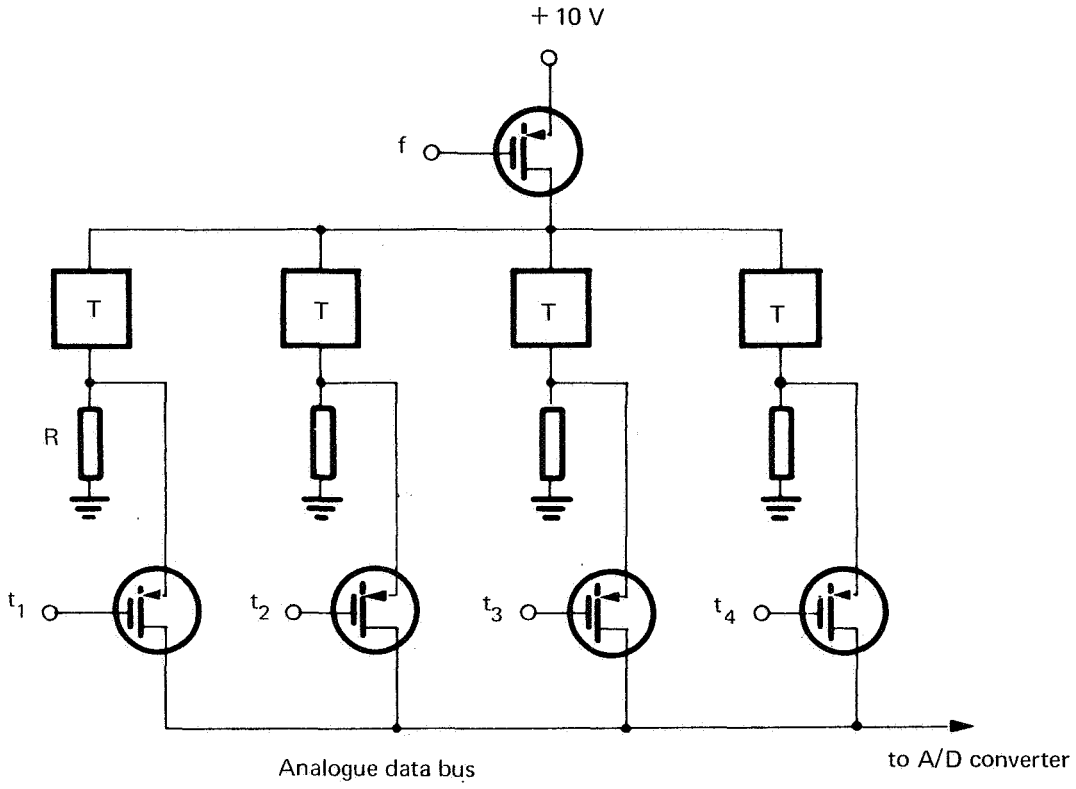


Figure 31.- Schematic of analogue data sequencer
(Each box with T is a simplified representation
of a thermistor and resistor network)

As an example, four temperature measurements were chosen, where thermistors are switched at certain times "t" on a bus line, which leads to the input of the A-D converter.

An additional signal "f" on the top switch supplies as "frame signal" the supply voltage to the whole group only when needed.

This configuration has certain limits set by the ratio of the sum of leakage currents of the closed switches to the current through the one open switch, which again is limited by the "On" channel resistance. The sum of this resistance and the ground resistor R is important, because it forms the input resistance to the A-D converter.

The time sequence signals t_i (see Figures 30 and 31) are produced the same way as the command signals, by decoding signals from the frequency divider in a decoding matrix. The timing of t_i is completely independent of the multiplexer and can be selected according to the time, when a certain value should be measured.

IV.5 Analogue Digital Converter

At the time of study, which led to this report, it was advisable to build a complete A-D converter with MOSFETs, bipolar transistors and a resistive ladder network. This single converter was used for all analogue data. More recently several A-D converters in integrated form have become available.

This new development will eventually lead to a configuration, where the sequencer plus following single A-D converter is replaced by a converter for each analogue value to be measured.

However to continue with the system described in Figure 1, a simple four-bit A-D converter is described, built of the above mentioned components.

Figure 32 shows the block diagram of the converter.

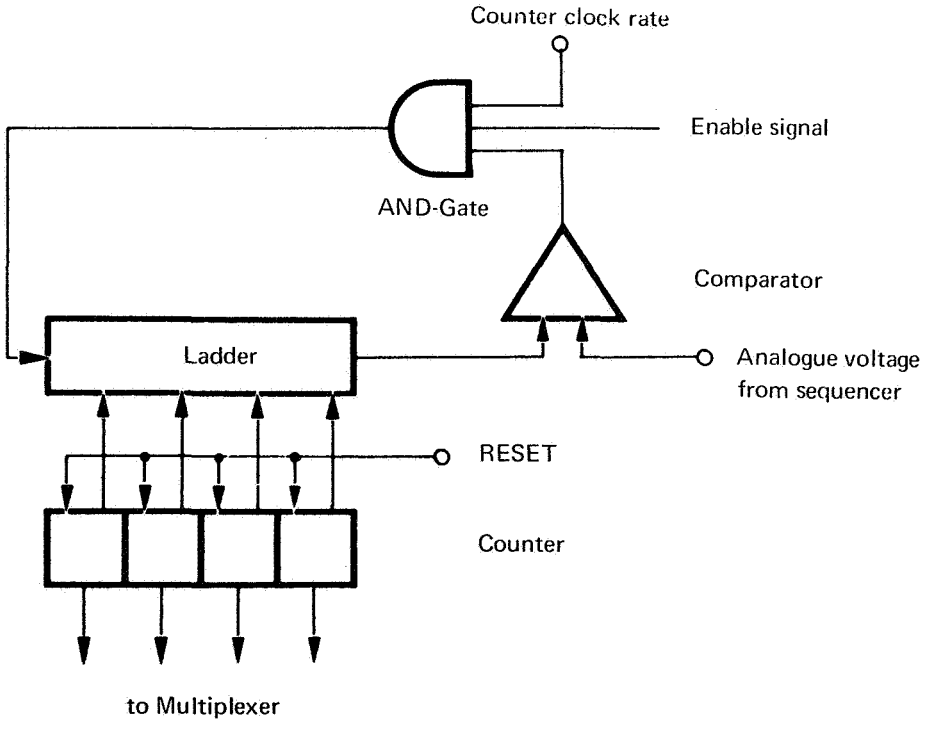


Figure 32.- Block diagram of the A-D converter.

The analogue voltage from the buffer sequencer goes to a *comparator circuit,* which consists of a difference amplifier with a constant emitter current source. The second input to the comparator comes from a resistor network of the usual R-2R-type. This ladder is switched by a four-stage binary counter (SC 1149), which counts from zero to 16, driven by a constant clock signal.

According to the binary number in the counter the voltage output of the ladder network increases in binary steps till its value is equal to, or bigger than, the analogue value. This condition is sensed by the comparator which stops the counter by closing the input gate of the clock signal. The number in binary form is the digital equivalent of the analogue voltage, and is stored in the counter till it is read out via the multiplexer to the parallel-serial converter.

Figure 33 shows the complete schematic of the A-D converter.

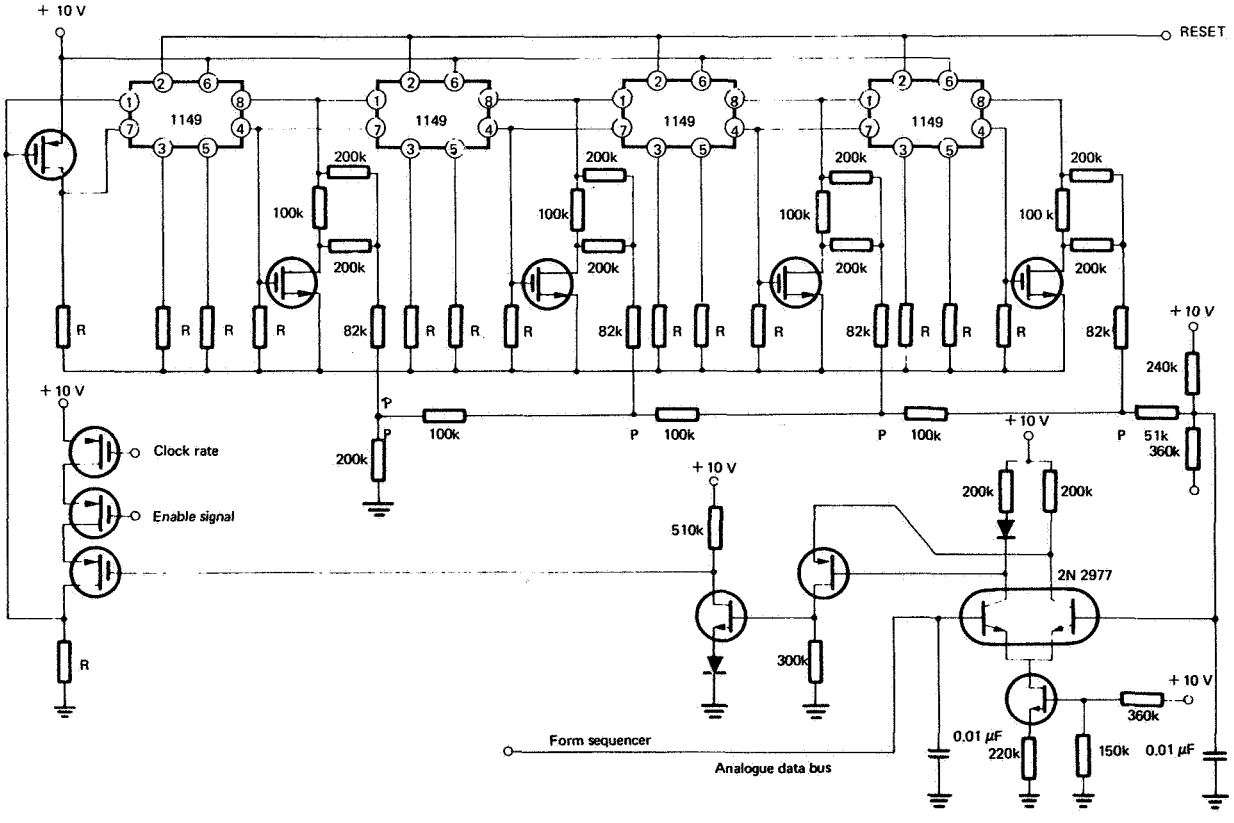


Figure 33. - Complete A-D converter

The ladder switch needs to be explained in more detail* . The principle of the ladder is based on the fact, that a node "P" (see Figure 33) must sense the value R to the left and to the right (R = 100 K). To do this constantly when being switched to ground and to the positive voltage, the branch of the ladder going up to the switch must always show 2R.

The switch (N-channel MOSFET) uses one output of the SC 1149 as gate input, and the other, complemented output as power supply.

When the gate is grounded, the power supply is positive, but the switch is non-conducting. The node P therefore senses 200 K (= 2R) towards the positive supply. If the gate is positive and the switch conducting, the power supply is at ground potential. Therefore the node P again senses 200 K, but now towards ground.

This ladder switch uses practically no power.

IV.6 Multiplexer

The multiplexer consists of a simple MOSFET switch for each bit of each digital value coming from the A-D converter and from the input buffers.

The switches are opened by signals, which are supplied again by decoded states of the frequency divider.

For a large number of channels it is convenient to use the direct connection property of MOSFETs to build a tree structure, thus minimizing the size of the decoding network, which supplies the timing signals.

Considerable progress has been made in this field recently, as there are integrated circuits now available, containing 4 to 16 channel MOSFET multiplexers on one chip (for example MEM 2002, 2003, etc. from General Instruments). Some include the whole address system.

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* This circuit was proposed by L. Jacobson in 1966 while working at the Center for Space Research of the Massachusetts Institute of Technology, Cambridge.

IV.7 Parallel Serial Converter

This sub-unit converts a full word into a serial bit stream for transmission. This can be done either by a multiplexer or by a shift register, which is loaded in parallel and emptied serially.

In Hauck [4] a 4-bit shift register is described using 18 integrated blocks (SC 1128 and 1173). At present, however, there is on the market a wide variety of MOS shift registers on one chip, having the "parallel in/serial out" characteristics (Philco-Ford, General Instruments). The ratio of 18 : 1 of the number of integrated blocks for a 4-bit shift register makes the old version rather obsolete and therefore is not treated here.

V. CONCLUSION

The experiments reported here prove that a digital sub-system for a small scientific spacec raft [4] can be built with a total power consumption of less than 500 mW with 950 MOS transistors (in integrated circuits) and 25 bipolar transistors.

As MOS technology is particularly applicable to large scale integration a tremendous reduction in space can be expected in the near future. Another big step will have been made when the complementary MOS technology leaves the laboratory stage. Its possible application to spacecraft electronics has been demonstrated.

ACKNOWLEDGEMENT

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REFERENCES

1. Harrington, J.V. et al. — Study of a Small Solar Probe (SUNBLAZER), Part I and II, Report Nr. PR 5255-6, Center for Space Research, M.I.T., Cambridge, Mass., July 1965.

2. Lumb, D.R., Hofman, L.B. — An Efficient Coding System for Deep Space Probes with Specific Application to PIONEER Missions, *NASA TN D-4105,* August 1967.

3. Lokerson, D.C. — Implementation of the AIMP D and E Telemetry Encoding System Employing MOSFETs, *Goddard Space Flight Center X-711-66-340* Greenbelt, Md, July 1966.

4. Hauck, H. — The Digital Subunit of SUNBLAZER, *Technical Report CSR-TR-67-5,* Center for Space Research, M.I.T., Cambridge, Mass., July 1967.

5. DeAtley, E.R. (ed.) — MOS Monolithic Subsystems : A Revolution in Microelectronics, Philco-Ford Microelectronics Division, Santa Clara, Cal., 1966.

6. Wallmark, J.T., Johnson, H. (ed.) — *Field Effect Transistors, Physics, Technology and Application,* Prentice Hall Inc., 1966.

7. Farina, D.E., Trotter, D. — MOS Integrated Circuits Save Space and Money, *Electronics,* 4 October 1965, p. 94.

8. Pettit, R.H. — Pulse Sequences with Good Autocorrelation Properties, *The Microwave Journal,* February 1967, p. 63-67.

9. Hauck, H. — On the Generation of Barker Codes, European Space Research Organisation, *ESRO TN-7,* September 1967.

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