NASA CONTRACTOR REPORT

NASA CR-1347

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RELIABILITY HANDBOOK FOR SILICON MONOLITHIC MICROCIRCUITS

Volume 2 — Failure Mechanisms of Monolithic Microcircuits

by Wilburn O. Shurtleff

Prepared by
TEXAS INSTRUMENTS INCORPORATED
Dallas, Texas
for George C. Marshall Space Flight Center

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION • WASHINGTON, D. C. • APRIL 1969

NASA CR-1347

RELIABILITY HANDBOOK FOR SILICON MONOLITHIC MICROCIRCUITS

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Issued by Originator as Report No. 03-67-04

Prepared under Contract No. NAS 8-20639 by
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NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

For sale by the Clearinghouse for Federal Scientific and Technical Information
Springfield, Virginia 22151 – CFSTI price $3.00

FOREWORD

This handbook was prepared as an aid in determining the most effective application, testing, handling, and quality and reliability assurance controls for integrated circuits. It was compiled in two books of two volumes each and deals primarily with the subjects of application, failure mechanisms, failure analysis, and reliability assessment. Some similarity may be noted between NASA CR 1110, "Microelectronic Device Data Handbook," and the data presented herein; however, NASA CR 1110 deals with microcircuits in general, while this document was prepared as a reliability handbook and deals with monolithic microcircuits only.

The effort resulting in the publication of this handbook was produced under the technical direction of the Parts and Microelectronics Technology Branch, Future Programs and Technology Office, Quality and Reliability Assurance Laboratory, George C. Marshall Space Flight Center, Alabama.

D. Grau
Director, Quality and Reliability
Assurance Laboratory

PREFACE

This publication, "Failure Mechanisms of Monolithic Microcircuits," is Volume 2 of a four-volume series entitled, "Monolithic Microcircuits Reliability Handbook." The Handbook was prepared for the National Aeronautics and Space Administration by Texas Instruments Incorporated, under Contract NAS 8-20639. The Handbook series consists of the following volumes:

Volume 1	Application of Monolithic Microcircuits
Volume 2	Failure Mechanisms of Monolithic Microcircuits
Volume 3	Failure Analysis of Monolithic Microcircuits
Volume 4	Reliability Assessment of Monolithic Microcircuits

The purpose of the Handbook is to provide aid in determining the most effective application and understanding of monolithic microcircuits, and the most effective quality and reliability assurance controls for the circuits.

Volume 2, "Failure Mechanisms of Monolithic Microcircuits," describes:

- Failure modes and mechanisms.
- The severity of the principal failure modes and mechanisms.
- A comparative evaluation of the frequency of occurrence of the principal failure modes and mechanisms.
- The failure modes and mechanisms associated with:
    - Packaging
    - Mounting of semiconductor chip or die.
    - Metallization and interconnection system.
    - Mask alignment.
    - Silicon dioxide defects.
    - Diffusion.
    - Electrical isolation and interaction between the various elements of the chip.
- Definition and identification of a type of control, inspection or screening test that is effective in detecting, for screening purposes, each of the principal failure modes and mechanisms.

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VOLUME 2

FAILURE MECHANISMS IN MONOLITHIC MICROCIRCUITS

SECTION I

INTRODUCTION

A. GENERAL

This volume of the Reliability Handbook discusses defects that are introduced into monolithic microcircuits during the various processes of manufacture, the impact of these defects on microcircuit failure rates, and the techniques that are used to correct or remove the defects from the processes. The techniques of processing that are used in the manufacture of monolithic microcircuits are sophisticated, numerous and complex. There is a finite probability that defects are introduced at each each step of the manufacturing process. These defects are of concern to both the manufacture and the user of monolithic microcircuits in two major respects:

- Defects reduce the effective yield of the manufacturer, thereby increasing the cost of each microcircuit bought by the user.
- Defects may cause microcircuit reliability problems which adversely affect the user's end product and the reputation of the microcircuit manufacturer.

It is essential, therefore, that defects be identified and that corrective actions and screening procedures be implemented to minimize the effect of imperfect processes.

Every manufacturing process produces varied results. The effect of variations within a given process is that the distribution of pieces will range from nearly perfect to totally unacceptable. The manufacturer must determine what degree of imperfection will affect the acceptability or reliability of his microcircuit. When this degree of imperfection is determined, his defect criteria is set. If the standard is set too high, acceptable parts are rejected and microcircuit cost is increased. If the criteria is set too low, defective parts are accepted and the microcircuit cost is increased. In the latter case, acceptable parts are sometimes manufactured which fail in system application at some later date; these are reliability failures.

The random distribution of parts which may occur within a given process is more readily divided into three categories:

- White. These pieces are totally acceptable and cause no problems with subsequent process yields or device reliability.
- Gray. It is not known whether these pieces are good or bad. They may fall out in later processing or be screenable from end products if bad. They may also cause reliability failures.

- Black. These pieces are totally unacceptable. Further processing would result in increased microcircuit cost from yield loss.

Most reliability failures result from the processing of "gray" category devices. These reliability failures are usually escapes from a screening process that is designed to remove the potentially unreliable pieces from the "gray" category.

B. DEFINITIONS

New terms and definitions are necessary to clarify the terminology which has arisen with the growth in manufacture and application of monolithic microcircuits. Although the terms "defect," "failure mode," and "failure mechanisms" are common among manufacturers and users of monolithci microcircuits, unfortunately, these terms have different meanings to different people. Also, they are fairly broad in nature and do not define exactly the information which is of concern to the manufacture and user of monolithic microcircuits. The following characterizations cover the varied combinations of information which are frequently encountered under "defect," "failure modes." and "failure mechanisms," and they provide complete and consistent terminology:

- Detector
- Indicator
- Physical cause of failure
- Design, process, or application cause of failure
- Generator
- Part or area affected

One or more of the first three characterizations is usually included under the term "failure mode." The last item is usually associated with the term "defect," and the last three items are recognized as "failure mechanism" characterizations. The following definitions of these items more clearly identify their intended usage:

- Detector. The inspection or test which detected failure. The scope of the inspection or test includes user returns and field failures, qualification tests, acceptance tests, pre-cap visual, etc.
- Indicator. The parameter that is out of limit, or failure of the part to meet any other specified requirement.
- Physical cause of failure. A description of those abnormal physical conditions and/or characteristics of the device which analysis has disclosed as the reason(s) for failure to meet specified requirement(s). Examples are open ball bond, shorted metallization, sagging lead wires, etc.
- Design, process, or application cause of failure. That which must be corrected to prevent future failures of the same kind. It can be elements of workmanship, material, process design, process control, device design, user application, etc.

NOTE

It is necessary to distinguish between the physical cause of failure and its antecedent cause in design, process, or application. Cause of failure is "that which must be corrected," while the physical cause is identified by the information disclosed in analysis. For example, contamination on the bar may have caused excessive current leakage; however, contamination was not the antecedent cause, but rather an inadequate wash cycle.

- Generator. The material, operation, inspection, or test which generated the failure. Included in this meaning are test, application, operation, and field use. An inspection or test is a generator only if the part was damaged during that inspection or test, or if the part is an escape from that inspection or test.
- Part or area affected. This may be metallization, lead wire assembly, weld seam, oxide, bulk material, diffusion, etc. The correct descriptive terminology locates the anomaly and establishes it as a "defect." Defects always have "failure mode" and "failure mechanism" histories.

The aforementioned definitions are particularly essential to the definition of the word "defect" and to its application. A resistor whose cross sectional area has been reduced during masking and diffusion has no history related to open circuitry. It would serve no purpose to call it "defective" on the basis of conjecture.

SECTION II

DEFECTS INTRODUCED BY MONOLITHIC MICROCIRCUIT PROCESSING

A. GENERAL

Many process operations are performed sequentially during the manufacture of monolithic microcircuits. These operations are subdivisions of six major process areas that are critical to the manufacture of microcircuits. These critical process categories are as follows:

- Mask and etch
- Diffusion
- Metal evaporation
- Scribe and break
- Mount and bond
- Packaging

This section briefly discusses the operations within each major process category which can be improperly or imperfectly performed to cause a defect(s) in monolithic microcircuits.

B. MASK AND ETCH AND RELATED DEFECTS

The mask and etch category provides the technique by which diffusions and metallizations are applied to a silicon slice to produce a microcircuit chip. The process uses a pattern mask to expose an etch resist material in some particular geometric pattern so that silicon dioxide or thin-film metallization may be preferentially etched from the silicon slice. The process variables can be evaluated as subcategories of mask, etch resist, and etch.

1. Mask Defects.

There are four major defect areas associated with the photolithographic mask. These defect areas are:

- Light areas in dark regions.
- Dark areas in transparent regions.
- Poor mask definition.
- Improper pattern dimensions.

The causes for these defect areas are factors of material, handling, cleanliness, equipment, and operator error. Regardless of the cause for the mask defects, only two process defects can result from them. These process defects are:

- Oxide or metal will be removed from areas where oxide or metal is required, or,
- Oxide or metal will be left in areas where oxide or metal is not wanted.

These two process defects can cause many different monolithic-microcircuit defects to exist. Some examples are:

- Open metallization,
- Shorted metallization,
- Shorted or degraded junctions,
- Regions of high or low resistivity,
- Poor oxide integrity, and,
- Poor ohmic contact between silicon and metal.

2. Etch Resist Material Defects.

The etch resist operation includes the application alignment, exposure, selective removal, and final removal of the etch resist material. The defect areas which can occur from incorrect or imperfect operations are:

- Impure photoresist material.
- Improper application of photoresist material.
- Poor adhesion of photoresist material.
- Improper mask alignment.
- Improper exposure of photoresist material.
- Improper development of photoresist material.
- Improper removal of photoresist material.
- Improper handling of slices during the photoresist operation.

The causes for these defect areas are factors of material, handling, cleanliness, equipment, and operator error. Only three process defects can result from the photoresist area:

- Oxide or metal will be removed from areas where oxide or metal is required.
- Oxide or metal will remain in areas where oxide or metal is not wanted, or,
- Etch resist material will be left on the slice, which could cause current leakage paths.

The three preceding process defects can cause many different monolithic microcircuit defects to exist. Some examples are:

- Open metallization.
- Shorted metallization.
- Shorted or degraded junctions.
- Regions of high or low resistivity.
- Poor oxide integrity.
- Poor ohmic contact between silicon and metal.
- Parameter degradation from contaminated surfaces.

3. Etch Defects.

The etch operation consists of the application of a silicon or metal etch to the masked slice and the removal of the etch by washing the slice. Some defect areas in processing at the etch operation are:

- Improperly mixed etches.
- Improper etch time.
- Improper rinsing of etch.
- Improper handling of material during the process operation.

These defect areas are caused by factors of material, handling, cleanliness, equipment, and operator error. There are only three process defects which can result from the etch operation. These defects are:

- Oxide or metal will be removed from areas where metal or oxide is required,
- Oxide or metal will be left in area where oxide or metal is not wanted, or,
- Etch residues will not be removed sufficiently from the slice.

Some microcircuit defects which are attributable to the etch operation are:

- Open metallization.
- Shorted metallization.
- Shorted or degraded junctions.
- Regions of high or low resistivity.
- Poor oxide integrity.
- Poor ohmic contact of metal to silicon.
- Parameter degradation from contaminated surfaces.
- Chemical decomposition of materials from etch residues.

C. DIFFUSION AND RELATED DEFECTS

The diffusion process provides the technique by which components are constructed within the monolithic microcircuit chip. Defects associated with this process and resultant conditions are as follows:

- Flaws in the starting slice material can cause nonuniform diffusion depths. The diffusion depths can be so nonuniform that shorting of junctions or complete shorting of components can exist. Nonuniform junction depth can also cause parameter variations within a microcircuit, which results in improper circuit operation. Some examples of flaws in the starting material are: dislocations, stacking faults, crystal misorientation and regions of high dopant densities.
- Improper resistivity of starting material can cause the diffusion gradients to be wrong in each component. Improper diffusion gradient can cause the component's parameters to be out-of-tolerance with respect to circuit design limits and can result in marginal circuits or malfunctioning circuits.
- Improperly cleaned slices prior to diffusion can cause regions of spurious diffusion. The contaminant on an improperly cleaned slice can act as a mask, which impedes the diffusion rate in the area of contamination. Contaminants also impede the proper growth of oxide during a diffusion process, thereby causing poor oxide integrity to exist in the area of contamination.
- Improper deposition, diffusion, and deglaze rates result in improper diffusion depths and/or improper impurity densities. These improper depositions or dopant concentrations are the primary cause of electrical parameter failures such as gain, breakdown voltage, resistor values, etc.
- Improper handling during the diffusion cycle can cause bulk silicon damage in the form of excessive dislocation densities and excessive lattice stains. These types of defects result from thermal and mechanical shock, and they change the silicon's crystalline structure, particularly at elevated temperatures. All the aforementioned defect areas are the result of improperly controlled process variables such as material, equipment, cleanliness, handling, and operator error. The microcircuit defects which result are usually functions of the bulk component characteristics, and they affect the electrical properties of the circuit.

D. METAL EVAPORATION AND RELATED DEFECTS

Metallization is the technique by which the components of a monolithic microcircuit are interconnected to form the complete circuit. The process consists of the combined operations of metal evaporation, metallization, pattern mask, and pattern etch. Since the defects associated with masking and etching were discussed previously, only those defects associated with evaporation will be discussed here.

Defects can be introduced at the metal evaporation operation by any of the following mechanisms:

- Improper slice cleanliness
- Improper evaporation equipment
- Improper metal purity control
- Improperly controlled operational procedures

These mechanisms by which defects are introduced at the metal evaporation operation are functions of variables in material, equipment, cleanliness, handling and operator error.

Some microcircuit defects which are related to metal evaporation are:

- Insufficient thickness of metal to meet the circuit's current design capabilities.
- Poor ohmic contact to the silicon or silicon dioxide.
- Improper alloying of metals into silicon, which results in bulk material degradation.
- Contaminated metal films which might bond poorly at the die-to-package bond operation.

E. SCRIBE AND BREAK AND RELATED DEFECTS

The scribe and break operation performs the function of reducing the slice into individual microcircuit wafers or chips. The microcircuit defects which are introduced by the scribe and break operation are chips, fractures and cracks. The process variables which induce chips, fractures, or cracks are factors of material, handling, equipment, procedures and operator errors.

The scribe and break operation is considered critical primarily because of the significant contribution to the reliability failure rate made by chips, cracks, and fractures. The high incidence of these defects occurs because the silicon material is thin, brittle, and crystalline in composition. Any significant reduction in the reliability failure rate of monolithic microcircuits must include the reduction of cracks, chips, and fractures.

no scratches here

F. MOUNT AND BOND AND RELATED DEFECTS

The mount and bond operation provides the technique by which a microcircuit chip can be used in electronic equipment. The microcircuit chip is too fragile and small to be useful in electronic equipment. The chip must therefore be properly packaged to become a useful tool. The mount operation makes the microcircuit chip stationary in the package, and the bond operation connects the active component of the chip to the leads of the package.

1. Mount Defects.

Two methods of mounting are popular in present packaging techniques. One method uses an alloy technique with a metal (usually gold) to connect the chip to the package. The silicon wafer is in ohmic contact to its platform which may or may not be isolated from the package. The second technique uses a low-melting-point glass to connect the package to the header. The two techniques are commonly refered to as alloy mount and glass or ceramic mount.

The defects introduced into monolithic microcircuits by the mount operation are functions of material equipment, cleanliness, equipments, procedural controls, and operator error. Some examples of defects which can be caused by an improper mounting operation are:

- Die separation from header.
- Crack, strains, fractures.
- Scratched metallization.
- Improper lead wire routing.
- Improper package seal from mount contaminants on header weld flange.

2. Bond Defects.

The bond operation uses thermocompression bonding techniques to connect the chip to the package with a small wire. Some variations of thermocompression bonding techniques are ball or nailhead bonds, wedge bonds, stitch bonds, and ultrasonically scrubbed bonds.

The bonding technique is perhaps the most critical with respect to monolithic microcircuit failure rates in that it is often the weakest point in the effort to achieve true microcircuit performance capability.

The defects which are introduced by the bonding operation are functions of material, cleanliness, equipment, procedural controls and operator variables. Some examples of defects which are introduced into microcircuits by the bonding operator are:

- Broken wires.
- Scratched interconnects
- Chipped or fractured dice.
- Weak bonds.
- Undesirable intermetallics (commonly called plague).
- Sagging or shorted wires.
- Improper wire routing.
- Improperly placed bonds.

G. Package Seal and Related Defects.

The final operation in the manufacture of monolithic microcircuits is the sealing of the package. Many different packages, packaging materials and sealing methods are used.

The packaging operation or the sealing operation must satisfy only two requirements:

- The chip and the interconnects to the package must be protected from external environments.
- The usefulness of the microcircuit as an electronic tool must not be affected.

Any portion of the sealing operation which causes either of these two requirements to be affected is considered a defect-introducing operation. Some examples of defects which result from an improper sealing operation are:

- Inadequate weld seal.
- Inadequate glass seal.
- Particles sealed into the package, and
- Internal damage to die, interconnects, or header from the sealing operation.

SECTION III

DISCUSSION OF FAILURE MECHANISMS

A. GENERAL

A basic ingredient of any system reliability program is the ability to analyze a system monolithic microcircuit failure and determine the proper course of action. This action may vary from concluding that the device is not a failure (i.e., the cause of failure is due to improper system application) to concluding that legitimate microcircuit failures which require manufacturer corrective action have occurred.

Proper determination of cause of failure is paramount. For this reason, an entire volume of this Handbook is devoted to failure analysis. The proper direction of investigation one should pursue in failure analysis is not always obvious from the failure indication. Often times, a cursory analysis will actually uncover the cause of failure. However, too many times, what may appear to be a workmanship problem by cursory analysis, may actually be unrelated to the real cause of failure.

Consequently, the failure mechanisms discussed in this section can be viewed from two standpoints. First, the discussion can be used to understand all observed deficiencies with respect to manufacturing processes. Secondly, and most important, if the failure mechanism is the actual failure cause, the discussion can be a starting point for determination of proper corrective action.

B. PROBABILITY OF ESCAPE OF DEFECTIVE DEVICE FROM MANUFACTURER

One method of determining the importance of known failure mechanisms is to compare the probability of escape from the manufacturer of devices with and without postprocess screening techniques. Such an estimate would be pessimistic with respect to unscreened devices, since the implemented screens are always in excess of use condition requirements.

The probability of escape by percentage for each mechanism of failure discussed herein represents the total percentage of defective devices shipped by the manufacturer of monolithic microcircuits. These percentages are shown in Table 1. The escape rate includes those parts which will be rejected by the user's incoming inspection, board check out, system acceptance test in user's house and user's reliability failures.

It is interesting to note that the no-screen devices show a total escape rate that is just below the one percent acceptable quality level (AQL), which is a standard acceptance level for "off the shelf" parts. Extensive screening processes improve the acceptable quality level by approximately one order of magnitude, and they allow consistant acceptance of 0.1 percent AQL lots.

Table 1. Probability of Escape With and Without Post-Process Screening Techniques

Failure Mechanism	Probability of Escape*	
	No Screening (%)	With Screening (%)
KMER, photolithographic and diffusion defects	0.04	0.002
Oxide defects	0.17	0.030
Metallization defects	0.03	0.004
Mechanical defects in the die	0.09	0.000
Parasitics, isolation	0.00	0.020
Mounting of the die elements	0.01	0.002
Die-to-package connections	0.10	0.010
Package integrity	0.50	0.012
Total	0.94	0.080

*The probability of escape estimated here represents the combined total of defective devices shipped by the manufacturer. This escape rate includes those parts which will be rejected by the user's incoming inspection, board check out, system acceptance test in user's house, and user's reliability failures. The numbers included here are not intended to be guarantees, but they are intended to give guidance as to the relative magnitudes of the various failure mechanisms.

The breakdown of escapes by percentage, which constitutes the reliability failure rate, is shown in Table 2. This breakdown represents the most recent information available from life test programs performed by the manufacturers and users of monolithic microcircuits.

Table 2. Contribution to Reliability Failure Rate by Failure Mechanism*

Failure Mechanism	Contribution (%)
KMER, photolithographic and diffusion defects	4.6
Oxide defects	16.0
Metallization defects	10.5
Mechanical defects in the die	8.6
Mounting of the die elements	10.5
Die-to-package connections	21.3
Package integrity	14.9
Marginal	5.5
Undetermined	8.1
	100.0

*These percentages represent the composite total of failures from operating and storage life tests which determined the reliability failure rate for all monolithic microcircuits.

C. IMPACT OF PROCESS DEFECTS ON FAILURE OCCURRENCE

1. General

A discussion of known failure mechanisms is presented here. These failure mechanisms have been observed in finished devices, in environmental screens, and in application. The discussion of the various failure mechanisms contains estimates based on both fact and opinion of the probability of failure occurrence.

2. Photolithographic and Diffusion Defects

The category of photolithographic and diffusion defects includes faulty alignment between one or more of the successive mask locations, and defects in the photolithographic mask itself. The mask defect may be one of definition, intensity or flaws which result in dark spots in the clear areas of the mask, as well as clear spots in an area which by design should not transmit light. These defects result in improper photoresist exposure in the area of the mask defect which, after development, will result in improper oxide removal or improper diffusion.

A significant number of defects of this type should not be encountered by the user. This failure mechanism, when observed, is clearly an escape from electrical testing. This defect is observable in the silicon slice form and the silicon slice electrical probe test as well as final electrical tests.

Failures attributed to diffusion, photoresist or photolithographic mask defects have been observed after a burn-in screen. The magnitude of incidence of burn-in failures attributed to this failure mode is less than 0.04 percent. This value is known to be pessimistic, since the finest failure mode breakdown of burn-in failures includes this mode in "other" die defects. These defects are those remaining after the bulk of the failures in the more general category of die defects have been individually itemized. This figure is the best estimate of the incidence a user of nonburn-in devices should expect to see. Devices which have survived burn-in and the associated redundant testing will have a lesser probability of escape — estimated to be less than 0.002 percent.

3. Oxide Defects

The oxide-defects mechanism pertains to defects in the surface passivation oxide layer that provides the dielectric between the die's surface and the evaporated lead pattern. Gross defects in, or removal of, this dielectric prior to lead application result in nonfunctional "shorted" devices with a probability of escape (from screening) to the customer so remote that discussion here is not warranted. This, however, is not the case for the "pinhole." Pinhole is the name commonly applied to small localized areas in the oxide layer with low dielectric strength. The more obvious causes for this defect include the presence of dust particles, minute photolithographic mask flaws and contamination. It is generally agreed that complete correction of these and other apparent pinhole sources will not resolve the total pinhole problem.

Complete understanding of the oxide-defect failure mode can occur only after successful completion of fundamental research on silicon surface passivation. At the present state of the art, the oxide layer is not completely uniform. It contains areas of greater and lesser dielectric strength. When an area of low dielectric strength occurs under the lead pattern a device will be produced that is shorted, has high leakage, or has reduced resistance to electrical overstress.

The location of the pinhole on a bar is random in nature. The sites which occur in inactive areas and not under the lead pattern are of no consequence. They cannot contribute to device failure.

Reduction in the incidence of this failure mode has been accomplished by the use of two coats and two exposures of the photoresist, using two different masks. This process minimizes pinholes resulting from mask flaws, because probability of alignment of minute flaws on two different masks is remote. Further impact on pinholes may be gained by the application of supplemental additional oxide or other oxide layers over the thermally grown oxide. These efforts fall into the category of "corrective action" by covering the inherent defect in the dielectric. This failure mechanism can also be reduced by overvoltage screens.

Significant quantities of products with double coat, double exposure and addition of supplemental oxides, have been processed through burn-in screen. The

incidence of burn-in failures attributed to oxide defects is 0.17 percent. Devices with the double coat, double expose process but without the addition of a final supplementary oxide, that have been processed through burn-in, show a 0.32 percent incidence of failure due to oxide defects. The majority of the defect sites were located where the maximum voltage on the die was available across the site. It is apparent that when a voltage is applied to a device that is in excess of any voltage the device has previously seen, breakdown of the dielectric can occur, since breakdown will occur when the applied voltage is in excess of the dielectric strength of the weakest point in the oxide layer. The overvoltage application can be either sustained or transient in nature. When the applied voltage is sustained and the current source is sufficiently high, localized heating will occur in the area of the breakdown. In this instance evidence of overheating, lead melting, and discoloration will be observable on the die. Such a failure should be attributed to electrical overstress rather than an oxide defect. If the electrical overstress is of short duration and transient in nature or the current source is limited, evidence of overstress on the bar will not be observable. This will be particularly true if the lead metallization system is not the weakest link in the circuit chain.

It is believed that many of the failures attributed to oxide defects are in fact a result of system transients. This however does not relieve the vendor of his responsibility for supplying parts with reasonable tolerance to overstress. The pinhole failure is one of the more severe problems encountered in system level failures. Probability of escape of devices with insipient oxide defects is estimated to be 0.03 percent for 100-percent burned-in devices.

4. Metallization Defects

Metallization defects include surface flaws, faulty evaporation, chemical reaction, gold migration from excess heat, scratches and smeared lead patterns (where opens or shorts result), insufficient lead thickness, and insufficient lead clearance. Comments in the introduction to this section concerning determination of the real problem are particularly pertinent to this mechanism. With sufficient magnification, minor discrepancies will be observable in the lead pattern of most devices. These "cosmetics" should not be confused with actual cause of failure. Overdesign of the lead pattern is usually such that less than 10 percent of the design lead width is sufficient to carry rated current for the device. This fact not withstanding, a common criteria for visual acceptance of the bar prior to sealing requires half of the lead width to be continuous. A scratch or flaw which exposes the underlying oxide for over 50 percent of the lead width is considered defective. Smears in the metallization which do not short to the adjacent lead are considered acceptable at visual inspection except on high reliability programs. Criteria for acceptance on these programs usually require isolation of adjacent leads to be at least 50 percent of the design width of the clearance between leads.

Significant metallization defects which result in device failure should not be encountered by the user. Such a failure would be an escape from both pre-cap visual inspection and final electrical test. Comments contained in the previous section with respect to tolerance to overstress of oxide defects are also applicable to lead metallization. If the cross section of a lead pattern is materially reduced, this location will be weakened with respect to current carrying capacity. When an overstress is applied to this lead, this weakest point will be the first to open. Melting will

usually occur, and evidence of lead damage prior to overstress will remain. The melting in such a case is not necessary, but if present it is usually evidence of overstress.

Device failures from burn-in that are attributable to metallization defects have been observed. All metallization defects combined account for 0.03 percent loss at burn-in. This is a reasonable estimate of the incidence a user of nonburn-in devices should expect to encounter. Devices which have survived burn-in and the associated redundant testing will contain significantly lower metallization escapes, estimated to be less than 0.004 percent.

3/10,000

4/100,000

5. Mechanical Defects in the Die

The failure mechanism of mechanical defects in the die includes bulk defects in the silicon, and cracks, chips and fractures in the die. This failure mechanism is considered to be a significant infant failure problem. Cracks are intentionally induced in the silicon slice scribing operation of the die separation process. Every force, bending moment, or torque applied to the die from that point forward could result in a cracked die failure.

The manufacturer quickly learns to avoid bending or torqueing the brittle silicon. In the hands of an uninitiated user this may not be the case. The finished flat pack device looks and feels like a solid block to which relatively fragile leads are attached. This is deceiving. The silicon die is rigidly attached to the base plate of the header. Every torque or bending moment applied to the case will be transmitted to the die. Sufficient force on the case to crack the die or propogate an existing crack may occur at device testing and board mount. In the event that the board is assembled such that the device body is rigidly attached to a printed circuit board, bending moments applied to the board will be transmitted to the silicon. Cracks will be encountered at board removal and at device decanning during the analysis of the failure. Proper device handling cannot be too highly emphasized as a deterrant to die cracks.

Items under control by the manufacturer which will impact cracked dice include a mounting method that insures bar support under the bonding pads without excessive build up of mount material around the edge of the bar. In the event the die is cantilevered and a bonding pad is on the unsupported area, the die is more susceptible to cracks induced by the bonding operation. Introduction of stronger packages is expected to significantly reduce the occurrence of die cracks.

Attempts to induce cracks with environmental stresses of thermal and mechanical shock, vibration, acceleration, temperature cycling and nondestructive electrical pulses have been relatively unsuccessful. Cracks associated with electrical overstress have been observed. The incidence of cracks has been observed to be greater on devices which contain excess mounting material such that the edges and corners of the die are below the surface of the mounting materials.

The incidence of cracked die failures from burn-in screen is 0.09 percent. This is a reasonable estimate of the incidence a user of nonburn-in devices should expect to see; however, the percentage could be larger or smaller, depending on the particular packaging technique that is used. This mode is second only to pin holes in severity at board test and system level failures. The estimated rate of incidence the user of devices which have survived environmental screens should expect to see is 0.02 percent.

6. Isolation of Parasitics

The presence or absence of undesirable and destructive parasitics is a function of device design. All monolithic microcircuits (especially junction-isolated) will contain parasitics by virtue of the fact that multiple elements are built on the same silicon die.

Most parasitics are undesirable; device performance can be degraded by their presence. Destructive parasitics are normally observed in application, when supply voltages are applied to a device in a sequence which the device has not previously seen. Normally, device testing is accomplished by simultaneous application of all supply voltages. Requirements for power supply sequencing have been imposed on some devices that were susceptible to destructive parasitics. These tests are composed of sequential applications of all conceivable combinations of supply voltages to which the device could be subjected in its application. Devices capable of surviving such a test may be assumed to be free from damaging parasitics as long as these devices are not subjected to overstress conditions. It is always possible to damage devices by subjecting them to electrical stresses that are beyond their rated limits. Parasitics are known to have been induced by overstress conditions.

Care is required in properly identifying the parasitics which cause a failure. Visual evidence of damage on the die surface of a device that has failed due to parasitic transistor action can be identical to the damage observed on a device destroyed by electrical overstress. When a particular pattern of lead melting is observed to be repetitious, both a search for overstress conditions and an analysis for parasitics should be initiated. The ability to reproduce the particular pattern of melting by use of rated supply voltage greatly facilitates the identification of the damaging parasitic.

The "state of the art" for monolithic microcircuits is continually being improved in order to reduce the effects of parasitics. The more recent designs are relatively free of undesirable parasitics. The newer concept of dielectric isolation is a good example of improved technology. Monolithic microcricuits manufactured by the dielectric isolation method are particularly impervious to parasitics, since they replace one parasitic diode with an oxide interface.

Unlike failure mechanisms previously described, the mechanism of failure due to parasitics is device-type oriented. Failure incidence is a function of system requirements that are designed into the device. The presence of parasitic failures in a system should be considered a major problem, because it implies that there is design incompatibility between the monolithic microcircuit and the system. In most cases, a design modification is required in one or the other. One should not expect parasitics to present a reliability problem when design compatibility exists. When such compatibility does not exist, it will be revealed in system test, if not before. Gross estimates of the anticipated incidence a user should expect to see in this case are meaningless.

7. Mounting of Monolithic Elements

Two mounting methods for monolithic elements are widely used. One is a frit mount that uses a low-melting-temperature glass. The other method uses a gold alloy mount. Either method of mounting may include a ceramic substrate for

case isolation. Mounting requirements include proper placement in the header cavity, orientation, clearance, support and integrity to withstand environmental stress. Improper placement can result in a die short to the internal header lead or cause undesirable bond wire dress.

The incidence of mount failures from burn-in screen is less than 0.01 percent. Failures with this mode are escapes from both postmount and pre-cap visual inspections as well as environmental screens of vibration, centrifuge and temperature cycling. This failure should not be expected to be a major system level problem. Probability of escape from these screens is estimated to be 0.002 percent.

8. Die-to-Package Connections

Connection between the die's evaporated bonding pad and the package lead is usually accomplished by means of a gold bonding wire and a thermocompression ball bond to the bonding pad, and a stitch, smear, or wedge bond to the internal header lead. Failure modes associated with this assembly process include open circuits resulting from broken wires, separation of the bond from the lead as a result of improper bond placement, improper bonding (temperature or pressure) chemical reaction and intermetallic degradation. Short circuits are observed to be a result of improper lead wire routing, sagging wires shorting to the die edge, evaporated lead, or the package. The reliability of this total process is extremely dependent upon the bonding operator. Failure incidence is affected by bonding-operator training and controls as well as by design revisions to simplify the bonding operation. Reduction of failures resulting from improper bond placement have been accomplished by redesign of bonding pads to increase the pad area and thus increase tolerance of bond location on the pad.

The impact of failures resulting from improper wire dress has been reduced by the introduction of new package designs. One such flat pack package allows the die's surface to be at a lower level than the internal header leads, making shorter and tighter wires possible, with a reduced probability of improper wire dress.

Screening procedures which use acceleration, vibration, isolation, and threshold tests are effective in further reducing the incidence of these failure mechanisms. Failure attributed to die-to-package connections are observed in burn-in failures at a rate of 0.22 percent. This figure is pessimistic in that it does not account for the most recent improvements. Failures attributed to sagging wires shorting to the die's edge account for 0.14 percent of the burn-in failures and are included in the previous figure. A significant reduction in this failure mode was accomplished with the introduction of an improved header, as previously described.

The best estimate of the incidence a user of nonburn-in devices should expect to see is in the range of 0.10 to 0.15 percent. The majority of devices subjected to these failure mechanisms are screened at pre-cap visual inspection and should be considered escapes from this inspection. Experiments have been conducted to determine the efficiency of pre-cap visual inspection. Review of possible improvements to increase this inspection efficiency are now under consideration. It is generally agreed, however, that a significant effect on these failure mechanisms will result from process improvement rather than inspection improvement.

The action a consumer should take in the event excessive failures attributed to faulty die-to-package connections are encountered, include:

- Review environmental screening tests for possible improvements or additions to afford a greater probability of defect removal.
- Review the qualification, training and certification the manufacturer requires for the bonding operator or operation.
- Review device design to insure incorporation of "state of the art" design for materials, package, and process.

9. Package Integrity

Package integrity failures consist of nonhermetic seals, terminal fatigue, external surface contamination, marking and plating deterioration. Hermeticity is considered to be the most significant package integrity indicator. Approximately 0.5 percent of hermiticity-screened devices have leak rates that are in excess of 5×10^{-7} std. atm. cc/s. The hermeticity screens performed on these devices included environmental screens of acceleration, vibration, temperature cycling, and burn-in, in addition to all postseal process handling and testing.

Experiments have been conducted to evaluate the probability of escape from an hermeticity screen. Of more than 16,000 devices that were subjected to redundant mass spectrometer helium leak tests, 0.012 percent were disclosed as failures on the second 100 percent test. This is considered to be within hermeticity test equipment capability with respect to repeatibility.

SECTION IV

SCREENING PROCEDURES

A. GENERAL

The purpose of screening is to select those devices which have the required characteristics for an intended application. In a production run of monolithic microcircuits there will be a range or distribution of values for each characteristic of the device. The desired characteristic may be a quality of workmanship, physical dimension or electrical property. Screening processes are used to select the microcircuits for which the desired characteristic meets specific requirements. Frequently this screen is merely the reading of an electrical parameter or the measurement of a physical dimension. However, the screening process may include environmental or electrical stressing that is designed to cause failure of those devices that cannot withstand a necessary stress. Again, this is a process of selection. Any processing, testing, or inspecting which selects devices with desired characteristics is a screening operation.

The term "screen" is a broad term which must be defined for each application of the device involved. Commonly, the term "screening" is used to identify the additional inspection, processing, and testing that are necessary to select microcircuits for special requirements that are more stringent than those specified in the manufacturer's data sheet, or to eliminate microcircuits that are potential early failures.

"Early" failures are those which occur during the first hours of operation. The failure rate decreases rapidly as the weak devices fail and are removed.

Some early failures are eliminated by mechanical stresses such as shock, vibration, centrifuge, and temperature cycling. Other early failures are eliminated by operating burn-in, where the devices are operated at higher loads and temperatures than those to be encountered in service. The exact loads and temperatures must be set high enough to remove those incipient failures which would occur under normal loads and temperatures. Conditions which produce a continually increasing failure rate should be examined as a possible indication of too severe a screen.

When determining the types of screening needed, it is advisable to obtain information on the particular part in question in order to compare its normal capabilities to the specific requirements of the intended application. It may be that recent corrective actions have eliminated or drastically reduced the frequency of a particular condition of failure that occurred in the past. It is also possible that new device designs may require new screening techniques for some previously unobserved failure mechanism.

Screens that require inspection to closer tolerances, or testing that is performed to more restrictive limits or electrical parameters have no physical affect on the microcircuits that are thus processed. Other screens which subject parts to

environmental or electrical stress, are intended to damage or degrade borderline microcircuits, thereby causing them to be rejected by later inspections or tests. It is vitally important that later inspections or tests have the capability of detecting the damage or degradation caused by additional stress, or the purpose of stressing will have been defeated.

Screening techniques can be divided into three general categories: visual, electrical, and environmental processing.

B. VISUAL SCREENING

All manufacturers of monolithic microcircuits perform visual screens in their production processing. Visual screens are performed by production-line operators, who accept or reject their own work on criteria of quality and workmanship. Additionally, visual inspection stations are strategically placed throughout the manufacturing process. The rejection criteria for each visual screening operation must be defined as exactly as possible. The inspector must know exactly which characteristics are undesirable. Rejection criteria that are not defined adequately can result in either of two extremes:

- The inspector, not knowing what to reject, will reject everything that is doubtful. This inspection will cause rejection of many good parts, and production costs will soar.

- The inspector, not knowing what to reject, will pass doubtful devices which could cause inherent reliability problems in use.

It is extremely important that the rejection criteria for visual screening be based on sound practical reasoning. Reject analysis and failure analysis must be relied upon to provide the foundation for rejection criteria. Arbitrary decisions to reject or accept are catastrophic. The temptation is too great to reject those devices which "do not look just right" but which cannot be correlated to mechanisms of failure.

Visual screens are very effective for removing some failure mechanisms and relatively ineffective for removal of other mechanisms. An example of the visual screen effectivity lies in the area of bond strength. Improper bond placement causes weak bonds because of the reduced alloy area beneath the misplaced bond. This mechanism of failure lends itself well to visual screening techniques. Bonds may also be weakened by the use of improper temperature. Improper bond temperatures usually leave no visual evidence of a weakened bond; therefore, visual screens are ineffective against them. From the aforementioned example, it may be readily seen that visual screens can have an important impact upon certain defect areas but cannot be expected to be completely effective in removing all defectives from a defect group.

Visual screens include the use of microscopes with magnifying power of sufficient proportion to properly evaluate the area to be inspected. Experience has shown that diffusion, oxide removal, and masking operations require magnification powers of 100X to 400X. Metallization and die inspections are satisfactorily performed at 70X to 120X, while mount and header inspections require only 7X to 40X magnification factors. Direct collimated light sources are required for die and metallization inspection. Header inspections are more satisfactorily performed with incident or oblique light sources.

Radiographic examination is also performed as a visual inspection. A complete microcircuit may be photographed with the aid of X-ray equipment, and the negatives may be examined for presence of extraneous matter, improper mount, pigtails, etc.

Manufacturers of monolithic microcircuits have visual inspection criteria which are applicable to each particular process or design. The buyer of microcircuits should communicate his requirements to the manufacturer. If visual screens are desired which are not a part of the manufacturer's normal processing, both parties should discuss the various aspects of the proposed additional screening. The discussion should enable the buyer to determine whether the additional screening cost is warranted in terms of reliability performance.

C. ELECTRICAL SCREENING

Electrical screens are performed at various intervals in the manufacturing processing of monolithic microcircuits. Some of the screens merely determine that the particular manufacturing process has been satisfactorily performed. An example of this is the resistivity measurement of slices, to determine that the proper starting material has been used. Electrical screens of this type are used more to control processes than to separate good devices from bad.

The multiprobe (silicon slice electrical probe) and final test electrical screens are designed to select microcircuits for further processing to ensure that the devices meet specified electrical requirements. Special electrical tests (called parameters) guarantee the functional capabilities of those microcircuits that meet the test requirements. The loading requirements that are imposed upon the microcircuits during these tests insure that each of the microcircuits can drive or can be driven by the proper number of other microcircuits. Also, at the final acceptance screen test the microcircuits are tested at different temperatures to insure that the devices will operate successfully in a specified temperature operating range.

The aforementioned tests guarantee that the microcircuit(s) in question meets a specific electrical requirement when shipped to the user.

Other electrical screens are designed to ensure that a microcircuit will operate in a given configuration over extended periods of time. One of the most widely used screens of this type is the burn-in screen. During burn-in, the microcircuit is normally biased in a use-condition configuration at maximum voltage levels. The maximum guaranteed temperature condition is imposed upon each microcircuit. Data that has been accumulated on burned-in microcircuits has revealed that elevated temperatures provide a means by which failure occurrence can be accelerated. The acceleration factors can be used to predict with good accuracy the expected failure rate for any given period of operating time at a given temperature. Burn-in data has also revealed that the reliability failure rate for microcircuits improves with operating time. This means that the failure rate for any given group of microcircuits will be improved by burn-in screen, and it attests to the effectivness of burn-in as a suitable screen for removing potential failures. Additional discussion of burn-in screens is contained in Volume 4 of this Handbook.

The monitored vibration test is another additional electrical screen that may be used to remove mechanically weak or potentially intermittent devices. The device is

operated for a period of time and simultaneously subjected to a mechanical vibration. However, losses on monitored vibrations are typically below 0.2 percent; this indicates that it is a relatively inefficient screening method.

Electrical screens also have the capability of detecting degradation of a microcircuit's capabilities. Often, variables data are obtained prior to and after an electrical or environmental screen. Thus, microcircuits that exhibit excessive drift or degradation may be screened from the stable microcircuits. Actual data that have been generated on many devices in a major military program indicate that this addition of variable data is a refinement that does not improve the burn-in efficiency considerably. The reason is that (as opposed to discrete failure history) only a small percent of the failures have pre-indicators of device parameter degradation. The vast majority fail without previous degradation indication. Consequently, before arbitrarily using this refinement, system requirements should be considered.

D. ENVIRONMENTAL SCREENING

1. General

A large number of environmental screens that are similar to many of the screens described in MIL-STD-750 have been sufficiently evaluated as screening tools to determine their effectivity. Most environmental screens are used to determine whether a microcircuit has the mechanical strength to withstand the environmental conditions of expected usage. All too often the buyer of monolithic microcircuits will "overbuy" with respect to environmental screens. For example, if the buyer expects to use his microcircuits in a large fixed computer which is housed in a controlled environment, why should he buy processing that includes 20,000 g levels of constant acceleration, and extreme temperature cycling? Conversely, some users of monolithic microcircuits have extreme environmental requirements, and therefore, need the added guarantee of the environmental screen techniques; however, they do not buy these screens.

Some environmental screens that have proven merit are discussed briefly hereafter.

2. Temperature Cycling

The specifications that control temperature cycling are many and varied. Generally, the purpose of temperature cycling is to determine that a device can withstand drastic temperature changes over an extended period of time without failure or degradation. The temperature cycle screen is effective in determining that thermal mismatch between materials is not sufficiently great to cause problems. Temperature cycling also has been effective for determining metallization faults. A typical temperature cycling screen will commonly specify 10 to 15 cycles from -55° C to +125° C, with thirty minutes of dwell time at each extreme. The ambient condition is generally air-to-air.

3. Thermal Shock

The thermal shock screen is merely an accelerated version of temperature cycling. Again, the purpose is to insure that drastic temperature changes will not affect microcircuit operation over an extended period of time. A typical thermal shock

will require 5 to 10 cycles from 0°C to +100°C, with 5 minutes of dwell at each temperature extreme. The heat exchange environment is usually liquid-to-liquid to insure extremely fast temperature excursions.

4. Mechanical Shock

The mechanical shock screen is designed to insure that a microcircuit is not sensitive to extreme mechanical violence. It is effective in determining that weak mechanical bonds to die and package do not exist. A typical mechanical shock will specify 1500 gravity forces to 6,000 gravity forces at 5 to 10 repetitions in each of the 3 mechanical planes. The kinetic energy dispelled in the drop test, and the time duration of the shock value determine the gravity force level. Although a strong argument can be made for electrically monitoring the device's operation for evidence of noise or intermittency, fixturing problems and very high cost usually preclude this possibility.

5. Constant Acceleration

The constant acceleration screen is sometimes called centrifuge screening. The purpose of this screen is to insure that the mechanical integrity of the microcircuit is sufficient to withstand extremely-high-gravity force levels. Constant acceleration levels of 10,000 gravity forces to 100,000 gravity forces are used to assure the buyer that he will receive quality devices.

To apply this screen, the devices are placed into a centrifuge machine and accelerated to the proper gravity level, which is determined by the radius of the centrifuge wheel and the acceleration factor. All three mechanical planes are usually investigated in reliability tests but are limited to a single plane in screen tests—the plane which tends to pull the bond away from the die. Three common mechanisms of failure uncovered by the constant acceleration screen are:

- Poor mechanical bond of die to package.
- Poor mechanical bond of lead wire to die or package.
- Excessively long lead wires that could short together, to the die, or to the package.

6. Vibration Variable Frequency

The vibration variable frequency screen is used to determine that the microcircuit is not sensitive to any reasonable frequency of vibration. The theory is to determine that the microcircuit is free to resonant frequencies that might cause degradation or failure—such as cracks in the die, or shattering of the mounting material, etc. Typical vibration variable frequency screens use 2 to 20 gravity forces with frequencies of 20 to 2,000 cycles per second; this is roughly the limitation of available equipment. The small size of microcircuits usually dictates that mechanical resonances will occur at higher frequencies. Therefore, this screen is of limited value.

7. Vibration Fatigue

The vibration fatigue screen is used to insure that the microcircuit is capable of withstanding extended periods of vibration without damaging effects. A

typical vibration fatigue screen consists of 2 to 10 gravity force levels at 60 cycles per second for approximately 100 hours. A microcircuit that has successfully passed this screen is considered to be free of vibration sensitive mechanisms of failure. The length of time required and difficulties in preparing and maintaining the equipment during the test make this extremely cost prohibitive as a 100 percent screen.

8. Destructive Screens

In addition to the previously mentioned environmental screens, other tests that have been developed destroy the microcircuit as a useful part. These destructive tests cannot be used in 100 percent processing of monolithic microcircuits. Statistical sampling of lots or groups of microcircuits can give a high degree of confidence that the lots or groups of microcircuits are capable of withstanding these environments. Some destructive tests that are conducted on a sample basis are included in the following list:

- Moisture resistance
- Solderability
- Lead fatigue
- Salt atmosphere
- Impressed voltage at elevated temperature and high humidity.

9. Storage or Shelf Life Screen

The storage or shelf life screen may be designed to be a nondestructive test. It is generally agreed that 1,000 hours of storage life at design temperature is not detrimental to a microcircuit's designed capabilities. It is also generally agreed that 1,000 hours of storage life at 350° C decreases significantly a microcircuit's expected life. The specific requirement of shelf life must be the determining factor of whether shelf life (storage life) is considered a destructive test. The storage life test is commonly used as a tool to determine the microcircuit's reliability failure rate, due to the fact that extensive studies have revealed that increased temperature causes accelerated life failures.

The user of monolithic microcircuits must carefully examine his intended usage to determine if the added cost of environmental screening is warranted.

SECTION V

CORRECTIVE ACTION

A. GENERAL

A process change that is implemented to reduce the occurrence of a failure mechanism is known as a corrective action. A corrective action may be as simple as to change the etch time required for metallization removal, or it may be so complex as to entail the complete redesign of the circuit. The specific corrective action required is determined by the mechanism of failure to be corrected.

That corrective action is required necessarily means that a problem has been observed that is not desirable. The need for corrective action is usually realized only after a sufficient quantity of failures have occurred to create a concern, and analysis of the failures has identified a common mechanism of failure. The fact that a common mechanism of failure has occurred is not enough to allow corrective action to be implemented. The mechanism of failure must be thoroughly understood so that the corrective action can be based upon sound engineering principles.

Once the mechanism of failure is understood and an engineered approach to corrective action has been resolved, the corrective action must be evaluated for effectiveness of its intended purpose. Even more important, it must be established that the corrective action does not introduce a new mechanism of failure that may be even more serious than the existant problem.

The corrective action may be considered adequate when it has met the following criteria:

- The mechanism of failure that made necessary the corrective action has been significantly reduced or eliminated.
- The corrective action has not introduced new mechanisms of failure that will create a significant problem in the future.
- The corrective action was properly engineered to include the best available state-of-the-art technology.

When microcircuits are continuously procurred during a program, experience gained at the beginning of the program results in corrective action. An increasing improvement in reliability can be expected as the later microcircuits are delivered. This procedure can often be the basis of the ultimate success of a reliability program.

B. UTILIZATION OF FAILURE ANALYSIS RESULTS

The purpose of failure analysis is to obtain results that can be used to reduce or to eliminate device failures. The absence of failures in any microcircuit application is a much dreamed of but seldom realized occurrence. As the state of the art in

semiconductor technology has progressed, the reliability failure rate of monolithic microcircuits has been reduced drastically. It has become increasingly difficult to prove how good microcircuits really are. Hundreds of millions of operating hours must be accomplished to prove the reliability failure rate. By the time the failure rate has been proved, the information has been obsoleted by technological advancements.

A concept of corrective action has evolved from the theory that a reduction in the occurrence of failure mechanisms will reduce the failure rate, regardless of its absolute value. This concept of corrective action is entirely dependent upon the ability to determine mechanisms of failure, and it has resulted in the advent of sophisticated failure analysis laboratories throughout the industry. The purpose of these laboratories is to analyze failures, identify the mechanism of failures, and to understand the physics of failure which induce these mechanisms. A corrective action cycle consists of the following steps:

- Generate failures that are related to use condition.
- Analyze the generated failures.
- Study the results of analysis.
- Implement corrective action.
- Determine results of corrective action from analysis of failures generated.

It appears that few users or manufacturers of monolithic microcircuits have difficulty generating failures. The ability to analyze the failures generated has been more difficult to accomplish. However, great strides have been made in this area of endeavor, with improved equipment and sophisticated analysis techniques. The first breakdown in the corrective action cycle occurs when the information gained from failure analysis is not used properly. For this reason, each failure analysis activity must have a group of people whose sole responsibility is to complete the link in the cycle between analysis and corrective action implementation. This group must perform a liaison function between the failure analysis laboratory and the individuals responsible for application of the corrective action.

In summary, it serves no useful purpose to perform failure analyses and to understand mechanisms of failure unless the information is used to improve product quality. Therefore, it is of prime importance that a program be instituted in conjunction with each failure analysis activity, that will enable the organization to fully use the failure results thus obtained.

C. RETRIEVAL OF FAILURE INFORMATION

The retrieval of failure information is much more widely accepted and practiced by manufacturers than by users of microcircuits. Most manufacturers of monolithic microcircuits have realized the importance of failure analysis and corrective action. These manufacturers have implemented corrective action cycles into their processes. Some of these manufacturers have also instituted sophisticated information retrieval programs that use data processing programs to determine significant problem areas. Problems observed "in house" have been quickly and satisfactorily solved.

The source of failure and reliability information that has remained relatively unexplored is the user. Users of monolithic microcircuits have untold quantities of performance data and failure information that could benefit both the user and manufacturer of microcircuits. This is especially true because the rapid technological advancements that are occurring in solid state circuits preclude a proper evaluation of parts prior to their use. The users of microcircuits cannot wait one or two years for parts to be evaluated and proven. Because of this, parts must be proven in the field where they are used.

The routing of failure and reliability information from the user to the manufacturer of microcircuits on a prompt and continuing basis could decrease the time required to reach a failure goal, by months or even years. Information retrieval and transfer between users and manufacturers should be an integral part of every purchase contract for large quantities of monolithic microcircuits.

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