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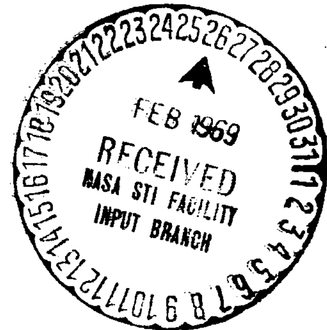
Final Report

DEVELOPMENT OF A MICROELECTRONIC MODULE



By H. Strack, F. Doerbeck, E. Harp,
and E. Mehal

November 1968

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Prepared under Contract No. NAS 12-537 by

TEXAS INSTRUMENTS INCORPORATED
Components Group
Dallas, Texas

for

Electronics Research Center
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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FOREWORD

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SECTION I

INTRODUCTION

The upper temperature at which transistors can be operated depends on the bandgap of the semiconductor material. Based on an operating temperature of 100°C for germanium, silicon transistors can be predicted to operate up to a temperature of 250°C, gallium arsenide transistors up to 450°C, and gallium phosphide or silicon carbide transistors at 1000°C and higher. No technology is presently available to fabricate gallium phosphide or silicon carbide transistors. Common silicon transistors are specified for a temperature range of about -60°C to 180°C case temperature and 200°C junction temperature. Gallium arsenide transistors have been operated at the theoretical limit of 450°C; however, the studies in this report show that the performance and stability of devices at this temperature are generally poor. Because of the much lower thermal conductivity of gallium arsenide, the difference between the maximum safe ambient temperature and the maximum junction temperature is larger than that for silicon. Based on our findings, we believe that a junction temperature of 350°C and an ambient temperature of 300°C are more appropriate maximum safe temperatures than the theoretical limit given above. These theoretical considerations are based on idealized assumptions of the thermal generation of carriers and do not take into account mechanisms for the generation of excess leakage currents prevailing in gallium arsenide transistors. The main limitation is indeed not the magnitude of the current gain but the excessive leakage current and the stability of the leakage current. This means that field-effect transistors, such as those described in this report, cannot be considered alternatives because of the high gate leakage current, though the transconductance stays fairly constant as expected based on the temperature variation of the majority carrier mobility. The leakage current, in turn, is related to the surface properties of gallium arsenide, which are quite different from those of silicon. It is therefore the inherent property of the material that limits the fabrication of devices which can be operated safely at temperatures near the theoretical limit. Surface problems in gallium arsenide also make it very difficult to fabricate MIS devices and are the major reason for the instability of other gallium arsenide devices such as light emitters.

Stability of passive components is determined by the type of chemical reaction that takes place between the resistor material and the ambient gas. Pyrolytically deposited carbon resistors encapsulated in glass perform well in the range where gallium arsenide transistors can be safely operated. They cannot be used easily, however, in microelectronic circuits. Thick-film palladium oxide resistors can be integrated but are not as stable. Thin-film resistors changed less than 10% during 500 hours of operation at 400°C and typically 1% during 1000 hours at 300°C.

Encapsulation techniques for present day semiconductor devices work satisfactorily at higher temperatures although can leakage occasionally was found to be the cause of device failure. Testing of devices and circuits at 400°C is difficult because of the oxidation of leads and circuit parts and because of the lack of suitable sockets and connectors. One conclusion of this report is that high-temperature electronics requires not only new technologies for active devices but also improved technologies for passive components, encapsulations, circuit fabrication and testing.

SECTION II

MATERIAL PREPARATION

A. GENERAL

Previous work on GaAs transistors has shown that device performance is affected by the material fabrication technique, by the type of impurity used for doping the substrate and the epitaxial layer, and by the doping level. Theoretical considerations, supported by experimental results obtained from GaAs devices (such as transistors, Gunn oscillators, and electro-optical devices) have shown that Group IV donors, such as tin, germanium or silicon, are preferred over Group VI donors, with the exception of sulfur. Therefore, a process was developed for the work on this program to deposit reproducibly Sn-doped epitaxial layers on Sn-doped, (100)-oriented substrates. The epitaxial deposition system was of the halide transport type. Other systems such as the water vapor transport reactor, the elemental source reactor, and solution growth techniques were also employed to find the most suitable material fabrication process. The different fabrication techniques are described in the following paragraphs. In addition to epitaxial GaAs, bulk material was used for device fabrication.

B. VAPOR PHASE EPITAXIAL GaAs

1. Halide Transport System (Sn-Doping)

The material used in this work is provided in the form of vapor-phase epitaxially deposited layers of GaAs that are grown in a system referred to as the automatic reactor. This TI-built system consists of all of the temperature controllers, furnaces, flow meters, and plumbing necessary to perform standard epitaxial processes. Temperature sensing devices, timers, electrical switches and relays, and solenoid-operated valves are controlled by an Acton programmer, which may be set up for several different types of operations. For a particular operation, such as a normal deposition run, the programmer automatically steps through the various operations involved, each time producing the prescribed conditions for a given function. Aside from occasional adjustments in the system, the only operator-dependent step in the preparation process is the predeposition clean-up of the substrate material.

GaAs slices from tin-doped crystals having carrier concentrations in the range of 4 to 8 $\times$ 10^{17} cm^{-3} are routinely used for substrates. These slices are cut in the (100) orientation and receive a chemical polish with hypochlorite solution. To prepare a substrate for deposition, degreasing with a suitable solvent such as methanol or trichloroethylene removes any traces of wax left after the sawing and polishing. A short chemical etch with 5:1:1 (H_2SO_4:H_2O_2:H_2O) etch is then used to remove any remaining surface damage. Immediately after the slice is dried in a stream of nitrogen gas, it is placed in the reactor under a flush flow of helium.

Epitaxial crystal growth is accomplished in a quartz reactor of the open-tube, gas-flow design, using "arsenided" gallium (gallium saturated with GaAs) as the feed material and $AsCl_3$ as the transporting agent. This system is described in more detail by others[1,2,3] and is shown schematically in Figure 1. The purity of the deposits obtained depends quite strongly on the starting materials which are: metallic gallium (99.9999+ %); $AsCl_3$, which is fractionally distilled in our laboratories (exact purity value unknown); and hydrogen (as a carrier gas), which is purified by means of a palladium diffusion process. Before the system can be used to grow epitaxial deposits, it is necessary to saturate the gallium feed source with arsenic. This "arseniding" step is performed by passing $AsCl_3$-saturated H_2 over the gallium boat, which is maintained at normal depositing temperature (900°C). After saturation, a film of arsenic can be seen to form at the exhaust end of the reactor, and the system is ready for use. Precompounded GaAs used with metallic gallium can also serve as feed material, reducing the time required for arseniding, but this approach also sacrifices to some extent the level of purity attainable in the deposited layers. Typical run conditions consist of temperatures of 900°C and 775°C for the feed and substrate, respectively, and a total gas flow of about 500 cc/min is maintained through the reactor. Of this total, 190 cc/min of carrier gas pass through the $AsCl_3$ bubbler. With these conditions, deposition rates of 5 to 7 μm/hr were observed. Recently, the reactor was modified by changing from a flat, fixed-position substrate holder (as illustrated in Figure 1) to one with an inclined holder at about 45° from horizontal. This new holder has a plate that measures about 1 inch by 2 inches and has improved flexibility over the previous design, in that the position of the substrate in the reactor can easily be changed. With this modification, growth rates ranging from 9 to 18 μm/hr have been achieved.

The epitaxial layers are tin-doped by using a diffusion cell which may be filled with anhydrous stannic chloride or mixtures of $SnCl_4$ and $AsCl_3$. The cell, depicted in Figure 2, consists of a chamber for the volatile liquid connected to the mixing chamber with a 1-mm-diameter and 10 cm long capillary tube. The doping mixture is then carried to the substrate zone of the reactor by sweeping out the mixing chamber with a stream of purified H_2. Doping levels obtained by this system depend on the concentration of the solution used and its temperature. In the present work, a 10 percent (volume) mixture of $SnCl_4$ in $AsCl_3$ is used. By maintaining the temperature of the reservoir at about 20°C, doping levels in the mid-10^{16} range are obtained on a reasonably reproducible basis.

The approach to the materials aspect of this program has been to attempt to develop the preparation process to a point that a reasonable consistency in the quality of the epitaxial layers can be achieved. Although the doping levels of the deposits have been found to be extremely sensitive to such factors as changes in total $AsCl_3$ flow rates and the temperature of the diffusion cell, the use of the automatic system serves to regulate these factors, keeping the doping levels reasonably consistent. Determination of the electrical properties of the layers has been limited to a simple point-contact reverse breakdown (PCRB) voltage measurement, and the layers deposited for the work typically exhibit breakdowns on the order of 30 to 40 volts. A sample of epitaxial material grown on a semi-insulating substrate has been evaluated by means of Hall measurements. This tin-doped slice, which exhibited 20 to 25 V (PCRB) was found to have a carrier concentration of 2.2×10^{17} cm^{-3} and a room temperature mobility of about 4100 cm^2/V$_{sec}$.

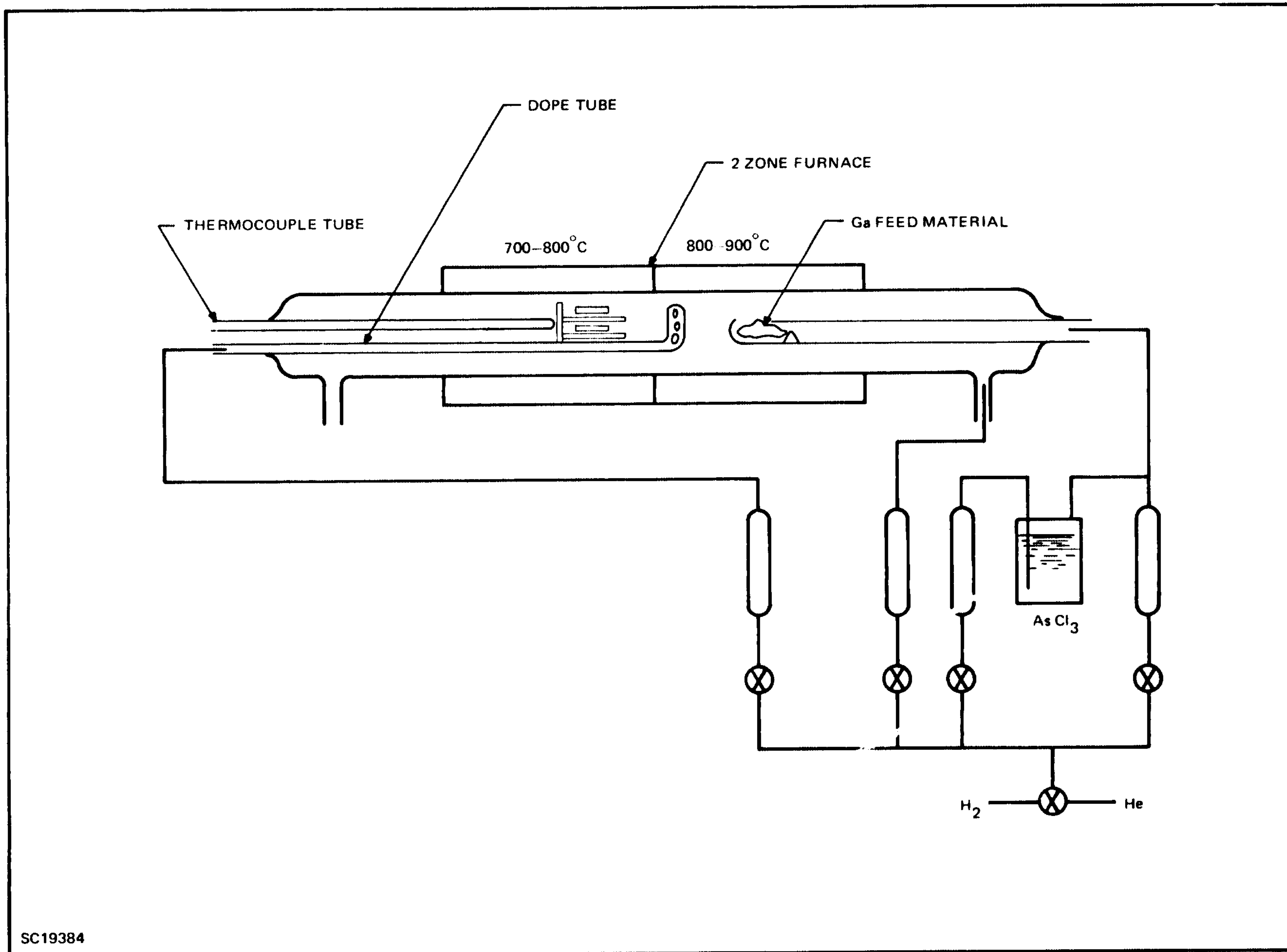


Figure 1. Epitaxial Reactor

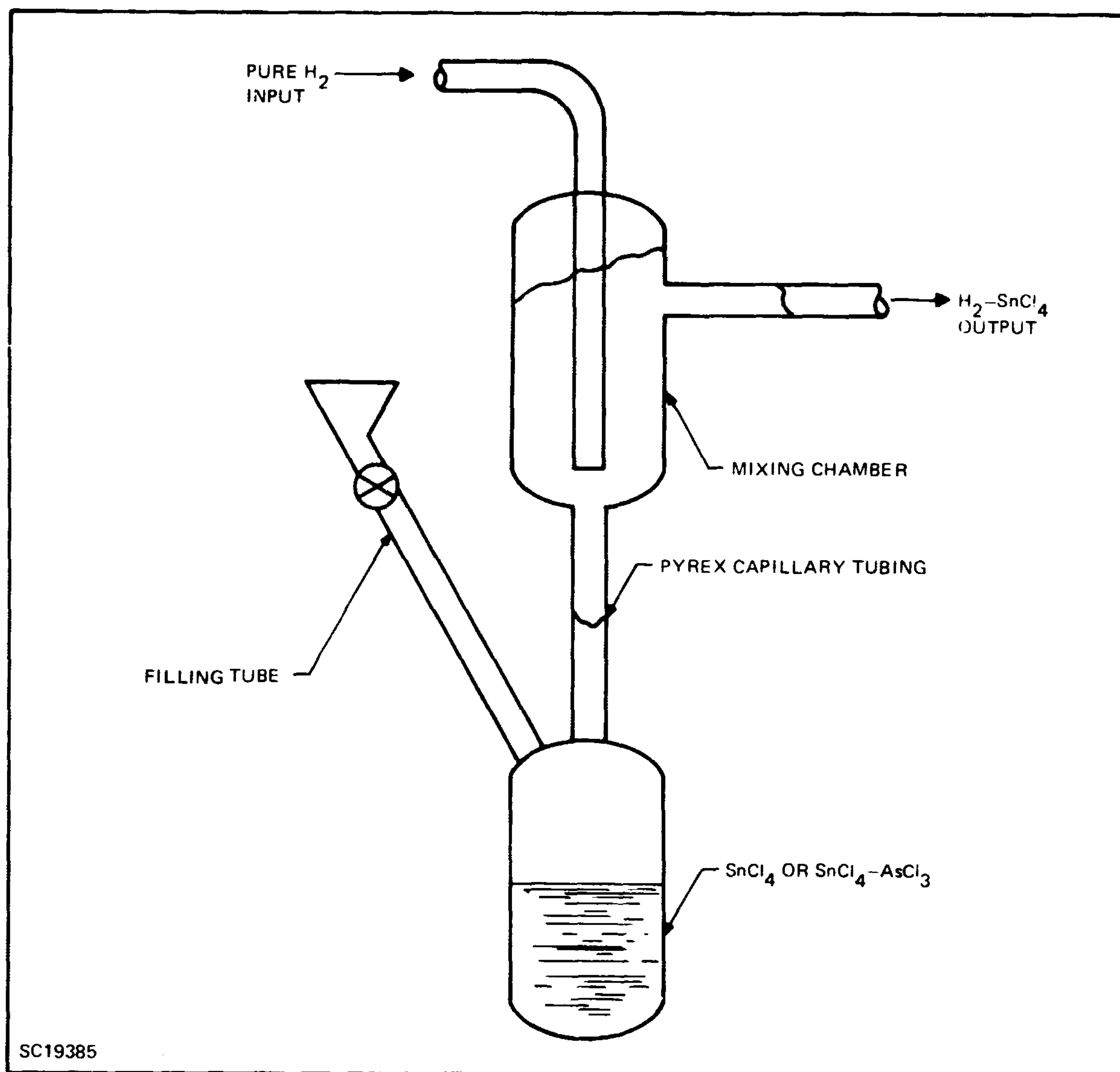


Figure 2. Diffusion Cell used for Tin Doping

Deposit thicknesses, which are not critical above a minimum value of 10 to 12 μm, have not achieved the run-to-run reproducibility desired. Thickness measurements are made by bevel-lapping a small piece of the deposited slice at a known angle (usually 5°) and using an electroless gold-plate solution to stain the lower resistivity substrate. By means of a calibrated microscope eyepiece and the appropriate calculations, the layer thickness is determined. For a given deposition time, successive runs may result in layers that differ in thickness by as much as 10 μm. Although the level of feed material in the source boat and the amount of extraneous deposition on the reactor walls probably affect growth rates, no consistent pattern has been observed to account for the difference in thicknesses. Very large area substrates generally exhibit a tapering effect, with a 5 μm thickness variation over the slice not uncommon.

2. Halide Transport System (S-Doping)

In order to obtain sulfur-doped deposits, the diffusion cell was filled with a solution of 0.5 percent (vol.) sulfur monochloride in $AsCl_3$. After several runs with the solution temperature maintained at 0°C, it was found that the doping level achieved was higher than the desired value, as indicated by point-contact reverse-breakdown (PCRB) measurements of 10 to 15 V. Further dilution of this solution to a value of 0.25 percent S_2Cl_2 was then made with $AsCl_3$. The epitaxial material prepared with this dopant concentration (again maintained at 0°C) has consistently yielded breakdown measurements of 20 to 30 V.

Since it was thought that material fabricated under a previous contract (AFAL-TR-66-361) and used here for manufacturing high temperature transistors was contaminated with Cd, a series of runs was made to produce Cd-compensated epitaxial slices. Cd was introduced by adding 50 mg of 1×10^{17} cm^{-3} Cd-doped bulk GaAs to the feed material. Donor doping was accomplished with S_2Cl_2. Carrier concentrations in these compensated slices ranged from 2 to 20×10^{15} cm^{-3}.

3. Water Vapor Transport System (Undoped)

In addition to the material produced in the automatic reactor chloride transport system, slices have been obtained from two other reactor sources. These slices make possible the relative evaluation of variables, such as substrate dopants, orientation, and layer doping levels, as well as the obvious comparison of the reactor systems themselves. The reactor used in the water-vapor transport system closely resembles that of the automatic reactor (see Figure 1), except that no modifications for doping are made with this method. Several major differences in operation are required by this process. Precompounded GaAs is used as a feed source, and by selecting the doping of the bulk feed material, the doping levels of the epitaxial layers can be controlled. As the name indicates, water is used as a transporting agent, replacing the $AsCl_3$ used in the automatic reactor system, but the method of introduction is the same, namely, saturating a stream of carrier gas (H_2) with the transporting agent by passing it through a bubbler. Although no extensive studies have been made to evaluate the effect of the purity of the water used, de-ionized water has been found to be satisfactory for use in this reactor system. Probably the most critical difference inherent in this method is the fact that substantially higher reactor temperatures must be used. Typically, the feed temperatures employed are on the order of 950°C to 1050°C with the substrates maintained at a temperature 50°C to 100°C lower than the feed.

4. Elemental Source System (Ge-Doping)

The elemental source method requires a modified reactor design (see Figure 3). High purity (99.9999+ %) gallium and arsenic, used as starting materials for the system, allow variation in the vapor phase stoichiometry. The arsenic content of the vapor stream is controlled by varying the temperature of the arsenic source boat, which determines the vapor pressure of the solid material. Purified H_2 sweeps the arsenic vapors down the reactor where it is mixed with the gallium species. The gallium is transported with HCl, which is generated from purified $AsCl_3$ by passing $AsCl_3$-saturated H_2 through a quartz reduction tube filled with crushed quartz and heated to 900°C. The arsenic produced by this reduction condenses out of the stream at the cold end of the

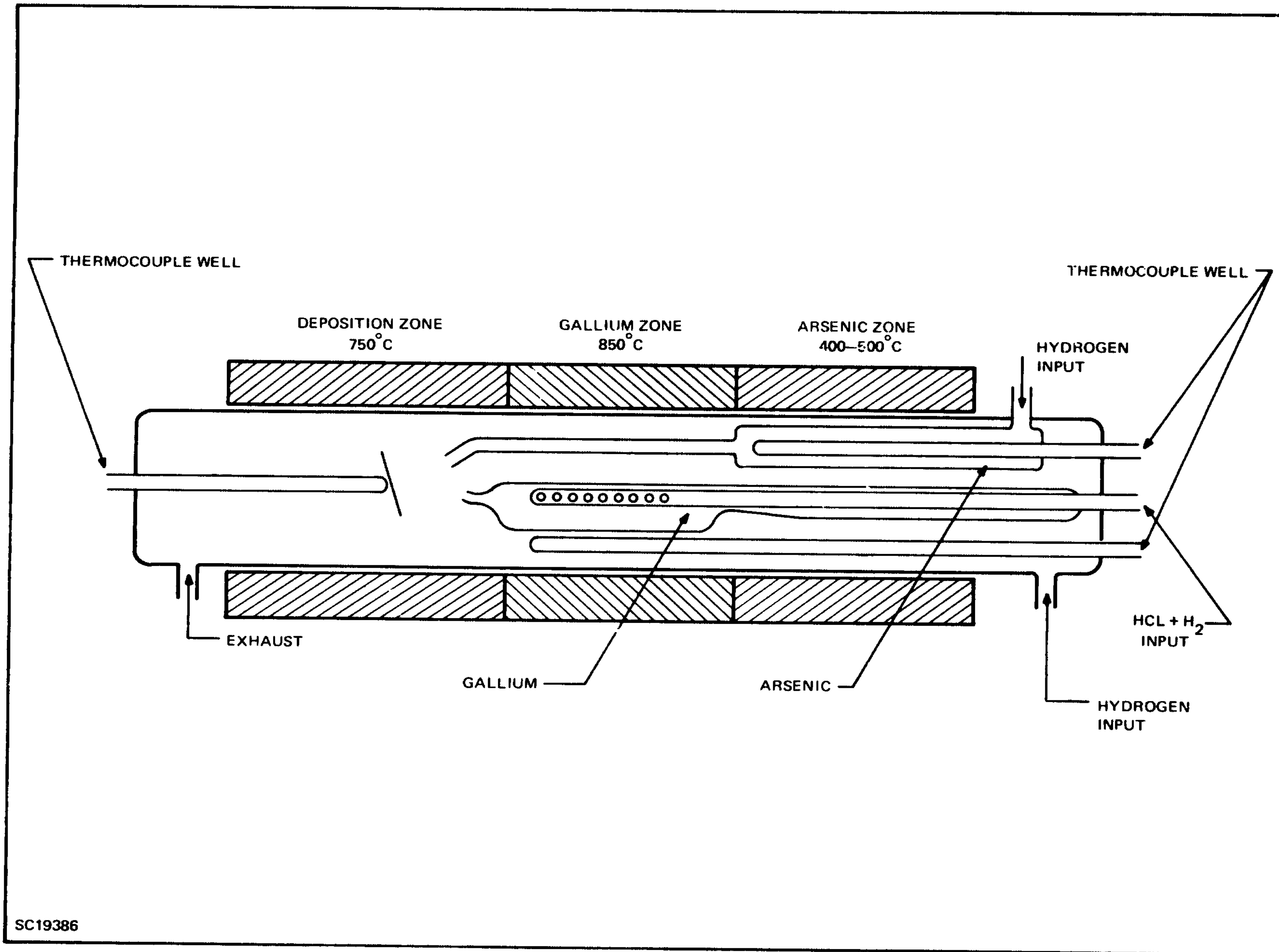


Figure 3. Elemental Source Reactor

reduction furnace and does not enter the reactor system. The amount of gallium transported by this process is controlled by the flow rate of the carrier gas through the $AsCl_3$ and the temperature (vapor pressure) of the $AsCl_3$ reservoir. Typical operating temperatures are shown in the schematic drawing, Figure 3, of this reactor system.

In the following section, it will become apparent that epitaxial GaAs prepared in the "$AsCl_3$-Ga" reactor, or in the "elemental" reactor system, was superior to GaAs produced by "water vapor" transport. Both the "$AsCl_3$-Ga" and "water vapor" transport systems are fixed gas composition systems; the "elemental" system can utilize variable gas-phase compositions, e.g., various Ga:As, or Ga:Cl gas-phase compositions. This system was thus selected to determine what effect gas-phase composition had on materials' properties as reflected by cathodoluminescence and device performance.

A series of samples was prepared with varying Ga:As ratios in the gas phase. Substrates were (100)-oriented and heavily doped N-type. No intentional dopant was added to the gas phase. These samples had apparent donor concentrations which varied depending upon the Ga:As ratio in the gas phase (see Figure 4). They were then used in the cathodoluminescence study.

A second set of samples was prepared in which $GeCl_4$ was added as a dopant to the gas phase. The dopant source was 10 percent $GeCl_4$-$AsCl_3$ in a diffusion cell. The dopant was added so that it mixed with the reactants in the zone immediately before deposition. These runs produced epitaxial layers which had carrier concentrations of $\sim$ 1 to 5×10^{18} cm^{-3}. This concentration did not vary with Ga:As ratio over the range investigated.

The next series that was prepared used a 0.1 percent $GeCl_4$-$AsCl_3$ dopant source. The results obtained are also shown in Figure 4. Carrier concentrations in these samples vary depending upon the Ga:As ratio. However, over most of the range investigated, the dependence is opposite to that seen with no intentional doping. This effect could be due to the dopants in each instance. It is suspected that with no intentional doping, the background is caused by a Group VI element, which could be introduced either from the elemental arsenic source (the $AsCl_3$ used as the HCl source) or the N-type substrate. Germanium, being a Group IV element, is incorporated differently from a Group VI element. Increasing arsenic concentration would tend to reduce the Group VI element solubility, while it would favor Group IV element solubility on gallium sites (donor sites for germanium). This means the yet unexplained portions of the curves are those with decreasing donor concentration at higher arsenic temperature when doped with germanium. It was also found that the growth rate increased with increasing Ga:As ratio, thus enhancing the probability for a dopant atom to be incorporated into the lattice.

To study the effect of the substrate, runs were repeated with Cr-doped, semi-insulating substrates, using a 0.1 percent $GeCl_4$-$AsCl_3$ dopant source. This time, the concentration of donors in the deposit decreased with arsenic temperature as shown in Figure 4. So far, only (100)-oriented substrates have been used. Other orientations might give different results. The standard starting material for transistor fabrication was prepared in the halide transport reactor. This system has a Ga:As ratio of about 2 if the Ga solution is not yet completely saturated with As. This ratio decreases with increasing degree of saturation.

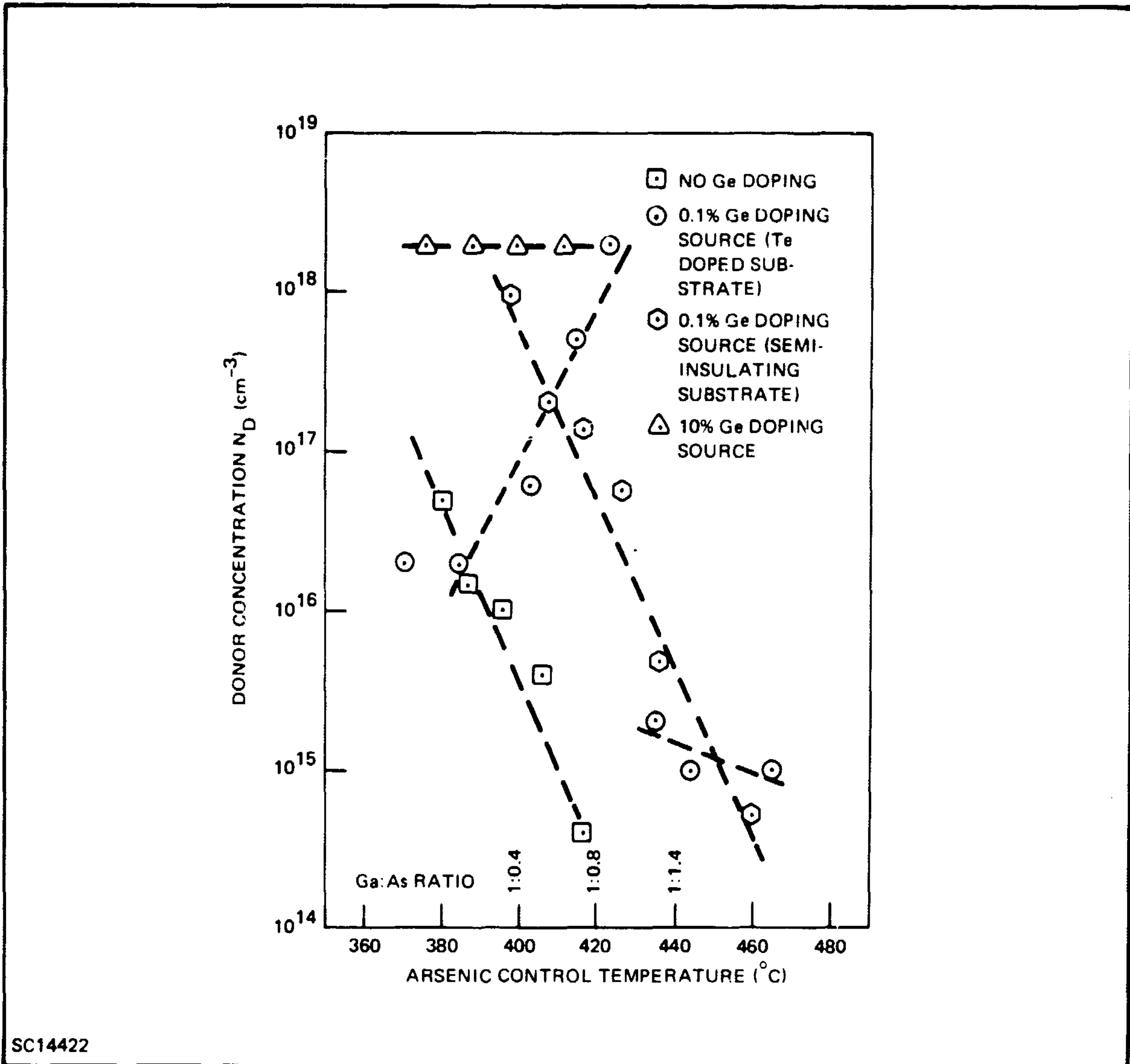


Figure 4. Donor Concentration versus Arsenic Control Temperature

Considering Figure 4 again, it is recognized that small changes in the concentration of dopant source and small changes in the Ga:As ratio can affect the electrical properties of the deposit considerably. Also, the element used for substrate doping and the substrate orientation have an influence.

C. SOLUTION EPITAXIAL GaAs

Solution growth of GaAs has developed into a technology that allows fabrication of high-quality material for many different devices such as Gunn oscillators[4] and light emitting diodes[5]. Recently, solution-grown GaAs P-N junctions have been formed that were doped amphoterically with silicon.[6] We have applied this technique to make materials for transistor fabrication. The apparatus is shown in Figure 5. The gap shown in the center of the crucible serves the purpose of providing growth boundaries. It was found empirically that such an arrangement yields better surfaces.

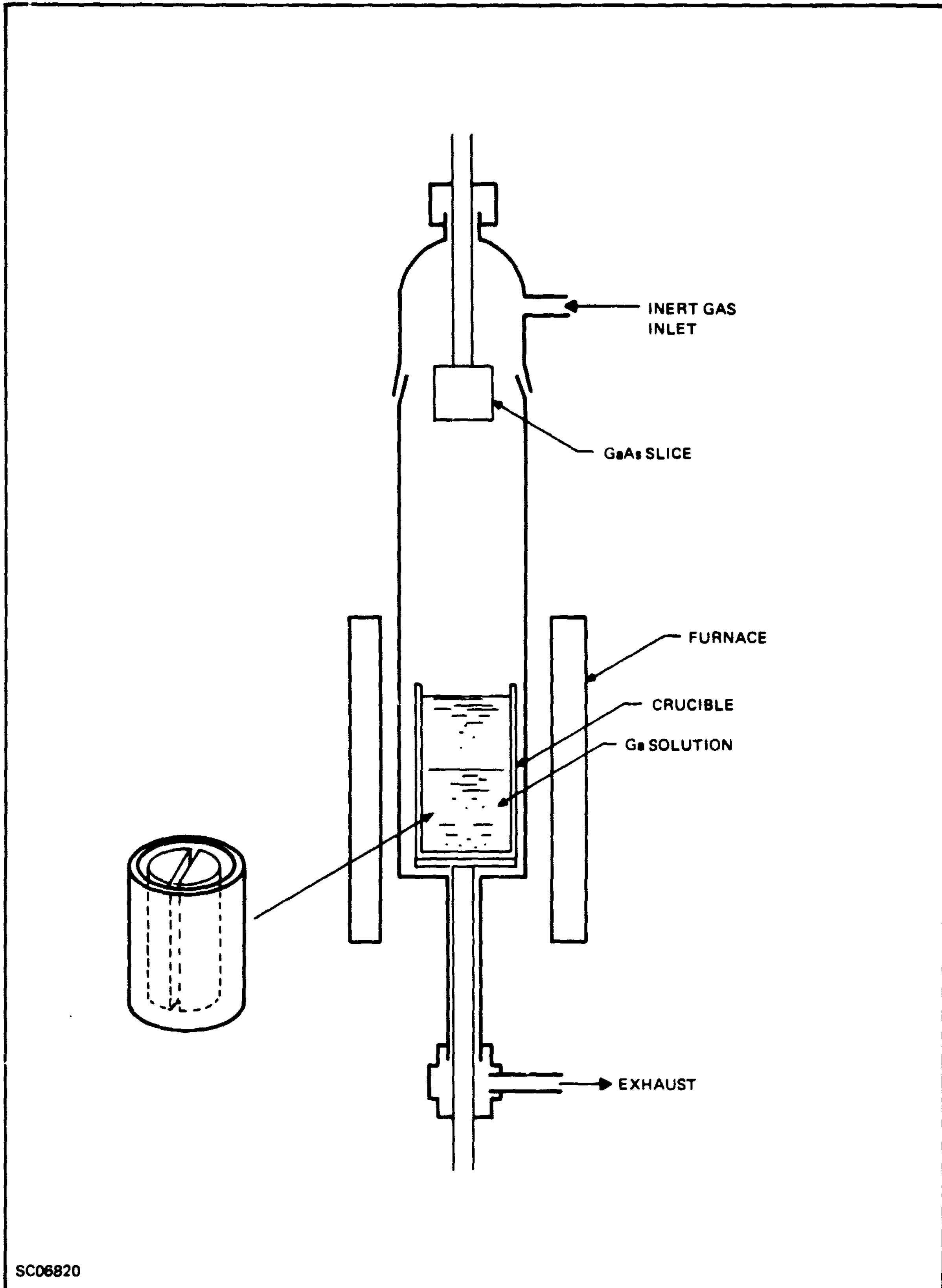


Figure 5. Apparatus for Solution Growth of GaAs

Solution-grown P-N-P-N layers were formed by inserting an N-type substrate into a gallium melt saturated at 860°C with GaAs. Silicon was added as a dopant, preferentially occupying donor sites at temperatures below 840°C. Upon cooling from 860°C, an N-P layer is grown on the N-type substrate. After reheating and cooling again, a second N-P junction is formed. The growth cycle is shown schematically in Figure 6. Solution-grown material is used for fabrication because of the long diffusion length observed in this material. A common-base current gain of 0.6 was observed for a 25-μm-thick base layer using a conventional sulfur-diffused emitter. This corresponds to a diffusion length of at least 20 μm, about one order of magnitude higher than in non-solution-grown GaAs. This property was also confirmed by cathodoluminescence measurements, the technique of which is described in Section III. The transistors were made by etching off the top P-layer and mesa-etching the emitter. All transistors had low gain because of the wide base layer and were not used in high temperature tests.

D. BULK MATERIAL

Though attempts have been made earlier in this laboratory and elsewhere to use bulk material for device fabrication, transistors were always inferior to those made on epitaxial GaAs. Recently, silicon-doped bulk GaAs pulled in a sealed system became available.* This material has properties

*Source: Bell & Howell, Pasadena, California

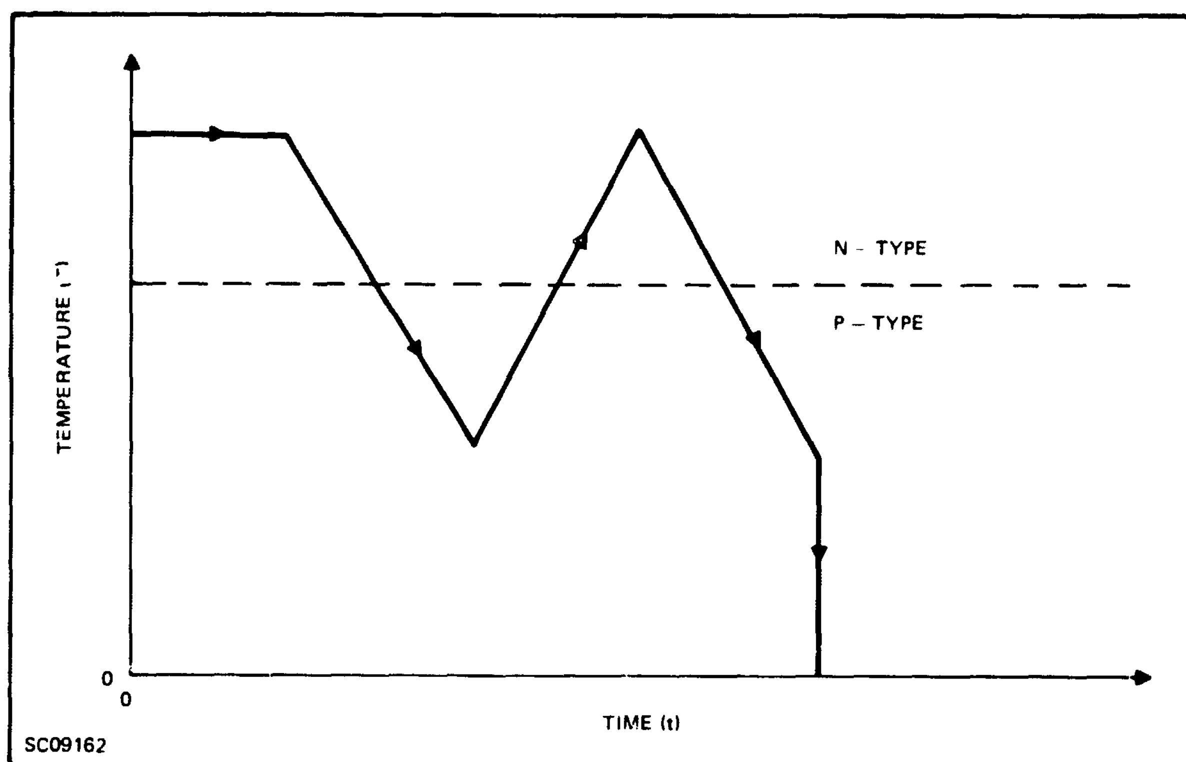


Figure 6. Growth Cycle for Fabrication on P-N-P-N Layers

similar to those of the epitaxial GaAs used for device fabrication, namely a donor concentration $N_D = 5 \times 10^{16}$ cm^{-3} and an electron mobility of $\mu_e = 5000$ cm^2/V sec Some runs on this material were very successful. If bulk material could be used for transistor fabrication, an increase in reproducibility and a reduction in cost could be expected. However the problem with Si-doped material is that it is obviously more difficult to grow. Many slices are not sufficiently uniform for a base diffusion. They show an irregular diffusion front and too low sheet resistance after etchback to the proper base-layer thickness. Only a small number of devices could be built.

For fabrication of PNP transistors, bulk GaAs doped with cadmium to 1×10^{17} cm^{-3} was used. Best results were obtained from a crystal which exhibited a very high hole mobility of $\mu_h = 680$ cm^2/V sec.

Heavily doped bulk material (2×10^{17} to 10^{18} donors/cm^3) was used as substrate for the vapor phase deposition of epitaxial GaAs. During the present work, a conversion problem was encountered that prevented for some time fabrication of transistors. The N-epitaxial collector region converted into P-type material after either the magnesium diffusion or the sulfur diffusion. This behavior could be traced back to the growth direction of the Czochralski pulled crystal. More than 70 percent of slices that came from (100)-grown material did not convert, while more than 60 percent of slices grown from (111) crystals converted. The substrates were doped with Sn in all cases. Earlier studies[7] on Te-doped material showed that the probability of conversion was higher on (100)-grown material than on (111)-grown substrate–opposite to our present findings with tin doping. One possible explanation is given in connection with the low-temperature diffusion data, in Section VI of this report.

At this point, some stated possibilities may be ruled out. Quite often, copper diffusion is given as a reason for the conversion. Though this was a possibility, we found that conversion also occurred when care was taken to remove any contamination due to copper–e.g., by rinsing slices and ampoules in KCN and employing Spectrosil instead of standard GE-quartz. Also, when a slice from one crystal that gave frequent conversions was diffused with a slice from another crystal that was not likely to convert, conversion occurred in the first slice and not in the latter. After many subsequent conversions of slices from one (111)-grown Sn-doped crystal, conversion stopped when a slice from a (100)-grown, tin-doped or a (111)-grown, Te-doped crystal was used.

Te-doped crystals showed the peculiar behavior that the Te concentration in (100)-grown crystals, as determined by mass spectroscopy, was generally lower than the electron concentration.[7] To find out whether this observation is related to the probability of conversion for tin-doped crystals, samples were analyzed for tin by an emission spectrography. In Figure 7, the tin concentration expressed in parts per million (ppm) is plotted versus the electron concentration found by Hall measurements. The solid line shows the 1 electron for 1 tin atom line. The tin concentration was found to be higher than electron concentration in all crystals, both (100)-grown and (111)-grown. Though there is not a very good correlation between tin concentration and electron concentration, the data points suggest a square law dependence. The correlation of either the electron concentration or the tin concentration in the crystal with the tin concentration in the melt is not as good. Other than growth direction, no crystal property could be found that related to the frequency of conversion of epitaxial layers. (111)-grown Te-doped crystals or (100)-grown Sn-doped crystals were finally specified for substrate material.

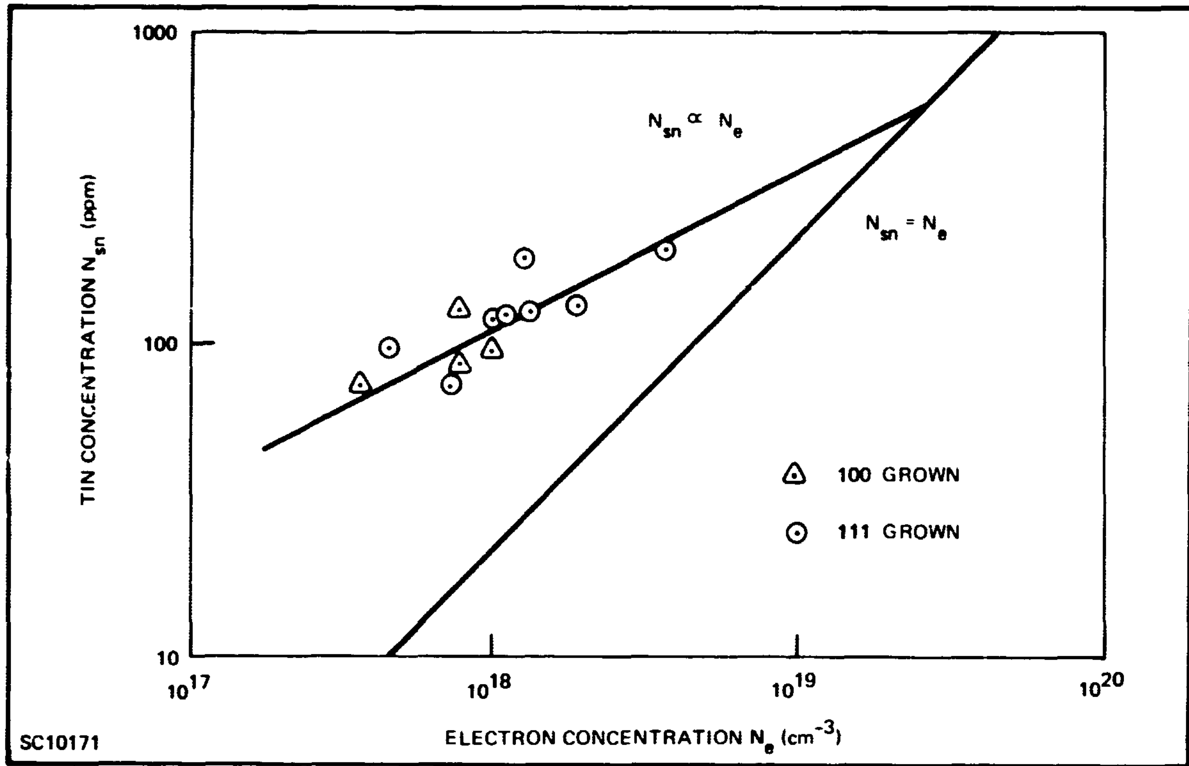


Figure 7. Electron Concentration as a Function of the Tin Concentration in (111) and (100) Grown GaAs

SECTION III

CATHODOLUMINESCENCE STUDIES ON GaAs

A. GENERAL

Transistor fabrication requires, besides the two diffusion steps, many other fabrication steps that are likely to contribute to the wide spread in transistor performance. This makes it difficult to separate the effects of the starting material from those introduced during fabrication. The three types of vapor phase epitaxial starting materials used were prepared by one of the methods described in Section II:

1) Material from the automatic reactor (A-material).
2) Material produced by the water-vapor transport technique (W-material).
3) Material from the elemental reaction (E-material).

Most good transistors made so far were fabricated on A-material. Transistors on E-material were marginal, and no good transistors were obtained on W-material. Thus, it was decided to use only A-material for device fabrication when epitaxial GaAs was called for.

Breakdown voltage, mobility dislocation density, or appearance of materials have given no criteria by which material can be selected. Cathodoluminescence experiments, then, were performed on all types of material to find out if measurements of the minority carrier properties in the materials indicate any differences.

B. THEORY

Cathodoluminescence is defined as light emission stimulated by electron bombardment of semiconducting materials. The theory was worked out by Wittry.[8] To obtain quantities such as the ratio of surface recombination velocity (s) to diffusion velocity (v_D), or the diffusion length of minority carriers (L), the cathodoluminescence intensity is measured as a function of the electron beam voltage for constant beam power. By curve fitting techniques, these quantities can be determined. The methods of calculation used by Wittry and the form of the distribution of primary electrons in the materials give a satisfactory description of the experimental results. For a first order estimate of the expected dependence of the intensity as a function of beam voltage, we will use a much simplified treatment which has the advantage of giving a clear picture of the process and a very simple form of the solution.

In a typical cathodoluminescence experiment, an electron beam is focused on an area, the diameter of which is large compared with the sum of electron penetration depth and electron diffusion length. The problem of calculating the light intensity is then reduced to a one-dimensional case. Since the energy for producing electron-hole pairs is in the order of a few times the bandgap, the electron-hole pair generation follows the primary electron distribution. In N-type GaAs (similar arguments apply to the excess electron concentration in P-type material), excess holes can recombine either radiatively, giving rise to the cathodoluminescence effect, or recombine nonradiatively. The balance equation for hoies under steady-state condition is given by

$$Dp'' - \frac{p}{\tau} + g(x, V) = 0 \qquad (1)$$

where

p = hole concentration
D = hole diffusion constant
τ = hole lifetime
x = distance from surface
$g(x, V)$ = generation function for holes

The first term gives the flux of holes due to diffusion into a given volume element per unit time, the second describes the loss of holes, and the third one stands for the number of holes generated by the incident electrons per unit volume per unit time. For a first order calculation, we will assume an exponential distribution of electrons so that the generation function is given by Lenard's law

$$g(x, V) = \text{constant } e^{-\alpha(V)x} \qquad (2)$$

where the voltage dependent parameter α is defined ˙ . analogy to the photoluminescence case as an "electron absorption constant." The constant is determined by the experimental condition that the total number of holes generated in the sample-per-unit time F, be constant. Equation (2) then assumes the form

$$g(x, V) = \alpha \ Fe^{-\alpha x} \qquad (3)$$

The hole distribution is obtained by integrating Equation (1) subject to appropriate boundary conditions. For infinitely long samples, the hole concentration zero at $x = \infty$, i.e.,

$$p_{(x = \infty)} = 0 \qquad (4)$$

At the surface, holes recombine at a rate determined by the surface recombination velocity, S, and the diffusion constant for holes. The recombination rate-per-unit are per-unit time at the surface can be expressed as

$$Dp'_{(x = 0)} = S \ p_{(x = 0)} \qquad (5)$$

The solution of Equation (1) subject to the boundary conditions (4) and (5) is

$$p = \frac{\alpha F \tau}{1 - \alpha^2 L^2} \left[e^{-\alpha x} - \frac{\alpha L + S}{S + 1} e^{-\frac{x}{L}} \right] \tag{6}$$

where we have defined

$$S = \frac{s}{v_D} = \frac{s}{D/L}$$

and

$$L = \sqrt{D\tau}$$

Equation (6) is of the same form used by Vilms[9] et. al., for the photoluminescence case except for the different meaning of α. The light intensity is proportional to the number of radiative transitions of holes and is given by

$$I = \kappa \int \frac{p}{\tau_r} e^{-\beta x} \, dx \tag{7}$$

where

τ_r = radiative hole lifetime

β = absorption constant for light generated in the sample

κ = constant depending on the optical properties of the light exit surface

Light absorption effects can be neglected for our first order calculation since the electron penetration depth is not larger than about 5 μm for 40 keV electrons (see Figure 8), while a typical absorption length for band edge light in GaAs is in order of 30 μm except for very lightly doped material, where the absorption length is shorter. Integration of Equation (7) leads to

$$I = \kappa \frac{\tau}{\tau_r} \frac{S + 1 + L\alpha}{(1 + \alpha L)(S + 1)} \tag{8}$$

or in normalized form

$$I_n = 1 - \frac{S}{S + 1} \frac{\alpha L}{\alpha L + 1} \tag{9}$$

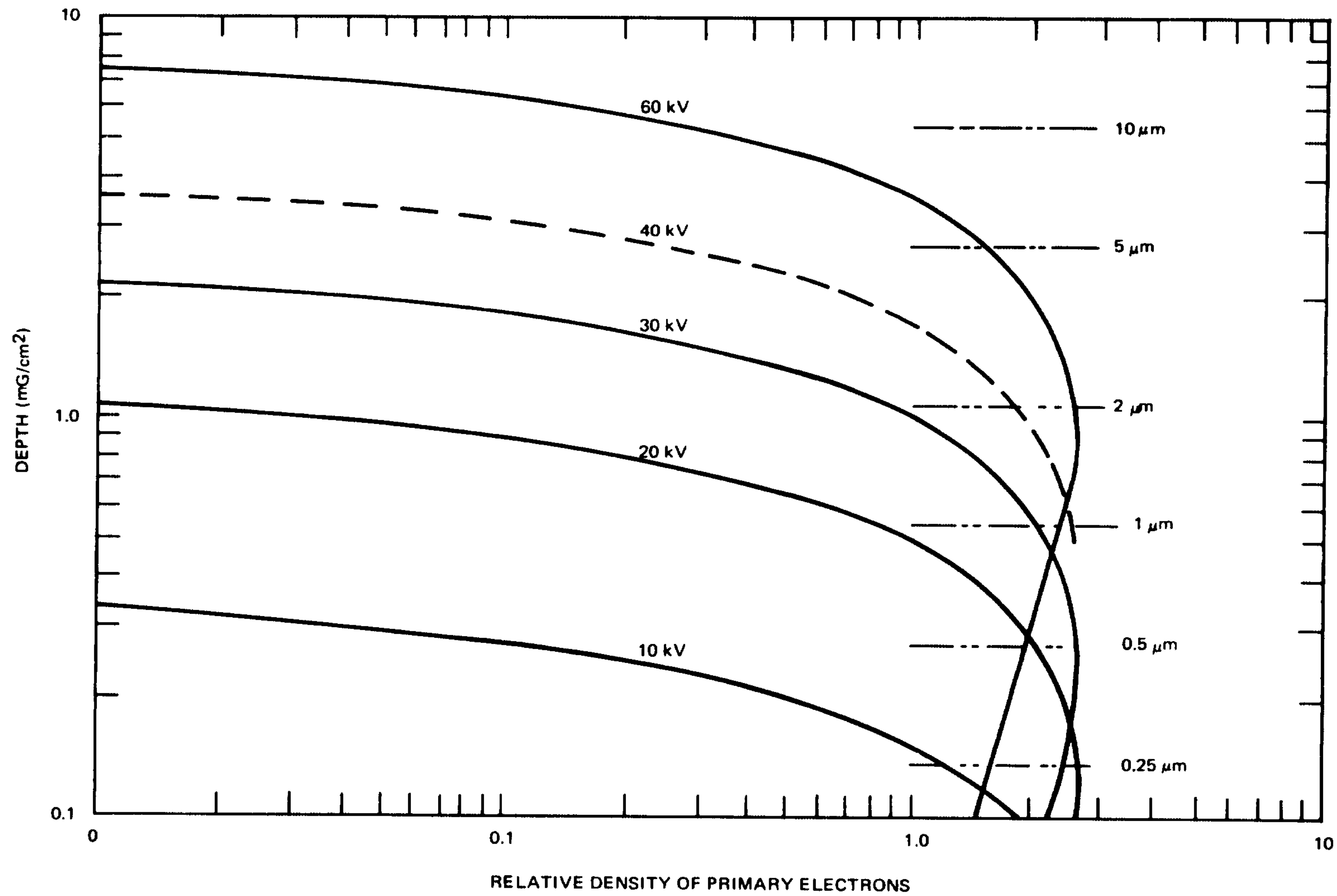


Figure 8. Electron-Beam Penetration in GaAs

where the normalization factor is

$$\kappa\tau/\tau_r$$

Equation (9) is plotted in Figure 9 (solid lines) as function of the dimensionless quantity $L\alpha$ for various values of the parameter S. As can be seen by inspection of Equation (9), the intensity is not a strong function of either S or $L\alpha$, which makes it difficult to determine one of these quantities by curve-fitting techniques. The voltage dependence of α will be taken to be that given by Cosslett and Thomas[10]

$$\alpha = 1.9 \times 10^{11} (\rho Z)^{1/2} V^{-2} = 574/V^2 \tag{10}$$

when α is measured in μm^{-1} and V in kV. A comparison with the data presented in Figure 8 shows that the absorption constant is reasonably well represented in Equation (10). For a voltage of 20 kV, the absorption length is 0.7 μm which agrees with a decrease of about a factor 2.7 of the electron concentration over that distance. Small values of $L\alpha$ correspond to large voltages and large penetration depths. For large penetration depths, Equation (8) asymptotically approaches the value

$$I = \kappa \frac{\tau}{\tau_r} \tag{11}$$

Expressing the total lifetime α as

$$\frac{1}{\tau} = \frac{1}{\tau_r} + \frac{1}{\tau_{nr}} \tag{12}$$

where τ_{nr} is the non-radiative lifetime, we obtain

$$I = \kappa \frac{\tau_{nr}}{\tau_{nr} + \tau_r} \approx \kappa \frac{\tau_{nr}}{\tau_r} \tag{13}$$

In GaAs, typical non-radiative lifetimes are in the order of 10^{-9} to 10^{-10} sec and radiative lifetimes are in the order of 10^{-8} sec so that the intensity at high voltages is proportional to the ratio of non-radiative to radiative lifetime. If we compare materials of the same donor concentration, which means roughly the same radiative lifetime, high cathodoluminescence intensity means long non-radiative lifetime. Light emitters require starting material with long non-radiative lifetimes in order to favor electron injection into the P-type region, from which almost all light is emitted. We will, therefore, consider material with a high cathodoluminescence intensity superior to material of lower intensity.

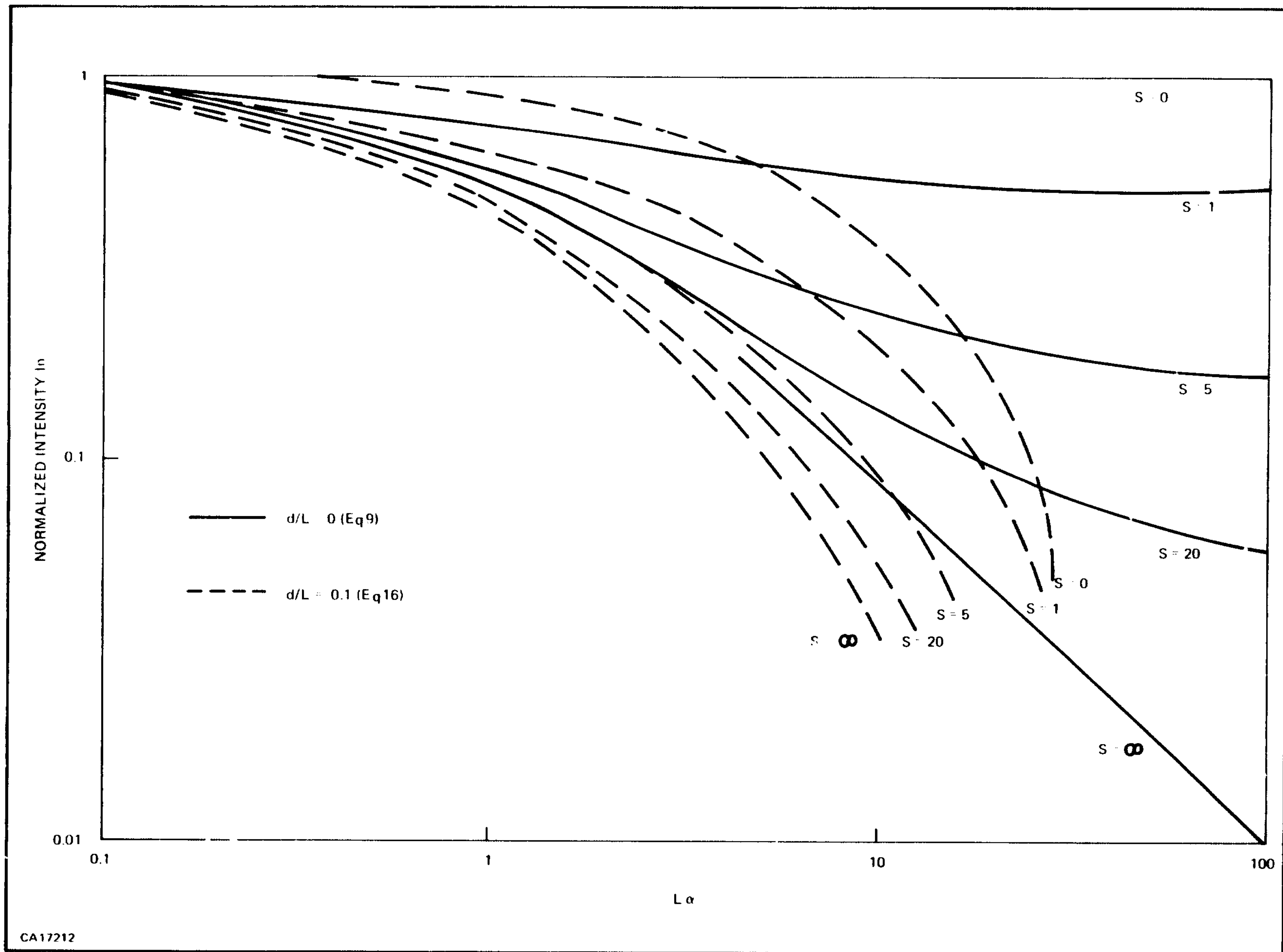


Figure 9. Normalized Cathodoluminescence Intensity as a Function of the Electron-Absorption Constant Multiplied by the Diffusion Length

Another quantity of interest and related to the total intensity is the minority carrier diffusion length. We will describe a simple technique that allows us to determine graphically the diffusion length. For this purpose, the following expression is derived from Equation (8)

$$\Delta = \frac{d(\ln I)}{d(\ln 1/\alpha)} = -\frac{L\alpha}{(S+1)+L\alpha} + \frac{L\alpha}{1+L\alpha} \tag{14}$$

For small values of $L\alpha$ and large values of S so that $L\alpha \ll 1 \ll S$, Δ increases as $L\alpha$. One can then obtain L from the slope of a plot of Δ versus α. At values of $L\alpha$, so that $S \gg L\alpha \gg 1$, Δ decreases as $1\text{-}L\alpha/S$. At $L\alpha_m = \sqrt{S+1}$, the quantity Δ reaches a maximum value

$$\Delta_m = \left(1 + \frac{S}{1+\sqrt{S+1}}\right)/(S+1) \tag{15}$$

In N-type GaAs, a typical value for (S + 1) is 20. In Figure 10, the dependence of Δ on $L\alpha$ for S + 1 = 20 is shown (dotted line). Though we have used only a rough approximation for the generation function, we expect that by plotting the experimental data in the manner suggested by Equation (14), it is possible to separate materials of different diffusion lengths.

To arrive at a value for the diffusion length from a presentation of experimental data, one first obtains the quantity d(ln I)/d(ln V) by graphical differentiation. This quantity is then plotted versus $(\text{voltage})^{-2}$. The slope of the linear portion of that curve at high voltages is then related to the diffusion length by

$$L = \left(\frac{d\frac{d\ln I}{d\ln V}}{d\,V^{-2}}\right)\frac{1}{1150} \tag{16}$$

where we have combined Equations (10) and (14). The diffusion length is obtained in μm when the voltage is expressed in kV. Though the value thus obtained for L is achieved under the simplifying assumption that the electron distribution can be represented by an exponential function, we expect that a material with a longer diffusion length also exhibits a larger value of the quantity derived in Equation (16).

The other quantity of interest, S, could be obtained similarly from the slope of a plot of Δ versus V for small voltages. For small voltages (close to the surface), the intensity is expected to change only weakly with bias, as can be seen in Figure 9. Wittry has observed that the intensity even

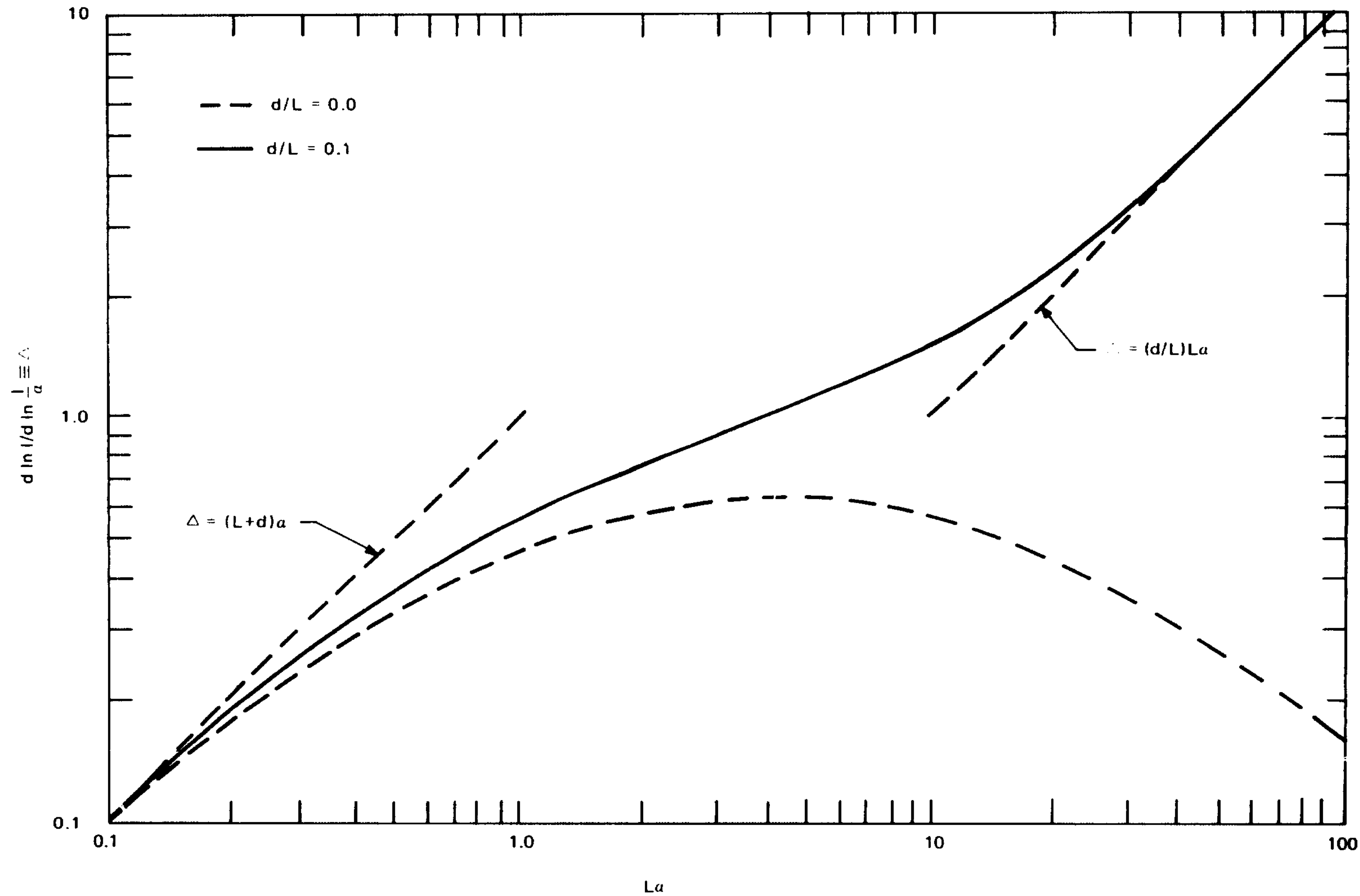


Figure 10. Logarithmic Derivation of the Cathodoluminescence Intensity as a Function of the Electron-Absorption Constant Multiplied by the Diffusion Length

at small voltages continues to drop. He explains this behavior with the existence of a "dead" layer in which no radiatve recombination takes place. We can modify Equations (8) and (14) to take account of the presence of a "dead" layer by writing

$$I = I_o \, e^{-\alpha L(d/L)} \tag{17}$$

$$\Delta = \Delta_o + \alpha L \, (d/L) \tag{18}$$

where the subscript "o" refers to the case without surface layer and d is the thickness of the dead layer. Modifying Equations (8) and (14) is equivalent to shifting the boundary of Equation (5) from $x = 0$ to $x = d$ and by integrating Equation (7) from $x = d$ instead of from $x = 0$. The solid line in Figure (10) is calculated for $S + 1 = 20$ and $d/L = 0.1$. We notice that the curves are about the same for $L\alpha < 1$ but that Δ increases with $(d/L)L\alpha$ rather than decreases as $1/L\alpha$. We expect therefore, depending on the magnitude of d/L, that for large values of α the quantity Δ either increases, stays about constant or decreases with $L\alpha$.

The term "surface effects" and "bulk properties" can now be defined more properly. We will consider the range in $L\alpha$ below the maximum of Equation (14) (see Figure 10) as dominated by bulk properties, the range in $L\alpha$ above the maximum as dominated by surface properties. That means the boundary between surface and bulk effects in our definition lies at $L\alpha_m = \sqrt{S + 1}$. For the typical values of $(S + 1) = 20$, we find $L\alpha_m = 4.5$. For a diffusion length of 1.5 μm, we obtain $\alpha = 3\ \mu m^{-1}$ and from Equation (10) a voltage of 15 kV. The voltage range for standard electron microprobes is 10 to 45 kV, thus covering the transition range from surface-dominated to bulk-dominated properties for typical GaAs samples.

C. EXPERIMENTAL ARRANGEMENT

In order to observe the cathodoluminescence output from a gallium arsenide target as a function of the depth at which the excitation occurred, the intensity of radiation is measured at several different beam accelerating voltages. As the accelerating voltage is increased, the excitation is produced at greater depths in the sample. Thus, we must measure both the intensity of the infrared radiation and the accelerating voltage. Further, we must monitor the current in the beam to maintain constant power. (The constant power requirement is essential for the derivation of Equation (8) in dimensionless quantities.) At constant beam power, the curves for intensity versus beam voltage should show an initial increase in intensity as the voltage increases. At very high voltages, the curve should level out because the surface no longer is a factor in the recombination process (see Figure 9).

The cathodoluminescence measurements were made on a Materials Analysis Company Model 400 Electron Microprobe Analyzer. The equipment is illustrated in Figure 11. A photomultiplier was fitted to the third eyepiece of the microscope on this microprobe. The radiation emitted from the sample was thereby focused onto the face of the photomultiplier. The output pulses were amplified

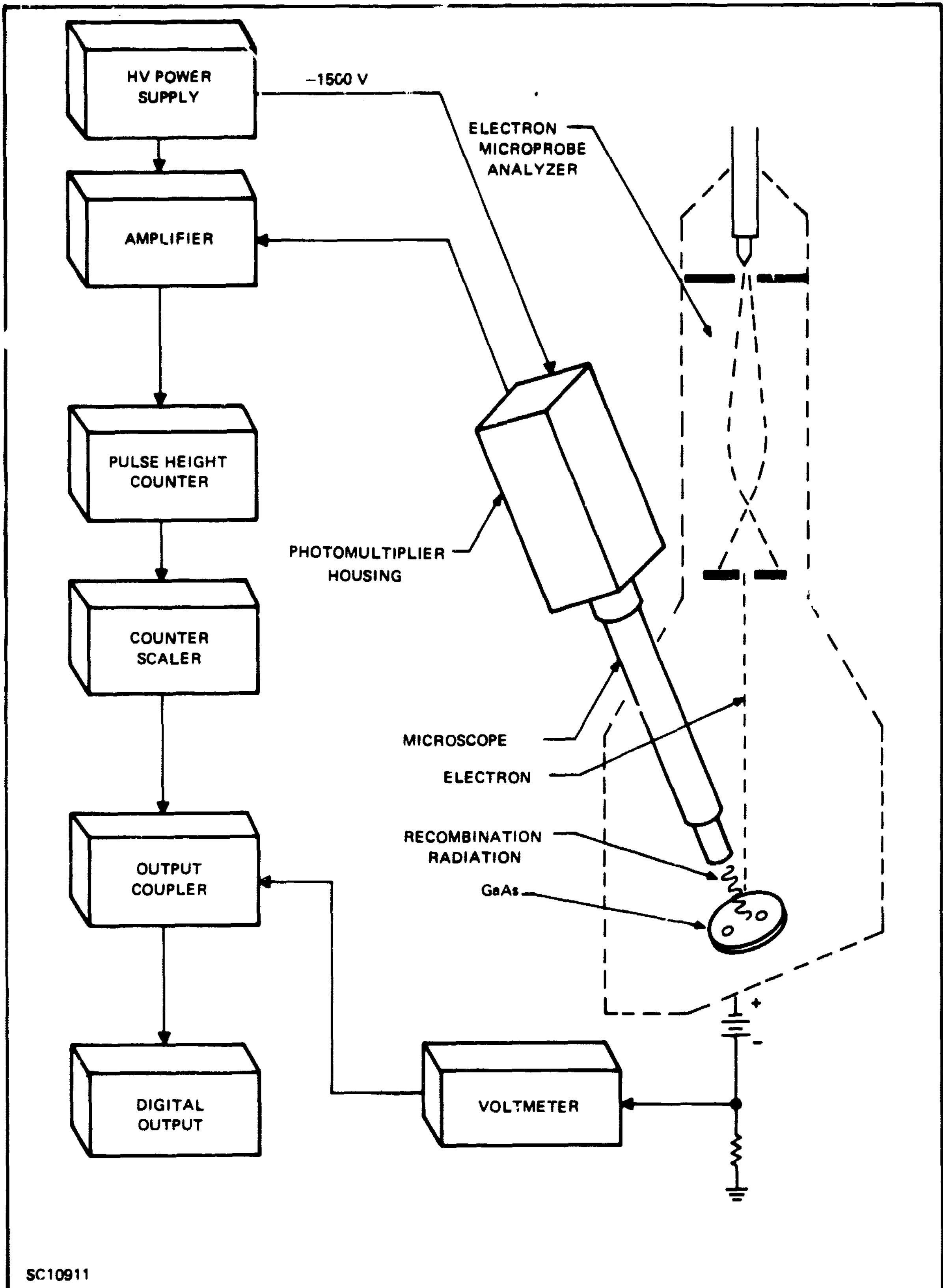


Figure 11. Diagram of the Electron Microprobe

and analyzed by a pulse height analyzer. The output pulses from the pulse height analyzer were counted and printed out. Instead of placing the photomultiplier directly on the microscope, a monochromator can be put between the microscope and the photomultiplier. This allows a study of the spectral distribution of the cathodoluminescence radiation. Experimental modifications of this type for microprobes and electron scanning microscopes are common[11-16]; therefore, we will not describe the instrumentation in detail. However, the need for careful experimental procedures is critical and should be elaborated.

The high voltage power supply was checked at the electron gun with an electrostatic voltmeter, and a correction curve was made to correct the meter readings. This correction was quite small throughout the voltage range

As the electron beam bombards the target, a contamination film deposits at the points of impact. This film is composed primarily of carbon, caused by the decomposition of vacuum grease and pump oil. It attenuates the cathodoluminescence output appreciably; therefore, the measurements must be made at the lowest possible sample currents and with the minimum time for bombardment. Two methods have been suggested for retarding the growth of the contamination film; one is by placing a cold finger just above the specimen surface, and another is by directing a jet of air or other gas at the point of impact. We did not use these methods because we found that this contamination film did not appear until the sample was bombarded for several minutes; the actual measurements require a total bombardment time of much less than a minute.

The surface recombination velocity and possibly the nature of the "dead layer" are very sensitive to the surface conditions. The exact effects of the initial electron beam bombardment and deposition of the contamination layer are unknown. It is not unreasonable to expect that a great change in surface properties can be initiated by a few seconds of electron beam bombardment. This is a matter for further investigation. On the other hand, permanent changes in the bulk semiconductor properties should not be expected at the beam energies we used.[17] However, studies on semiconductor devices by electron scanning microscopes have been shown to alter the device characteristics for short periods of time, but it has not been illustrated that this is due to a change in the bulk properties.

The measurements were all made at constant beam power, that is iV_0 = constant. This assures that the same amount of energy loss occurs at each accelerating voltage provided that i truly relates to the total power dissipation. The absorbed current can be carefully measured and printed out with the intensity data, but the effect of backscattered and secondary electron loss should be considered. The electrons striking the target are not all absorbed; some electrons dissipate energy in the target and are then backscattered. This is generally not a problem since the portion backscattered, and its energy distribution is not dependent on the accelerating voltage; thus, the backscattering always represents the same amount of power loss. Secondary electron emission from the sample is, however, dependent on the accelerating voltage. At voltages beyond a few kV, there exists an inverse relationship between secondary electron emission and beam acceleration potential. As secondary electrons are lost, the measured current becomes lower than the actual current. We therefore produce some ionizations, creating positive holes, which are not recorded by the current measurement. To compensate for this, one would increase the total beam current, but this would only compound the error. In order to reduce this error, we biased the sample at +67 volts to hold the majority of the secondary electrons in the sample.

The electron beam can heat the sample at the point of impact, thereby reducing output intensity; it can also create an electrical charge in a poor conducting sample, thereby distorting the distribution of excitation. The heating effect in gallium arsenide is not large, and when constant beam power is maintained, this effect should not be a source of error[11]. Maximum power level was 4 mW, at a current density of 5×10^{-2} A/cm^2. Charging in this semiconductor has also been shown to be minor.[18]

Before each experimental determination, an examination of the signal output as a function of absorbed current was made. Generally, this is a linear relationship, and the range of linearity of these determinations defined the experimental conditions for obtaining good data. By examining these data, the limitations imposed by dead time, poor pulse-height analyzer settings, current saturation, heating effects, etc., could be detected. Strictly speaking, the intensity should not be linear with current. Actually, we observed a very slight nonlinearity. These effects have been discussed by other workers.[12, 19] However, within the range of our normal measurements, the current and intensity are essentially linear.

We did not use a monochromator to separate the spectral distribution of the emitted light since at least with a low resolution instrument, this radiation appeared as a single, sharp spectral peak. The benefits derived by spectral selection would therefore be small; furthermore, the integrated radiation was much more intense than that which was transmitted through a light pipe and a monochromator.

The measurements were made at several random 3-mil diameter spots on each sample at each accelerating potential. The 3-mil spot size was reproduced after each change in potential. Other workers used a 5-μm diameter spot for their measurements; further, they made all observations at the same point. However, the major purpose of our study has been to develop a means for quickly evaluating bulk material. For an "on-line" evaluation, a 3-mil spot is much more realistic than a 5-micron spot. We also found that the integrating effect of the larger spot gave us more meaningful data than a smaller spot, because the samples that we studied were generally quite heterogeneous in cathode-luminescence output as far as areas in the order of several square μm are concerned. Furthermore, by observing several spots on each sample at each potential, the effects of carbon contamination buildup were held to a minimum.

D. RESULTS

GaAs samples were obtained from materials with a known device history. This means that the performance of devices from these materials is known for at least several hundred units. No attempt was made to relate the performance of one single device to the specific chip of material from which it was made. The purpose of these experiments was to determine if differences in material preparation or differences among one type of crystal are reflected in the performance of devices. Studies were made on N-type epitaxial material and on bulk material used for transistor fabrication.

1. Comparison of Epitaxial Materials Used for Device Fabrication

GaAs vapor phase epitaxial N-type GaAs was fabricated using three different reactors. The concentration was in the mid 10^{16} cm^{-3} range. Material A was grown in an automatic deposition reactor employing the halide transport technique. Material W was produced in the water vapor transport reactor and material E in the elemental source reactor. A detailed description of the three fabrication processes is given in Section II. Transistors fabricated on type A-material had gains up to 300 and were superior to those fabricated on the other materials. Transistors fabricated on type E-material had current gains up to 10, while no transistors with gains higher than 1 were fabricated on type W-material.

The cathodoluminescence intensity of these three materials is shown in Figure 12, as a function of the beam voltage. The vertical lines on each of the measurement points indicate the spread obtained when data were taken in 10 different spots. The spread is small, indicating that there are no gross nonuniformities over a 3-mil diameter in all three materials. We notice that the best material for fabrication of transistors also had the highest intensity, followed by the type E and type W material. In this experiment, all three samples were mounted on a quartz slide and received the same surface clean-up. Graphical differentiation of the curves in Figure 12 yielded the quantity d(ln I)/d(ln V), which is plotted in Figure 13 as a function of V^{-2} as suggested by Equation (16). As expected, all curves follow a straight line at high voltages and then level off (except material W, for which the sensitivity in the low voltage range was too small). The magnitude of the slopes of the straight line portions of the curves follow in the same order as the absolute intensities. In Table I, a description of the materials and the diffusion length derived from the curves using Equation (15) are given. We notice that the best transistor material also has the highest minority carrier diffusion and the highest ratio of nonradiative to radiative lifetime, while the worst transistor material exhibits the lowest such values. It should be noted that the data for the best material ($L = 2.2\ \mu m$) agree with these obtained by Wittry, et al.[18] ($L = 3\ \mu m$) and Biard, et al.[20] ($L = 3.5$) who made measurements on bulk GaAs in the same concentration range used here.

At low voltages, the curves in Figure 13, level off as can be expected from inspection of Figure 10. Values for the surface depletion layer thickness d or the reduced surface recombination velocity S cannot be obtained. It can, however, be said that the ratio d/L must be very small. A rough estimate for S can be obtained as follows: The knee in the curves of Figure 13 corresponds roughly to the point where $L_M = \sqrt{S+1}$. Using Equation (10) and rearranging the equation, S can be calculated from

$$S = 3.35 \times 10^5 \left(\frac{L}{V_M^2}\right)^2 - 1 \qquad (19)$$

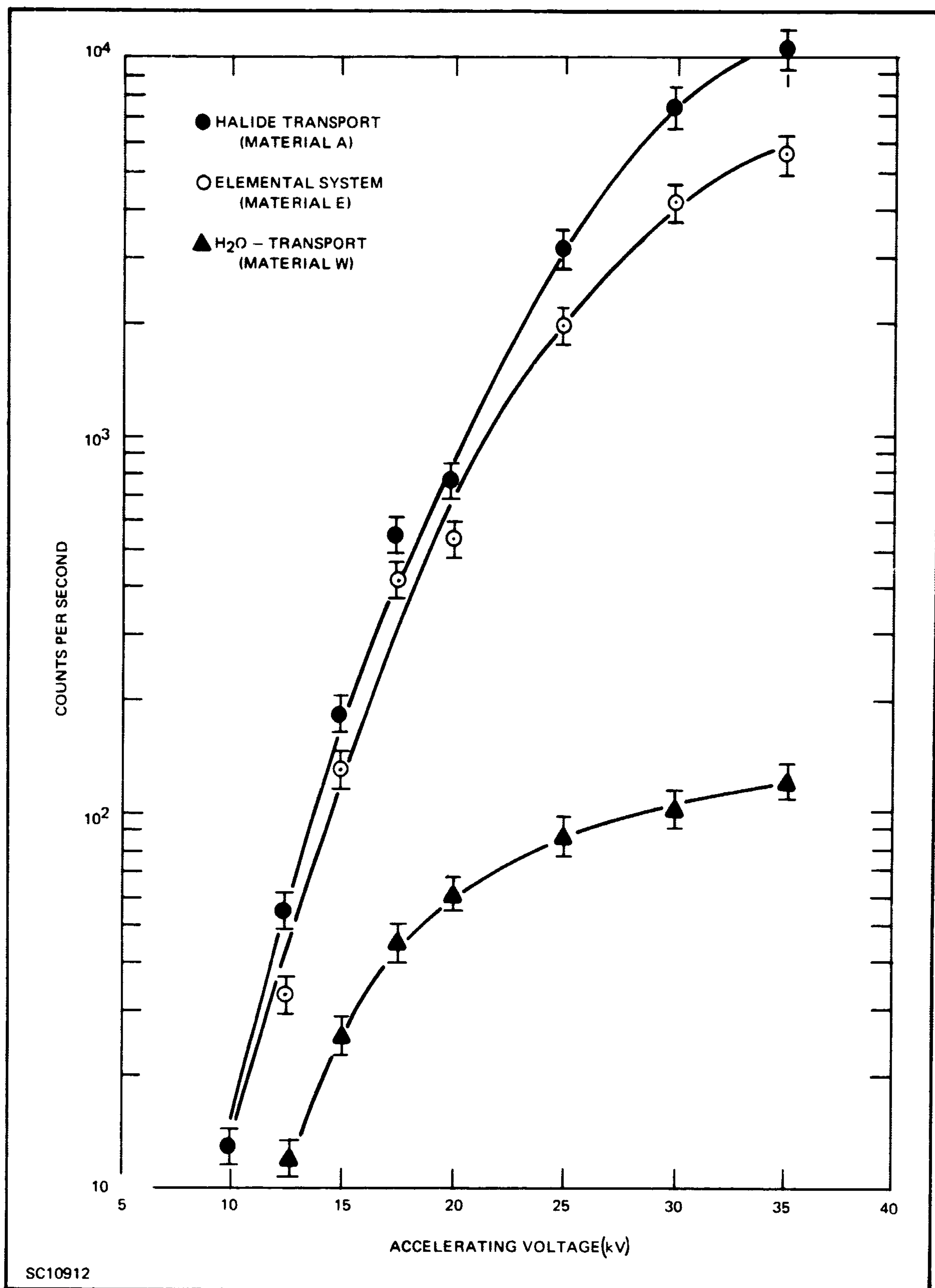


Figure 12. Intensity of Cathodoluminescence as a Function of Accelerating Voltage (Epitaxial Material)

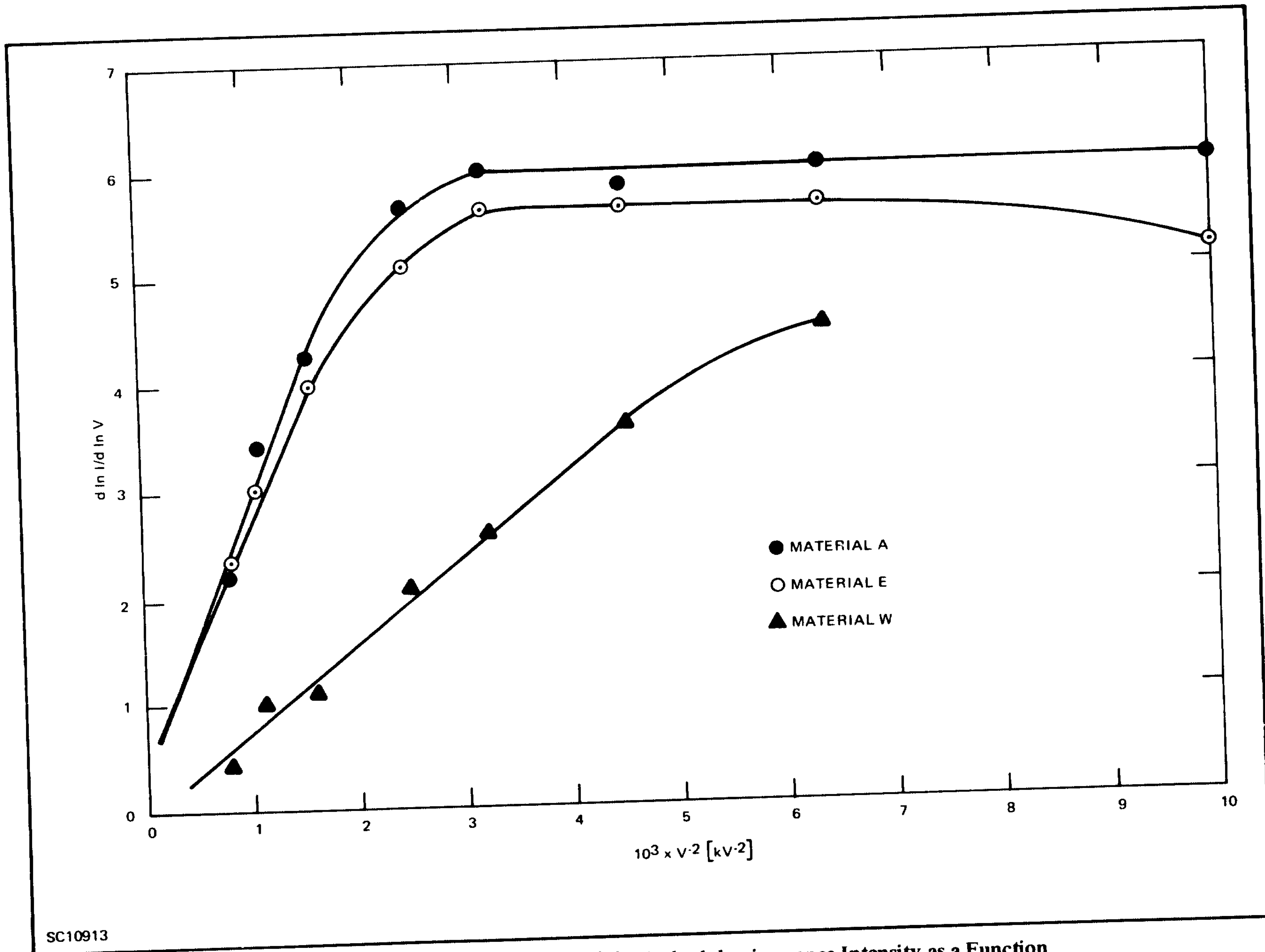


Figure 13. Logarithmic Derivation of the Cathodoluminescence Intensity as a Function of the Square of the Reciprocal Voltage (Epitaxial Material)

Table I. Comparison of Material and Device Properties

Material	Description	Dopant	Concentration	Device	Diffusion Length	Relative Intensity ($V \rightarrow \infty$)	S
Material A	Vapor Phase Epitaxy Halide Transport	Sn	$\sim 5 \times 10^{16} cm^{-3}$	Transistors	2.2 μm	107	$\sim$10
Material E	Vapor Phase Epitaxy Elemental Sources	Unknown	$\sim 5 \times 10^{16} cm^{-3}$	Transistors	1.8 μm	57	$\sim$10
Material W	Vapor Phase Epitaxy Water Vapor Transport	Sn	$\sim 5 \times 10^{16} cm^{-3}$	Transistors	0.7 μm	1	$\sim$10

For all three samples, this leads to values for S of about 10. Wittry obtained for a similar material d/L = 0.05 and S $\sim$ 20, while Biard finds S $\sim$ 14. The surface recombination velocity is estimated to be 4×10^5 cm^2/sec using a hole mobility of 200 cm^2/V sec and the experimentally determined values of S = 10 and L = 2.2 μm. The importance of the type of analysis performed here is not as much the yield of quantitative results as the fact that materials can be selected by cathodoluminescence measurements. It further means that the minority carrier diffusion length of the starting material is a meaningful parameter that relates to device performance. Because of the involvement of many parameters, the method described here will not easily yield information about comparable materials but will have merits in separating material that can be used for device fabrication, e.g., material A and E from material that is unsuitable for this purpose, e.g., material W.

2. Studies on the Spatial Distribution of Cathodoluminescent Light

A comparison of four types of transistor grade materials was made by studying the spatial distribution and the intensity of the cathodoluminescent light. The relative intensities are shown in Figure 14 over an area comparable in size to a transistor mesa. The four types of materials were

a) S-doped epitaxial material (grown under contract AFAL-TR-66-361), probably contaminated with Cd ($N_D = 5 \times 10^{15}$ cm^{-3}).

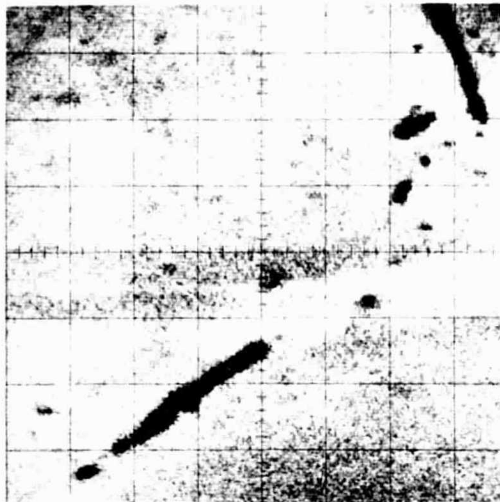
b) Standard epitaxial material grown under this contract ($N_D = 5 \times 10^{16}$ cm^{-3}).

c) S-doped epitaxial material, counterdoped with Cd ($N_D = 5 \times 10^{15}$ cm^{-3}).

d) Si-doped bulk material ($N_D = 2 \times 10^{16}$ cm^{-3}).

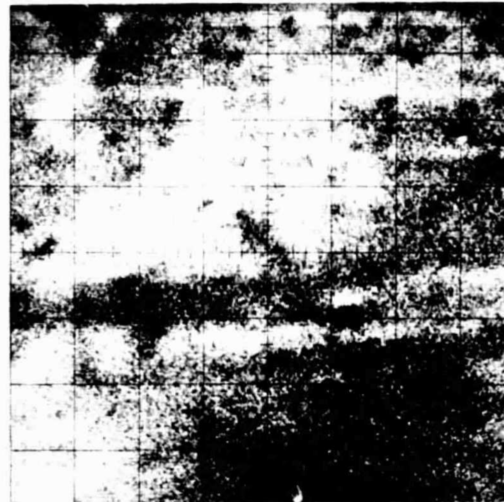
The absolute intensity measured on sample (b) was highest probably due to the higher donor concentration. Next followed the intensity of samples (a) and (c) both of comparable value. The lowest intensity by far was measured on sample (d).

A detailed analysis indicates a similarity between material (a) and (c) as far as the uniformity and intensity of the cathodoluminescence output is concerned, though the diffusion length of material (a) was somewhat larger. The bulk material showed an erratic behavior caused by gross nonuniformities in the material, though portions of this material might be superior to the epitaxial materials. This was borne out by the fa[illegible] good transistors on bulk material were distributed at random over the slice. Also, the base d[illegible]on front shows irregularities.



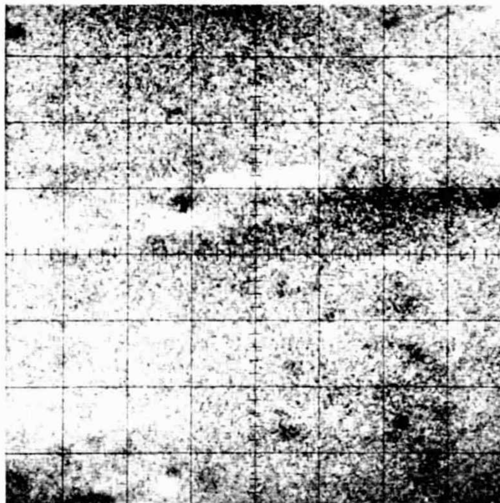
(a)

S–DOPED EPITAXIAL LAYER, (AFAL)
$N_D = 5 \times 10^{15} cm^{-3}$



(b)

S–DOPED EPITAXIAL LAYER, NEW
$N_D = 5 \times 10^{16} cm^{-3}$



(c)

Cd + S–DOPED EPITAXIAL LAYER
$N_D = 5 \times 10^{15} cm^{-3}$

(d)

BULK Si–DOPED, BELL & HOWELL
$N_D = 2 \times 10^{16} cm^{-3}$

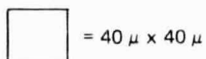


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Figure 14. Spatial Distribution of Cathodoluminescence Light

Figure 14 shows that, in many cases, the substrate material is not uniform even over the extension of a single transistor. Adding a compensating impurity such as Cd seems to improve the uniformity.

3. Dependence of Materials Parameter on the Ga:As Ratio

Experiments described in Section II show that for a given fabrication method, the properties of the material vary widely with small change in the growth conditions. Cathodoluminescence measurements were performed to characterize the deposited layer. The only other information that can be obtained is the breakdown voltage measurements which give an estimate of the donor concentration. Hall measurements are not possible because of the N^+ substrate, while deposits on semi-insulation material are not representative because the influence of the substrate materials is neglected. Though earlier experiments have shown that material from the elemental source reactor is somewhat inferior from the device point of view, this epitaxial deposition system is the only one that allows studying the effect of growth conditions on growth rate and quality of the deposit.

In Figure 15, the maximum cathodoluminescence intensity (at high beam voltage) is plotted versus the donor concentration. Donor concentration was obtained by measuring the point breakdown voltage in several regions. The average breakdown voltage was used to determine the donor concentration from published charts.[21] The numbers next to the measurement points are

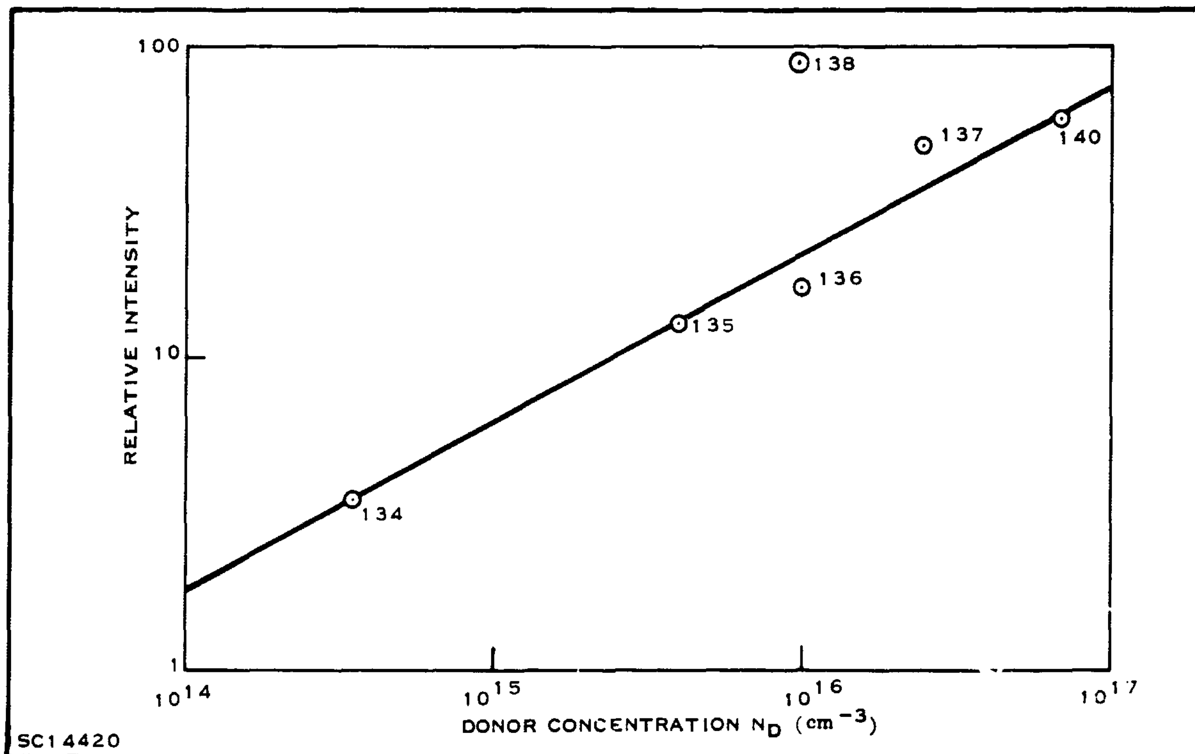

Figure 15. Cathodoluminescence Intensity versus Donor Concentration

referred to in Table II. Accuracy of the donor concentration is not better than ±50 percent. Nevertheless, the quantum efficiency increases monotonically with the exception of sample 138. So far, no explanation has been found for the high efficiency of run 138. It is of interest, however, to note that the growth rate decreases monotonically with decreasing arsenic control temperature while the donor concentration increases. But this also is with the exception of run 138.

Table II. Properties of Vapor-Phase Epitaxial GaAs (No Doping Source)

Run No.	Substrate Doping	Orientation	Breakdown Voltage (V)	Net Donor Concentration (cm^{-3})	Growth Rate (μm/h)	Arsenic Control Temperature (°C)	Relative Quantum Efficiency	Diffusion Length (μm)
134	Sn	(100)	150	3.5×10^{14}	27.0	416	35.5	1.8
135	Te	(100)	60	4.0×10^{15}	15.0	406	130.0	1.5
136	Te	(100)	40	1.0×10^{16}	12.0	396	170.0	4.7
137	Te	(100)	30	2.5×10^{16}	6.0	387	480.0	2.3
138	Te	(100)	40	1.0×10^{16}	6.8	387	920.0	3.3
140	Te	(100)	20	7.0×10^{16}	2.4	377	570.0	2.4

The quantum efficiency is proportional to the ratio of the total lifetime to the radiative lifetime, or, if the radiative lifetime is large compared with the non-radiative lifetime, the efficiency is proportional to the ratio of nonradiative to radiative lifetime. In lightly doped N-type material, the latter will be the case. The radiative transitions in lightly doped N-type material are thought to be due to donor-valence band transition.[22] Consequently, the transition probability will increase with increasing donor concentration. The quantum efficiency is therefore expected to increase due to the smaller radiative lifetime at higher donor concentrations. The efficiency, however, increases only by a factor of 20 for a 200-fold increase in the donor concentration. Cusano[23] and Casey[24] have found that for donor concentrations larger than 10^{16} cm^{-3}, the intensity increases linearly or even supralinearly with donor concentration, up to about 10^{18} cm^{-3}.

Considering now the diffusion length obtained from cathodoluminescence data, it is found that the hole diffusion length for most N-type samples is in the 1.5 to 4 μm range (Figure 16). Earlier measurements indicated that this is the case even up to a donor concentration of $\sim 8 \times 10^{17}$ cm^{-3}. Over the concentration range from 3.5×10^{14} to about 10^{18} cm^{-3}, the mobility drops by a factor of 3. The diffusion length seems to increase slightly up to 10^{16} cm^{-3}, then decreases lightly. This means that the minority carrier lifetime, which has been assumed to be approximated by the nonradiative lifetime, must increase up to 10^{16} cm^{-3}, and then stay about constant. If this conclusion is correct, the increase in quantum efficiency demonstrated in Figure 15 is due to an increase in the nonradiative lifetime rather than to a decrease in the radiative lifetime.

Another way to explain the reduction of the diffusion length at donor concentrations below 10^{16} cm^{-3} is that the diffusion length appears shorter only because of absorption effects. It has been observed that the absorption coefficient of the energy of the peak of the emission increases for decreasing donor concentration in GaAs. This means that at a lower donor concentration (10^{16} cm^{-3} and lower) the absorption length becomes comparable to the diffusion length. In this case, it is

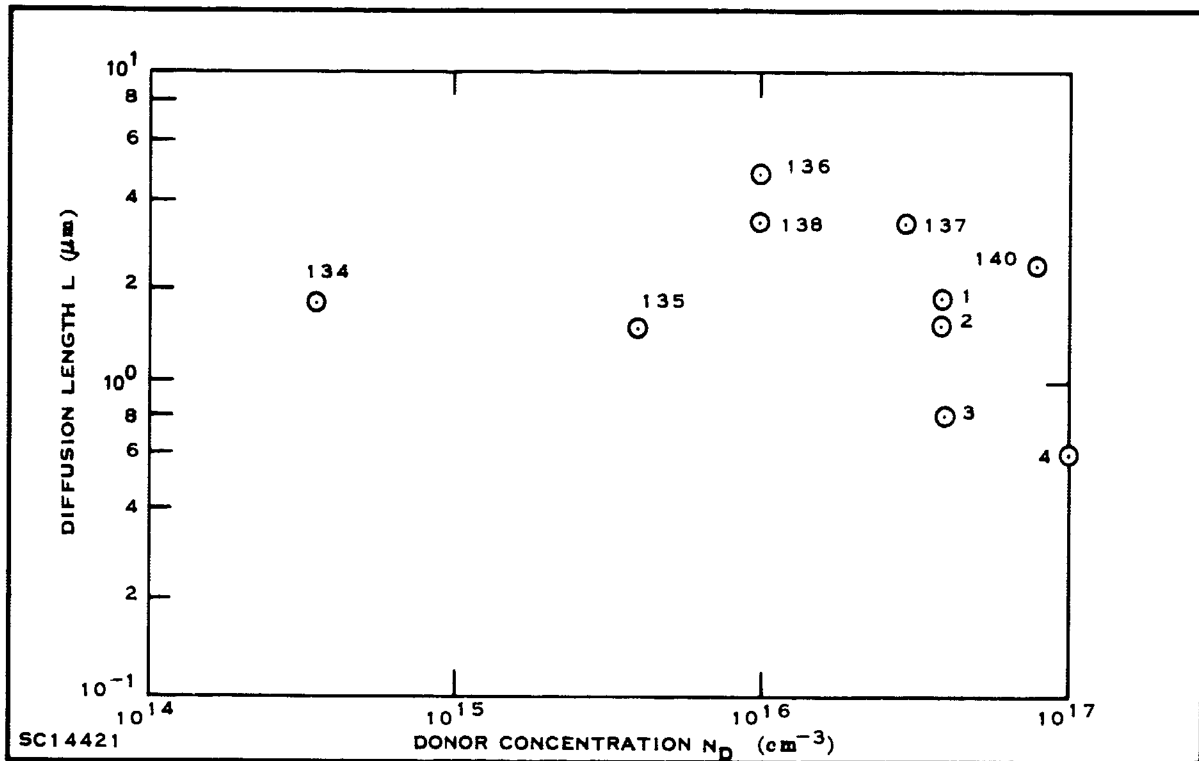

Figure 16. Diffusion Length versus Donor Concentration

difficult to perform the quantitative analysis described earlier to obtain values of diffusion length and the ratio of the non-radiative to radiative lifetime and the data might be in error. If the electron microprobe is equipped with an attachment for a monochromator so that only the low energy portion of the spectral distribution, which is not so much affected by absorption, were recorded, an improved quantitative analysis could be performed.

For comparison, we have shown results summarized in Table I, namely:

Earlier runs with the same reactor (sample No. 2, material A)
Runs with the halide transport system (sample No. 1, material B)
Runs with the water-vapor transport system (sample No. 3, material C)
Tellurium-doped bulk material (sample No. 4, not listed in Table I)

So far, experience has shown that material with a high quantum efficiency and a high diffusion length gives better devices. This means epitaxial materials in the lower 10^{16} cm^{-3} range (e.g., sample No. 136) and high deposition rates (e.g., sample No. 138) are to be preferred.

SECTION IV

DEVICE FABRICATION

A. GENERAL

GaAs transistors have been fabricated with different starting materials, bulk slices as well as epitaxial slices, different doping materials and different device geometries. Transistors with current gains up to 300 at 25°C have been fabricated which showed an exceptionally low saturation resistance, as low as 5 ohms. Planar structures had current gains up to 50. Devices with the best high temperature performance were made from Si-doped bulk GaAs, using a special double oxide technique for the emitter diffusion. The best of those devices were useful up to 340°C. The yield for these transistors is generally low, probably due to nonuniform doping of the GaAs crystals. The limiting factor for high temperature operation is I_{CEO}, while the current gain for those devices is comparatively temperature independent. One of the basic limitations of NPN transistors is the low-emitter doping, due to the low solubility of donors in GaAs. This prevents use of a higher-doped base layer and causes high-base resistance and sometimes conversion problems of the collector material. This limitation does not hold for PNP devices. Emitter concentrations above $10^{19}cm^{-3}$ are possible. On the other hand, the higher electron mobility favors the injection of electrons, and the shorter diffusion length of holes requires a narrower base for the PNP structure. For comparison of high temperature performance, PNP transistors were built in bulk Cd-doped GaAs. The best had useful characteristics up to temperatures above 400°C.

B. THE FABRICATION OF NPN MESA TRANSISTORS BY STANDARD PROCESS

1. Base Formation

The GaAs mesa transistor was used as a standard device for high temperature tests as shown in Figure 17. The circular emitter has a diameter of 3 mils. The mesa size is 11 mils, and the base contact ring has an inside diameter of 6 mils and an outside diameter of 9.5 mils. Also, a stripe geometry was used often, with a mesa size of 7 X 8 $mils^2$ and an emitter and base contact area of 2 X 4 $mils^2$.

The starting material is N-type epitaxial GaAs with a carrier concentration in the 1 to 5 X 10^{16} cm^{-3} range. The fabrication of this material is described in Section II, paragraph B. The slices are etched in diluted hot NaOCl, followed by a rinse in de-ionized water and methanol. Several slices are placed into a diffusion ampoule together with the dopant, consisting of 0.5 mg of Mg_3Sb_2 and 0.3 mg of As for a 15 cm^3 ampoule. After evacuation to 10^{-5} Torr, the ampoule is heated to 300°C to expel any arsenic oxide (As_2O_3). The diffusion ampoule then is sealed and placed in a diffusion furnace for 75 minutes at 1050°C. To provide a constant temperature zone across the ampoule during diffusion, the ampoule is positioned inside an Inconel plug. This procedure also helps prevent surface erosion due to the condensation of arsenic in colder parts of the ampoule during the cooling cycle.

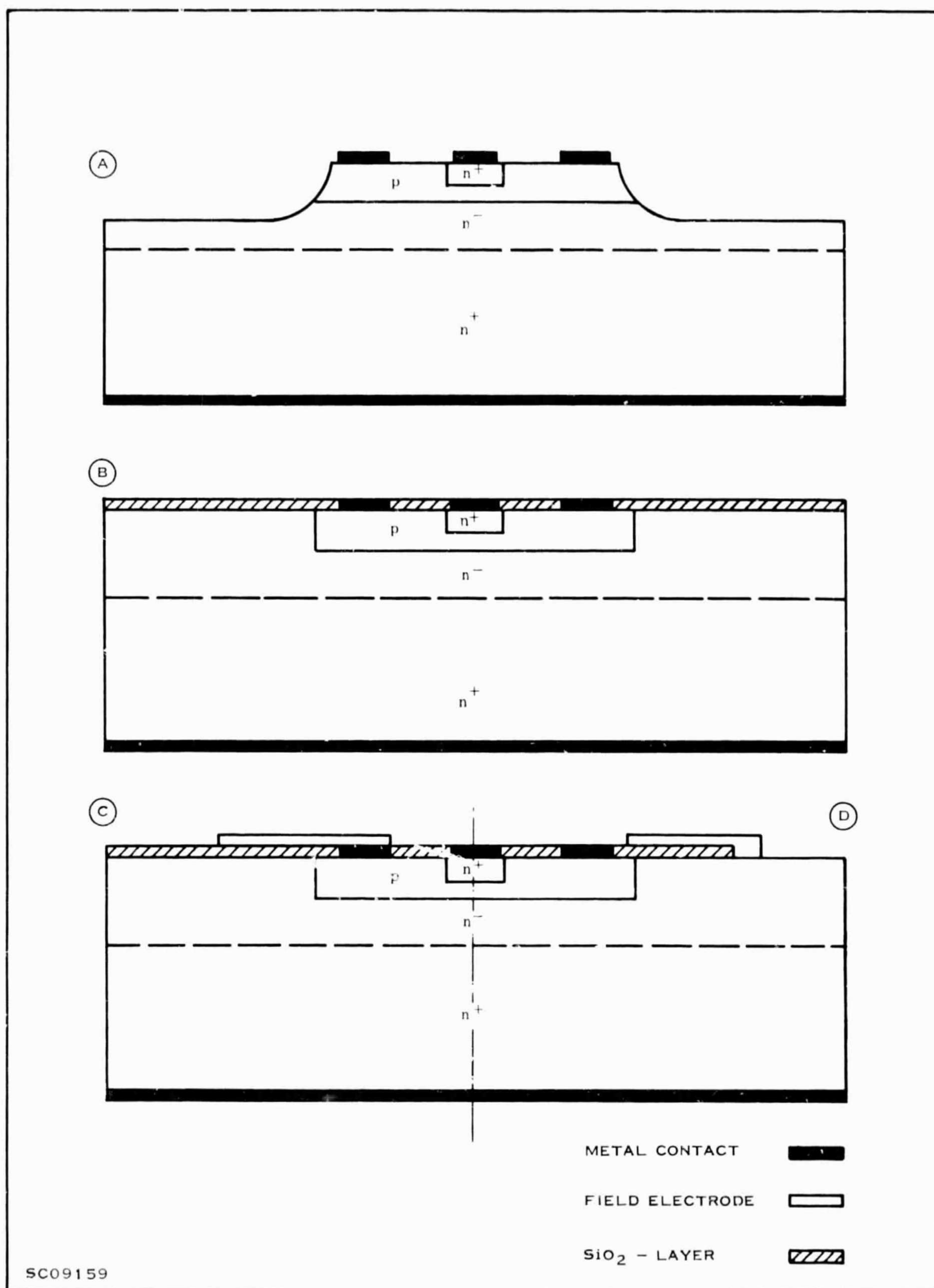

Figure 17. Cross-Section Views of GaAs Transistors

The diffused P-layer, with a thickness of 3 to 4 μm, has to be etched back to a thickness of 1.5 to 2.0 μm and a sheet resistance of 500 $\Omega/\square$. The etching solution consists of 0.7 mole H_2O_2 and 1 mole NaOH. The etch rate of this solution (0.5 μm/minute at room temperature) has been found to be limited by the rate of chemical reaction rather than by the diffusion rate of etchant molecules, yielding a very uniform etching of the whole area of the slice. The remaining thickness of the P-layer is measured by angle-lapping and staining in diluted HNO_3 to which some iron has been added.

2. Emitter Diffusion

The emitter is formed by a planar-diffusion step through holes in a SiO_2 layer. Directly after the etch-back procedure, the slice is cleaned in isopropanol and is placed in the TEOS* reactor at 450°C. At this temperature, oxidation of the TEOS takes place, and the produced SiO_2 is deposited at a rate of 100 Å per minute. The use of O_2 instead of N_2 as carrier gas has the advantage that the reaction temperature can be lowered from 700°C to 450°C. The lower temperature not only prevents any arsenic loss and damage to the GaAs surface, but also makes TEOS layers available for other technological purposes, e.g., covering of already deposited metal layers which would otherwise alloy at higher temperatures.

For the emitter diffusion mask, a layer of 3000 Å SiO_2 is deposited. Then the emitter openings are etched, using standard photolithography. After a short cleaning etch (5 seconds in 8-1-1),** the slice is placed in a quartz ampoule together with 2 mg of Ga_2S_3, 1 mg of Fe, and 5 mg of As for a 15 cm^3 ampoule volume and sealed after heating to 300°C. The emitter diffusion takes place at a temperature of 925°C held for 30 minutes.

3. Metal Contacts

All metal contacts have basically the same structure: Ag (80 percent) and In (10 percent) to which Ge is added as N-type dopant for the emitter contact and Zn is added as P-type dopant for the base contact. After the emitter diffusion, the slice is covered by a photoresist layer with openings somewhat smaller than the emitter diffusion openings. Ag-In-Ge is evaporated over the whole surface while the slice is held at 200°C. Then the photoresist with the excess metal is stripped. After depositing an additional layer of 1500 Å of TEOS over the whole slice to give extra protection to the emitter area, the base contact ring is cut into the SiO_2 layer. Then Ag-In-Zn is evaporated, and the excess metal stripped from the SiO_2. Both contacts are then alloyed simultaneously at [illegible]10°C in a forming gas atmosphere. Finally, all remaining SiO_2 is removed.

---

*Tetraethylorthosilicate

**8-1-1: 8 parts H_2SO_4
1 part H_2O_2
1 part H_2O

4. Final Processing

To form the mesa area, the slice is covered again with a 1500-Å-thick SiO_2 layer. The oxide is removed from all parts other than the mesa area. The mesa etch consists of one part bromine and four parts methanol. Typical etching time is about five seconds. Then the slice is thinned down to a thickness of about 8 mils. After evaporation of an Ag-In-Sn layer onto the back side, the slice is scribed and diced. The single transistor chips are alloyed to the gold-plated headers (TO-18 or TI-Line®) at 610°C in forming gas atmosphere. Connections from the base and emitter contacts to the posts of the header are made in the usual manner using 0.7-mil gold wire. Finally, the header is canned in a dry N_2 atmosphere.

C. SPECIAL FABRICATION RUNS

1. Passivated Transistors (Planar)

The technology described above also applies to the fabrication of planar devices, such as shown in Figure 17 (b through d). The base diffusion condition, the etching back of the base layer, the emitter diffusion, and the preparation of the contacts are the same.

For the fabrication of planar devices, the collector base junction area is not defined by an etching step, but by a diffusion mask during the base diffusion. It is well known that the masking properties of a TEOS layer can be improved by adding phosphorus, forming an SiO_2-P_2O_5 glass. A 2500-Å-thick layer of TEOS plus phosphorus is deposited onto the GaAs wafer after the wafer has been cleaned by a slight etch in hot, diluted NaOCl. The phosphorus is added to the system by passing oxygen through trimethylphosphate and mixing it with the TEOS stream. The reaction temperature is 500°C. Into this layer, base windows 11 mils in diameter are formed by photolithography. Also formed is a 2-mm-wide stripe used to make four-point probe measurements at the edge of the slice. Then the base diffusion is made in the same way as that for the mesa devices. The oxide layer is removed and the slice etched back. The emitter is diffused as described above through a mask of sputtered SiO_2. The sputtered oxide layer serves at the same time as a passivating layer, protecting the junction areas. Sputtered oxide was found to give better I-V characteristics than dielectrics deposited by other means Contact formation is the same as described above.

2. Transistors with Zinc-Doped Base Region

Magnesium as P-type dopant was replaced by an alloy of 0.1 percent zinc in gallium. Twenty-five milligrams of As were added into the diffusion ampoule. The ampoule was heated to 300°C before being sealed off to evaporate the arsenic oxide. The diffusion resulted in a 3.5 μm thick P-layer in the 5×10^{15} cm^{-3} doped epitaxial layer. The layer was then etched back to 0-2 μm. This thickness variation was introduced intentionally in order to obtain devices of different base thicknesses on the same slice. For the emitter, the standard process with Ga_2S_3 plus Fe + As was used. Transistors with a current gain of up to 100 were obtained. The temperature dependence of the current gain resembled that of Mg-diffused base devices.

3. Transistors with Zinc Added to the Emitter

To support the effect of iron, which is added to reduce the temperature sensitivity of the transistors, zinc was added to the emitter dopant. After a standard Mg base diffusion and etch back, the emitter was diffused using Ga_2S_3, Fe, As and 0.05 mg of an alloy consisting of Ga plus 0.1 percent zinc.

4. Experiments Using Si-Doped Bulk GaAs Slices and Double Oxide Techniques

GaAs transistors were fabricated using bulk Si-doped starting material. To evaluate the influence of the type of oxide mask used during the emitter diffusion, different kinds of oxide combinations were tried. To simplify the comparison, bulk GaAs Si-doped to about 3×10^{16} cm^{-3}, grown in a sealed crystal puller, was used.* After the magnesium diffusion and etchback to 2 μm, the following oxides were deposited on four separate samples:

a) 1000 Å of sputtered SiO_2, followed by 3000 Å of TEOS,

b) 1000 Å of sputtered SiO_2, followed by 3000 Å of phosphorous-doped TEOS,

c) 3000 Å of TEOS doped with phosphorous,

d) 3000 Å of TEOS.

The standard emitter diffusion process with Ga_2S_3, Fe, and As was employed. Transistors were obtained from runs 1, 2, and 3. The room temperature current gain was approximately 40 for run 2 and somewhat smaller (approximately 15) for runs 1 and 3. Devices from run 1 showed the smallest temperature dependence of current gain and of I_{CEO}. They were useful up to a temperature of 340°C. Due to problems described in Section II, paragraph D, the fabrication yield of these devices was low.

5. Experiments with S Plus Cd-Doped Epitaxial Layers

The temperature dependence of transistors built under contract AFAL-TR-66-361 was weaker than experienced with recently fabricated devices. For comparison, experiments were performed with epitaxial slices grown under the former contract, employing the present standard fabrication process. The yield of these experiments was generally low. The performance of the devices, however, resembled that of transistors built under the former contract.

Because it was thought possible that epitaxial slices which yielded high temperature transistors had a high background of cadmium doping, slices intentionally Cd-doped were prepared. Transistor fabrication runs using standard mesa process as well as double oxide technique, resulted in transistors showing medium current gain and strong temperature dependence.

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*Source: Bell & Howell, Pasadena, California

6. Fabrication of PNP Transistors

Experiments with bulk P-type GaAs were performed with slices from two different crystals. Slices from the first crystal with a cadmium concentration of 10^{17} cm^{-3} were base diffused at 925°C for 2 hours. The dopant consisted of 2 mg Ga_2S_3, 5 mg As and 1 mg Fe. The resulting N-layer was 2 μ thick. Without any etchback a layer of sputtered SiO_2 (1000 Å) and phosphorus-doped TEOS oxide (3000 Å) was deposited and the emitter windows were cut. For the emitter formation the slices were diffused for 30 minutes at 625°C with 1 mg zinc and 1 mg As in the ampoule. After applying Ag-In-Sn and Ag-In-Zn contacts for base and emitter respectively, mesas were etched. The devices showed first a leaky emitter-base junction due to a thin P-channel at the surface, probably caused by small amounts of zinc diffused through the oxide. After a cleaning etch in $NH_4OH + H_2O_2$, devices had good junction characteristics and current gain. Devices from this run had the best high temperature performance of any devices built under this contract.

The second crystal had a Cd-doping level of about 5 × 10^{16} cm^{-3}. In one experiment we fabricated devices which were diffused under identical conditions but had a different base width. Ten slices were base diffused together. Then they were etched back to a different amount for each slice and finally emitter diffused together. The diffusion conditions were the same as mentioned above. The current gain ranged from 10^{-2} for devices with the thickest base layers up to 300 for thin base layers. The devices were temperature sensitive however, as will be reported in Section V, paragraph C.

D. FABRICATION OF DIODES

1. Diodes in P-Type GaAs

Chips with several diodes diffused into P-type GaAs are required in the logic gate. Bulk crystal slices, doped in the high 10^{16} cm^{-3} range were planar diffused, similar to the standard emitter process. Different diffusion times were tried. After completing the diodes, the SiO_2 layer serving as a diffusion mask was etched off in some cases for comparison of the electrical performance of the devices. It was found that diodes diffused for 3 hours at 925°C and passivated with an oxide mask gave lowest leakage currents. For a 4.5 mil^2 diode, the leakage current at 1 volt was below 10^{-11} A. After the device was heated to 280°C, the 25°C leakage current was still about 10^{-11}A.

2. Diodes in N-Type GaAs

Diodes were fabricated in epitaxial and bulk GaAs doped with Si, Te, Sn or S by diffusing Mg, Zn, or Cd. The doping level of the starting material ranged from 10^{15} cm^{-3} to 10^{18} cm^{-3}. For the Mg diffusion, the slices were heated to 1050°C for 1 hour with 0.5 mg Mg and 0.5 mg As in a 15-cc quartz ampoule. Zinc was diffused at 650°C for 45 minutes with 3 mg Zn and 1 mg As in the ampoule. Cadmium was diffused at 1050°C for 40 minutes with 5 mg Cd and 1 mg As as dopant. Some planar diodes were built using the combination of 1000 Å sputtered SiO_2 plus 3000 Å of TEOS-oxide. For the ohmic contacts to the P-layer, Ag-In-Zn (80-10-10) was used. Before being canned, the mesa diodes were cleaned and etched in 1% bromine-methanol.

E. FIELD EFFECT TRANSISTORS

GaAs bipolar transistors can be expected to be more temperature sensitive than field effect transistors. For comparison GaAs field-effect transistors were built. Due to a relatively uncomplicated technology, the Schottky-barrier-gate approach was chosen. Figure 18 shows the geometry of the device. The fabrication process was as follows:

The epitaxial layer was grown in the reactor normally used for bipolar transistor slices. The substrate was (100) oriented, chromium-doped, semi-insulating GaAs. The epitaxial layer was Sn-doped ($\sim 3 \times 10^{15}$ cm^{-3}) and about 1 μm thick, as found by angle lapping and staining. The doping level of the grown layer was estimated from a two-point probe breakdown voltage reading, and calculated later from data of the completed devices and from Hall measurements.

After a short cleaning etch in 8-1-1, EDTA* and HF, Ag-Zn-Ge (80-10-10) was evaporated over the whole slice. Source and drain areas were defined by etching the excess metal, and the contacts were then alloyed at 610°C in forming gas. The complete slice was then covered by a ~ 3000 Å thick layer of SiO_2 deposited by low temperature oxidative decomposition of TEOS. After

*Ethylenediaminetetraacedic Acid

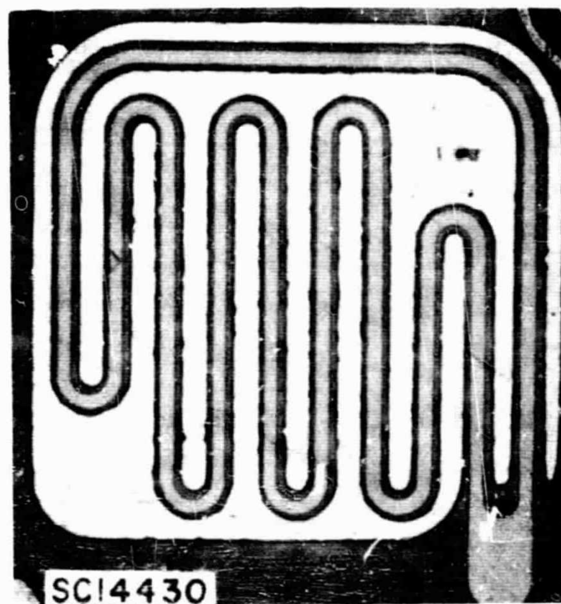

Figure 18. GaAs FET Structure (Gate Length 10 μm, Length to Width Ratio 275)

removing the oxide and the epitaxial layer outside the active device area by a KMER and etching step, the gate area was opened. Then the exposed GaAs surface was cleaned with EDTA, and Mo-Au evaporated over the whole slice. After stripping the excess Mo-Au and opening the SiO_2 at the bonding areas, the slice was lapped to a thickness suitable for easy scribing and breaking. The chips were mounted on TO-18 headers or in high frequency TI-Line® microwave packages and were canned under dry nitrogen gas.

SECTION V

DEVICE MEASUREMENTS

A. REVERSE LEAKAGE CURRENTS

1. Transistor Junctions

The reverse collector-base leakage current of an NPN GaAs transistor is shown in Figure 19. It can be seen that at low reverse bias the leakage current increases rapidly, while at higher bias (for not too high temperatures) the leakage current does not change much with temperature. This weak temperature dependence suggests some sort of tunnel current. At present there is no theory that describes quantitatively the leakage current in GaAs in any temperature range. We have considered internal field emission as a possible explanation for the excess leakage current. The simplest functional dependence of field emission current on bias is given by Chynoweth:[25]

$$I_o = K'(V_i - V_a) \exp\left(\frac{-B}{E}\right) \tag{20}$$

where

V_i = the built-in voltage

V_a = the applied voltage, and

E = the electric field of the P-N junction

B includes the constants of the semiconductor:

$$B = \frac{\pi (m_{eff})^{1/2}\, Eg^{3/2}}{2\sqrt{2}\, q\, \hbar} \tag{21}$$

where

m_{eff} = the effective mass

Eg = the bandgap

q = the electron charge, and

$\hbar$ = the Planck-constant divided by 2π

Using GaAs data and $1/m_{eff} = 1/m_{hole} + 1/m_{electron}$, one can calculate $B = 1.7 \cdot 10^7$ V/cm.

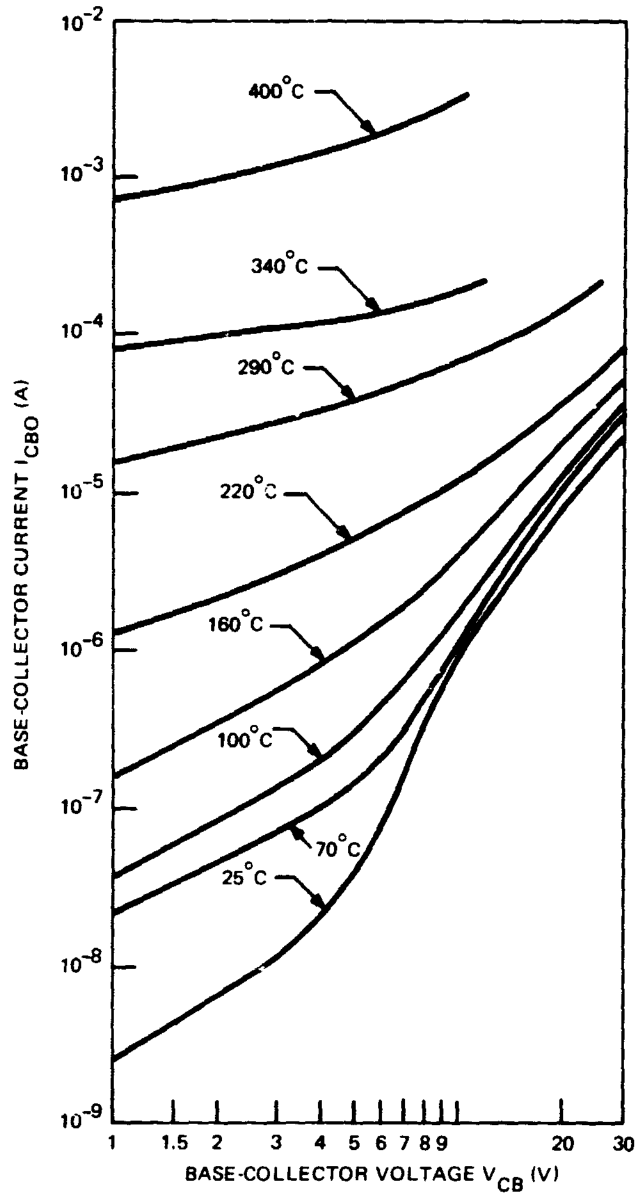

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Figure 19. Reverse Collector-Base Junction Characteristics of a NPN Transistor at Various Temperatures (Junction Area 90 mil^2)

Moll[26] has derived an expression of the tunnel current density under reverse bias conditions for direct bandgap materials such as GaAs:

$$j = K V_a E \exp\left(\frac{-B}{E}\right) \quad (22)$$

In this equation the constant B is the same as in Chynoweth's equation. The major difference is the product of the applied voltage times electric field in front of the exponential function. We have tried both Equations (21) and (22) to explain the reverse leakage currents. To obtain the junction field the capacitance C' per unit junction area was measured as a function of the voltage. Finding the junctions to be graded, the maximum electric field,

$$E_{max} = \frac{3}{2} \frac{(V_i - V_a) C'}{\epsilon} \quad ; \; C = C' \times \text{Area} \quad (23)$$

was used for the electric field in Equations (22) and (23) ($\epsilon = 10^{-10}$ F/m).

A plot of $\ln I/(V_i-V_a)$ versus $1/(V_i-V_a)C$, or in the case of Equation (22), a plot of $\ln I/V_a(V_i-V_a)C$ versus $1/(V_i-V_a)C$ should give a straight line.

A plot of the data of Figure 19 for 25°C using Equation (20) results in a straight line for higher voltages with a slope corresponding to $B = 2.5 \cdot 10^5$ V/cm. The discrepancy can be explained in the following ways:

First, in calculating the electric field the area of the junction was used, thus giving an average field. In our model, we assume that the current is a consequence of localized high field regions, so that the actual field can be much larger.

Second, according to Franz,[27] an equation with the same exponential dependence like Equation (20) is obtained if one considers not interband tunneling but tunneling from impurity levels into the conduction band. In this case, the bandgap is replaced by the activation energy of the impurity. Both effects can be sufficiently large to explain the discrepancy.

It is of interest to point out one other property of this junction. Since due to the lower value of B a tunnel mechanism dominates already at relatively low voltages and the resulting current might originate in small areas close to the surface, no appreciable multiplication of field generated carriers is expected. Measurements of the multiplication factor, defined as the photocurrent at a given bias divided by the photocurrent in the bias independent voltage region, yielded a multiplication factor between 1 and 2 even in the breakdown region.

At low voltages, we find that the current is due to other mechanisms. The current increases rapidly with temperature. A plot of the logarithm of the current at constant voltage versus the reciprocal temperature yields an activation energy close to the half bandgap of GaAs.

During heat treatment at 400°C, the junction degrades. We find that the constant B has not changed. The factor A, however, has increased by about one order of magnitude. This means that the mechanism by which the carriers are produced stays the same; however, the number of centers participating in the internal field emission has increased. We believe that all of the current in the temperature range where field emission dominates, originates at the surface. Etching the surface reduced the leakage current to about the starting value prior to the heat treatment.

We conclude that the leakage current at high bias and low temperatures is caused by field emission at the periphery of the junction. At high temperatures and low bias, the current is a result of bulk generation current via levels in the forbidden gap. At medium temperature and medium bias, the current results from a combination of both processes and is hard to predict in detail.

2. Diffused Diode Junctions

As will be shown in Section V, paragraph B the emitter-collector leakage current limits the high temperature application. Only in devices with exceptionally high room temperature common-emitter current gain, h_{FE}, a decrease in current gain plays the dominant role. To compare the leakage current behavior of transistors with that of diodes, mesa and planar diodes were diffused into different N-type GaAs, as discussed in Section IV, paragraph D2.

In Figure 20 the leakage current at 2 volts reverse bias is given as a function of the reciprocal temperature for different diodes. The lowest 400°C leakage current was obtained from zinc-diffused planar diodes built into epitaxial GaAs doped with sulfur to 10^{16} cm^{-3}. These diodes had at 400°C a leakage current of 10^{-4} A at 2 volts reverse bias. This corresponded to a leakage current density of 0.2 A/cm^2. However, a direct relationship between the area of the diodes and the leakage current did not hold. Many diodes exhibited a linear relationship between the leakage current and the reciprocal temperatures and in the first approximation an activation energy corresponding to one-half the bandwidth of GaAs is calculated from the slope of the straight line. This is similar to results obtained for the base-collector leakage currents of transistors discussed in the preceding paragraph. The similarity of the temperature dependence between diode and transistor junctions indicated that the emitter diffusion had no deleterious effect on the high temperature performance of the collector-base junction for transistors.

3. Solution-Grown Junction

Since work on solution-grown amphoterically doped P-N junctions showed that these diodes have properties different from those of other GaAs P-N junctions, the reverse leakage currents of solution-grown junctions were studied. The technique for fabricating these junctions is described in Section II.

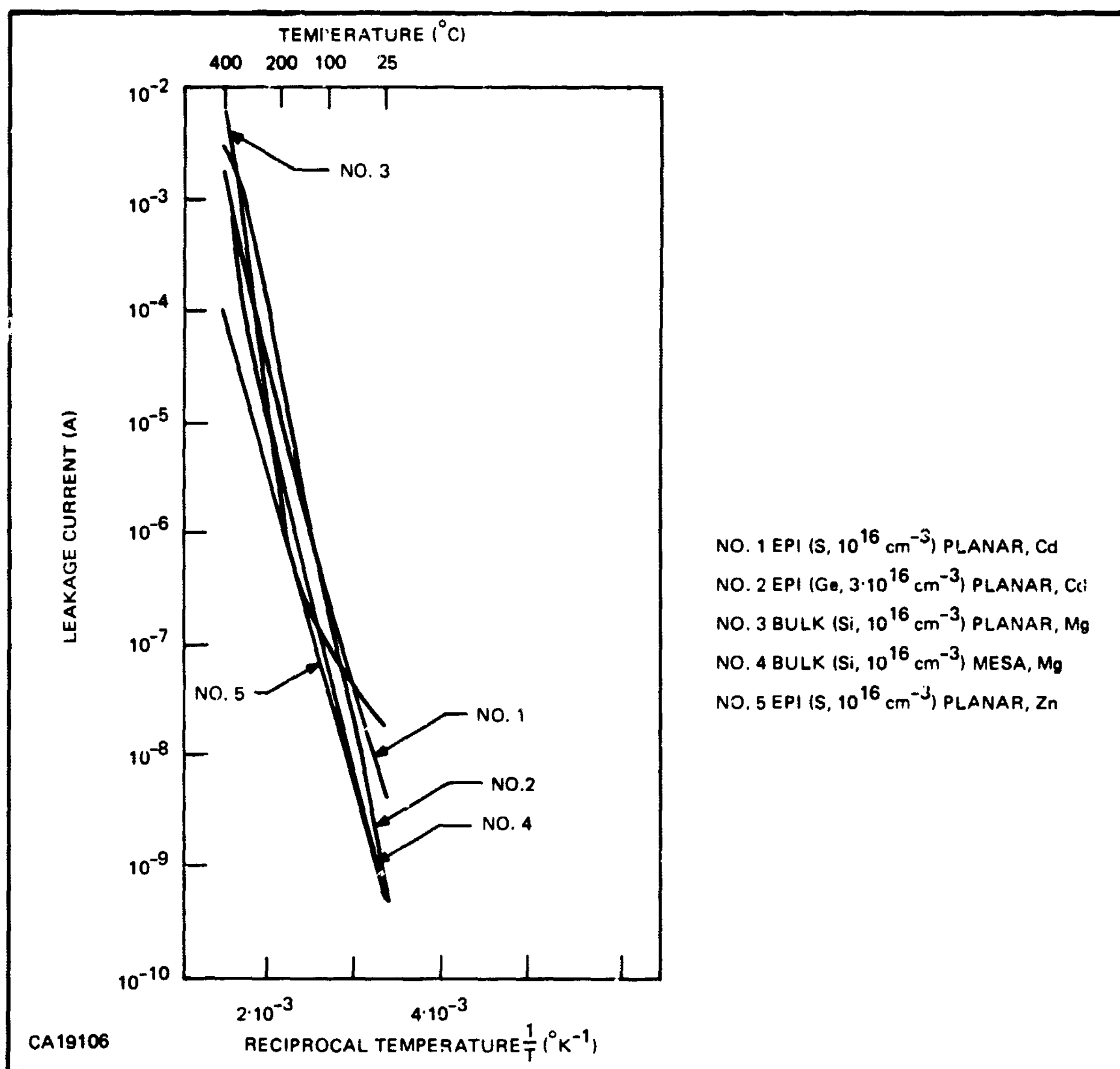


Figure 20. Reverse Leakage Current of Various Diodes versus Reciprocal Temperature (Junction Area 78 mils^2)

In Figure 21 the reverse-leakage current I_R of a solution-grown diode is plotted versus the reverse bias for various temperatures before and after degradation. The leakage current at room temperature is too low to be measured with the present equipment. A plot of $\ln I_R/T^{3/2}$ versus the reciprocal temperature yields an activation energy of 0.72 eV. The bandgap at 0°K is 1.53 eV, so that the current generation centers responsible for the leakage current appear close to mid-band. Extrapolation to 400°C shows that the leakage current is 140 μA for a diode area of 2.9×10^{-4} cm^{-2}. Extrapolation to low temperatures yields a leakage current of 10^{-11} A at 25°C. All measurements were made at - 1V. The leakage current, particularly at the higher temperatures, increases as $V^{1/n}$ where $2 < n < 3$ as predicted by Sah et al.[28] The breakdown of these diodes is not due to internal field emission (Zener breakdown) but to an avalanche process. Solution-grown

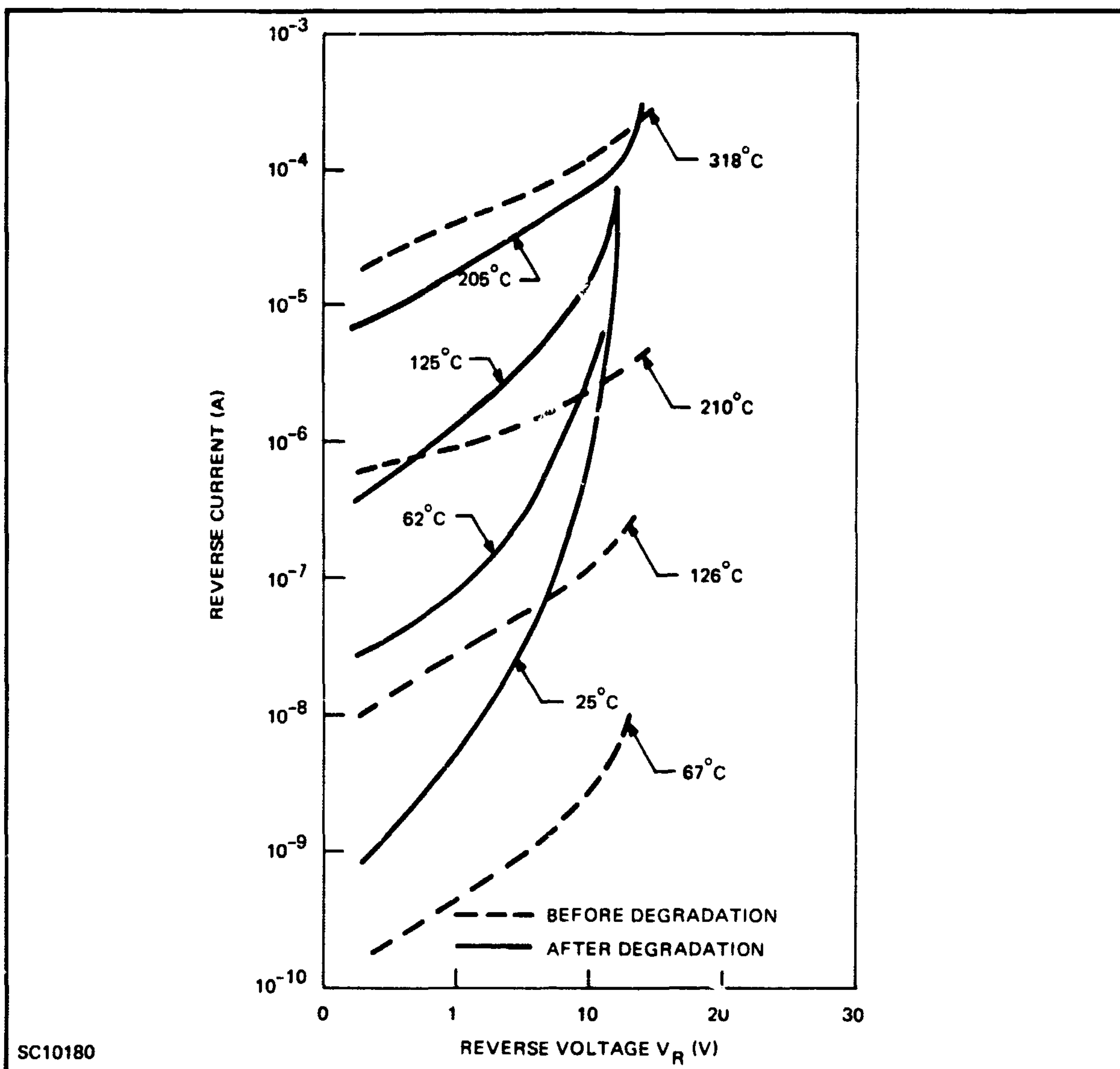


Figure 21. Reverse Leakage Current of a Solution-Grown Junction as a Function of Bias (Before and After Heat Treatment)

diodes yielded multiplication factors of M = 20, as shown in Figure 22, where 1/M is plotted versus reverse bias. As predicted by Shockley,[29] 1/M extrapolates linearly to the breakdown voltage of 29.5 V. The ionization coefficient α was calculated from

$$\alpha = \frac{1-\frac{1}{M}}{0.4W} \tag{24}$$

where the space charge width W is obtained from capacitance measurements. At the highest voltage measured (28.5 V), the ionization coefficient was 2.65×10^4 cm^{-1}. In Figure 23 the quantity

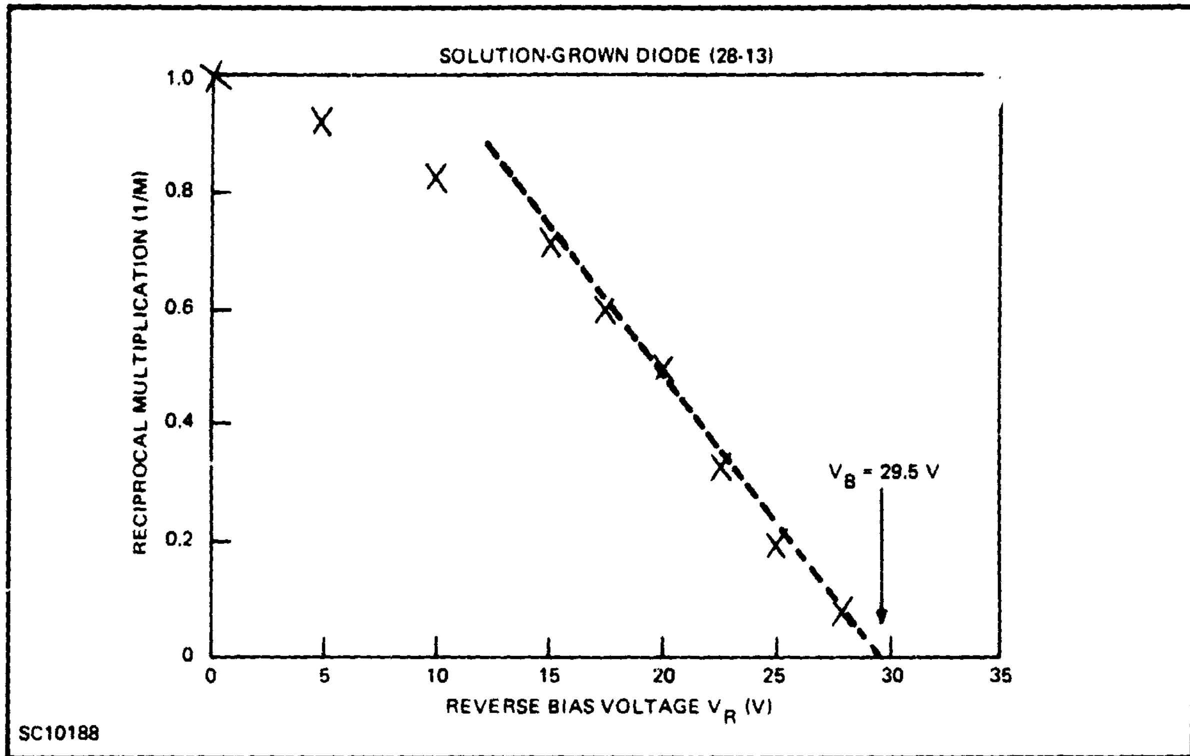


Figure 22. Reciprocal Multiplication as a Function of the Reverse Bias for a Solution-Grown Diode

α/E_{max} is plotted semilogarithmically versus $1/E_{max}$ giving a straight line, as predicted by Shockley's theory. Here E_{max} is the maximum junction field,

$$E_{max} = 1.5 \frac{-V_a + V_i}{W} \tag{25}$$

where V_i is the built-in voltage and V_a is the reverse bias. The factor 1.5 applies since capacitance measurements show that the junction is graded and not a step-junction. The impurity gradient was found to be 3.6×10^{21} cm^{-4}, and $V_i = 1.27$ V. Also shown in Figure 22 is a plot that shows ln α as function of $1/E^2$ max. This plot should give a straight line if Wolff's[30] theory applies. Obviously the experimental results speak for Shockley's theory. Earlier work of Logan et al.[31] had yielded evidence that Wolff's theory would apply for GaAs P-N junctions.

All measurements made so far on solution-grown diodes show that solution-grown GaAs P-N junctions follow laws and equations derived from silicon diodes. This applies also to studies of the forward characteristics. A value of n between 1.5 and 2 in the exponent of the diode equation

$$I = I_o \exp \frac{V}{nkT} \tag{26}$$

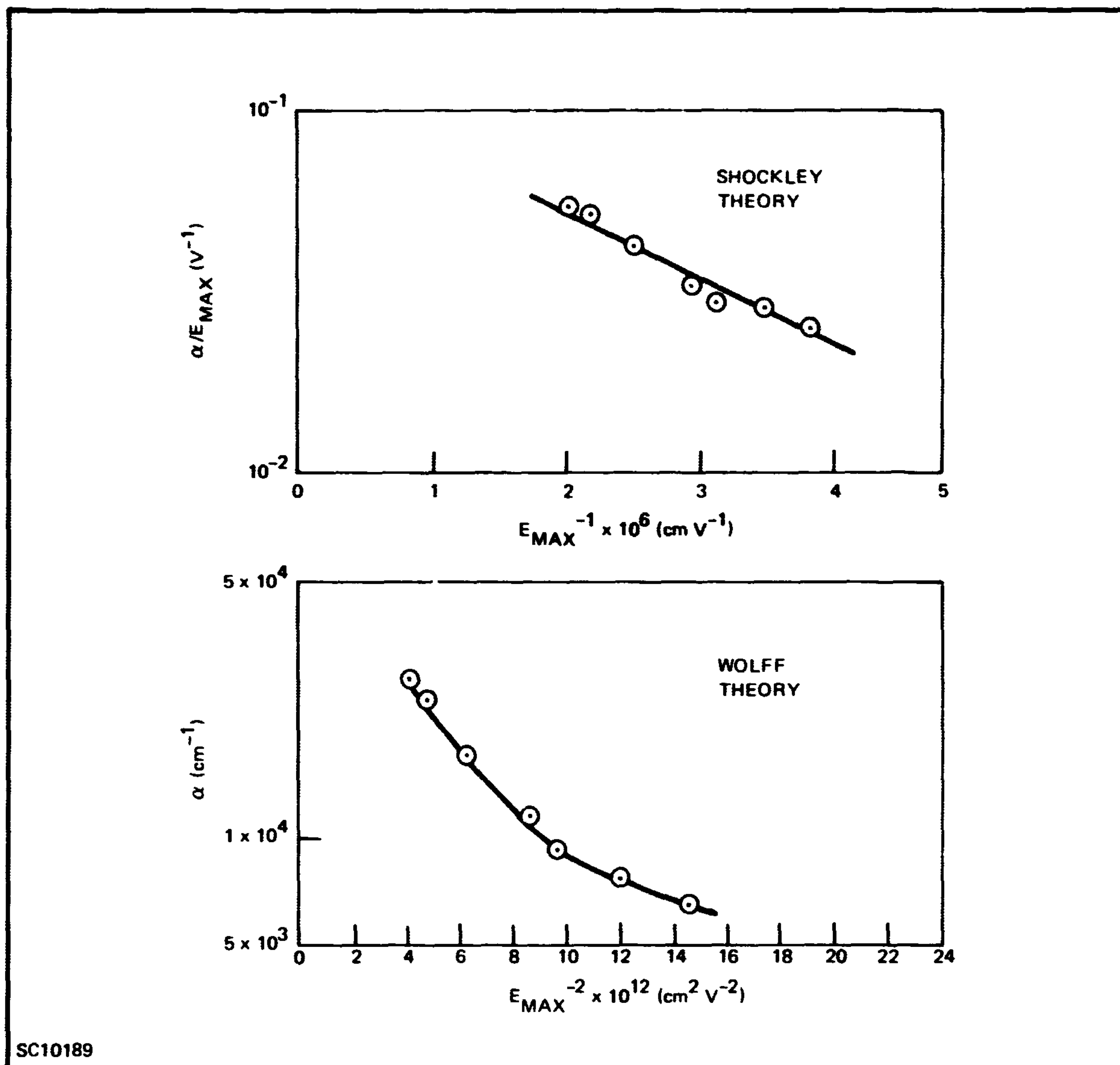


Figure 23. Ionization Coefficient for GaAs as a Function of the Electron Field According to Shockley's and Wolff's Theory

was found between 77° and 25°C. Generally, GaAs diodes exhibit much larger apparent values for n, due to contributions from temperature-insensitive tunnel currents. In the sense that silicon diodes can be considered as "normal", solution-grown GaAs diodes were the first observed that behaved normally.

While solution-grown diodes, as grown, behave normally, the degradation mechanism seems to be similar to that found in other diodes. In Figure 21, the leakage current (solid lines) is shown after heat treatment. The leakage current has increased by two orders of magnitude and is strongly bias dependent. In Figure 24 the reverse leakage current, "after degradation" (i.e., after heating the diode to 318°C when the first data were taken), were plotted according to Equation (22),

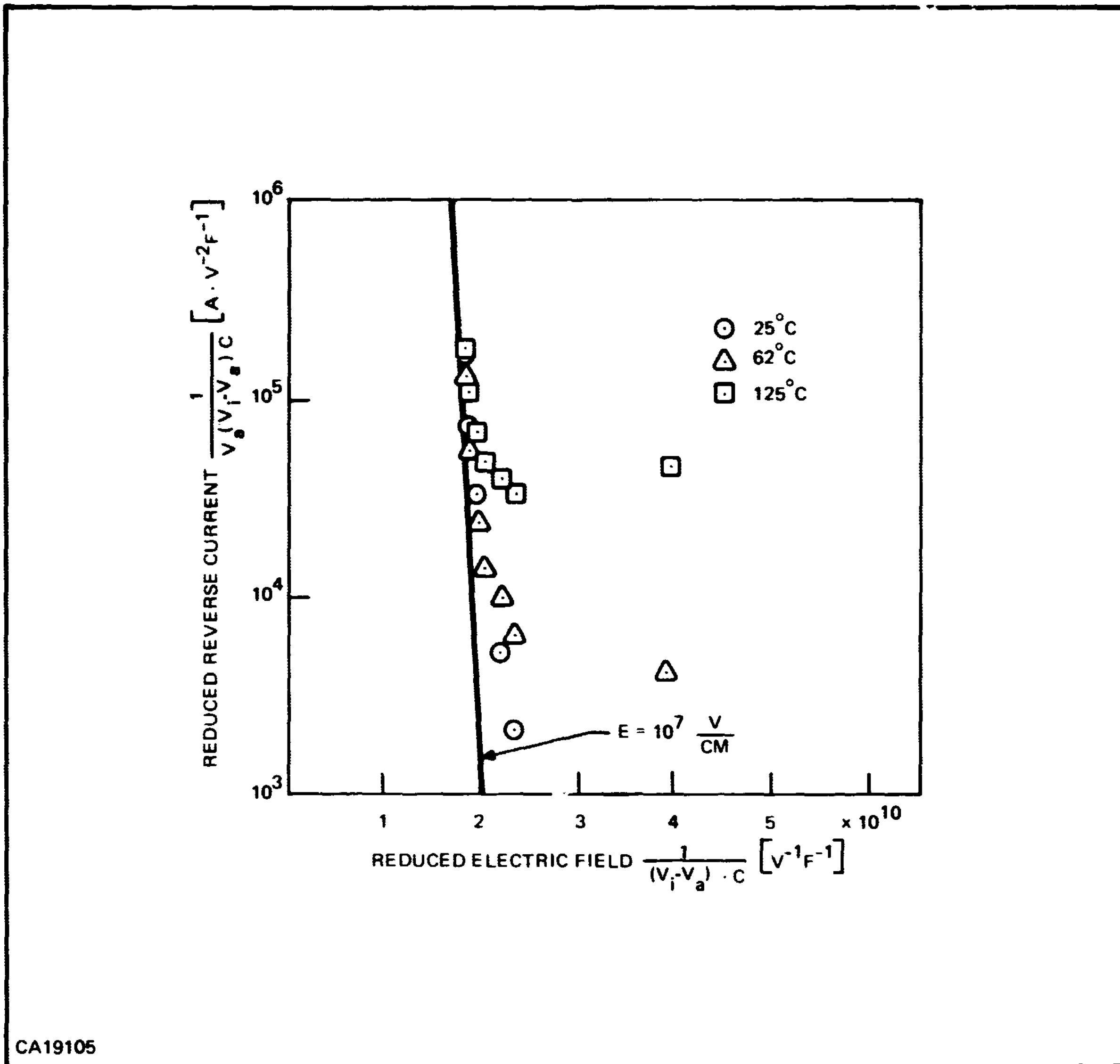


Figure 24. Reduced Reverse Current as a Function of the Reduced Electron Field for a Solution-Grown Diode

$$\text{i.e.,} \quad \frac{I}{V_a\,(V_i - V_a)C} \quad \text{versus} \quad \frac{1}{(V_i - V_a)C} \tag{26a}$$

For higher voltages the reduced current at 25°C, 62°C and 125°C approached a straight line with a slope corresponding to $B = 10^7$ V/cm. Considering the accuracy of the data, the agreement with the theoretical value of $1.7 \cdot 10^7$ V/cm is very good. This is in contradiction to results obtained with diffused P-N junctions, where we found the value for B about a factor of 1/70 too low. The fact that the breakdown can be described by Equation (22) means that most of the current is due to

tunneling from the valence band to the conduction band. Since the field measurements are based on measurements of the capacitance-per-unit junction area, the results further mean that the total junction area participates in this conduction mechanism rather than the periphery area only, as was concluded from measurements on diffused junctions in vapor phase epitaxial material. Etching of the surface is therefore not expected to reduce the leakage current in degraded solution-grown diodes. This conclusion has been supported by experiments. One explanation for the increase of leakage current is that metallic precipitations were introduced–probably along dislocation lines during the aging process. At low bias and high temperature, this current is mostly due to space-charge generation of the type already present before degradation. Though this current also increased, the relative increase of the leakage current was less at higher temperatures than at lower temperatures and also less at lower voltages than at higher voltages. For use as high temperature diodes, the solution-grown amphoterically Si-doped diodes did not offer an advantage compared to diffused diodes because of the instability of the leakage current.

B. DC CHARACTERISTICS OF NPN TRANSISTORS

In this section, we will compare the dc characteristics at different temperatures of transistors fabricated from different GaAs materials, epitaxial slices and bulk slices, using different technologies, as described in the device fabrication section. A few transistors fabricated under contract AFAL-TR-66-361 (AFAL Devices) were still available, and were evaluated for comparison with recently built devices. It appears to be difficult to combine good 25°C performance, that is, high current gain and low saturation voltage, with weak temperature dependence. The devices also differ in the current dependence of the current gain.

Let us consider first the transistor characteristics of a device with high h_{FE} at 25°C. Figure 25 shows the current gain versus collector current for different temperatures. This device was made by the standard mesa process, using a Sn-doped epitaxial layer. Table III summarizes typical values for these transistors.

The devices had current gain down to the nA region. The current gain increases as the square root of collector current, as predicted for a transistor which has in addition to the diffusion current component a recombination current component proportional to exp (qV/2kT). The current gain levels off at values in the order of 100 at 1 mA. The reverse current gain increased from 1 at 10 nA to 17 at 0.2 mA also following a square root dependence. In Figure 26, the current gain of different transistors is plotted versus the reciprocal temperature. Device Y-7-2 is the device being discussed now. This current gain exhibits an activation energy of 0.2 eV. Since the reverse current gain followed the same activiation energy, it was concluded that the properties of the base region are changing with temperature rather than the emitter properties. Since the current gain is proportional to the square of the diffusion length, and the diffusion coefficient does not have an exponential temperature dependence, the lifetime seems to decrease with increasing temperature with an activation energy of 0.2 eV. Strong temperature dependence of the current gain is observed even at the lowest current levels. At very low currents, the Fermi level for the electrons is close to that of the holes. The recombination cross section for electrons is dominated by deeper-lying levels only if the base region is heavily compensated. One of the possibilities for base region compensation is the presence of oxygen.[32,33] It is possible that the advantageous effect of iron, on frequency performance and temperature stability, is due to a compensation of oxygen. Sulfur from the emitter diffusion also has a compensating effect on the base region.

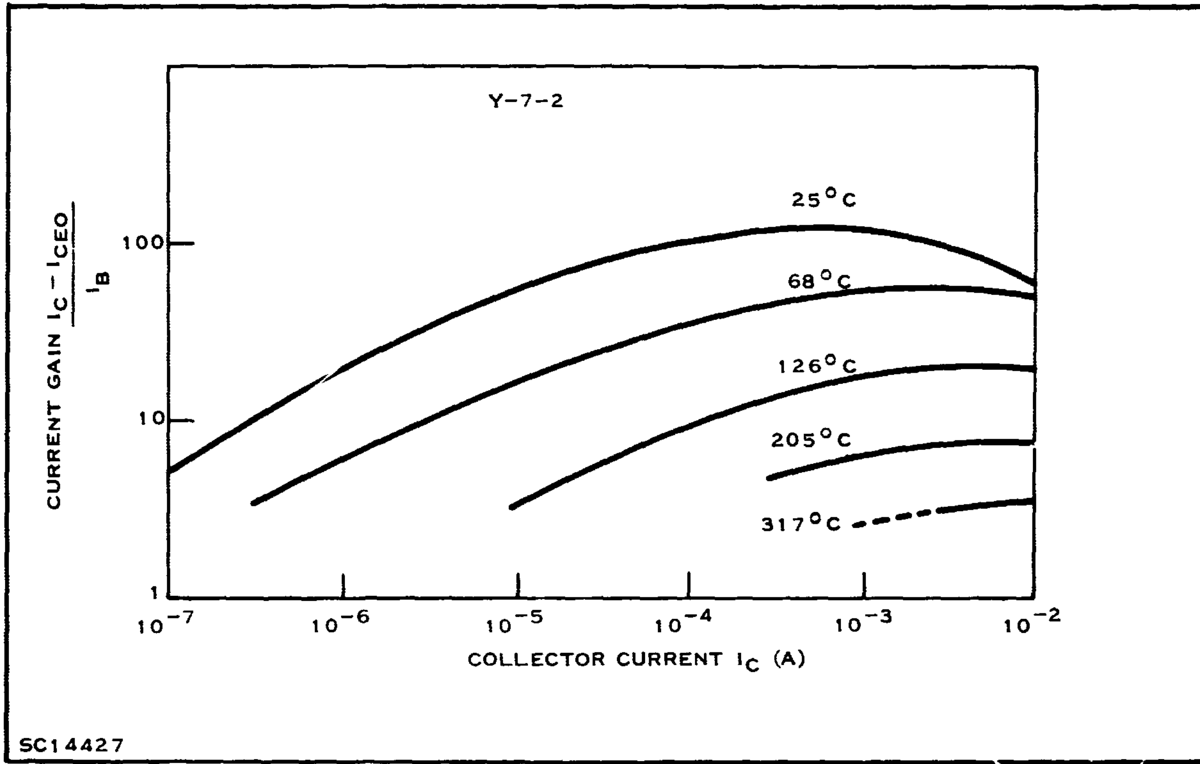


Figure 25. Current Gain versus Collector Current of a NPN GaAs Transistor at Various Temperatures

Table III. Typical dc Characteristics of Good 25°C - GaAs Transistors

h_{fe}	30 to 75
BV_{CBO}	70 to 100 V
BV_{EBO}	10 to 14 V
BV_{CEO}	50 to 100 V
R_{SE}	5 to 10Ω
$V_{CE(sat)}$ at 5 mA	0.15 to 0.25 V
C_{cb}	1.4 to 1.7 pF
C_{eb}	0.7 to 0.8 pF

Direct evidence that the strong temperature dependence is connected with the degree of compensation is found by comparing transistors fabricated on tin-doped and on sulfur-doped epitaxial material. In Figure 26, all devices, except those fabricated on Sn-doped epitaxial layers, show that the temperature dependence is determined by the 0.2 eV level only at higher temperatures. The difference between the transistors is that after etchback of the base layer to the required 2 μm thickness, the sheet resistance was in the order 700 Ω/□ for the tin-doped layers, and as low as 250 Ω/□ for the other material. The likely explanation is that such behavior is due to the amphoteric nature of tin. Combining the charge-balance equation and the equation describing the distribution of tin atoms between acceptor and donor sites, one finds that diffusion of an acceptor such as Mg forces tin atoms into donor sites. Thus, a compensating effect can be expected for

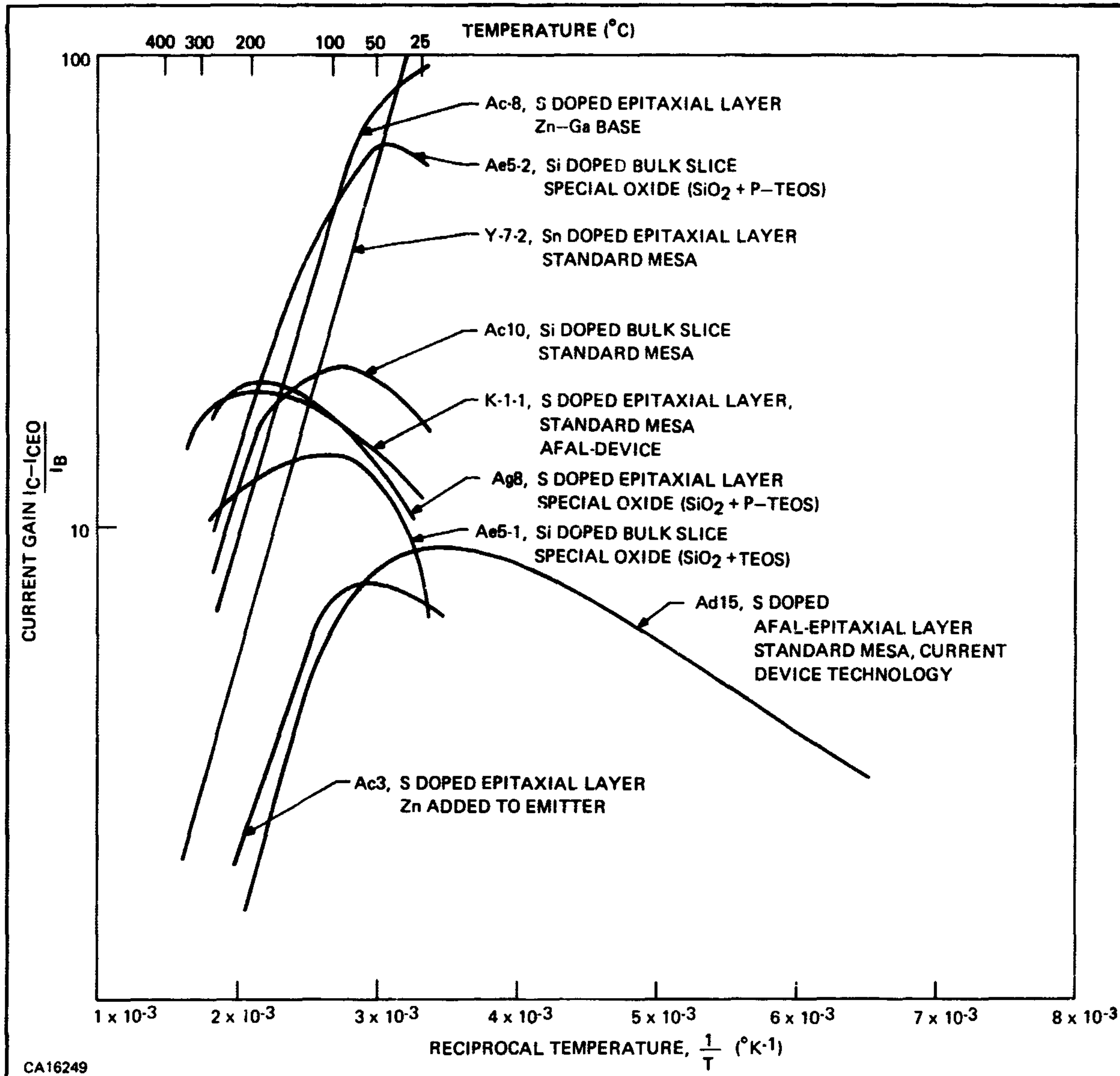


Figure 26. Current Gain versus Reciprocal Temperature of Various NPN GaAs Transistors Using Different Crystal Materials and Technologies

Group IV elements but not for Group VI elements. The assumption is made in this explanation that the P-layer is extrinsic to begin with at the diffusion temperature. The intrinsic carrier concentration at 1050°C is 8×10^{16} cm^{-3}, while the surface concentration of Mg is about 3×10^{17} cm^{-3} after etchback. Therefore, we can expect partial compensation of the base layer.

Next we will discuss the performance of AFAL-transistors fabricated by the standard mesa process. Current gain versus reciprocal temperature for such a device (No. K-1-1) is shown in Figure 26. With rising temperature the current gain increases to a maximum value at about 190°C. Above 190°C, the gain decreases and approaches the same slope as all other devices, i.e., an activation energy of 0.2 eV.

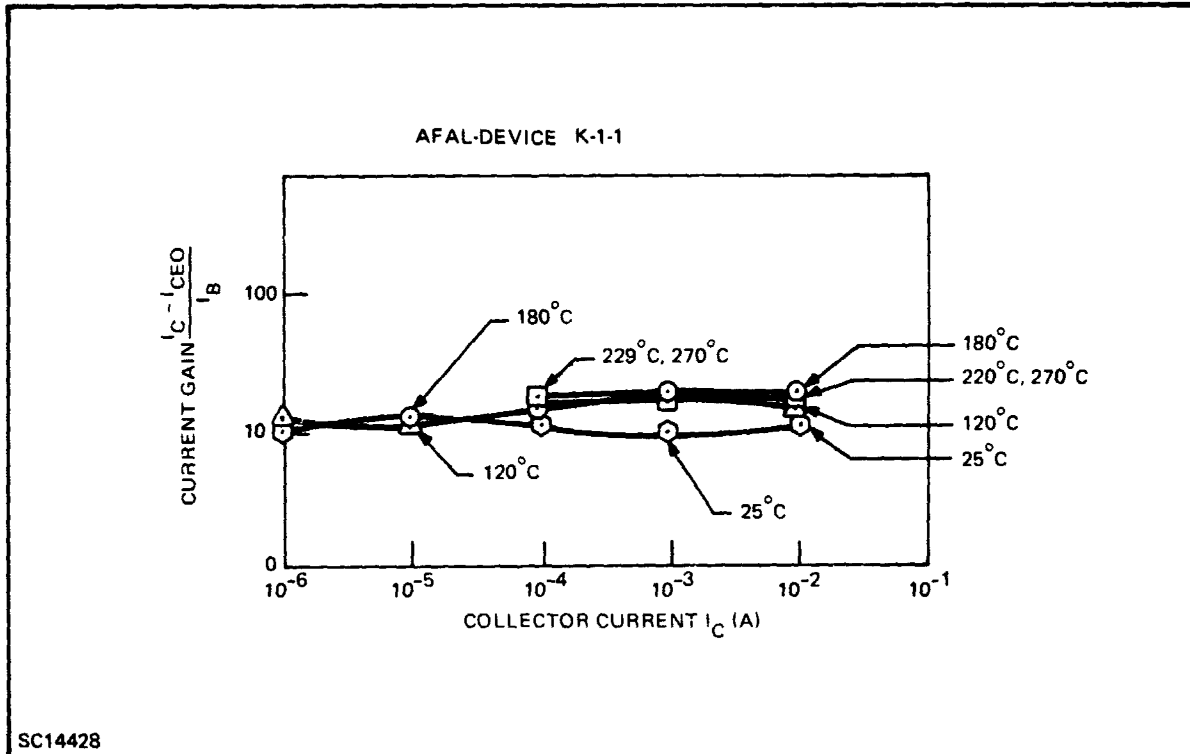


Figure 27. Current Gain versus Collector Current of a NPN GaAs Transistor (AFAL-DEVICE)

In Figure 27, the current gain for this device is shown as a function of current for various temperatures. It can be seen that the current gain is relatively independent of both current and temperature. The absolute value of current gain is low, in the range of 10 to 20. The fact, that the current gain does not decrease at higher currents (caused by conductivity modulation) and is typically lower than in devices such as represented in Figure 25, indicates that the base region is more heavily doped. As suggested earlier, cadmium background doping might be responsible for the higher temperature stability of transistors built on this material. This observation certainly could tie in with the previously mentioned findings. Also, the fact that iron doping improves the temperature stability in certain types of materials is in agreement. As already mentioned, the reverse current gain follows the same square-root relationship of the collector current. Furthermore, the temperature dependence of the reverse current gain is very similar to the forward current gain. These are indications that the P-region is the determining element. Experiments on silicon devices[34] have shown that the exponential increase of current gain with reciprocal temperature is related to an increase in emitter efficiency. In this case, the bandgap on the heavily doped emitter side is smaller than the bandgap on the P-region, and the forward current gain can be shown to increase in the observed way. Since the low-doped collector does not exhibit any bandgap shrinkage effect, the reverse gain of silicon transistors is relatively temperature-insensitive. N-type GaAs generally has a higher bandgap than P-type GaAs because of the overlap of the acceptor impurity band and the valence band. This could qualitatively explain why both the forward and the reverse current gain decrease with temperature. Quantitatively, the concentration of the acceptors in the base regions is not high enough and the activation energy is too high to explain the decrease in current gain due to a decrease of the emitter efficiency.

There is another reason for ruling an emitter efficiency influence. A detailed study of the data presented in Figure 25 shows that the current gain decreases with about the same activation energy, even at very low currents. In this range, the current gain increases roughly as the square root of the collector current, indicating that a 2 kT current is responsible for the drop-off of the gain. Let it be assumed that the emitter bandgap is E_E, the base bandgap is E_B, and the temperature dependence of the 2 kT leakage current I_l has the form

$$I_l = K_l \cdot e^{-\frac{E_E + E_B}{4kT}} \cdot e^{\frac{qV}{kT}} \tag{27}$$

while the hole and electron current $I_{h,e}$ may be given by

$$I_{h,e} = K_{h,e} \cdot e^{-\frac{E_{E,B}}{kT}} \cdot e^{\frac{qV}{kT}} \tag{28}$$

where

V = the applied voltage
$K_{h,e,l}$ = temperature independent coefficients
kT = thermal energy

The emitter efficiency, η for an N-P-N transistor is then given by

$$\eta(T) = \frac{1}{1 + \frac{K_h}{K_e} \cdot e^{-\frac{E_E - E_B}{kT}} + \frac{K_l}{K_e} e^{-\frac{(E_g - 3E_B + 2qV)}{4kT}}} \tag{29}$$

One sees that at low currents (small voltages), where the emitter efficiency is small, the temperature dependence of emitter efficiency is completely different from that at higher currents, in contradiction to the observed results. The temperature dependence of the current gain is therefore thought to be determined by the base transport factor.

For any high-temperature application of such a transistor, the leakage current is as important as the current gain. In our NAND-gate, I_{CEO} must be below 5×10^{-4} A. In Figure 28, I_{CEO} is plotted versus the reciprocal temperature for different types of GaAs transistors. As can be seen by a comparison of Figures 26 and 28, I_{CEO} appears to be the factor limiting the high temperature operation, rather than the current gain. This is borne out in the 400°C data shown in Table IV. The performance of a GaAs transistor as a function of temperature is given in detail in Table V. The data refer to device Ae 5-1 of Figure 26 and Figure 28.

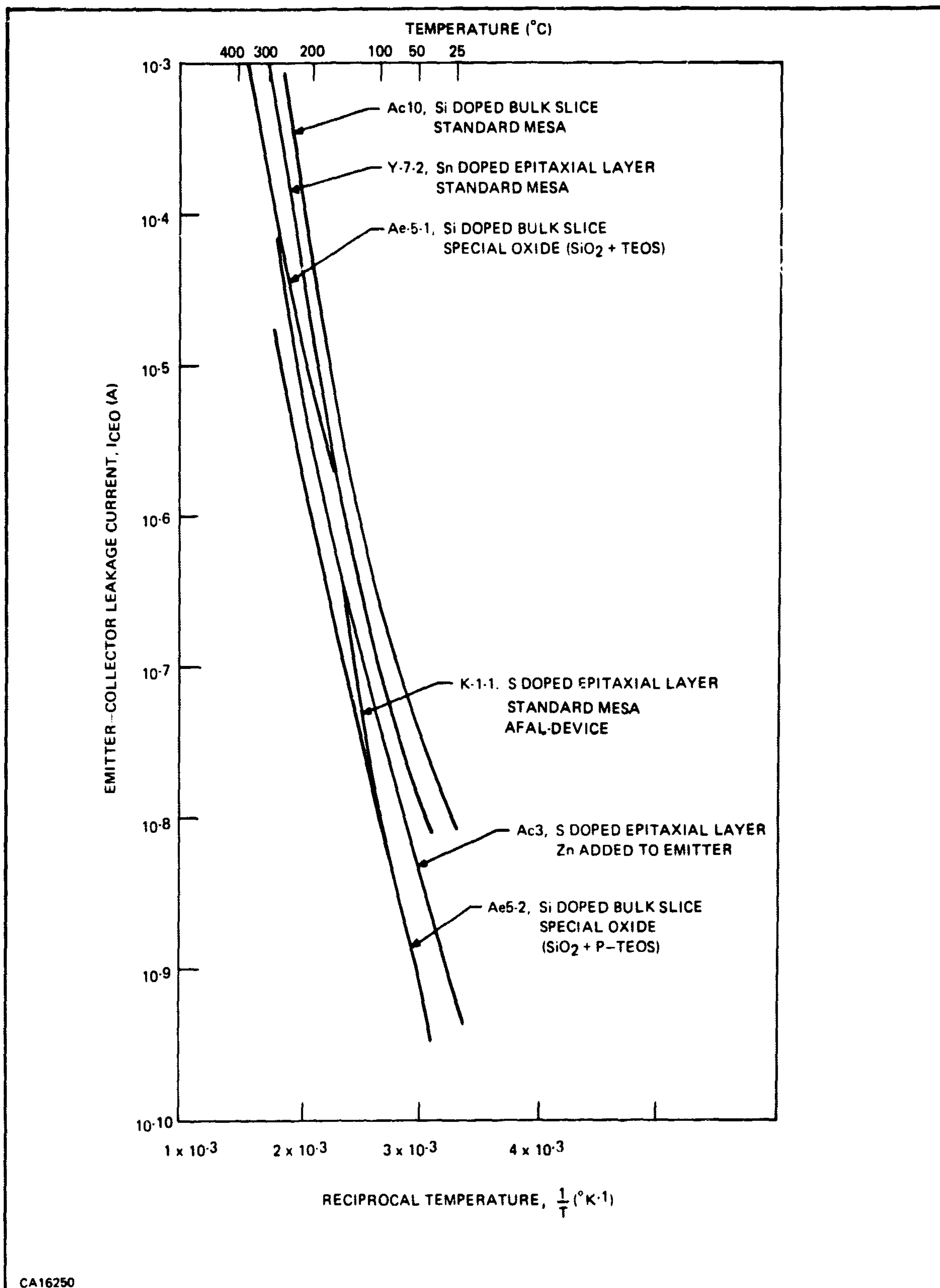


Figure 28. I_{CEO} versus Reciprocal Temperature for Various GaAs NPN Transistors Using Different Crystal Materials and Technologies. (The Collector-Junction Area is 90 mils^2 for Device Y-7-2 and 56 mils^2 for all Other Devices)

Table IV. Performance Data of GaAs Transistors at 400°C (Collector Junction Area 56 mils^2)

Device No.	Current Gain (25°C)	Current Gain (400°C)	Leakage Current, I_{CEO} (400°C)
Ai15 No. 28	30	4	6 mA
Ai16 No. 42	20	4	8 mA
Ai16 No. 44	30	7	6 mA
Ag1 No. 51	154	6	14 mA
Ag1 No. 55	105	4	7 mA
Ag1 No. 51	62	6	2.2 mA

Table V. Performance of GaAs Transistor Ae 5-1 as a Function of Temperature (Collector Junction Area 56 mils^2)

Temperature (°C)	Current Gain	Leakage Current (I_{CEO})
25	6.4	10^{-5} mA
80	13	3×10^{-5} mA
120	14	3×10^{-4} mA
180	12	4×10^{-3} mA
220	11.5	3×10^{-2} mA
270	11	0.1 mA
320	9.5	0.3 mA
340	9	0.5 mA

From the Ebers-Moll equation, one finds that the emitter-collector leakage I_{CEO} is larger by a factor of $1/1\text{-}\alpha$ than I_{CBO}, the collector-base leakage. The quantity α is the common-base current gain. Both for stripe geometry and for circular geometry, where the emitter is completely surrounded by the base contact, devices showed I_{CEO} to I_{CBO} ratios of only 2 to 3 at all temperatures. This can be explained by the very small current gain of the GaAs transistors for collector currents in the order of I_{CEO}.

C. DC CHARACTERISTICS OF PNP TRANSISTORS

PNP transistors were built from two different cadmium-doped bulk crystals. Figures 29 and 30 show the emitter-collector leakage current and the current gain of PNP devices as a function of the reciprocal temperature. Devices from one crystal, like Al-12 No. 1, were very temperature insensitive. Figure 31 displays the transistor characteristics of this device at different temperatures. The current gain at 25°C for V_{EC} = 2.5 V is 4 and increases to 6 at 400°C. The emitter-collector leakage at 25°C is high compared to NPN devices, however it has a weak temperature dependence. Figure 32 gives the emitter-collector leakage as a function of applied voltage at different temperatures. At 400°C and V_{EC} = 4 V, I_{CEO} is still below 0.4 mA.

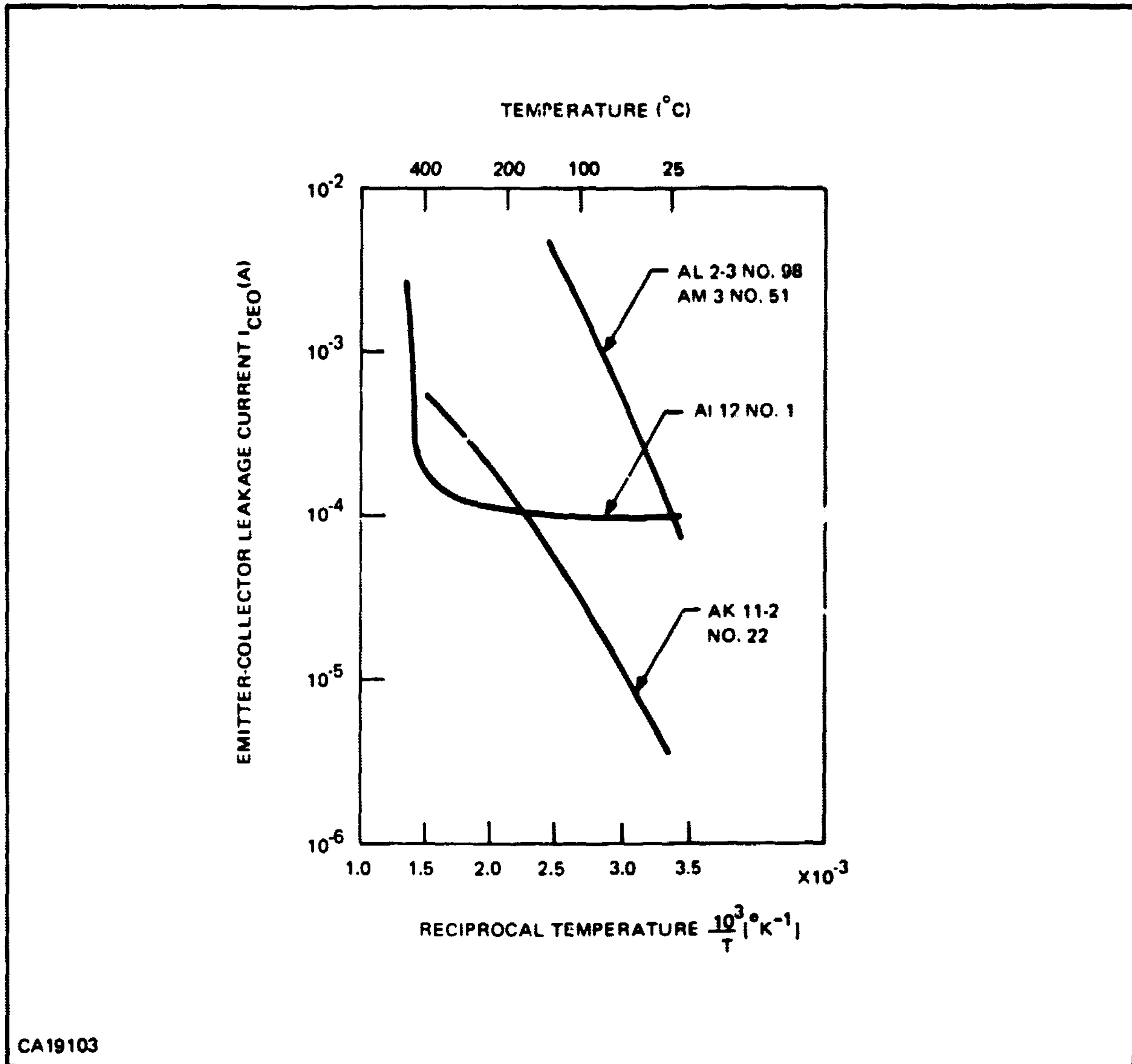


Figure 29. I_{CEO} versus Reciprocal Temperatures of PNP GaAs Transistors (Collector Junction Area 56 mils^2)

Another interesting property of this device is the low saturation voltage. Despite the use of a bulk GaAs slice, a saturation voltage of 0.5 V at 10 mA collector current was observed. It increased to 0.75 V at 400°C.

The current gain cutoff frequency, f_T, was measured to be 310 MHz, which compares with $f_T \approx 100$ MHz usually found for recently made NPN devices.

All properties of this device agree well with the experience that transistors combining the following properties:

1) low saturation voltage,

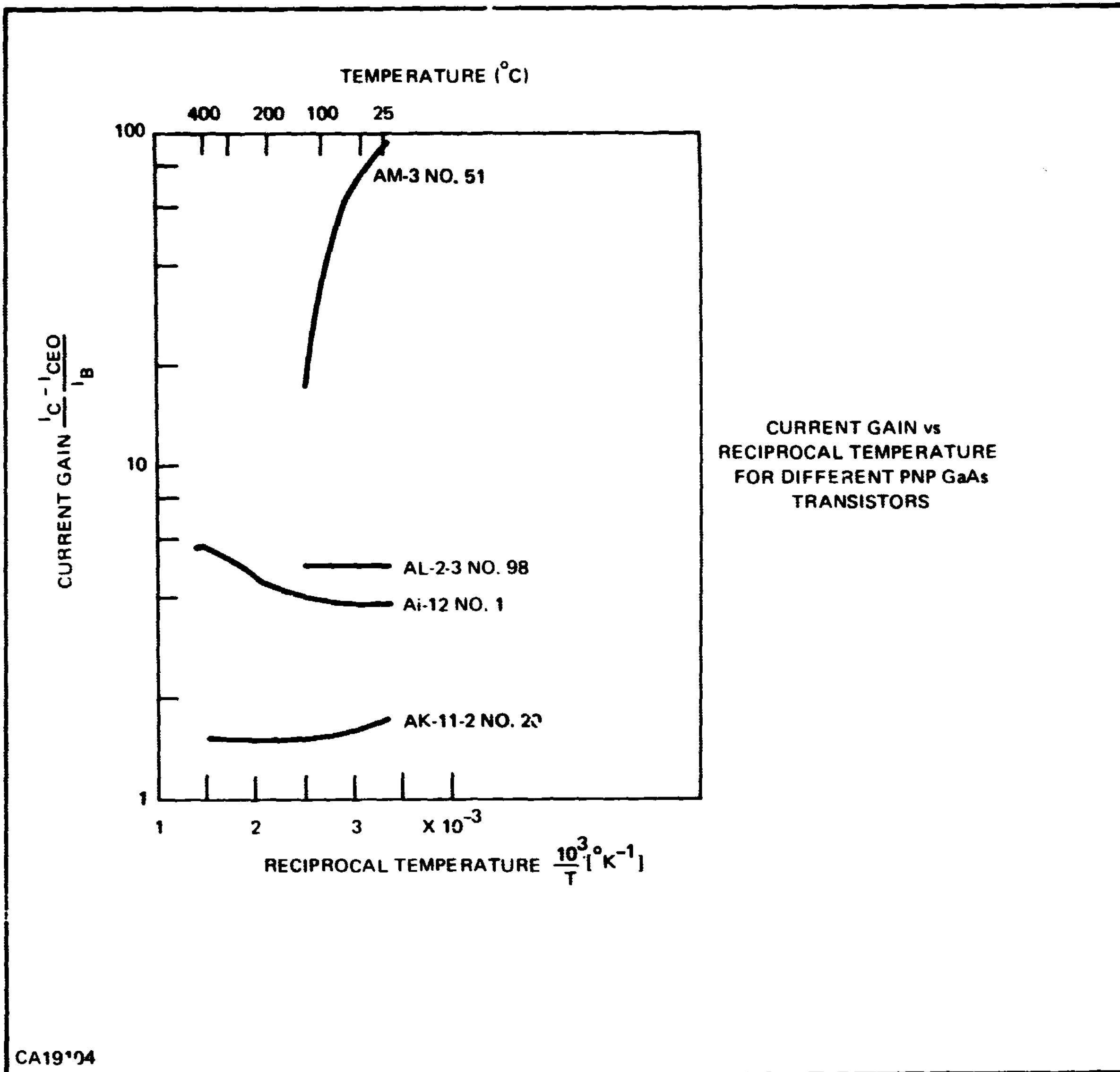


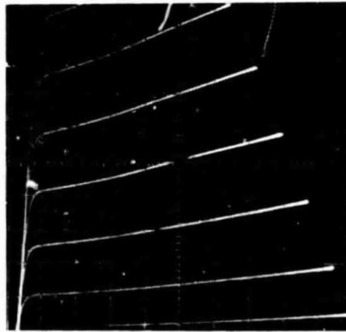
Figure 30. Current Gain versus Reciprocal Temperatures of PNP GaAs Transistors

2) low 25°C current gain, which is independent of the collector current, and

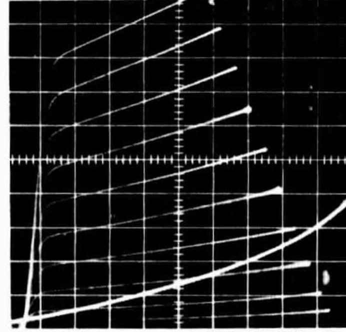
3) relatively high f_T

are also good high temperature devices. They are also not strongly affected by traps with long time-constants at 25°C, as indicated by the absence of loops in Figure 31.

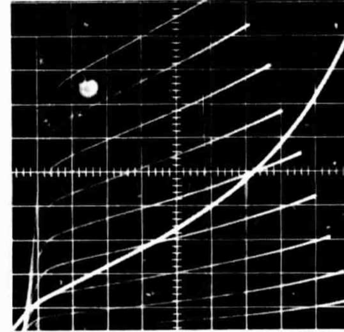
The other PNP devices, whose data are given in Figures 29 and 30, were built from slices of a second crystal. The 25°C current gain of these devices ranged from 10^{-2} to 300, due to intentional differences of the base width. The current gain of devices with high 25°C h_{FE}, as AM3 #51 of Figures 29 and 30, decreased very strongly with increasing temperature, while the current gain which is already low at 25°C stays nearly constant with increasing temperature. The limiting factor for high temperature operation is the emitter collector leakage. Devices with sufficiently high current gain at 25°C had an I_{CEO} in the mA range already at 100°C. High I_{CEO} values also prohibited a continuation of measuring h_{FE} toward higher temperatures.



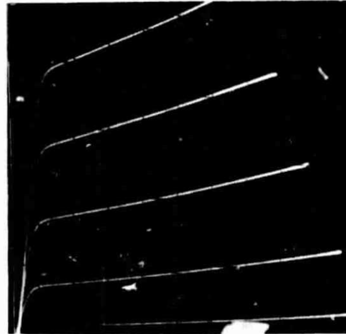
(a) 25°C
1 mA/DIV
0.5 V/DIV
0.5 mA/STEP



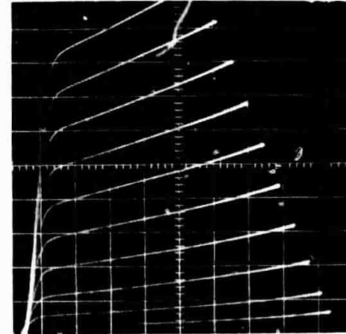
(d) 320°C
1 mA/DIV
0.5 V/DIV
0.2 mA/STEP



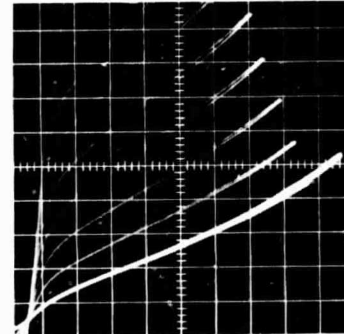
(g) 433°C
1 mA/DIV
0.5 V/DIV
0.2 mA/STEP



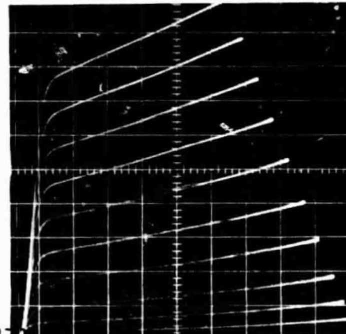
(b) 270°C
1 mA/DIV
0.5 V/DIV
0.5 mA/STEP



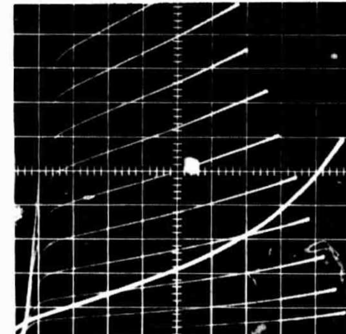
(e) 350°C
1 mA/DIV
0.5 V/DIV
0.2 mA/STEP



(h) 450°C
1 mA/DIV
0.5 V/DIV
0.2 mA/STEP

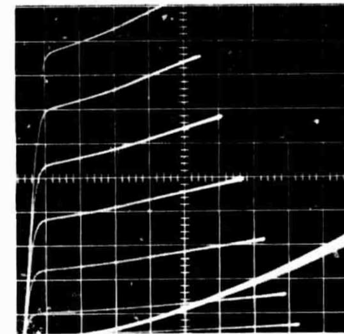


(c) 300°C
1 mA/DIV
0.5 V/DIV
0.2 mA/STEP



(f) 400°C
1 mA/DIV
0.5 V/DIV
0.2 mA/STEP

I_{CEO}:
0.1 mA/DIV
0.5 V/DIV



(i) 25°C AFTER TEST UP TO 450°C

1 mA/DIV
0.5 V/DIV
0.5 mA/STEP

I_{CEO}:
0.1 mA/DIV
0.5 V/DIV

CA17...

Figure 31. Performance of a PNP GaAs Transistor at Different Temperatures

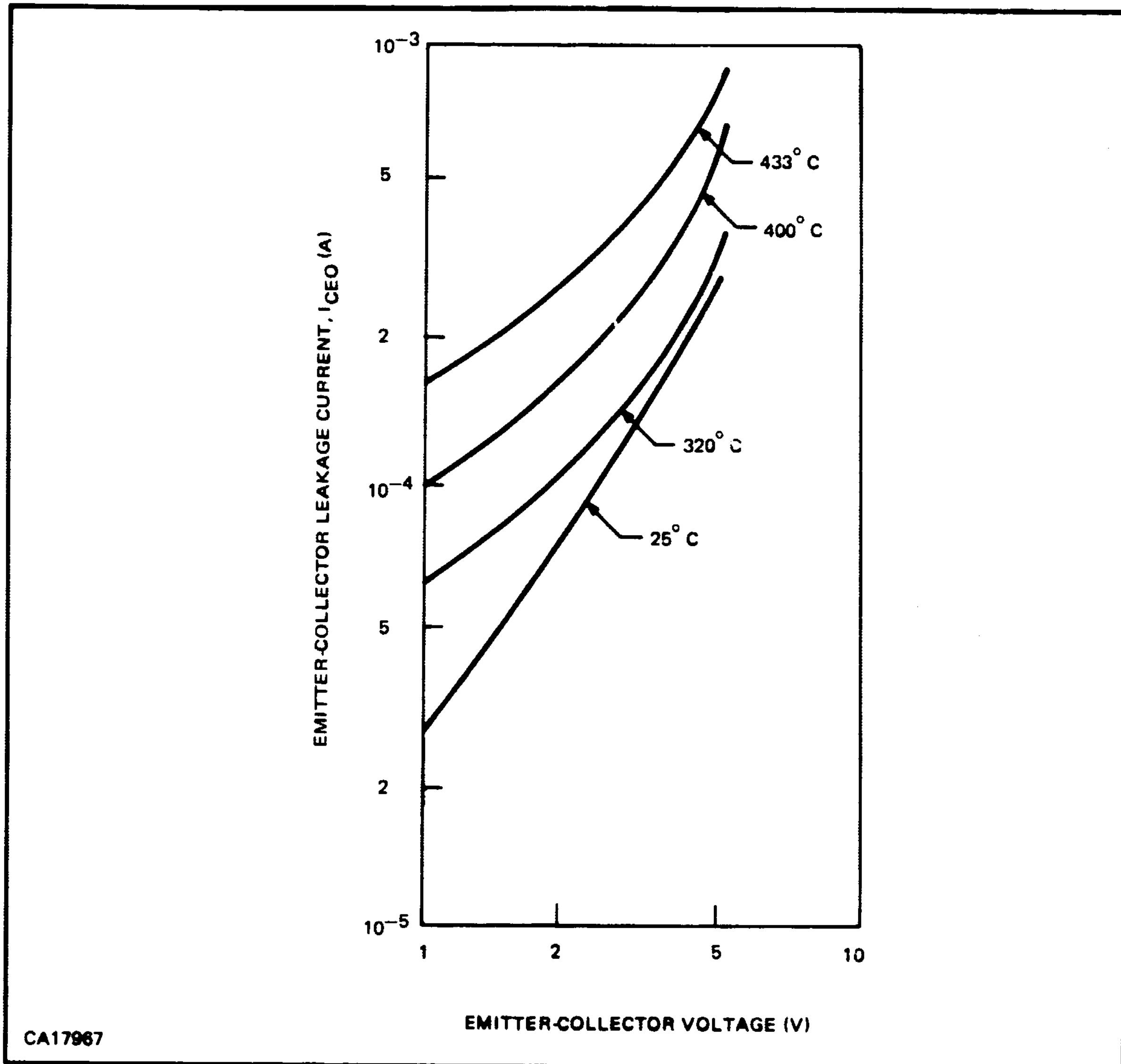


Figure 32. Emitter-Collector Leakage versus Emitter-Collector Voltage of a PNP GaAs Transistor at Different Temperatures (Collector-Base Junction Area 56 mils^2)

D. LARGE SIGNAL CHARACTERISTICS

The switching characteristics of GaAs transistors at various temperatures have been tested using the circuit of Figure 33. This basic circuit is frequently used to discuss and calculate general transistor switching characteristics. In this discussion, it is assumed that the input current is initially zero. For an input drive sufficient to saturate the transistor, the total switching transient can be described in terms of four switching times: delay time, t_d; rise time, t_r; storage time, t_s; and fall time, t_f. The following conventions describe these terms:

1) t_d – the time it takes for the collector current to increase to ten percent of its final value after the input pulse is applied.

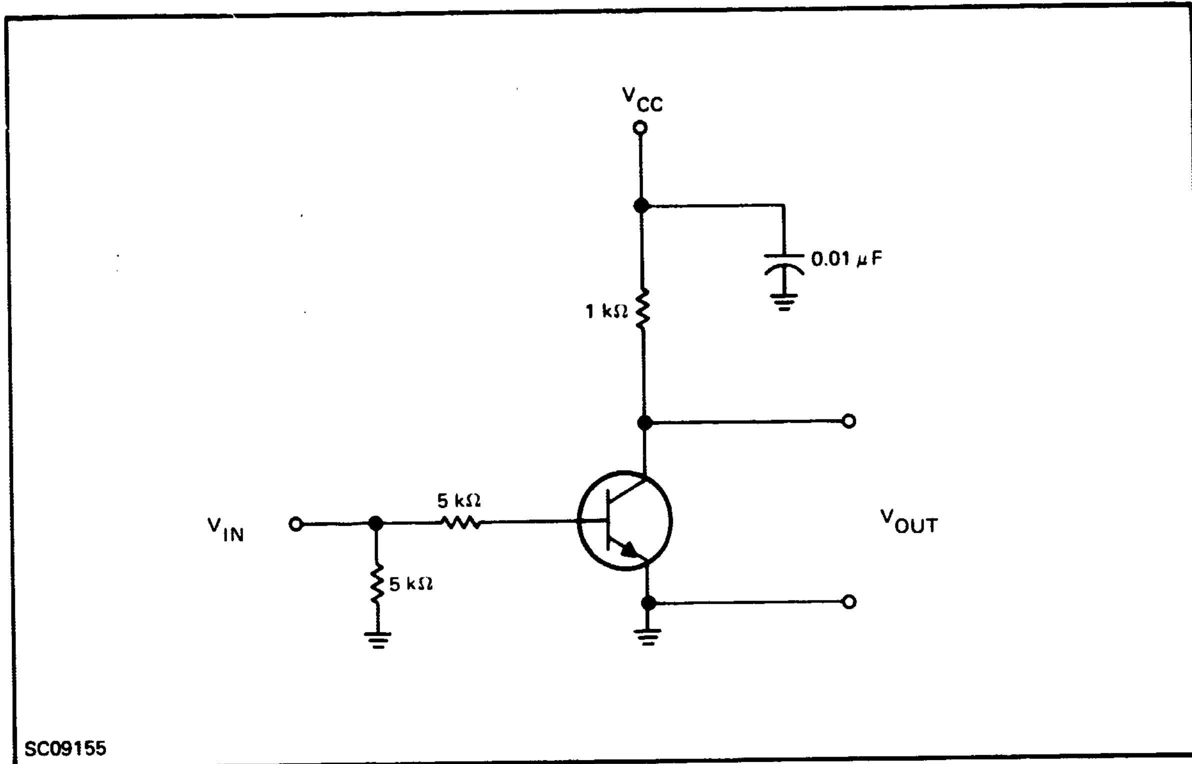


Figure 33. Test Circuit for Pulse Measurements

2) t_r – the time it takes for the collector current to increase from ten percent to ninety percent of its final value.

3) t_s – the time it takes for the collector current to decrease to ninety percent of its maximum value after the input ends.

4) t_f – the time it takes for the collector current to decrease from ninety to ten percent of its maximum value.

The following expressions can be written to approximate these terms.[35] In these expressions, rise time is calculated from zero to ninety percent output and fall time from the end of storage to ten percent output.

$$t_r = T_b \ell n \left[I_{b1}/(I_{b1} - 0.9 I_{cm}/h_{fe})\right] \quad (30)$$

$$t_s = T_s \ell n \left[(I_{b1} - I_{b2})/(I_{bs} - I_{b2})\right] \quad (31)$$

$$t_f = T_b \ell n \left[(I_{b2} + I_{cm}/h_{fe})/(I_{b2} + 0.1\, I_{cm}/h_{fe})\right] \quad (32)$$

I_{b1} = base current during input pulse

I_{cm} = maximum collector current during pulse

h_{fe} = common-emitter current gain

I_{b2} = base current turning off transistor

I_{bs} = base current required to just saturate the transistor

T_s = shortage time constant

T_b = effective lifetime of stored charge

No expression for delay time is included because the complexity of expressions for delay time exceeds their usefulness for current GaAs transistors.

GaAs transistors switching times have been measured in the temperature range between 25°C and 400°C. Results for a typical device are given in Table VI, and waveforms are shown in Figure 34.

Table VI. GaAs Transistor Switching Times Versus Temperature

	Temperature				
	25°C	100°C	200°C	300°C	400°C
t_d (μs)	0.07	0.07	0.06	0.01	0.01
t_r (μs)	0.16	0.17	0.16	0.07	0.06
t_s (μs)	38.0	6.0	0.16	0.01	0.01
t_f (μs)	138.0	10.0	0.42	0.07	0.06

The dominant switching time component at room temperature is fall time. Fall time decreases sharply with temperature, so that for temperatures greater than 200°C the sum of all four switching time components is less than one microsecond.

Referring to Equations (27) through (29), the base current after the input pulse ended, I_{b2}, is zero for GaAs transistors. The times recorded as storage time, t_s, in the table are not related to ordinary minority carrier excess charge stored in the base as in silicon and germanium transistors. That charge is stored is apparent from the long fall times at lower temperatures. In silicon and germanium transistors, the collector current and base voltage remain constant for some time after the input pulse ends; then they decrease rapidly to zero as the input pulse ends and increasing base drive past the edge of saturation has little effect. According to Equation (27), with I_{b2} = 0, fall time reduces to

$$t_f = 2.303 \ T_b \tag{33}$$

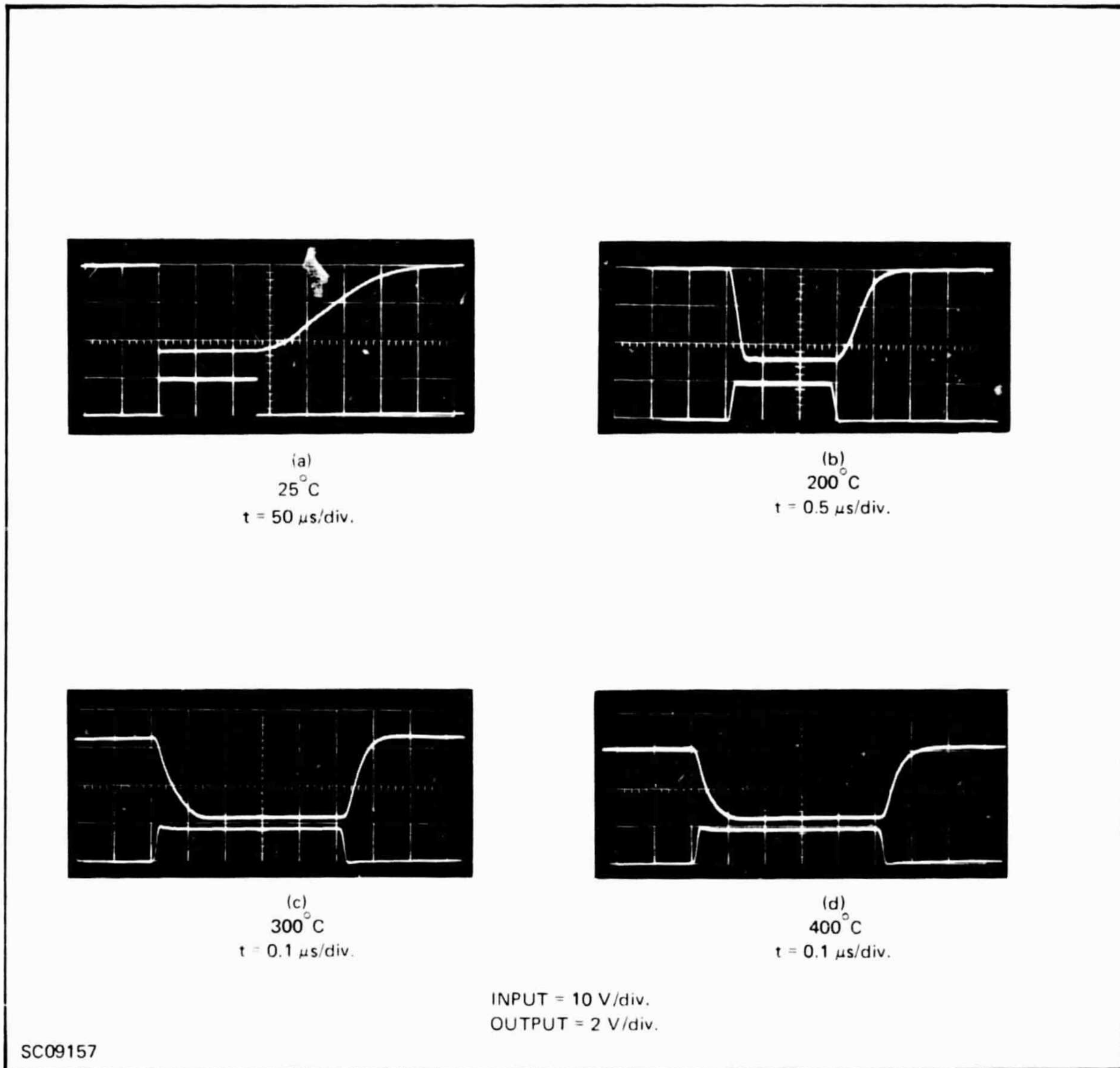


Figure 34. Common-Emitter Pulse Measurements at Various Temperatures

and the ratio of fall to rise times is

$$\frac{t_f}{t_r} = 2.303 \ \ell n \left(1 - \frac{0.9 \ I_{cm}}{h_{fe} \cdot I_{b1}}\right) \tag{34}$$

For

$$h_{fe} = 15 \text{ and } \frac{I_{cm}}{I_{b1}} = 3 \tag{35}$$

Equation (27) predicts

$$\frac{t_f}{t_r} = 0.46 \tag{36}$$

which is clearly wrong. When $I_{b2} = 0$ and the devices are not saturated and $I_{cm} = h_{FE}I_{b1}$, the equations predict $t_f = t_r = T_b$.

The rapid decrease of the fall time between 25°C and 300°C follows an exponential law. Although no satisfactory explanation is available, charge storage related to trapping centers is the suspected source of the long fall time at lower temperature. A semilogarithmic plot of the reciprocal of the fall time versus the reciprocal temperature yields an activation energy of about 0.4 eV in the above temperature range. This can be interpreted as the activation energy for releasing charge from a trapping center about 0.4 eV below the appropriate band. It is suspected that oxygen, which introduces such a level in GaAs, is responsible for the long time constant.

E. FIELD-EFFECT TRANSISTORS

Low-frequency data of GaAs FET's between 25°C and 345°C ambient temperature were taken with the curve tracer. Transistor characteristics are shown in Figure 35. Because of the high saturation current of 94 mA, the actual temperature of the active device area was considerably higher than the measured case temperature. Due to nonuniformities of the epitaxial layer in thickness and/or electrical properties, the saturation currents of the devices varied from 1 mA to 100 mA. Usually, for more thickly grown epitaxial layers, the thickness does not differ by more than 10 percent; however, this must not be necessarily true for these extremely thin layers. A nonuniform doping could be caused by out-diffusion of impurities from a substrate crystal. Our device was selected because of its high transconductance (19 mmhos at 25°C). The temperature dependence of the mobility for that doping level, ($\mu \sim T^{-1.4}$), and the temperature dependence of the heat conductivity ($\kappa \sim 1/T$) is sufficient to explain the decrease in transconductance from 19 to 6.7 mmhos between 25° and 345°C. Furthermore, the gate leakage current increased, and the unmodulated part of the source drain current increased to about 1.3 mA.

After cooling to room temperature, the low frequency data were the same as before the experiment. This is remarkable because the actual chip temperature exceeded 400°C. The weak dependence of the transconductance on the gate voltage at low voltages suggests an appreciable series resistance between source and gate.

For the device in Figure 35, the properties of the expitaxial layer were estimated in several ways. From the slope of a plot $1/C^2$ versus gate voltage for low voltages one finds $N_D = 3.5 \times 10^{15}$ cm^{-3}.

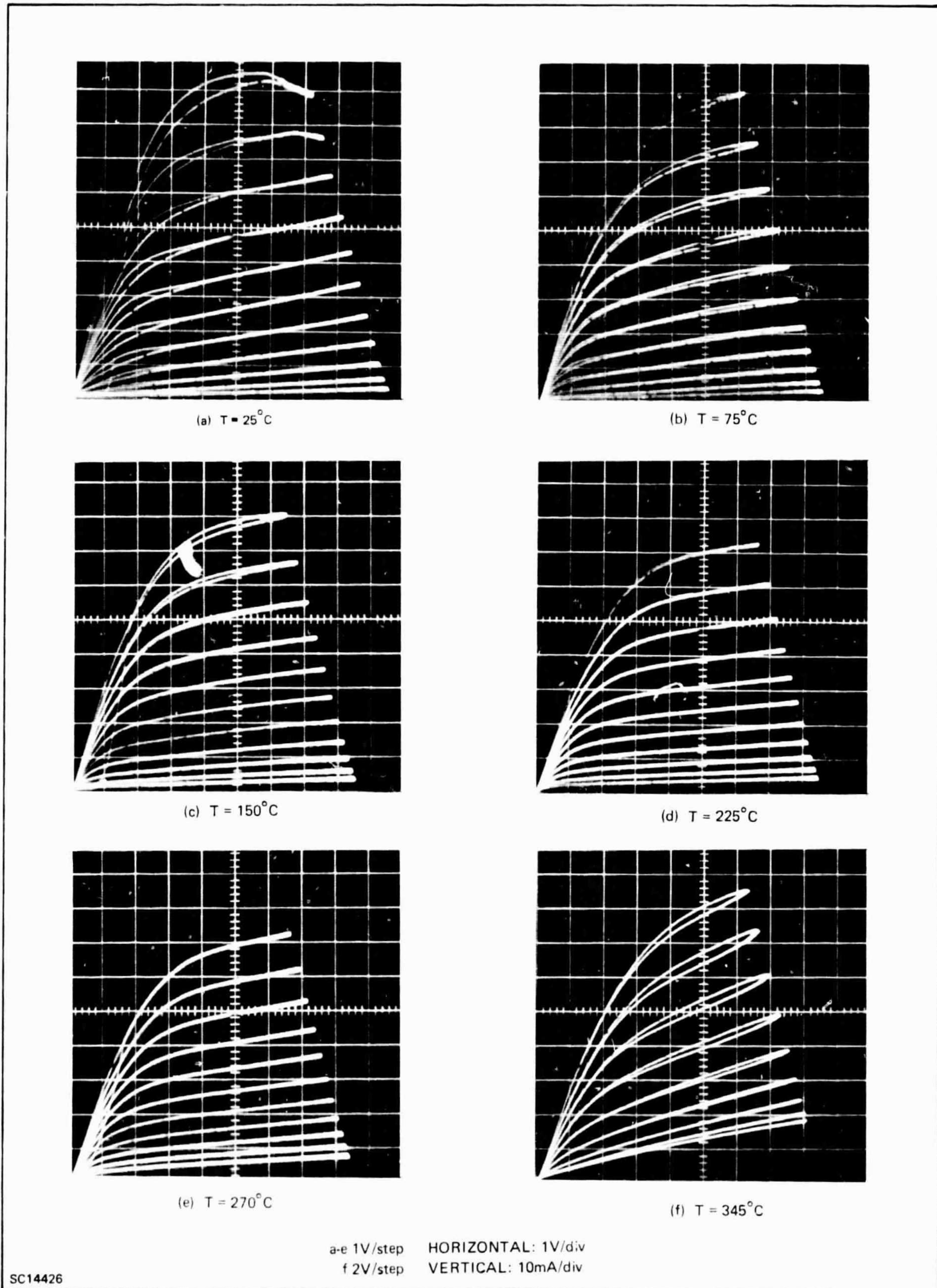


Figure 35. GaAs FET Characteristics at Different Temperatures

From

$$g_m = \frac{W}{L} \cdot q \cdot \mu \cdot N \qquad (37)$$

where

g_m = transconductance (measured)
W/L = gate width-to-length ratio
μ = carrier mobility
q = electron charge
N = carrier concentration

a carrier mobility of $\mu = 8000\ cm^2/Vsec$ is found. The following relationship holds for conventional junction FET's:

$$I_{DP} = I_{DSS}\left(1 - \frac{V_{gs}}{V_p}\right)^2 \qquad (38)$$

where

I_{DP} = pinch-off drain current
I_{DSS} = drain-source saturation current with the gate shorted to the source
V_{gs} = gate-source voltage
V_p = turn-off voltage

Plotting

$$\frac{I_{DP}}{I_{DSS}} \text{ versus } \left(1 - \frac{V_{gs}}{V_p}\right)^2 \qquad (39)$$

gave the expected straight line, when V_p = 11.6 V was used. This statement is equivalent to the following statement that the figure of merit for the nonlinearity of the forward transfer characteristic M has the value

$$M = \frac{V_p\, g_m}{I_{DSS}} = 2 \qquad (40)$$

which is typical for a spike profile rather than a uniform profile.

The y-parameters at 400 MHz of a typical device were measured with a General Radio Bridge.

$$y_{11} = (2.0 + j\ 9.2) \text{ mmhos}$$
$$y_{12} = (0.2 - j\ 3.0) \text{ mmhos}$$
$$y_{21} = (10.0 - j\ 7.4) \text{ mmhos}$$
$$y_{22} = (2.8 + j\ 6.0) \text{ mmhos}$$

for the following operating conditions:

$$V_{SD} = 4 \text{ V},\ I_{SD} = 15 \text{ mA},\ V_{SG} = -\ 0.14 \text{ V} \tag{41}$$

From these results one calculates $|g_m| = 12.5$, which also is the low-frequency value of this device.

The matched power gain was calculated using the following equation:

$$PG = \frac{|y_{21} - y_{12}|^2}{4\,(\text{Re } y_{11} \cdot \text{Re } y_{22} - \text{Re } y_{12} \cdot \text{Re } y_{21})} \tag{42}$$

For the cited values of the y-parameters, one obtains PG = 8.0. The dependence of g_m at 400 MHz on V_{gs} is similar to that at 120 Hz.

As a high temperature device this transistor is limited by the gate leakage current and by the increasing conductivity of the semi-insulating substrate. Measurements of the substrate conductivity as a function of temperature showed that the conductivity increased 4 orders of magnitude between 25°C and 250°C.

F. SILICON TRANSISTORS

To compare the high temperature performance of GaAs transistors with silicon devices, several different types of available Si transistors were evaluated. Best results were obtained from radiation-hardened transistors. The transistor was a NPN device built into a 0.5 Ω-cm epitaxial layer. The base surface concentration was 10^{18} cm^{-3} and the base thickness 1.4 μ. The minority carrier lifetime was shortened by a gold diffusion. Figures 36 and 37 show leakage currents and current gain at different temperatures. The collector-base leakage at 5 V is below 0.4 mA up to 320°C. The high temperature transistor performance is limited by the I_{CEO} increase, while the current gain shows only a slight temperature dependence. Up to 230°C this device can be operated under normal conditions. Figure 38 shows the transistor characteristics at this temperature. In addition, I_{CEO} and I_{CES} are given in different scales. At temperatures above 230°C I_{CEO} increases beyond reasonable values for normal transistor operation. However, the collector-emitter current can be controlled to values below I_{CEO} by having an electron current flowing into the base of the

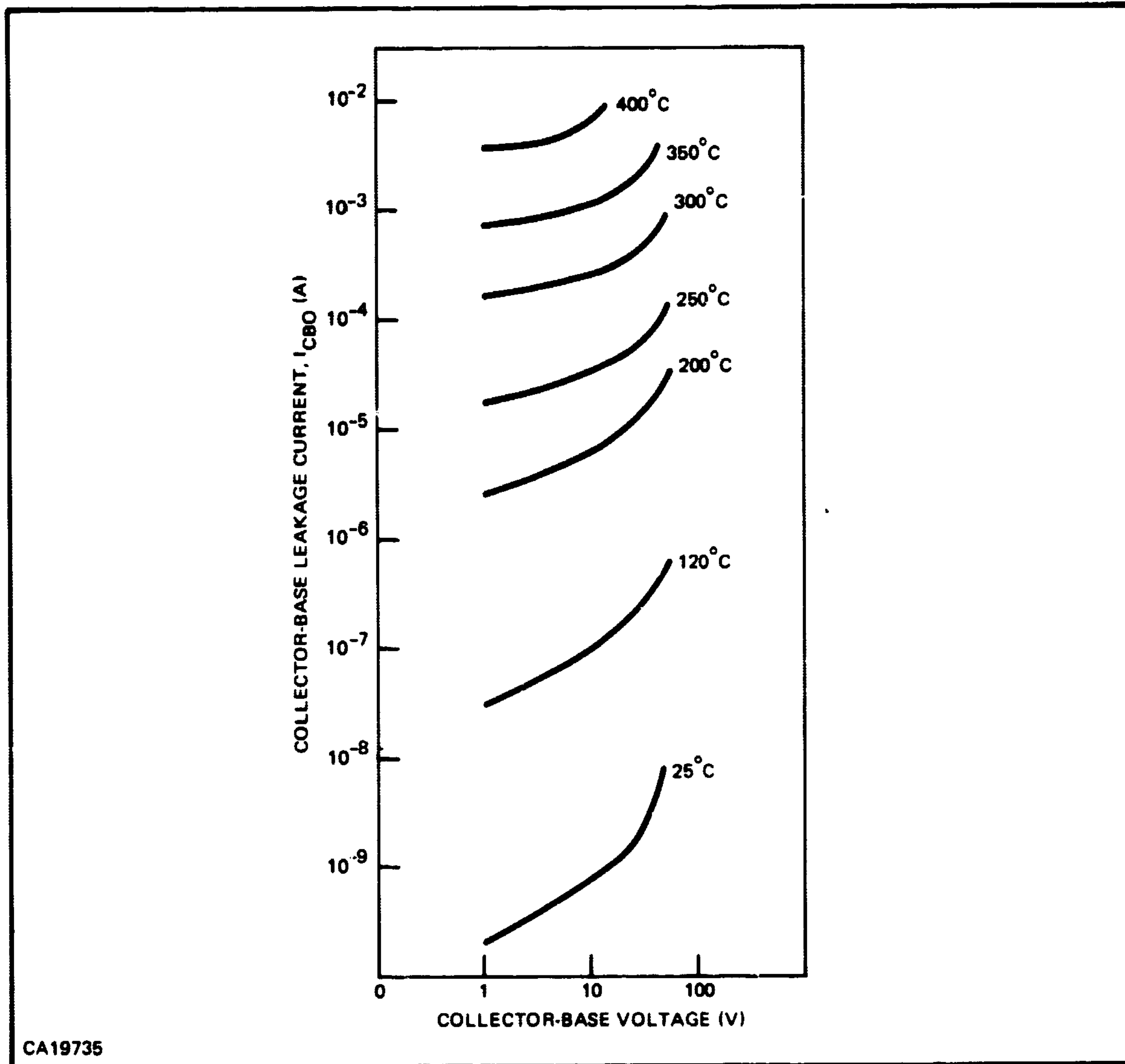


Figure 36. Collector-Base Leakage Current of a Radiation Hardened Silicon Transistor versus Collector-Base Voltage at Different Temperatures (Collector-Base Junction Area - 10 mils^2)

NPN transistor. This is equivalent to reverse biasing both the emitter and the collector junction. Figure 39 shows the performance of the device in this mode of operation at 300°C. With no base current flowing I_{CEO} versus U_{EC} is displayed (highest upper curve). Negative base-current steps cause a decrease of the emitter-collector current which finally approaches I_{CES}. I_{CES} is displayed. separately in Figure 39 in a different scale. Using this mode of operation for silicon transistors, circuits working up to 300°C can be constructed. The emitter-collector current could be controlled between I_{CEO} = 10 mA and I_{CES} = 0.2 mA with a base current of about 0.15 mA, corresponding to a "current gain" of about 50. The Si devices tested here were devices already available and were not designed particularly for high temperature application. It was thought desirable to test devices with a higher doped collector region, that is, a lower collector base breakdown voltage and a lower 25°C-current gain. The fabrication of special Si devices was beyond the scope of this program.

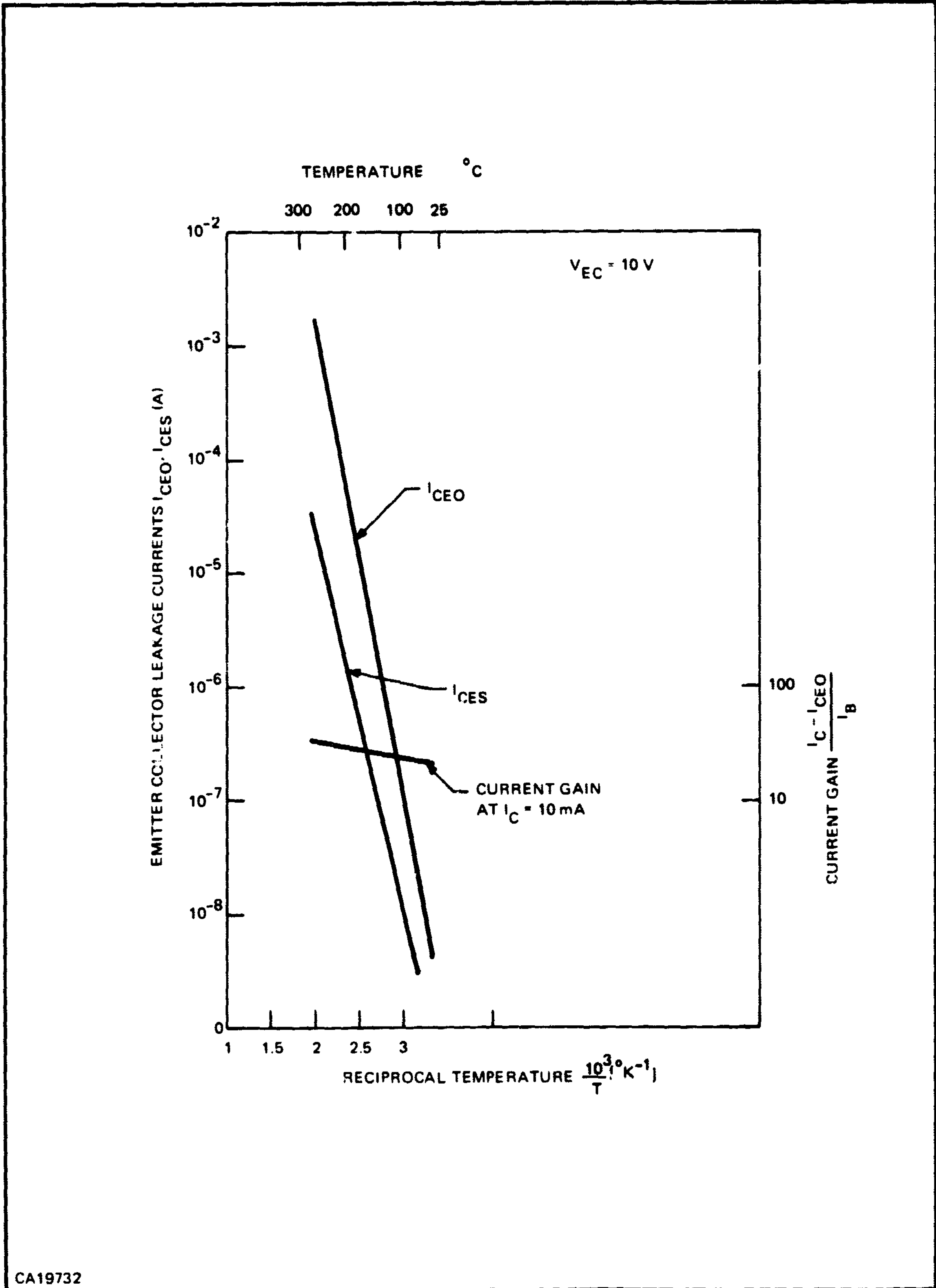


Figure 37. Collector-Emitter Leakage Currents and Current Gain versus Reciprocal Temperatures of a Radiation Hardened Si Transistor (Collector-Base Junction Area - 10 mils^2)

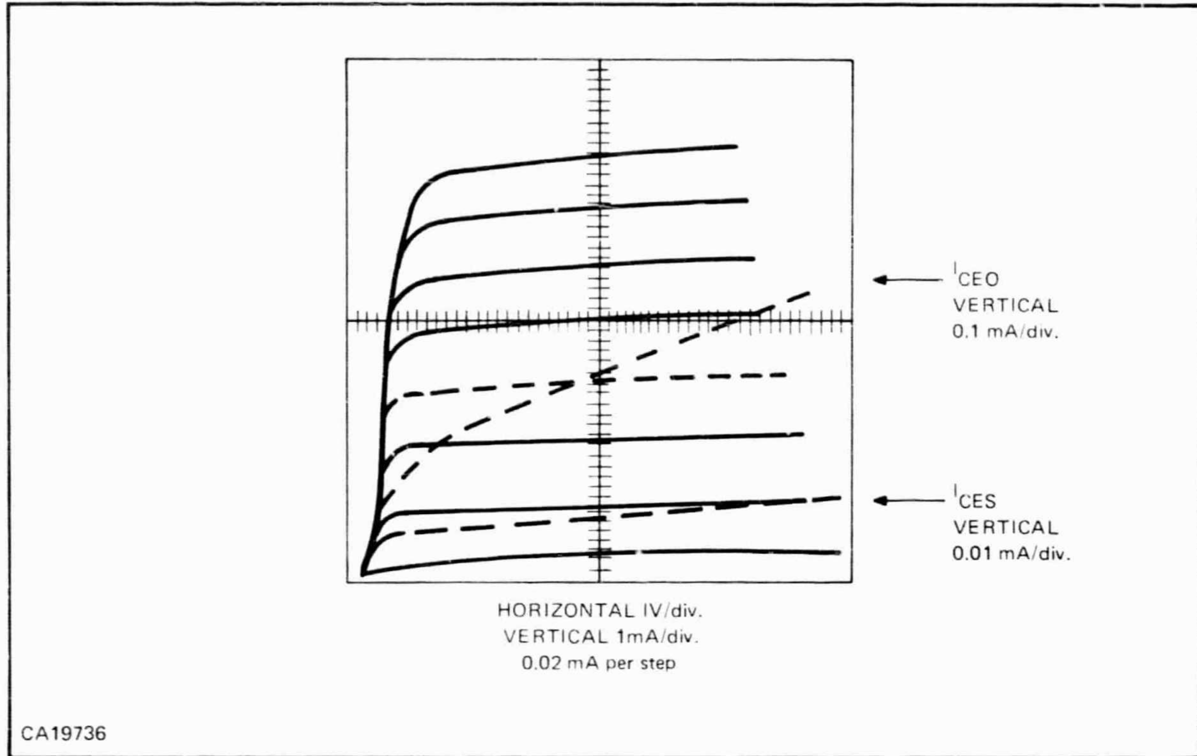


Figure 38. Transistor Characteristics of a Radiation Hardened Si Transistor at 230°C

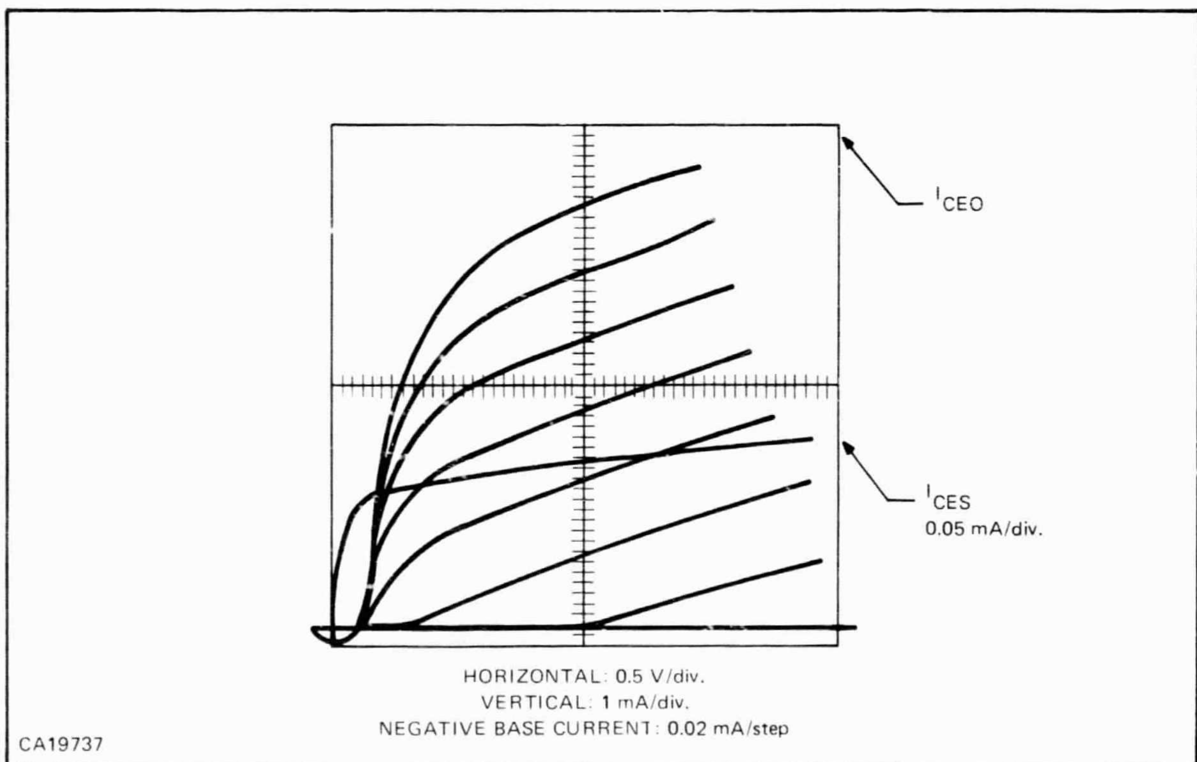


Figure 39. Transistor Characteristics of a Radiation Hardened Si Transistor at 300°C

SECTION VI

DEVICE STABILITY

A. BASIC LIMITATIONS ON STABILITY

Studies were performed on the rediffusion of emitter and base regions at a temperature of 500°C. Samples were diffused at first with magnesium, then with sulfur, under conditions identical to those used for transistor fabrication. Emitter and base junctions were measured for reference purposes. All samples were sealed individually in ampoules and placed into 500°C test furnaces. At square roots of time intervals of about 8.5 $(\text{hours})^{1/2}$, samples were removed from the furnace and the junction depths remeasured. The base layer had advanced from 2 μm to 2.8 μm after a diffusion of 108 days. An estimate for the diffusion constant is obtained from

$$D_2 = \frac{1}{4\, t_2} (x_2{}^2 - x_1)^2 \tag{43}$$

where

x_2 = junction depth after second diffusion at 500°C
x_1 = junction depth after first diffusion at 1100°C
t_2 = diffusion time for second diffusion at 500°C
D_2 = diffusion constant at 500°C

The diffusion constant for magnesium at 500°C obtained in this way is 2×10^{-15} cm^2/sec. High-temperature diffusion experiments, performed earlier in this laboratory, yielded an activation energy of 2.7 eV and a value for D_o of 2.6×10^{-2} cm^2/sec. The diffusion constant at 500°C, extrapolated from these data, is 7×10^{-20} cm^2/sec, and is more than four orders of magnitude too low.

One possible explanation is that the observed change is not due to a diffusion process but to an in-site conversion of neutral species into acceptor-type impurities within the crystal. The source of such neutral species can be sought in the concentration of electrically inactive sulfur introduced during the emitter diffusion process. In Figure 40, the circles indicate the distribution of sulfur atoms in depth as determined by radio-tracer measurements. The sulfur was diffused into an Mg-diffused layer so that the resulting N-P-N regions were similar to those in transistors. The sulfur distribution profile exhibited two diffusion fronts. The slow-diffusion portion had a surface concentration of 1×10^{19} cm^{-3}, which is a factor of about 5 higher than the electrically active sulfur. The fast-diffusing component, however, has not been observed as yet. The surface

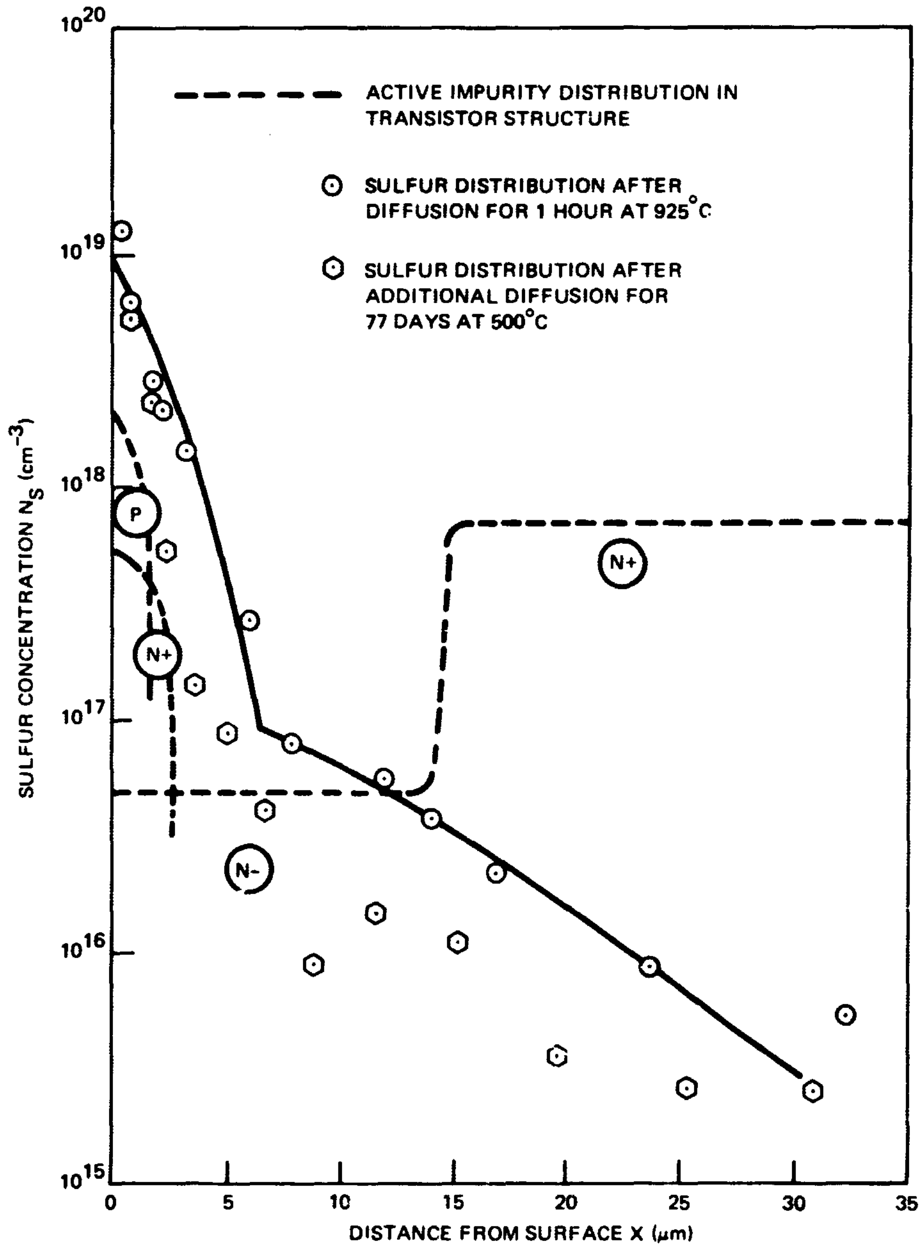


Figure 40. Impurity Distributions for Emitter-Base and Collector Dopants in NPN GaAs Transistors

concentration of this component was 1.4×10^{17} cm^{-3}, and the diffusion constant was 5.6×10^{-11} cm^2/s. Both profiles follow complementary error-functions (solid lines in Figure 40). Autoradiograms have shown no evidence of localized diffusion. Results indicate that all regions of the transistor, including all of the N-region, are dominated by the sulfur diffusion. The diffusion tail does not contain sulfur on acceptor sites since no conversion of the collector region is observed. Sulfur is absent on donor sites also, at least above a concentration of about 10^{16} cm^{-3}, since the junction depth in low concentration P-type material is given by the electrically active portion of the fast-diffusing species. The electrically active impurity distributions in the emitter, base and collector region are indicated in Figure 40 by the dashed lines. To explain the unexpected high-diffusion constant for Mg, it is conjectured that a portion of the electrically inactive sulfur changes sites, or forms a complex, with the result that the acceptor concentration in the base-collector region increases. Since the inactive sulfur concentration is greater at the base-collector junction than it is deeper in the collector region, and since the background-acceptor concentration due to the magnesium diffusion is higher at the base-collector junction, a type conversion appears at first on the N-type side nearest the collector junction. This has the effect of an apparent out-diffusion of the base region.

Measurement of the emitter-base junction, by staining techniques, has shown no evidence for a widening or narrowing of the emitter region. Measurements of the sulfur distribution profile using radio-tracer techniques show, however, a loss of sulfur (see Figure 40) after a diffusion of 77 days at 500°C. The mechanism by which the sulfur concentration was reduced has not yet been determined. Diffusion of the sulfur into the bulk can be excluded because of the low concentration measured beyond a depth of 20 μm. Out-diffusion to the surface is possible, since the surface concentration was found anomalously high, perhaps due to the formation of a gallium-sulfur compound at the surface. Since the concentration gradient is directed away from the surface, sulfur atoms cannot diffuse to the surface in their neutral state. Acceptor-type sulfur atoms could diffuse to the surface, aided by the electric field of the electrically active sulfur concentration in the emitter. More studies are necessary to determine the reason for the change in the total sulfur concentration that comes with long-term, low-temperature heat treatment.

Summarizing the 500°C diffusion results, we conclude that the electrically active emitter region stays constant over a period of at least 108 days within the limits of accuracy of the measurement technique, which is 0.1 μm. The base region widens at a rate which corresponds to a diffusion constant of 4 to 5 orders of magnitude higher than expected from extrapolation of high-temperature magnesium diffusion data. The total sulfur concentration is higher than the electrically active impurity concentration in all regions of the transistor. An in-site conversion of these neutral sulfur atoms has been assumed to explain the changes in the base layer. At this point, it should be mentioned that a similar effect could also explain the conversion of the N-type collector discussed earlier. During vapor-phase epitaxial deposition, out-diffusion of neutral species from the substrate can occur with subsequent conversion at the diffusion temperature. At the same time, it can be assumed that the electron concentration in the epitaxial substrate is much smaller than the total tin or sulfur concentration in the substrate. Both effects would lead to a concentration of neutral species much higher than deduced from electrical evaluation of the epitaxial collector material. Based on these results, it is recommended that present state-of-the-art GaAs devices are not used at operating temperatures of the junction close to 500°C when long term stability is required.

B. DEVICE STABILITY

To determine the stability of devices, transistors were stored at 300°C with no bias applied. The collector-base current, the current gain at different collector currents (10^{-7} to 10^{-3} A) and the emitter-base voltage at different collector currents were measured at 25°C, between storage times. The total storage time added up to 225 hours. The collector-base leakage increased about 30 percent. The current gain data did not show changes that exceeded the data spread of about 20 percent. The emitter-base voltage did not change either, so that no indication was found for severe deterioration under those stress conditions.

NPN transistors built with S-doped epi-layer slices having an intentional Cd background were life tested at 300°C with 5 volt emitter-collector voltage applied and 2 mA dc collector current. The data between the steps of the experiment were taken from curve tracer pictures. The devices were first measured at 25°C, then heated to 300°C and measured, remeasured at 25°C and finally inserted into the lifetime chamber.

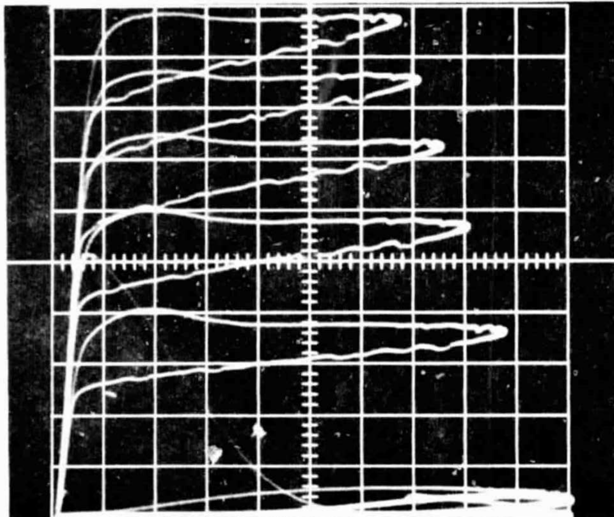
With the devices at 300°C, data were taken after 25, 75, 160, and 250 hours. After the life test, 25°C data were taken again. We started with 12 devices; two were damaged during the measurements. The current-gain data for 25°C are subject to an appreciable error due to strong loops of the curve-tracer pictures.

Figure 41 shows the transistor characteristics of a device before life test at 25°C and 300°C and after 260 hours of life test, also at 25°C and 300°C. In addition, I_{CEO} is shown in a different current scale, 0.01 mA/division and 0.1 mA/division for 25°C and 300°C respectively.

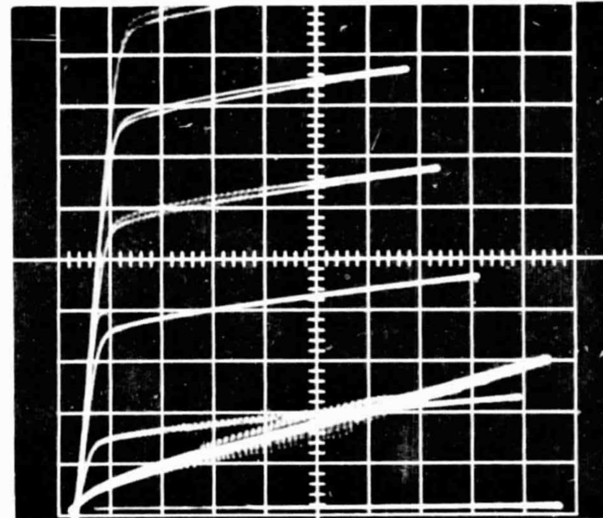
Table VII summarizes the results of the life test showing the current gain, h_{FE} and the saturation voltage, V_s, at 10 mA at different stages of the experiment.

I_{CEO} at the first 300°C heating was about 0.2 mA to 0.5 mA, decreased to 0.1 to 0.2 mA at the beginning of the life test, and then stayed stable until the end of the experiment. Similar results were obtained in other life test experiments with different kinds of NPN devices. The 300°C characteristics do not change appreciably. The degradation is apparent in the 25°C current gain data. Some devices survived cycling and life testing without change.

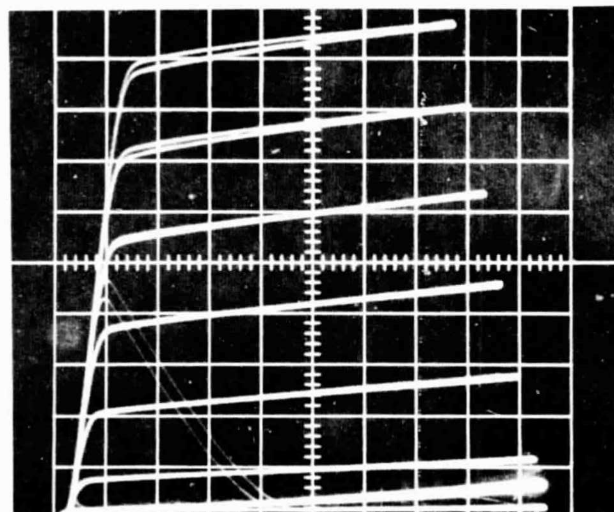
Life test experiments with standard NPN transistors were performed at 400°C, monitoring the collector-base leakage current I_{CBO}, as a function of time with 5 volts reverse bias applied. The 400°C leakage currents were between 0.3 mA to 1 mA at the beginning, and stayed unchanged for the first 20 to 50 hours. In the following 100-200 hours, I_{CBO} increased typically by a factor of two to three. Also, a significant increase of the saturation voltage by a factor of two was observed several times. It has to be concluded that operation at 400°C is beyond the safe temperature range for these devices.



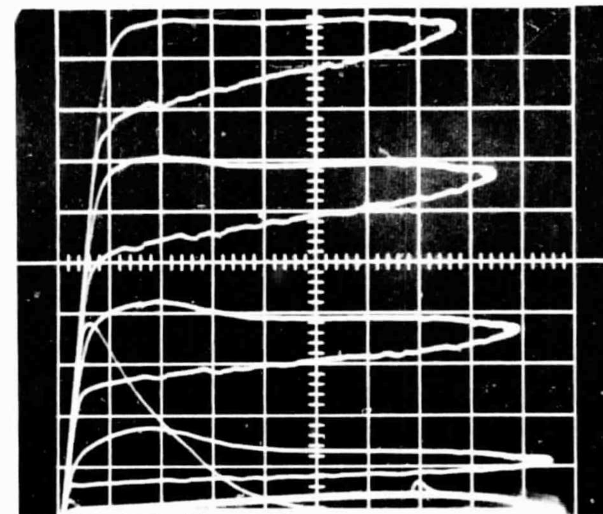
(a) VERTICAL, 1 mA/DIV; HORIZONTAL, 1 V/DIV
0.02 mA/STEP
I_{CEO}: 0.01 mA/DIV; T = 25° C BEFORE LIFE TEST



(b) VERTICAL, 1 mA/DIV; HORIZONTAL, 1 V/DIV
0.2 mA/STEP
I_{CEO}: 0.1 mA/DIV; T = 300° C BEFORE LIFE TEST



(c) VERTICAL, 1 mA/DIV; HORIZONTAL, 1 V/DIV
0.2 mA/STEP
I_{CEO}: 0.1 mA/DIV; T = 300° C AFTER 260 HOURS



(d) VERTICAL, 1 mA/DIV; HORIZONTAL, 1 V/DIV
0.1 mA/STEP
I_{CEO}: 0.01 mA/DIV; T = 25° C AFTER 260 HOURS

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Figure 41. Performance of NPN GaAs Transistor at 20°C and 300°C Before and After Life Test at 300°C for 260 Hours

Table VII. Life-Test Data of NPN Transistors

Device Temperature: 25°C					300°C				
Device		Before Test	After First Heating to 300°C	After 250 Hrs Test at 300°C	After First Heating	After 25 Hrs	After 75 Hrs	After 160 Hrs	After 250 Hrs
1	h_{FE}	33	28	27	5	5	4.5	5	6
	V_s[V]	1.0	1.3	1.0	2.0	2.0	2.0	2.0	2.0
2	h_{FE}	62	50	46	8	9	9	9	9
	V_s[V]	0.8	0.9	1.0	1.5	1.5	1.5	1.5	1.3
3	h_{FE}	70	56	56	11	12	11	11	13
	V_s[V]	0.6	0.9	0.9	1.5	1.5	1.5	1.5	1.5
4	h_{FE}	20	20	15	8	7	7	7	6.5
	V_s[V]	2.5	2.7	2.8	3.0	3.0	3.0	3.0	3.3
5	h_{FE}	40	40	40	6	6	6	6	6
	V_s[V]	1.2	1.5	1.2	2.8	2.8	2.8	2.8	2.8
6	h_{FE}	40	33	18					
	V_s[V]	0.8	0.8	1.5	1.5	1.5	1.5	1.5	1.5
7	h_{FE}	120	100	60	26	20	20	19	15
	V_s[V]	0.8	0.8	1.0	1.5	1.5	1.5	1.5	1.5
8	h_{FE}	83	66	56	20	20	20	15	13
	V_s[V]	0.5	0.5	0.5	0.9	0.9	0.9	0.9	1.0
9	h_{FE}	140	130	90	16	16	16	16	16
	V_s[V]	0.8	0.8	0.8	1.5	1.5	1.5	1.5	1.5
10	h_{FE}	90	90	25	12	12	12	9	8
	V_s[V]	0.8	0.8	1.0	1.5	1.5	1.5	1.5	1.5

Similar experiments were performed with diodes built into N-type GaAs. Diodes from different fabrication runs were measured at different temperatures up to 300°C, temperature cycled, life tested at 300°C for 200 hours, remeasured and finally life tested at 400°C. Table VIII summarizes the results. It shows the reverse leakage current at 2 volts and the voltage across the diode with 10 mA forward current flowing.

After the 300°C life test the devices did not show changes in their characteristics. Many showed even a decrease of the leakage currents. After the 400°C life test, two diodes were severely degraded. The 400°C leakage currents of the other diodes showed increases not higher than 30 percent. Since this increase is consistent for all diodes, we assume that the temperature was slightly higher (~5°C) when remeasuring the diodes. The main difference between 300°C and 400°C testing is the much higher number of catastrophic failures when cycling from room temperature to the higher test temperatures. No striking difference could be found between planar diodes (devices No. 31 to No. 35) and mesa devices (device No. 41 to No. 45 of Table VIII).

Table VIII. Life-Test Data of Diodes from Different Fabrication Runs

Device		Before Test		After 300°C Cycling	After 215 Hours at 300°C		Begin of 400°C Test	After 212 Hours at 400°C	
		25°C	300°C	25°C	25°C	300°C	400°C	25°C	400°C
31	I_L	4.5×10^{-9}	5×10^{-4}	3×10^{-9}	3×10^{-9}	3×10^{-4}	2×10^{-3}	4.4×10^{-9}	2.4×10^{-3}
	V_F	0.95 V	0.5 V	0.90 V	0.95 V	0.55 V	0.42 V	0.95 V	0.35 V
32	I_L	6×10^{-8}	5.5×10^{-4}	6×10^{-8}	6×10^{-9}	2×10^{-4}	2.1×10^{-3}	6.5×10^{-8}	2.6×10^{-3}
	V_F	1.0 V	0.48 V	0.90 V	1.0 V	0.55 V	0.42 V	1.0 V	0.35 V
33	I_L	2.3×10^{-7}	4×10^{-4}	5×10^{-7}	10^{-7}	1.6×10^{-4}	10^{-3}	3.2×10^{-7}	1.3×10^{-3}
	V_F	1.1 V	0.5 V	1.0 V	1.1 V	0.6 V	0.48 V	1.2 V	0.55 V
34	I_L	1.8×10^{-7}	3.5×10^{-4}	1.2×10^{-7}	1.2×10^{-7}	1.5×10^{-4}	1.5×10^{-3}	1.3×10^{-7}	2×10^{-3}
	V_F	0.9 V	0.45 V	0.8 V	0.9 V	0.5 V	0.4 V	0.9 V	0.35 V
35	I_L	10^{-7}	5×10^{-4}	4.5×10^{-8}	4.5×10^{-8}	2×10^{-4}	1.6×10^{-3}	6.8×10^{-8}	2.1×10^{-3}
	V_F	0.85 V	0.45 V	0.8 V	0.82 V	0.5 V	0.32 V	0.85 V	0.32 V
41	I_L	7.5×10^{-10}	2.4×10^{-5}	1.1×10^{-10}	1.1×10^{-10}	8×10^{-6}	10^{-4}	7×10^{-10}	1.6×10^{-4}
	V_F	1.2 V	0.7 V	1.1 V	1.2 V	0.75 V	0.6 V	1.15 V	0.55 V
42	I_L	4×10^{-7}	2.5×10^{-5}	4×10^{-7}	2.5×10^{-7}	1.4×10^{-5}	2×10^{-4}	2×10^{-7}	2.4×10^{-4}
	V_F	1.2 V	0.7 V	1.1 V	1.2 V	0.75 V	0.58 V	(XX)	3.0 V
43	I_L	4.5×10^{-7}	2.8×10^{-5}	4.5×10^{-7}	4.5×10^{-7}	1.2×10^{-5}	1.7×10^{-4}	7.0×10^{-9}	2.3×10^{-4}
	V_F	1.2 V	0.7 V	1.15 V	1.15 V	0.75 V	0.6 V	1.2 V	0.55 V
44	I_L	6×10^{-11}	3.5×10^{-5}	2.2×10^{-11}	2.2×10^{-11}	1.4×10^{-5}	2×10^{-4}	4.5×10^{-10}	2.5×10^{-4}
	V_F	1.2 V	0.7 V	1.15 V	1.15 V	0.73 V	0.6 V	(XX)	3.5 V
45	I_L	6×10^{-7}	3×10^{-5}	6×10^{-7}	6×10^{-7}	1.3×10^{-5}	1.8×10^{-4}	9×10^{-9}	2.1×10^{-4}
	V_F	1.2 V	0.7 V	1.15 V	1.15 V	0.74 V	0.6 V	1.2 V	0.55 V

Leakage Current I_L [A] at 2V

Forward Voltage V_F [V] at 10 mA

(XX) Severe Degradation

More severe and less predictable degradation was observed when the devices were cycled between 400°C and 25°C. A similar general experience was made with GaAs transistors. Catastrophic degradation occurs mainly during temperature changes and not during operation, even at 400°C. As a result of our experiments, we concluded that 300°C as case temperature and 350°C as junction temperature were the maximum safe temperatures for GaAs devices.

SECTION VII

CIRCUITS

A. GENERAL

To study the performance and stability of high temperature microelectronic circuits using GaAs components, thick- and thin-film circuits were designed and built. A NAND-gate circuit was realized in thick-film technology. The resistors were fabricated by silk-screening and sintering a mixture of palladium oxide, silver and a glass frit. As an example of a thin-film circuit, a feedback pair amplifier was fabricated with NiCr-resistors. Conventional photomasking techniques were used. A nickel-chromium deposit over an entire alumina substrate was plated selectively to define good conductor areas and all metal was removed except in the regions where either resistors or conductors were required. An oxide was deposited to protect the Ni-Cr resistors during high-temperature processes. The oxide was removed over conductor areas for semiconductor chip mounting and wire bonding. These resistors proved to be sufficiently stable for operation at 400°C over a time period of more than 500 hours.

B. THICK-FILM CIRCUITS

1. Circuit Description

The basic NAND gate was selected for design and fabrication because it is a common logic circuit. A wide distribution of device characteristics is acceptable. The NAND function is obtained if the output voltage is low when all input voltages are high; if any input voltage is low, the output voltage is high. Two transistors are used in the circuit to provide adequate circuit gain to drive a load consisting of at least three similar NAND gates. Depending on the characteristics of the circuit elements, several variations of the basic circuit can be used. The basic circuit is shown in Figure 42. Terminal R1 is connected to either terminal V_{CC} or terminal C_1 depending on the values of circuit resistance obtained. Diode D_3 can be short-circuited internally before a device is canned, if the base-emitter voltages of Q_1 and Q_2 are large due to high base resistance. The layout of metallized lines and thick-film resistors is shown in Figure 43. Both ends of each circuit resistor are available for external resistance measurements. In addition, the same metal pattern can be used with discrete external resistors, such as glass-encapsulated carbon-film resistors.

2. Circuit Design and Operation

The high- and low-output voltages of the circuit are provided by control of transistor Q_2. When Q2 is OFF, the output voltage is high. Q_2 is driven by Q_1. Transistor Q_1 is never biased to cutoff. When the input voltage is low, Q_1 is biased into its normal active region. When the input

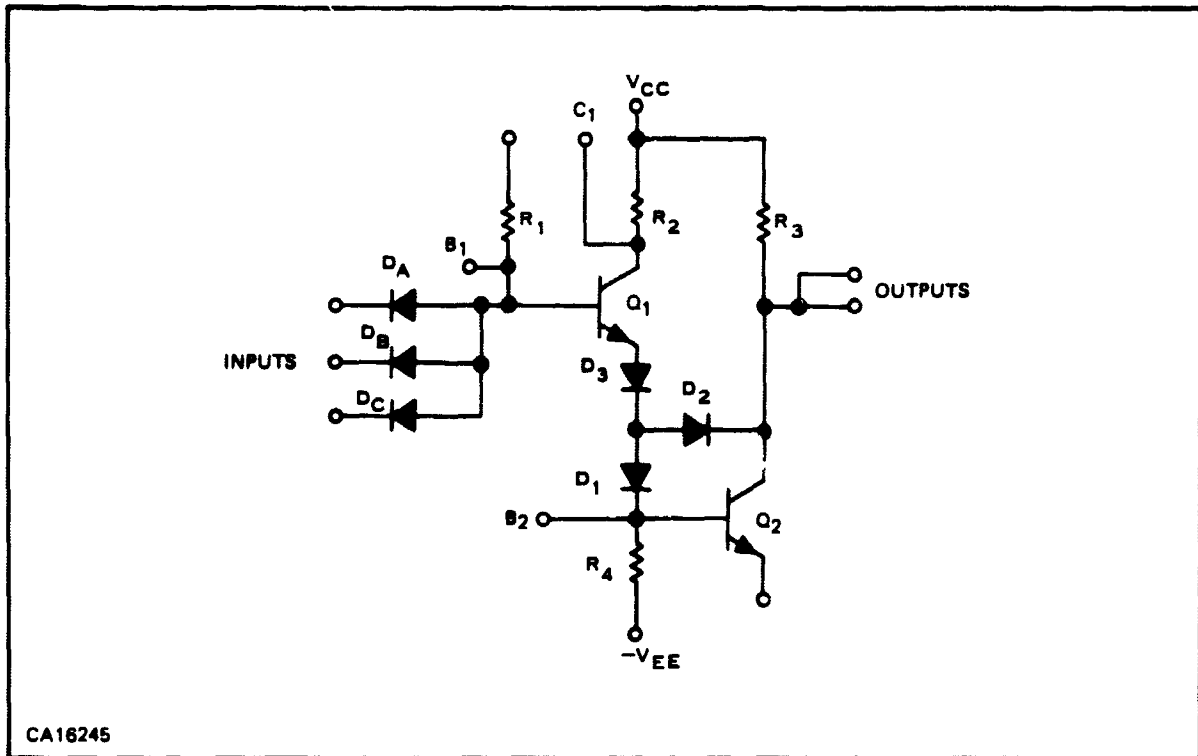


Figure 42. Basic NAND Gate Circuit

voltage is high, Q_1 is biased to saturation. Diodes D_1 and D_3 are always forward biased. When the input voltage is small, the emitter junction of Q_2 is reverse biased because the voltage at the base of Q_2 is fixed by the sum of the input voltage and the voltage across one of the conducting input diodes, minus the sum of the junction voltages of D_1 and D_3 and the emitter junction of Q_1. With the emitter junction of Q_2 reverse biased, the collector current of Q_2 is nearly zero, and the output voltage at the collector of Q_2 is approximately the supply voltage, V_{CC}. Diode D_2 is reverse biased.

When the input voltage is high for all input diodes, diodes D_A, D_B and D_C are reverse biased. Transistor Q_1 conducts more current, and the voltage at the base of Q_2 rises above zero. Q_2 starts drawing base current, causing collector current through the load to decrease the output voltage. If the output voltage decreases to less than the base voltage of Q_2, diode D_2 is forward biased and part of the available base current for Q_2 is shunted to the collector. The base current of Q_2 is controlled in this fashion to keep Q_2 at the edge of saturation without extreme overdrive. The switching time of Q_2 is also enhanced by preventing hard saturation. When the input voltage is decreased, the output voltage stays relatively constant until D_2 stops conducting, then increases toward V_{CC}.

The design of the circuit with terminal R_1 connected to V_{CC} is given in this section. Resistors R_1 and R_2 are designed in terms of the minimum current gains of transistors Q_1 and Q_2 and the mininum acceptable fan-out number, N, of the circuit. The fan-out number is the ratio of the maximum output load current when Q_2 is ON to the maximum input current when Q_2 is OFF. The maximum input current is calculated from

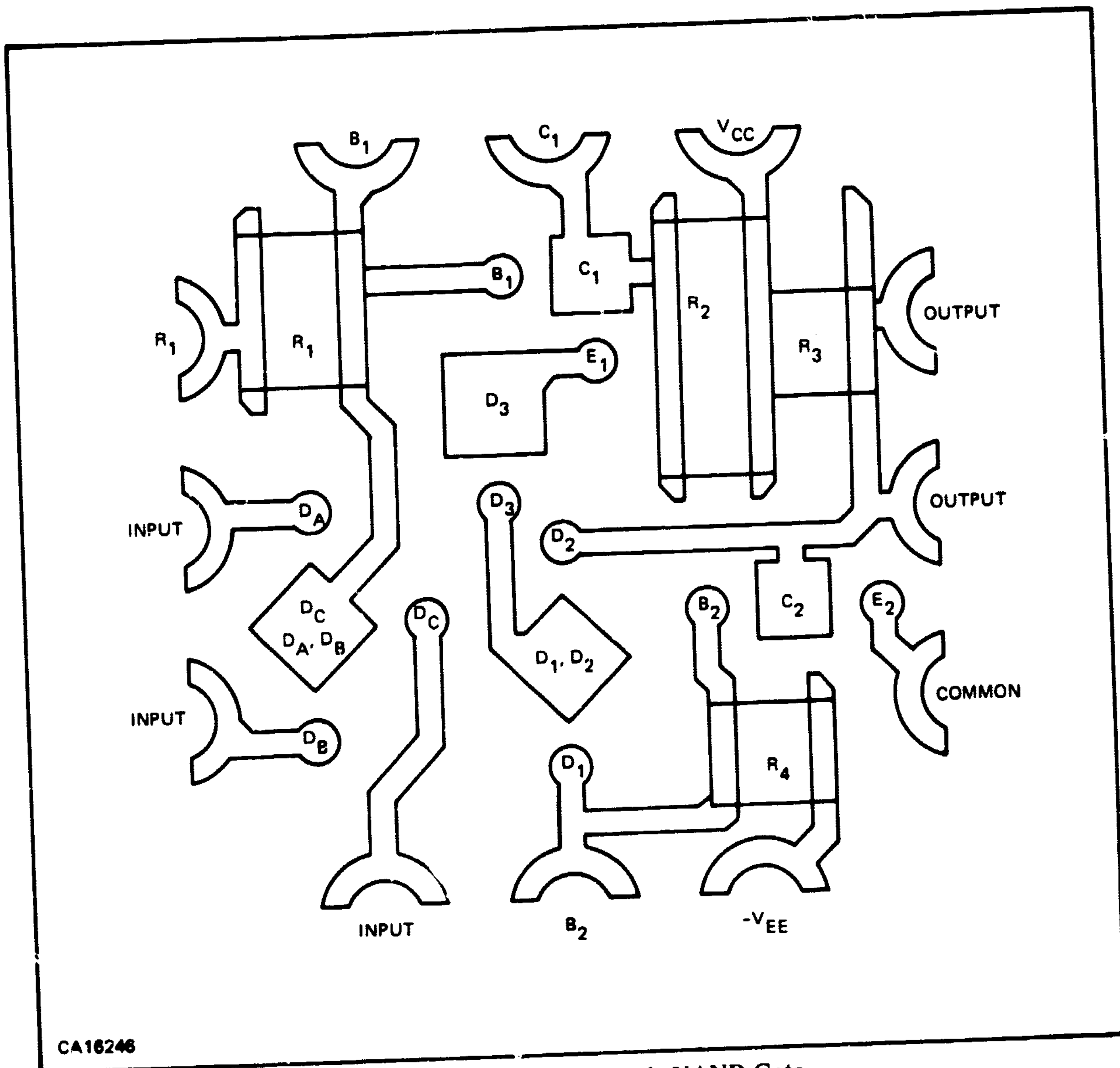


Figure 43. Layout for Basic NAND Gate

$$V_{R1(OFF)} = V_{CC} - V_{DA} - V_{IN} \tag{44}$$

$$I_{IN} = \frac{V_{R1(OFF)}}{R_1} - \frac{I_{E1}}{1 + h_{FE_1}} \tag{45}$$

If the gain of Q_1 is larger, the second term in Equation (45) can be neglected, giving

$$I_{IN} = \frac{V_{R1(OFF)}}{R_1} \tag{46}$$

When all inputs are high enough to turn Q_2 ON, the relations shown hereafter hold for minimum gain transistors. Currents through diodes D_A, D_B, D_C, and D_2 are negligible. The collector current of Q_2 is given by

$$I_{C_2} = I_{R_3} + I_L \tag{47}$$

where I_L is the maximum load current. Other circuit equations are

$$I_L = N\ I_{IN} \tag{48}$$

$$I_{B_2} = \frac{I_{C_2}}{h_{FE_2}} \tag{49}$$

$$I_{E_1} = I_{B_2} + I_{R_4} \tag{50}$$

If it is assumed that Q_1 is not in hard saturation for a low gain transistor, then

$$I_{B_1} = \frac{I_{E_1}}{1 + h_{FE_1}} \tag{51}$$

$$I_{B_1} = \frac{V_{R_{1(ON)}}}{R_1} \tag{52}$$

$$V_{R_{1(ON)}} = V_{CC} - V_{B_1} - V_{D_3} - V_{D_1} - V_{B_2} \tag{53}$$

These equations can be combined to form

$$N = \frac{h_{FE_2}(1 + h_{FE_1})\, V_{R_{1(ON)}}}{V_{R_{1(OFF)}}} - \frac{R_1\ (I_{R_3} + h_{FE_2} \cdot I_{R_4})}{V_{R_{1(OFF)}}} \tag{54}$$

Equation (54) is the final design equation. A selection of values for R_1 and minimum equal values for h_{FE1} and h_{FE2} are assumed. From experimental results, with $V_{CC} = -V_{EE} = 6$ V and $R_3 = R_4 = 5$ kΩ, design values are:

$$V_{R_{1(ON)}} = 2.8\ \text{V}$$

$$V_{R_{1(OFF)}} = 4.5\ \text{V}$$

$$I_{R_3} = 1.07 \text{ mA}$$

$$I_{R_4} = 1.33 \text{ mA}$$

$$V_{R_{2(ON)}} = 3.1 \text{ V}$$

Table IX gives values of N as a function of $h_{FE\ MIN}$ and R_1.

Table IX. Fan-Out Factor "N"

Assumed Value of $h_{FE\ MIN}$	N (For assumed values of $h_{FE\ MIN}$ with R_1 as indicated)		
	$R_1 = 3\ k\Omega$	$R_1 = 3.5\ k\Omega$	$R_1 = 4\ k\Omega$
2.0	1.25	0.83	0.42
2.5	2.51	2.03	1.54
3.0	4.09	3.53	2.97
3.5	5.98	5.35	4.71
4.0	8.18	7.47	6.76

Resistor R_2 is given by

$$R_2 = \frac{R_1 \cdot V_{R_{2(ON)}}}{h_{FE\ MIN} \cdot V_{R_{1(ON)}}} \quad (55)$$

Small values for R_1, indicating large values of N in Table IX, give large values for the collector current of Q_2. Choosing values for $h_{FE\ MIN}$ and R_1 which exceed the desired fan-out of three but demand a reasonable value for I_{C_2}, the following values are obtained:

$$h_{FE\ MIN} = 3$$

$$R_1 = 3.5 \text{ k}\Omega$$

$$R_2 = 1.3 \text{ k}\Omega$$

$$I_{C_{2MAX}} = 5.6 \text{ mA}$$

A breadboard evaluation of this circuit at 100°C and 270°C gives the characteristics shown in Figure 44. A 1.2 kΩ resistor connected between V_{CC} and the circuit output is used to simulate a fan-out of three. As shown in Figure 44 an input signal equal to the output of an ON gate will not operate the circuit (thus giving a safe region of operation), and an input substantially less than V_{CC} is sufficient for complete switching.

3. Circuit Tests

The resistor values obtained on the delivered circuits were measured before circuit assembly. Resistors R_1 and R_2 were near the design values, but R_3 and R_4 values in the 3 to 4 kΩ range rather than 5 kΩ were obtained. After diode and transistor wafers were mounted and bonded, the resistors were remeasured. In several cases the resistances were decreased. Because the resistors were small, an alternate connection was used. Terminal R_1 was connected to C_1 and V_{EE} was decreased from 6 V to 2.5 V. The circuit was tested at 25°C, 100°C, 200°C, and 275°C. Plots of output voltage as a function of input voltage for these temperatures are shown in Figure 45. Input current as a function of input voltage is shown in Figure 46. A fan-out load of three was simulated by a 750-ohm resistor and a silicon diode connected between V_{CC} and the output.

After this test, three circuits were operated at 300°C for 200 hours with the same simulated fan-out. A full-wave, rectified, line-frequency, 6 V signal was connected to the circuits to operate them at 120 Hz. One circuit failed; the remaining two were degraded but still switched at elevated temperatures.

C. THIN-FILM CIRCUITS

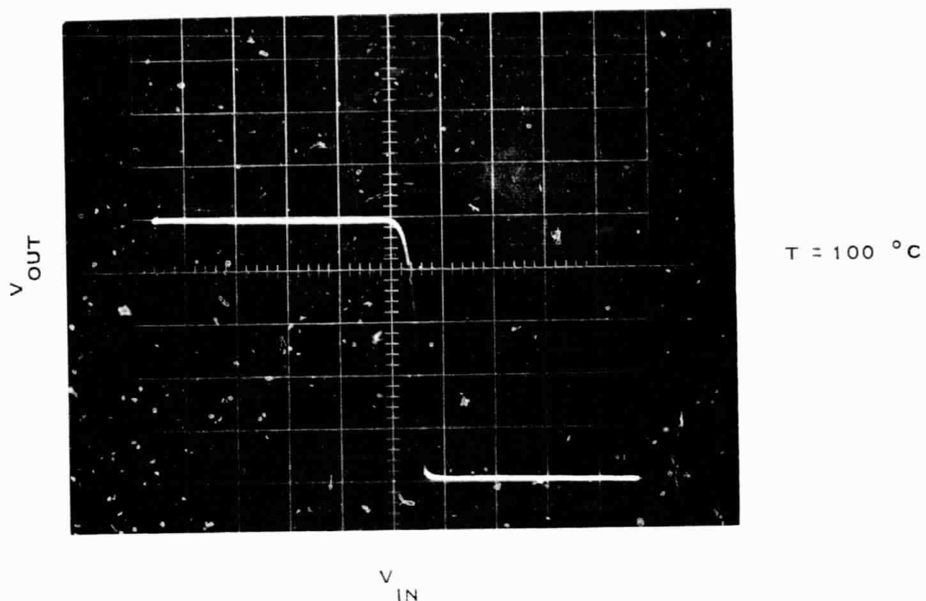
1. Circuit Description

A linear, feedback-pair amplifier has been designed for operation at high temperatures. This circuit requires fewer semiconductor chips than the basic NAND gate, simplifying device assembly. In addition, the circuit to be described will tolerate a wider range of device base-emitter voltages.

Thin-film circuit technology was evaluated for high-temperature applications. Some of the advantages of thin-film circuitry compared to available thick film processes used for the basic NAND gate include improved control of resistor geometries in batch processing, greater density of circuitry, and sheet resistances smaller than required circuit-resistor values. When sheet resistance and circuit resistor values are comparable, as in the thick-film circuit, the nearly square resistor geometries are difficult to control accurately because of conductor leads at the resistor ends.

2. Circuit Design and Operation

The circuit for the feedback-pair amplifier is shown in Figure 47. It is a transimpedance amplifier; that is, the output voltage is proportional to the input current. For high values of transistor current gain, the amplifier gain approaches $-1/R_2$.



VERTICAL: 1 V/DIV
HORIZONTAL: 0.5 V/DIV.

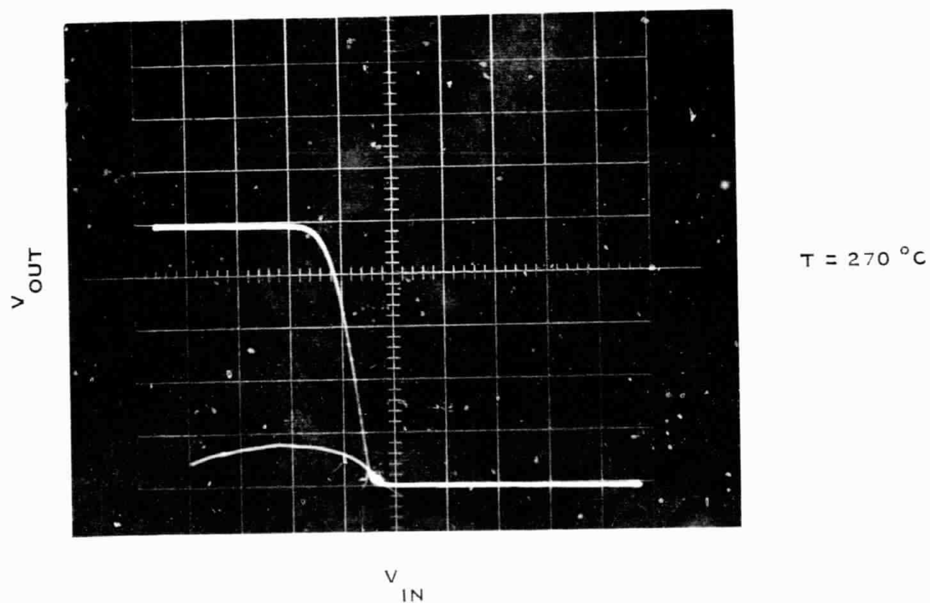


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Figure 44. Characteristics of Modified NAND Gate

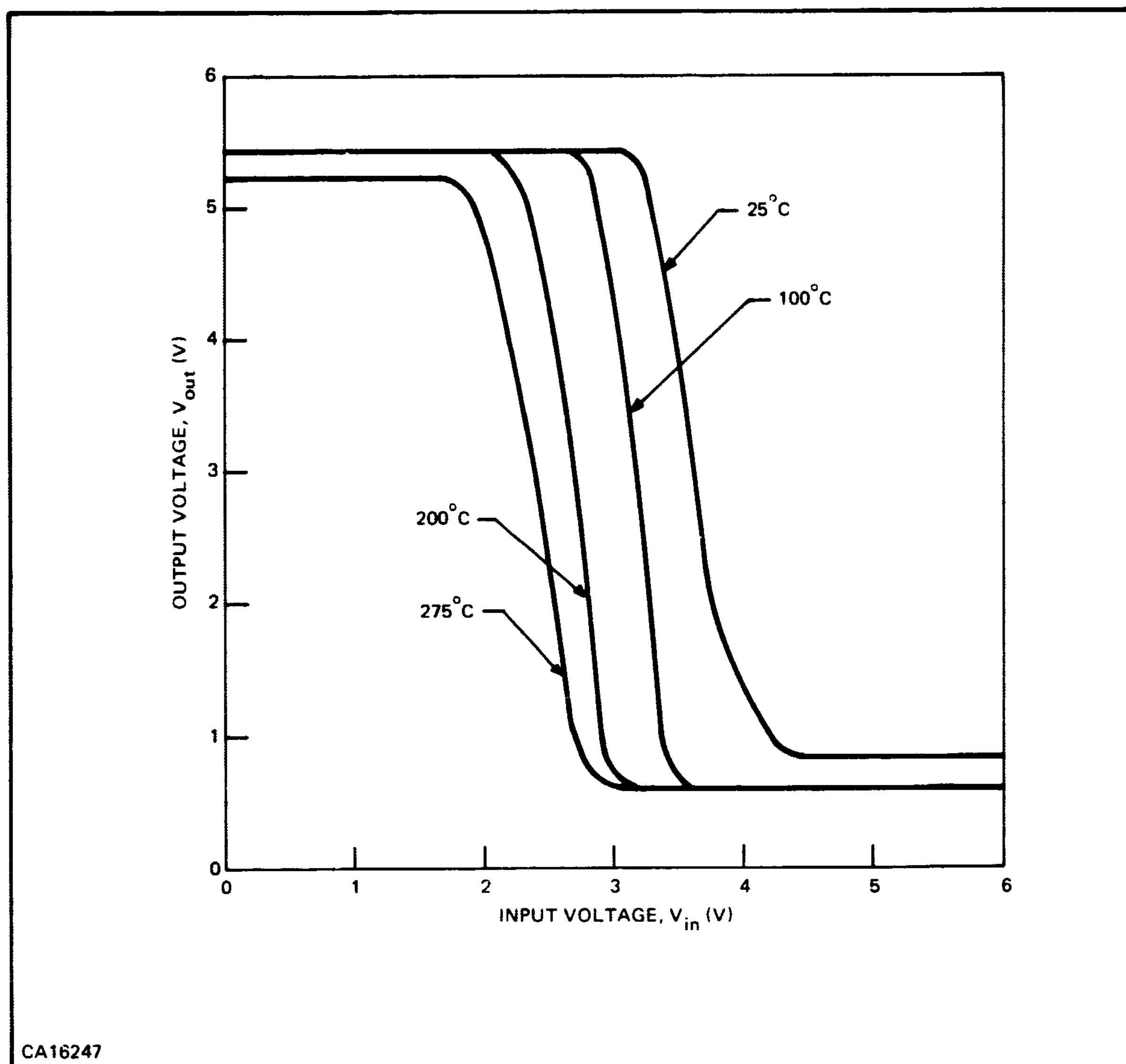

Figure 45. NAND Gate Transfer Characteristics as a Function of Temperature

For convenient dc circuit analysis the signal flowgraph in Figure 47 is used. The results for output voltage and transistor emitter currents can be expressed in terms of the output resistance, R_o, where

$$1/R_o = 1/R_3 + (1+h_{FE2})/R_1 + (1+h_{FE1} + h_{FE1}\, h_{FE2})/R_2 \qquad (56)$$

$$V_o/R_o = -h_{FE1}\,(1+h_{FE2})I_S + (V_{CC} - V_{B2})(1+h_{FE2})/R_1 \qquad (57)$$

$$+ V_{B1}\,(1 + h_{FE1} + h_{FE1}\, h_{FE2})/R_2$$

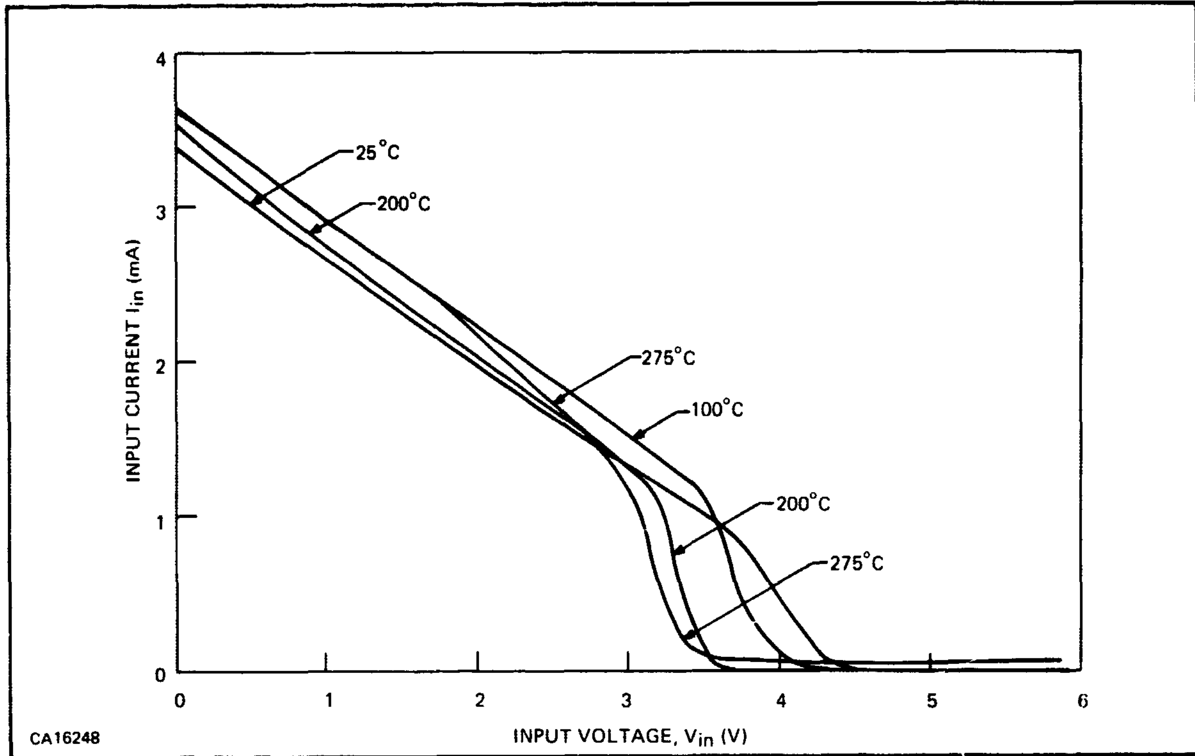

Figure 46. NAND Gate Input Characteristics as a Function of Temperature

$$I_{E1}/R_o = (1/R_2+1/R_3+(1+h_{FE2})/R_1)(1+h_{FE1})I_S + (V_{CC} - V_{B2})(1+h_{FE1})(1+h_{FE2})/R_1 R_2 - V_{B1}(1+h_{FE1})(1/R_3 + (1+h_{FE2})/R_1)/R_2 \quad (58)$$

$$I_{E2}/R_o = - h_{FE1}(1+h_{FE2})(1/R_2 + 1/R_3) I_S + V_{B1}(1+h_{FE2})(h_{FE1}/R_3 - 1/R_1)/R_2 + (V_{CC} - V_{B2})(1+h_{FE2})(1/R_2 + 1/R_3)/R_1 \quad (59)$$

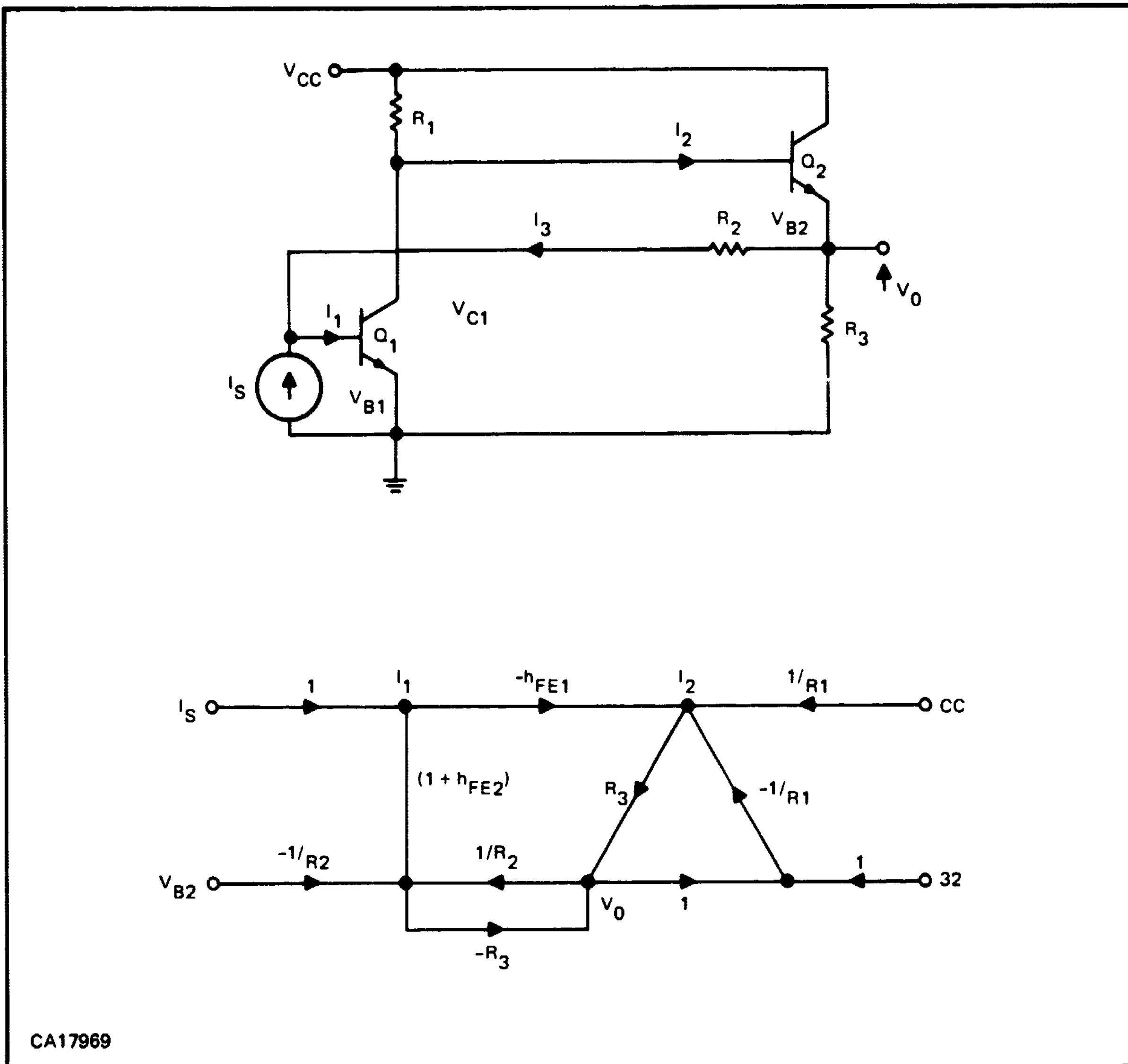

Figure 47. Circuit and Signal Flowgraph for Feedback-Pair Amplifier

For large values of gain these relations reduce to

$$R_o = R_2/h_{FE1}\ h_{FE2} \tag{60}$$

$$V_o = V_{B1} - I_S\ R_2 + (V_{CC} - V_{B2})\ R_2/h_{FE1}\ R_1 \tag{61}$$

$$I_{E1} = R_2\ I_S/R_1 + (V_{CC} - V_{B1} - V_{B2})/R_1 \tag{62}$$

$$I_{E2} = -(1 + R_2/R_3)\ I_S + V_{B1}/R_3 + (V_{CC} - V_{B2})(1 + R_2/R_3)/h_{FE1}\ R_1 \tag{63}$$

With no signal ($I_S = 0$) the emitter current of Q_2 is determined by the base-emitter voltage of Q_1 and R_3. The emitter current of Q_1 is determined by both base-emitter voltages, V_{CC} and R_1. While these currents will change as the base-emitter voltages change with temperature, the transistors will continue to be biased into their active regions and function as small-signal amplifiers.

The dynamic range of the amplifier tends to favor negative polarity current inputs. The limit of linear operation for positive inputs is reached when the emitter current of Q_2 goes to zero, and is given by

$$I_{S(max\ pos)} = V_{B1}/(R_2 + R_3) \tag{64}$$

Similarly, the maximum negative input excursion is reached when the emitter current of Q_1 goes to zero:

$$I_{S(max\ neg)} = -(V_{CC} - V_{B1} - V_{B2})/R_2 \tag{65}$$

The frequency response for moderate to large values of R_2 is determined by R_2 and C_{cb1}, the collector junction capacitance of Q_1. The gain as a function of frequency may be written as

$$v_o/i_s = -R_2/(1 + j\omega\ R_2\ C_{cb1}) \tag{66}$$

At frequencies much greater than $f_o = 1/2\pi\ R_2\ C_{cb1}$ (or for small values of R_2) other critical time constants can be important,[36] but for the values to be used in this work Equation (66) will suffice. Analogous to the gain-bandwidth product in amplifiers with dimensionless current or voltage gains, a transimpedance-bandwidth product (TBP) can be defined for this amplifier.

$$TBP = 1/2\pi\ C_{cb1}\ \Omega Hz \tag{67}$$

From switching time and frequency response measurements made earlier with GaAs transistors, the frequency response may be temperature dependent, improving with increasing temperature, in which case Equation (66) may not predict frequency response at room temperature.

The values selected for R_1, R_2, and R_3 are

$R_1 = 2.25\ K\Omega$

$R_2 = 3.0\ K\Omega$

$R_3 = 600\ \Omega$

Substituting these values in Equations (56) and (57)

$$1/R_o = 1.67 + (1 + h_{FE2})(.44) + (1 + h_{FE1} + h_{FE1} h_{FE2})(.33)$$

$$V_o/R_o = - h_{FE1} (1 + h_{FE2}) I_S$$

were contributions to the value of V_o when $I_S = 0$ are neglected. For $h_{FE1} = h_{FE2} = 3$ the gain is within 6 dB of the maximum possible value, and, with $h_{FE1} = h_{FE2} = 6$, within 3 dB. It can be seen that, for moderate values of R_2, high-gain transistors are not required. This circuit can be used with NPN or PNP GaAs or silicon transistors.

Figure 48 is a composite drawing of the patterns designed for the feedback-pair amplifier.

Figure 49 shows a photograph of a circuit with 2 GaAs transistors before the gold wire connections are made.

3. Circuit Tests

The first part of the testing was concerned with possible changes of the resistor values during circuit assembly. The resistors were checked between each step in the assembly with the result that all changes are small enough to be neglected. The resistors also proved to be stable during temperature cycling experiments between 300°C and 25°C. The life tests of circuits with no transistors incorporated were performed at 300°C for 1000 hours and at 400°C for 500 hours. During these tests the resistors were biased for a current density of 0.6 mA/mil-width. During the 300°C test the typical increase in resistance was 1 percent with a maximum value of 6 percent. The resistor-value increases during the 400°C test were below 10 percent. From these results can be concluded that these resistors are stable for operation at 300°C over longer periods of time and suited for operation at 400°C for at least 500 hours.

Some feedback-pair amplifier circuits were assembled with GaAs transistor wafers and tested at room temperature and at 300°C. Results of frequency response measurements are shown in Figures 50 and 51. In Figure 50, which shows the frequency dependence of the transimpedance, the transimpedance at 250°C begins to decrease at a relatively low frequency. At high temperatures there is little dependence of transimpedance on frequency. This result agrees with the results obtained in switching speed measurements in which the switching speed decreases with increasing temperatures. Both results are attributed to a large, current dependent collector capacitance, called diffusion capacitance, which is observed in GaAs transistors. Diffusion capacitance decreases with temperature, reducing negative feedback and resulting in improved frequency performance.

The input impedance characteristic, shown in Figure 51, depends on amplifier gain. The input impedance is the parallel combination of the input impedance of transistor Q_1 and R_2/A, where A is the voltage gain of the circuit. Because the circuit gain at 25°C decreases with increasing frequency, R_2/A increases, as shown.

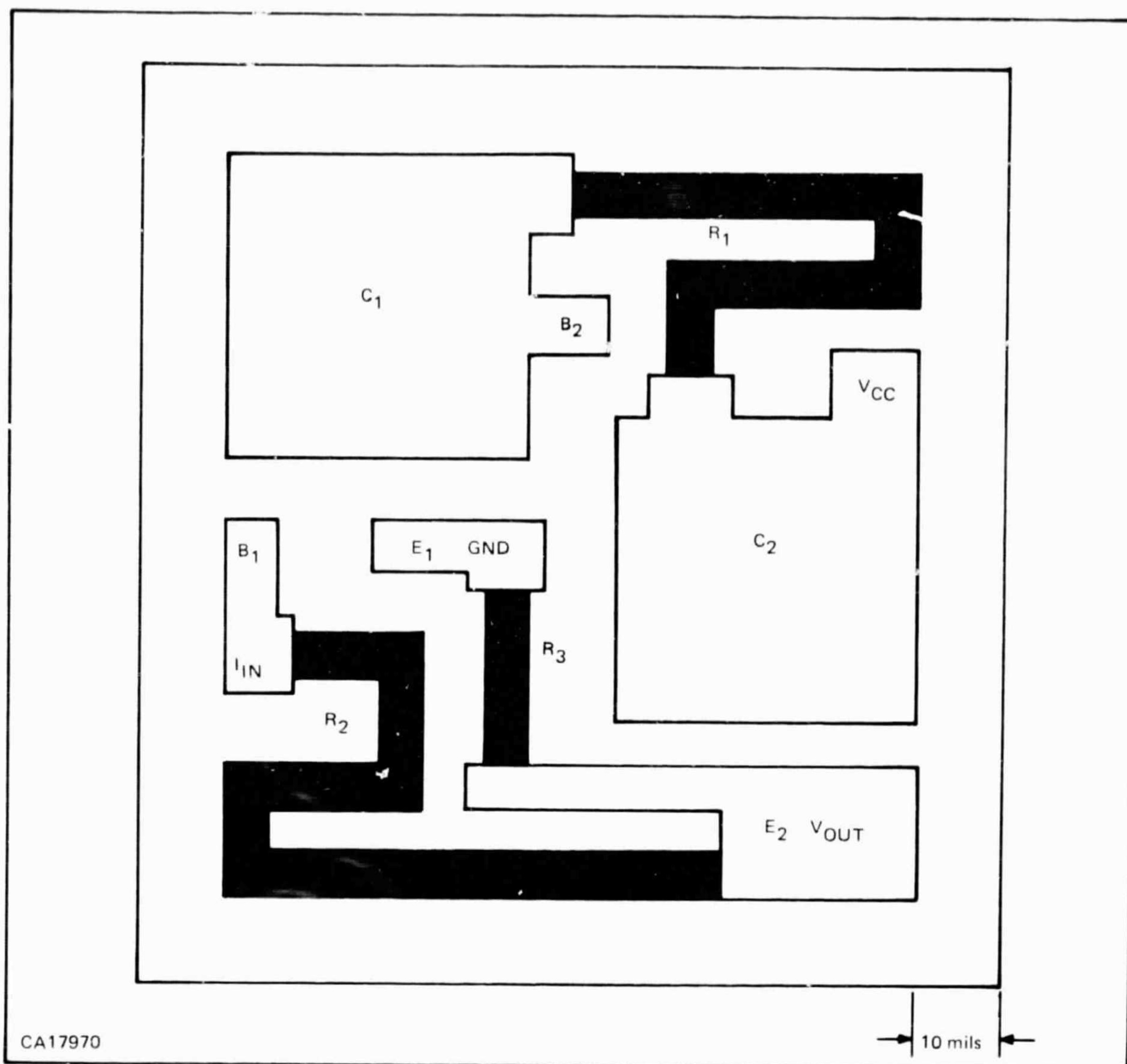

Figure 48. Thin-Film Layout for Feedback-Pair Amplifier

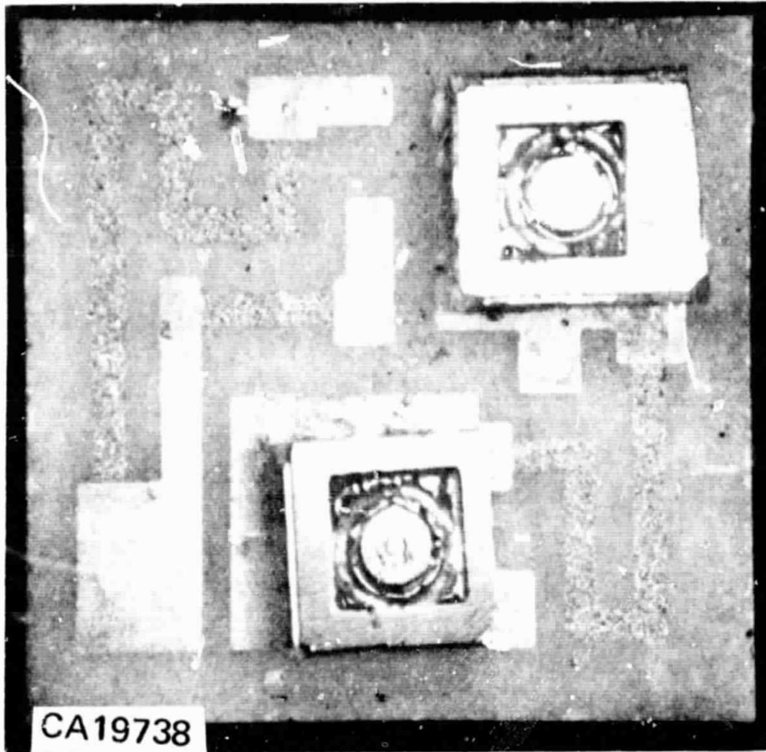

Figure 49. Photograph of the Thin-Film Circuit with 2 GaAs Transistors (Before Wire-Bonding)

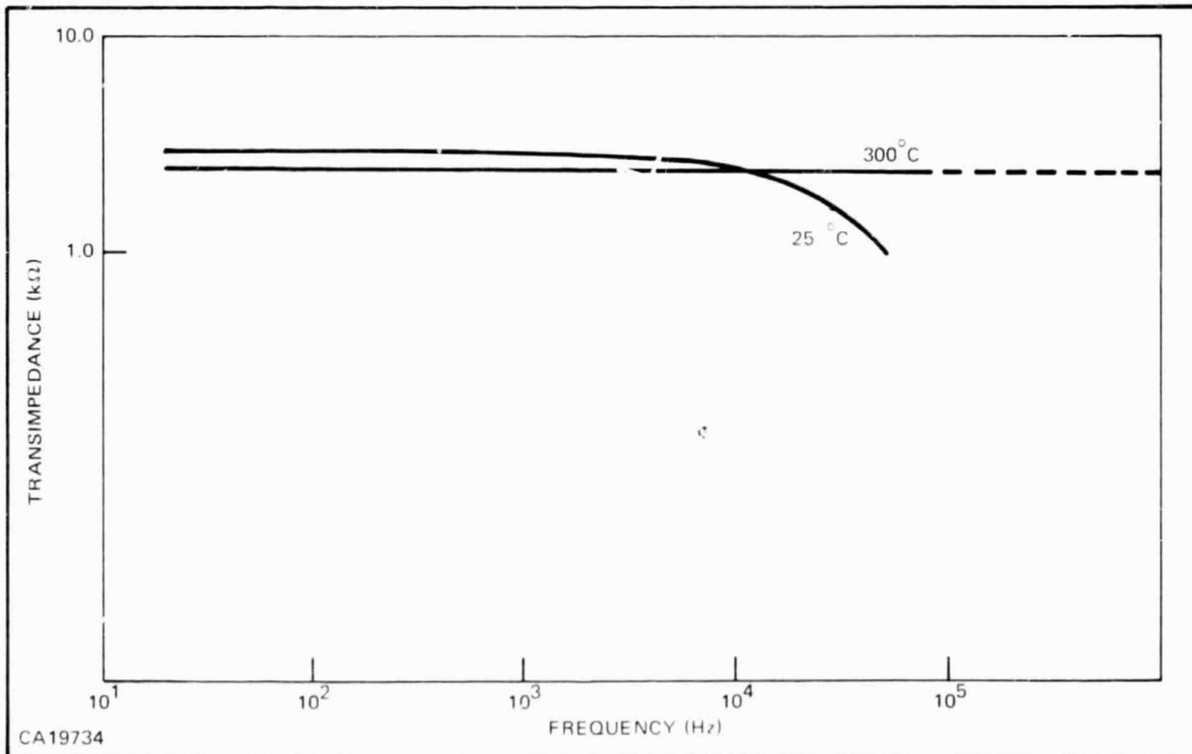

Figure 50. Transimpedance versus Frequency of a Thin-Film Feedback-Pair Amplifier at 25°C and 300°C

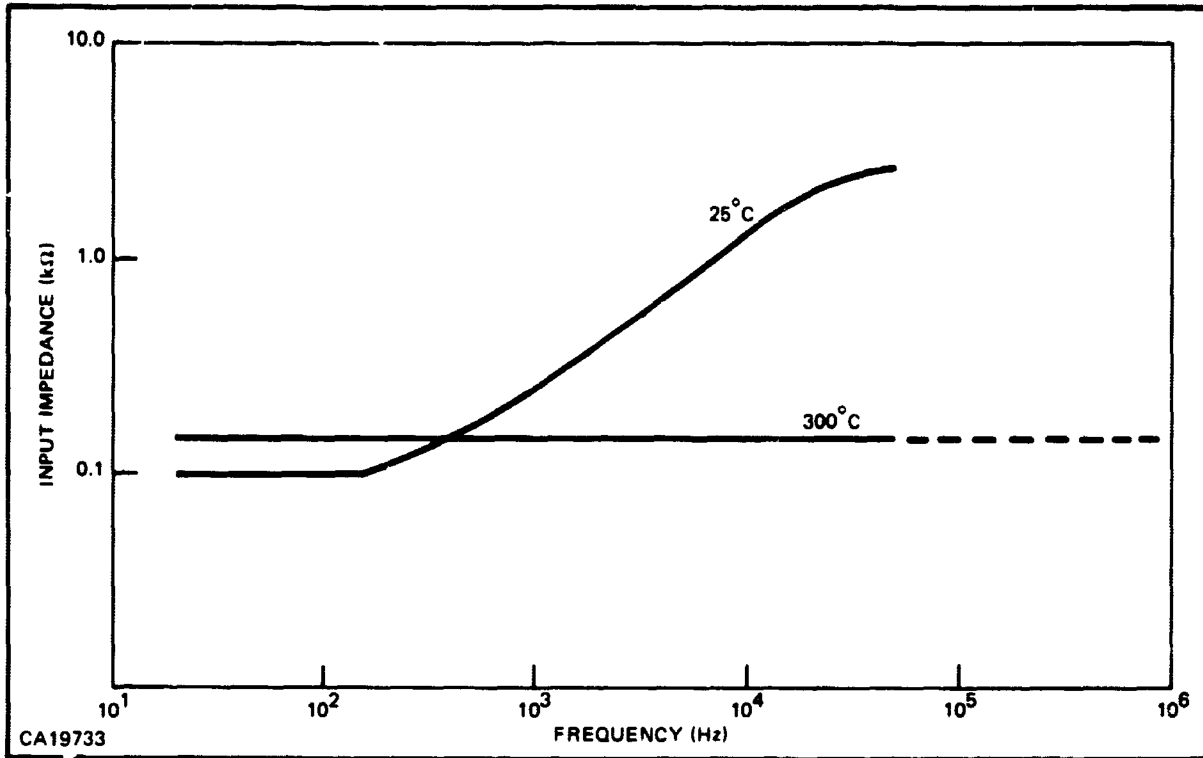

Figure 51. Input Impedance versus Frequency of a Thin-Film Feedback-Pair Amplifier at 25°C and 300°C

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SECTION VIII

SUMMARY

A study was made on the feasibility of operating GaAs devices in high-temperature microelectronic circuits. Thick-film and thin-film circuits were fabricated utilizing GaAs transistors and diodes. To compare the high-temperature properties of various types of GaAs devices, GaAs N-P-N and P-N-P devices were studied as well as GaAs Schottky-barrier field-effect transistors. GaAs diodes were diffused into P-type and N-type GaAs to evaluate the dependence of the high-temperature voltage-current characteristics on fabrication methods. The following list summarizes the variables introduced in the manufacturing techniques for GaAs transistors and diodes:

Substrate Materials

I. Czochralski-grown bulk material
   - a) Silicon-doped material grown in a sealed puller
   - b) Cadmium-doped material.

II. Epitaxial Material
   - a) Material grown in a halide transport system
   - b) Material grown in a water-vapor transport system
   - c) Material grown in an elemental-source vapor phase system
   - d) Solution-grown epitaxial material.

Doping Elements

1) Substrate: tin, sulfur, sulfur/cadmium, silicon, germanium, tellurium, cadmium
2) Base: magnesium, zinc, sulfur, cadmium
3) Emitter: sulfur, zinc

Transistor Fabrication

1) Planar devices (ring-dot configuration)
2) Planar devices with expanded contacts over junction areas
3) Mesa devices (ring-dot and stripe configuration).

These variations were introduced into the fabrication process to find out whether the high-temperature performance of GaAs devices depends on the fabrication techniques for device and material or is related to GaAs as such.

No correlation could be found between high-temperature parameters such as the junction leakage current and the type of devices or the fabrication method. Typical leakage current density values were $4 A/cm^2$ at 5 V and 400°C. Lower values have been measured occasionally. Also, the decrease of current gain at high temperature is common to all the devices. Typical 400°C common-emitter current gain values are about 5. The combination of the two parameters in high-temperature circuits leads to poor performance at 400°C.

Operation of GaAs devices at 300°C leads to greatly improved performance. Leakage current density at 5 V for typical devices is $0.2 A/cm^2$, while the common-emitter current gain is about 10. Also the short-term (200 hours) stability is improved. The main difference between 300°C and 400°C is that catastrophic failures rarely occur at 300°C. They do occur at 400°C, particularly during cycling from room temperature to 400°C. Performance degradation at 400° (except for catastrophic failure) is not more severe than that observed at 300°C, as can be seen in Table VIII.

The long-term stability is determined by rediffusion of the transistor junctions. Low-temperature (500°C) diffusion experiments indicate that the base-collector junction moved from a depth of 2 μ to 2.8 μ after a diffusion time of 108 days.

High-temperature electronic microcircuits are affected by the performance of the active elements as described above, and by the performance of the passive components. In our experiments thin-film circuits employing nickel-chromium resistors were more stable than thick-film resistors employing palladium-silver resistors.

Several silicon transistors were tested for comparison with GaAs devices. As a result of these investigations, the temperature ranges for active devices can be defined as follows: a) temperature range below 200°C, silicon devices; b) temperature range from 200°C to 300°C, competition between silicon and GaAs devices, whereby silicon devices at the present time have a performance advantage; c) temperature range from 300°C to 400°C, GaAs devices, provided stability can be improved and the leakage current can be decreased; d) temperature range above 400°C, devices made from other materials such as GaP or SiC.

SECTION IX

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