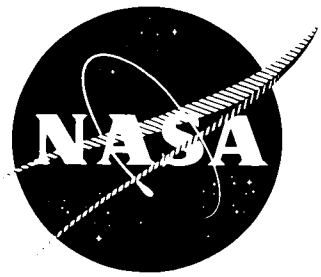

DEVELOPMENT OF ION IMPLANTANTION TECHNIQUES FOR MICROELECTRONICS

By R.G. HUNSPERGER, H.L. DUNLAP, O.J. MARSH,

OCTOBER 1968

PREPARED UNDER CONTRACT NO. NAS 12-124 BY

HUGHES RESEARCH LABORATORIES
A DIVISION OF HUGHES AIRCRAFT COMPANY
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DEVELOPMENT OF ION IMPLANTATION FOR MICROELECTRONICS

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I. INTRODUCTION AND SUMMARY

The potential of the ion implantation process for the fabrication of active device has been demonstrated for semiconductor materials such as silicon and germanium. The objectives of this program have been to demonstrate the usefulness of this process for fabricating devices in higher bandgap materials for device operation at higher temperatures.

In the earlier work, reported in October 1967, it was demonstrated that p-n junctions could be formed in GaAs and SiC by implantation. The effort in this reporting period has been concentrated on evaluating the conduction processes in the implanted layers for various conditions of implantation and subsequent annealing. In particular, implanted layers of Zn, Cd, Sn, and S were evaluated in GaAs and Sb and Bi in SiC.

The cadmium and zinc implants in GaAs were made with 20 kV ions into heated substrates held at 400°C. Electrical characteristics of the implanted layers were studied as a function of isothermal and isochronal annealing cycles. The surface resistivity, average mobility, and carrier concentration in the layer have been determined by Hall measurements; it has been observed that these electrical properties are dependent on post implantation annealing and generally tend to improve significantly with annealing at relatively low temperatures for short times. For example, annealing of cadmium implanted samples at temperatures up to 800°C for less than 1 hour was sufficient to increase mobility from a value of 4 cm^2/V sec to approximately 180 cm^2/V sec, and to reduce sheet resistivity from approximately 8×10^4 Ω/□ to about 6×10^3 Ω/□. Additional annealing for 20 min at 900°C further reduced sheet resistivity to 300 Ω/□ and increased surface carrier concentration to a maximum of $2 \times 10^{15}/cm^2$. The increased carrier concentration eventually resulted in decreased mobility because of impurity scattering.

The tin implants were made at 35 kV into heated substrates held at 400°C. It was found that some means of covering the implanted surface was necessary to prevent outdiffusion of tin during postimplantation annealing. A 10 min anneal at 700°C resulted in a measurable carrier concentration of 6×10^{13} donors/cm^2.

It has been found that room temperature implantation of sulfur into p-type GaAs produces an n-type layer and a resulting p-n junction without requiring any subsequent annealing.

The room temperature sulfur implantations into n-type GaAs have also resulted in a possible n-type ohmic contact. Metal probes to this implanted region do not exhibit any surface barrier behavior normally observed on n-type GaAs surfaces.

It has been found that ion implantation doping results in the generation and diffusion of defect species forming deep trapping levels. The effect of these levels on the electrical characteristics of zinc implanted GaAs diodes has been observed for the case of 70 kV implantation at 400°C into substrates with n-type concentrations ranging from 1×10^{16} to 1.8×10^{18} atoms/cm^3. Capacitance-voltage measurements have indicated the presence of a semi-insulating layer in the diodes, varying in thickness from 0.18 μ for the most heavily doped substrate to 2.7 μ for the lightest. Frequency dependence of the junction capacitance and power law variation of forward current versus voltage have also been observed and are attributed to deep levels.

The direct nature of the bandgap of GaAs has made it an attractive material for use in optical devices and injection luminescence measurements, a powerful tool for analyzing materials preparation and processing techniques. We have included this measurement technique in order to gain more insight into the electrical nature of implanted regions. A broad emission band around 1.25 μ was observed in junction devices prepared in a similar fashion to those which showed the presence of an i region. Annealing of such diodes to temperatures as high as 900°C resulted in the emergence of a second emission peak at 0.85 μ, very near the expected "band edge radiation." These diodes show low radiation efficiency compared with devices prepared by standard techniques. The presence of the i region may be responsible for the low efficiency and our objectives are to eliminate or control this i region in the hope that more efficient devices can be made.

Damage studies in implantation in GaAs using the Rutherford scattering technique show that GaAs anneals in a significantly different manner from equivalently implanted silicon. Such studies as these may lead to our understanding, control, and elimination of the deep centers observed in the hot implanted diodes.

Examination of the annealing of damage in zinc implanted GaAs by Rutherford scattering measurements indicates anneal stages at 75°C and 200 to 400°C. Heavy implants still show considerable damage after 600°C anneals.

Our previous results in SiC showed that n-type layers could be obtained by implanting antimony. We have extended this work to include bismuth implants.

Hall measurements on 25 kV antimony implanted layers in p-type α-SiC indicate an electron mobility of 9 cm^2/V-sec and surface donor density of $8 \times 10^{13}/cm^2$. The samples had been implanted at 500°C and annealed for 30 sec at 1500°C. Considerable attention has been devoted to the etching behavior of SiC. Such attention is important for two reasons: (1) good p-n junction current-voltage behavior is dependent on well-etched surfaces, and (2) the etching characteristics of implanted layers may be (and indeed appear to be) different from those of surfaces resulting from other types of doping processes.

Bismuth implants into SiC produce n-type regions after 1000°C anneals. Good ohmic contacts are possible with bismuth implants. A compression bond contact technique has been developed which appears to result in excellent contacts.

We have had to retrace our steps in implant studies in SiC and attempt to evaluate the "as grown" β-SiC. Many unexplainable results obtained during evaluation of implanted samples can be related to the original material, as this material appears to contain grown in p-n junctions. A new source of better-characterized α-SiC has been found and material has been purchased for these studies.

A paper entitled "Electrical Characteristics of Ion Implanted Gallium Arsenide," by R.G. Hunsperger and O.J. Marsh, was presented by R.G. Hunsperger in the session on Electron and Ion Beams in Science and Technology, Ion Beams and Microelectronics, at the Electrochemical Society Meeting, Boston, Massachusetts, May 7, 1968. A major part of the information presented resulted directly from the investigation performed on this contract and reported in Quarterly Progress Report No. 6. Both authors visited with the technical monitors, Dr. John Shier and Dr. K. Behrndt, while in Boston for the Electrochemical Society Meeting.

A paper entitled "The Presence of Deep Levels in Ion Implanted p-n Junctions in GaAs and Their Effect on the Electrical Characteristics," by R.G. Hunsperger, O.J. Marsh, and C.A. Mead, was presented at the IEEE Solid State Device Research Conference, Boulder, Colorado, June 17, 1968. The material presented in this paper resulted from work performed during the present report period and is discussed in detail in this report.

II. IMPLANTATION STUDIES IN GALLIUM ARSENIDE

A. Gallium Arsenide Surface Protection

In order to extend the study of the properties of ion implanted layers to samples which were annealed at temperatures above 600°C, it was necessary to develop and implement methods of surface protection. The two major problems associated with annealing of ion implanted GaAs are outdiffusion of the implanted ions, as described in a previous report,[1] and decomposition of the GaAs above 650°C. Covering the sample with a polished wafer of GaAs during annealing not only greatly retards outdiffusion, but also prevents decomposition of the surface at elevated temperature. This technique thus offers a simple alternative to the usual sealing of GaAs in arsenic charged ampoules during annealing.

A third technique which is effective in protecting against decomposition and outdiffusion is to encapsulate the GaAs samples in a layer of SiO_2 which has been either sputter deposited or deposited by reaction of a vapor of tetraethyl orthosilicate with oxygen. The effectiveness of sputter deposited SiO_2 films has been evaluated, using films prepared by a Hughes developed SiO_2 sputtering process (for which we thank Dr. Hugh Garvin and his associates). Polished samples of GaAs have been encapsulated in an 1800 Å thick layer of SiO_2 and annealed at temperatures of 600°C and higher. Both nonimplanted and 35 kV zinc-implanted samples were used in the experiments. The following results were obtained: No samples, either encapsulated or nonencapsulated, exhibited surface damage due to decomposition when observed under 200x magnification after annealing at 600°C for up to 16 hours. Following annealing at 700°C for 16 hours the encapsulated samples had not changed from their initial appearance (Fig. 1(a)), but heavy erosion was apparent on the surface of the nonencapsulated samples (see Fig. 1(b)). The small specks on the surface of the encapsulated sample were present prior to annealing and implantation, and are attributed to the nonuniformity of the bromine-methyl alcohol etch polishing technique which was used. No difference was observed between the behavior of implanted and nonimplanted samples. Both implanted and nonimplanted nonencapsulated samples decomposed about the same amount, and encapsulated samples did not decompose regardless of whether they were implanted. The SiO_2 encapsulation was effective in preventing decomposition up to 800°C; above that temperature, however, the film separated from the GaAs and formed small "bubbles" under which decomposition occurred. Improved surface preparation may enhance adhesion of the film and minimize this problem.

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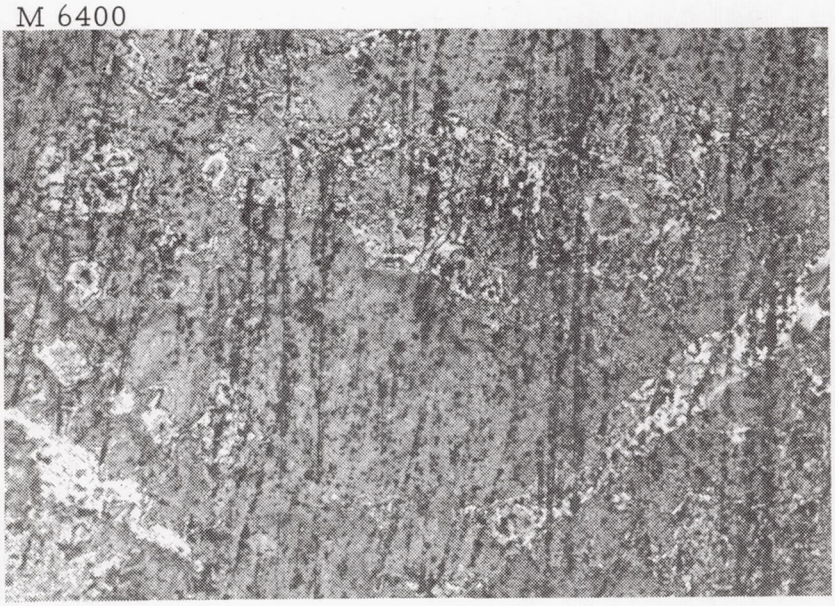
(a)

M 6400



(b)

Fig. 1. Surface of zinc implanted GaAs after annealing at 700°C for 16 hours. (a) SiO_2 encapsulated sample, (b) nonencapsulated sample.

In addition to visual observation of surface erosion, weight change measurements were used to detect decomposition. An encapsulated GaAs sample weighing 65.975 ± 0.003 mg and a non-encapsulated sample weighing 30.280 ± 0.003 mg were annealed first at 600°C and then at 700°C for 16 hours. No weight change was measured for either sample after the 600°C anneal; however, the non-encapsulated sample weighed 30.270 ± 0.003 mg after the 700°C anneal, while the weight of the encapsulated sample remain unchanged.

In order to determine whether the protective SiO_2 layer introduces contaminants by diffusion during annealing, a nonimplanted sample of high resistivity GaAs was totally encapsulated with SiO_2 and annealed at 800°C for 16 hours. Hall measurements showed that the electrical properties of the GaAs had not changed significantly after annealing.

Although all of the samples described in the foregoing paragraphs were coated by sputtering SiO_2, a method for chemical deposition is known. In this process a vapor of tetraethyl orthosilicate is reacted with O_2 in a nitrogen medium at 450°C in the vicinity of the sample. SiO_2 is deposited on the sample as a result of the reaction. It has been reported[2] that the tetraethyl orthosilicate (TEOS) method "produces a better film in terms of density and leakage than sputtering does." We have assembled a system for depositing SiO_2 films from a TEOS vapor and have used such films for protecting the GaAs surface during annealing. The chemically deposited films were found to be superior to the sputtered films because they provided the same protection against decomposition and outdiffusion but were not significantly subject to "bubbling" even at 900°C.

B. Hall Measurements on Zinc- and Cadmium-Implanted GaAs

The arc discharge source described in a previous report[1] has been used to create a beam of 70 kV Zn^+ ions, and high resistivity n-type substrates have been implanted with these ions. The p-type layers obtained by such implantations have somewhat improved electrical characteristics compared with layers created by implantation with 20 kV ions. For example, a 70 kV ion implant at 400°C, when annealed at 600°C for 2 min, produced a p-type layer with ρ_s = 598 Ω/□, μ = 45.8 cm^2/V-sec, and N_s = 2.28 x 10^{14}/cm^2 (as determined by Hall measurements). The corresponding values for a 20 kV ion implanted sample, similarly annealed, where ρ_s = 3100 Ω/□, μ = 19.5 cm^2/V-sec, and N_S = 1.05 x 10^{14} cm^2. The enhanced mobility and reduced surface resistivity of the higher energy implanted layer probably result because most of the dopant ions lie deeper within

the semiconductor crystal and thus are less affected by surface defects. The average projected range of 70 kV zinc ions implanted into GaAs is 283 Å, as calculated from the Lindhard[3] range-energy relations (see Fig. 2). In a substrate of doping $n = 10^{16}/cm^3$ the junction would occur at about 650 Å. In comparison, the average projected range of 20 kV ions is 124 Å and the junction depth in the same substrate would be about 325 Å.

The use of chemically deposited SiO_2 protective covering films has permitted study of the anneal behavior of implanted layers at elevated temperatures without the problem of outdiffusion and decomposition.

Implantations were performed with 20 kV ions using the arc discharge source. The pulsed nature of this source makes it very difficult to measure ion current density. The implanted ion densities ranged from 10^{15} to $10^{16}/cm^2$, as determined by Rutherford scattering measurements.* A heated stage was used to maintain the substrate at an elevated temperature (400°C for most samples) during implantation. After implantation the samples were annealed at various temperatures up to 900°C. The annealing was performed in a nitrogen atmosphere, and for temperatures of 600°C or greater the samples were encapsulated in a film of SiO_2, deposited by chemical decomposition of tetraethyl orthosilicate at 480°C. Below 600°C, extended annealing (24 hours) of the implanted samples revealed no observable decomposition of the GaAs even without the protective SiO_2 film.

The electrical characteristics of the implanted layers (sheet resistivity ρ_s, effective surface carrier concentration N_s, and effective mobility μ) were determined using the van der Pauw[4] Hall measurement technique. A "cloverleaf" shaped mesa was etched onto the samples in order to minimize the effect of contact size on the measurements. The junction between the p-type implanted layer and the n-type substrate provided the necessary electrical isolation of the implanted layer during measurement. All Hall measurements were made at room temperature, after the samples were quenched in air from their anneal temperature.

Figure 3 shows the effect on a typical 20 kV zinc implanted sample of annealing in a series of 10-min anneals from 500°C to 900°C. The sample was implanted at 400°C. The sheet resistivity decreased monotonically as a result of increasing mobility, and above 700°C also as a result of increasing carrier concentration. In the temperature range below 700°C the surface carrier concentration first increased and then decreased somewhat with further annealing. The increase is thought to result from implanted ions moving to electrically active substitutional positions in the lattice, while the decrease is not well understood at present and may be attributed to a number of possible causes. The

*This work is currently in progress, in collaboration with J. Mayer, T. Picraux, and E. Westmoreland, California Institute of Technology.

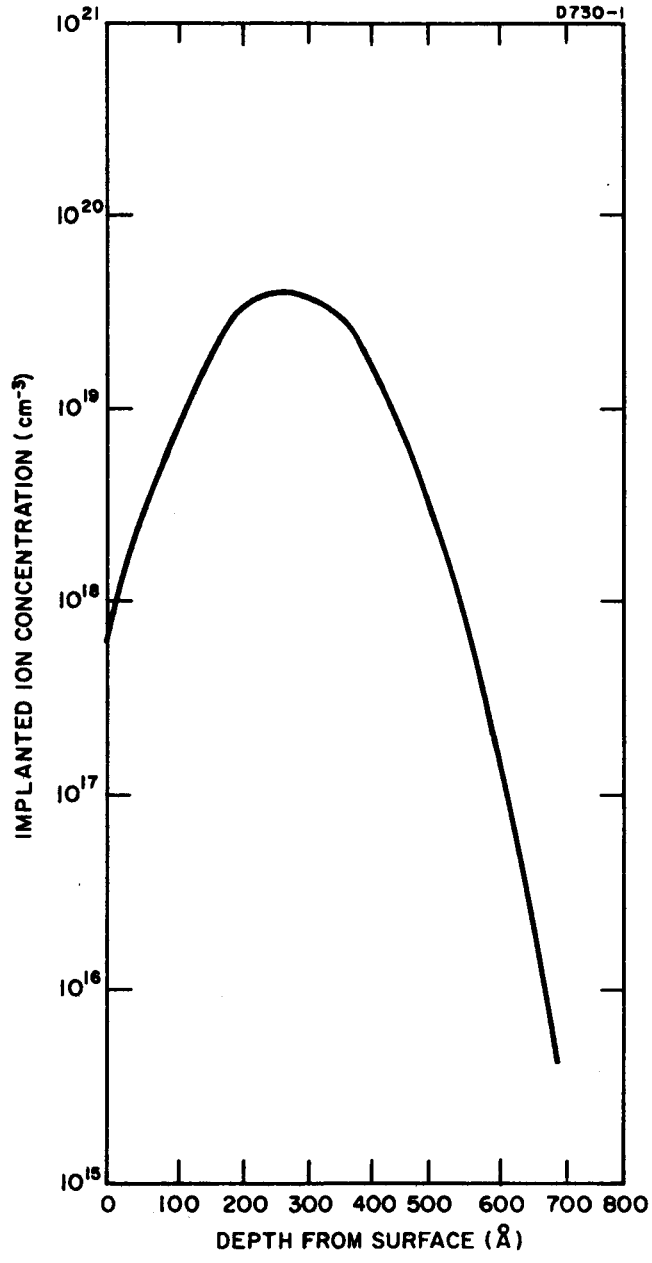


Fig. 2. Concentration versus depth profile for 70 kV zinc ions implanted in GaAs.

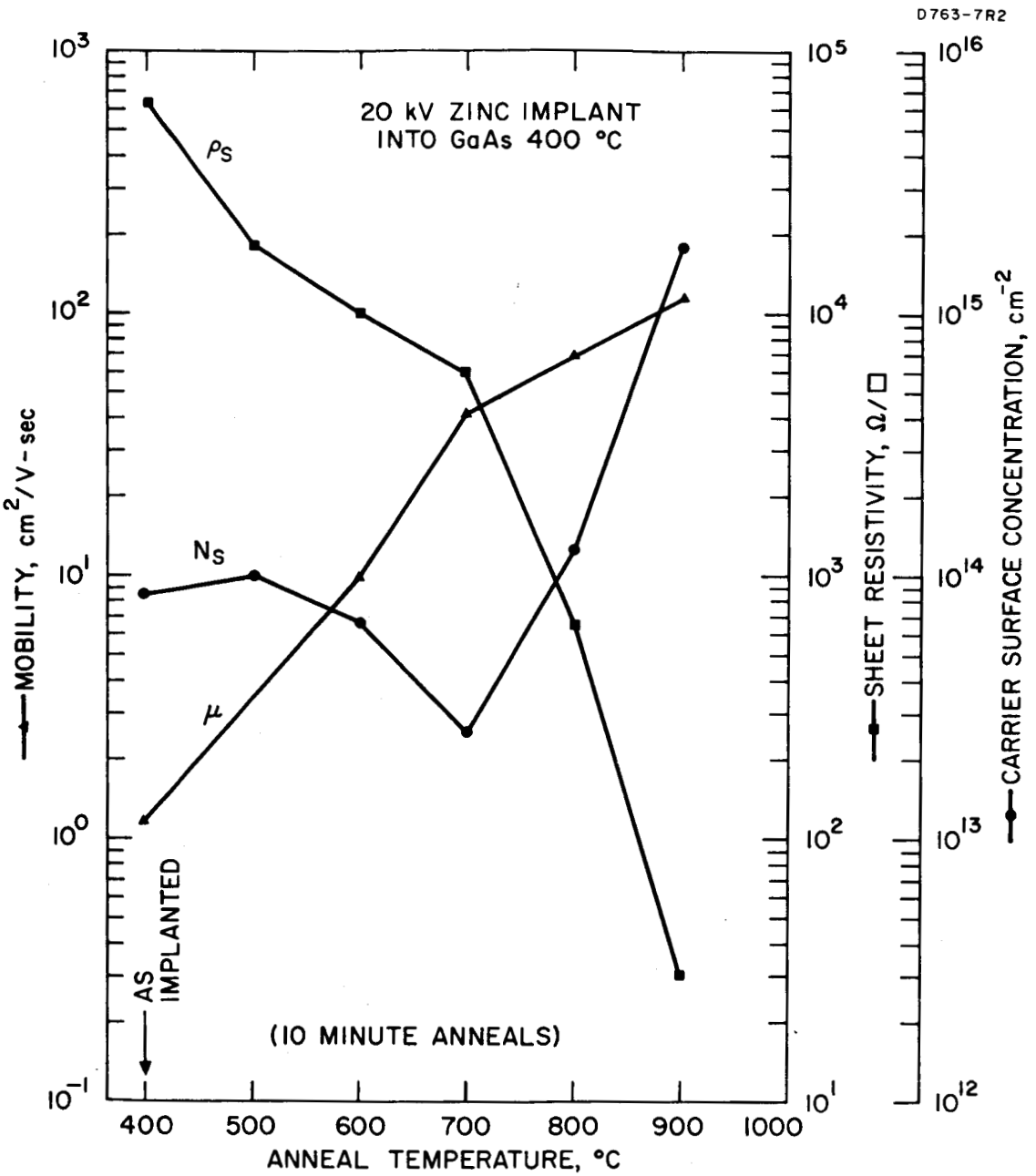


Fig. 3. Effect of isochronal (10 min) anneals on zinc implanted GaAs.

decrease may result from compensation by defect centers which are released when damage clusters dissociate upon annealing. An effect of this type in n-type GaAs has been reported by Fuller, Wolfstern, and Allison.[5] The apparent decrease in effective surface carrier concentration also may result because the mobility in implanted layers is nonuniform with depth, and the calculation of surface concentration from van der Pauw Hall data stresses more heavily the contribution from higher mobility regions. Therefore, if we assume that the distribution and number of electrically active atoms does not change significantly between 500 and 700°C but that the mobility in the more lightly doped regions would increase appreciably, the effective mobility measured in the layer would increase and cause an apparent decreasing in the surface concentration N_s. (This effect has been described by Mayer, et al.[6])

The relatively large increase in carrier concentration above 700°C may be attributed to increased solubility of zinc ($7 \times 10^{19}/cm^3$ at 700°C to $3 \times 10^{20}/cm^3$ at 900°C (Ref. 7)) in conjunction with the fact that the doped layer thickens with annealing because of the very rapid diffusion of zinc in GaAs. For an anneal cycle such as that of Fig. 3, calculations based on the work of Shih, et al.[8] (which considers diffusion from a constant vapor source) predict a total diffusion depth of approximately 90 μ. However, the implanted layer more closely represents diffusion from an infinitesimally thin layer.[9] Theoretical diffusion depths for the case considered herein are approximately 75% as great as those for diffusion from a constant vapor source such as that used by Shih. Assuming that there are sufficient implanted atoms present that the concentration of electrically active (substitutional) zinc per cubic centimeter is constant or increasing with increased solubility, the thickening of the layer due to diffusion would result in a higher measured value for surface concentration per square centimeter.

For a series of isothermal anneals of zinc implanted GaAs, as shown for a typical 20 kV, 400°C implant in Fig. 4, the variation of ρ_s, μ, and N_s with anneal temperature agreed with that observed in the series of 10 min anneals of Fig. 3. In addition, it can be seen from the data of Fig. 4 that much of the change in electrical properties (at temperatures up to 700°C) occurred during the first few minutes of each cycle at a new, higher temperature. Mobility increased to a value of about 150 cm^2/V sec after annealing at 900°C. This behavior contrasts with that of cadmium implanted samples, as shown in Figs. 5 and 6, in that the mobility in the cadmium case peaked after annealing at 800°C and then decreased with further annealing. This difference between the mobility behavior for zinc implants and that for cadmium is believed to result because cadmium diffuses three orders of magnitude more slowly in GaAs than does zinc.[10] Angle lap and stain techniques (using standard Sirtl etch solution as the stain) on the cadmium implanted

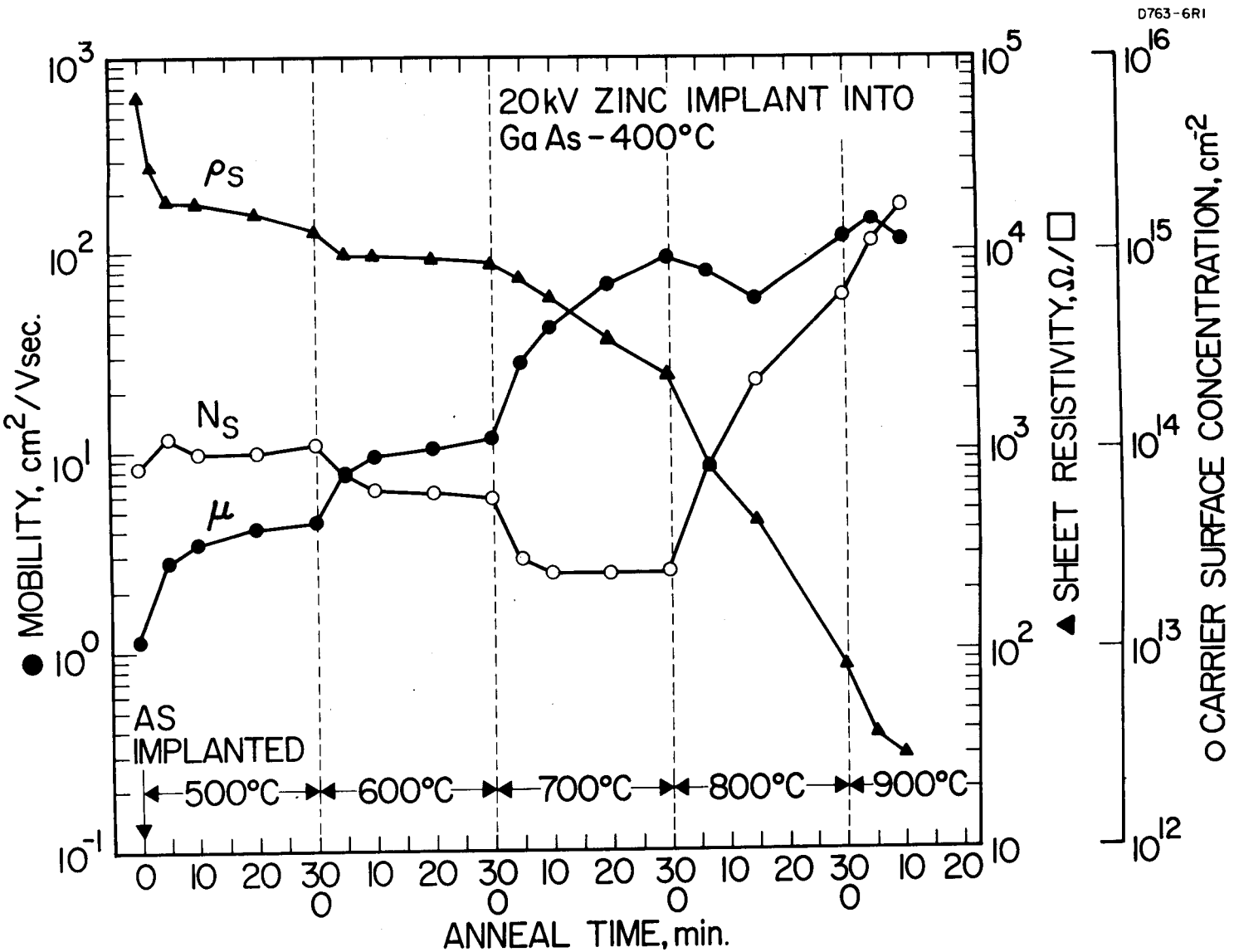


Fig. 4. Effect of isothermal anneal cycles on zinc implanted GaAs.

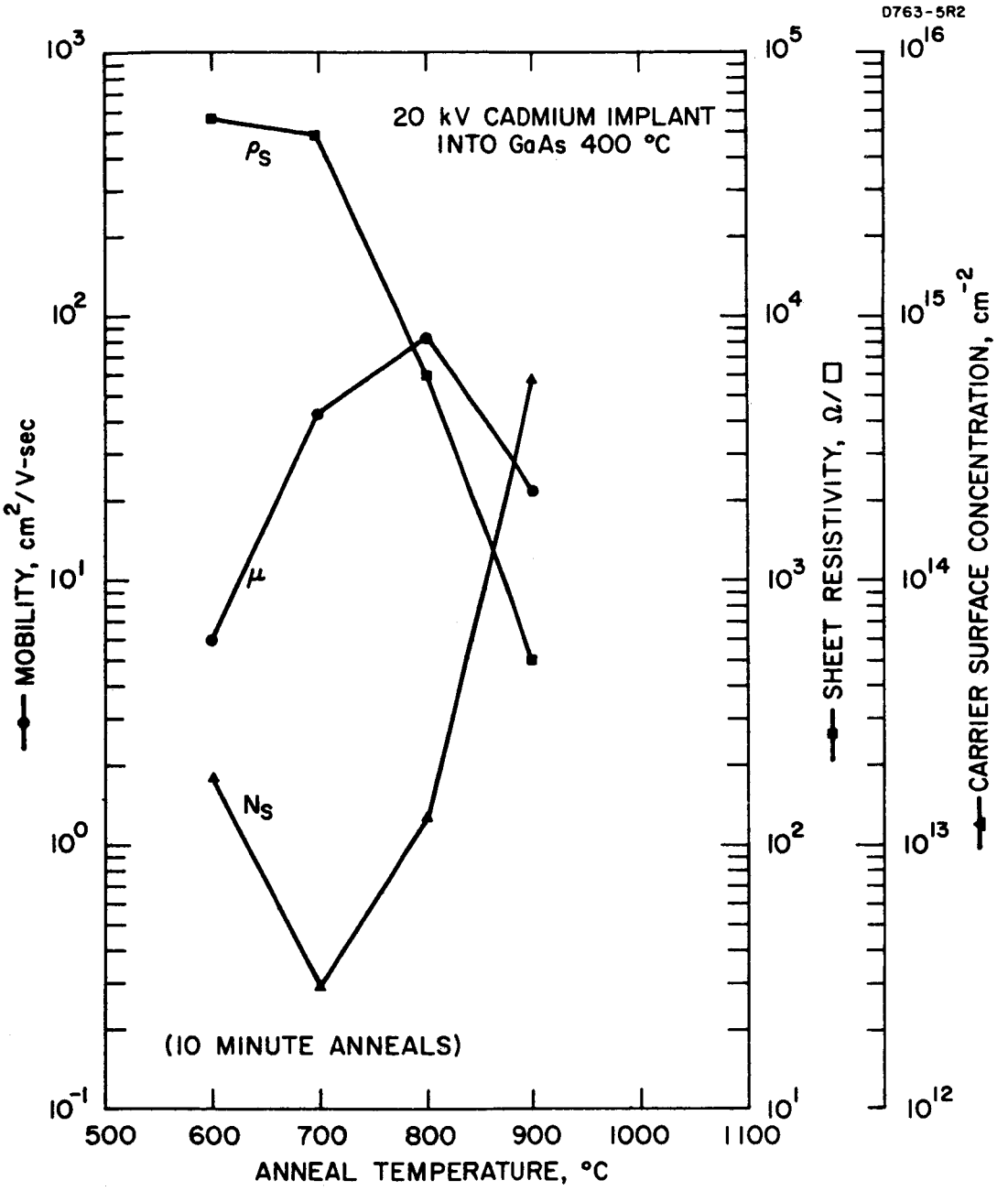


Fig. 5. Effect of isochronal (10 min) anneals on cadmium implanted GaAs.

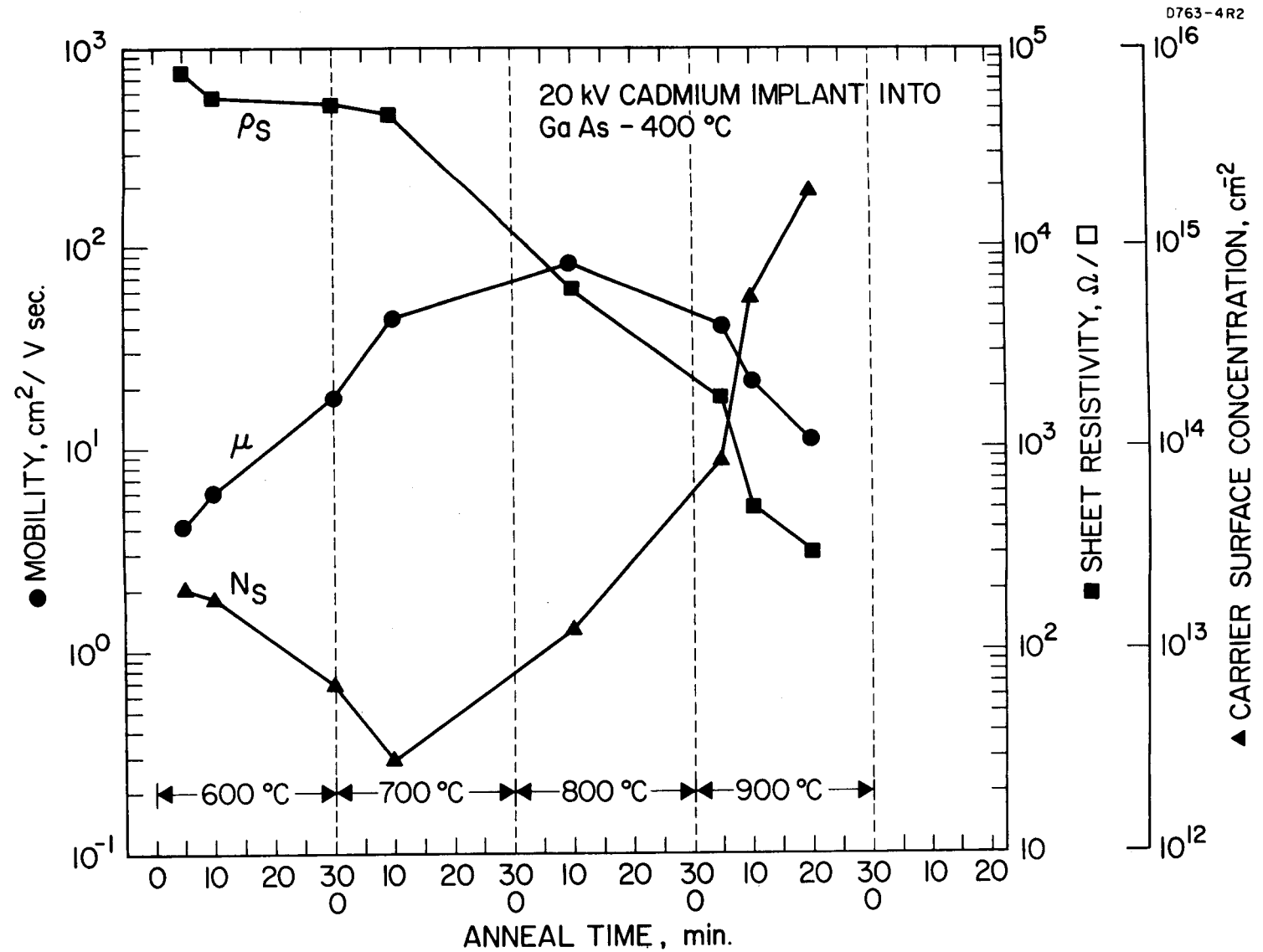


Fig. 6. Effect of isothermal anneal cycles on cadmium implanted GaAs.

samples indicated a junction depth of 0.3 μ after the 600°C annealing and showed negligible diffusion after the 900°C anneal (to within a measurement accuracy of 0.05 μ). The junction depth of 0.3 μ is considerably greater than the 250 Å depth expected from the theoretical Lindhard-Scharff projected range of the ions in amorphous material. It is possible that the larger junction depth results from channeling and/or enhanced diffusion of the ions during implantation. As more cadmium atoms enter substitutional sites (and become electrically active) as a result of increasing solubility at higher temperature, the doped layer does not thicken as in the case of zinc. Hence the concentration of electrically active cadmium atoms per cubic centimeter increases, and ionized impurity scattering tends to decrease mobility. A comparison of the observed decrease in mobility with the Brooks-Herring[11,12] relation for ionized impurity scattering, assuming a lattice mobility of 450 $cm^2/V\text{-}sec$ (Ref. 13), shows that in this case the mobility decreased somewhat more slowly with increasing ion impurity concentration than would be expected (see Fig. 7). This may result because the competing process of damage annealing is reducing defect scattering. It can also be seen in Fig. 7 that mobility remains below the value expected for only ionized impurity scattering until annealing at 900°C for 20 min has been performed. This indicates the presence of lattice damage and resultant defect scattering. Such persistent damage is typical only for the extremely heavy implants (10^{15} to 10^{16} ions/cm^2) used in these experiments. The damage produced by smaller doses anneals at temperatures below 600°C.*

With the exception of mobility, the electrical properties of cadmium implanted samples changed with annealing in a similar fashion to those of zinc implants. The surface carrier concentration increased above 700°C as it did for zinc. In the case of cadmium this increase presumably results almost entirely from an increase in solubility, since negligible diffusion was observed. A further difference between cadmium and zinc implants was that cadmium samples generally had to be annealed to higher temperatures to achieve equivalent values for sheet resistivity and mobility. No measurable p-type layers were obtained in cadmium implanted samples until after annealing at 600°C.

C. n-Type Layer Formation

In most of our work to date on ion implantation doping of GaAs, p-type dopants have been implanted into n-type substrates. This has been done because it is easy to make contact to p-type implanted layers using gold pressure contact probes, while surface barriers form when pressure contact is made to n-type GaAs. These surface barriers make

*As discovered in our current work with Mayer, Picraux, and Westmoreland.

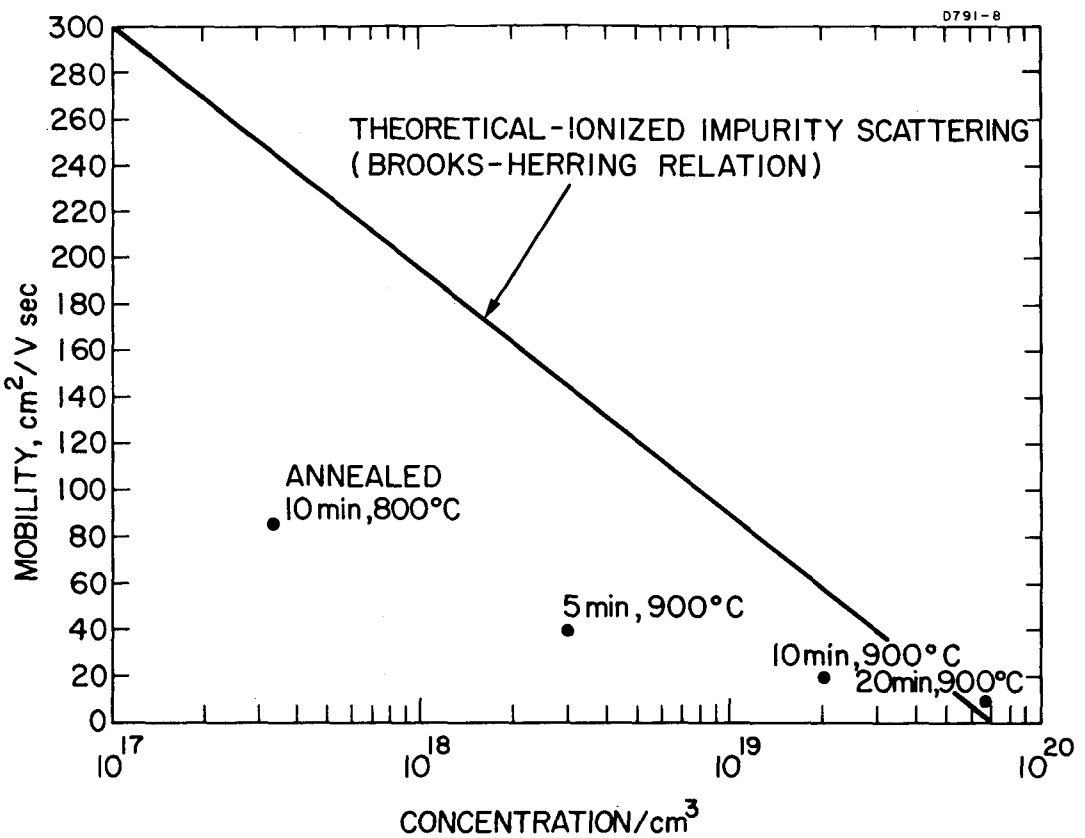


Fig. 7. Variation of mobility with ionized impurity concentration (theoretical curve[11] assumes a hole lattice mobility of 450 $cm^2/V\text{-}sec$[13]). Concentrations were calculated using an implanted layer thickness of 0.3 μ obtained from angle-section and stain junction depth measurements.

it more difficult to measure the electrical properties of n-type layers. Previous attempts to make ohmic contact to n-type implanted layers by using standard alloyed contacts have failed because the contact penetrated more deeply than the shallow implanted layer and "shorted out" to the substrate.[1]

Successful contact to n-type layers has been made recently by either of two techniques: (1) a modified "microalloy" method which has come into general industrial use for contacting bulk n-type GaAs, and (2) a room temperature ion implantation technique developed at Hughes Research Laboratories under company funded general research.

The microalloy contacting technique has been used to make Hall measurements on tin ion implanted n-type layers in GaAs. The contact is formed by evaporating a small (approximately 0.5 mm) tin dot onto the implanted layer at the desired point, after the implanted sample has been annealed as desired. The thickness of the evaporated tin layer is not critical; any thickness which is opaque to visible light is sufficient. A layer of nickel (about 10% as thick) is deposited on top of the evaporated tin dot in order to keep the tin from "balling up" due to surface tension during subsequent heat treatment. The sample is then heated at 450°C for 2 min. This heat treatment forms a very shallow alloyed contact to the n-type implanted layer. In about 80% of the cases it has been found that such contacts do not penetrate to the substrate; hence the technique is very useful, although not totally effective. Using this contacting method, Hall measurements were made on a number of tin implanted GaAs samples.

Previous attempts to produce an n-type layer in p-type GaAs substrates by tin implantation were unsuccessful[1]; however, it has been found that the failure resulted from an outdiffusion of implanted tin during annealing rather than from a lack of electrical activity of the implanted ions. This was determined by implanting a sample of high resistivity p-type GaAs with 35 kV tin ions at 400°C and annealing at 600°C for 5 min with the sample covered by a polished wafer of GaAs to inhibit outdiffusion of tin. (Hughes company-funded research has shown that a cover wafer is effective in preventing decomposition of the GaAs above 650°C.) Following anneal, an n-type region was present in the sample as determined from thermal probe measurements and from observation of the implanted layer-substrate V-I characteristic. The V-I characteristic of a diode cleaved from a tin implanted wafer is shown in Fig. 8. In addition, an n-type layer was observed in the cover wafer, into which tin atoms from the implanted wafer had apparently diffused. Hall measurements could not be made because the n-type layers were of extremely high resistivity. Similar tin implanted samples of p-type GaAs were annealed for 10 min at 700°C with a cover wafer, and the resulting n-type layer was of sufficiently low resistivity to permit Hall measurements. Typical values for the surface

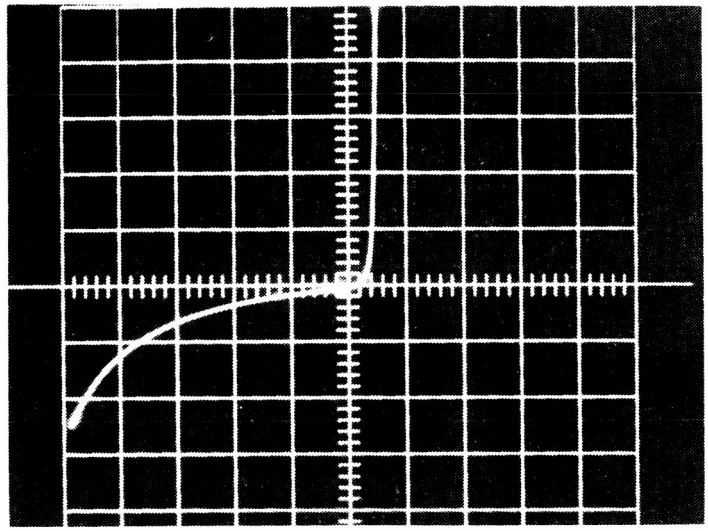
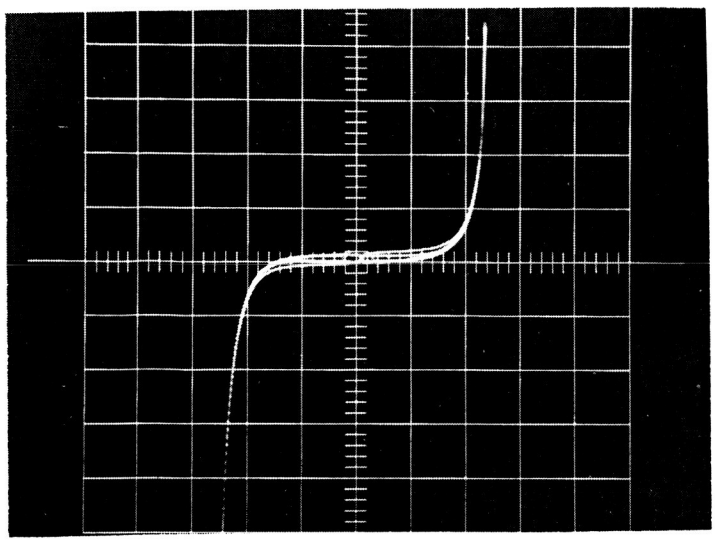


Fig. 8. V-I characteristic of a tin implanted diode. Horizontal scale = 10 V/div; vertical scale = 0.5 mA/div.

resistivity, mobility, and carrier concentration were ρ_s = 17,800 $\Omega/\square$, μ = 5.63 $cm^2/V\text{-sec}$, and $N_S = 6.24 \times 10^{13}/cm^2$, respectively. In order to produce an n-type tin implanted layer in GaAs, it has been necessary in all cases to protect the sample against outdiffusion by covering it with another GaAs wafer during annealing or by coating it with a layer of SiO_2, as described in Section II-A.

n-type layers have also been formed in GaAs by sulfur ion implantation. Contact was made to the sulfur implanted layers using room temperature implantation. It has been found that if sulfur (or tin) is implanted into GaAs with the substrate held at room temperature, the surface barriers which form at the contacts to annealed, n-type implanted layers are not observed. For good ohmic contact to a room temperature implanted layer it is necessary only to place gold probes upon the surface. This lack of surface barriers at the contacts to room temperature implanted n-type layers appears to result from damage effects rather than from the particular dopant involved, since the same effect has been observed for both sulfur and tin implants. This phenomenon offers a simple technique for contacting n-type layers which have been annealed and/or implanted at elevated temperature, and hence cannot be contacted directly with gold probes without the formation of surface barriers. The surface barriers can be eliminated by implanting contact "pads" at the desired points on the annealed sample, with the sample maintained at room temperature during this second implant. Figure 9 shows the IV characteristics measured between two gold probes contacting an annealed sulfur implanted layer both before (Fig. 9(a)) and after (Fig. 9(b)) the addition of room temperature (sulfur) implanted contact pads. The room temperature implantation of contacts does not affect the characteristics of the p-n junction between the original sulfur implanted layer and the substrate.

It has been observed that room temperature implantation of sulfur into p-type GaAs produces an n-type layer and a resulting p-n junction without requiring any subsequent annealing. The implantations were made using the electron bombardment ion source described previously.[1] The design of this source permits accurate measurement of the ion dose and hence represents a significant improvement over the spark discharge ion source. The characteristics of a diode made by implantation of $10^{15}/cm^2$ sulfur ions at 35 kV and room temperature are shown in Fig. 10. Room temperature sulfur implantations at 65 kV also yielded n-type layers without annealing; however, diodes formed from 65 kV implants had a higher forward resistance than those formed from 35 kV implantation. It was not possible to make Hall measurements on most of the samples because of very high resistivity and low mobility. However, a typical set of values for the few measurable samples is ρ_s = 11,300 $\Omega/\square$, μ = 0.5 $cm^2/V\text{-sec}$, $N_S = 1 \times 10^{15}/cm^2$. The room temperature sulfur implanted diodes were observed to emit light when biased in the forward direction. This effect is discussed in Section II-E.



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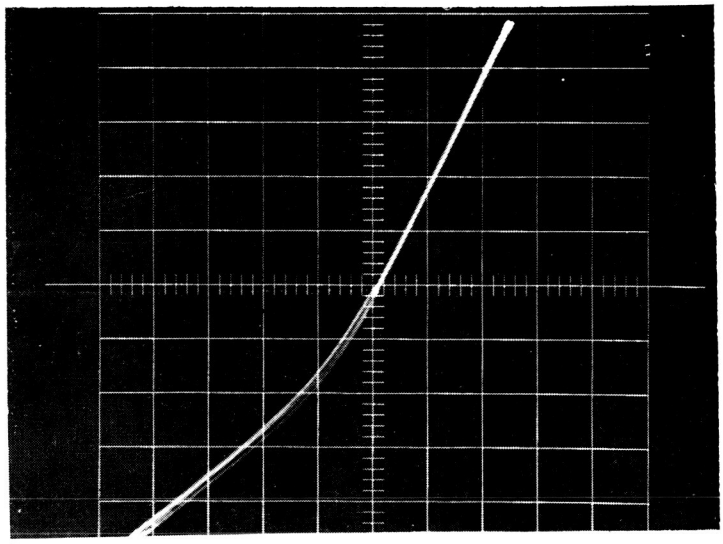


Fig. 9. I versus V measured between gold probe point contacts to an annealed sulfur implanted layer. (a) Directly touching layer (vertical = 10 μA/div; horizontal = 10 V/div). (b) Touching layer through room temperature implanted "pads" (vertical = 10 μA/div; horizontal = 0.2 V/div).

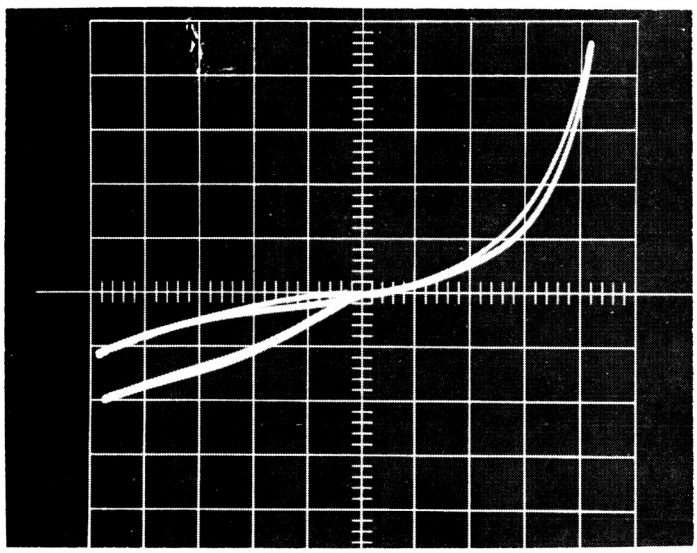


Fig. 10. V-I characteristic of sulfur implanted diode, showing the reverse bias current for both illuminated (lower curve in 3rd quadrant) and darkened condition (upper curve in 3rd quadrant.) (Vertical = 20 μA/div; horizontal = 2 V/div).

We believe the observed n-type region in room temperature sulfur implants may be caused by either substitutional sulfur atoms or defects. Theoretical work[14] indicates that it is possible for implanted ions to penetrate deeper than the maximum damage region under certain conditions, and we have observed substitutional behavior for bismuth implants at room temperature in silicon in our work supported by the Air Force.* Further effort is now being devoted to gaining an understanding of the nature of sulfur implanted layers in GaAs.

D. Semi-Insulating Layer Formation in Implanted Diodes

We have observed that diodes formed by zinc ion implantation into n-type GaAs at 400°C have a p-i-n structure rather than the normal abrupt p-n junction. Some of the results of these experiments have been published.[15, 16]

The diodes used in these experiments were formed by implanting a dose of approximately 10^{15} to $10^{16}/cm^2$ zinc ions at 70 kV into n-type GaAs substrates held at 400°C. After implantation the samples were annealed at 500°C for 5 min and etched to produce mesa diodes of approximately 0.5 mm diameter. We found that annealing was necessary to reduce the resistivity of the implanted layer to a reasonable value. However, the anneal time was kept as short as possible and the temperature as low as possible so that significant diffusion of the zinc would not take place. Contact was made to the p-type side of the diode using indium solder, and to the n-type side with evaporated tin heat treated at 425°C for 2 min.

The presence of a semi-insulating layer and a resultant p-i-n structure can best be seen from the capacitance-voltage characteristics for a typical diode, as shown in Fig. 11. The curve of $1/C^2$ versus reverse bias voltage is given for comparison for both an implanted diode and an evaporated aluminum surface barrier. The surface barrier was formed on a sample of the same substrate material as the implanted diode, after the substrate had been subjected to all of the processing and annealing steps except the actual implantation of ions. The offset observed for the diode curve thus results from implantation rather than processing or heat treating. It corresponds to a decrease in junction capacitance, indicative of an effective series capacitance, which we believe results from the formation of a semi-insulating layer

* Contract AF 33(615)-3821.

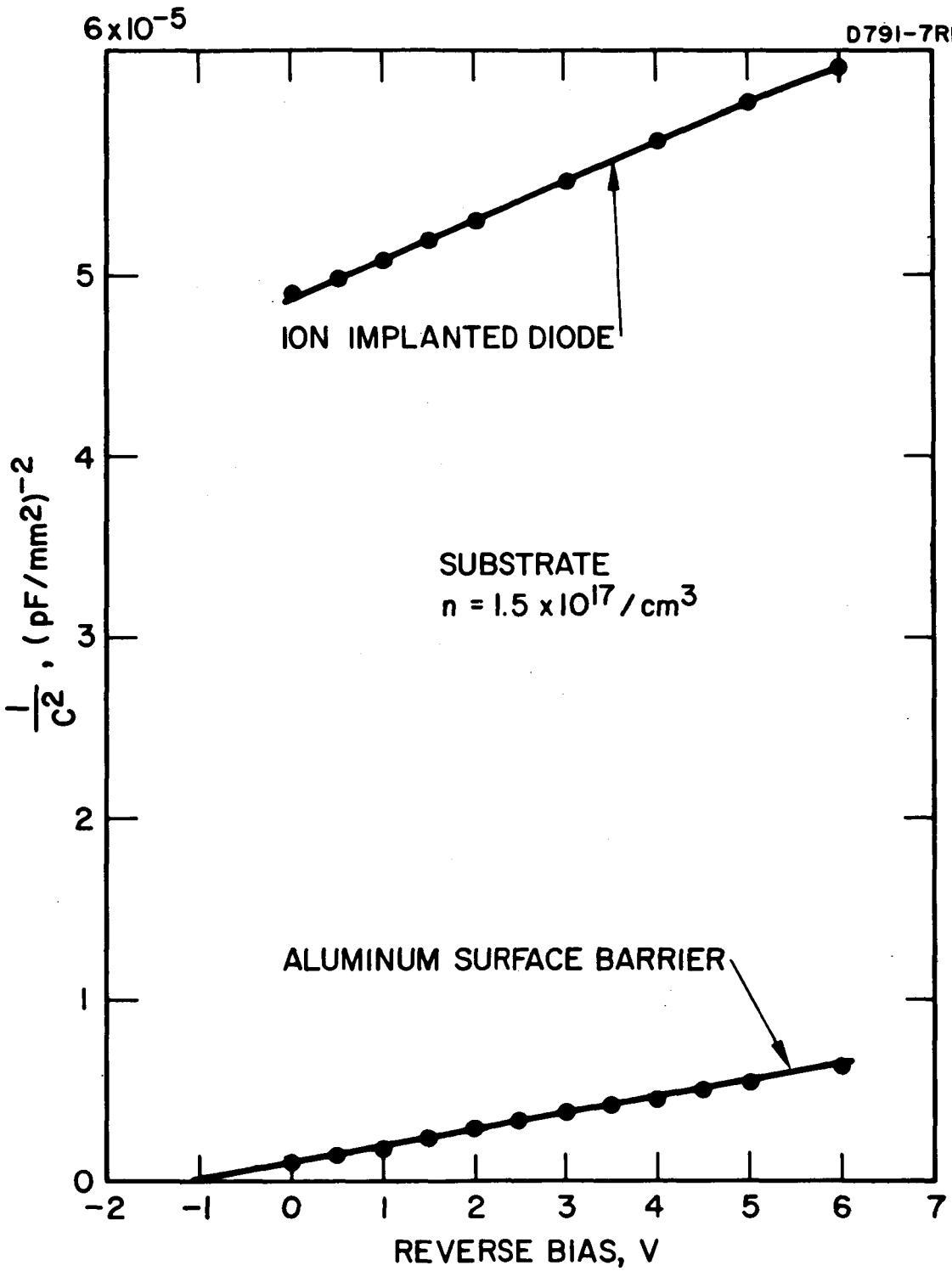


Fig. 11. Comparison of $(1/C^2)$-V characteristics of a zinc implanted diode and a surface barrier diode.

in the junction. Reverse bias capacitance measurements were made on diodes implanted with identical implant conditions into a number of substrates of various n-type background doping concentrations. In all cases the $1/C^2$ versus V curve was offset from that expected for a normal abrupt p-n junction, as can be seen in Fig. 12. Note that the amount of offset is smaller for more heavily doped samples, indicating a larger C or thinner semi-insulating region. From the amount of offset of the $1/C^2$-V curve it is possible to calculate the effective series capacitance and hence to determine the thickness of the semi-insulating layer in each case. The results of such calculations (given in Fig. 13) show that the thickness of the semi-insulating region depends on the substrate background doping concentration, varying approximately as the inverse of the square root of the concentration. Note that in all cases the thickness of the semi-insulating layer far exceeds the theoretical Lindhard-Scharff and Schiøtt[3] range of the ions and also appears to be too large to be attributed to channeled ions. Zinc diffusion is negligible for the temperatures and times involved in these implantations. We have observed similar behavior of deeply penetrating electrical centers resulting from antimony ion implantation in silicon.[17] The centers behaved as donors in silicon and followed an $N \propto (x + B)^{-n}$ dependence over four orders of magnitude in N, where $x \equiv$ depth, $B \cong 0.15\ \mu$, and $n \cong 2.2$.

We believe that the relatively thick semi-insulating layer results from deep diffusing defects (as a result of either the implantations or subsequent anneal) which produce compensation to the depth where the concentration of defects equals the substrate doping concentration. The data of Fig. 13 for diodes formed on substrates of different impurity concentration thus represent a profiling with depth of the defect concentration. The defects responsible for the deep level traps and resultant compensation are believed to be generated as described below.

When a semiconductor is bombarded by a beam of high energy particles, as in ion implantation doping, a damage layer is produced which extends to a depth on the order of the projected range of the particles.[3] Subsequent annealing causes the damaged layer to "heal," leaving a residual concentration of localized defects (vacancies and interstitials) which may diffuse through the lattice to form more complex and more stable defects at depths exceeding the projected range of the implanted ions. These defects can cause deep level states in the energy bandgap.

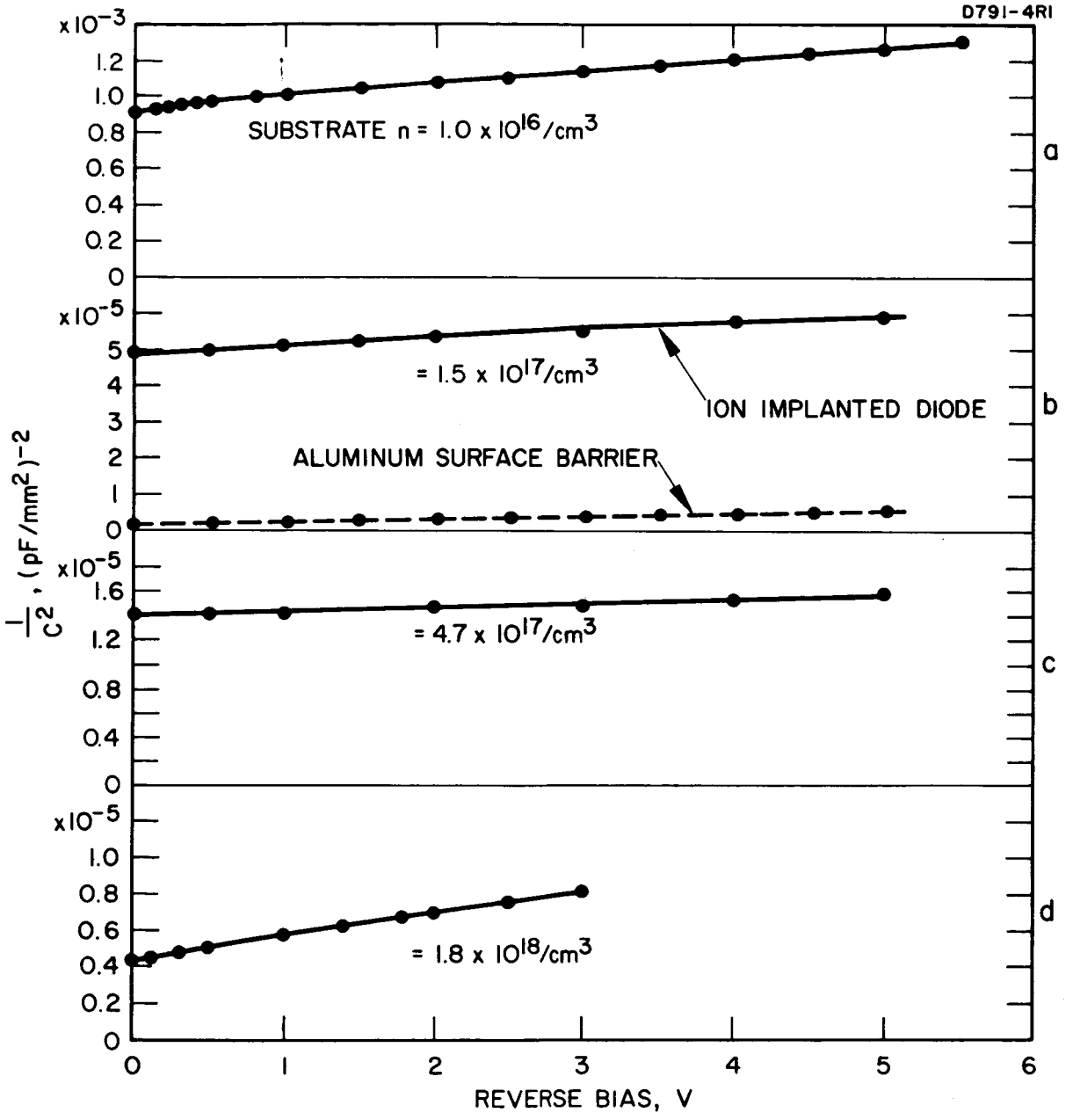


Fig. 12. $(1/C^2)$-V characteristics of zinc implanted diodes.

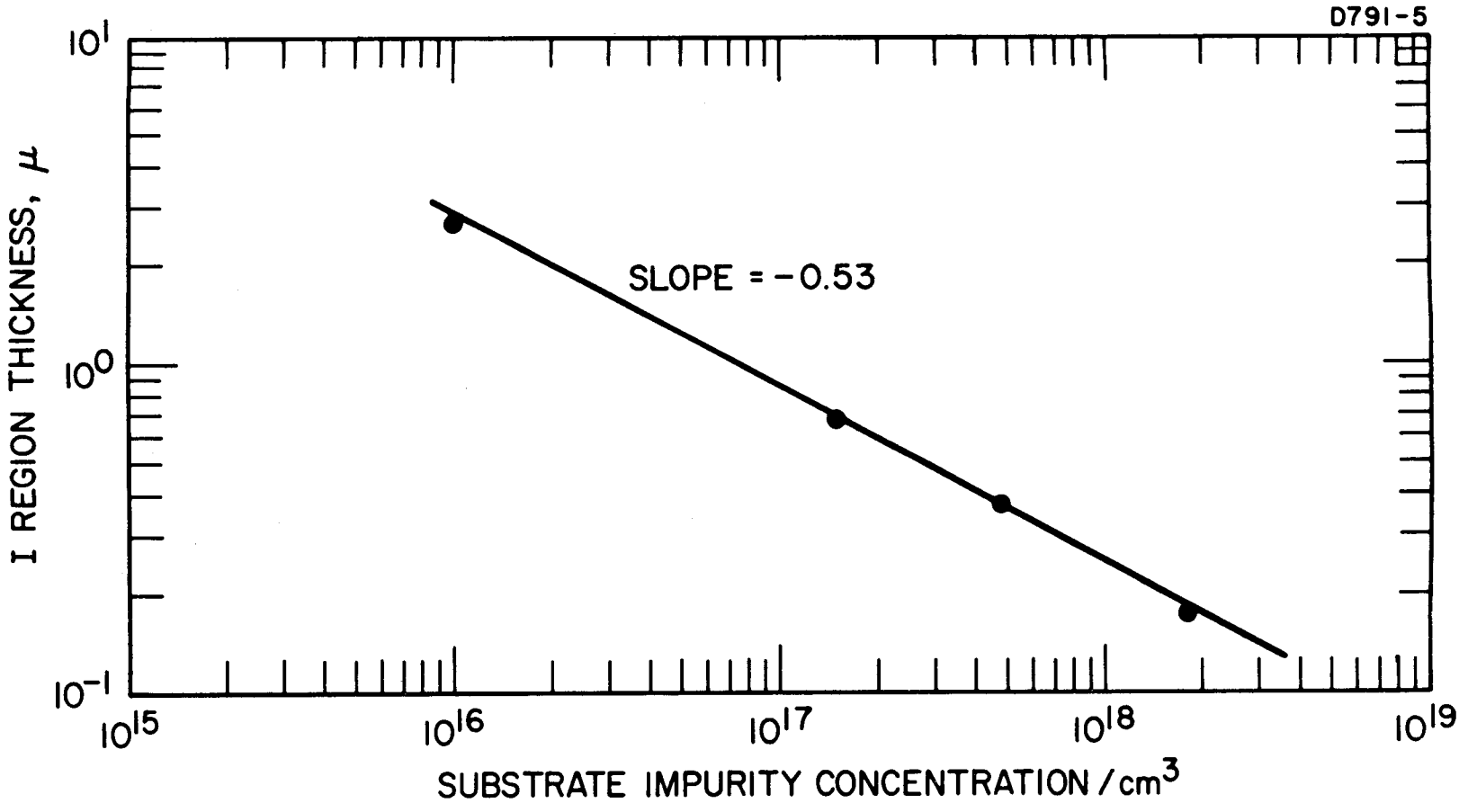


Fig. 13. Dependence of semi-insulating region thickness on substrate impurity concentration. All samples are implanted identically.

The forward bias V-I characteristics of these implanted diodes were found to be somewhat unusual, as can be seen in Fig. 14. Above the 10^{-8} A level the current follows a V^4 relation over a variation of about five orders of magnitude.

Current versus voltage measurements have been made on additional zinc implanted diodes with substrate impurity concentrations from $1 \times 10^{15}/cm^3$ to $1.8 \times 10^{18}/cm^3$. In all cases the current followed a V^n relationship for V greater than about 0.1 V, where n = 4 to 5. Such a power law dependence is characteristic of double injection of carriers into a semi-insulating region.[18-21]

Another characteristic of these diodes which is indicative of the presence of deep level traps is an observed frequency dependence of the junction capacitance, as shown in Fig. 15. Data are given for two different substrate concentrations, and for two different temperatures in the case of the more lightly doped substrate. It can be seen that in all cases the junction capacitance decreases with increasing frequency of measurement. This decrease can be explained by the fact that the defect trapping centers cannot charge and discharge rapidly enough to follow the applied signal at high frequencies; thus they cannot contribute to the capacitance. It should be noted that the capacitance measurements used previously to calculate the thickness of the semi-insulating layer were made at 500 kHz, the highest available frequency, so that traps would not contribute to capacitance and the true thickness of the semi-insulating region thus would be measured. From the results shown in Fig. 15 it can be seen that there was less frequency dependence of the capacitance for the sample formed on the more heavily doped substrate. An increase in temperature also resulted in larger capacitance at a given frequency, since the detrapping time was diminished. Such behavior of capacitance with frequency, doping, and temperature is qualitatively in agreement with the behavior observed by Sah and Reddi[22] for deep levels in gold-doped silicon and that observed by Schibli and Milnes[23] for deep levels in indium-doped silicon.

Detailed measurement of the temperature dependence at 5 kHz indicated an exponential increase of capacitance with rising temperature, as shown in Fig. 16. The slope of the curve corresponds to a phenomenological activation energy of 0.29 eV. In order to determine the dependence of semi-insulating layer thickness on annealing, a series of diodes was prepared by implanting 70 kV zinc ions into n-type ($n = 1 \times 10^{15}/cm^3$) substrate material, and various samples were annealed at $500^{\circ}C$ for periods ranging from 5 min to 1 hour. No significant difference in layer thickness was observed between diodes annealed for brief periods and those annealed longer. Thus it appears that the thickness of the semi-insulating layer is established during implantation or in the first few minutes of annealing at a given temperature. One diode, with implantation identical to that of the others, was annealed at $600^{\circ}C$ for

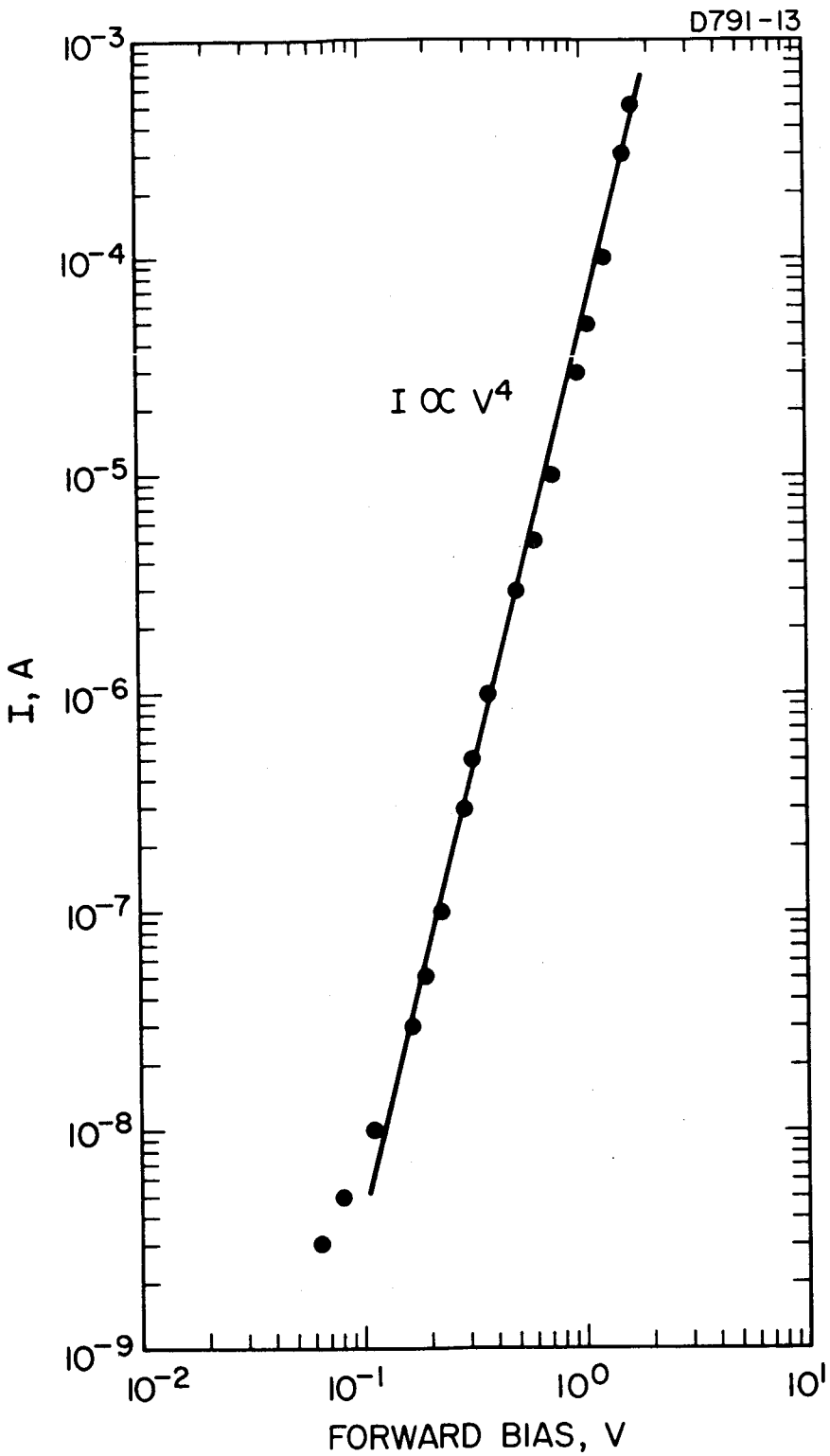


Fig. 14. Forward V-I characteristics of a zinc implanted diode.

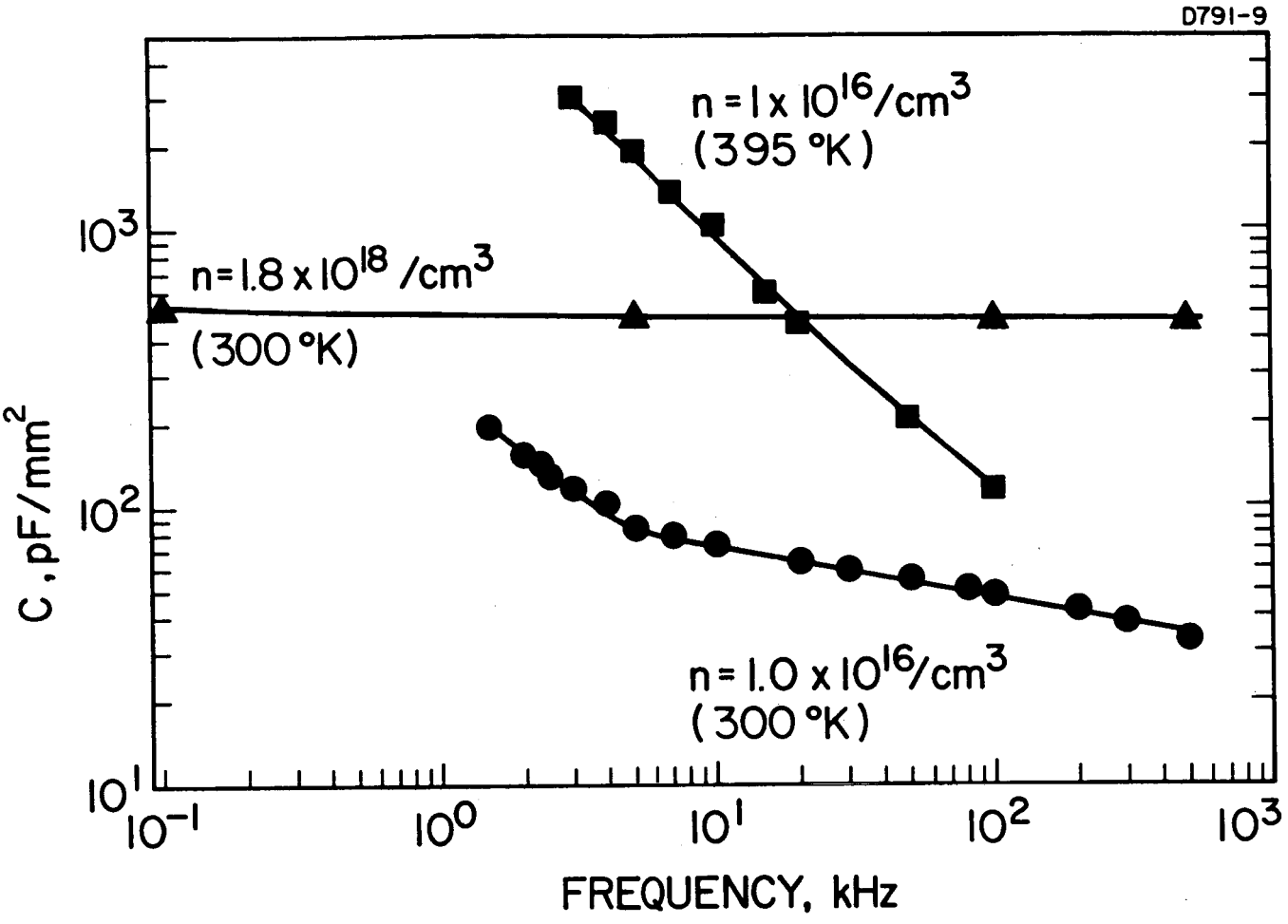


Fig. 15. Frequency dependence of zinc implanted diode junction capacitance.

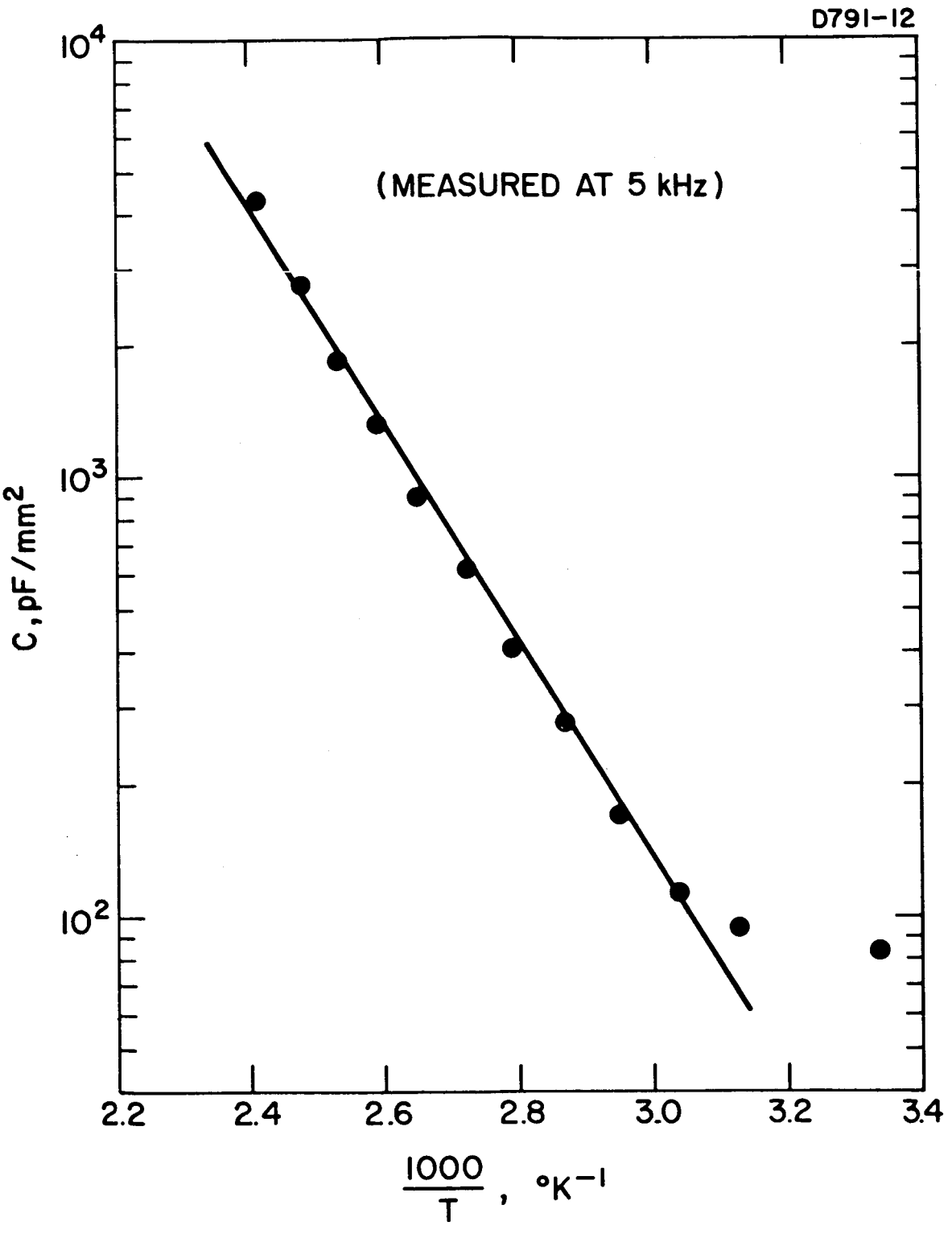


Fig. 16. Temperature dependence of zinc implanted diode junction capacitance.

10 min. The resulting semi-insulating layer was found to be thinner by a factor of about 4 than that obtained with 500°C annealing. More samples annealed at 600°C and higher will have to be tested before any definite conclusion can be drawn, but the indication is that higher temperature annealing may reduce the thickness of the semi-insulating layer. For example, a sample of 20 kV zinc implanted GaAs (substrate doping concentration $n = 1.8 \times 10^{18}/cm^3$) was annealed for 10 min at 900°C. Capacitance-voltage measurements indicated a semi-insulating region thickness of only 0.06 μ, compared with 0.18 μ measured for similarly implanted samples annealed for 5 min at 500°C.

Another experiment has been performed which supports the proposition that p-i-n diodes are formed by zinc implantation into GaAs at 400°C. In this experiment two samples of n-type GaAs were implanted at 400°C with 70 kV zinc ions. One sample was annealed at 600°C for 16 hours, and the other for 5 min. p-type layers were formed at the surface of each sample. However, when the samples were strip-etched to remove a layer ≅ 300 Å thick, the surfaces of both samples had extremely high sheet resistivity and developed no measurable Hall voltage, as would be expected for an intrinsic region. It should be noted that Roughan and Manchester[24] report the formation of p-i-n diodes by implanting zinc into GaAs at room temperature and subsequently annealing at 650° for 18 hours. This long annealing time results in diffusion, which produces graded p-i-n junctions similar to those we have observed in 400°C implantations. However, they report that room temperature zinc implants and shorter annealing (3 hours) yield normal abrupt p-n junctions.

The formation of the semi-insulating layer is not limited to the case of zinc implants. Capacitance-voltage measurements were made on a cadmium implanted diode and the results revealed the presence of a semi-insulating layer such as that observed in zinc implanted diodes. The fact that this layer forms whether implantation is with zinc or cadmium supports the theory that it results from defect centers rather than from the implanted ions themselves.

E. Ion Implanted Electroluminescent Diodes

The direct bandgap of GaAs makes it an attractive material for use in optical devices. In addition, measurement of the optical emission of electroluminescent diodes formed by ion implantation is useful for determining the nature of implanted layers. For these reasons we have undertaken a number of experiments involving observation of optical emission from ion implanted diodes. Much of the work described in this section was done in collaboration with Dr. William Jeffers of the University of Illinois, who joined Hughes Research Laboratories for the summer of 1968.

Light emitting diodes have been fabricated by implanting n-type GaAs substrates ($n = 1 \times 10^{15}/cm^3$ to $1.8 \times 10^{18}/cm^3$) with 70 kV zinc ions at 400°C and annealing at 500°C for 5 min. These diodes were found to emit near infrared radiation when biased in the forward direction. The emission was observable with a "snooperscope" at forward bias currents ranging from several milliamperes to several hundred milliamperes at room temperature, depending on the area of the diode. Cooling the diodes to 77°K improved the efficiency and resulted in increased light output, as would be expected. The spectral output of these diodes was measured using a cooled (77°K) 7102 photomultiplier tube to cover wavelengths from the visible spectrum to about 1.1 μ. A cooled (193°K) lead sulfide detector was used to observe the emitted spectrum out to a wavelength of about 4.5 μ. The implanted diodes were operated on a dc basis, but the light output was "chopped" mechanically at a frequency of 177 cps to permit the use of a "lock-in" amplifier. This technique considerably reduced background noise. The output wavelength was determined using a Jarrell-Ash 0.25 m Ebert monochromator. A mirror focusing system was used to guide the light from the diodes to the monochromator, with the diodes being mounted on the cold finger of a cryostat and maintained in a vacuum.

Spectral output was measured at 77°K for a number of diodes implanted and annealed as described (70 kV, 400°C implant; 500°C, 5 min anneal), and a very broad emission peak in the near infrared was observed for all samples. The peak of this emission was at 9750 Å and the half width was about 1500 Å. A typical line width for a diffused junction GaAs light emitter is about 200 Å. A very slight amount of near band edge emission was also observed at approximately 8700 Å. No significant dependence on substrate doping was observed. It should be noted that these light emitting diodes are exactly the type for which capacitance-voltage measurements indicate the presence of a semi-insulating layer. The unusually broad line width observed is suggestive of the presence of radiative states in the bandgap, which may be associated with implantation caused defects similar to those thought responsible for the semi-insulating layer. It is also possible that this emission results from the inadvertent presence of impurities in the GaAs, as will be discussed later.

Diodes in a second set of samples, implanted like the first, were annealed for 10 min at 600, 700, 800, and 900°C. The emission spectrum at 77°K was observed to change with increasing temperature of anneal, as seen in Fig. 17. The 9750 Å peak narrowed somewhat in bandwidth and a new peak at 8500 Å emerged. This new peak was relatively narrow (several hundred Angstroms bandwidth) and is probably associated with "band edge" radiation. The efficiency of these diodes is generally low compared with that of commercially available GaAs light emitters. However, one diode annealed at 900°C

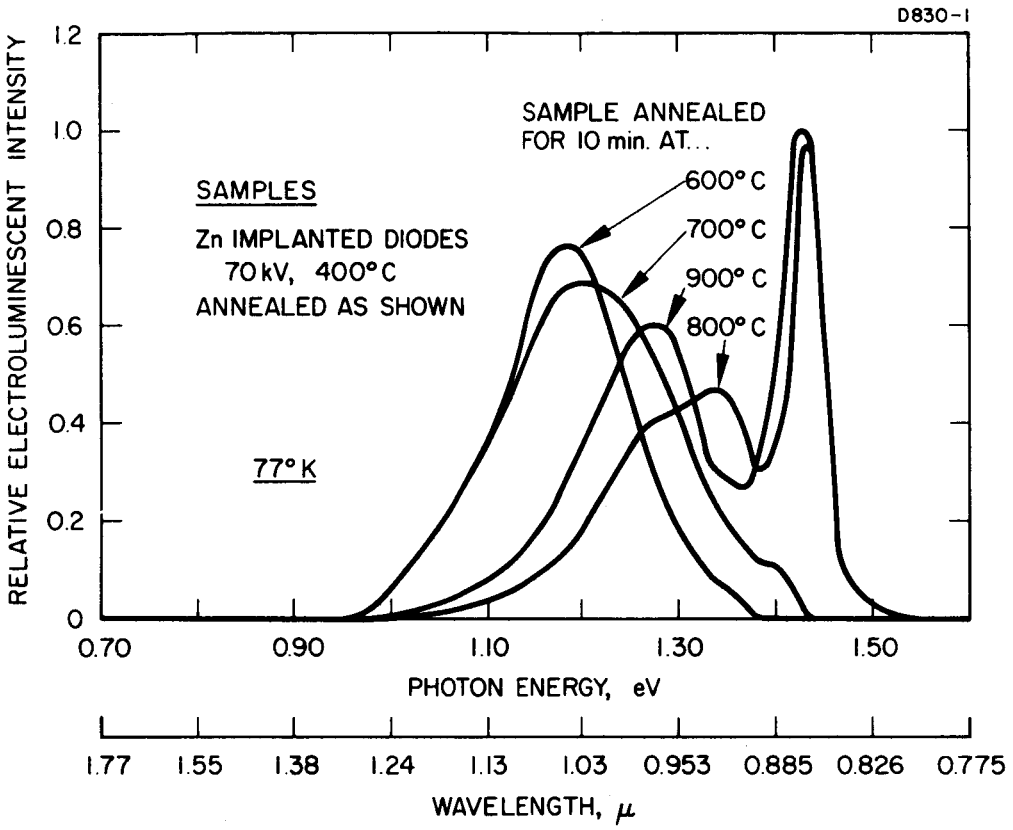


Fig. 17. Emission spectra of zinc implanted diodes; dependence on anneal temperature.

for 5 hours had an output in the 8500 Å peak approaching that of commercial units (see Fig. 18). The samples used in these experiments were handmade, and of irregular shape. It is expected that efficiency could be greatly improved by using more sophisticated geometry and contacts. It is also necessary to determine what implantation conditions produce the best results. For example, we have reason to believe that hot (400°C) implants such as those used may generate numerous dislocations which could serve as nonradiative recombination centers.[25]

The output spectrum of the 5 hour, 900°C annealed sample (shown in Fig. 18) exhibits an interesting feature which may also be present in more briefly annealed samples but not detectable because of the extremely low efficiency. The 9750 Å peak has shifted slightly to about 9540 Å, and a third emission peak at 1.25 μ is also clearly visible. Other authors have reported observing two emission peaks in addition to the band edge emission in GaAs diodes at wavelengths corresponding to those of Fig. 18 to within the limits of experimental error. Larsen[26] reports observing a secondary peak at 0.95 eV (1.30 μ) in diffused GaAs diodes at 300°K. He conclusively identifies this peak with copper impurities by the controlled addition of copper to the samples. Nathan, et al.,[27] report observing two secondary peaks at 1.02 eV (1.22 μ) and 1.28 eV (9680 Å) in diffused GaAs diodes at 77°K. They attribute the emission peaks to unidentified defect levels and suggest that more than one kind of center probably is involved. Morgan, Pilkuhn, and Rupprecht[28] have observed broad low energy peaks in the emission spectra of diffused GaAs diodes at 1.29 eV (attributed to copper) and 1.0 eV (attributed to an unidentified donor level lying 0.5 eV below the conduction band). All of these authors report unusually low external quantum efficiencies, indicating that considerable nonradiative recombination is taking place in diodes with the low energy emission peaks in addition to band edge emission. This nonradiative recombination is quite likely associated with whatever defect centers are present. The broad, low energy emission peaks observed in ion implanted diode light emitters appear to be the same as those observed in diffused diodes. Hence we are optimistic that the efficiencies of implanted diode emitters can be improved by eliminating whatever defects or impurities are responsible for the centers.

Diodes formed by implantation of sulfur into p-type substrates at room temperature (such as those described in Section II-C) also have been found to emit infrared radiation. A typical emission spectrum is shown in Fig. 19 for a diode formed by implanting 1×10^{15} ions/cm^2 of sulfur at 60 keV into a high resistivity p-type substrate at room temperature. Contact was made to the diode with silver epoxy in order to avoid any type of heating. Only one emission peak was observed, at 1.04 μ. However the intensity was very low and other peaks might be observable in a more efficiently emitting sample. Considerable

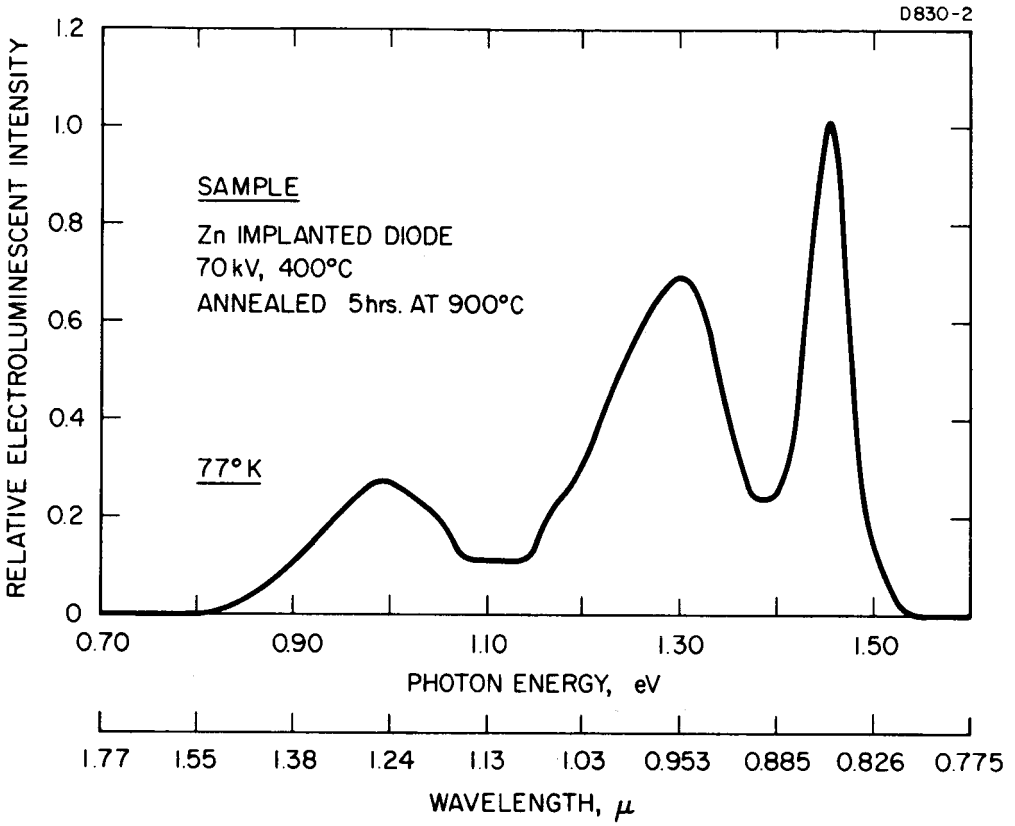


Fig. 18. Emission spectra of diode annealed at 900°C for 5 hours.

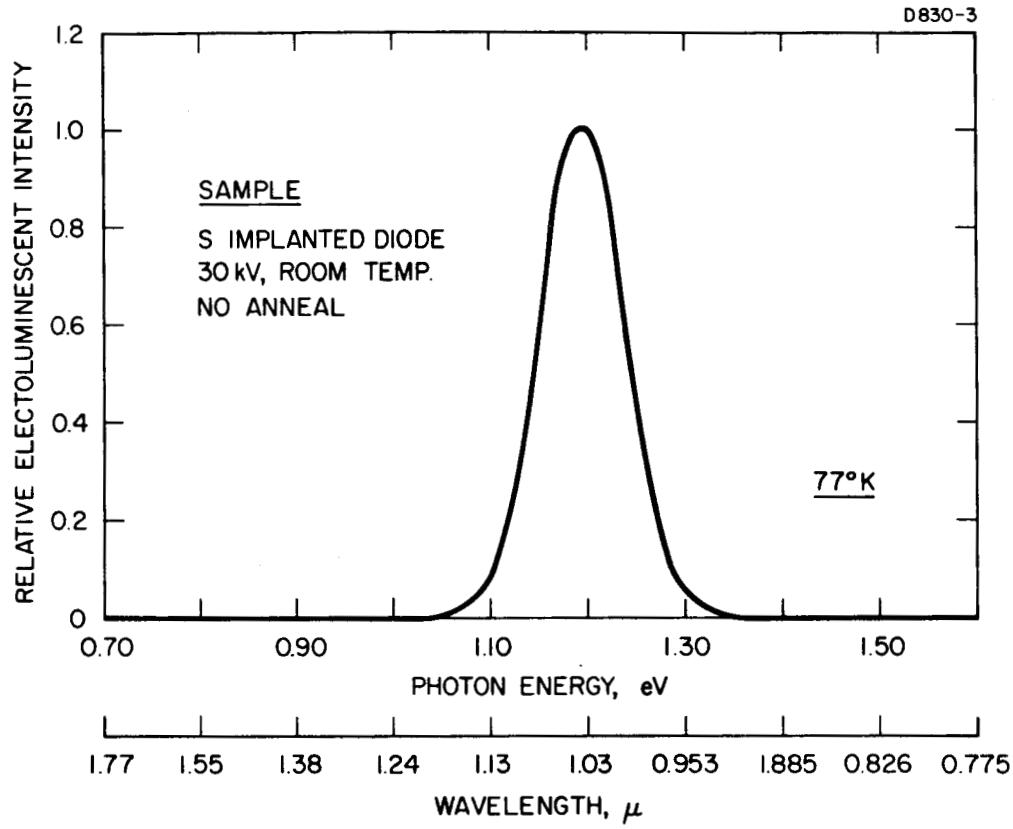


Fig. 19. Emission spectra of a sulfur implanted diode.

work remains to be done in this area. It is nevertheless impressive that it is possible to form light emitting diodes in GaAs by means of a room temperature process utilizing ion implantation.

In summary, light emitting diodes have been formed in GaAs by both zinc and sulfur implantations. The quantum efficiencies were generally low, with little or no band edge radiation, emitted until after anneal at elevated temperatures. However, observed emission in broad, low energy peaks accompanying the band edge radiation suggests the presence of defects or impurities which are known to greatly reduce efficiency by providing nonradiative recombination centers. The elimination of these centers by means of improved material handling and annealing procedures would hopefully produce diodes of respectable efficiency.

F. Damage Studies

The anneal behavior of ion implanted damage in GaAs has been measured in a cooperative program with J. W. Mayer, E. Westmoreland, and T. Picraux at the California Institute of Technology.

A series of room temperature 70 keV Zn^+ implantations were made with doses ranging from $\approx 10^{14}/cm^2$ to $10^{16}/cm^2$. Exact doses were not determined for these initial experiments. The amount of damage introduced into the GaAs was measured by the Rutherford scattering technique using 1 MeV He^+ ions generated with the Cal Tech 3 MeV van de Graaf accelerator. Annealing studies were then performed while each sample was in place in the apparatus. The experimental procedure was to make a scattering analysis at 23°C, anneal the sample at a selected temperature for 10 min, return the sample to room temperature, and remeasure the residual damage in the sample. Figure 20 presents the results of such measurements on the series of zinc implantations. The heaviest implants do not show complete annealing even after a 600°C anneal. The mobility data for heavy Zn and Cd implants shown in QPR 6 would suggest the same damage condition, even though those implants were performed at 450°C. However, it should be noted from Fig. 20 that there is apparently some annealing at ~250°C. Lighter implants show less damage and lower anneal temperatures, with the lightest annealing at ≈75°C. Such behavior is significantly different from that observed for silicon, where "light" damage requires 280°C for annealing.

More quantitative measurements are now required, as well as some comparison with electrical behavior for these implant conditions. Continuation of the scattering measurements will be delayed slightly because the Cal-Tech equipment is scheduled for some modifications; measurements will be resumed in approximately six weeks.

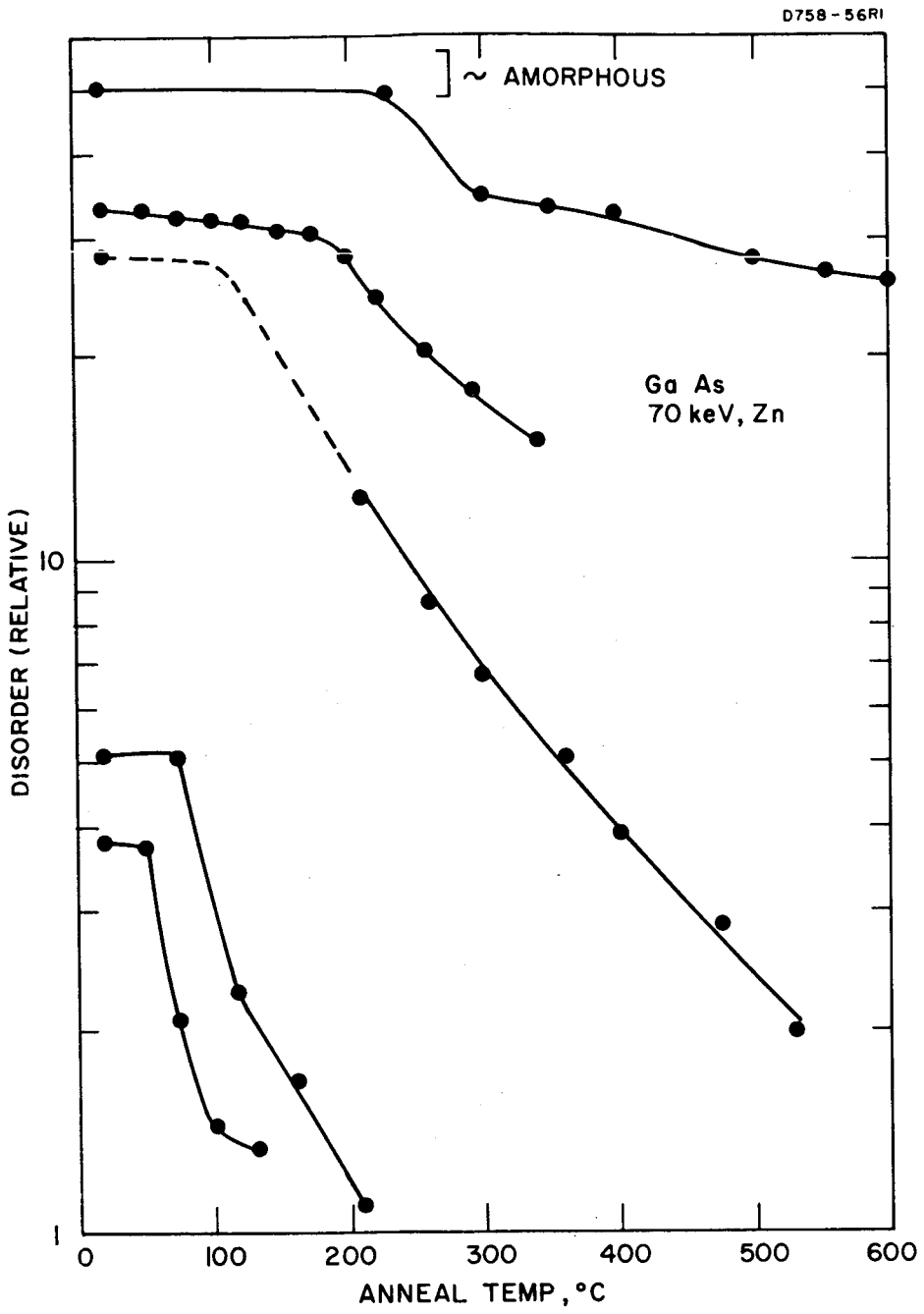


Fig. 20. Dependence of lattice disorder on annealing for zinc implanted GaAs (curves are shown for increasing ion doses from approximately 10^{14} to above $10^{16}/cm^2$).

Initial scattering measurements performed on unimplanted α-SiC supplied by Sylvania reveal the presence of a considerable amount (≈ 0.1%) of high Z impurities, such as Ge, Se or As, and lighter impurities in larger amounts.

G. Future Plans

The study of the dependence of the electrical characteristics of ion implanted layers on implantation conditions and annealing will be continued, with the emphasis probably being shifted to such n-type dopants as tin, sulfur, and tellurium. Room temperature implantation will be investigated particularly because it appears (somewhat surprisingly) to offer advantages over hot implants.

Further determination of the nature of the semi-insulating layer found in implanted diodes will be attempted, with a major objective of controlling or eliminating the layer, as required for device applications.

Measurement of the output spectra of implanted diode light emitters will be continued as a tool for obtaining better understanding of damage and annealing. Efforts will be made to identify and eliminate defects or impurities which reduce quantum efficiency, thus producing practical light emitters by ion implantation.

III. IMPLANTATION STUDIES IN SILICON CARBIDE

A. Material Studies

Studies of donor implantation into SiC were made in a small amount of p-type, aluminum-doped, α-SiC supplied by the Westinghouse Research and Development Center. This was highly compensated material with a net acceptor concentration of 1.5×10^{16} cm^{-3}. Because only a few pieces were available, it became necessary to remove previously implanted layers from these crystals in order to obtain fresh surfaces for additional studies. The temperatures used in the studies were far below those reported to affect the bulk properties of α-SiC, so that cumulative effects were not expected and were not observed.

n-type α-SiC was available in larger quantities, but implantation of acceptor ions does not convert this material to p-type, and little work was done with these crystals.

Layers implanted with acceptors were examined using small, solution-grown platelets of β-SiC supplied by a group headed by F. Halden at Stanford Research Institute. Crystals from two growth batches were studied; each batch had a carrier concentration of approximately 10^{17} donors/cm^3, as determined by Hall measurements. No dopant was added intentionally during the growth; nitrogen is suspected to be the residual dopant. Determination of the carrier concentration by capacitance-voltage measurements on evaporated gold surface barriers indicates a slightly higher doping level. This higher concentration is consistent with the Hall measurements because deeper levels may be ionized during the capacitance-voltage measurements, contributing additional centers.

Visual inspection of these β-SiC crystals has shown that they are free of inclusions to a greater degree than most of the SiC obtained previously. Electrical probing with gold or tungsten points indicates that there are possible variations in the conductivity within each sample. Material which had not been implanted or otherwise changed has been found to have areas on the surface, less than 0.5 mm across, where the resistance to an electrical probe drops by an order of magnitude or more. These places do not appear to be related to any visual characteristics of the material.

X-ray examination of the solution-grown platelets at Stanford Research Institute has shown that twin planes occur commonly in these crystals. These planes are not always parallel to the surface of the crystal, and thus can intersect the surface. SRI reports that p-n junction behavior in the material can be attributed to the existence of these planes. Current-voltage characteristics of two contacts on the same face of a crystal have exhibited saturation and current limitations; this is also an indication of layers of varying conductivity. Ion implantation involves only thin layers near the surface, however, and this layered structure has affected examination of the implants in only a few cases.

An unexplained phenomenon has been observed with these β-SiC crystals. One side of the crystals consistently gives no response to the thermoelectric probe when both hot and cold probes are on this same side. The other side gives a strong n-type response, and with the probes on opposite sides of the sample there is again indication of n-type material. No attempts have been made to identify these faces with the "A" or "B" crystal face, or to determine why one side does not respond to the thermal probe.

B. Electrical Contacts

Substantial improvements have been made with respect to making contacts to SiC. Low-resistance, no-barrier contacts have been applied to β-SiC at moderate sustained temperatures without using controlled atmospheres. A modified molecular bonder, Weltek model 800, is used to attach gold wires directly to the surface of the SiC. The crystal is held on a substrate at a temperature of about 100°C, and the gold wire with a "nail head" ball is lowered to the contact area. A small amount of silicon is already at the contact area, and the heat pulse to the molecular bonder tip serves to melt the gold-silicon mixture and bond it to the SiC surface. Care must be taken to use a small piece of silicon so that it will be completely melted into the gold; a short heating pulse must be used to prevent the bonder tip from melting the lead wire inside it. This contact method also may be used to attach gold to the crystal for alloying in high temperature furnaces so that jigs will not be needed for positioning. Contacts have been made to both α- and β-SiC. The α-SiC exhibited small barrier voltages to this contact, but this might be prevented by using a dopant along with the silicon wetting agent. The β-SiC exhibited no such barrier voltage, and the contacts have shown good current-voltage characteristics.

Electrical measurements of the crystals both before and after ion implantation have been made primarily at room temperature. Other investigators have customarily used alloyed metals for contacts to SiC. At present, these alloyed contacts are not feasible for use in studying implanted layers, both because the contacts may short out the junction and because the additional heat treatments of annealing may degrade the alloy. Gold bonded contacts will not short out a junction because they will not penetrate the material. Point contacts of either gold or tungsten have been used for preliminary measurements, but they are inadequate for reproducible, dependable electrical measurements.

Soldered indium-silver has been found to be a quiet, dependable contact to SiC of sufficiently low resistivity. The β-SiC crystals which we have tested may be measured using these contacts. The gold bond contacts, which will function properly on these crystals, have not yet been required. Implanted layers in α-SiC usually have been measured using the soldered indium-silver.

C. Surface Preparation

Ion implants have been made into surfaces prepared in several ways. The larger α-SiC crystals have been etched in molten sodium peroxide to provide a clean surface. This process is much too rigorous for the small β-SiC pieces, and these have been implanted "as grown" or after an etch in hot hydrogen. In some cases the hot hydrogen has resulted in a "frosted" finish, however, and the implants are usually into surfaces which have merely been cleaned in etches designed to etch silicon. There are no indications that this chemical treatment removes any part of the SiC surface.

Other methods of etching SiC have been tried during this report period. Phosphoric acid has been reported to etch SiC,[29] and its use was attempted earlier on α-SiC; however, we have observed no etching.

This substance is reported to etch α-SiC at its boiling point of 215°C. One crystal face is attacked and turned into a white gelatinous substance.[38] However, phosphoric acid has a boiling point of 215°C only for a particular water content, and condensers must be used to maintain any given water content and boiling point. Although the etch is orientation-dependent for α-SiC, it is not orientation-dependent for silicon itself.[30] Because β-SiC has the same crystal structure as silicon, it appears possible that phosphoric acid will etch this type of SiC without crystal preference. If this is true, it is possible that a mask can be found against this lower temperature etch. No work has been reported in the literature of phosphoric acid on β-SiC. Some

etching runs have been made in this laboratory. Etching of β-SiC for an hour at 215°C in the phosphoric acid bath has not removed a verifiable amount of material. Etching can be measured by weight loss (or weight gain in the case of formation of an insoluble substance), but weight changes in the sample have been small enough to be indistinguishable from measurement deviations. Weight measurements were made on a Cahn electrobalance of 1 μg sensitivity.

Molten sodium peroxide is another widely used etchant for SiC. Although one side of α-SiC crystals is etched roughly and unevenly, the other side is etched smoothly. Sodium peroxide is a reactive substance at the necessary 500°C etch temperature, and masks for controlling it have not been found. Attempts have been made to dilute the etch with sodium nitrite. Various proportions of the nitrite have been mixed with the peroxide in an effort to slow the etch sufficiently to allow some masking. We have been able to slow the etch rate of the SiC, but the reaction rates of the various masks have not been reduced. We still are unable to mask against this etch, except with platinum clamps held firmly against the surface. This method obviously cannot be used with the delicate flakes of β-SiC.

A method for etching SiC is reported in the literature which presumably can be controlled. When SiC is heated in oxygen at low pressure, a volatile oxide is formed. This removes material from the surface at a slow, controlled rate. Antimony-implanted, p-type α-SiC which had been annealed in vacuum to 1000°C was heated to 1000°C in oxygen at 0.1 Torr. The electrical characteristics changed little, if any, after periods of 1 and 5 min at the elevated temperature. Subsequent etching of this sample in molten sodium peroxide revealed great numbers of etch pits tracing lines of dislocations. There were also rough, eroded surface areas and severely etched holes at sites of electroluminescence tests. Since this sample had already been etched many times in hot sodium peroxide, the new pits must be directly attributable to action of the oxygen upon the crystal. Although this will be an interesting study itself, it offers little promise at present for the formation of volatile oxides as an etch.

Electrolytic etching in a modified CP_4 solution[32] is an easily performed and easily controlled etch for p-type SiC. This applies to both the grown p-type α-SiC and the aluminum implanted p-type regions in n-type β-SiC. For a thin n-type region on a p-type substrate, electrolytic etching can be used if the hole mobility and lifetime are sufficiently high to permit a hole current through the donor layer. The literature has reported the use of ultraviolet light[32] for generating holes in an n-type region in order to sustain an etching current, but we have not achieved a successful etch using this method. No room temperature etch has been found for n-type SiC.

An etch process using chlorine and oxygen has been used for β-SiC at SRI. This involves temperatures above 800°C, but oxides can be used as masks for sample shaping. This process has not been used here, but will be available for device fabrication in the next period.

D. Implantation in Silicon Carbide

1. Donors — Two species of donor implants have been made in this year. The spark discharge source with a swept beam for even ion distribution was used to implant bismuth at 500°C with 50 kV implant voltage. A piece of lot C-359, p-type α-SiC was used. Following implantation and prior to annealing, thermal probes indicated weak n-type response in the implanted area. Following anneal at 1000°C in helium, the thermal probes give stronger n-type response; however, the entire crystal surface now gives an n-type response. Further electrical probing of the entire crystal shows that the bismuth implanted region raises no barriers against tungsten probes, while the nonimplanted area has substantial surface barriers against tungsten probes. Controlled cleaning methods are not yet available for detailed examination of the implanted region. Bismuth implanted characteristics will be examined thoroughly when investigative methods have been improved.

The larger part of the study of donor implants concerned antimony ions. Aside from the formation of p-n junctions, antimony has been used as a low-resistance contact site to bulk n-type material. The presence of the antimony layer permits pressure and solder contacts which are frequently unsatisfactory otherwise.

The p-type α-SiC available for use as a substrate in the formation of ion-implanted p-n junctions has been in short supply, making it necessary to clean and reuse some crystals. Annealing cycles and implant temperatures were such that no changes in the bulk characteristics were expected, and none were observed. Molten sodium peroxide was used to remove completely all traces of earlier implants.

Aqua regia and etches designed to dissolve silicon were used to clean implanted surfaces so that they would be annealed without danger of contamination.

For some samples, it is necessary to anneal the samples to 1700°C in order to bring the resistivity of an antimony-implanted layer in p-type SiC into the range required for the use of the soldered indium-silver contacts. Heating SiC in vacuum to 1700°C has been shown to result in surface decomposition.[33] This effect was seen clearly in our samples by comparing the nonimplanted surface of a

p-type crystal, after heat treatment and after a subsequent electrolytic etch. The conducting surface layer is very thin for our anneal conditions of 3 min at 1700°C in a vacuum of 10^{-5} Torr; this effect is readily separable from any effect resulting from the implanted conditions. The heated surface shorts out the implanted region, however, and must be removed before meaningful tests can be made. For p-type material, this surface can be removed simply by electrolytic etching. A very slight etching to remove this conductive surface is adequate to increase the resistance between two tungsten probes 0.25 mm apart from nearly $10^5\ \Omega$ to greater than $10^9\ \Omega$. The same etch treatment of the implanted surface results in an increase of resistance from $10^4\ \Omega$ to $10^5\ \Omega$. Soldered indium-silver contacts are adequate to make reproducible Hall measurements for this surface.

Observations of a nonimplanted p-type surface have shown that the etch quickly removes p-type material. An antimony-implanted surface is not removed, reaffirming that this region is an n-type layer. An n-type region is capable of maintaining a small hole current by diffusion, however. If mobilities and lifetimes are adequate, the holes can diffuse to the surface of the n-type region and cause a slow etch rate. This can explain the etch removal of the heat-decomposed layer, which may or may not have remained p-type.

Even after the heat-decomposed layer was removed from the α-SiC, the V-I characteristics of the implanted p-n junction remained poor. The reverse current is consistently higher than desired and the breakdown voltage is lower than expected. The same situation exists in the β-SiC although the high anneal temperatures are not required. There has been no evidence of surface decomposition in the heat-treated β-SiC.

The resistance of the antimony-implanted surface to the electrolytic etch is shown in Fig. 21, which is a photomicrograph of the edge of an electro-etched antimony implant. A sodium peroxide etch prior to implantation has brought into sharp relief a small crystal plane. This ridge had sharp edges which are still visible in the implanted area. The electrolytic etch has removed the p-type surface and smoothed out and rounded the sharpness left by the peroxide. In the area converted to n-type by the antimony ions, the crystal has not been rounded and retains the sharp planes of the peroxide etch.

Various methods have been attempted for improving the V-I characteristics of the devices by cleaning and etching, with little success. Electrolytic etching of an implanted antimony layer in p-type bulk etches and slightly undercuts the implanted area, but the implanted region will etch only slightly. Minute holes also visible in Fig. 21 have been etched in many implanted surfaces, however; the existence of these holes is evidence that junction irregularities of some sort are present, which serve to degrade the V-I characteristics.

M 6392

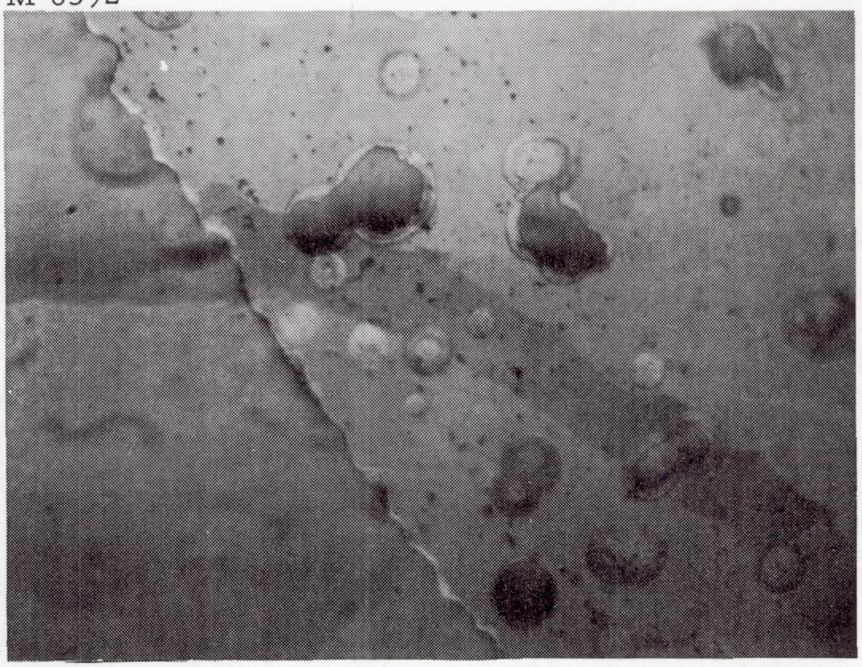


Fig. 21. Electrolytic etch silicon carbide; n-type layer on p-type bulk.

An antimony-implanted sample which had been annealed to 1000°C in vacuum was heated to the same temperature in oxygen at 0.1 Torr, as described in Section III-C. The condition of the sample after the subsequent sodium peroxide etch indicated an oxygen reaction with some sort of damage sites. There was no correlation of these damage sites with the antimony implant area, however, and the affected areas are presumed to be caused by the crystal morphology or mechanical handling damage. On the other hand, work on GaAs described in Section II indicates that some of the difficulties with junction quality may be caused by a large amount of crystal damage and vacancies which have not been annealed; this may be true even at 1700°C for SiC. Because higher anneal temperatures will cause other problems as a result of surface decomposition, known-dose implants will be studied when more p-type SiC has been received. The use of capacitance-voltage and capacitance-frequency measurements should determine acceptable dose rates and anneal temperatures.

Hall measurements of the van der Pauw type have been made on the antimony-implanted layers. One sample of aluminum-doped, p-type α-SiC was implanted at 500°C with 25 kV antimony ions. This was later annealed in vacuum at 1500°C for 30 sec. Hall measurements of this implanted layer show that it is n-type with a sheet resistivity of 9000 Ω/□, an electron mobility of 9 cm^2/V-sec, and a surface concentration of $8 \times 10^{13}/cm^2$. This mobility value is consistent with reported mobilities in other similarly doped and grown SiC samples.

On some antimony-implanted samples of p-type α-SiC, the junction formed was too poor to permit isolation of the implanted layer from the bulk material. Hall measurements on a layer of this sort indicate p-type because of the poor isolation. However, even though an implanted region cannot be isolated sufficiently to permit satisfactory Hall measurements, it is possible to examine the effect of the diffused-hole-controlled etch on the conductivity of the implanted layer. Short electrolytic etches of the implanted surface were made with sheet resistivity measurements before each etch. Surface irregularities and growth steps in the material, coupled with the transparency of the SiC, prevented measurement of the thickness of material etched off, but a steady increase in sheet resistivity was obtained as the etch progressed. This process would appear useful as a method of examining the profile of the implanted ions, and this method of stripping shall be applied on the known-dose implants.

2. Acceptors — Because both boron and gallium completely failed to exhibit acceptor action when implanted into SiC, all acceptor implants in this period have been of aluminum. Aluminum implanted into n-type α-SiC has also failed to exhibit acceptor characteristics. Aluminum implanted at room temperature and 50 kV into a sample of p-type α-SiC even prevented that material from being electrolytically

etched. Instead of contributing holes to conduct the etching current, the implanted ions apparently formed enough recombination centers to absorb the hole current sustained by the bulk SiC.

Aluminum implanted into β-SiC has converted the n-type bulk to p-type, however. It has not yet been determined why the cubic form is converted rather than the hexagonal crystal, but it has been observed that the implanted layers respond as p-type to the thermal probe and in thin-film Hall measurements.

Aluminum implanted into β-SiC at 500°C and annealed at 1000°C has been examined through Hall measurements. The small size of the β-SiC samples makes it impossible to make the implanted layer in shapes suitable for van der Pauw examination,[4] but measurements confirm that the aluminum layer is p-type. Measured sheet resistivity was 900 Ω/□, with an unexpectedly high Hall mobility of 400 $cm^2/V\text{-}sec$. The approximations required because of sample size and shape give a high mobility; this indicates that the true hole mobility probably is much less than the 400 $cm^2/V\text{-}sec$ obtained.

One of the samples of β-SiC was implanted with aluminum at 500°C and 20 kV, using the spark-gap ion source. This resulted in a p-type region before higher temperature annealing. A 5 kV implant in a piece of the same sample required 1000°C anneal before a p-type signal could be obtained by the thermal probe. Both of these implants were performed at 500°C.

Annealing the 20 kV implant at 1000°C weakened the p-type response to the thermal probe, and strong variations in response to electrical probing over the implanted surface served to emphasize the fact that the "spottiness" in the base material was swamping any effect from the aluminum implant. The 5 kV implant also was variable in response over the implanted surface. The sample shattered, however, and has not been given higher temperature anneals.

Studies of acceptor ions implanted into silicon have encouraged the use of room temperature implants. It has been observed that for a given dose, annealing at an intermediate temperature serves to produce more available carriers from a room temperature acceptor implant than from an acceptor implant done at that anneal temperature.

Following an antimony implant on the back to serve as a bulk contact, a piece of β-SiC was given two implants of aluminum ions at room temperature; one at 50 kV and one on top of that at only 10 kV to prevent a buried junction.

Silicon carbide of semiconductor quality is a transparent substance. It may be yellow, as in β-SiC, or grey, green or blue as in various grades of α-SiC. The transparency has been useful in locating inclusions in low grade material and in ascertaining the boundaries of ion-implanted regions. An ion-implanted region is consistently a dark one before annealing. This darkness probably results from disruption of the lattice, because there appear to be few free carriers to cause free carrier absorption. Determination of the cause requires optical investigation, which has not yet been attempted. It has been observed, however, that the optical density of the dark layer decreases upon annealing.

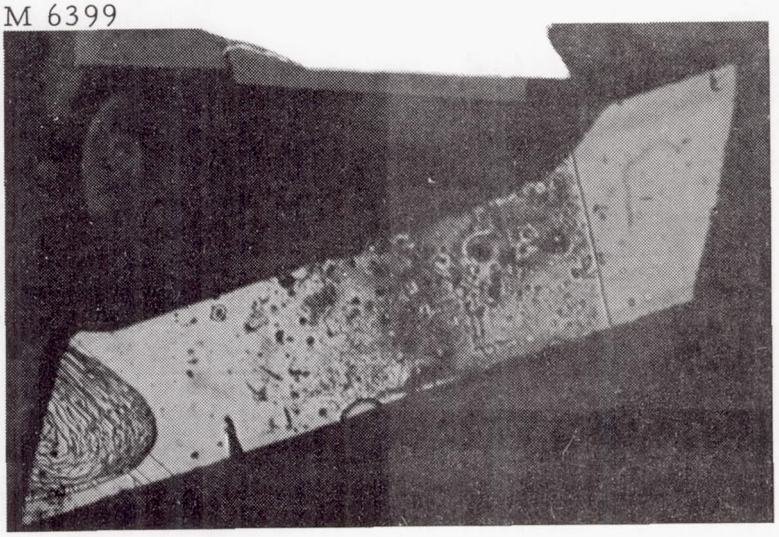
This 50 kV aluminum implantation was considerably darker than those made earlier. The edge of the implanted region was clearly defined. Annealing steps of 1000°C and 1200°C in helium lightened the region to almost the original yellow color, although there was no difficulty in locating the implant edge. The effect of this annealing on electrical probing was minimal, and the sample was then annealed at 1500°C in a helium atmosphere.

This anneal caused severe erosion of the aluminum-implanted region. It should be brought out here that this decomposition of SiC at only 1500°C is not to be expected. A hydrogen-rich atmosphere can cause a small amount of decomposition at this temperature and has been used as an etch. An oxygen atmosphere at a higher temperature can also cause decomposition and growth of silicon oxide coatings. The erosion experienced in this case is not evenly distributed over the aluminum-implanted region, and is not evident on either the non-implanted nor the antimony-implanted regions. Earlier, similarly implanted samples annealed in vacuum showed no evidence of decomposition.

Since this experiment was performed, it has been reported[34] that heating SiC in an inert atmosphere is a process which is extremely sensitive to adsorbed gases on the furnace parts. The fact that this "trace gas etching" was most noticeable on the aluminum implanted area appears to indicate unannealed damage from these ions. This sample had been implanted with a greater implant voltage and lower implant temperature than previous samples, and the increased damage is not inconsistent with these conditions.

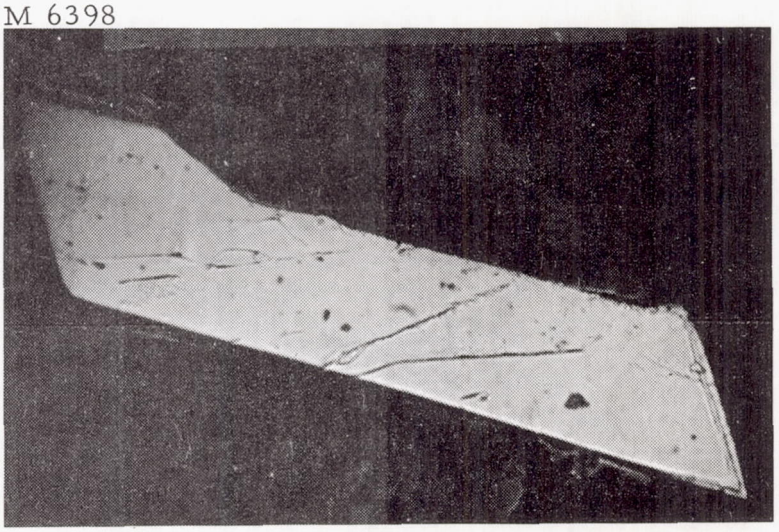
Figure 22(a) shows the present condition of this eroded aluminum implanted sample. Note the sharp demarcation of the limit of the aluminum implant in the straight line near the right end and the unblemished condition of the nonimplanted region. Figure 22(b) is a picture of the antimony-implanted side which of course received the same heat treatment, but shows none of the erosion evident on the aluminum-implanted side.

M 6399



(a) Aluminum implanted side.

M 6398



(b) Antimony implanted side.

Fig. 22. Surface condition of eroded silicon carbide.

A distinct p-type response was obtained over part of the implanted surface when tested with the thermal probe. A poor but distinct FET characteristic can now be obtained on this aluminum-implanted surface. Current depletion is obtained with negative voltage applied to the antimony-implanted layer serving as the gate. This is opposite to the bias required for depletion from an n-type gate and, coupled with the evaluation of the original material, leads us to believe that there is a submerged, grown p-type bulk region. The current-carrying channel is now presumed to be the original n-type surface of the SiC sample which has been eroded to suitable "thinness" by ion bombardment and the trace gas etching. The present p-type response probably is from a region where the implanted ions and the rest of the n-type surface have the original n-type surface layer in only small islands.

As a tool for examining crystal damage in our samples, x-ray investigation has been inconclusive. There are indications that alloyed contacts cause considerable strain in the thinner crystals but this cannot be examined fully at our facility. The surface after ion implantation has not shown any regions of strain. Sufficient work has been done on contact methods to permit us to avoid alloyed contacts; therefore, effort on x-ray examination has been suspended.

Another piece of β-SiC was implanted with a dose of 5×10^{14} ions/cm^2 at room temperature with 25 kV implant voltage. The controlled, lighter dose and lower implant is an attempt to cause less damage. This sample has been inspected through the use of the thermoelectric probe, surface barriers and their electrical characteristics, and Hall measurements. The results of Hall measurements on the implanted layer have indicated n-type behavior regardless of anneal conditions. This response is to be expected in a thin p-type layer if there is poor junction quality or high leakage current which prevents good isolation of the implanted layer. This layer is such a small fraction of the total bulk of the sample that the changes in it as a result of annealing are too small to be detected in measurements of the complete sample. Etching and other junction cleaning processes have not yet been used for these samples.

Quantitative results have been obtained with the thermoelectric probe. Two tungsten probes, one hot and one cold, on the same surface of the implanted sample indicate n-type material regardless of anneal conditions. As described in earlier reports, if μ_n/μ_p is large, we may have $n_p\mu_n > p_p\mu_p$ in the p region which will result in an n-type response even though $p_p > n_p$. If one of the probes is on the implanted surface and one on the opposite non-implanted surface and ultraviolet light from a mercury lamp is applied to the sample, a photon generated current results, indicating

either that there is a p-type layer in the sample or that a twin plane exists in the material. These twin planes have been verified to exist in some samples by the makers of the material at SRI, and they have observed them to have junction characteristics.

The response to ultraviolet light is affected by annealing processes, however. Annealing the sample to 1250°C removes all trace of the junction response. Since a crystallographic condition in the β-SiC could not be removed at this temperature, this may mean that a p-type region exists as a result of the light aluminum implant. The extent of any crystal damage cannot be examined by the hot probe technique, but a p-type response could be noticed due to a significant increase in hole mobility from annealing. Such a result has not been found.

The use of evaporated surface barriers for evaluating the impurity concentration and its profile in materials has proven to be a very valuable analysis tool. It was felt that such an analysis might lead to some insight on the electrical behavior of these aluminum implanted layers. Surface barriers of evaporated gold were made in the past on unimplanted SiC material obtained from SRI. Capacitance-voltage measurements established that the barrier height for gold on n-type β-SiC was 0.7 V. The current-voltage characteristics were those expected from surface barriers on n-type material.

Attempts to make gold surface barriers on material recently obtained from SRI have been unsuccessful, suggesting that this material is in some way different from that obtained previously. When barrier type behavior, although of poor quality, has been observed on the new material, the capacitance-voltage measurements have indicated a carrier concentration of 10^{18} cm^{-3}. The possible existence of internal p-n junctions as a result of the twin planes may well be the source of this difficulty.

Gold was evaporated onto the implanted regions in the hope that some useful data could be obtained, but the results could not be interpreted. This examination will continue when other known dose implants are obtained.

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