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STUDY OF FAILURE MODES OF MULTILEVEL LARGE SCALE INTEGRATED CIRCUITS

November 1968

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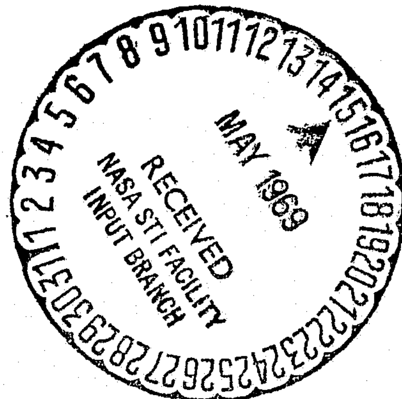
N69-24951
(ACCESSION NUMBER) (THRU)
132 1
(PAGES) (CODE)
CR 96146 09
(NASA CR OR TMX OR AD NUMBER) (CATEGORY)
FACILITY FORM 602

Prepared Under Contract NAS12-544

by

PHILCO-FORD CORPORATION
Microelectronics Division
Blue Bell, Pennsylvania



Electronics Research Center

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

NASA CR -

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NASA CR -

National Aeronautics and Space Administration
Electronics Research Center

Advanced Technology Directorate
Technology Assistance Division
Failure Mechanisms Branch
Cambridge, Massachusetts 02139

Interim Scientific Report No. 3

This report describes studies performed in accordance with Contract No. NAS12-544, dated April 15, 1967, and Modification No. 1 to that contract, effective October 15, 1967. The report covers work performed between April 15, 1968 and October 14, 1968.

Submitted by:

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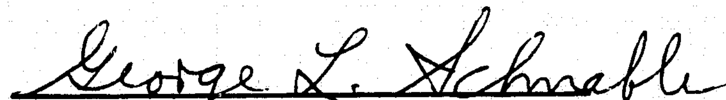

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SUMMARY

Empirical and theoretical investigations have resulted in techniques for improving the reliability and performance of large scale multilevel microcircuit arrays. The model for the factors influencing the electrical properties of the silicon surface has been extended, and several types of complex ion migration that influence device stability have been described. A number of new test structures have been designed that have a higher measurement sensitivity or that require less area on the chip.

Considerations concerning the most effective use of test structures are discussed for five types of applications. It is shown that the results from single test structures can be combined to provide additional information. Specific sets of test structures for use with either MOS or bipolar production microcircuits are described. A specific set of test patterns made by a change in the metal pattern on a standard production microcircuit chip is described. Techniques are presented for conserving space taken up by test structures.

The use of thick oxides for minimizing the effects of surface ions has been subjected to both quantitative theoretical analysis and experimental verification. The use of qualified test wafers for quality monitoring of the materials, procedures and equipment used for building microcircuits is discussed.

Experimental data are given on the annealing of fast states which indicate the need to evaluate areas both covered by metal and not covered by metal. Vapor plated titanium oxide and aluminum oxide, and r-f sputtered SiO_2 from a high purity target were evaluated as candidates for second-layer oxides. It has been shown experimentally that the density of mobile ions in an oxide depends on the proximity of a p-n junction and of an oxide surface not covered by metal. The use of a second-layer metal to minimize surface ion effects was experimentally evaluated. Data are presented that show an instability of the transconductance of an MOS transistor that appears to be due to an instability in the mobility of carriers in the inversion layer. Data are presented from a study of the effects of a deposition of a second layer of phosphosilicate over MOS transistors made by a production process. The effects of each of the steps in a complex processing sequence used to produce bipolar microcircuits on the electrical properties of the oxide have been measured.

The significance of the results of the work performed during this period is that multilevel microcircuits, of both MOS and bipolar types, can be produced with better yield, performance and reliability by the improvements in understanding of the factors that influence the surface properties of the

silicon, in the procedures for measuring these factors and in the knowledge of ways by which these factors can be controllably altered.

INTRODUCTION

Background

A necessary part of the successful development of LSI circuitry is the development of practical means for process development, process control, failure analysis and reliability prediction. The increasing complexity of microcircuits greatly increases the problems of and the need for measuring the fundamental parameters of the basic structures in the silicon chip.

The fabrication of complex LSI circuits having multilevel metal, or of glassed single-metal-layer circuits, requires a number of new materials and fabrication processes. Thermally grown oxide is generally used for the first insulator layer because its interface with silicon has a low density of states at the silicon surface. Since the second layer of insulator material must cover the first layer of metal interconnections, its formation requires a technique other than thermal oxidation. The process by which the second insulator layer is formed must be compatible with the processes and materials used in making the microcircuit. For example, if the first-layer is aluminum, the structure cannot be heated above the aluminum-silicon eutectic temperature (577°C) during the formation of the second insulator layer. Or, if one uses molybdenum-gold, the gold-silicon eutectic temperature is 370°C,

which could create a problem at a pinhole in the molybdenum layer. A third metal system being used in significant volume is the titanium-platinum-gold system. In this case, diffusion through a pinhole or through the platinum barrier causes titanium-gold compounds to form, at temperatures above 500°C, that greatly increase the resistivity of the metal layer.

The materials and processes chosen for the formation and delineation of the second insulator layer and the second metal layer must not contaminate the thermally grown oxide with mobile ions (sodium ions or protons) that can drift into the first insulator layer. It is desirable that the second insulator layer act as a protective barrier to such contamination. This second layer must also be free from pinholes that could cause shorts between metal layers. Vapor plated oxides are known to have a much higher water content than thermally grown oxides and this water may alter the properties of the oxide-silicon interface.

The reliability and performance of LSI circuitry must not be compromised by failure modes arising from the additional steps required to obtain multilevel metallizations. The probability of failure may increase because of a decrease in stability or because of a change in the initial characteristics which reduces the tolerance to instability.

At the present time, multilevel LSI circuit structures are generally of the bipolar type. The techniques described in this

report are applicable to both bipolar and MOS microcircuit structures. Present trends in the industry point to the increased use of deposited second-layer insulator materials for electrical passivation and mechanical protection of microcircuits with a single layer of metal. Developments that increase the sensitivity of a circuit to instabilities in the electrical properties of the insulator, increase the need for evaluating the properties of the insulator-silicon interface. An example of such a development is the use of <100> oriented silicon.

The development of basic test structures provides a valuable means for measuring the fundamental properties of the insulator-semiconductor interface. Such test structures are now used for process development, for in-process control and for reliability studies. Herr, et al.[1,2] changed the metallization patterns on microcircuit structures on selected chips on an integrated circuit wafer to permit the testing of discrete devices in the chips. The data taken from these devices were then used for process control and for reliability predictions. Farley[3] described the use of test patterns for reliability evaluations of MOS circuits having a single layer of metallization. Barone and Myers[4] described the use of test patterns for multilevel arrays. Birk[5] used test patterns for studying sputtered SiO_2 for use with multilayer interconnects. Test patterns have also been discussed by Stern[6].

Objectives

The objectives of this program are to:

1. Develop fundamental information to improve the understanding of possible failure modes of LSI circuitry.
2. Develop basic models to facilitate the discussion and understanding of the variations in the performance and reliability of LSI circuitry.
3. Develop test structures for measuring the fundamental parameters of the silicon surface.
4. Correlate data taken from test structures with that taken from actual devices so as to determine which individual effects degrade yield or reliability.
5. Establish practical techniques for eliminating or circumventing these effects to improve the yield and reliability.

The scope of this program has been limited to yield and reliability problems related to the electrical properties of the surface of the microcircuit. Although the limited scope does not include problems due to pinholes in the dielectric layer, contact resistance, metal continuity over oxide steps, Philco-Ford has other programs in which these other influences on microcircuit performance and reliability are being studied. Some of the results of these other efforts are included in a paper by

Schnable and Keen[7] that was prepared for the Seventh Annual Symposium on Reliability Physics, December 2-4, 1968 in Washington, D.C.

Summary of Accomplishments Reported in Previous Interim Scientific Reports

During the periods covered by Interim Scientific Reports No. 1 and No. 2, we accomplished the following:

1. Prepared an extensive bibliography of the pertinent literature.[8,9]
2. Developed a useful model that embodied the known possible factors that influence the performance and reliability of large scale multilevel integrated circuits.
3. Designed and fabricated monolithic integrated circuit test structures for the evaluation of LSI production processes, and evaluated such test structures on conventional production microcircuit wafers.
4. Made measurements on test structures:
   a. To study the repeatability of measurements,
   b. To study the repeatability of properties of specific types of oxides,
   c. To compare properties of oxides made by different processing techniques,
   d. To compare oxides made with different materials,

e. To compare the properties of oxides taken from various points in a complex processing sequence for building microcircuits,

f. To compare the properties of vapor plated oxides having different levels of phosphorus content.

5. Developed preliminary concepts for eliminating or circumventing the causes of poor microcircuit yield and reliability.

This report covers the third six-months period of the program. It covers the work performed from April 15, 1968 to October 15, 1968, and contains the details of the following main accomplishments:

1. The development of a more complete model for the factors influencing the performance and reliability of large scale multilevel integrated circuits.

2. The continued surveillance of the pertinent literature and the compilation of additional items (see Appendix A) to update our previous bibliographies[8,9].

3. The design of a second generation set of test structures for measuring the fundamental properties of the dielectric-silicon interface.

4. The continuing effort to study empirically the effects of various materials and processes on the fundamental properties of the dielectric-silicon interface.

5. The correlation and interpretation of the empirical data, of predictions from the theoretical models, and of the results reported by other investigators.
6. The extension of the model of the individual factors influencing the performance and reliability of microcircuits to include complex interactions of the individual influences.
7. The further development of concepts for eliminating or circumventing the causes of poor microcircuit yield and reliability.

ELECTRICAL FACTORS INFLUENCING CIRCUIT RELIABILITY

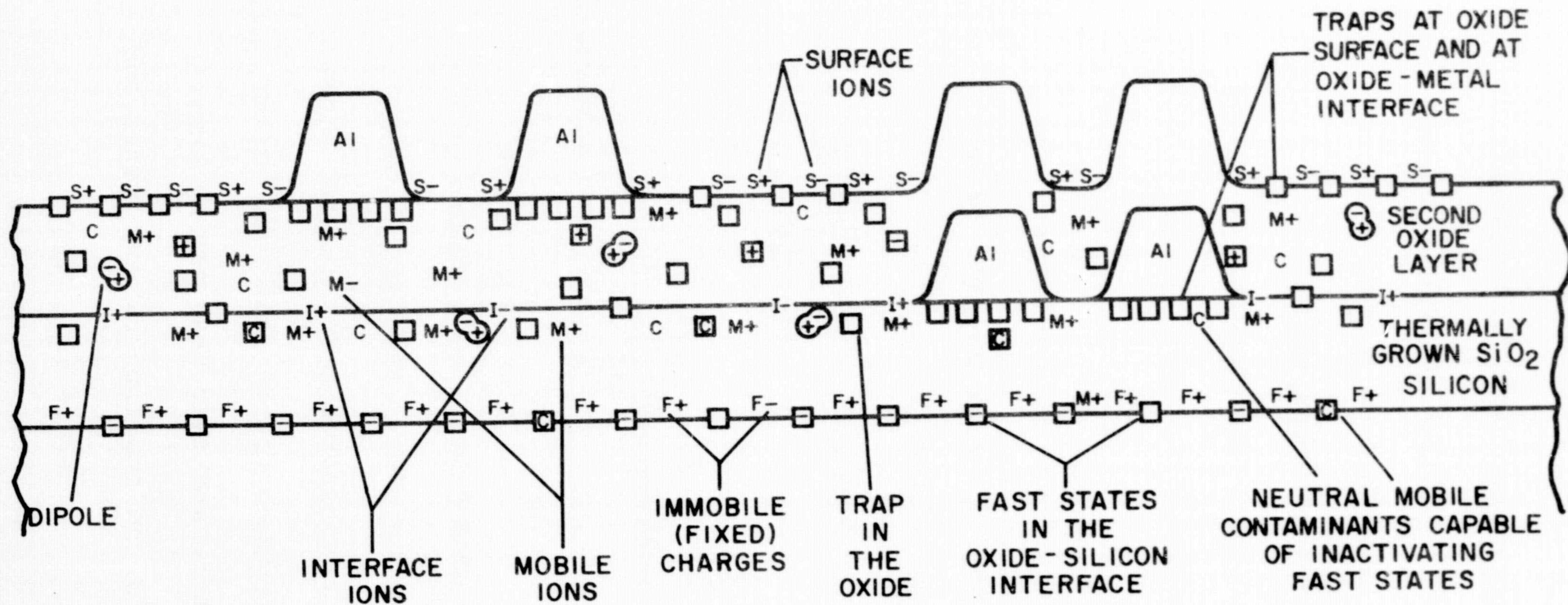
Model of Charge Distribution in Multilevel MOS Structure

To facilitate the understanding of the electrical factors influencing LSI circuit reliability, we have developed the model given as Figure 1 that depicts the charge distribution in an MOS structure having two insulator layers and two metal layers. The following charges and states are embodied in Figure 1.

Immobile Charge. - This charge, usually designated as Q_{SS}, is generally found to be positive. Its nature is summarized in a paper by Deal, et al.[10].

Mobile Charge in the Oxide. - Extensive investigations have established that the mobile charges found in oxides made with today's technology are sodium ions[11] and protons -- both cations[12]. Kuper et al.[13] have shown the existance of mobile anions at temperatures above 800°C. Mobile charge is frequently designated as Q_O.

Charge on the Oxide Surface. - We include three kinds of charge on the oxide surface -- mobile cations and anions and immobile charge. The specific types of charge that exist at the oxide surface have not yet been determined. The kinetics and behavior of mobile surface ions have been studied by various investigators[14, 15, 16, 17].



OTHER FACTORS

METAL - SEMICONDUCTOR WORK FUNCTION DIFFERENCE

INSULATOR - INSULATOR CONTACT POTENTIAL

SCALES

VERTICAL ······ = 1.0 MICRON (10,000 Å)

HORIZONTAL ··· = 6.0 MICRONS (0.25 MIL)

Figure 1. Factors influencing silicon surface potential.

Ions at the Insulator-Insulator Interface. - The existence of mobile ions at the insulator-insulator interface has not yet been experimentally established but the possibility of their existence cannot be excluded at this time.

Traps. - Traps near the oxide-silicon interface can be filled and emptied by the tunnelling of carriers from the silicon -- these traps are also referred to as slow states. Traps that are farther away from the interface are filled by ionizing radiation and can be emptied with ultraviolet light or heat. Slow trapping has been discussed by Hofstein[18].

Barrier Energy Difference Between Metal and Semiconductor. - The metal and semiconductor barrier energy difference has been discussed by Deal, et al.[19].

Contact Potential Between Insulator Layers. - The insulator-insulator contact potential for Al_2O_3 and SiO_2 has been discussed by Nigh, et al.[20, 21].

Fast States. - Fast states have been studied by a number of investigators by a variety of techniques. Fast states are believed to be associated with unsatisfied bonds at the oxide-silicon interface. It has been demonstrated that fast states can be created by a vacuum bake[22], and that they can be annihilated by a hydrogen bake or by the reaction between water and a reactive metal[23, 24].

Mobile Ion Trapping at Interfaces with the Oxide. - Hofstein[12] has postulated that traps exist at the oxide-metal interface that capture mobile charge in the oxide. This postulate was made to explain the asymmetry in charge motion through the oxide. Szedon[25] has postulated that deep traps exist at an interface between silicon dioxide and silicon nitride in order to explain the observed instability found in double-layer insulator structures containing these two materials. Frohman-Bentchkowsky and Lenzlinger[26] have discussed a model for the charge transport and storage at the interface between silicon dioxide and silicon nitride. They proposed that steady state currents flow through these layers and that the charge trapped at this interface is determined by the balance of the currents.

Mobile Ion Trapping at the Outer Oxide Surface. - We have included the possibility that the outer surface of the oxide can act as a getter for mobile ions from the interior of the oxide or for surface ions that would otherwise be mobile.

Dipoles. - Phosphosilicate glass has been shown[27] to have a polarizability of the dipole type.

Influence of Surface Potential

Each of the above charges and states influences the surface potential of the semiconductor. This surface potential:

1. Determines whether or not a channel exists.
2. Influences the surface carrier generation or recombination rate, thereby influencing the current of a diode at a reverse bias.
3. Influences the width of a depletion layer at the edge of a p-n junction, and thereby influences the following:
   a. The drain-to-source punchthrough voltage of an MOS transistor;
   b. The diode breakdown voltage of a p-n junction;
   c. The lateral punchthrough voltage between adjacent parts of a complex microcircuit structure;
   d. The effective channel length of an MOS transistor, and therefore the transconductance of an MOS transistor.
4. Influences the threshold voltage of MOS transistors.

Influence of Fast States

In addition to their influence on the surface potential, fast states influence:

1. The surface generation or recombination rates, and thereby influence:
   a. Diode leakage current,

b. Bipolar transistor (double-diffused and lateral) current gain, especially at low current levels.

2. The dependence of the semiconductor surface potential on the voltage on the oxide surface due to charge on the surface or on an overlying metal, and thereby influences:

   a. The threshold voltage of an MOS transistor. This is increased because surface states must be filled before an inversion layer of mobile carriers can be established.

   b. Field inversion voltages, for the same reasons as in a.

   c. The capacitance-voltage relationship of an MOS capacitor.

   d. The transconductance of an MOS transistor.

   e. The effect of temperature on the semiconductor surface potential.

Influence of Carrier Mobility

An additional electrical property of the semiconductor surface that is not shown in Figure 1 is the mobility of carriers in the inversion layers. Information about the inversion layer carrier mobility is included in References 18, 28, 29, and 30.

The inversion-layer carrier mobility is an important determinant of the transconductance of MOS transistors.

COMPLEX MIGRATION OF IONS

In addition to the relatively simple factors, influencing the surface potential, shown in Figure 1, complex migration of ions must also be taken into account in studies of the electrical properties of the MOS system.

Interaction of Ions in the Oxide with Ions on the Oxide

The interaction of mobile ions in the oxide with mobile ions on the oxide surface increases the effect of the surface ions. According to the model for the effects and behavior of surface ions, the highest voltage that develops across an oxide due to surface ions in a region adjacent to a metal is the voltage applied to the metal. One can calculate the thickness of oxide that prevents surface-ion-induced inversion by a given operating voltage. The microcircuit structure can then be designed to have this thickness of oxide in all of the regions on the chip that must not invert, thereby preventing circuit failure due to surface-ion-induced inversion. However, if there are mobile ions in the oxide, they can greatly increase the effect of the surface ions and cause inversion at the lower applied voltages than could be caused by the surface ions alone. Figure 2 illustrates this mechanism. Positive surface charge would cause mobile ions in the oxide to move in the direction to make the net charge in the

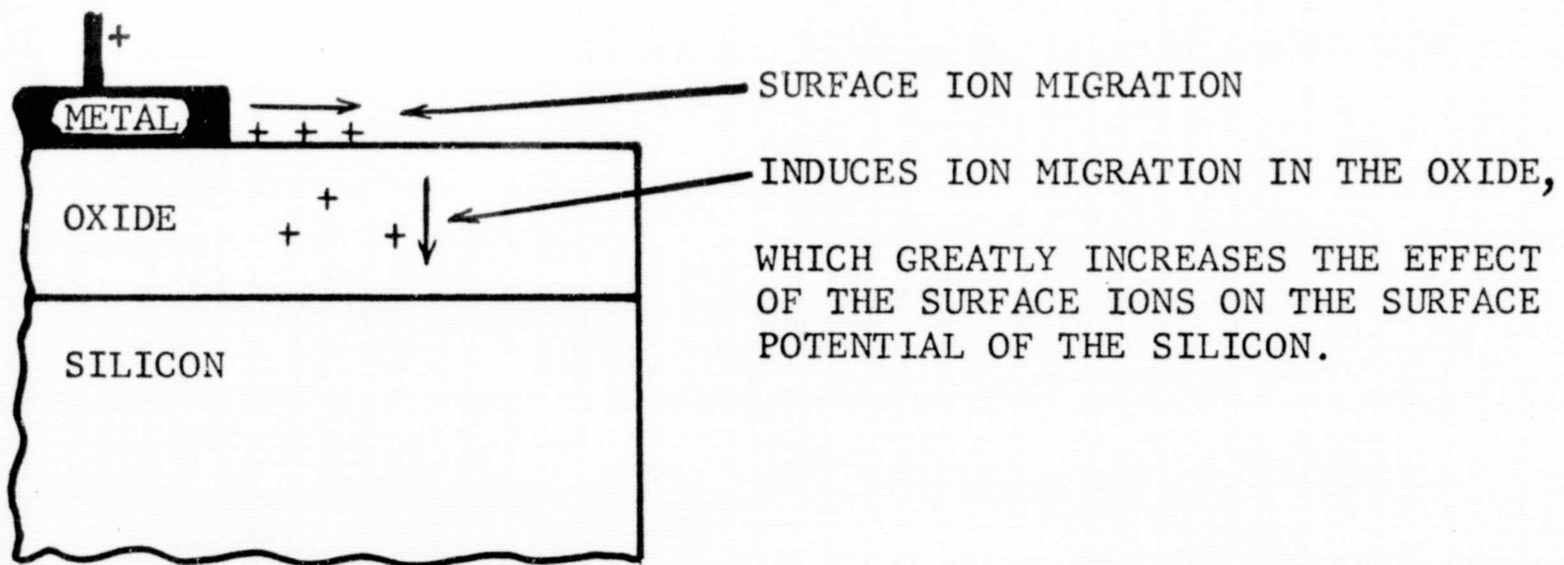


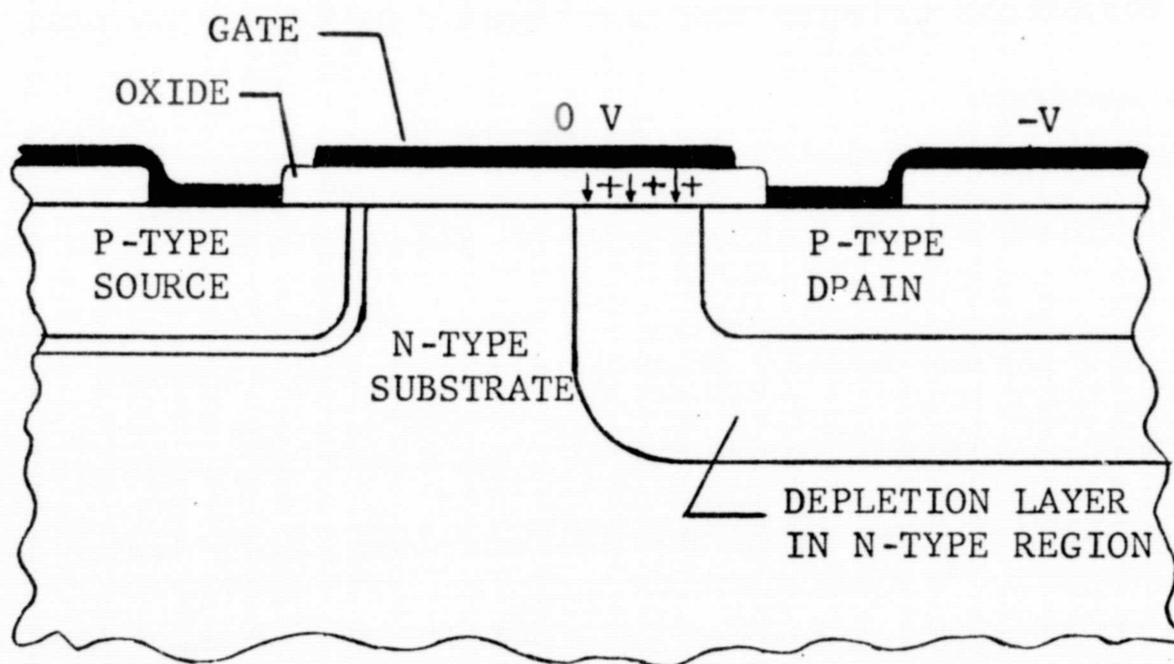
Figure 2. Interaction of ions on the surface and in the interior of the oxide.

oxide near the silicon more positive and, conversely, negative surface ions would cause mobile charge in the oxide to move in the direction to make the net charge in the oxide near the silicon more negative.

Drift of Mobile Charge Between Metal and Diffused Regions

All of the mobile charge in the oxide observed to date is positive. Since this is found[27] to drift spontaneously toward the metal and away from the silicon, one might infer that, under the application of a negative voltage to the gates and drains of p-channel devices in an MOS microcircuit, the mobile charge in the oxide would hardly affect the surface potential of the silicon. However, there are points in the structure where the metal may be at ground or substrate potential while diffused p-type regions (sources, or drains of MOS transistors, diffused resistors or crossunders) are at a negative potential. In this situation, negative applied voltages cause positive mobile ions in the oxide to drift toward the silicon. An example of this is illustrated in Figure 3.

PART OF MOS TRANSISTOR



NEGATIVE VOLTAGE ON DRAIN AND ZERO VOLTAGE ON GATE DRIFTS POSITIVE IONS TOWARD SILICON, CAUSING AN INCREASE IN THRESHOLD VOLTAGE AND A DECREASE IN TRANSCONDUCTANCE.

Figure 3. Example of positive ion drift toward silicon under negative applied voltage.

TEST STRUCTURES

In Interim Scientific Report No. 1, we described a set of basic test structures that had been prepared to provide a means for measuring the fundamental electrical properties of the insulator-silicon interface. In Interim Scientific Report No. 2, we discussed the effective use of these test structures, possible improvements that might be made in them, and a number of ways in which they could be used for process control and for the analysis of yield and reliability problems. In the portion of the program covered by this report, we have extended our understanding and use of test structures in the following ways.

1. A standard routine procedure has been set up in which test patterns are used to monitor the quality of the materials, processes and equipment used for fabricating microcircuits.
2. New test structures have been designed to have improved sensitivity and decreased area requirements.
3. Specific sets of test structures have been suggested for several specific applications.
4. An analysis has been made of the types of area that should be evaluated in MOS and bipolar microcircuit structures.
5. Techniques have been proposed for conserving the chip-area requirements of test structures.

Quality Control Monitoring

We have set up a standard routine procedure for maintaining a continuing record of our control of the quality of the materials, processes, equipment and procedures used in the fabrication of microcircuits. The test structures used in this effort are MOS capacitors built with 2000 Å of oxide grown thermally in dry oxygen. To monitor the chemicals, the glassware, the handling procedures and environment, and the oxidation tube and sample oxidation ambient, sample MOS capacitors are prepared at least once each week. The immobile and mobile (both at 300°C and then at room temperature) are measured in these capacitors. We also monitor the aluminum evaporator system. For this we maintain a supply of wafers that have been oxidized in large lots that were determined to be free of mobile charge. One of the wafers from this supply is metallized with each batch of wafers to be metallized so that any mobile-ion contamination from the metallizer system will be detected.

The dryness of the gases used for the oxidation and the subsequent anneal and cooling are evaluated by the use of MOS capacitors formed by a gold ball probe, shown in Figure 4, and unmetallized, oxidized wafers. The fast state density is measured by the technique of Brown and Gray[22]. They have shown that fast state densities fall sharply as the water content of the oxidation ambient is decreased.

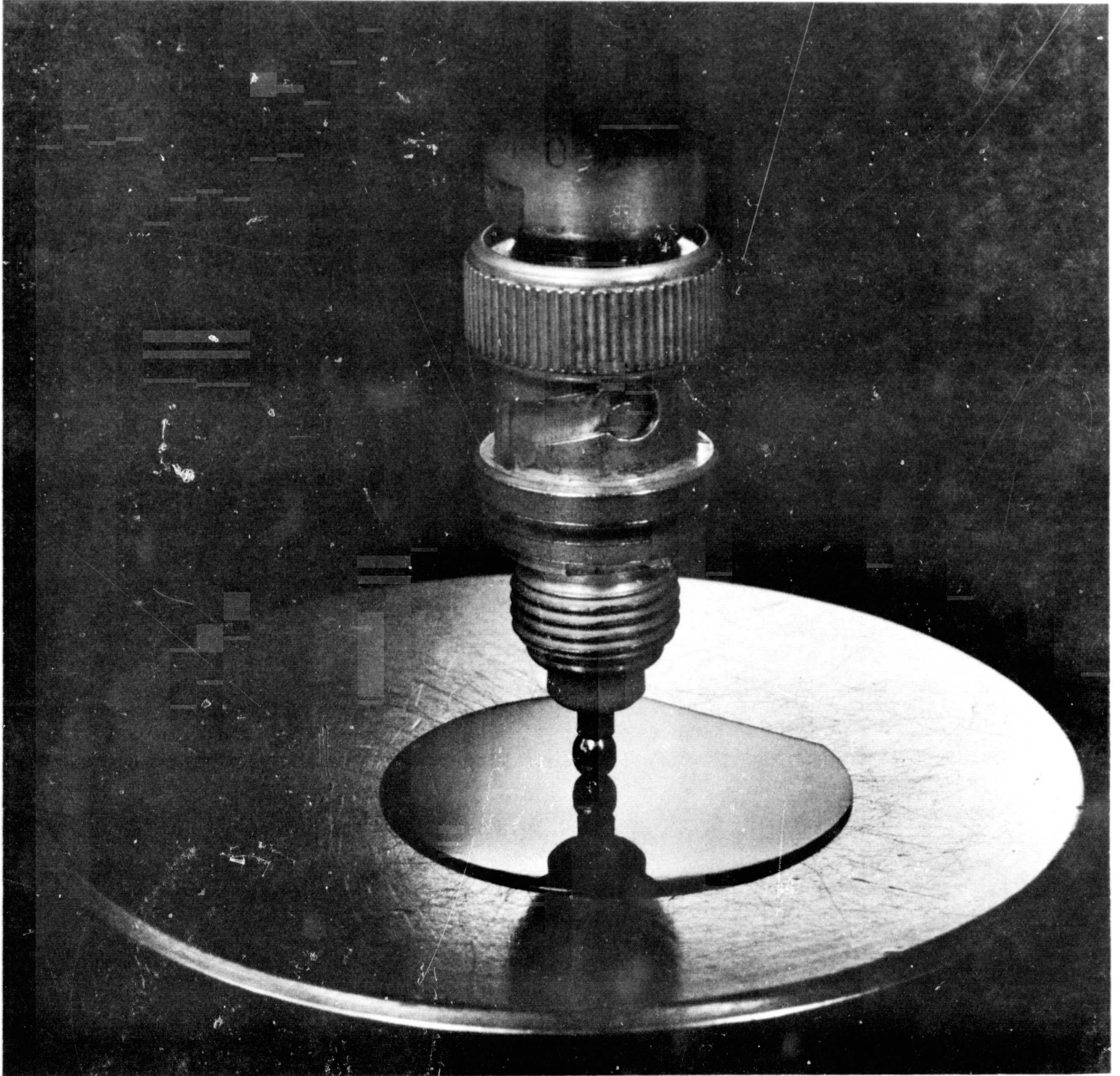


Figure 4. Gold ball probe.

The ability to measure fast state densities before the metal is deposited simplifies the processing required to make the evaluation and, more importantly, increases the sensitivity of the test. (Later in this report we show that the metal evaporation process decreases the density of fast states.) As we now perform this test, the gold probe and the oxide are immersed in liquid nitrogen for the measurement of the capacitance-voltage curve at the low temperature. We find this adds a large amount of mobile charge to the oxide. This contamination may come from the vessels used to hold the liquid nitrogen.

Improved Test Structures

We have made two design improvements to increase the sensitivity of the test structure for the measurement of the effects of surface ions. First, we have digitated the gate electrode. Second, we have added the capability to cut an opening in a second layer of dielectric material that was deposited over the metal layer. This cut in the second dielectric layer was introduced on the assumption that it would increase the ease with which surface ions can move from the metal to regions on the top surface of the oxide.

We have added to the set of available test structures a digitated junction diode to make the diode reverse current more sensitive to the properties of the surface.

Types of Application of Test Structures

In addition to the improvements that have been made in the set of available test structures, we have developed a better understanding of the considerations that relate to the most effective use of these test structures. We have considered a number of types of application for which test structures might be useful. This report discusses test structure sets for five kinds of applications:

1. Preliminary evaluation of experimental materials or processes,
2. Development of promising materials or processes,
3. General use in MOS microcircuit production,
4. General use in bipolar microcircuit production,
5. Specific use on individual microcircuit types, formed by a change in the metal pattern.

In the following sections of this report we discuss in detail sets of test structures for five types of application.

<u>Test Structures for the Preliminary Evaluation of Experimental Materials and Processes.</u> - For the preliminary evaluation of experimental materials or processes, we use MOS capacitors. Unmetallized oxides can be evaluated using a simple gold ball probe to create an MOS capacitor to measure the surface potential and the fast state density (by the technique of Brown and Gray[22]).

Metallized oxides (metallization can be deposited through a metal mask to avoid the time, cost and inconvenience of the photolithographic and metal etching processes) can be studied by contacting the metal electrode of each MOS capacitor on the wafer. In particular, one can evaluate the mobile ion content and both slow and fast state effects of metallized capacitors on the wafer.

Test Structures for the Development of Promising Materials and Processes. - For the development of promising materials and processes, we have made extensive use of the set of test structures shown in Figure 5. This 70 x 70 mil chip contains:

1. A large area MOS capacitor for measuring surface potential and its stability.
2. A digitated MOS capacitor for studying the migration of contaminants from areas adjacent to areas beneath the metal.
3. An MOS transistor for measuring threshold voltage and the mobility of carriers in the inversion layer.
4. An MOS transistor with a gate width that is smaller than the channel width formed by the source and the drain -- for studying surface ion effects. This transistor is referred to hereinafter as the surface-ion MOS transistor.

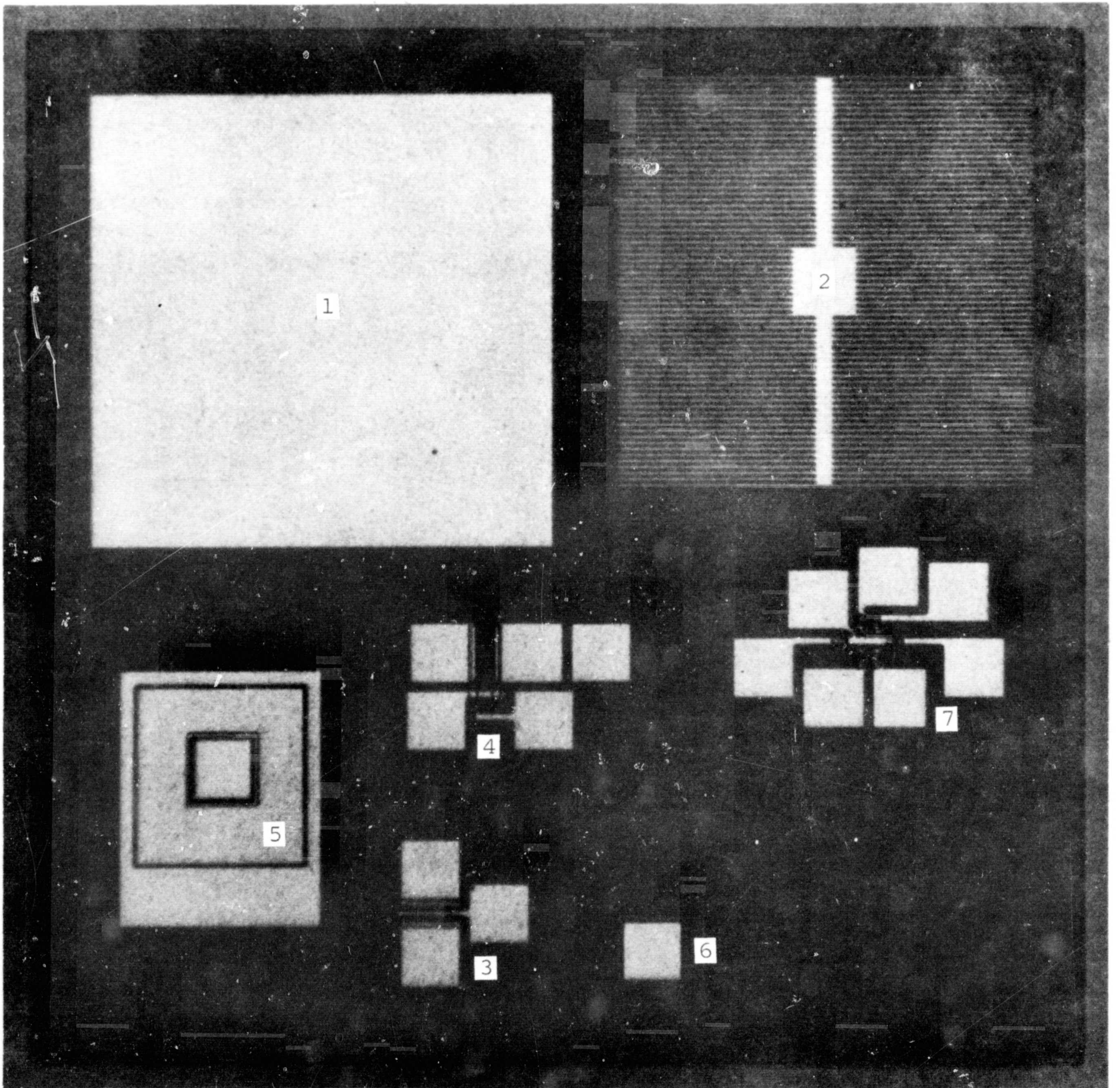


Figure 5. Basic test structure chip.

5. A gate controlled diode for studying surface recombination velocity.

6. A p-n junction with an internal contact for measuring diode reverse currents and breakdown voltages.

7. An MOS transistor with the configuration for measuring the Hall mobility of the carriers in the inversion layer.

Test Structures for General Use in MOS Microcircuit Production. - From the experience obtained with the initial set of test structures shown in Figure 5, we have designed a set of test structures for general use in MOS microcircuit production. MOS microcircuits having a single layer of oxide and a single layer of metal have three types of areas to be evaluated:

1. The areas of thin oxide found under the gates of the MOS transistors,

2. The areas of thick oxide (like that in the field of the microcircuit) covered by metal,

3. The areas of thick oxide not covered by metal.

The set of test structures that we have selected for single layer MOS microcircuits includes:

1. MOS capacitors on

   a. Gate oxide,

   b. Field oxide;

2. MOS transistors on

   a. Gate oxide,

   b. Field oxide;

3. Surface-ion MOS transistor on field oxide;

4. Gate controlled diode for measuring surface recombination velocity under field oxide;

5. Lateral bipolar transistor;

6. Diffused junction diodes:

   a. Some with high and some with low periphery-to-area ratio,

   b. With the edge of the junction in the three types of areas mentioned above.

The above structures have been designed on a single chip having dimensions that are equal to or smaller than the chips of nearly all of the MOS microcircuits now in or planned for production.

The MOS capacitors permit one to measure surface potential and its stability under gate and field oxides. MOS transistors permit one to measure the fundamental parameters of the basic component in the circuit. Comparisons of measurements taken on capacitors and on transistors can be used to determine the causes of undesirable or variable threshold voltage levels in MOS transistors. The transconductance of MOS transistors can be used to measure the mobility of the carriers in the inversion layer.

We believe that it is desirable to include MOS transistors having different channel lengths.

The surface-ion MOS transistor permits one to measure instability due to surface ions. Further, it provides some information on the inversion voltage in the field regions not covered by metal -- which voltage might not always be the same as the field inversion voltage in a region covered by metal. If the surface-ion MOS transistor is designed to have a significantly longer channel than the conventional MOS transistor, it can be used to study the effects of channel length on transistor characteristics. The surface-ion MOS transistor could also be measured in the bipolar mode as a lateral transistor to obtain a measure of the surface recombination velocity or fast state density in a region not covered by a metal. (The effect of surface potential on the beta of bipolar transistors has been investigated by Sah[31,32].) The effect of surface ions on the surface recombination rate could also be studied with this test structure. To increase the sensitivity of the surface-ion MOS transistor to surface ion effects, we have designed the gate to be digitated so that the area capable of being affected by surface ions is relatively large compared with the area under the gate. Also, the mean distance of areas capable of being

influenced by surface ions from the metal is short so that the time required to produce surface-ion-inducing channels is short.

Kooi[33] has demonstrated that surface state densities can be determined from a comparison of the capacitance-voltage curve of an MOS capacitor and the drain current-gate voltage curve of an MOS transistor. The capacitance of an MOS capacitor becomes insensitive to voltage, in the region of lower capacitance, when either an inversion layer forms or when fast states are being filled or emptied. The conductance of an MOS transistor increases only after the fast states are filled. Therefore, if fast states are present, the voltage at which the capacitance become insensitive to voltage is not the same as the voltage at which the transistor becomes conductive. The difference between these two voltages is a measure of the fast state density.

The fast state density can be measured in an MOS transistor by the technique developed by Heiman and Miiller[34]. In this technique, the rate of change in the gate voltage necessary to maintain a constant drain current, as the temperature is being varied, is used to calculate the fast state density.

Fast state densities can also be measured using MOS capacitors. Deal, et al.[24] have described how an MOS capacitor on a silicon substrate that contains a p-n junction adjacent to the capacitor, (the gate controlled diode in our set of test structures) can be

used to measure the fast state density. Since the presence of the p-n junction permits the inversion layer carrier density to follow changes in the signal voltage, the measured capacitance in the inversion region approaches that of the oxide. A comparison of the capacitance-voltage curve of such a capacitor taken at room temperature and at 78°K shows that both of the rapidly changing (with voltage) parts of the curve shift along the voltage axis due to the change in temperature. The magnitude of these shifts is a measure of the number of fast states whose occupancy is changed between accumulation and inversion. The reason for the shifts in the characteristic capacitance-voltage curve can be understood as follows. Brown and Gray[22] have shown that the shift occurs at the accumulation end of the curve because the change in temperature causes a change in the number of fast states that are filled because the Fermi level moves closer to the band edge. The shift in the inversion part of the curve is due to the filling of the fast states before the inversion layer forms. This shift occurs for the same reason as the shift in the turn-on voltage in the transistor characteristics described by Kooi[33].

Fast state densities can also be measured on MOS capacitors without the presence of a nearby p-n junction by a technique developed by Nicollian and Goetzberger[35,36]. They have shown

that the a-c conductance of an MOS capacitor provides a quantitative measure of the fast state density.

Qualitative information concerning fast state densities can be obtained from diode reverse currents and from the low-current beta of lateral bipolar transistors. A comparison of measurements taken on a gate controlled diode with those taken on a diode with an internal contact provides a means for studying differences between regions covered by a metal and those that are not.

Test structures for MOS circuits having second layers of dielectric and/or of metal should include additional test structures to study the effects of the additional layers of oxide and metal. The additional structures should include MOS capacitors, transistors and a gate controlled diode, all having the metal on top of the second oxide layer. An additional lateral bipolar transistor or a diode with an internal contact are not needed because measurements taken on those that are included in the set of structures built to characterize the first-layer oxide will be influenced by the second-layer oxide.

<u>Test Structures for General Use in Bipolar Microcircuit Production.</u> - Test structures for general use in the bipolar microcircuits should include those used for MOS microcircuits. MOS capacitors

and transistors are used because they provide basic information about the surface potential. In this connection, it can be noted that MOS capacitors and MOS transistors provide similar information and that each of these types of devices has some advantages. Capacitors yield a more explicit measure of the flatband voltage and of the surface potential. Capacitors are also useful for measuring oxide thickness and the resistivity of the silicon. On the other hand, transistors use less of the chip area. Transistors are sufficiently small that several can be included on each chip. Further, transistors can be used to evaluate the surface potential of silicon having a higher density of dopant atoms than can MOS capacitors. For this reason MOS transistors can be used to provide a useful qualitative measure of the control of the diffusion layer used for the bases of bipolar transistors.

Bipolar microcircuit structures contain both p- and n- type regions having relatively low dopant density. The process used to fabricate bipolar microcircuits permits one to make test structures in both types of regions. This is, in a bipolar microcircuit having npn transistors, the base diffusion can be used to form the source and drain regions of a p-channel MOS transistor, and the emitter diffusion can be used to form the source and drain regions of an n-channel MOS transistor.

Test structures for bipolar microcircuits should include discrete bipolar transistors to provide data on the basic component in the microcircuit.

A set of test structures for bipolar microcircuit wafers having a single metal layer should include the following:

1. MOS capacitors on collector region;
2. MOS transistors on
    a. Collector region,
    b. Base (and resistor) region;
3. Surface-ion MOS transistors on
    a. Collector region,
    b. Base region;
4. Gate controlled diode;
5. Bipolar transistors of each type in the circuit:
    a. Double diffused,
    b. Lateral,
    c. Substrate collector;
6. Diffused junction diodes:
    a. High and low periphery-to-area ratio,
    b. Both within the collector and within the base.

Bipolar microcircuits with more than one layer of dielectric and of metal require additional test structures of the same kind and for the same reasons as those described above for MOS microcircuits.

Test Structures for Specific Use on Individual Microcircuit Types, Formed by a Change in the Metal Pattern. - As an alternative approach to the building of general purpose test structures for an entire family of circuits, one can build custom test structures for a specific microcircuit type, with little more than a modification of the metal pattern. One can form test structures in a standard microcircuit chip that has been processed as a production wafer up to the point of metallization. Examples of test structures that can be made in standard bipolar microcircuit chips by a simple change in the metal pattern include:

1. Discrete bipolar transistors of each basic type existing in the chip. The basic types are:
   a. Double-diffused transistors (npn),
   b. Lateral bipolar transistors (pnp),
   c. Substrate collector bipolar transistors (pnp).
2. MOS transistors
   a. In an npn bipolar chip, isolation, base, or diffused resistor regions can be used as source and drain regions of p-channel MOS transistors.
   b. Similarly, in the same type of chip, the collector and emitter regions can be used as source and drain regions of n-channel MOS transistors.
3. Junction diodes.

Figure 6 is a photograph of test structures we have made by a change in the metal pattern of a PA7709 high performance operational amplifier. The chip shown in Figure 6 contains a standard production microcircuit structure with the exception of the metallization pattern. The metallization pattern was formed on five widely separated chips on a 1-1/2" diameter wafer. The test structures include:

1. An MOS capacitor on the n-type (collector) silicon,
2. A p-channel MOS transistor formed by contacts to each of two diffused resistors and a metal gate.
3. An n-channel MOS transistor formed by two diffused regions (that were formed by the emitter diffusion) and a metal gate. Note that both the p- and n-channel MOS transistors have a gate width that is narrow compared to the width of the source and drain regions. This makes these structures sensitive to surface ion effects and therefore provides a means for studying the effects of surface ions on the circuit.
4. Contacts to diffused resistors to monitor the line width of the resistors and the parameters of their diffusion layer.
5. A discrete lateral pnp bipolar transistor.

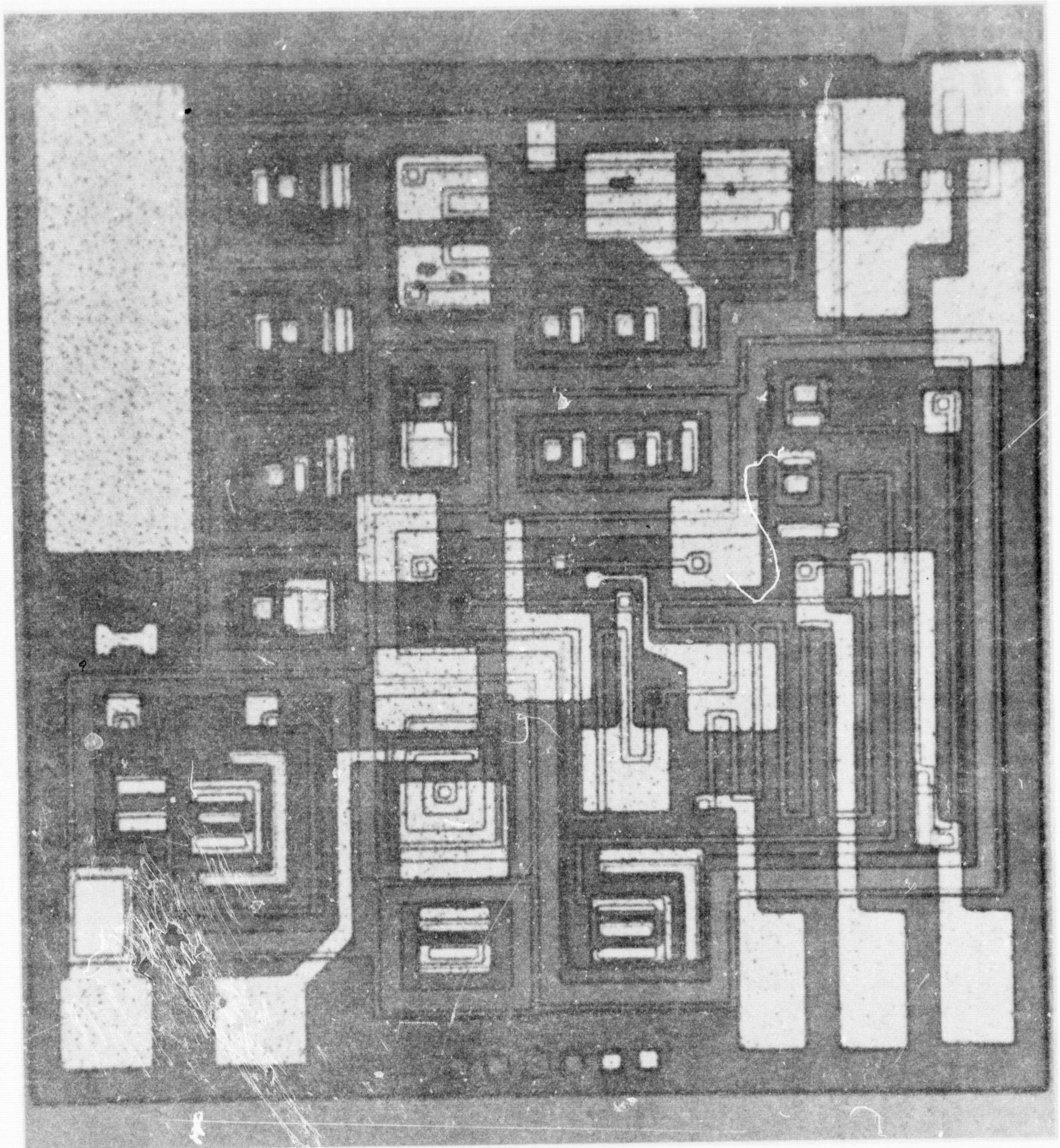


Figure 6. Test structures created by a change in the metal pattern on a production microcircuit.

6. Land areas for probing other discrete devices.

7. A region indicated by the arrow in Figure 6 for measuring the thickness of a second insulator layer.

Area Conservation

Chip area can be saved by several techniques. The capacitor having the high periphery-to-area ratio that was described in the earlier reports can be replaced by the surface-ion test structure having the digitated gate. An MOS transistor can be made significantly smaller in area than an MOS capacitor. Also, the digitated gate MOS transistor combines into one structure the ability to measure the migration of contaminants from regions adjacent to regions beneath a metal and the ability to measure the effects of surface ions. We show later in this report that a p-n junction can influence the immobile charge density in its vicinity. For this reason, the channel length of the surface-ion test structure should be at least one mil in length to minimize such effects of the p-n junction. Chip area can also be conserved by using a single contact for more than one test structure. An obvious example of this is the use of one land for the gates of two or more MOS transistors.

EXPERIMENTAL DATA

Fast States

We have used a gold ball probe to measure fast state densities by the technique of Brown and Gray[22] in unmetallized oxides using the gold ball probe shown in Figure 4. Silicon wafers (⟨111⟩ oriented, phosphorus doped, 5 ohm-cm resistivity) were polished and HCl etched at 1200°C. They were then immersed in a mixture of H_2SO_4 and HNO_3, and rinsed in H_2O. They were oxidized in dry oxygen to a thickness of 1700 Å at 1150°C. The oxidation was terminated by a bake in dry N_2 for 15 minutes at 1150°C in situ. They were then removed from the furnace by a technique that insures the dryness of the ambient during the process of cooling to room temperature. The measured charge densities are given in Table I.

Evaluation of Candidates for Second Layer Oxide Materials and Processes

We have also used simple MOS capacitors for the preliminary evaluation of a number of possible candidates for second-layer oxide materials and processes. Data from the first two Interim Scientific Reports are summarized in Table II.

During the period covered by this report, we have evaluated additional samples of vapor plated Al_2O_3, several samples of vapor plated titanium oxide, and SiO_2 layers that were r-f sputtered from a target having the highest available purity.

TABLE I

Fast State Densities (Gray and Brown), Measured with Gold Ball Probe

	10^{11} Fast States/cm^2
Oxide Grown Thermally in Dry Ambient	24-40
H_2 Bake, 350°C, 30 min.	7
H_2 Bake, 350°C, 120 min.	7
H_2O Boil, 5 min.	30
H_2O Boil, 60 min.	10
Metallized (Al)	13
Metallized and Alloyed (550°C)	<1
Metallized, Metal Removed, 550°C Bake	6-25
Bake at 300°C, 45 min., 10^{-6} Torr, Subsequently metallized and alloyed	3

TABLE II

Typical Measured Charge Densities in Various Kinds of Oxides on Thermally Grown SiO_2

Oxide Type	10^{11} Charges/cm^2		
	Immobile	Mobile (300°C)	Mobile (25°C)
None, Control	2	0.5	0.1
Vapor-plated SiO_2	8	5	0.1
Vapor-plated phosphosilicate (3% phosphorus by weight)	2.6	1	0.1
R-F sputtered SiO_2	3	28	1.0
Vapor-plated Al_2O_3	5	20	---
Evaporated Al_2O_3	-4	20	---
Vapor-plated mixed Al_2O_3-SiO_2	-1.5	3	---

Vapor Deposited Aluminum Oxide. - We have vapor plated aluminum oxide at 400°C over 2000 Å thick layers of thermally grown SiO_2. The thickness of the Al_2O_3 was 6000 Å.

Because of our uncertainity of the exact values of the insulator-insulator contact potential and of the polarity of the mobile charge, we report the measured electrical properties in terms of flatband voltages rather than in terms of charge densities. We have measured the effective charge density after each of the following drift steps:

Initial

After ±100 V at 27°C for 15 minutes;

After ±100 V at 300°C for 12 minutes;

After ±100 V at 27°C for 15 minutes.

The measurements, summarized in Table III, support the data in Scientific Interim Report No. 1 in which we reported that aluminum oxides deposited at 400°C are highly unstable. Also, as previously reported, we find that the instability ranges from strongly negative to strongly positive net charge in the oxide.

TABLE III

Flatband Voltage

Sample		27°C		300°C		27°C	
Number	Initial	-100V	+100V	-100V	+100V	-100V	+100V
920	-10V	-8V	-13V	+74V	-90V	+65V	-86V
921	-9V	-7V	-12V	+57V	-83V	+47V	-78V

It is our understanding that all of the stable Al_2O_3 layers reported in the literature were deposited at higher temperatures (>800°C). These high temperatures are incompatible with the processes used for building multilevel microcircuits.

Vapor Deposited Titanium Dioxide. - Lepselter[37] has indicated that the use of titanium in beam-lead sealed-junction technology imparts improved properties to dielectric layers. We have conducted a few preliminary experiments to evaluate titanium oxide that is vapor plated at 400°C. The reactants were tetra-iso-propyl-titanate (TIPT) and oxygen, with nitrogen as a carrier.

The test samples were made with a first layer of 5500 Å of thermally grown SiO_2 and a second layer of roughly 4500 Å of titanium oxide. These thicknesses were determined by angle lapping and counting fringes and assumming the index of refraction of titanium oxide to be 2.7. Table IV shows the conditions by which the layers were deposited.

TABLE IV

Deposition Conditions for Titanium Oxide Layers

Wafer Number	TIPT (cc/min)	O_2 (cc/min)	Temperature (°C)	Time (Minutes)
948	500	300	400	15
949	500	600	400	15
950	500	900	400	15
951	500	1200	400	15

We fabricated MOS capacitors and measured the effective charge densities in the oxide. For these exploratory experiments, we chose to use an evaporator system that contaminates the samples with mobile charge. Hence our control sample had a mobile charge density of 12×10^{11} cm^{-2}. The mobile charge densities were measured at room temperature, then at 300°C, and again at room temperature. The measured charge densities are given in Table V.

TABLE V

Measured Charge Densities in Titanium Oxide

Sample Number	10^{11} Charges/cm^2 Immobile	Mobile 27°C	Mobile 300°C	Mobile 27°C
947*	4.4	0.2	12.0	8.0
948	4.0	<0.1	1.7	1.7
949	3.7	<0.1	3.2	1.6

*(Control, no second layer oxide)

We were unable to take significant data from Samples No. 950 and 951 because the capacitors had a high leakage current. We do not understand why the 5000 Å thick layer of thermally grown SiO_2 developed such a high leakage current.

These initial results appear to indicate that titanium oxide getters, or is a barrier to, mobile ions. The severity of the leakage current problem has not yet been determined.

If titanium oxide is to be used in microcircuit fabrication, more work will need to be done to develop a good etchant for this material. Harbison and Taylor[38] have recently reported that titanium oxides vapor deposited at temperatures below 850°C exhibit poor electrical properties and are not stoichiometric TiO_2.

R-F Sputtered SiO_2. - As a follow-up to the work done early in the program to evaluate r-f sputtered SiO_2 layers as a potential second layer oxide material, we have prepared r-f sputtered SiO_2 layers from a purer target. The analysis of the purer target follows. These data were provided by the supplier, Thermal American Fused Quartz Company, Montville, N.J., and were taken on samples similar to those supplied to us.

Material	PPM
Al	<0.02
Sb	<0.0001
As	<0.0002
B	<0.01
Ca	<0.1
Cu	<0.0002
Ga	<0.004
Fe	<0.1
Mn	<0.001
P	<0.001
K	<0.004
Na	0.04

Measurements taken on the sputtered oxides made with the purer target revealed the following information:

1. Sample No. 903 consisted of 7000 Å of sputtered oxide on bare silicon. It had an initial charge density of 45 x 10^{11} cm^{-2}. Room temperature drift tests (15 min.) shifted this to 39 x 10^{11} under -36 V and to 40 x 10^{11} under +36 V. Next, the samples were drifted under ±36 V at 300°C for 12 minutes. This shifted the charge densities to 55 x 10^{11} for -36 V and to 83 x 10^{11} for +36 V. The drift voltage polarities were then reversed and they were maintained at 27°C for 15 minutes; then the charge densities were remeasured to be 60 x 10^{11} at -36 V and 87 x 10^{11} at +36 V.
2. Sample No. 901 was prepared in the same way as Sample No. 903 except that it had a 2000 Å layer of thermally grown oxide on the silicon before the 7000 Å sputtered oxide was deposited. This sample initially contained 9 x 10^{11} charges/cm^2. The first drift at room temperature shifted this to 35 x 10^{11} at -36 V and to 38 x 10^{11} at +36 V. At 300°C, the charge densities shifted to 31 x 10^{11} at -36 V and to 54 x 10^{11} at +36 V. Then, under reversed polarities, they shifted at room temperature to 32 x 10^{11} at -36 V and to 56 x 10^{11} at +36 V.

On the basis of these results, which are consistent with the earlier results reported in Interim Scientific Report No. 1 in November 1967, we have concluded that r-f sputtered oxides are not as promising as second-layer oxide materials as are vapor plated oxides. Further, the simplicity of the vapor plating equipment and techniques, in comparison with those of r-f sputtering, also leads us to favor vapor plating for the preparation of second-layer oxides.

Surface Conductivity

We tried to directly measure the conductivity of oxide surfaces by means of the test structure shown in Figure 7. In this structure an interdigitated pair of electrodes forms on the oxide surface a conducting channel that has a width-to-length ratio of 5000. Information gained from this structure would be useful to supplement the information obtained from the surface-ion MOS transistor used in our previous work and to provide the means for further testing of our model. On the basis of the work so far completed, we conclude the following:

1. The direct measurement of surface conductivity is very difficult. A serious problem is the lack of knowledge of the amount of the current that flows through the

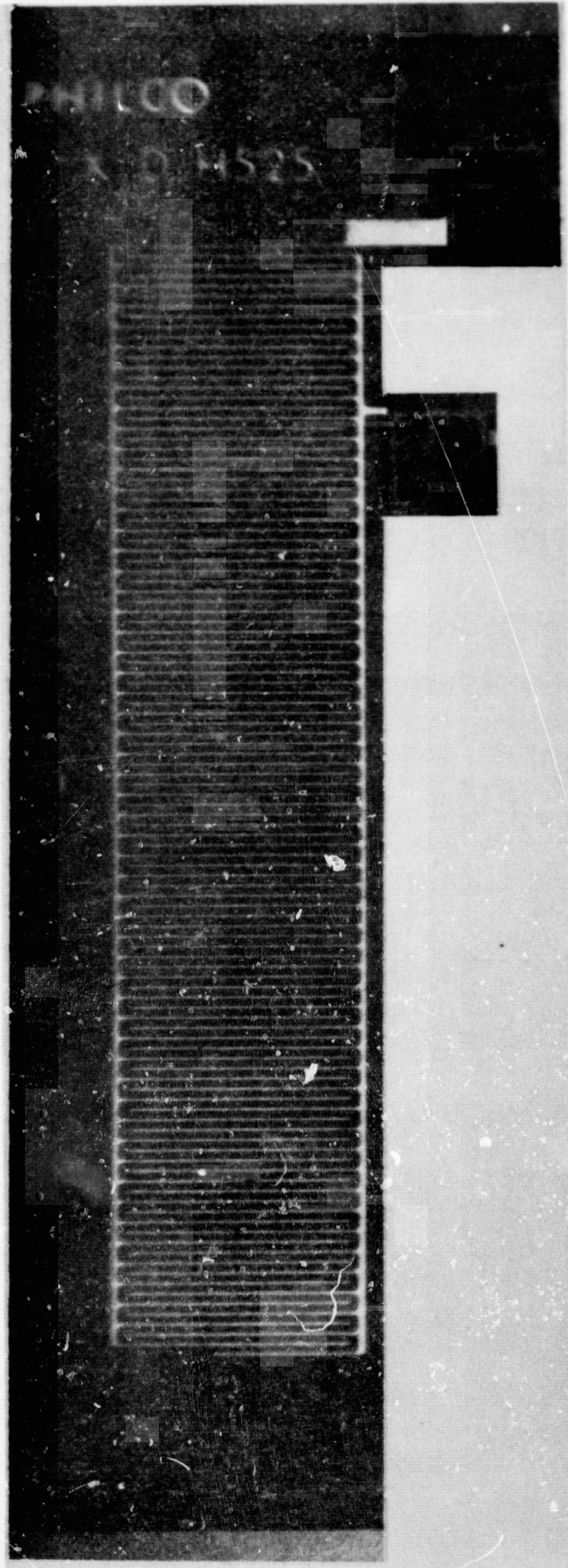


Figure 7. Test structure for the direct measurement of surface conductivity.

oxide to the silicon and back up through the oxide, or through other extraneous paths, such as through the glass in a package or through the probing apparatus.

2. The direct measurement of surface conductivity would be most feasible at the highest levels of relative humidity where the ratio of the current flowing on the surface to that flowing through the oxide is highest. In studies of microcircuit reliability problems, conductivity measurements would be more useful when made at much lower levels of relative humidity.

3. Our surface-ion MOS transistor discussed on page 24 is much better suited for our work because:

   a. Extraneous current paths do not affect the measurements.

   b. The structure is more nearly like that of a circuit, and therefore one can measure directly each of the pertinent effects of surface ions in a micro-circuit -- channel development, instability in diode leakage current or breakdown voltage, and instability in the current gain of a lateral bipolar transistor.

Data from Capacitors Having a High Periphery-To-Area Ratio

The test structure MOS capacitor with the high periphery-to-area ratio was designed to study the migration of charge between the region under the metal and regions beyond the edge of the metal. The data in Tables VI and VII demonstrate several types of results that we have obtained from test structures No. 1 and 2 in Figure 5. In Table VI, we show that if there is a high density of mobile charge in the region outside of the metal electrode, it can move to regions under the metal. On the other hand, the data in Table VII show that when there is a low level of mobile charge, the capacitors with the high periphery-to-area ratio contain a lower mobile charge density than the large area capacitors. This might be explained by the postulate that the surface oxide acts as a getter for mobile charge

Effects of Various Processes in a Complex Bipolar Microcircuit Processing Sequence

To obtain a good understanding of the effect of various processes in a complex bipolar microcircuit processing sequence, we made MOS capacitors on oxides that were taken out of a microcircuit fabrication processing sequence at different points. The silicon wafers were ⟨111⟩ oriented, 5 ohm-cm n-type.

TABLE VI

Comparison of Charge Densities in Capacitors Having Different P/A, Samples with High Mobile Charge Density

	10^{11} Charges/cm^2					
	Immobile		Mobile (300°C)		Mobile (25°C)	
	1*	2*	1*	2*	1*	2*
n-type substrate						
Not vapor plated	2.4	2.4	1.0	2.2	0.1	0.1
Vapor plated	2.4	1.5	1.2	3.5	0.2	1.5
p-type substrate						
Not vapor plated	2.7	2.8	1.6	5.0	0.3	2.2
Vapor plated	1.5	3.0	2.2	2.5	0.5	0.8

*Test structures 1 and 2 in Figure 5.

TABLE VII

Comparison of Charge Densities in Capacitors Having Different P/A, Samples with Low Mobile Charge Density

	10^{11} Charges/cm^2					
	Immobile		Mobile (300°C)		Mobile (25°C)	
	1*	2*	1*	2*	1*	2*
n-type substrate						
Not vapor plated	4.2	4.1	0.2	0.1	0.5	0.0
Vapor plated	4.5	4.0	0.3	0.0	0.0	0.0
p-type substrate						
Not vapor plated	4.1	3.8	0.9	0.0	0.2	0.0
Vapor plated	3.8	3.8	0.9	0.1	0.1	0.0

*Test structures 1 and 2 in Figure 5.

The charge densities that were measured on these samples are summarized in Table VIII. The metal on these samples was evaporated from a resistance heated tungsten coil. Samples with an A in their numbers were alloyed; those without an A were not alloyed. Diffusion, photolithographic and etching steps were performed on the samples at the appropriate parts of the process. The ultraviolet exposure was always included in the photolithographic process without the use of a mask. All of the measurements were on samples mounted on TO-5 headers. The charge densities were measured in the as-mounted state, after drifting at room temperature, and after drifting at 300°C.

Table VIII shows that in the early stages of the process the immobile charge density is widely variable and the mobile charge density is high. This is not unexpected in a bipolar process where the precautions against contamination are less stringent than those taken in an MOS process. The emitter diffusion (phosphorus) greatly increases the uniformity of the immobile charge density and reduces the level of the mobile charge density. The ability of phosphorus to immobilize mobile charge is well known. Subsequent processes in which some of the phosphorus is removed do not degrade the stability of the oxide. However, the addition of a layer of vapor plated SiO_2 caused a large increase in the mobile charge density because

TABLE VIII

Effects of Various Processes in a Complex Microcircuit Processing Sequence

Oxide Preparation (Process)	Sample Group	Sample Number	10^{11} Charges/cm^2 Initial	Room Temperature -100V	Room Temperature +100V	Room Temperature Δ	300°C -100V	300°C +100V	300°C Δ
A	1	765	3.3 - 32.	4.3	27.	+23.	3.5	> 58	> 54
		765A	3.7 - 28.	10.	29.	+19.	5.0	> 56	> 51
		766	4.3 - 12.	4.3	9.	+ 4.7	3.5	50	46
		766A	27. - 34.	8.6	28.	+19.	5.2	> 58	> 53
A.B	2	767	5.7 - 12.5	8.3	9.4	+ 1.1	3.6	> 45	> 41
		767A	16. - 40.	22.	40.	+18.	2.9	> 41	> 38
		768	37. - 42.	17.5	37.	+20.	2.3	> 46	> 43
A.B.C	3	769	4.6 - 5.5	4.4	5.7	+ 1.3	5.1	6.4	+1.3
		769A	4.7 - 5.1	4.2	5.5	+ 1.3	4.7	6.3	+1.6
		770	4.6 - 5.1	4.3	5.6	+ 1.3	7.1	6.6	-0.5
		770A	4.7 - 5.1	4.4	5.6	+ 1.3	4.9	6.6	+1.7
A,B,C,D	4	771	3.9 - 4.9	4.4	5.3	+ 0.9	5.3	6.2	+0.9
		771A	4.1 - 4.7	4.0	4.9	+ 0.9	4.3	6.1	+1.8
		772	4.1 - 4.4	3.8	4.7	+ 0.9	4.3	5.5	+1.2
		772A	3.7 - 4.3	3.4	4.4	+ 1.0	3.6	5.5	+1.9
		820	1.6 - 2.1	1.4	3.0	+ 1.6	1.2	3.4	+2.2
		819A	1.6 - 2.1	1.4	2.7	+ 1.3	0.6	3.5	+2.9
A,B,C,D,E	5	826	3.8 - 4.1	2.0	2.8	+ 0.8	0.5	21.5	+20
		825A	3.5 - 4.9	4.4	4.2	- 0.2	1.4	29.	+28

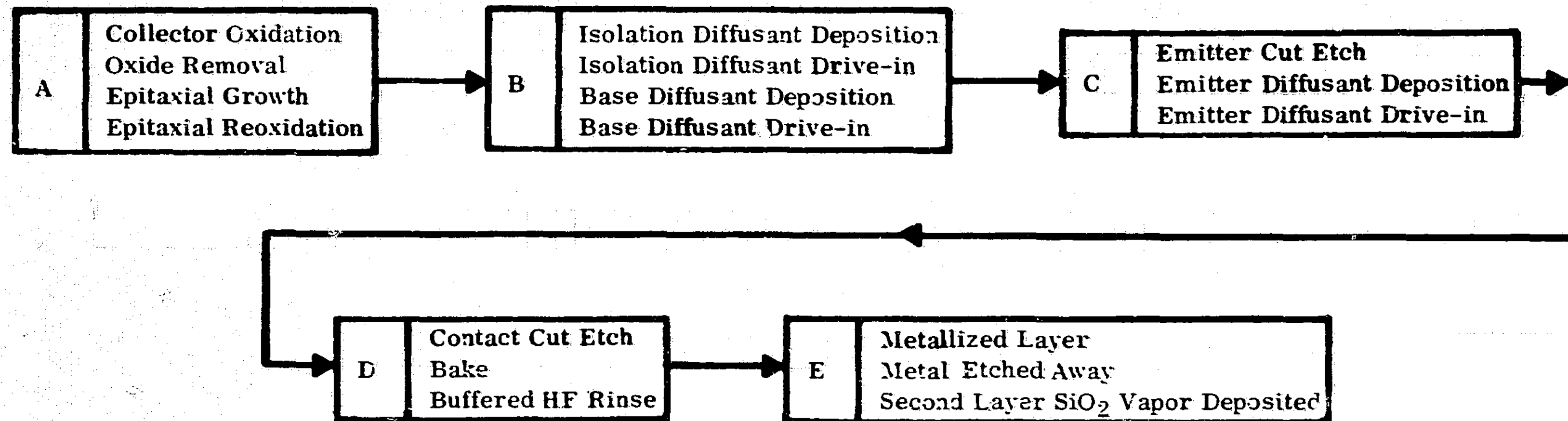
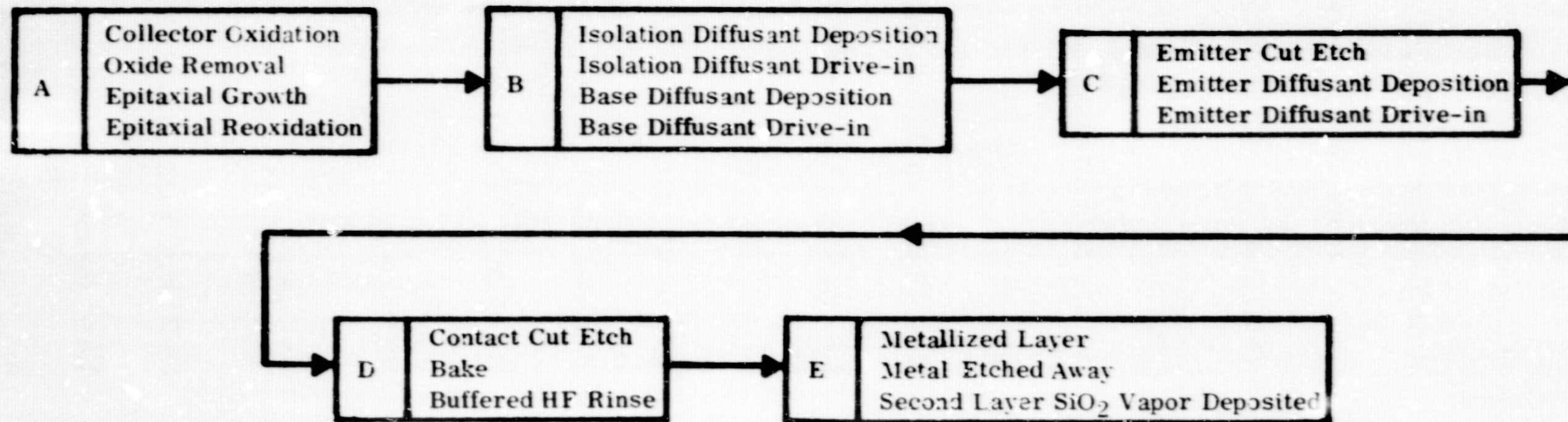


TABLE VIII

Effects of Various Processes in a Complex Microcircuit Processing Sequence

Oxide Preparation (Process)	Sample Group	Sample Number	10^{11} Charges/cm^2 Initial	Room Temperature -100V	Room Temperature -100V	Room Temperature Δ	300°C -100V	300°C +100V	300°C Δ
A	1	765	3.8 - 32.	4.3	27.	+23.	3.5	> 58	> 54
		765A	8.7 - 28.	10.	29.	+19.	5.0	> 56	> 51
		766	4.8 - 12.	4.3	9.	+ 4.7	3.5	50	46
		766A	27. - 34.	8.6	28.	+19.	5.2	> 58	> 53
A, B	2	767	5.7 - 12.5	8.3	9.4	+ 1.1	3.6	> 45	> 41
		767A	16. - 40.	22.	40.	+18.	2.9	> 41	> 38
		768	37. - 42.	17.5	37.	+20.	2.3	> 46	> 43
A, B, C	3	769	4.6 - 5.5	4.4	5.7	+ 1.3	5.1	6.4	+1.3
		769A	4.7 - 5.1	4.2	5.5	+ 1.3	4.7	6.3	+1.6
		770	4.6 - 5.1	4.3	5.6	+ 1.3	7.1	6.6	-0.5
		770A	4.7 - 5.1	4.4	5.6	+ 1.3	4.9	6.6	+1.7
A, B, C, D	4	771	3.9 - 4.9	4.4	5.3	+ 0.9	5.3	6.2	+0.9
		771A	4.1 - 4.7	4.0	4.9	+ 0.9	4.3	6.1	+1.8
		772	4.1 - 4.4	3.8	4.7	+ 0.9	4.3	5.5	+1.2
		772A	3.7 - 4.3	3.4	4.4	+ 1.0	3.6	5.5	+1.9
		820	1.6 - 2.1	1.4	3.0	+ 1.6	1.2	3.4	+2.2
		819A	1.6 - 2.1	1.4	2.7	+ 1.3	0.6	3.5	+2.9
A, B, C, D, E	5	826	3.8 - 4.1	2.0	2.8	+ 0.8	0.5	21.5	+20
		825A	3.5 - 4.9	4.4	4.2	- 0.2	1.4	29.	+28



the amount of mobile ion contamination exceeded the ability of the remaining phosphorus to getter the mobile ions. This mobile charge is insidious - it was not observed in initial measurements but only after bias aging experiments.

One might expect that the mobile ions known to be present (Table I) in SiO_2 that was vapor plated at a temperature of $\approx 400^{\circ}C$, would not be immobilized by the phosphorus in the underlying oxide if the mobile charge had not been drifted by an alloying step. Therefore, the high level of mobile charge in the samples having the vapor plated second-layer of SiO_2 is not surprising. On the other hand it might be expected that the mobile charge could be immobilized by the application of heat and voltage to cause the mobile ions to migrate to the phosphorus. For this reason Sample Group No. 5 was subjected to the following sequence of temperature and voltage treatments:

+100 V, 300°C, 12 min.
-100 V, 300°C, 12 min.
+100 V, 300°C, 30 min.
-100 V, 300°C, 12 min.
-100 V, 300°C, 45 min.

C-V curves were recorded after each of these drift periods. The data taken show that even after these attempts to migrate the mobile charge to the phosphorus there was very little diminution of the mobile charge density. It was also observed that for these oxides the drift of the mobile charge was not

nearly saturated by the application of 100 V of either polarity at 300°C for 12 minutes.

Test of Proposed Solutions to Surface Ion Problems

One can calculate a thickness of dielectric layer that will prevent a given change, due to the migration of surface ions under the influence of a given applied voltage on an electrode, in the surface potential of the silicon. For example, 5 ohm-cm n-type silicon will invert when the area charge density in the silicon is 8.5×10^{11} cm^{-2}. Typically, an oxide contains an immobile charge density of 2.9×10^{11} positive charges/cm^2. Therefore, a surface charge density of 2.9×10^{11} negative charges/cm^2 will invert the silicon. Therefore, the voltage necessary to invert the silicon can be calculated as a function of the thickness of the oxide from the equation:

$$\frac{C}{A} = \frac{\epsilon}{t} = \frac{qN_s}{V} ,$$

or

$$V = \frac{qN_s t}{\epsilon} = 0.45\ N_s t, \qquad \text{(Equation 1)}$$

where N_s is the surface charge density (in units of 10^{11} cm^{-2}), t is the thickness of the oxide (in units of 10^3 Å), V is the voltage across the oxide (volts).

To test the effectiveness of a thick oxide for preventing surface ion problems we fabricated two types of test structures by the established processes used to produce complex bipolar microcircuits for a standard product line. Only the metal pattern of these test structures was different from that of the production microcircuits. The overall chip is shown in Figure 8 and Figure 9 is a close-up view of a test structure used in this experiment. In Figure 9, contact D contacts the p-type diffused base of the bipolar transistor, which becomes the source of the p-channel MOS transistor. Contact C contacts the p-type diffused resistor, which serves as the drain of the MOS transistor. Contact B contacts the collector of the bipolar transistor and the substrate of the MOS transistor. Contact A forms a gate that bridges the region between the source and drain. The narrow width of the gate relative to that of the source and drain makes this MOS transistor sensitive to surface ion effects.

The first layer of oxide over the region that forms the channel of the MOS transistor is 13,000 Å thick. We deposited an additional (> one micron) layer of phosphosilicate over this structure to make an empirical determination of the effectiveness of thick oxides for the prevention of surface-ion-induced instability. According to Equation 1, 13,000 Å thick oxides permit inversion

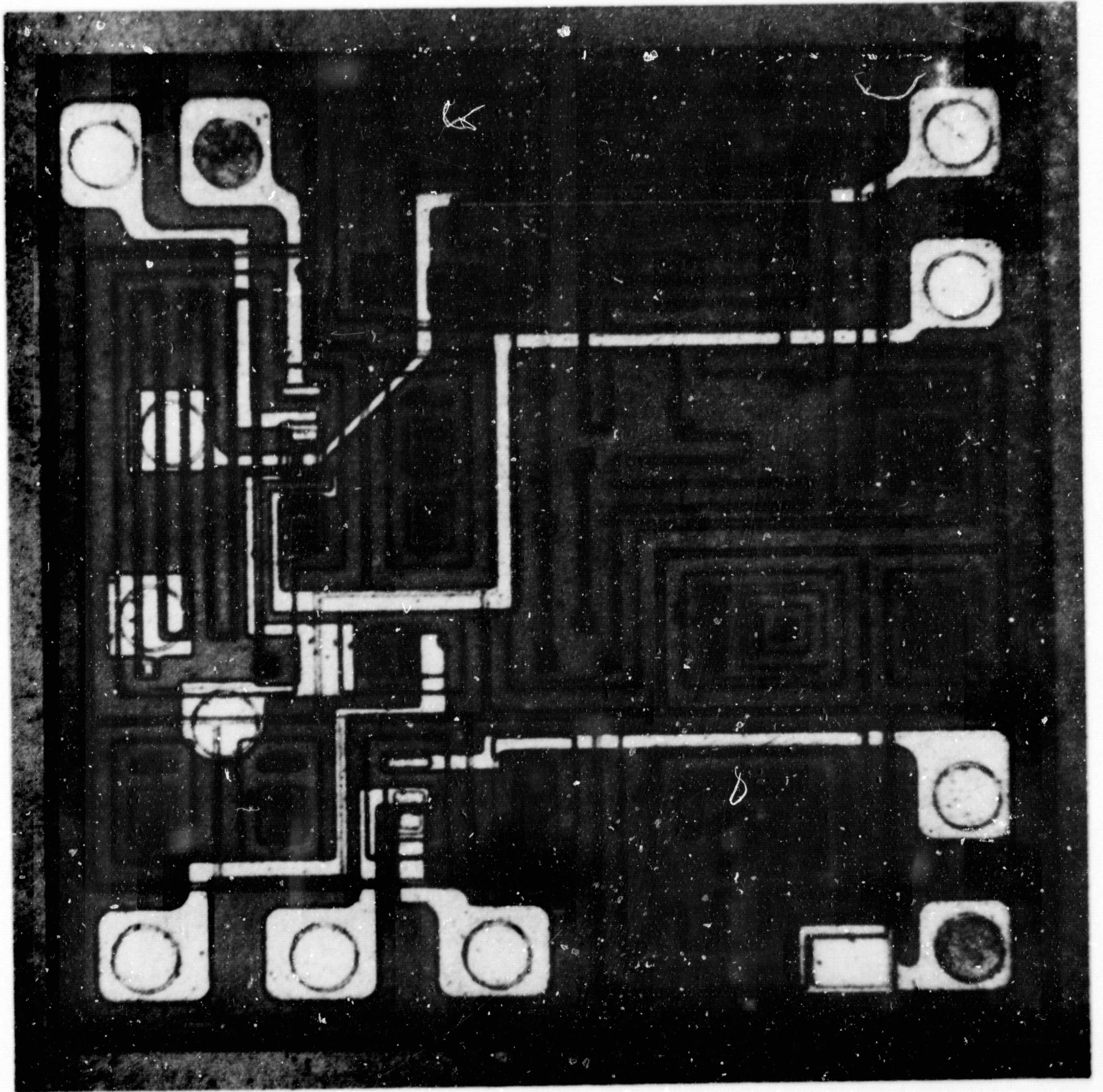


Figure 8. Structure used for studying surface ions.

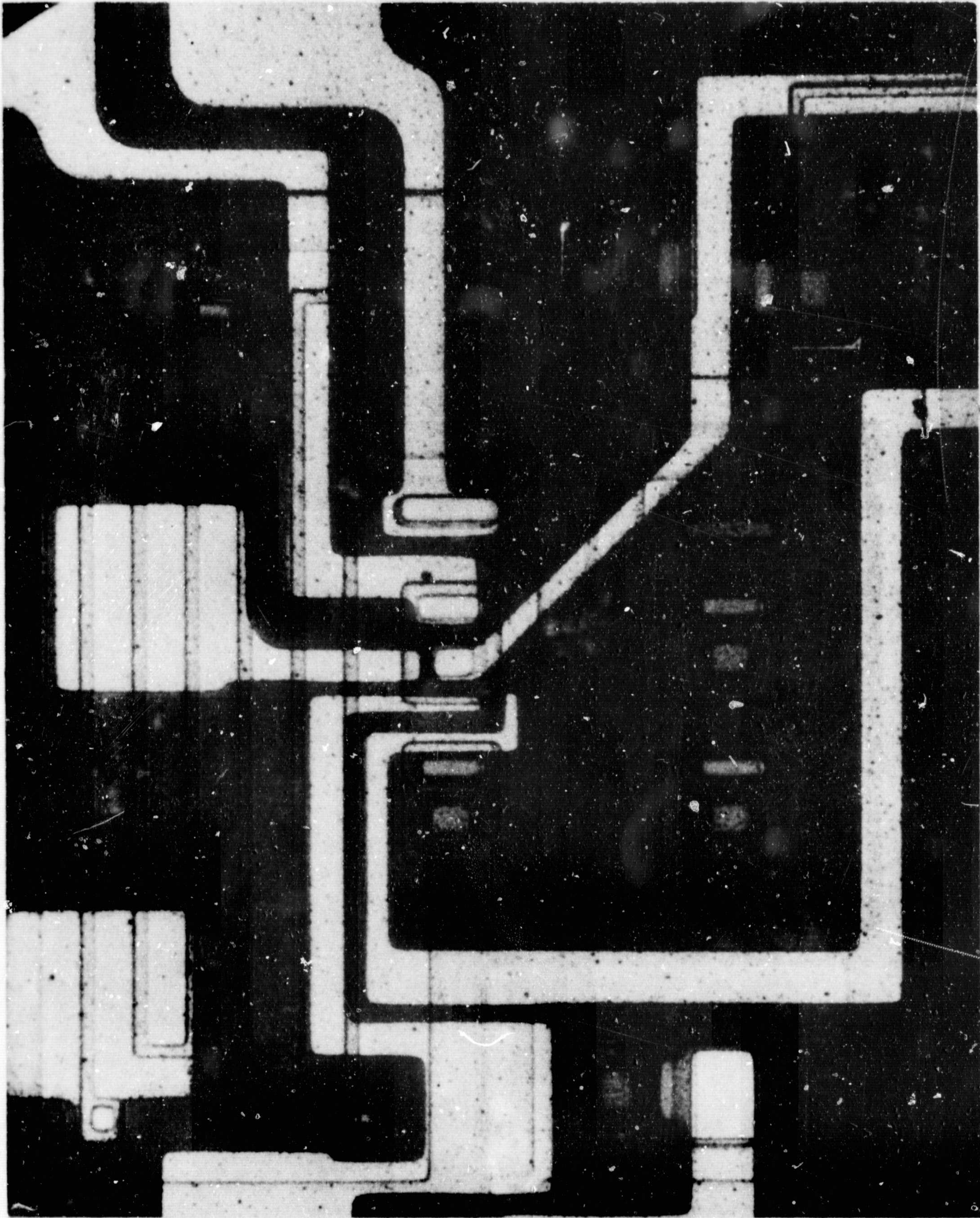


Figure 9. Close-up view of structure used for studying surface ions.

when the applied voltage is 17 volts, while the 23,000 Å thick oxides should not permit inversion until at least 30 volts is applied.

On some of these test structures, an additional layer of metal was deposited over the sensitive areas of the chip, as shown in Figure 10. The dark regions in the second-layer metal are regions where there is underlying first-layer metal, and should not be mistaken to be openings in the second-layer metal.

Having the two types of experimental test devices described above, and a number of control devices that had only a single layer of oxide and a single layer of metal, we sealed a number of the three types of devices in hermetic TO-5 packages in which the ambient was dry nitrogen, with a moisture content of less than 15 ppm. The devices were then subjected to the type of treatment that should induce surface ion effects.

To detect surface ion effects, we measured:

1. The drain current at -1.5 V with the gate shorted to the source and substrate.
2. The collector-base diode breakdown voltage at 10 μA.
3. The collector-base diode reverse current at 1.5 V.

The surface ion effects were created by applying a negative voltage to the gate metal relative to the substrate (contact A relative to contact D). All of the drifting of surface ions was done at room temperature.

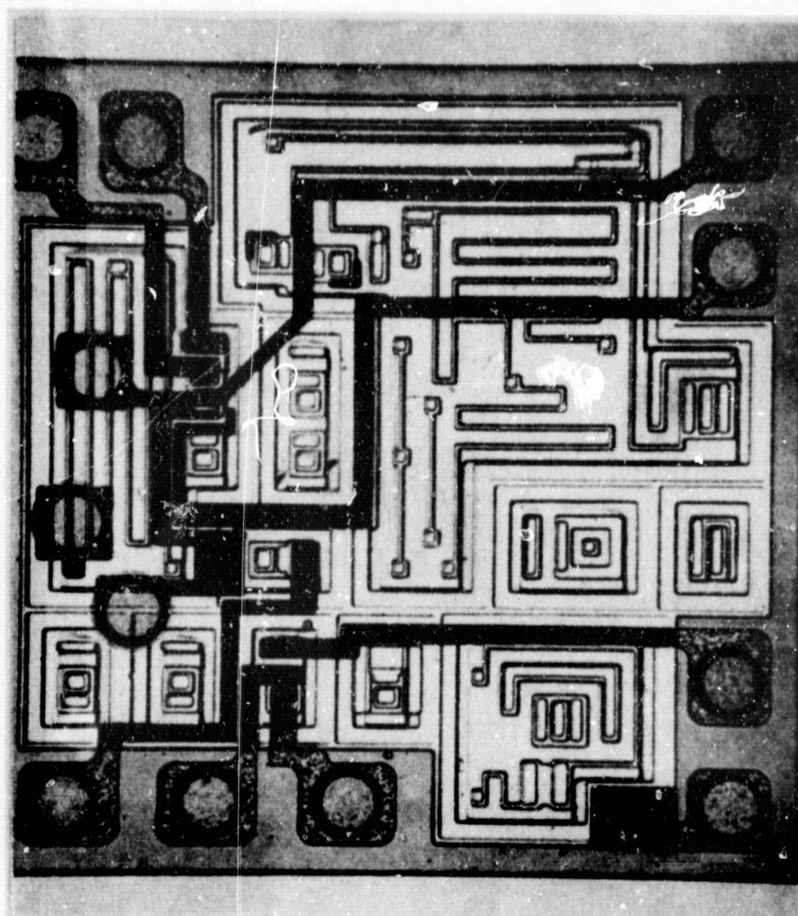


Figure 10. Second-layer metal over structure used for studying surface ions.

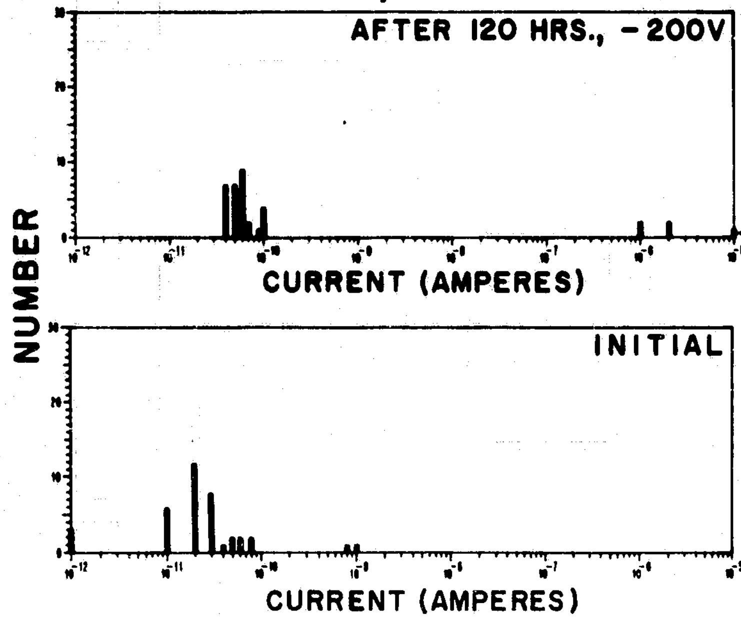
The first finding was that it was more difficult to develop surface ion effects than our calculations lead us to predict. The following bias aging schedules did not change any of the devices significantly:

-50 V for 4 hours,
-50 V for 66 hours,
-100 V for 18 hours,
-150 V for 18 hours.

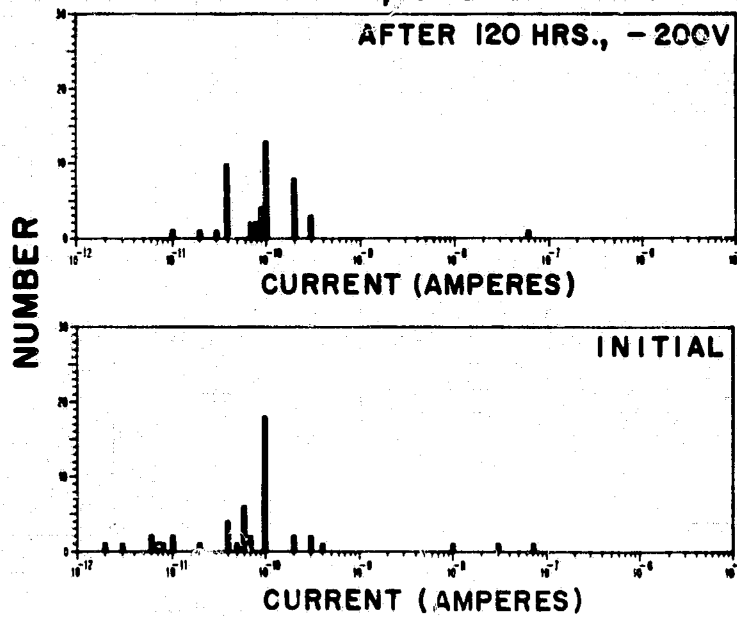
Next, we punctured each of the packages to increase the mobility and possibly the density of surface ions. We bias-aged the devices at -100 volts for 18 hours, and again found no significant change in the measured parameters. Finally, we subjected the devices to -200 volts for 120 hours, and obtained the data given in Figures 11 through 13.

Figure 11 shows the effect of -200 volts for 120 hours on the gate relative to the substrate on the surface-ion-induced channel current at 1.5 volts between the source and drain. The control devices channelled strongly, both in terms of the change in current level and in terms of the percentage of devices channelled. The devices with a second level of oxide, but no second level of metal, were very stable. The devices with both a second layer of oxide and of metal were somewhat less stable than were the devices in the second group. Further examination revealed the fact that the devices that channelled in the third group could not support 200 volts on the second layer of metal relative to the substrate, whereas those that did not channel could.

TWO LAYERS OF OXIDE, TWO LAYERS OF METAL



TWO LAYERS OF OXIDE, ONE LAYER OF METAL



ONE LAYER OF OXIDE, ONE LAYER OF METAL

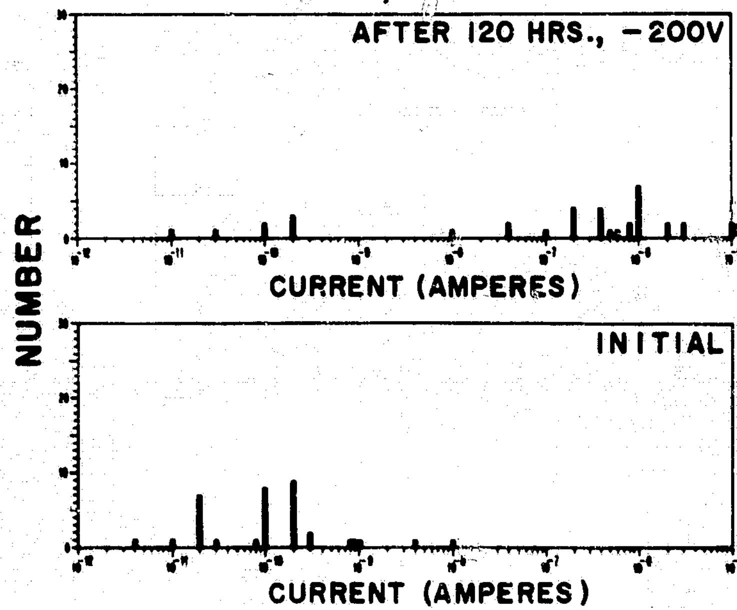
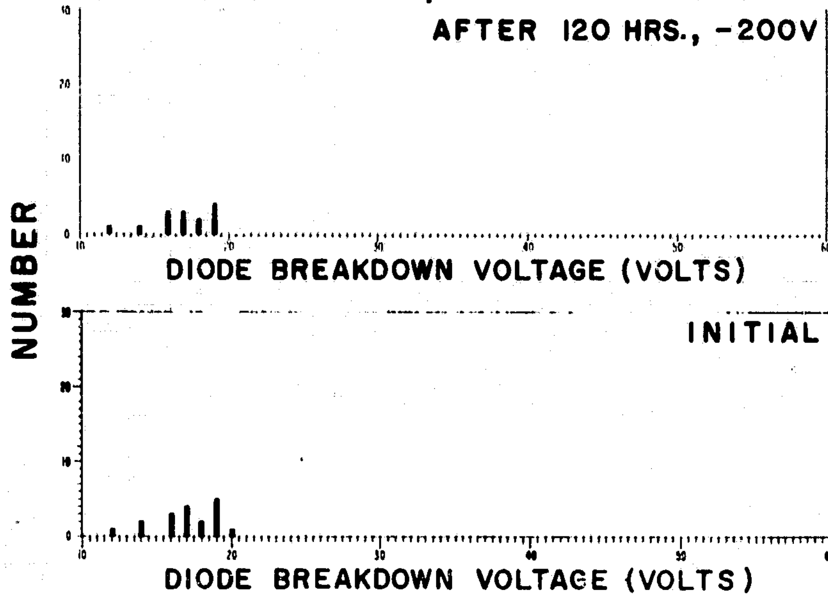
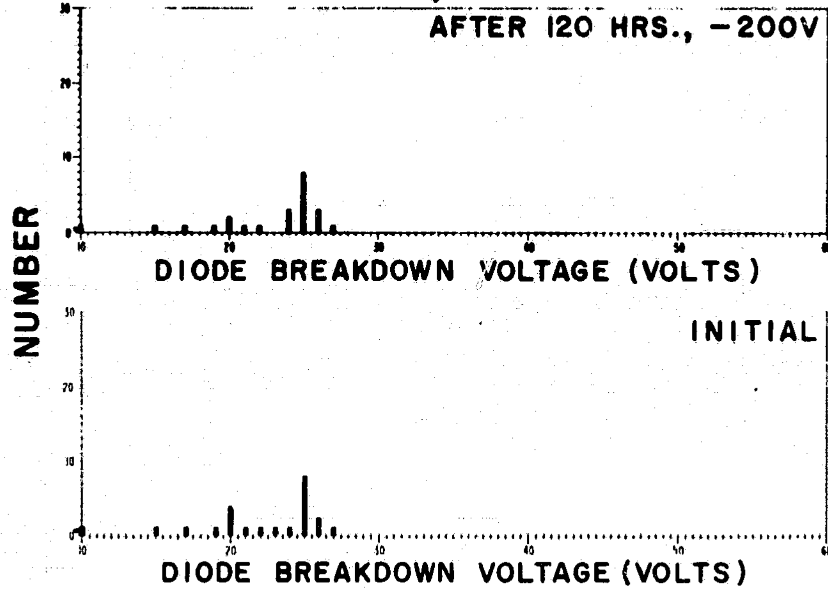


Figure 11. Test of proposed solutions to surface ion problems -- channel current.

TWO LAYERS OF OXIDE, TWO LAYERS OF METAL



TWO LAYERS OF OXIDE, ONE LAYER OF METAL



ONE LAYER OF OXIDE, ONE LAYER OF METAL

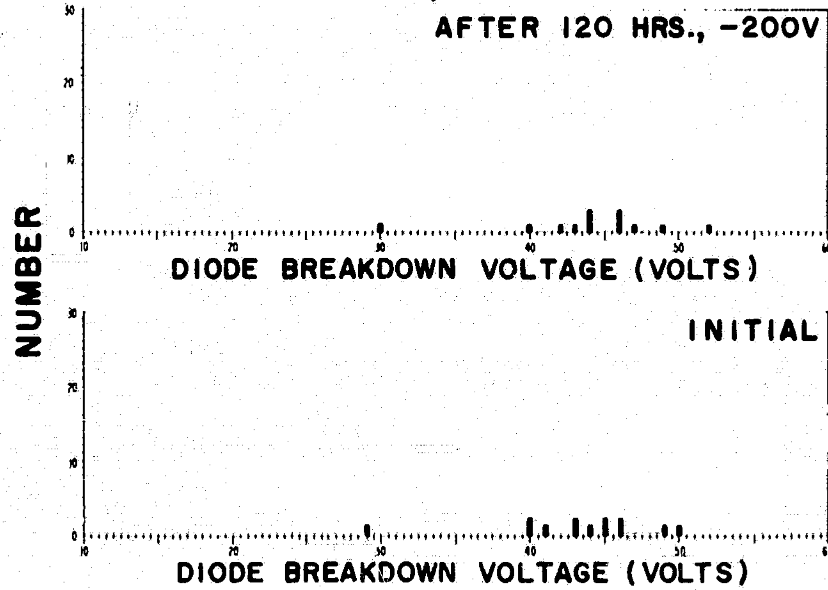
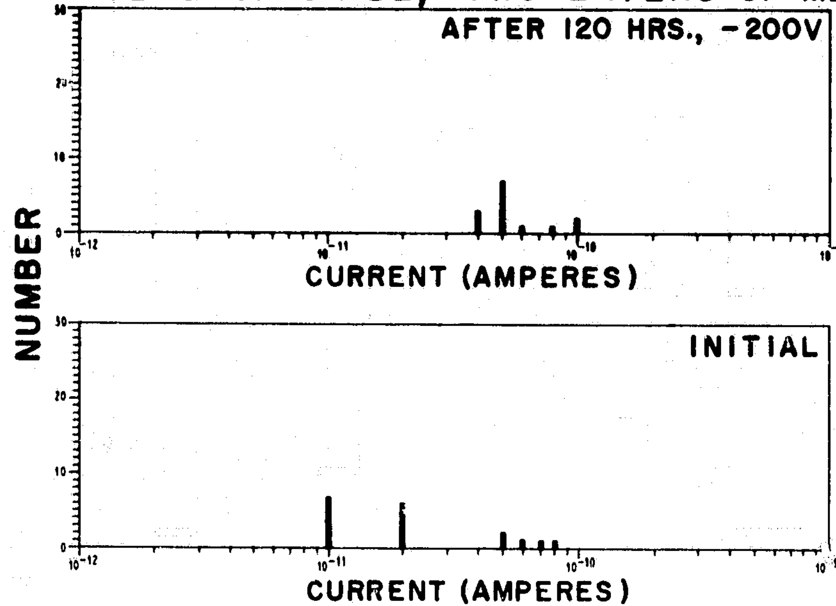
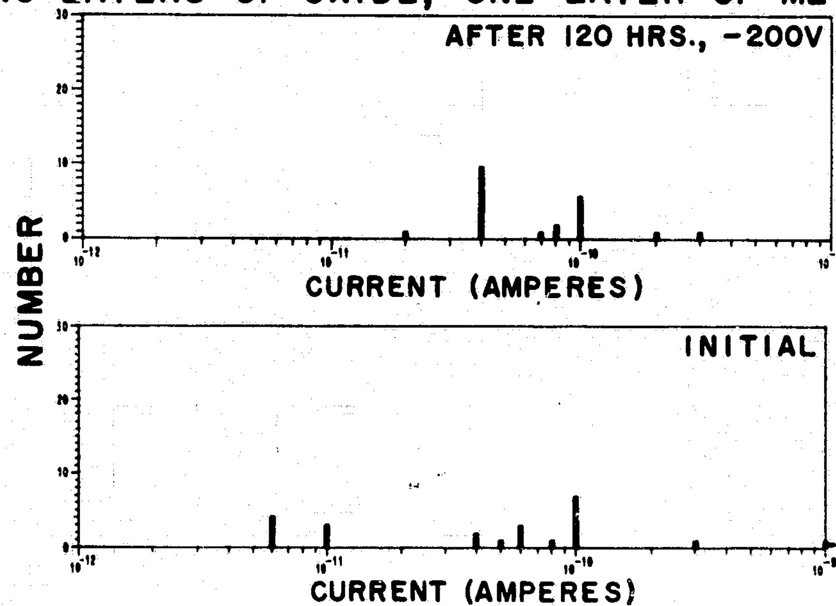


Figure 12. Test of proposed solutions to surface ion problems -- diode breakdown voltage.





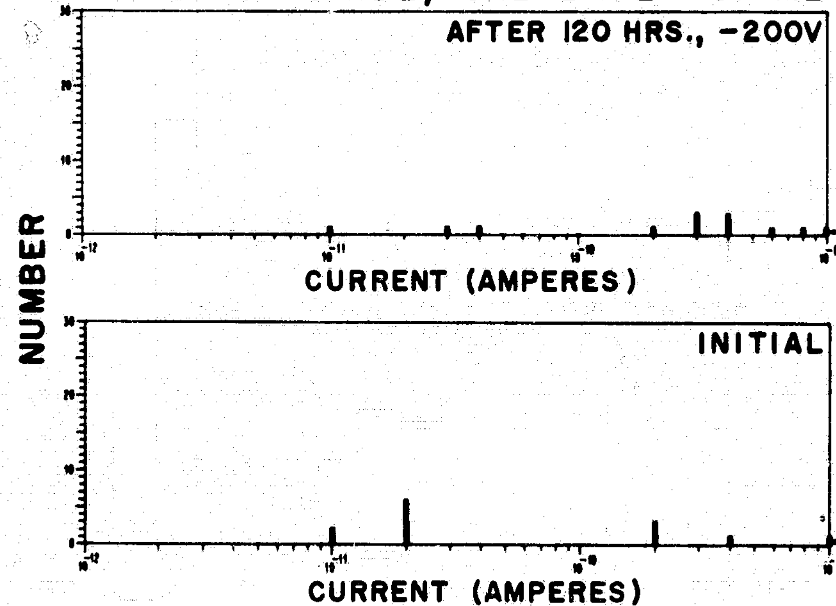


Figure 13. Test of proposed solutions to surface ion problems -- diode leakage current.

We conclude that the extra steps needed to produce a second layer of metal do not provide an advantage over the use of a thick second layer of dielectric. Further, it appears that if the integrity of the oxide under the second-layer metal is imperfect, the presence of the second-layer metal introduces an added failure mechanism.

Figure 12 shows that the diode breakdown voltage was not degraded on any of these groups of devices by the bias-aging. However, the deposition of the phosphosilicate very significantly decreased the breakdown voltage of the collector-base diode. This would indicate that the effective positive charge density in the oxide over the n-type collector region was increased by the deposition of the second layer of oxide. It is not known whether this occurred in the region under the metal, or in the region not under the metal, or in both regions.

Figure 13 shows the data on the diode reverse current. The control group shows the least stability for this parameter, and all of the groups show some instability in this parameter.

Effects of Second-Layer Oxide on MOS Transistors Made by Processes Used for Standard MOS Microcircuits

In Interim Scientific Report No. 1, we presented experimental data that show the effect of vapor plated second-layer

oxides on bipolar transistors made by the standard processes used to build microcircuits in production quantities. In this part of this report, we present similar data on the effects of second-layer phosphosilicate on MOS transistors on wafers made by the processes used to build MOS microcircuitry in production quantities.

Our measurements were taken on two types of discrete MOS transistors that are on each microcircuit chip on the wafer. One of the transistors has under its gate metal an oxide of the type found under the gates in the actual microcircuit. The other transistor has under its gate an oxide of the same type as the thick oxide found in the field of the microcircuit. Both of these devices are at least partially sensitive to the properties of the thick oxide in regions not covered by metal.

Two microcircuit wafers were simultaneously fabricated by the standard MOS process. Each wafer was scribed into halves, and one-half of each wafer was covered with a layer of of vapor plated phosphosilicate, greater than 1 micron in thickness.

Figures 14 through 16 provide a summary of the data taken by testing the transistors with gate oxides on all four half-wafers. The data show that:

1. The spread in the distributions of BV_{DSS}, shown in

WAFER 4

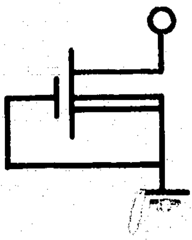
VAPOR PLATED

NOT VAPOR PLATED

NUMBER

BV_{DSS} (VOLTS)

TEST CONFIGURATION



WAFER 1

VAPOR PLATED

NOT VAPOR PLATED

NUMBER

BV_{DSS} (VOLTS)

Figure 14. Effects of second-layer oxide on MOS transistors made by processes used for standard MOS microcircuits -- BV_{DSS}, at 10 μA, measured on wafer.

WAFER 4

VAPOR PLATED

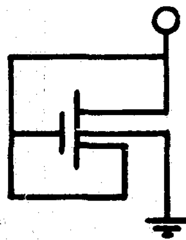
NUMBER

DIODE BREAKDOWN VOLTAGE (VOLTS)

NOT VAPOR PLATED

DIODE BREAKDOWN VOLTAGE (VOLTS)

TEST CONFIGURATION



WAFER I

VAPOR PLATED

NUMBER

DIODE BREAKDOWN VOLTAGE (VOLTS)

NOT VAPOR PLATED

DIODE BREAKDOWN VOLTAGE (VOLTS)

Figure 15. Effects of second-layer oxide on MOS transistors made by processes used for standard MOS microcircuits -- diode breakdown voltage, at 10 μA, measured on wafer.

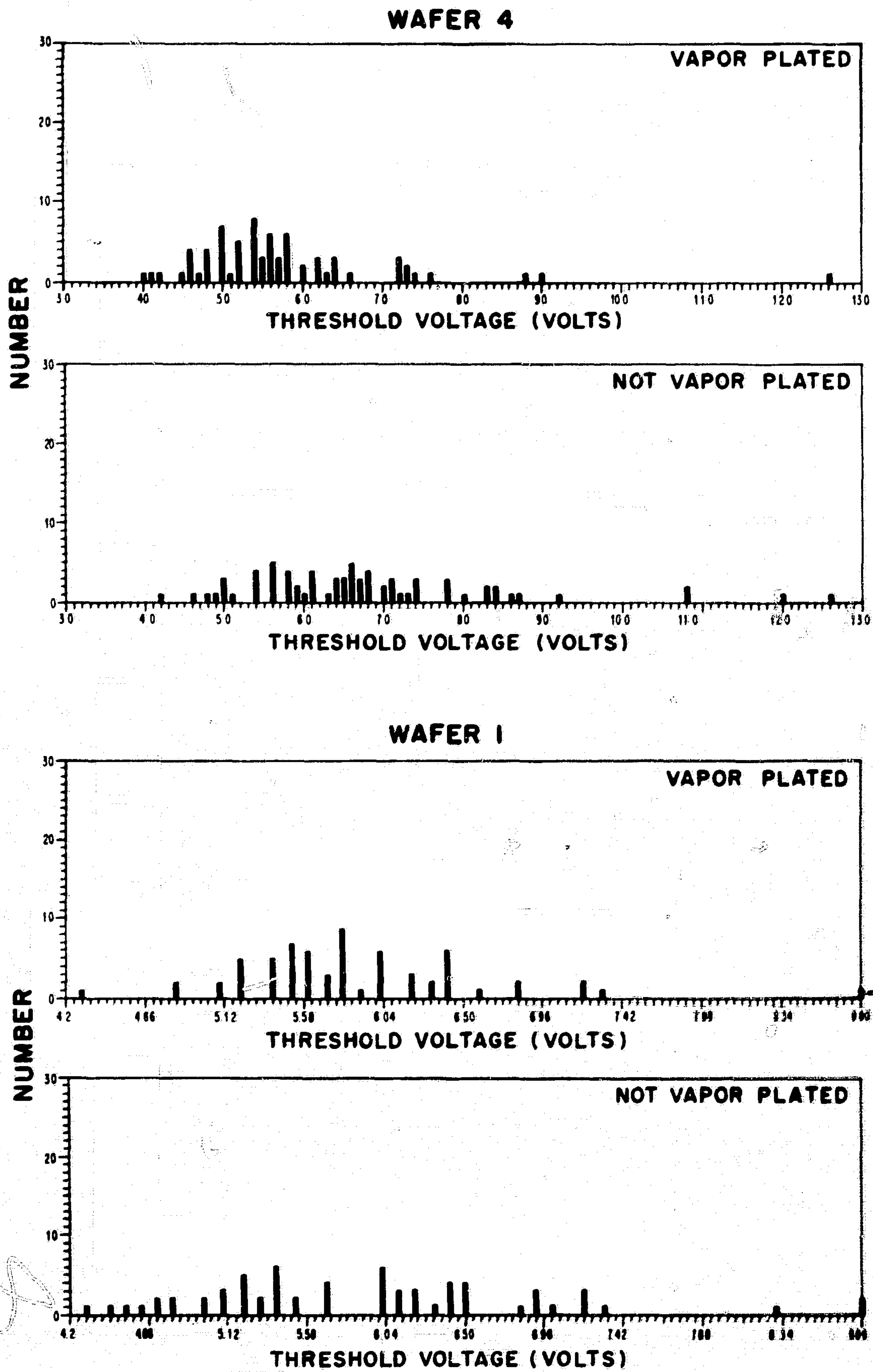


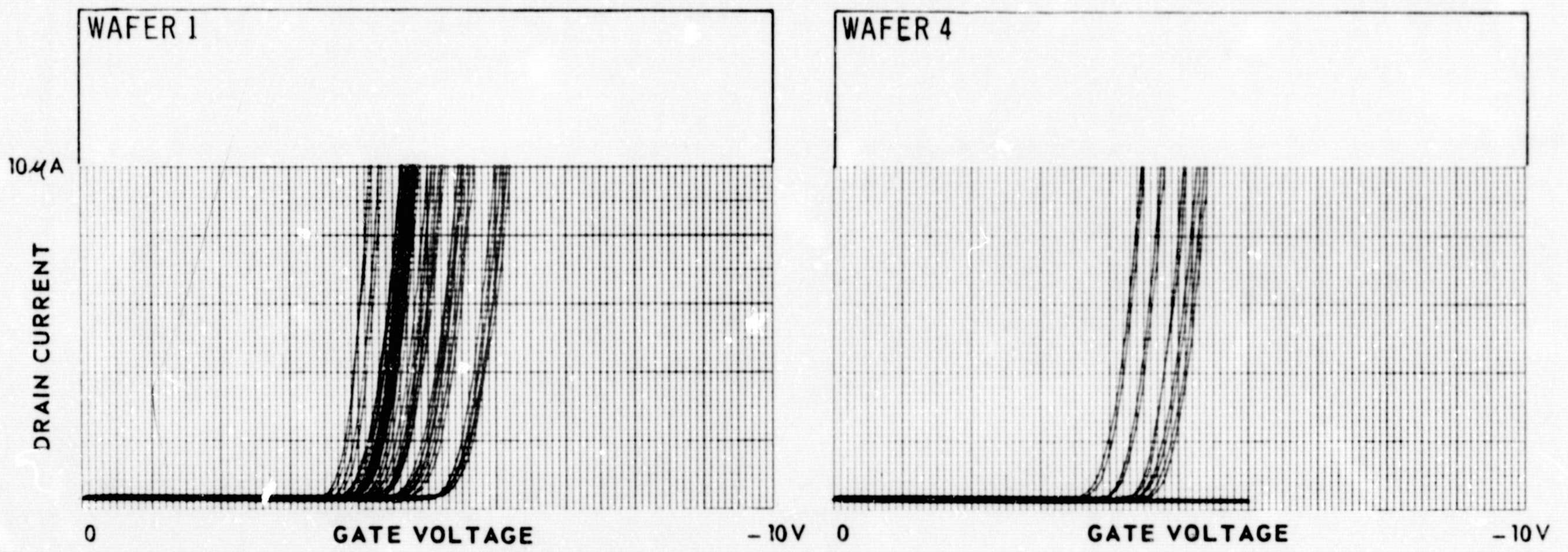
Figure 16. Effects of second-layer oxide on MOS transistors made by processes used for standard MOS microcircuits -- threshold voltage, at 10 μA, measured on wafer.

Figure 14, was increased significantly by the vapor plating step, both in increasing and decreasing directions. (BV_{DSS} was measured as sketched in Figure 14 at currents of 10 μA.)

2. The level of the diode breakdown voltage, shown in Figure 15, (measured as sketched in Figure 15 at 10 μA) was increased by the vapor plating step. The spread in the distribution was not increased.
3. The threshold voltage level at 10 μA, shown in Figure 16, appeared to be slightly decreased by the vapor plating process on one of the wafers. The other wafer showed no change in this parameter.

The same devices were retested after they were scribed, and assembled in TO-5 packages. The results were as follows:

1. Figures 17 and 18 show the dependence of the drain current on the gate voltage at a constant drain voltage of 5 volts. There was no significant change due to the vapor plating in either the transistors with the gate oxide or those with the field oxide.
2. Figures 19 and 20 show the source-to-drain leakage current at 1.5 volts (gate tied to source) on devices that were, and on others that were not, vapor plated. The vapor plating step decreased this leakage current in both types of transistors of both wafers.



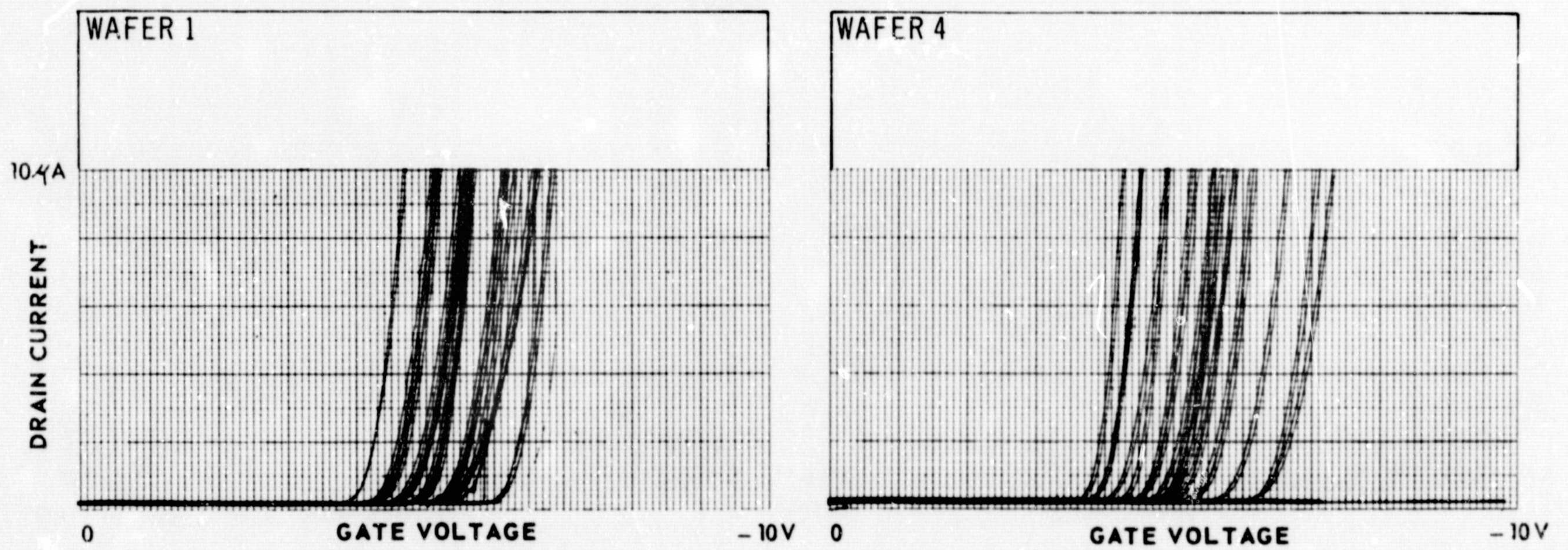
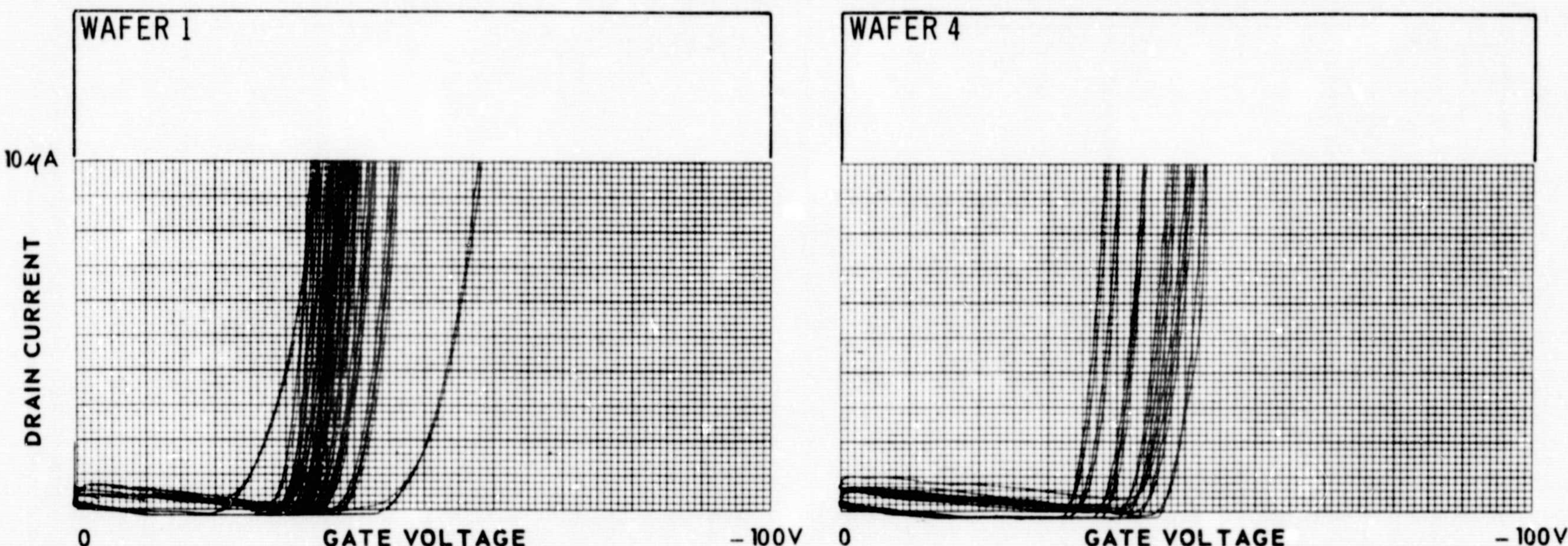


Figure 17. Effects of second-layer oxide on MOS transistors made by processes used for standard MOS microcircuits -- drain current-gate voltage relationships measured on packaged units -- gate oxide.



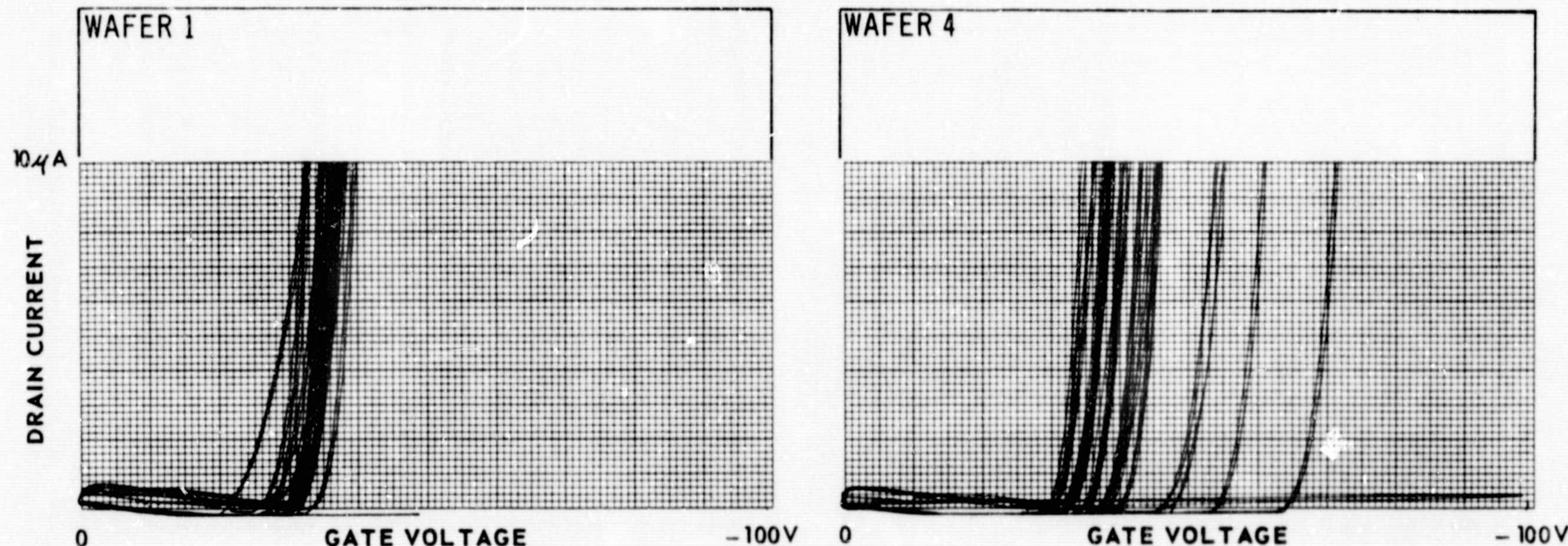


Figure 18. Effects of second-layer oxide on MOS transistors made by processes used for standard MOS microcircuits -- drain current-gate voltage relationships measured on packaged units -- field oxide.

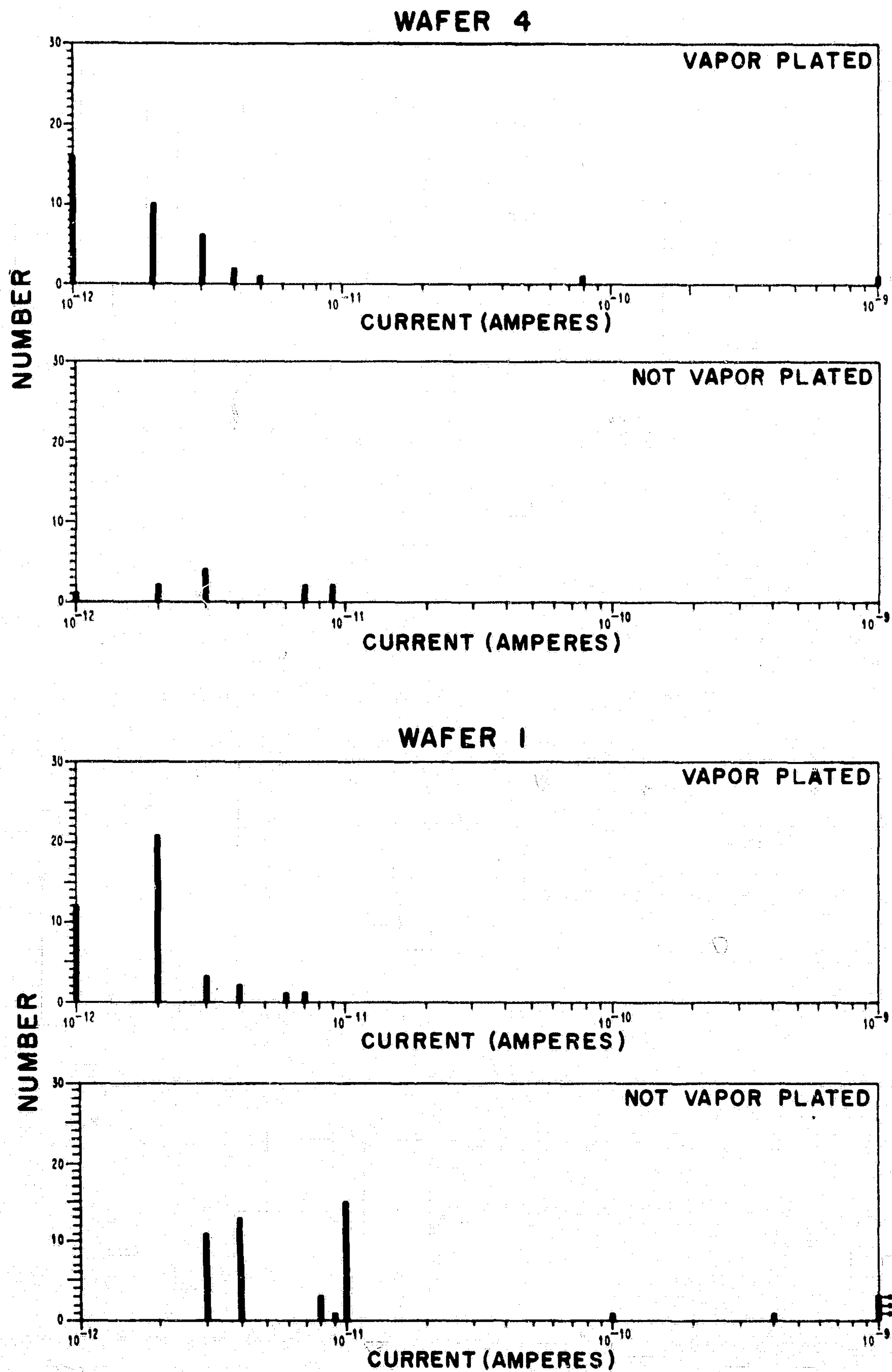


Figure 19. Effects of second-layer oxide on MOS transistors made by processes used for standard MOS microcircuits -- source to drain leakage current measured on packaged units -- gate oxide.

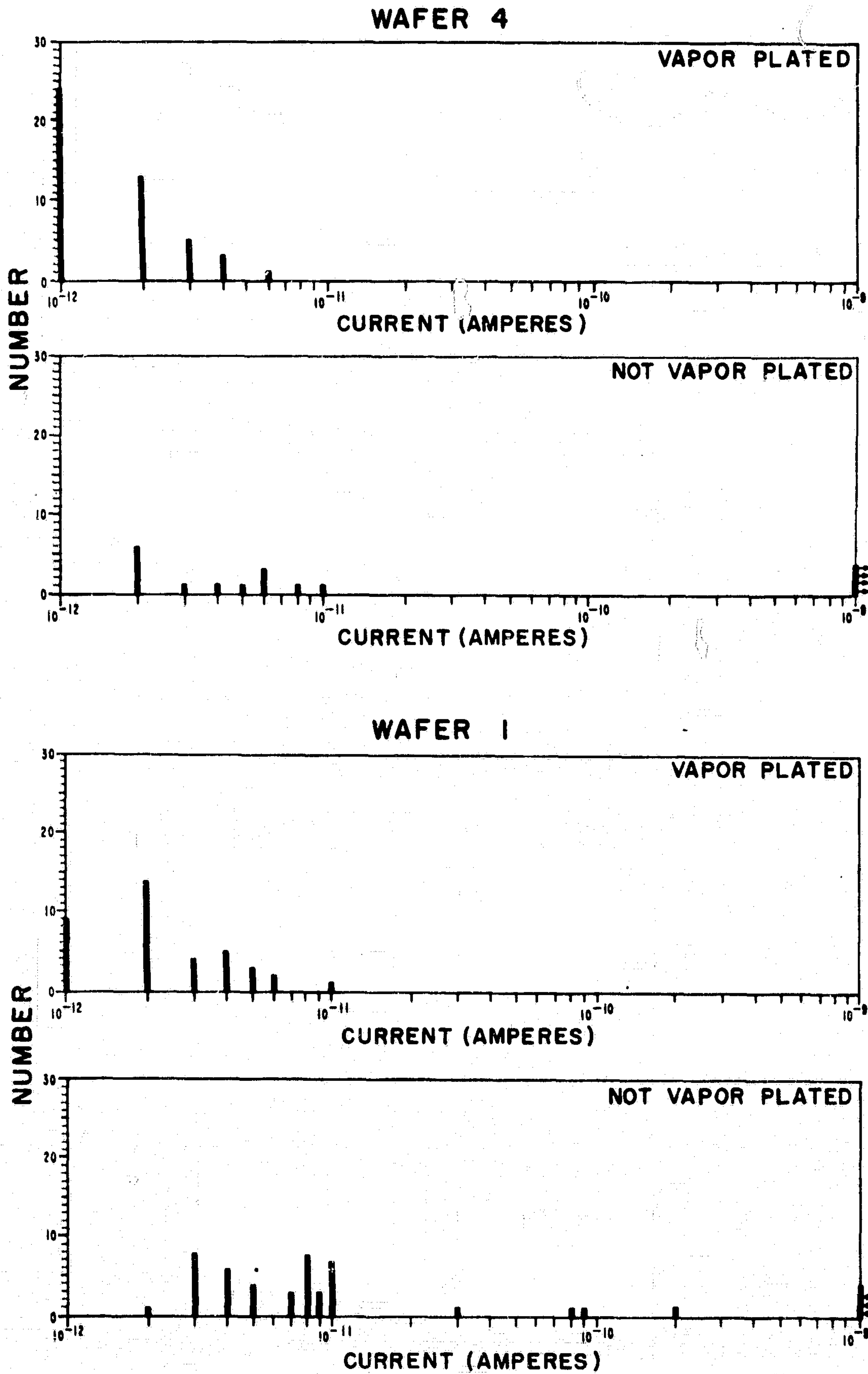


Figure 20. Effects of second-layer oxide on MOS transistors made by processes used for standard MOS microcircuits -- source to drain leakage current measured on packaged units -- field oxide.

3. Figures 21 and 22 show the BV_{DSS} taken after the devices were packaged. They did not show the decrease in BV_{DSS} level due to the vapor plating step that was observed when the devices were tested on the wafers.

4. Figures 23 and 24 show that the diode breakdown voltage is increased as much by the header bonding and wire attaching operations as by the vapor plating process. After packaging, there is no difference between vapor plated and non-vapor plated samples insofar as diode breakdown voltage is concerned.

We conclude:

1. There is no evidence after the devices are packaged that the phosphosilicate glass degrades the MOS transistors.

2. Diode leakage current is decreased and diode breakdown voltage is increased during the vapor plating step. (We infer from this that the Q_{SS} is decreased in the region under the field oxide.) There is some evidence that Q_{SS} also decreases in the gate region.

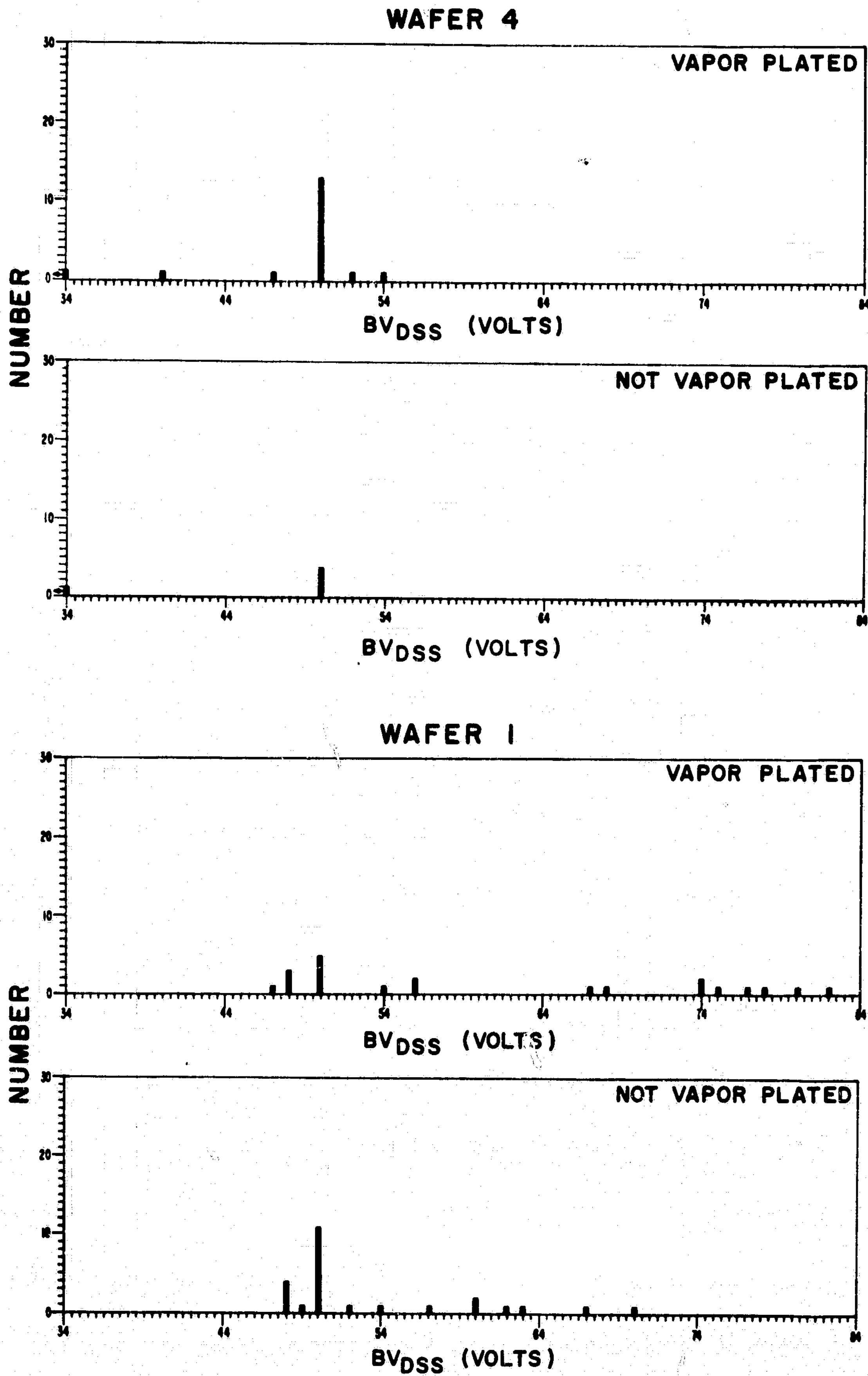


Figure 21. Effects of second-layer oxide on MOS transistors made by processes used for standard MOS microcircuits -- BV_{DSS} measured on packaged units -- gate oxide.

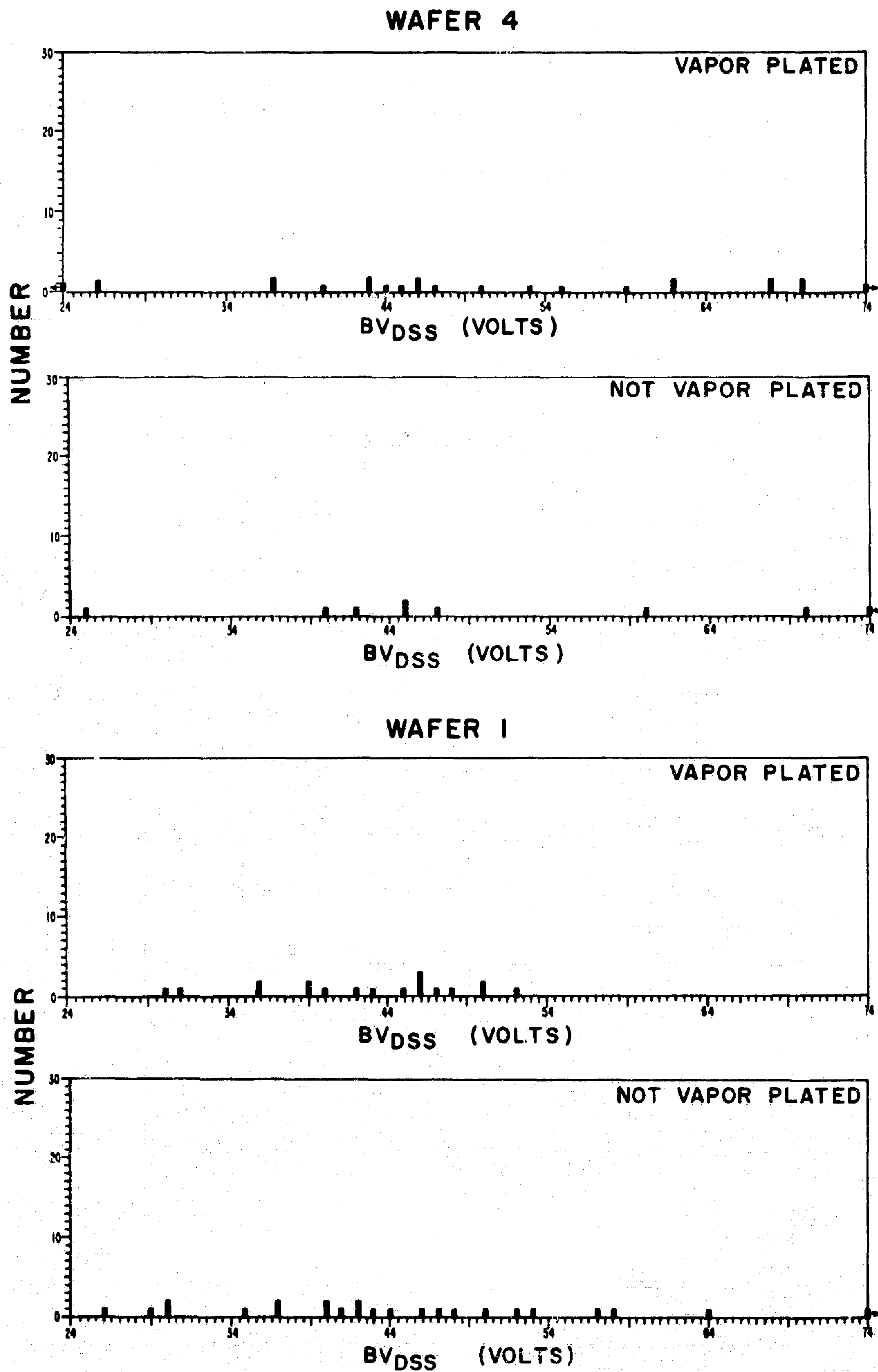


Figure 22. Effects of second-layer oxide on MOS transistors made by processes used for standard MOS microcircuits -- BV_{DSS} measured on packaged units -- field oxide.

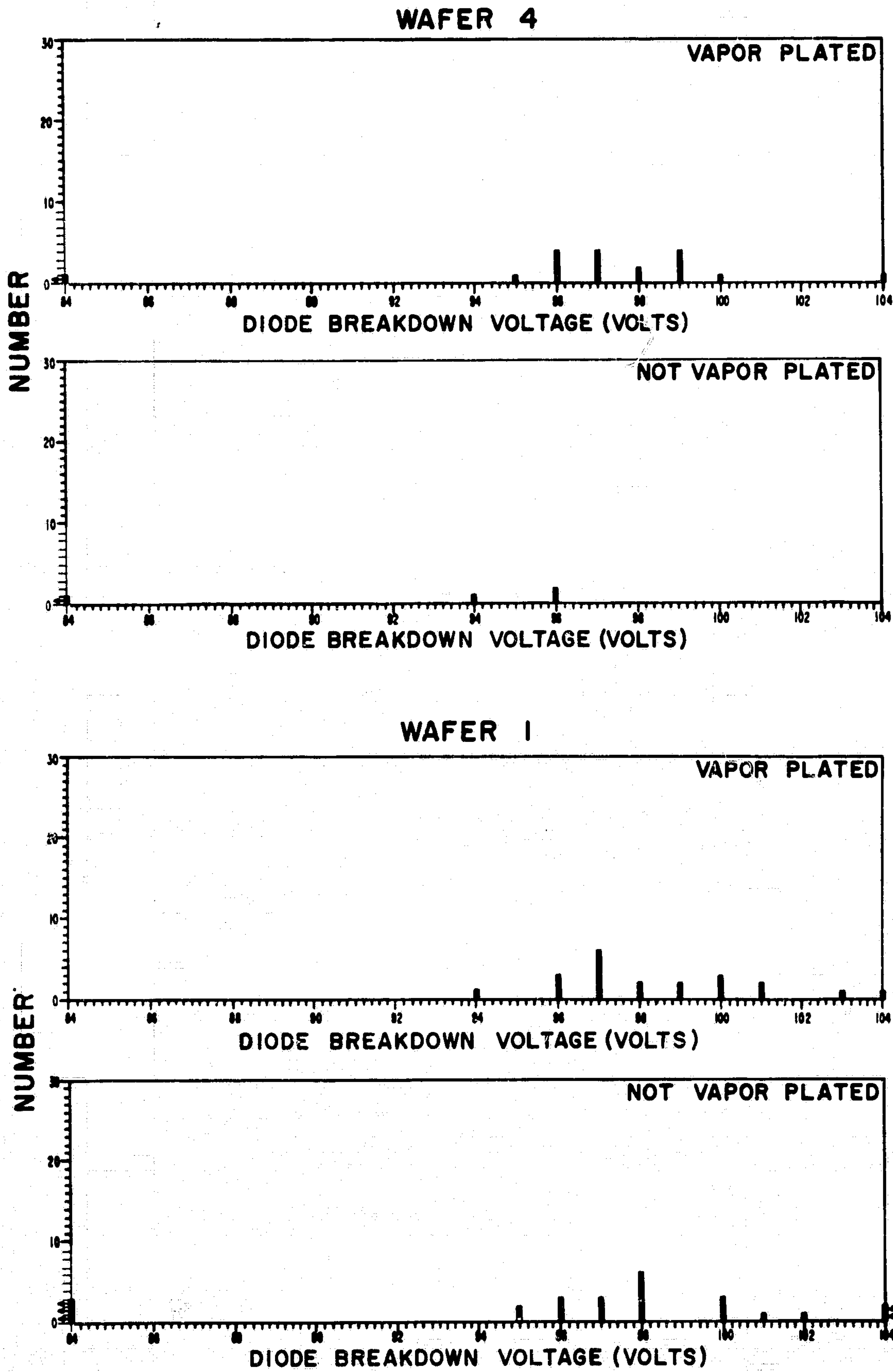


Figure 23. Effects of second-layer oxide on MOS transistors made by processes used for standard MOS microcircuits -- diode breakdown voltage measured on packaged units -- gate oxide.

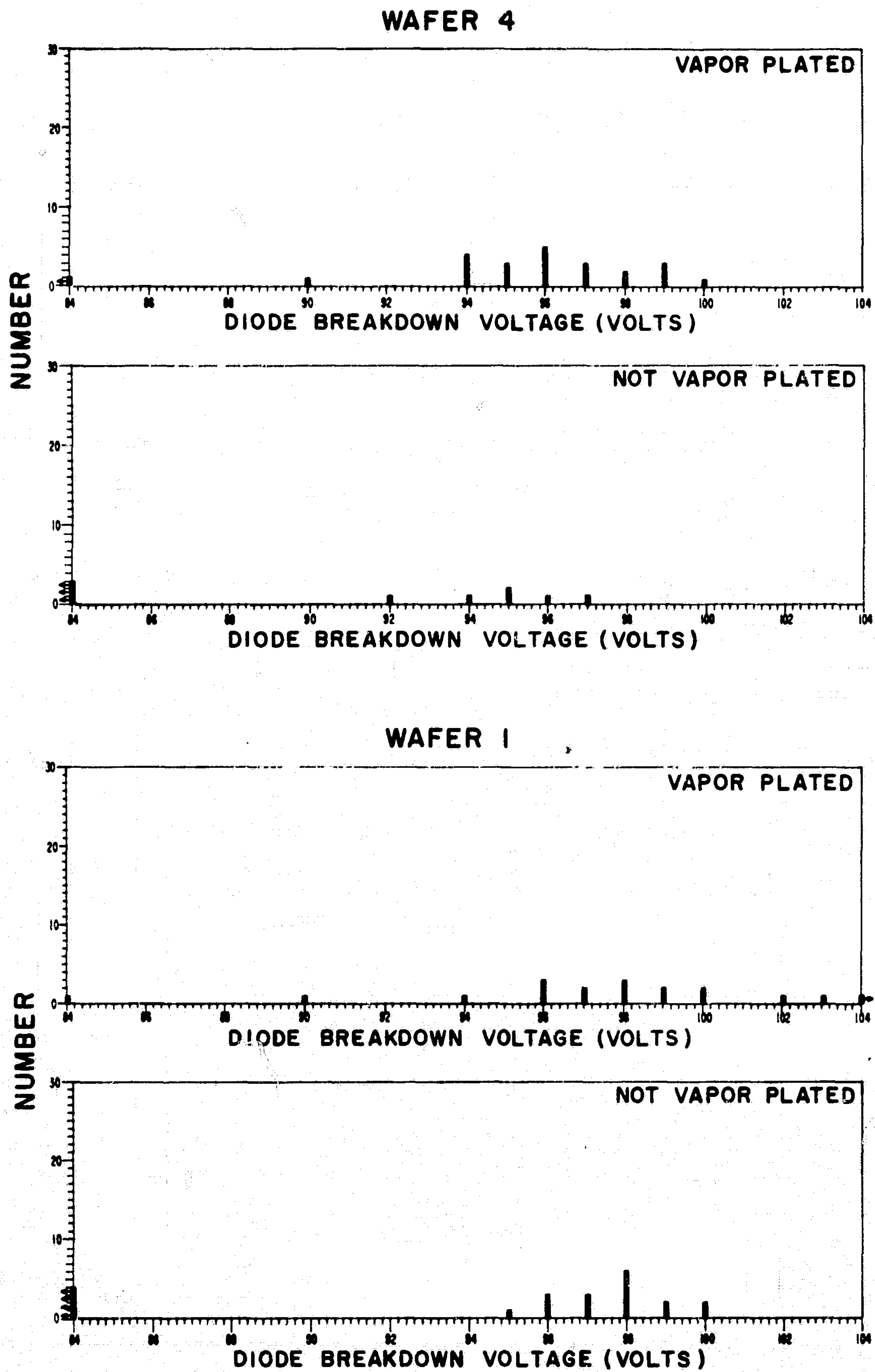


Figure 24. Effects of second-layer oxide on MOS transistors made by processes used for standard MOS microcircuits -- diode breakdown voltage measured on packaged units -- field oxide.

Influence of Mobile Ions on the Transconductance of MOS Transistors

In our list of factors (page 12) influencing circuit reliability, we included the possibility that mobile charge in the oxide can influence the channel length, and therefore the transconductance of MOS transistors. This can be understood as follows: A typical dopant density in a silicon substrate is 10^{15} cm^{-3}. A 1,000 Å thick layer of this silicon contains 10^{10} charges/cm^{2}. Typical Q_{SS} levels (2×10^{11} cm^{-2}) should be quite significant, therefore, in determining the drain depletion layer width out into the channel region. Figure 25 shows instability in the transconductance of MOS transistors. These transistors were selected from a lot known to contain mobile ions. The data show that when the transistor leads are shorted or when there is a positive voltage applied to the gate metal, the transconductance is decreased; and when there is a negative voltage on the gate metal, the transconductance is increased at 300°C in a fraction of an hour.

These transistors have a channel length of 0.24 mils and a width of 2.0 mils. The oxide thickness is 1,500 Å. Figure 26 shows the drain current as a function of the gate voltage for several constant values of the drain voltage for these same samples. Figure 26A shows the initial characteristics

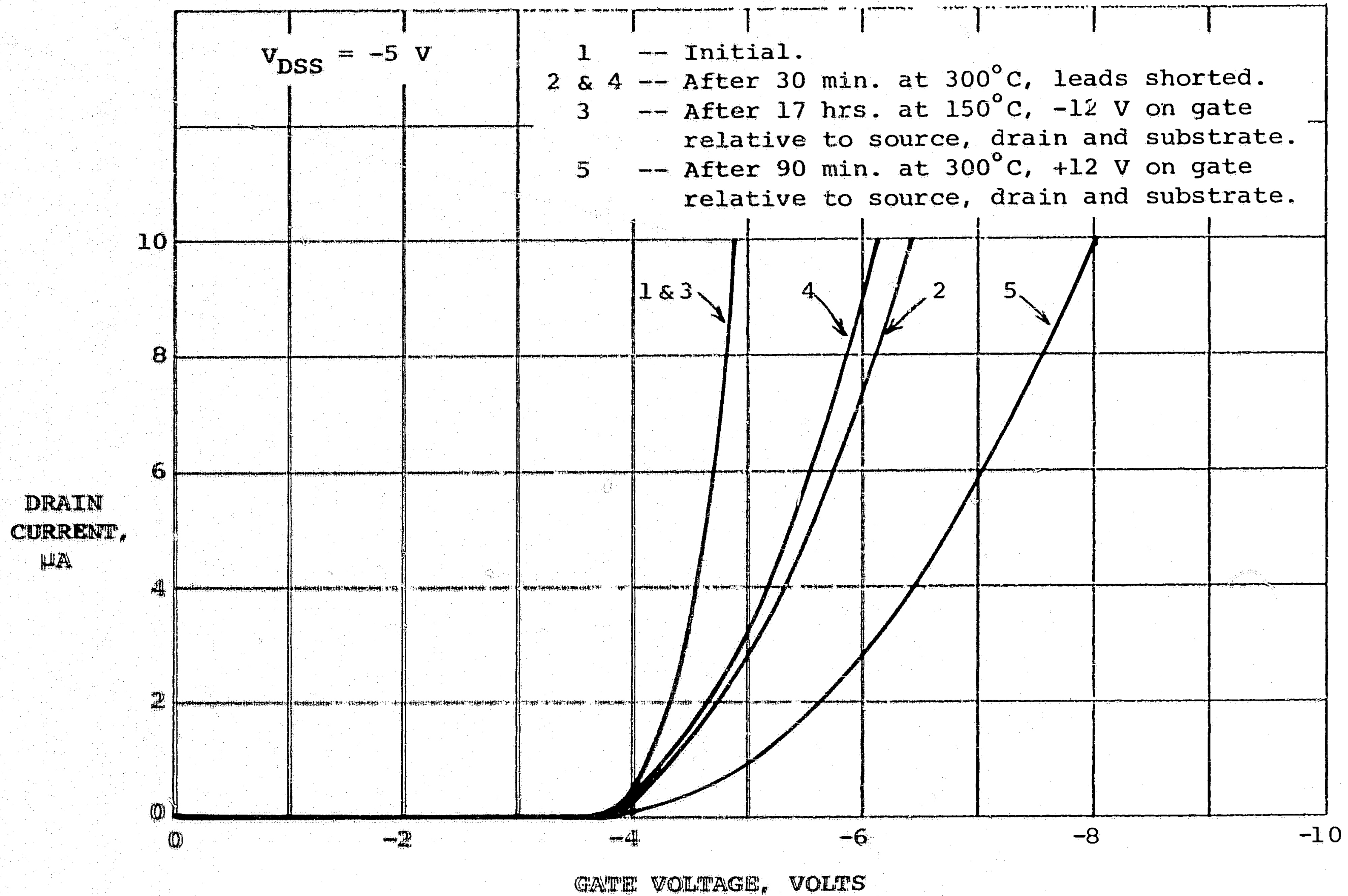


Figure 25. Effect of bake and bias on the transconductance of MOS transistors.

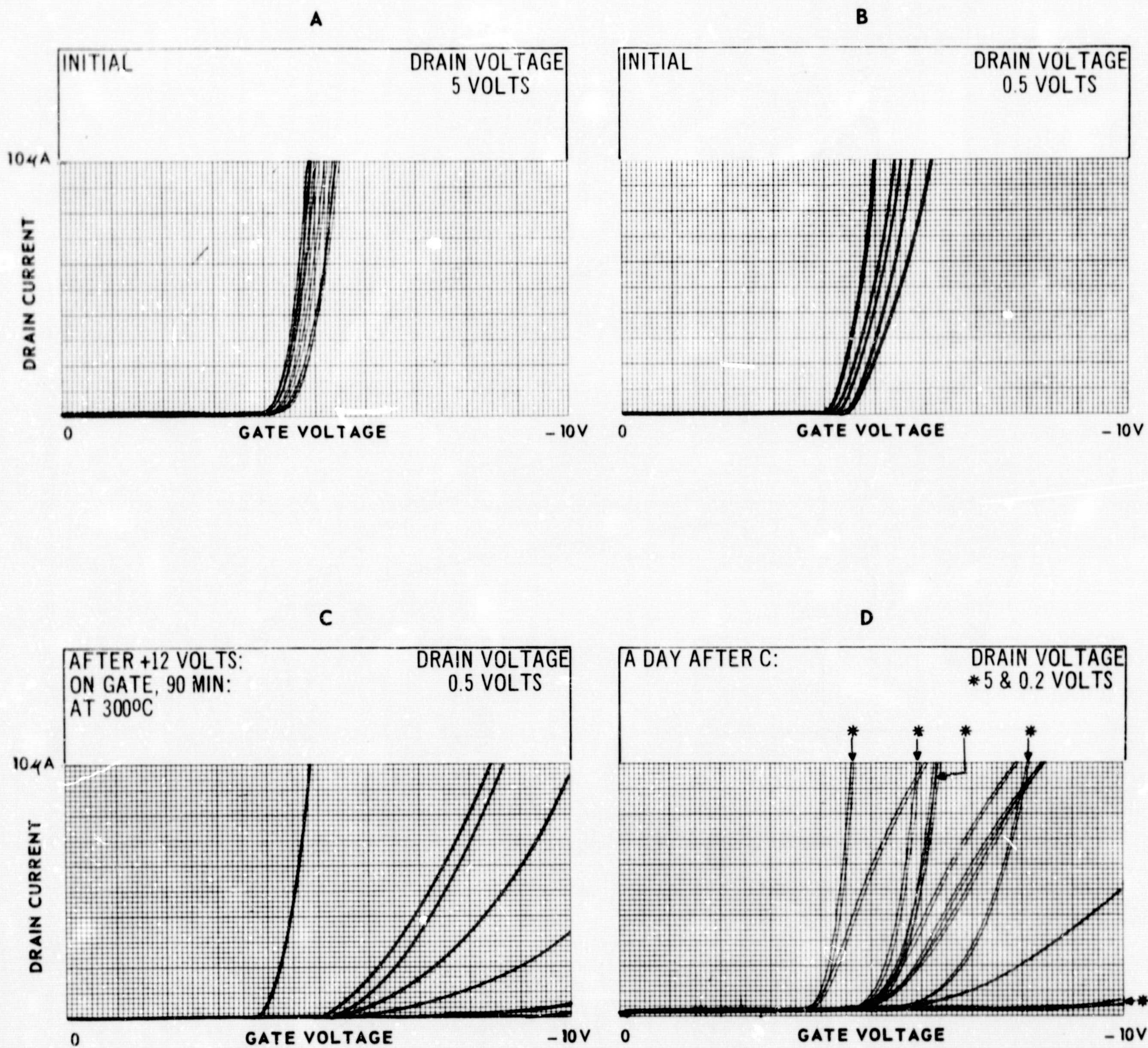


Figure 26. Effects of bake, bias and drain voltage on the transconductance of MOS transistors.

at a drain voltage of 5 volts. Figure 26B shows the initial characteristics at a drain voltage of 0.5 volts to show the effect of drain voltage. This comparison provides a measure of the importance of a change in the electrical (not the metallurgical channel length) channel length. Figure 26C shows the characteristics at a drain voltage of 0.5 volt after +12 volts had been applied to the gate relative to the substrate for 90 minutes at 300°C. This drift treatment would be expected to increase the effective charge density in the oxide. At this point, it was not clear whether the degradation of the transconductance was due to an increase in the electrical channel length because of an increase in the charge density in the oxide, or whether it was due to a decrease in the mobility of the carriers in the inversion layer. A day later, these devices were remeasured at drain voltages of 5.0 and 0.2 volts. The data, in Figure 26D, from these remeasurements show that the characteristics recovered partially but, more importantly, that the transconductance was fairly insensitive to a large change in the drain voltage. Further testing showed that subsequent drifting under negative and positive applied voltages produced reversible changes in the transconductance.

Our interpretation of these data is the following: It appears that the change is due more to a change in the carrier mobility than to changes in the length of the channel.

This might be due to the introduction of fast states in the interface by the mechanism postulated by Goetzberger et al.[39, 40]; that is, the drift of sodium ions toward the silicon interface may create coulombic centers in the oxide that act as surface states, and thereby immobilize carriers that would otherwise contribute to the conductivity of the inversion layer. Further work is necessary to more clearly define the exact mechanism involved in the observed dependence of the transconductance on the position of the mobile ions in the oxide.

Information Obtained from the Correlation of Data from Several Test Structures

Having a combination of different test structures on the same wafer creates opportunities for correlation studies among data taken on different structures. For example, we have measured the mobile charge in the two MOS capacitors, in the MOS transistor having a 1-mil channel length (the surface-ion test structure), and in the MOS transistor having a 0.40-mil channel length between oxide cuts (0.24 mils between diffused junctions). These devices were chosen from an experimental lot that were known to have a fairly high density of mobile charge. The measured charge densities were those given in Table IX.

TABLE IX

Mobile Charge Densities Found in

Different Structures on the Same Chips

Structure	Mobile Charge ($300^\circ C$, ± 12 V, 12 min.)
MOS capacitor, 30 x 30 mil	$7. \times 10^{11}$ cm^{-2}
MOS capacitor, high perimeter-to-area ratio	2.9×10^{11}
MOS transistor, 1 mil channel length	1.8×10^{11}
MOS transistor, 0.4 mil channel length	0.4×10^{11}

CONCLUSIONS

1. The model for the factors infuencing the silicon surface potential has been revised with the addition of fast states at the oxide-silicon interface; dipoles in the oxide; and mobile ion traps at the oxide-metal interface, at the insulator-insulator interface and at the top surface of the oxide.

2. Models have been developed for possible instabilities that might occur due to complex migration of ions. Specifically, these models include the interaction between ions on the oxide surface with those in the oxide, and a situation in which positive ions drift toward the silicon under the application of a negative voltage on the metal.

3. Several new test structures have been added to the set of available test structures.

   a. An MOS transistor with a digitated gate has been designed to combine the functions of the surface-ion test structure and the capacitor with the high periphery-to-area ratio into one structure. This dual function structure is much smaller in area than that needed for the two structures it replaces. The digitation increases the sensitivity of the surface-ion test structure to surface-ion effects.

b. A surface-ion test structure has been designed to have cuts in a second-layer oxide over the first-layer metal to increase the sensitivity of the test structure to surface-ion effects, when a second-layer oxide is present over the metal.

c. A p-n junction diode has been designed to have a high periphery-to-area ratio to increase the sensitivity of the diode characteristics to surface effects.

d. MOS transistors with different channel lengths have been designed to provide means for studying the effects of variations in channel length.

e. A test structure has been prepared for the direct measurement of surface conductivity.

f. A lateral bipolar transistor has been included to provide additional means for studying surface generation and recombination.

4. In addition to the improvements made in the design of the set of test structures, we have improved the understanding concerning the most effective use of test structures. MOS microcircuits have three types of area that should be evaluated -- gate oxide under metal, field oxide under metal, and field oxide not under metal. Bipolar microcircuits surface properties should be evaluated in both the base (isolation) and collector types of area in regions that are, and those that are not, covered by metal.

5. The use of test structures has been described in detail for five types of applications:

a. Preliminary evaluation of experimental materials and processes.

b. Development of promising materials and processes.

c. General use in MOS microcircuits production.

d. General use in bipolar microcircuit production.

e. Specific use on individual microcircuit types in which the test structure is formed by a change in the metal pattern.

6. The use of test structures in combinations is shown to provide additional data that cannot be obtained from single test structures.

a. Comparisons of MOS capacitor and MOS transistor data provide a measure of the fast state density.

b. Comparisons of properties of transistors having different channel lengths provide a means for studying variations along a channel length of MOS transistors, e.g., variations due to the effects of the p-n junction.

c. Comparisons of mobile charge densities in MOS capacitors having narrow metal regions with densities in large area capacitors may provide a measure of the gettering of mobile ions by the top surface of the oxide.

7. Additional information can be obtained by making measurements at different temperatures. The effect of temperature on MOS capacitors or on MOS transistors provides a measure of fast state densities.

8. Specific sets of test structures have been suggested for general use with MOS microcircuit production wafers and with glass passivated and multilevel microcircuit structures.

9. It has been demonstrated that test structures can be made for a given type of microcircuit by a change in the metal pattern to create test structures from the regular microcircuit structure.

10. Specific techniques have been proposed for conserving the area needed for test structures. One example is the combining of the surface-ion test structure with the MOS capacitor having the high periphery-to-area ratio. In this case, area is conserved both by the replacement of two test structures with one, and by choosing a transistor structure rather than a capacitor structure (capacitors require a much larger area than transistors). Another example is the sharing of a common contact by two or more test structures.

11. A detailed theoretical analysis was given of the use of a thick oxide layer to reduce or prevent the effects of surface ions.

12. The use of qualified test wafers for quality monitoring of materials, procedures and equipment has been found very useful for control of the standard process used for microcircuit production, and as a standard against which experimental results are compared.

13. Capacitance-voltage measurements taken with a gold ball probe on unmetallized oxides provide a sensitive measure of the dryness of the oxidation ambient.

14. Experimental data show the effects of hydrogen, water and aluminum on the annealing of fast states. Our experiments show that the removal of aluminum by the standard process used in microcircuit production significantly diminishes the annealing of fast states in an alloying process. Therefore, we believe it to be important to evaluate both regions under a metal and those not under a metal in a microcircuit.

15. Additional evaluations have been made of oxides suitable for second-layer insulators. Vapor plated aluminum oxide deposited by techniques that are compatible with structures having multilevel metal have been evaluated for possible use as second-layer insulator materials and have been found to be unstable. All of the stable vapor deposited aluminum oxides of which we are aware have been deposited at temperatures

that are too high to be compatible with the processes used for building multilevel-metal microcircuits. Vapor plated titanium oxides appear to provide some stability but, if they are to be used in fabricating microcircuits, etching techniques will have to be developed. SiO_2 layers that were r-f sputtered from sources of the highest available purity were found to be quite unstable.

16. It has been observed that the density of mobile ions in transistor structures is lower than in large area MOS capacitors on the same chip. This has been interpreted as being due to two mechanisms:

a. The electric field at a p-n junction appears to drift mobile ions from the oxide over an n-type region to that over a p-type region -- this is a stabilizing influence on p-channel MOS transistors, and of npn bipolar transistors in which the region of highest resistivity is the n-type collector.

b. A top surface of an oxide which is not covered by metal appears to be capable of gettering mobile charge. This would tend to increase the stability of devices that are dimensionally small.

17. Two proposed solutions to surface ion problems have been evaluated experimentally. The use of a thick oxide (the exact thickness being calculable, given the charge density in the oxide and the operating voltage) has been demonstrated to provide a stabilizing effect on production microcircuits. On the other hand, it was observed that the addition of a second layer of metal over the second layer of oxide can add instability.

18. Experiments have shown that the transconductance of an MOS transistor can be significantly altered in structures known to contain mobile charge in the oxide, even when the threshold voltage of the transistor is not altered. This change has been tentatively attributed to a change in the average carrier mobility in the channel. A comparison of the influence of drain voltage on the transconductance and the effect of the drift-bias treatment indicates that the change in the transconductance is not due to a change in the effective channel length that could be expected from a change in the effective charge density in the oxide.

19. Data have been taken that show how the electrical properties of an oxide change as the oxide is subjected to each step in a complex bipolar microcircuit production process. The data show that the charge densities in the oxide are improved by the phosphorus emitter diffusion. Subsequent steps that remove

some of the phosphorus glass do not degrade these charge densities. A subsequent deposition of vapor plated SiO_2 can add a mobile charge density that is too high for the phosphorus to getter. The mobile charge added by the vapor deposited SiO_2 is insidious -- it was not observed in the initial measurements but only after bias aging experiments.

20. An experiment has been conducted to determine the effect of a vapor plated phosphosilicate over MOS transistors that were fabricated in an MOS microcircuit fabrication process. There was no significant degradation of the transistor parameters. There was an increase in the transconductance.

RECOMMENDATIONS

We recommend that studies be continued to:

1. Conduct theoretical and experimental studies of the factors which affect the fundamental electrical properties of the Si-SiO_2 interface of structures having two dielectric layers on silicon.
2. Further develop the models and the understanding of each of the surface-related causes of instability in multilevel microcircuits.
3. Conduct correlation studies to establish the value of test vehicles for the determination of the reliability of actual microcircuit structures of both the bipolar and MOS type.
4. Correlate effects of deposited second-layer insulators over structures used in LSI arrays on life test data with measurements taken on test structures.
5. Conduct investigations to evaluate specific process changes for the improvement of microcircuit reliability.
6. Experimentally determine the effects of complex ion migration of various kinds.
7. Determine the exact nature of the cause of the degradation in the transconductance of MOS transistors.

8. Experimentally evaluate the new test structures which have been designed for addition to the set of available test structures.

9. Establish whether mobile ions exist at an interface between two insulator layers.

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APPENDIX A

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APPENDIX B

NEW TECHNOLOGY

To conform to the requirements of the New Technology clause of the contract, a review meeting was held to determine the reportable items. Personnel participating in the review included G.L. Schnable, the Program Manager, and E.S. Schlegel, the priniple investigator on the program.

A list of reportable items is given below. The items are innovations or improvements in the technology. No inventions were made during the performance of the work under the contract, nor have any invention disclosures been prepared. Philco-Ford does not consider these items to be susceptible to protection under United States patent laws and thus does not consider the provisions of parts (1) and (2) under paragraph (h) of Section III of the New Technology clause to be applicable.

No subcontracts were let under this contract.

1. Improved model of charge distribution. (Pages 8-11.)

Based on information assembled from the literature and from experiments performed during the program, the model for the distribution of electric charge in multilevel metallized metal-insulator-semiconductor structures was extended to include additional types of charge and charge states to those that were in the model developed earlier in the program.

2. Model for complex ion migration. (Pages 15-18.)

Models have been developed to improve the understanding of instabilities due to the complex migration of mobile ions. These models extend the understanding of instability beyond that of the effects of individual influences contained in the model of charge distribution covered in item 1 above.

3. Improved test structure for studying the effects of surface ions and of contaminant migration beneath metal layers. (Pages 22 and 37.)

An MOS transistor has been designed with a digitated gate that combines the following capabilities into a single structure having a smaller area.

a. It can be used to study the migration of contaminants to and from regions beneath a metal layer. This device requires significantly less chip area than its predecessor, the MOS capacitor with a high perimeter-to-area ratio.

b. It can be used to study the effects of surface ions. The digitated gate makes it more sensitive to surface-ion effects than its predecessor, which had only a single gate digit.

4. Structure for studying surface ion behavior on a second-layer insulator. (Page 22.)

To increase the sensitivity of the test structure for studying the effects of surface ions on a second-layer insulator over a metal layer, a test structure has been designed to have openings in the second-layer insulator to make it easier for ions to drift from the metal to the top surface of the insulator.

5. Effective use of test structures. (Pages 23-37.)

Studies of various ways in which test structures can be most effectively used for the development and production of reliable microcircuits have resulted in a number of specific recommendations. These recommendations pertain to the types of microcircuit area to be evaluated, to the types of application for which test structures are useful, and to possibilities by which the results taken from several test structures can be combined to yield data that could not be obtained from single test structures.

6. Test structures created from microcircuit chips. (Pages 34-37.)

It has been shown that test structures can be created from existing microcircuit structures by changing the pattern of the metallization.

7. Review of the application of test structures for the study of surface effects in LSI circuitry. (Entire report.)

A detailed summary of considerations in the application of test structures for the study of surface effects in LSI circuitry was prepared. This information was prepared for oral presentation at the Seventh Annual Symposium on Reliability Physics and for submission as a manuscript to the IEEE Transactions on Electron Devices for consideration for a special issue, covering selected papers from that symposium. This paper combines in one article a thorough review of the use of test structures for the improvement and control of the performance and reliability of microcircuits of all types.