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N 69 26281

NASA CR 101139

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STUDY OF SEMICONDUCTOR HETEROJUNCTIONS

OF ZnSe, GaAs and Ge

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April 1969

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Prepared under Research Grant No.
NGR 39-087-002 by
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ABSTRACT

The fabrication and properties of GaAs-Ge, ZnSe-Ge and GaAs-ZnSe heterojunctions are being studied. The problems associated with autodoping in the growth of GaAs on Ge encountered with a close-spaced HCl process are discussed. The doping and contacting of ZnSe layers grown by this process are also considered in depth. A high-frequency transistor measuring system was completed and checked on commercial homojunction transistors. Three methods of growing Ge epitaxially on ZnSe or GaAs at low temperatures are presently being investigated and are considered in this report.

I. INTRODUCTION

The research in progress comprises a detailed study of several classes of semiconductor heterojunction structures. The studies are aimed at obtaining a better basic understanding of the conditions for minority carrier injection, the transport mechanism for carriers across the interface and the photo-voltaic properties of n-p heterojunctions.

The heterojunction pairs being studied are nGaAs-pGe, nZnSe-pGe and nZnSe-pGaAs. In the previous report,[1] the general nature of the problems to be considered as well as the benefits to possibly be obtained from heterojunction were discussed. In addition, the properties and the problems to be considered in heterojunction fabrication were reviewed. The work to date on this grant has been concerned with investigating the problems of making good diode and transistor structures for the above semiconductor pairs.

During this report period the problems concerned with the fabricating of GaAs-Ge heterojunctions, particularly the autodoping of the GaAs with Ge and the Ge with As were investigated. The problems of doping grown ZnSe layers and of making ohmic contact to them were thoroughly considered and some tentative conclusions reached. Initial growths of ZnSe on GaAs were accomplished and some diodes made. Attempts to grow the GaAs on ZnSe, however, were unsuccessful probably because of the formation of H_2Se which interfered with the transport process. A high-frequency transistor measurement capability was developed and some measurements were made on commercial homojunction transistors prior to those on our heterojunction units. The investigation of the low temperature growth of Ge on ZnSe by the solution growth method and Ge on GaAs or ZnSe by the disproportionation of germanium diodide was continued with changes made in both systems. In addition work was initiated to evaporate Ge on ZnSe or GaAs in an ultra-high vacuum system at a low substrate temperature.

2. GROWTH OF GaAs-Ge HETEROJUNCTIONS

During the past report period the work in this area fell into the three categories as discussed below.

2.1 Autodoping of GaAs Epitaxial Layers

Although conditions of growth had previously been established which produced thick GaAs layers of good quality, some observations indicated that a region of comparatively high resistivity or a barrier to current flow existed near the interface. Typically the bulk region of the GaAs layers has a mobility of about 3000 cm^2 $(V\text{-}sec)^{-1}$ and a carrier concentration of about 5×10^{16} cm^{-3} or less. Even in the case of degenerate n-n heterojunctions, however, the resistance between ohmic contacts to the GaAs surface and the Ge surface was larger than the measured contact resistance of the particular ohmic contact. The relatively ohmic nature of n-GaAs layers grown on degenerate p-Ge (so as to prevent conversion of the p-layer by arsenic) also indicated that the GaAs near the Ge interface was heavily doped. This lead to the study of the carrier concentrations in the regions near the GaAs-Ge interface.

Carrier concentration profiles were made of GaAs films grown on Ge under various conditions. The procedure was to fabricate Schottky barrier diodes on the surface and measure the variation of capacitance with voltage, then etch away a small thickness and make another diode. The layers studied were grown at 600°C and 650°C on (100) and 8° off (111) Ge seeds. The HCl concentration varied from .03% to .2%. It was found that for all layers the carrier concentration increased rapidly within 1μ of the junction. In all layers at 0.3 to 0.5μ from the interface the electron concentration was greater than 2×10^{17} cm^{-3} whereas the concentration at a thickness of 2-3 μ was 1 to 5×10^{16} cm^{-3}. An extrapolation of the data indicates that the carrier concentration near the interface should be greater than 10^{18} cm^{-3}. The results appear to be reasonably independent of the growth conditions studied and most likely are a result of Ge autodoping.

2.2 Autodoping of Ge Substrate by Arsenic

We have determined that for normal growth conditions at moderate HCl concentrations the concentration of arsenic incorporated at the surface is about 1 to 2 x 10^{19} cm^{-3} which agrees with the solid solubility data. In cases where extraordinarily high HCl concentrations are used the concentration may be such as to overcompensate a diffused p-type layer of surface concentration $\sim 5 \times 10^{19}$ cm^{-3}. This may be explained by concentration enhancement of the solubility of arsenic. There appears to be some surface limitation for diffusion of arsenic from the GaAs layer because we find that the surface concentration is lower for higher substrate growth temperatures (longer arsenic diffusion lengths).

In a previous report we discussed the effect of varying the growth system start-up procedure on the arsenic surface concentration of the Ge substrate. It was shown that by doubling the flow rate during the early part of the run so as to raise the HCl concentration quickly the As surface concentration could be lowered to about 8 x 10^{18} cm^{-3} for substrate temperatures of 600°C. Increasing the initial flow rate to five times the normal value in a separate growth run resulted in an As surface concentration of 2 x 10^{19} cm^{-3}. A further experiment indicates that an HCl concentration of .01% coupled with a high enough temperature gradient to achieve a reasonably high growth rate results in a very thin arsenic converted layer in p-type Ge. No definite measurements of diffused depth could be made, presumably because of the very shallow depth and proximity of the junction to the surface.

For growth runs where the initial gas flow is twice the normal flow for a period equal to the time constant for filling the growth system, the shallow diffusion depths of arsenic into p-Ge seeds have been measured by precise angle lapping and photo-voltage measurements. The sheet resistances of the diffused layers have also been measured by an analogous technique. The arsenic surface concentration may be calculated from the diffusion coefficient (D) appropriate to the temperature cycle of the growth run and the measured junction depth (x_j).

It may also be calculated from the measured sheet resistance and the measured junction depths. For this purpose published curves by D.B. Cuttriss [(2)] are used.

The surface concentration (C_s) calculated from D and x_j, has a value of about 8×10^{18} cm^{-3} for runs made at 600°C. This agrees in most cases with the value obtained from the sheet resistance. A portion of the material (nGaAs layer on pGe) from one such run was subsequently diffused in a sealed, evaluated ampoule of small volume at 650°C for 6 days. The resulting x_j using the appropriate value of D implies a value of C_s of $2 - 3 \times 10^{18}$ cm^{-3}. The sheet resistances measured are in general agreement with this result. The lowering of the arsenic concentration by post-diffusion indicates that there is a limitation of the supply of arsenic to the Ge surface from the GaAs. The values normally obtained for these runs are near the solid solubility for the growth temperature. The specific conditions referred to are a substrate temperature of 600°C-650°C, HCl concentration of .036%, initial flow rate of double the final rate, and substrate orientation of 8° off the (111) plane toward (100). In order for there to be a limitation of the arsenic supply from the GaAs to the Ge there must either be a large difference in the diffusion rates or there must be a barrier to the diffusion process at the interface.

Goldstein[(3)] has measured the self-diffusion of Ga and As in GaAs and found a relatively temperature independent diffusion coefficient of 4×10^{-14} cm^2/sec. below 1200°C. However, Kendall[(4)] has reviewed the available literature and finds that values of D_o and Q of .7 $cm^2 sec.^{-1}$ and 3.2 eV are in better agreement with theoretical predictions. The value of the self-diffusion coefficient of As in GaAs calculated from Kendall's data is 3×10^{-19} $cm^2 sec^{-1}$ at 600°C. The value for As in Ge is 10^{-13} $cm^2 sec^{-1}$ at the same temperature. From simple diffusion theory the ratio of the concentration at the interface between the two materials will be equal to the square root of the ratio of the diffusion coefficients in the two materials. The interface concentration ratio calculated from the above data is 1.7×10^{-3}. This yields an arsenic surface concentration of about 4×10^{19} cm^{-3}.

Although this is about an order of magnitude higher than the observed As surface concentrations after post diffusion it is not unreasonable to suppose that simple theory accounts for the observed behavior, especially in view of the large uncertainty in the self-diffusion data for GaAs.

2.3 Device Characteristics and Fabrication

Two growth runs made during this period illustrate, together with previous work, the essential limits on heterojunction transistor formation by this growth system. The first was made at 0.036% HCl concentration and 600°C seed temperature onto two n-type seeds with a diffused p-layer. The surface concentration of one was approximately 4×10^{18} cm^{-3} and of the other 2×10^{19} cm^{-3}. The surface of the seed diffused at $4 \times 10^{18} cm^{-3}$ was converted to n-type while that diffused at 2×10^{19} cm^{-3} was not converted. After the growth run the base-collector junction of the resulting nGaAs-pGe-nGe transistor showed the typical low leakage and good saturation of a good Ge diode. The emitter-base junction or heterojunction was very lossy and none of the devices fabricated exhibited any current gain.

The second run was done at 0.036% HCl concentration at a seed temperature of 570°C onto a seed diffused with a surface concentration of approximately 5×10^{18} cm^{-3}. The resulting heterojunction transistors exhibit very good base-collector junctions and the DC current gain (β) ranges from 1 to 5 with the β of most devices lying between 1 and 2. The gain of these devices is reasonably constant with increasing emitter current.

Previously, transistors have been made in our laboratory under conditions favoring rapid growth and poor GaAs crystal quality. These transistors exhibit values of β from 2-10. Some devices with relatively poor base-collector junctions show gains up to 50.

These devices all had a high resistance emitter. Conversely, transistors made under conditions favoring good crystal quality, as above, show low gains, yet have low emitter resistances. Our results suggest that in this system, the growth of good quality layers is always accompanied by heavy autodoping of the GaAs near the heterojunction by Ge as was reported previously. On the other hand, by maximizing the growth rate by means of increased HCl concentrations, the effective carrier concentration in the GaAs at the interface appears to be lower. Gain is realized but is traded for high emitter resistance due to low mobility.

Also during this period static current-voltage characteristics have been studied for some heterojunction diodes grown at 550°C and 600°C on .003 Ω-cm p-type Ge and for the emitter heterojunctions of the most successful transistor run. The transistors were grown at 570°C on a base region with an approximate acceptor surface concentration of 5×10^{18} cm^{-3}. Capacitance-voltage curves have also been taken for a few of the heterodiodes which have sufficiently low leakage.

The interpretation of the current-voltage characteristics of these junctions is unclear at this point. If the v-i relations are plotted on log-log paper they exhibit a straight line region indicating a power law variation for a portion of the characteristic. The exponent varies from 2-4 at room temperature and increases to 7 or 8 at low temperatures. On the other hand, if the v-i relations are plotted as ln I vs. V they also exhibit a straight line region for a portion of the characteristic indicating the normal thermal diode behavior.

The power law variation is normally associated with space-charge-limited current in the presence of traps in high resistivity material. The capacitance-voltage curves of the heterodiodes grown at 550°C, however, show a variation of $1/C^2$ vs. voltage from which a fairly consistent value of about

4×10^{17} cm^{-3} is derived, presumably for the electron concentration in the GaAs. This value represents a lower limit, since any errors in the effective area of the diode due to a possible high value of film resistivity would result in increasing the value. Values of moderate resistivity might result for low values of mobility in these heavily autodoped thin films. The electron concentration of the surface of the GaAs in the transistors was found to be about 5×10^{17} cm^{-3} by Schottky diode measurements.

One possible explanation is to assume that current-voltage characteristic is dominated by the properties of a region near the interface which may be compensated to a moderate or high resistivity or else has a high concentration of interface states which affect the characteristic. If the heavy doping level remains up to the junction it would lead to a very narrow depletion region so that tunneling effects may be important. At present we are attempting to arrive at a satisfactory explanation for these seemingly contrasting observations.

3. DOPING GROWN ZnSe LAYERS

For some time attempts have been made to dope layers of ZnSe 2-5 μ thick grown on Ge and GaAs by the HCl close-spaced epitaxial process. Grown ZnSe has resistivities of 10^{6}-10^{8} ohm-cm if no attempt is made to suppress Zn vacancies (acceptors) which form above 400°C. These acceptor-like vacancies compensate any donors, and the ZnSe becomes high resistivity. ZnSe can be doped to 0.1-10 ohm-cm by submerging it in molten zinc (suppress Zn vacancies) plus a donor dopant (Ga, Al, In) at temperatures above 900°C. Such a technique is not directly applicable to grown layers of ZnSe since Zn attacks the Ge and GaAs substrates and introduces excessive strain at temperatures above 900°C. Thus other methods of doping at lower temperatures have to be resorted to.

High resistivity grown ZnSe shows space-charge-limited current flow which masks the true characteristics of ZnSe-Ge and ZnSe-GaAs junctions, and creates excessively large emitter resistances in ZnSe-Ge and ZnSe-GaAs transistors. It is imperative that this high resistance ZnSe be made more conducting. Several methods were used to lower grown layer resistivity. All make use of Zn overpressure to suppress Zn vacancies, donor incorporation by diffusion, growth from doped sources, or a combination of all these. However, all these methods have failed to produce grown layer resistivities less than 1000 ohm-cm, for which space-charge characteristics are still dominant.

A list of the methods tried to lower grown ZnSe resistivity is given below. A brief discussion of each method along with its results follows.

Method I. Growth from Ga doped ZnSe sources followed by passing Zn vapor over the growth as it is cooled to room temperature.

Method II. Diffusion of Zn from evaporated Zn layers into ZnSe grown from Ga doped sources.

Method III. Placement of Al in the HCl line during the growth process.

Method IV. Open tube diffusion of Ga immediately after growth.

Method V. Closed tube diffusion of Ga and Zn after growth.

Method I. This method was previously employed [4,5] and appears to give the best results. Ga sources with a donor concentration of 10^{17} cm^{-3} give 10^{14} cm^{-3} Ga grown material (1000 ohm-cm) indicating a low dopant transfer ratio. Al doped sources with a donor concentration of 5 x 10^{18} cm^{-3} yield 10^5 -10^6 ohm-cm grown material and therefore have not been used. It is believed that any free Ga or Al reacts with the HCl to form stable Ga and Al chlorides. V-I characteristics of the ZnSe-Ge (GaAs) junctions so treated show a high power law (space-charge) forward current (ZnSe negative) and a good reverse characteristic ($< 1 \mu a$, 10V). It should be pointed out that this method provides doped ZnSe as it emerges from the growth system allowing the zinc step to occur during slow cool-down. No further strain or crack producing heat treatments are necessary. All the other methods except Method III require after-growth heat treatments or excessive temperatures.

Method II It was thought that diffusion of Zn from an evaporated layer might be more effective than Zn vapor diffusion (Method I). In this method a thin (1000-2000 Å) layer of Zn is evaporated onto the grown layer surface along with an overlayer of protective Al to prevent Zn evaporation. The heterojunction and its Zn-Al layer is then heated slowly (2°C/min) to 450°C-500°C for periods of 10 min. to 2 hours and then cooled at the same rate to prevent cracking. ZnSe layer thicknesses ranged from 1 μ to 8 μ on (111) and (100) Ge substrates and on (111) GaAs (Ga-face). V-I characteristics indicated ZnSe resistivities and forward characteristics as good as Method I. However, the reverse characteristic was usually similar to a 10K-100K resistor indicating a possible pile up of Zn at the interface. ZnSe-GaAs junctions had better reverse characteristics than did ZnSe-Ge probably because the diffusion coefficient of Zn in GaAs is much larger than that for Ge allowing for less Zn pile up.

It appears that zinc diffusion from the vapor and from evaporated layers is equally effective in reducing ZnSe resistivity by Zn vacancy suppression. To reduce the resistivity further it will be necessary to incorporate more donor atoms such as Al or Ga into the lattice. The next three methods attempted to do this.

Method III ZnSe was grown on Ge using a Ga doped source along with some Al placed in the growth system HCl line immediately before the growth area. The Al would react with the HCl, be carried to the growth area as $AlCl_3$, and be incorporated into the growth as elemental Al or a chlorine compound. Al was chosen over Ga because 1) elemental Ga in the active part of the growth system promotes ZnSe etching and poorly grown layers and 2) Al dopes ZnSe more heavily than Ga does. The results of the experiments however, indicated that the $AlCl_3$ was too stable to allow incorporation of Al in the ZnSe. Layers grown by this method were no better than those grown with only Ga source material (10^3 - 10^5 ohm-cm).

Method IV Ga vapor diffusion in the growth system appeared attractive because separate experiments with vapor diffusion of Ga into bulk ZnSe gave resistivities of 0.1-0.2 ohm-cm whereas the same experiment with Al yielded 1-10 ohm-cm material - which is no better than that obtained with only a zinc vacancy suppression step. Also at elevated temperatures Ga is less reactive with Si than is Al, thereby reducing attack on the growth system quartz and Si blocks. A diffusion temperature of 900°C was chosen as necessary for Ga to diffuse through grown layers a few microns thick in a matter of 1/2 hour. This high temperature restricted this method to ZnSe-GaAs since Ge melts at 940°C and might form a solid solution with ZnSe. All exposed GaAs was protected by a 2000-3000 Å layer of SiO_2.

The open-tube diffusion was performed in the growth system immediately after growth. The source and seed were brought to the growth temperature of 640°C, and then were slowly elevated from 640°C to 900°C (2°C/min). During growth the system had contained a quartz boat of Ga placed upstream of the growth region so that it was not in direct contact with HCl or temperatures greater than 150°C. This boat was then heated to 900°C and Ga vapor was carried by flowing H_2 gas down the tube and over the grown ZnSe layer for 1/2 hour. Then the ZnSe layer was cooled quickly (4-5°C/min to freeze in the Ga) to 800°C and finally slowly (1°C/min) to room temperature. Results for several runs showed that the ZnSe layer tended to be removed by a combination of Ga and H_2 etching at elevated temperatures. It was concluded therefore that this method of doping was not controllable and attention was turned to the possibility of closed tube diffusion of Ga.

Method V In the closed-tube diffusion experiment a grown ZnSe-GaAs heterojunction was sealed up in a quartz ampoule with enough Zn (to suppress Zn vacancies) and Ga to maintain their equilibrium vapor pressures at 900°C. This method is limited to ZnSe-GaAs junctions because Ge is soluble in Zn. The GaAs was protected by SiO_2. The ampoule was heated (2-3°C/min) to 900°C, held there for 1/2 - 2 hours (depends on ZnSe thickness), cooled (4-5°C/min) to 800°C, cooled (2-3°C/min) to 700°C and then quenched in water.

The fast cool from 900°C to 800°C freezes in Ga while the quench freezes in Zn in the ZnSe lattice. This method can produce as much as 10 μ of Ga doped skin on semi-insulating bulk ZnSe. Quenching has not produced cracked material, and the resulting forward V-I characteristic resembles that of the best ZnSe-Ge diodes made using Method I. The presence of Ga has not appeared to lower the resistivity below 1000 ohm-cm.

The reverse characteristic is usually 100-200 KΩ. Figure 1 shows such a V-I characteristic. There still appears to be some degradation of reverse characteristic.

To test the effectiveness of the quenching step one sample heated in Zn and Ga but not quenched was subjected to a separate Zn vapor diffusion step (Method I). The resulting V-I characteristic and ZnSe resistivity was no better than the best obtained by quenching. Also ZnSe-Ge samples grown from Ga doped sources were subjected to quenching after heating in Zn vapor at 750°C. The result was again 1000 ohm-cm ZnSe.

It appears that there is still some problem of getting Ga into the ZnSe lattice; or of excessive compensation due to lattice strain defects, incomplete Zn vacancy suppression, and acceptor impurities; or of lattice mobility reduction seriously hampering conduction. Mobility experiment measurements are being undertaken to see how mobility is affected by the Ga diffusion step. To reduce compensation a ZnSe-GaAs sample was subjected to Method V treatment with no zinc present and no quenching. Omission of Zn should produce more Zn vacancies into which Ga might diffuse thereby enhancing the total amount of Ga in the lattice. Later a Zn vapor diffusion step could remove any remaining Zn vacancies. Results of this experiment were negative because the absence of a Zn overpressure allowed the ZnSe to dissociate and be dissolved by the Ga. Experiments planned on doping ZnSe grown on (100) GaAs and Ge may prove more fruitful due to better grown layers. As of now doping will be done by Method I until a better method can be devised.

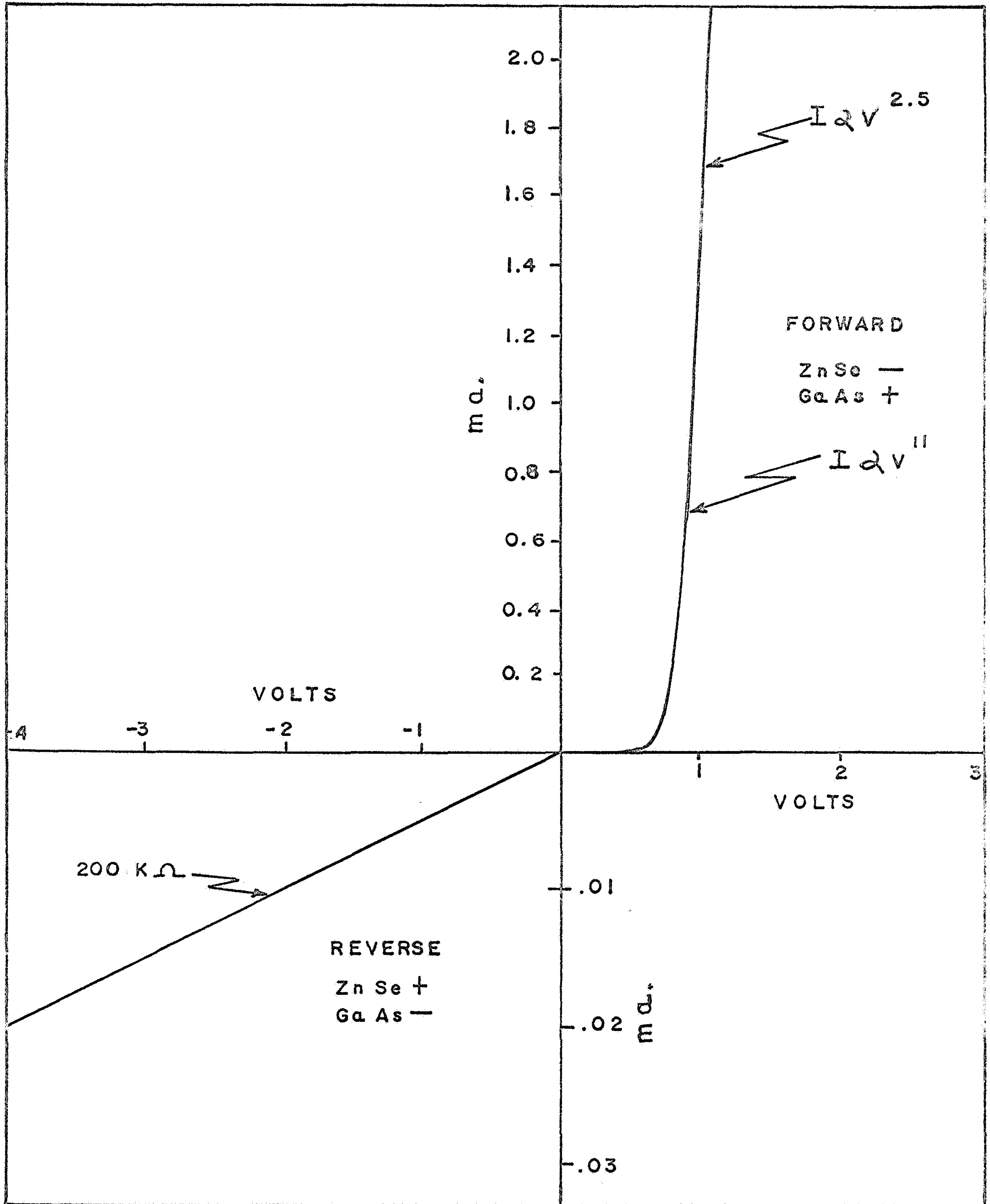


FIG. I ZnSe -GaAs
V-I CHARACTERISTIC

4. PLANAR OHMIC CONTACTS TO ZnSe FOR HETEROJUNCTION TRANSISTORS

By using photomasking techniques it is hoped to produce ZnSe-Ge transistors of controlled geometries. To this purpose emitter etching and evaporated metal contacts experiments were carried out on doped bulk ZnSe crystals that were lapped and were chemically polished either in HCl-methanol or in bromine-methanol etches. It was soon realized however, that the performance of the evaporated contacts on ZnSe etched in this way was far from satisfactory. In general such contacts were non-ohmic with a resistance depending upon the current flowing through the sample. Moreover the resistance was several times larger than the resistance of alloyed contacts on the same material. A closer examination revealed that the main problem was that of wetting the semiconductor surface by the evaporated metal. Since satisfactory contacts in planar geometry are needed before proceeding to photolithographic processes for making ZnSe-Ge transistor, the problem of making ohmic contacts to ZnSe was considered as the first step.

Following the guidelines that In when alloyed makes ohmic contacts to ZnSe crystal, it was decided first to evaporate In on lapped and chemically polished ZnSe samples followed by a heat treatment at 300°C similar to alloyed contacts. Problems arose when the evaporated In layer was heat treated since on melting, the layer broke up into an array of small spheres that spread in random on the ZnSe surface. Also the wetting of the ZnSe surface by the molten In metal was found to be poor, and could not be improved by using HCl gas as a flux. To cope with the first problem a layer of Al was evaporated on the top of In and the heat treatment applied. Since the melting point of Al is higher than the temperature at which heat treatment is carried out (300-400°C) the breaking of the In into small spheres was prevented by this evaporation of Al. However, the wetting of ZnSe surface by the metal was still poor and the resulting contacts were nonohmic and of poor quality. For some samples a thin layer of Ni was evaporated before evaporating the In and Al layers but there was no significant improvement.

Sandwich layers of Zn, In, Al, Ni heated to 500°C for an hour or two were also tried, but showed contact resistances orders of magnitude higher than for alloyed contacts. Alloyed contacts themselves were found to suffer from wetting problems. For contacts alloyed in an inert atmosphere using Hel gas as a flux, it was found that only those parts of the In sphere where the Hel gas is able to penetrate before melting of the In makes contact with the ZnSe surface. Thus on melting the In sphere and on subsequent cooling only a peripheral ring is responsible for the contacts. The central area where HCl gas flux is unable to penetrate is not wetted by In metal properly and does not contribute to the ohmic contact formation. Clearly there is some insulating layer on ZnSe surface that prevents proper wetting of the sample by the molten metal so that contact quality will be sensitive to the surface preparation. This compelled us to examine the question of surface preparation more closely.

In all of the above experiments the ZnSe sample was prepared by lapping successively by 3μ, 1μ, and 0.05μ Al_2O_3 and subsequent etching in 5% Hel + 95% methanol solution for a few minutes. Finally the sample was dried in methanol and was directly taken into the vacuum system. After evaporation and heat treatment a number of regions of about 30 to 40 mil diameter (i.e. of the same order of magnitude as the spheres used to make alloyed contacts to ZnSe) were covered with black wax and the rest of the metal was etched away thus leaving a few circular areas which could be contacted by probes.

A search of the literature on the surface preparation of ZnSe revealed that most chemical treatments leave a thin insulating film on the surface.[6] From these figures it became obvious that no significant improvement in the contact quality can be expected unless this remnant film thickness is reduced. Hence, a special cleaning proceedure very similar to one recommended in reference (6) is being tried. No provision was made to measure the film thickness in the laboratory and the results reported in reference (6) were taken as guidelines. The proceedure is as follows.

The sample is lapped with 1μ Al_2O_3, etched in 1/2% bromine + methanol solution to get a smooth looking surface. After removing

bromine traces the sample was etched for times ranging from 10 to 30 minutes in conc. H_2SO_4 + $KMnO_4$ solution at room temperature. This is followed by a rinse in warm deionized water and soaking in warm KCN solution for about 5 minutes and a subsequent rinse in hot deionized water. Before taking it into vacuum system the sample is dried in methanol as usual.

Since the progress of loading the sample surface may absorb oxygen and other impurities from the atmosphere, a pre-evaporation heat treatment of the sample may be helpful in providing a cleaner surface than otherwise. It was also anticipated that the remnant film may contain some volatile constituents that may evaporate upon heating in vacuum. To heat the sample, a stainless steel holder was made. A nichrome wire heater wrapped in mica sheet was sandwiched between two stainless steel plates. The heating coil was insulated from the metal by mica sheets. A number of experimental runs were made after this new surface cleaning procedure was adopted and the provision for heating the substrate was used. Table (1) shows the results obtained. Although these new procedures bring considerable improvements in the contact quality, the state of affairs is still far from satisfactory. As can be seen from the table, contacts with roughly linear relation between current and voltage are obtained on a substrate heated to 300°C for about one and one-half hour before evaporating In but the quality of these contacts is 3 to 5 times inferior to that of the alloyed contacts on the same material under similar conditions. This discrepancy is definitely due to poor wetting and poor contact area between liquid In and ZnSe surfaces. The use of Ni improves the wetting of ZnSe surface by the molten metal but also introduces something that makes the contacts rectifying instead of ohmic. These contacts breakdown at about 5 volts and the post breakdown value of the resistance is about the same as that of the alloyed contacts. The reason for the rectification is not very clear but probably partly lies in the fact that the material used for evaporation was not pure enough.

Expt. No.	evaporated	Temper.	After evaporation heat treatment	Surface Wetting	Characteristics	Sensitivity	with alloyed contacts	Conclusions	improvem't
9	In & Al	280°C followed by a 3 min heating at 310°C	None	Very poor	5mA 25V 25V 5mA	Very sensitive to light intensity	No comparison	No wetting & no formation of highly doped skin on the surface	(1) Preheating a substra[te] for a long time (2) After evap., hea[t] treatment
10	In & Al	300°C for 1-1/2 hrs.	1 Hour at 500°C in forming gas	Poor	400 to 500Ω resistor	None	3 to 5 times higher resistance	Poor surface wetting. Patchy contacts.	Use of Ni as wetting agent
12	In & Al	Room Temp.	1 Hour at 500°C in forming gas	Poor	Slightly rectifying but very high resistivity ohmic symmetrical.	Slightly	10 to 12 times higher resistance	Pre-evaporation heating essential	Use a wetting agent
13	Electroless Ni In & Al	Room Temp. 300°C	1 Hour at 500°C in forming gas	None	All metals came off during etching.	-	-	Poor adhesion of Ni plating to polished ZnSe surface.	Evaporat[e]
14	Ni In & Al	300°C for 5 min.	80 min. in forming gas at 500°C	Moderately good	15mA 8 4 4 8V 15mA	Slightly	3 to 4 times higher resistance	Either an insulating film or p-n junction	Pre-evaporati[on] heating o[f] the sampl[e]
16	Ni In & Al	300°C for 2 hours	75 min. in forming gas at 500°C	Good	15 ~70 Ω 4V 4V	Sensitive to light	1.2 to 2 times higher resistance	Formation of Rectifying junctions	Use pure [...] Improve polishing

TABLE #1 Ohmic Contact Experiments on ZnSe

However, when Ni was chemically plated instead of evaporating the results could not be improved either. Two problems must be solved: a) a means must be found to get good wetting of ZnSe surface by the molten metal, b) the thickness of the high resistivity insulating layer at the ZnSe surface should be reduced to a minimum. Speculation on the nature and composition of the insulating layer suggests that ZnO is an important constituent of this surface layer. The important points that have been brought into light are:

(a) In the pre-evaporation of sample for making ohmic contacts, chemical etching by diluting HCl or bromine-methanol is to be avoided. Preferably an unetched and solvent-clean surface should be used.

(b) If chemical etching seems to be necessary at some stage than an etch in $K_2Cr_2O_7 + H_2SO_4$ solution at 80°C followed by a rinse in warm water and subsequent treatment in KCN solution is advisable.

(c) To promote wetting, use of Ni or some halide flux such as $NH_4Cl + InCl_3$ or $NH_4Cl + ZnCl_2$ offers promise. These fluxes react with ZnO and are expected to reduce the insulating layer thickness at the surface of ZnSe.

(d) Use of liquid alloys such as In-Tl, Hg or In-Ga should be tried. In the latter case there are some indications [7] that the insulating film is penetrated if the sample temperature is raised to above 400°C. To avoid the out diffusion of Zn, this rise in temperature and subsequent cooling has to be relatively rapid.

(e) Ion bombardment of the semiconductor surface immediately prior to metal evaporation has produced ohmic contacts on CdS [8,9]. This may also be helpful in providing ohmic contacts to ZnSe surface.

5. FABRICATION OF ZnSe - GaAs JUNCTIONS

During this period the feasibility of ZnSe growth upon GaAs, and GaAs upon ZnSe was studied in the HCl close-spaced epitaxial growth system. nZnSe-pGaAs is an attractive pair for optical studies such as the window effect and junction electroluminescence. Preliminary runs in the HCl system indicated successful growth of ZnSe upon GaAs [5]. In these runs Ge was present in the growth system to enhance the ZnSe growth rate. However in this study to be reported

here no Ge was ever present in the growth system. The previous 6 month report [1] describes the growth of ZnSe upon Ge and the salient features of the HCl growth system. The growth morphology and single crystallinity of ZnSe layers prepared in the system is shown in Figure 2 for growth on (111) and (100) Ge surfaces. The (111) surface produces very nice pyramids while the (100) surface produces a mosaic structure of canals a few hundred Å deep. Laue spots on 12 μ thick (111) and (100) growths show well defined sharp spots of 6 fold and 4 fold symmetries respectively. This indicates good single crystal material.

Several growth runs of ZnSe upon GaAs were done (Fig. 3) and the results are summarized in Table 2. In all cases the ZnSe was prepared by lapping to 3 μ (alumina) and etching in HCl. GaAs was hand lapped to 1 μ, hand polished with a 3:1 solution of water and Chlorox, and polish etched in $H_2SO_4:H_2O_2:H_2O$, 5:1:1. All GaAs areas not grown upon were protected with SiO_2. The growth rates on As (111) faces are more than twice that on Ga (111) faces. Ga face growths consist of small pyramids less than 1/2 μ in height, and As face growths are flat with irregular depressions of about 1 μ. This behavior on the Ga (111) plane has already been observed [10]. Single crystallinity of these layers has not yet been determined, since most grown layers are only a few microns thick.

Figure 4a shows a chip of GaAs from which all but a circular portion of grown ZnSe has been removed by concentrated hydrochloric acid. Hydrochloric acid etches ZnSe about 100 times as fast as GaAs so that the ZnSe can be selectively removed. The appearance of the GaAs shows it has not been etched during the growth process as is evidenced by its pre-growth smoothness. This means that the ZnSe-GaAs junction is as flat as the original GaAs surface and that solid solutions of ZnSe and GaAs are unlikely at the interface. Figure 4b shows the smooth ZnSe surface obtained in the middle of a rough ZnSe growth on an As face. This may be an anomolous result, but a guess is that it occurred from a small smooth region between two twin bands in the ZnSe source directly above it during growth. The rest of the ZnSe source was roughened from HCl gas etching during

TABLE 2 Summary of Runs of ZnSe upon GaAs

Run #	Seed Orientation	ZnSe Temp.	GaAs Temp.	HCl Concentration	Growth Rate
CS-38	Ga(111)	760°C	640°C	.045%	1.5μ/hr
CS-39	Ga(111)	760°C	640°C	.10%	3.0μ/hr
CS-44	Ga(111)	780°C	640°C	.045%	2.5μ/hr
CS-45	As(111)	760°C	640°C	.045%	3.2μ/hr
CS-46	As(111)	760°C	640°C	.03%	2.5μ/hr
TR-2	As(111)	760°C	640°C	.045%	3.5μ/hr

Seed to source spacings ranged from 12-17 mils.
H_2 flow rate was approximately 200 cc/min in a reaction tube of about 3.8 cm inside diameter.

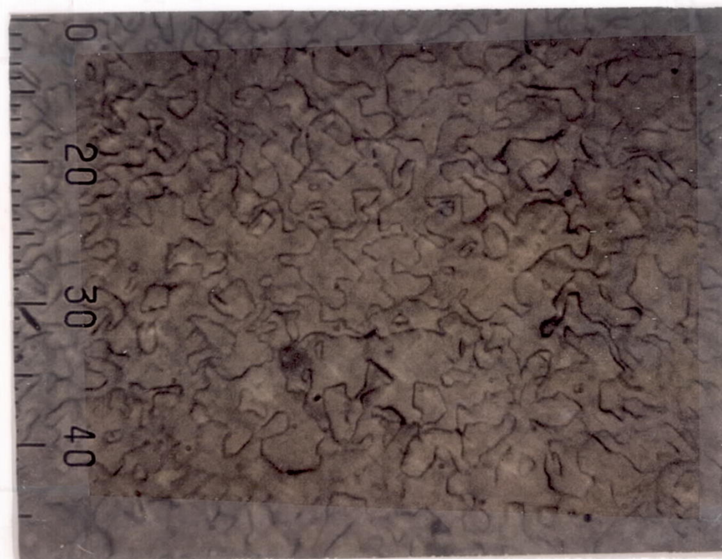
growth. The morphology of the HCl etched ZnSe source was probably transferred to the grown layer. Smooth growths of ZnSe are desirable for ZnSe-GaAs transistor studies (planar base region) and reasons for this smooth growth are being investigated. Also growths on (100) GaAs are planned to see whether these provide smooth growth surfaces.

V-I characteristics of grown ZnSe-GaAs junctions resemble those of ZnSe-Ge. The forward characteristic (ZnSe−) shows a power law dependence (space-charge) while the reverse is a fairly high resistance. Figure 1 shows such a ZnSe-GaAs V-I characteristic after Zn and Ga treatment at 900°C.

Several runs in the HCl system were made to determine whether or not Ge and GaAs could be grown onto doped ZnSe by interchanging source and seed. Here the dopant would be incorporated in the ZnSe before growth and would remain during and after growth because growth temperatures are far below dopant outdiffusion temperatures. This would eliminate the problem of ZnSe doping after growth for only a simple zinc vapor diffusion step would render the ZnSe conducting. Chlorox polished single crystal (110) ZnSe was used along with p-type GaAs or Ge source material. Source temperatures varied from 570°C to 740°C while seed temperatures ranged from 460°C to 625°C. HCl concentrations varied from .04% to .2%. Source to seed temperature difference was kept at its maximum of 125°C to 130°C to allow for the maximum material transport.

All attempts to grow GaAs on ZnSe failed. In all cases both ZnSe and GaAs were etched, but no material was deposited on the ZnSe, Si blocks, or growth tube near the blocks. All deposit appeared on the growth tube at least 3 inches from the blocks. GaAs was severely etched (10-50 mg.) while ZnSe weight measurements indicated etching of 1-2 microns of material. When both ZnSe and Ge were simultaneously used as seeds, the same results occurred - etching of GaAs, ZnSe, and Ge with no growth or deposit except on the growth tube 3 inches from the blocks. When the ZnSe was removed and GaAs grown only upon Ge under the same conditions, growths of 20-25 μ resulted. Thus the presence of the ZnSe and ZnSe etching is probably disturbing the chemical thermodynamics favorable to epitaxial growth.

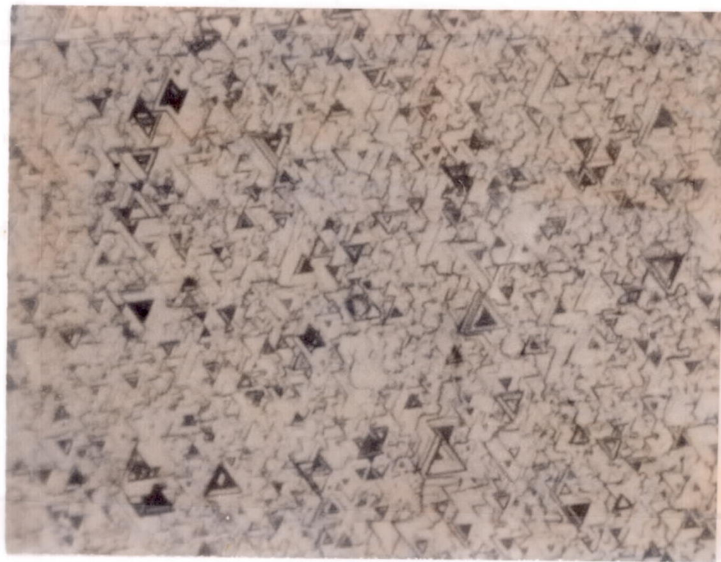
(a)



(b)

Fig. 2 Growth of ZnSe upon Ge

(a) (111) Ge 400X oblique illumination to show pyramids
(b) (100) Ge 400X normal illumination

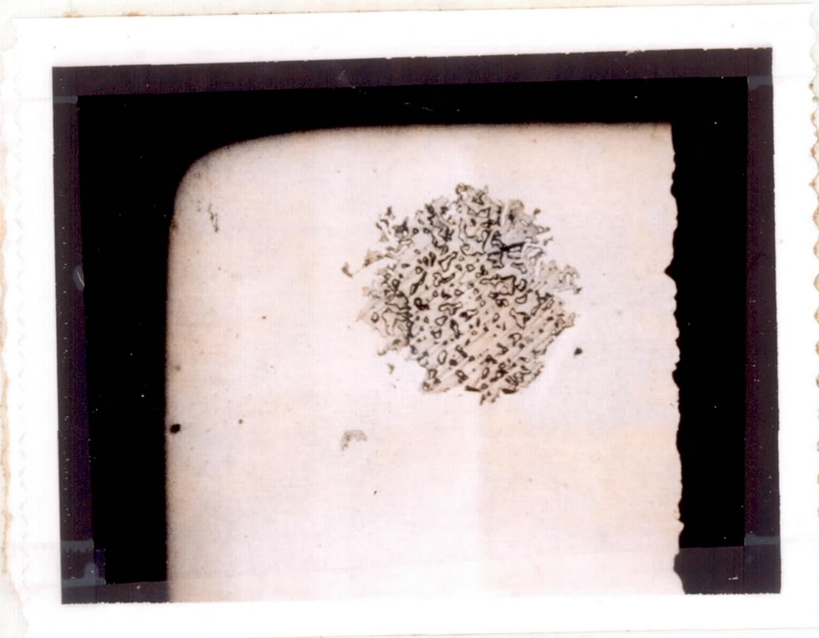


(a)

(b)

Fig. 3 Growth of ZnSe upon GaAs

(a) Ga (111) 400X normal illumination
(b) As (111) 200X oblique illumination



(a)

(b)

Fig. 4 Smooth ZnSe Surface Obtained on As (111) Face

(a) ZnSe removed to show undamaged GaAs surface
(b) Smooth ZnSe surface

Similar runs using Ge as a source yielded poor results. Again the ZnSe was etched. However a thin ($1/2\mu$) polycrystalline-looking layer of what appeared to be Ge was deposited on the ZnSe. There was no epitaxy, and the layer was easily scraped off. Because of these negative results more work in this line has been postponed, or abandoned in favor of ZnSe growth upon GaAs and attempting to develop a better method of doping grown ZnSe layers.

6. HIGH FREQUENCY TRANSISTOR MEASUREMENTS

The measuring circuit as described in the previous report was put together after checking the individual components for operation and a low VSWR. The whole system was checked by measuring the scattering parameters of some commercial transistors and comparing them with the data given on, or calculated from, the data sheets.

Original measurements were made using a strip line jig as the transistor fixture. Poor agreement was obtained between our measurements and those reported on the data sheet. The emitter could not be well grounded in that jig resulting in poor values of S_{11} and S_{22} as shown in Table 3. At the end of this report period a new coaxial transistor fixture ordered from Hewlett & Packard was finally received and the measurements were repeated using that fixture. Results in much better agreement with the reported data were obtained. A summary of the data obtained using both the stripline and new coaxial fixture is shown in Table 3.

For the 2N918 a lot of calculations were involved to convert the Y parameters on the data sheet to S parameters for comparison. For the TIXM101 the S parameters given on the data sheet are those of the improved version of the transistor. Even so, the agreement between the measured and known scattering parameters with the use of the new jig is quite good. The improvement made by the new jig is more clearly seen in the values of S_{11} and S_{22}. The problem of grounding the emitter seems to have disappeared. S parameters of heterojunction transistors are currently being measured.

TABLE 3 S Parameter Measurements on Commercial Transistors

S parameters of epitaxial NPN transistor 2N918 at I_c=5ma V_{ce}=10 volts

	Data Sheet*	Stripline Fixture	New Coaxial Fixture
Measuring frequency 100 MHz			
S_{12}	.05 < 74°	.03 < 74°	.04 < 74°
S_{21}	5.3 < 117°	5.8 < 112°	5.5 < 114°
S_{11}	.49 < -37.8°	.58 < -32°	.52 < -35°
S_{22}	.80 < -15°	.95 < 2°	.85 < -12°
Measuring frequency 400 MHz			
S_{12}	.12 < 67.8°	.1 < 82°	.1 < 80°
S_{21}	2.22 < 75.6°	1.9 < 83°	1.9 < 78°
S_{11}	.22 < -92.5°	.21 < -53°	.22 < -85°
S_{22}	.70 < -24.7°	.70 < 26°	.7 < -15°

S parameters of PNP epitaxial planar Ge transistor TIXM101 at V_{ce} = -5V I_c = -3ma

	Data Sheet**	Stripline Fixture	New Coaxial Fixture
Measuring frequency 100 MHz			
S_{12}	.05 < 75°	.059 < 74°	.055 < 75°
S_{21}	6.8 < 148°	7.0 < 142°	7.0 < 145°
S_{11}	.79 < -35°	.80 < -10°	.80 < -26°
S_{22}	.86 < -18°	.9 < -6°	.88 < -15°

* The S parameters were not given directly on the data sheet but were calculated from the y parameters.

** The S parameters are given for the improved version of TIXM101 (i.e. 2N5063) in the data sheet.

7. LOW TEMPERATURE GROWTH OF Ge ON ZnSe

7.1 Solution Growth

Epitaxial growth of Ge on ZnSe substrates using Zn solvent system was continued and improved upon. A new sapphire boat was tried to reduce the contamination problems from the graphite boat being used. During the run no surface film was seen on the solution and the Ge growth looked much cleaner. However, the growth had features similar to those obtained using the graphite boat, namely, scattered growth of Ge crystallites (approximately 50 x 50 x 30 mils size) over the ZnSe seed surface. Moreover, similar looking Ge crystallites also grew on the sapphire boat walls and adhered so well that they had to be etched in white-etch. The Zn-solution, after solidification also adhered to the boat and had to be etched away. These features discouraged the use of the sapphire boat. It developed a crack after a few more runs and its use was discontinued.

A new method was devised to outgas the graphite boat before each growth run. After this heat treatment of the boat no oxide layer was seen over the solution during the growth run. A new seed holding arrangement was also designed to allow easy pour-off of the solution from the seed. This reduces the time required to etch away the excess Zn from the seed for observing the growth structure.

A study of the effect of different operating conditions on growth structure revealed that a slow cooling rate ($\sim$1°C/min) encourages growth to start at few preferred sites and then the growth continues at those sites only, resulting in rather thick growth at few sites. However, if the growth is initiated by a fast cooling rate ($\sim$6°C/min) the growth structure tends to be planar, but the growth was usually thin, patchy and with very poor adhesion to the surface. The latter problems were thought to be because of some oxide film on ZnSe seeds after the cleaning process. The ZnSe surface preparation process was therefore reviewed and a new process established which seemed to leave the ZnSe surface freer of any oxide film. This process involves final etching in a potassium permanganate - sulfuric acid etch and rinsing with warm KCN solution. However, final exposure to air can result in oxide layer thickness of the order of 20 Å.

When ZnSe substrates were prepared using this new surface preparation process and growth process started by a fast cooling rate, the resulting growth was still patchy but this time it had quite good adherance at several places. This result indicates that the chemical cleaning process above is not sufficient.

In order to improve the substrate surface, some method which cleans the surface just before the epitaxial deposition is desirable. A study was therefore made of the use of a zinc solution as an etchant for ZnSe seed. At the growth temperatures (500-550°C), the solubility of ZnSe in Zn is negligible. However the vapor pressure of Zn is high enough that zinc evaporates from the boat and deposits at colder regions of the growth tube. This changes the composition of the zinc-Ge solution and therefore the ZnSe seed should be held in contact with the solution for as small a period as is sufficient for the purpose. Initial experiments indicate that a period of 45 minutes at about 550°C may be needed to get rid of the surface film. This treatment gave a planar growth over the surface of the seed exposed to the solution, but the growth was very thin ($\sim 1\mu$) and shows no features to indicate its crystallinity. It has good adherance to the seed. Attempts will now be made to get thicker growths.

7.2 Vacuum Evaporation System

Work in this area was started to have an alternative approach to obtain epitaxial growth of Ge on ZnSe. It has been reported that single-crystal Ge layers can be obtained on GaAs seeds in ultra high vacuum systems at seed temperatures as low as 320°C. The reason why the minimum seed temperature for single crystal growth of Ge on Ge seeds is normally greater than 600°C in 10^{-6} mm vacuum systems is thought to be the result of an oxide layer (GeO_2) which inhibits proper nucleation at lower substrate temperatures. Our experience with ZnSe seems to indicate that this material also may have a very thin oxide layer (ZnO) covering the surface which must be reduced before depositing the Ge layer.

An ultra-high vacuum system equipped with an ion pump and electron-beam Titanium sublimator will be used. Various components to go into the system are being fabricated and assembled. A vitreous carbon crucible will be used for heating the source Ge. Tungsten coils have been wound to act as heater element for the crucible. Substrate heating will be by a molybdenum ribbon heater coil wound around a one inch diameter quartz tube. This tube has arrangements for holding the substrate and thermocouples. It can also be modified to incorporate a fine tungsten wire near the substrate which can be heated to produce atomic hydrogen in the vicinity of the substrate to reduce the surface oxide layer. This system will be in operation soon.

8. LOW TEMPERATURE GROWTH OF Ge on GaAs

The basic iodide disproportionation system described in the previous report was improved during this period and a dopant system added. The first few growths in the basic system indicated some deficiencies which required minor changes in the system. Introduction of quartz wool plugs into the exhaust tubing prevented troublesome transport of reaction products beyond that part of the system which is cleaned between runs. Extension of the HI converter winding toward the iodine column now prevents iodine from depositing in the tube between the column and converter. Early operation of the system showed that it is important to provide a bleed for the iodine column during warm-up. This prevents an initial surge of hydrogen iodide down the growth tube due to a sudden pressure release from the column when the exit valve is opened fully. Without bleeding, rapid growth takes place during the initial few minutes and causes low quality interface material.

After these problems were realized and corrected, a purging run was made to clear free iodine from parts of the system and to clean the surface of the germanium source material. An initial series of undoped growth runs posed a paradox: n-type seeds grew n-type layers and p-type seeds grew p-type layers. It had been shown previously in this lab and by others that good undoped single crystal layers always grow n-type. The cause of the difficulty

was finally traced to improper substrate preparation of the p-type, but not the n-type, seeds. A confirming run was made with four seeds: one adequately polished and one improperly prepared seed of both n-and p-types. As expected, the well polished seeds grew n-type layers while the poorly prepared seeds grew p-type without regard for substrate type.

A total of 8 seeds from all runs to this point were prepared into Van der Pauw samples for resistivity and mobility measurements, and samples for Laue back reflection X-rays studies. The Laue patterns indicated all growths to be single crystal with proper spot orientation and no apparent smear for the W target shots and no visible rings in the Cu target shots.

Work was done to complete the dopant metering and introduction system. An analysis was made of all possible column IIIA and VA dopants in their tri-iodide form, particularly the p-type dopants since arsine had already been chosen as the most convenient n-type dopant. Consideration of temperature dependence of vapor pressure, melting point, water vapor absorption, decomposition (due to light and heat), purity of available supplies, and time to delivery led to the choice of BI_3. Evidence of accomplished doping exists for this material in the literature.[11].

A quartz end fitting which includes the dopant introduction tip was made by the glassblower and some final shaping of the tip was done in the lab. While the system was down and apart, many other replacements and recleanings were made. These included: a new thermocouple gauge tube and a large cold trap installed in the vacuum line; a new growth tube thermocouple installed; a second quartz growth tube liner fashioned; the iodine column filler tube permanently sealed with a glass plug; the entire vacuum and exhaust lines, valves, and fittings cleaned and reinstalled with worn fittings replaced. Source germanium and growth tube were then cleaned and the entire system assembled and leak checked. As a result of this extensive maintenance and replacement, the system is now extremely leak tight.

A run has been made to purge the iodine column and bring the surface of the source germanium to conditions for growth. An undoped control run has been made with a GaAs seed with all doping fittings in place. Runs are now being made to establish doping level control for both n-type and p-type germanium layers on GaAs.

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