MODIFICATION OF THE DIGITAL COMPUTER PROGRAM DLANET TO INCLUDE THE EFFECTS OF DIFFERENTIAL-INPUT VOLTAGE-CONTROLLED VOLTAGE SOURCES

Prepared under Grant NGL-03-002-136 for the
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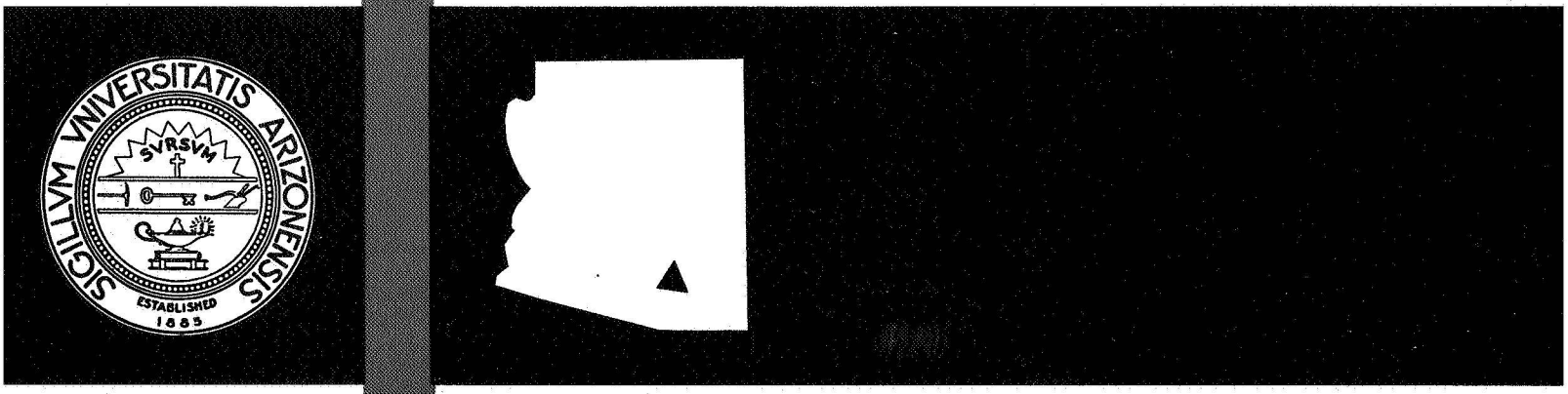

ENGINEERING EXPERIMENT STATION
COLLEGE OF ENGINEERING
THE UNIVERSITY OF ARIZONA
TUCSON, ARIZONA

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M.L. Gentry
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Department of Electrical Engineering
University of Arizona
Tucson, Arizona

ABSTRACT: This report describes a modification of DLANET[1], a digital computer program for the analysis of distributed-lumped-active networks. The modification extends DLANET's capability to include active elements which are differential-input voltage-controlled voltage sources of finite gain.

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I. Introduction

This is one of a series of reports describing the use of digital computational techniques in the analysis and synthesis of DLA (Distributed-Lumped-Active) networks. This class of networks consists of three distinct classes of elements, namely, distributed elements (modeled by partial differential equations), lumped elements (modeled by algebraic relations and ordinary differential equations), and active elements (modeled by algebraic relations). Such a characterization is applicable to a broad class of circuits, especially including those usually referred to as linear integrated circuits, since the fabrication techniques for such circuits readily produce elements which may be modeled as distributed and active, as well as ones which may be considered as lumped. In a previous report[1] the use of a digital computer program DLANET (for Distributed-Lumped-Active NETwork analysis) was described which had the capability of providing a sinusoidal steady-state analysis of a broad class of DLA networks over a prescribed frequency range, and displaying the results in tabular and plotted form. DLANET's original capability included active circuit elements which were single-input voltage-controlled finite-gain voltage sources, herein referred to as VCVS's. Figure 1 illustrates the schematic and circuit model for such a VCVS. This paper describes a modification of DLANET which extends its capability to also include active elements which are differential-input voltage-controlled finite-gain voltage sources, herein referred to as DI/VCVS's. Figure 2

illustrates the schematic and circuit model for a DI/VCVS. A DI/VCVS may be referred to as a finite-gain differential amplifier, and may be used to implement many interesting DLA network configurations.

DLANET employs matrix methods in its analysis of a DLA network. A network's admittance matrix is formed and then constrained by a subroutine of DLANET, called CONST, in such a way as to include the effects of the VCVS active elements using well-known techniques.[2] The modification of the techniques for DI/VCVSs is discussed in the following section.

II. Theory of Constraint Operations

For a general n-terminal network, Kirchhoff's Current Law yields n independent equations described in matrix notation as:

$$\begin{bmatrix} I_1 \\ I_2 \\ \cdot \\ \cdot \\ \cdot \\ I_n \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} & \cdots & y_{1n} \\ y_{21} & y_{22} & \cdots & y_{2n} \\ \cdot & \cdot & \cdots & \cdot \\ \cdot & \cdot & \cdots & \cdot \\ \cdot & \cdot & \cdots & \cdot \\ y_{n1} & y_{n2} & \cdots & y_{nn} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ \cdot \\ \cdot \\ \cdot \\ V_n \end{bmatrix} \qquad (1)$$

The square matrix is called the admittance matrix.

Suppose a DI/VCVS of gain K is connected such that nodes i (+) and j (-) are the controlling voltages and the output is connected to node n. The situation is shown in Fig. 3. The effect of each active element is to reduce the rank of the admittance matrix by one. Because node n is connected to an ideal voltage source, the current variable

at node n is no longer an independent variable. Thus, row n may be deleted from the Y-matrix and the current variable I_n may be deleted from the current vector. Also, one voltage variable is now dependent, say V_n. If $(KV_i - KV_j)$ is substituted for V_n in (1), the following equations result:

$$\begin{bmatrix} I_1 \\ \vdots \\ I_i \\ \vdots \\ I_j \\ \vdots \\ I_{n-1} \end{bmatrix} = \begin{bmatrix} Y_{11} & \cdots & y_{1i}+Ky_{1n} & \cdots & y_{1j}-Ky_{1n} & \cdots & y_{1,n-1} \\ \vdots & & \vdots & & \vdots & & \vdots \\ y_{i1} & \cdots & y_{ii}+Ky_{in} & \cdots & y_{ij}-Ky_{in} & \cdots & y_{i,n-1} \\ \vdots & & \vdots & & \vdots & & \vdots \\ y_{j1} & \cdots & y_{ji}+Ky_{jn} & \cdots & y_{jj}-Ky_{jn} & \cdots & y_{j,n-1} \\ \vdots & & \vdots & & \vdots & & \vdots \\ y_{n-1,1} & \cdots & y_{n-1,i}+Ky_{n-1,n} & \cdots & y_{n-1,i}-Ky_{n-1,n} & \cdots & y_{n-1,n-1} \end{bmatrix} \begin{bmatrix} V_1 \\ \vdots \\ V_i \\ \vdots \\ V_j \\ \vdots \\ V_{n-1} \end{bmatrix} \quad (2)$$

Thus, the Y-matrix is reduced by one row and one column. Notice that either column i or j could have been eliminated instead of column n with the appropriate column manipulation. There are, then, three cases which can arise depending upon which node or Y-matrix column is to be eliminated.

CASE 1: Eliminate the output node n.

The constraining relation is: $V_n = KV_i - KV_j$. This requires the elements of column n of the Y-matrix to be multiplied by K and then added and subtracted respectively to the elements of columns i and j. Note

that the operation of adding K times column n to column i is exactly the operation required for a VCVS connected from node i to node n where again node n is to be eliminated. The logic for this operation was already programmed into the subroutine CONST in the original DLANET.

CASE 2: Eliminate the positive input reference node i.

The constraining relation can be written: $V_i=V_n/K+V_j$. This requires column i to be added to column j and also divided by the source gain and added to column n. Again, the divide by K and add to column n operation is also required for a VCVS from node i to node n in which node i was to be eliminated. This operation was also already available in CONST.

CASE 3: Eliminate the negative input reference node j.

The constraining relation can be written: $V_j=V_i-V_n/K$. This requires column j to be added to column i and column j divided by the source gain to be subtracted from column n. Neither of these operations was previously required in CONST.

The modifications necessary to permit the subroutine CONST to handle the three cases listed above are described in the following section.

III. Modifications of the Subroutine CONST

Fortunately, DLANET's input data format included provision for two additional node variables for each VCVS. One of these (NG2) is employed as the negative-input node for DI/VCVS's. This read in I3 format in columns 4-6 of Card No. 3 in the Input Data Format section of the report describing DLANET.[1] The correspondence of nodes and

node variables is as shown in Figs. 1 and 2. The subroutine CONST tests the value of NG2 to differentiate between VCVS's and DI/VCVS's (NG2 = 0 implies a VCVS, NG2 ≠ 0 implies a DI/VCVS). Thus, the data input to DLANET is unchanged with the exception that NG2 may be set equal to a node number indicating that a DI/VCVS, negative reference input terminal is connected to that node.

The portion of CONST which eliminated rows and columns from the admittance matrix did not need to be altered. The rows eliminated correspond with the nodes at which the source portion of the VCVS's or DI/VCVS's is connected. The columns that are eliminated are those associated with either the controlling node voltage(s) or the node at which the source is located. Note that the flexibility of eliminating any node associated with a given active element is maintained.

The portion of CONST that required modification was the section that performs the column addition operations. For a VCVS, the constraining operation is to add the column to be eliminated to the column which is not eliminated after first multiplying or dividing its elements by the gain of the source. For a DI/VCVS, the three cases as outlined in the previous section were implemented. Fig. 4 shows the flow chart for the section of CONST which was modified. The portion within the dotted rectangle is additional or new logic. A listing of the entire modified subroutine CONST is given in the Appendix. It should be noted that a DI/VCVS cannot be simulated by using a combination of VCVS's. This is because a DI/VCVS requires

two column constraining operations per node and column elimination whereas a VCVS requires only one column constraining operation per node and column elimination.

Some cautions must be observed with regard to input data. The data for the active elements in a network must not specify that a given node or column be eliminated more than once. In addition, the order in which the data for the sources is read into the program must be such that no operations are made on a column <u>after</u> it has been eliminated. For example, consider the cascade of sources shown in Fig. 5. For this connection, examples of permissible input data are:*

<u>Example 1</u>

```
c     a     a     GAINA.
d     b     b     GAINB.
e  d  c     c     GAINC.
```

Here, nodes a, b, and c are eliminated.

<u>Example 2</u>

```
e  d  c     e     GAINC.
c     a     c     GAINA.
d     b     d     GAINB.
```

Here, nodes e, c, and d are eliminated.

<u>Example 3</u>

```
d     b     b     GAINB.
e  d  c     e     GAINC.
c     a     c     GAINA.
```

Here, nodes b, c, and e are eliminated.

---

*The five columns shown read the variables NG1(I), NG2(I), NG3(I), JL(I), GA(I).

Examples of improper input data are:

Example 1

```
c      a      c      GAINA.
d      b      d      GAINB.
e  d   c      e      GAINC.
```

Here, operations on columns c and d are required after they have been eliminated and thus violates the rule.

Example 2

```
e  d   c      c      GAINC.
c      a      a      GAINA.
d      b      d      GAINB.
```

Here, node c is eliminated too soon.

IV. Example of Application

As an example of the application of the modified DLANET program, consider the circuit shown in Fig. 6. This circuit contains two controlled sources, a VCVS and a DI/VCVS. Nominal values of +4.0 for the DI/VCVS and 0.59 for the VCVS give a Q of approximately 40. Fig. 7 shows the circuit's response for these gain values for a restricted range of frequencies in the vicinity of the resonant peals.

V. Conclusion

The modification to the digital computer program DLANET described in this report provides a considerably broader range of circuits. This report makes it possible to apply the program to a considerably broader range of circuits. Future developments are planned to increase the capabilities of DLANET even further. These will be described in forthcoming reports.

Acknowledgement

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1. L. P. Huelsman, "DLANET - A Digital Computer Program for the Analysis of Distributed-Lumped-Active Networks," Report prepared under NASA Grant NGL-03-002-136, 46 pages, Nov. 1968.

2. A Nathan, "Matrix Analysis of Constrained Networks," Institution of Electrical Engineers, Monograph No. 399E, Sept. 1960.

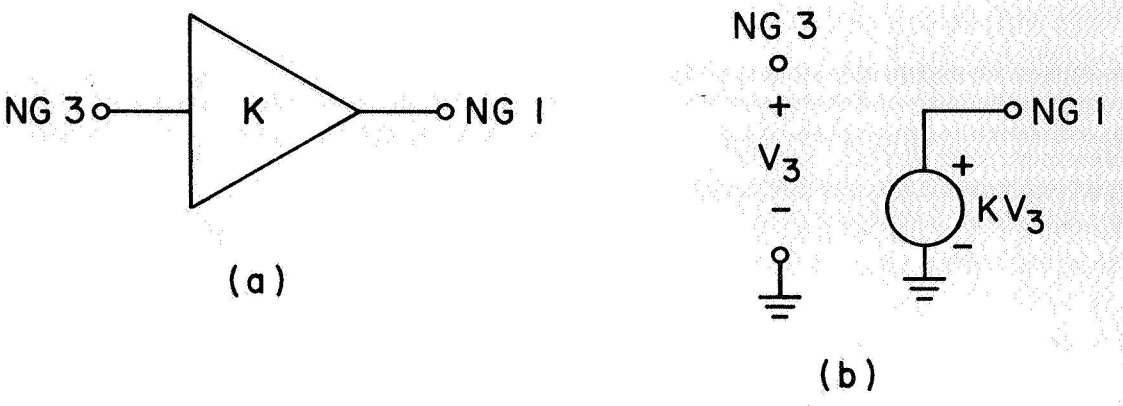


Fig. 1. Voltage-controlled voltage source: (a) schematic; (b) circuit model.

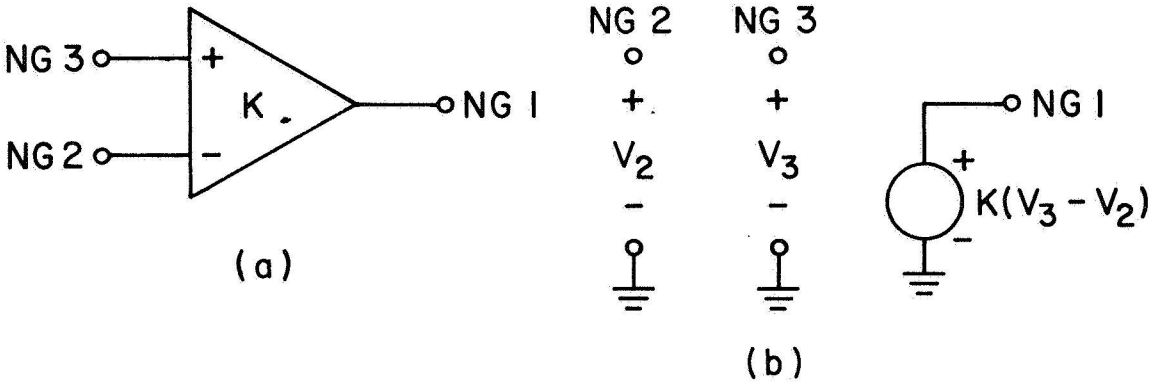


Fig. 2. Differential-input voltage-controlled voltage source: (a) schematic; (b) circuit model.

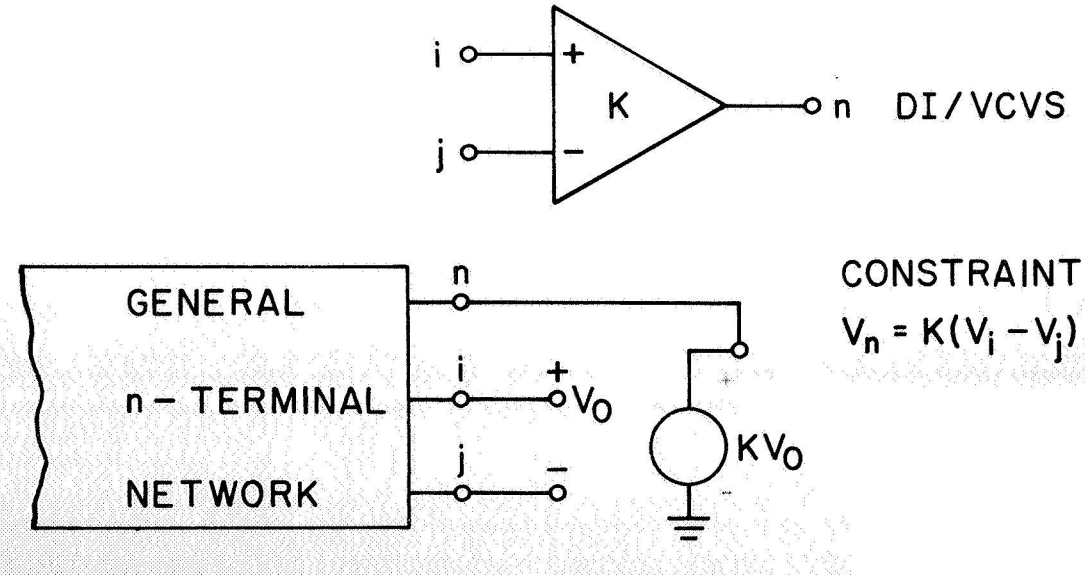
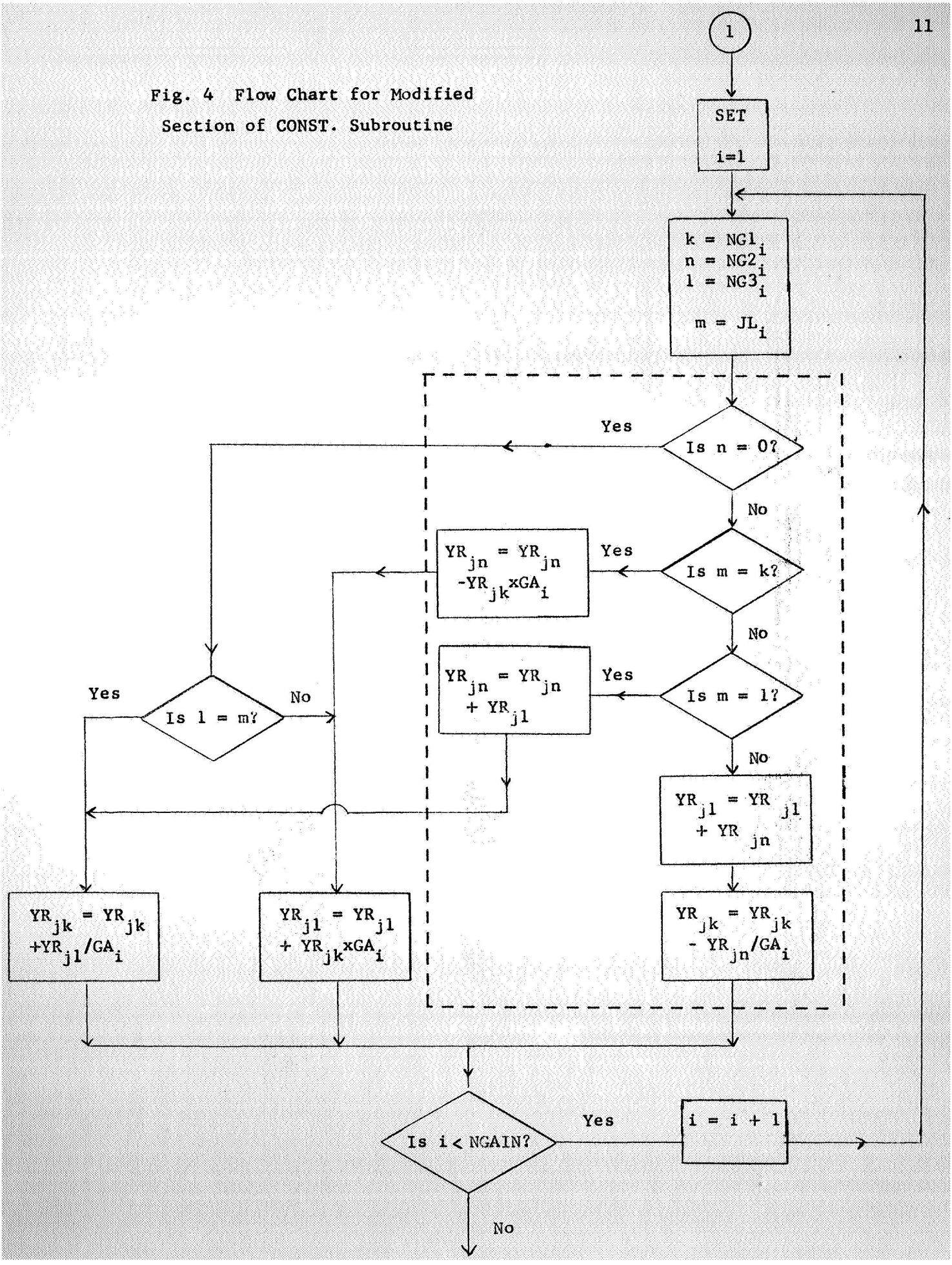


Fig. 3. Constraining an n-terminal network.

Fig. 4 Flow Chart for Modified Section of CONST. Subroutine



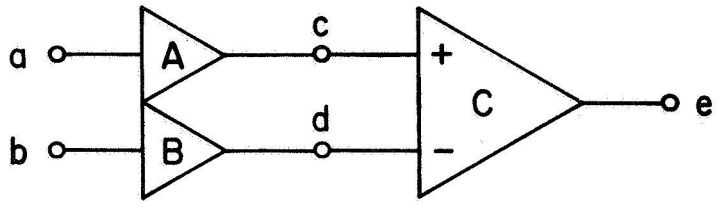


Fig. 5. An interconnection of sources.

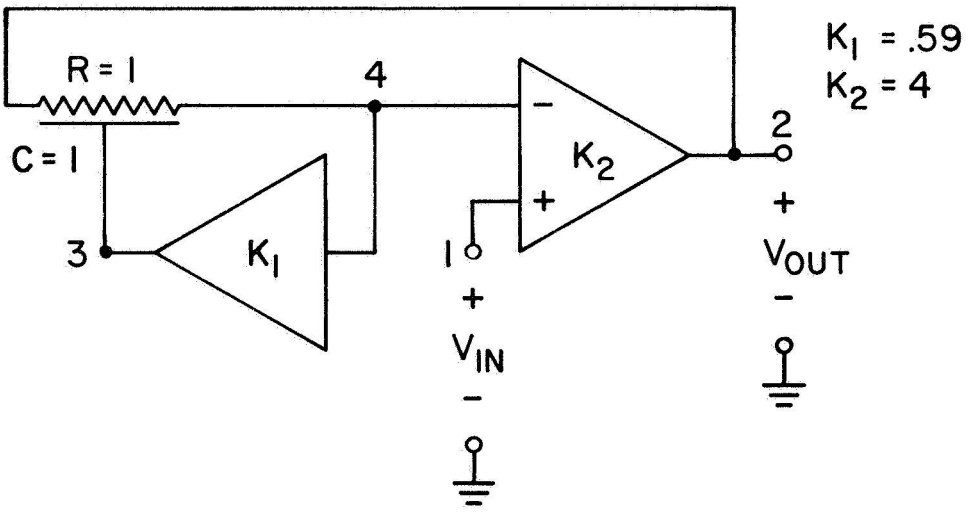


Fig. 6. A resonant circuit.

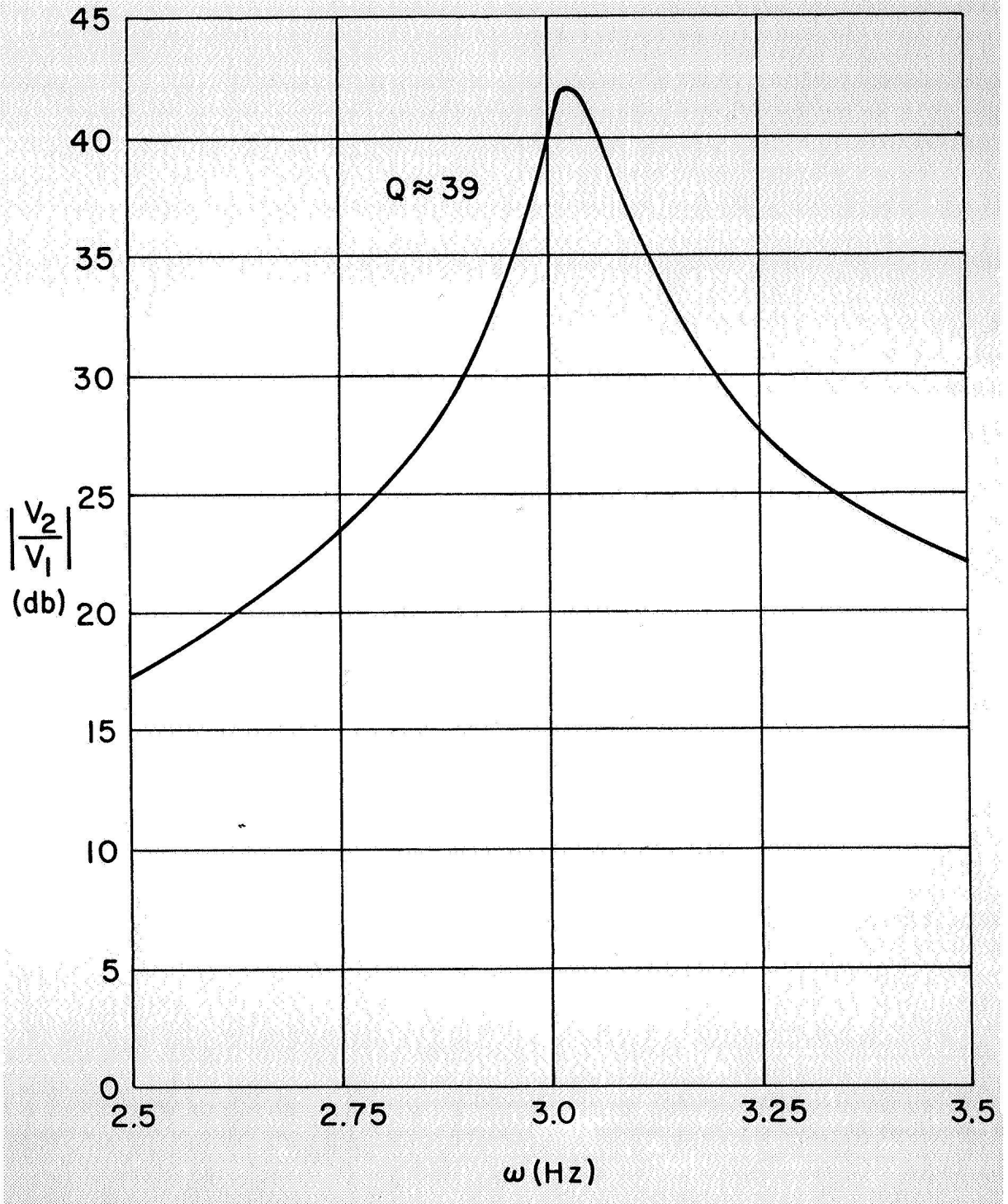


Fig. 7. Frequency response.