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FOURTH INTERIM PROGRESS REPORT

ON

THE STUDY OF INFRARED EVALUATION

IN

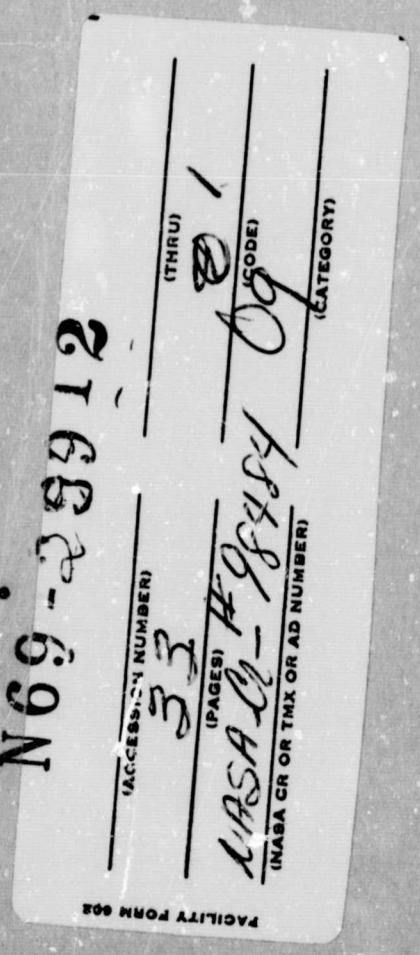
QUALIFICATION AND FAILURE ANALYSIS

OF

SEMICONDUCTOR DEVICES

covering the period

28 April 1968 to 28 July 1968



Prepared for

GEORGE C. MARSHALL SPACE FLIGHT CENTER
HUNTSVILLE, ALABAMA

Under

CONTRACT NAS8-21219

by

W. M. Berger and R. H. Soltau

PHILCO-FORD CORPORATION
Microelectronics Division
Blue Bell, Pennsylvania • 19422

SQT-55811

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L I S T O F I L L U S T R A T I O N S (cont'd)

Section I - INTRODUCTION

1.1 SCOPE OF REPORT

This report describes the work performed during the period 28 April through 28 July 1968 on the program, "The Study of Infrared Evaluation in Qualification and Failure Analysis of Semiconductor Devices." This program is being conducted for the George C. Marshall Space Flight Center under Contract NAS8-21219.

1.2 PROGRAM OBJECTIVES

The main objectives of the program are:

a. The development of valid infrared techniques and acceptance criteria for use in the qualification of microcircuits.

b. The establishment of detail procedures by which infrared analysis and evaluation techniques may be used to perform the failure analysis of semiconductor devices.

1.3 SUMMARY OF WORK PERFORMED

During this reporting period the major effort was directed toward:

a. The study of localized heating at scratches in interconnecting metalization patterns.

b. The evaluation of heating patterns exhibited by electrically good and electrically defective microcircuit devices of identical construction.

c. The evaluation of localized heating at vias in bilayer metalized devices.

d. The initiation of a study of heating and cooling rates of discrete diffused components to optimize the conditions necessary to generate most significant infrared information.

Other work performed during this reporting period was, assistance to Raytheon personnel during the attempted modification of the Fast Scan Infrared Microscope and some preliminary evaluation of flip chip devices.

SECTION II - FACTUAL DATA

2.0 GENERAL

A detailed description of the work performed during this reporting period and the significant data derived as a result of this work is contained in the subsequent paragraphs of this section.

2.1 LOCALIZED HEATING AT METALIZATION SCRATCHES

Scratches in the aluminum interconnecting metalization patterns on integrated circuits represent a severe reliability hazard when they cause a constriction in the metalization pattern that results in a sufficient increase in the current density to initiate mass migration of the aluminum. The rate of mass migration of aluminum is a function of current density, operating temperature, and the temperature gradient along the conductor stripe.

Preliminary investigations, detailed in the Third Interim Progress Report, did not show any indication of localized heating at purposely induced metalization scratches when the current density in the scratch area was of the order of 1×10^5 Amps/cm^2.

Additional investigations performed, during this reporting period, did show that localized heating occurred in the scratch area when the current density in the constriction approached 2×10^6 Amps/cm^2. The five devices in which this heating was observed were then subjected to a 125°C operational life test. The life test circuit was arranged so that current density in the scratch area was about 4×10^6 Amps/cm^2. All five devices failed prior to electrical measurements after 100 hours of test because of open metalization at the scratch location in the stripe.

2.2 COLOR MODULATED INFRARED DISPLAYS OF ELECTRICALLY GOOD AND ELECTRICALLY DEFECTIVE BILAYER METALIZED DTL DEVICES

During this reporting period color modulated infrared threshold displays of the infrared characteristics of four electrically good and ten electrically defective devices were generated. The devices used in this evaluation were silicon planar epitaxial DTL triple three input gates fabricated with bilayer metalization patterns. A photomicrograph of the device is shown in figure 1.

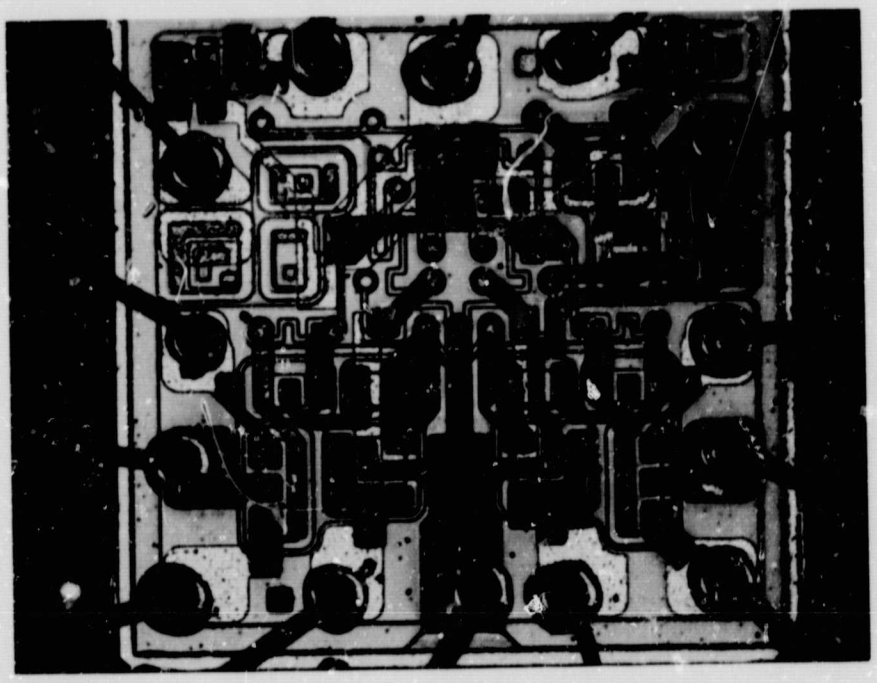


Figure 1- Photomicrograph of Bi-layer DTL three input gate.

The infrared displays were obtained by scanning the devices during the time they were operating under identical voltage conditions. The electrical test circuit is shown in figure 2.

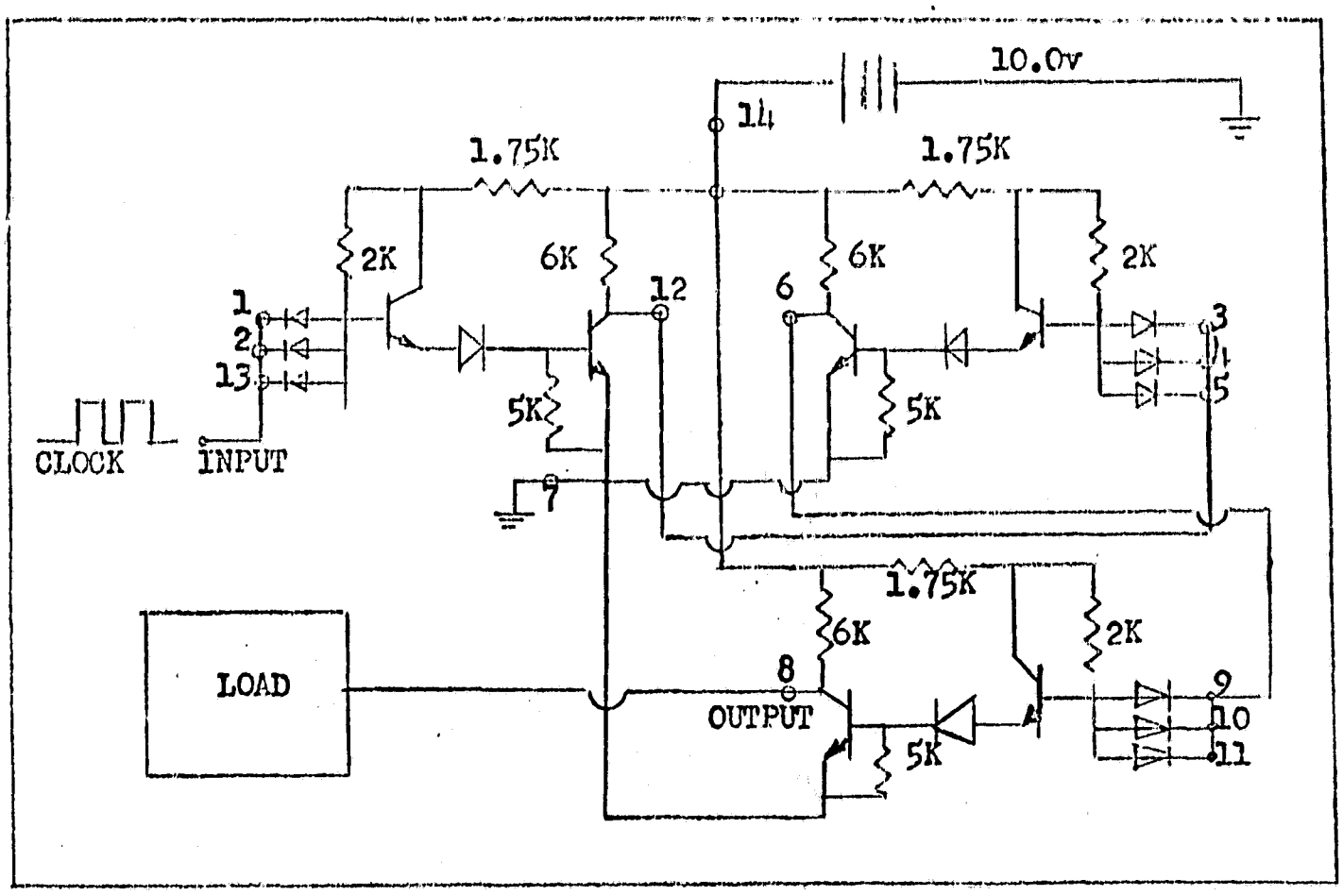


FIGURE 2.Bilayer Triple Three Input Gate Test Circuit.

All of the defective devices were subjected to a physical analysis to determine the failure mode, and to a circuit analysis to determine how the failure mode associated with each defect should effect the infrared characteristics of those devices when compared to infrared characteristics of an electrically good device. Because the infrared data was collected with each device operating under identical impressed voltages there were differences in total chip dissipations since the normal variation in resistor values and the effect of the defects caused different currents to flow in each device. The high dissipation devices (high current level) operated at slightly higher temperatures than the low dissipation devices. Therefore it was necessary to compare heating patterns in addition to the actual operating temperatures of these devices to

evaluate the data. The infrared characteristics of five of the ten defective devices were significantly different from the characteristics of the good devices. The devices with significantly different characteristics were those devices that were located at the extremes of the current level distribution (See table 1). Figure 3 in a display of device #20 (low current), figure 4 is of device #216 (good device) and figure 5 is of device #12 - (high current). The remaining 5 defective devices were devices that were located near the center of the current level distribution and exhibited only subtle difference in infrared characteristics from the good devices. Figure 6 is a color modulated infrared display of such a device. These subtle differences in infrared characteristics appear to be slightly higher temperature regions in or near areas that dissipated more than normal power because of the device defect, but further evaluation is required to substantiate this result. The good electrical devices exhibited slightly different operating temperatures, but the heating patterns were consistent. These devices had a relatively tight current level distribution and were located near the median of the total distribution. The analysis of this data is summarized in table 1.

T A B L E I

DEVICE No.	Vcc VOLTS	CURRENT mA	FAILURE MODE	INFRARED CHARACTERISTICS
20	10	10.0	Open Metal Common Cathode Gate 3	Significantly different from good device Chip runs relatively cool.
14	10	12.6	Shorted C-E Output Transistor Gate 2	Significantly different from good device Chip runs relatively cool
17	10	12.7	Resistive shunt C-E Output transistor Gate 2	Subtly different from good device differences may be related to device defect.
11	10	13.2	Open Emitter Output transistor Gate 2	Subtly different from good device differences may be related to device defect.
218	10	13.9	Good Device	Consistent heating pattern
219	10	13.9	Good Device	Consistent heating pattern
216	10	14.2	Good Device	Consistent heating pattern
419	10	14.6	Good Device	Consistent heating pattern
19	10	14.8	Shorted C-E Output transistor Gate 3	Subtly different from good device difference may be related to device defect.
16	10	15.1	Shorted C-E Output transistor Gate 3	Subtly different from good device differences may be related to device defect
13	10	15.2	Resistive shunt Output transistor Gate 3	Subtly different from good device differences may be related to device defect.
15	10	15.3	Resistive shunt C-E Output transistor Gate 3	Significantly different from good device chip runs relatively hot
18	10	15.6	Resistive shunt C-E Output transistor Gate 3	Significantly different from good device chip runs relatively hot
12	10	16.5	Output of Gate 1 Shorted to input diodes.	Significantly different from good device Chip runs relatively hot

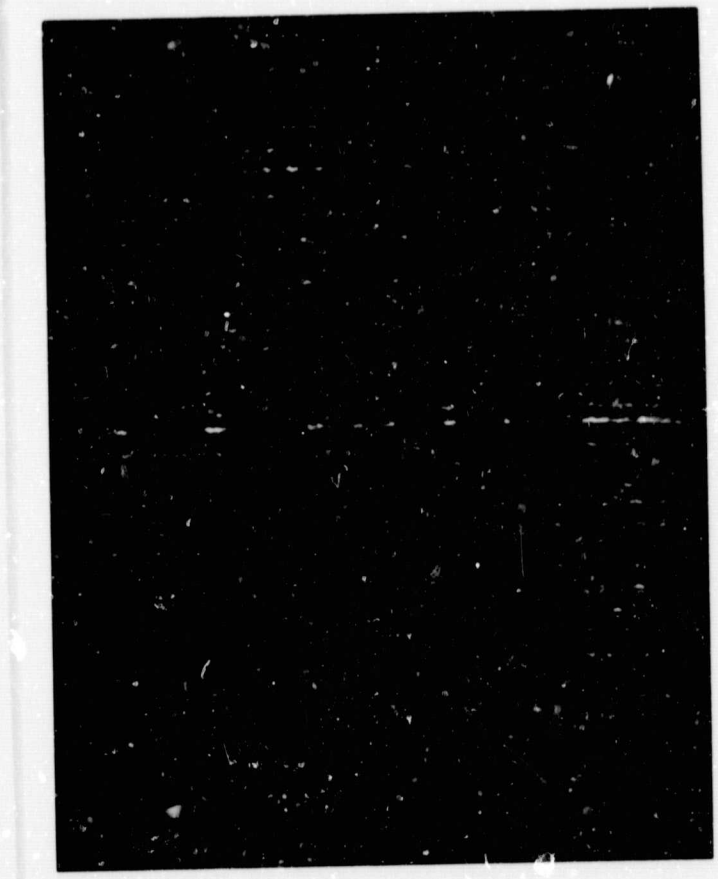


Figure 3-Color modulated infrared display of defective Bi-layer device showing a significant difference from good devices.

Figure 4-Color modulated infrared display of good Bi-layer devices.

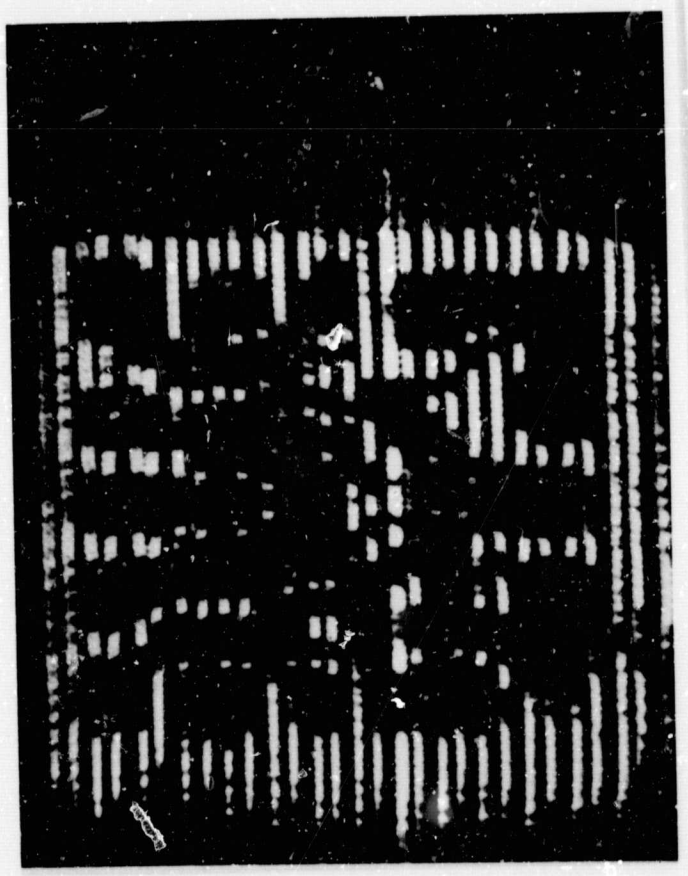


Figure 5- Color modulated infrared display of defective Bi-layer device showing significant difference from good device.

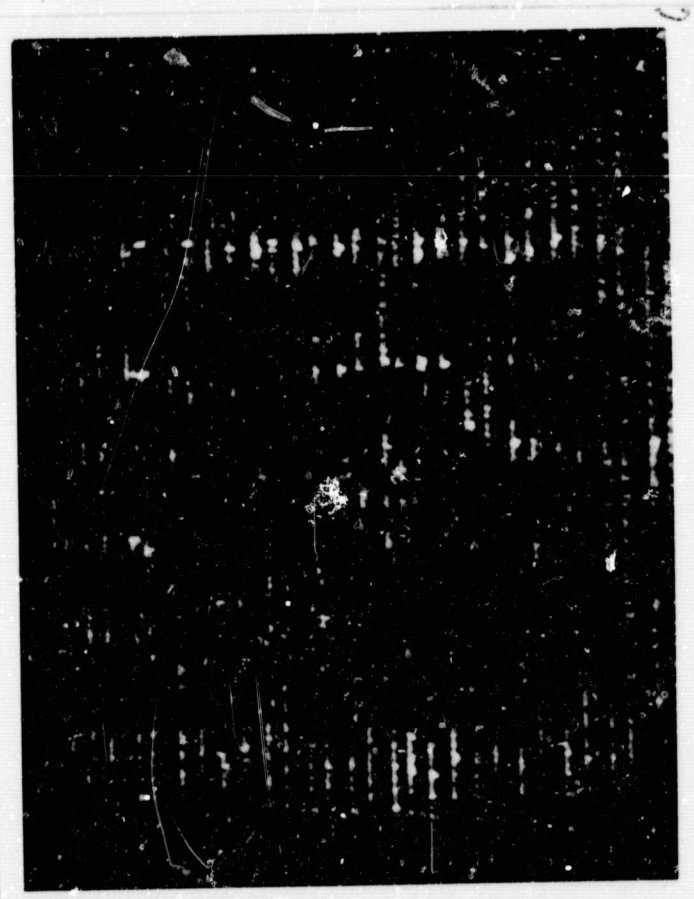


Figure 6-Color modulatedinfrared display of defective Bi-layer device showing subtle differences from good device.

Based on the analysis given in table 1, and the color modulated infrared displays of figures 3, 4, 5 and 6, to the extent that a given device process in uniform, it is possible to determine some device operational condition that will permit definite infrared differentiations of some electrically defective devices from good electrical devices. In this evaluation devices 12, 14, 15, 18, and 20 exhibited infrared characteristics sufficiently different from the electrically good devices to immediately characterize them as defective. Devices 11, 13, 16, 17 and 19 were also electrically defective, but the infrared characteristics of these devices appear to show only subtle differences from the good devices. These subtle differences however may be related to the failure mode. Further evaluation of this data is necessary to substantiate whether these differences are significant.

2.3 COLOR MODULATED INFRARED DISPLAYS OF ELECTRICALLY GOOD AND ELECTRICALLY DEFECTIVE RTL DEVICES

A total of six silicon epitaxial planar dual two input gate devices were subjected to infrared analysis. Four of these devices were electrically good and two were made defective by opening metalization patterns as indicated in figure 7.

The infrared analysis was performed by generating color modulated displays of the infrared characteristics of each device during the time it was operating in the test circuit of figure 8.

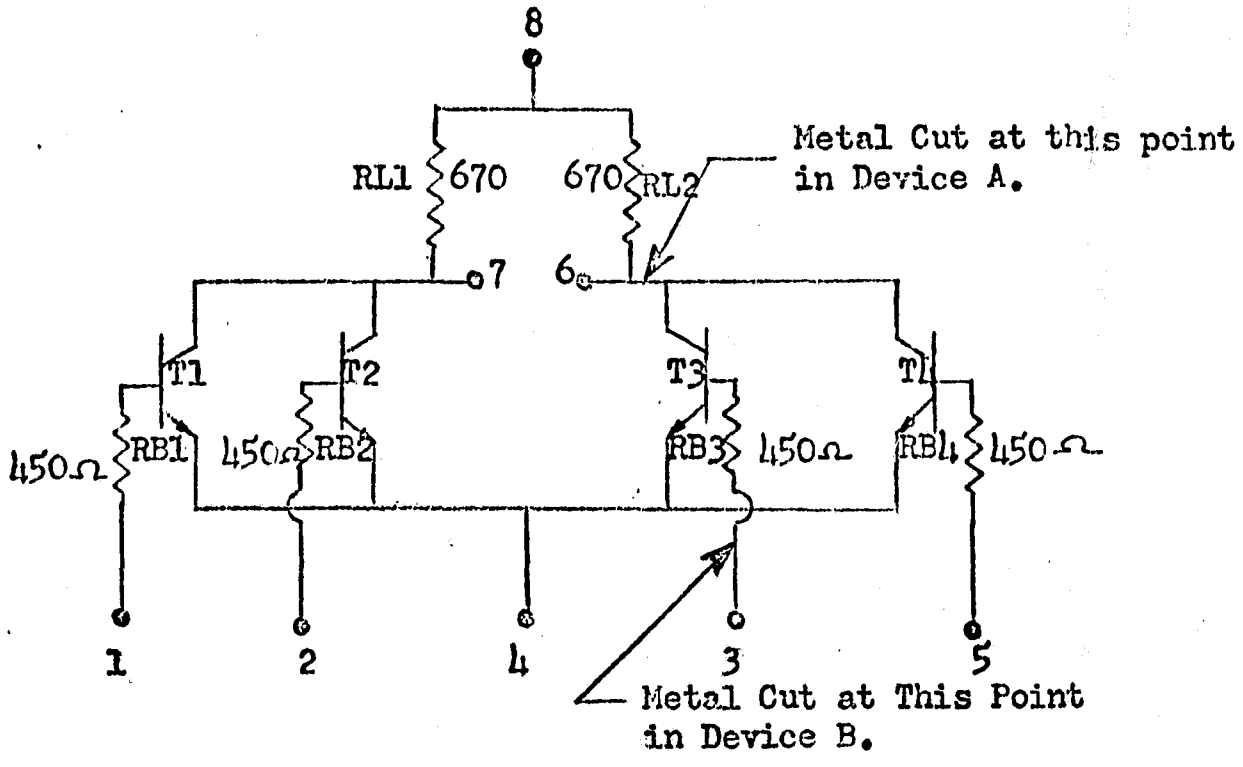


FIGURE 7. Location of induced defects in dual two input gate devices.

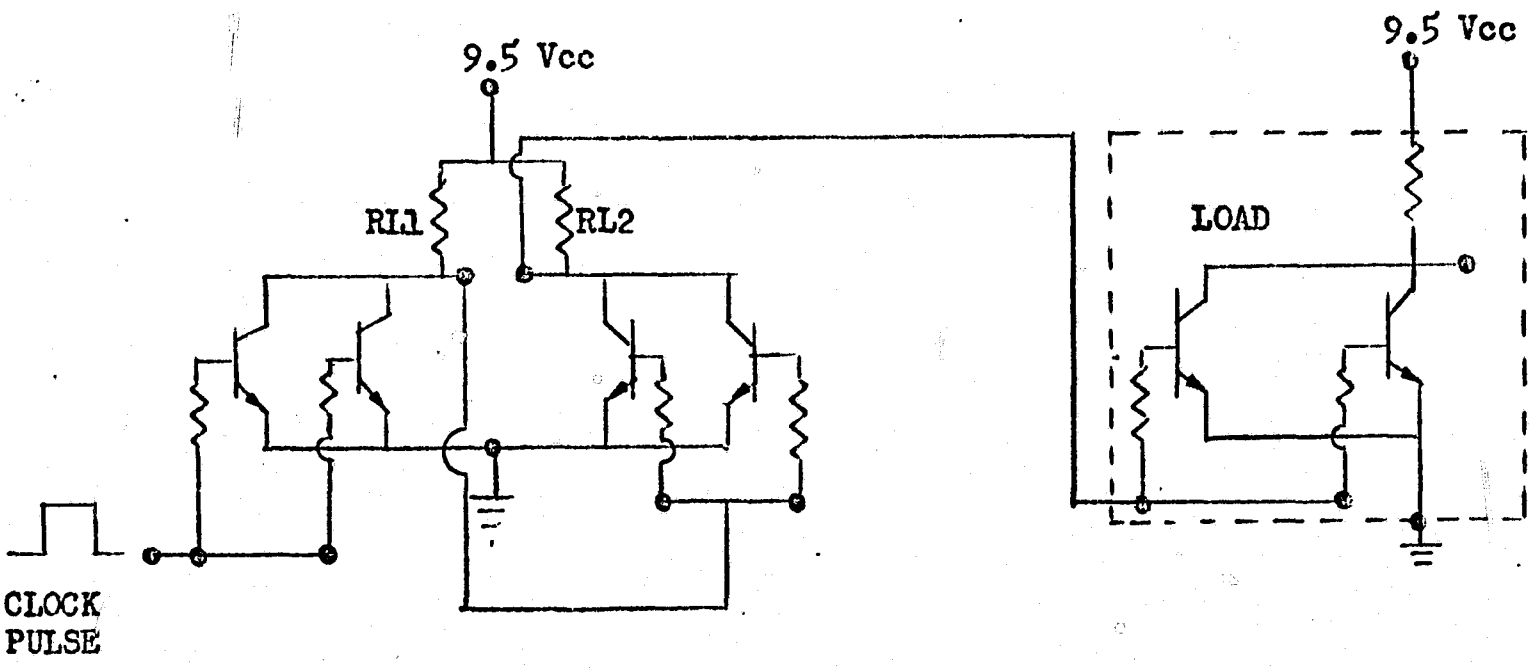


FIGURE 8. Electrical Test circuit for dual two input gate devices.

In this circuit the average dissipations in the individual components of a normal device and of the device with open collector metalization (point A of figure 7) would be:

COMPONENT	NORMAL DEVICE	DEVICE WITH DEFECT AT POINT "A"
R_{L1}	96 MW	96 MW
R_{L2}	96 MW	67 MW
R_{B1}, R_{B2}, R_{B3}, R_{B4}	2.2 MW	2.2 MW
T_1 and T_2	3.4 MW	3.4 MW
T_3 and T_4	3.4 MW	1.5 MW

In the case of the device with the open base metalization, the dissipation levels are essentially the same as the normal devices. If the infrared characteristics of the defective device (defect at point A) are to show some differences from the normal devices, it could be expected that R_{L2} would operate at a slightly lower temperature than R_{L1} because this resistor dissipates an average of 30 MW less than R_{L1}; and that the defective device chip would operate at a slightly lower temperature than a normal device because the average calculated input current into the defective device at 9.5 volts is 2.15 mA, as opposed to the average current into a normal device is 23 mA at the same voltage. Inspection of the color modulated infrared display shows that chip does operate at a lower temperature, but the display does not resolve a temperature difference between R_{L1} and R_{L2}.

In the case of the device with the open base resistor metalization, one would not expect the infrared display to vary significantly from the normal devices, and no appreciable difference is seen. Figure 9 is a photomicrograph of the test vehicle and figures 10, 11 and 12 are photographs of the infrared displays of the device with the

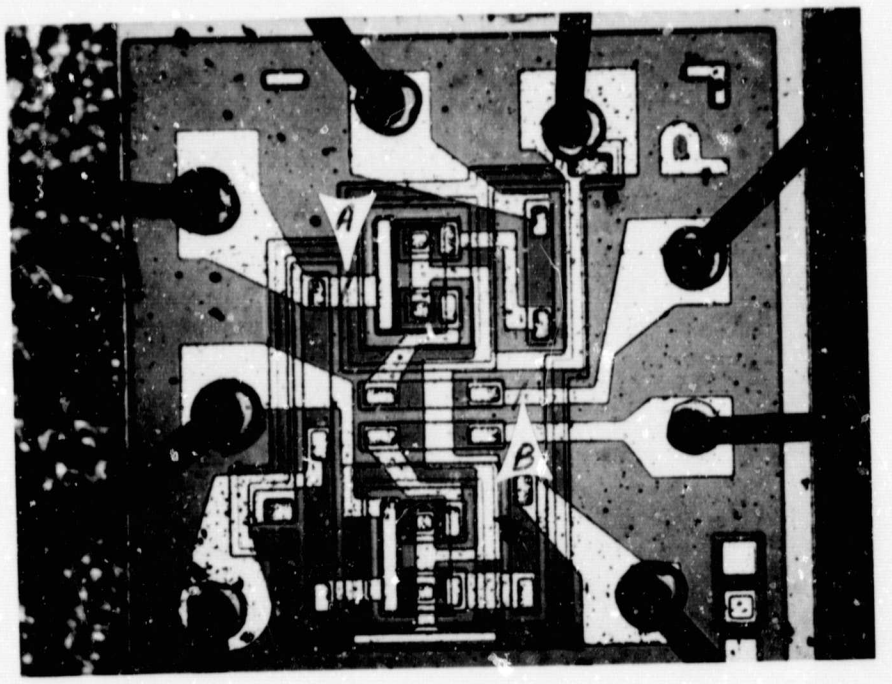


Figure 9- A photomicrograph of a dual two input gate

Figure 10- A color modulated infrared display showing a defect in point A.

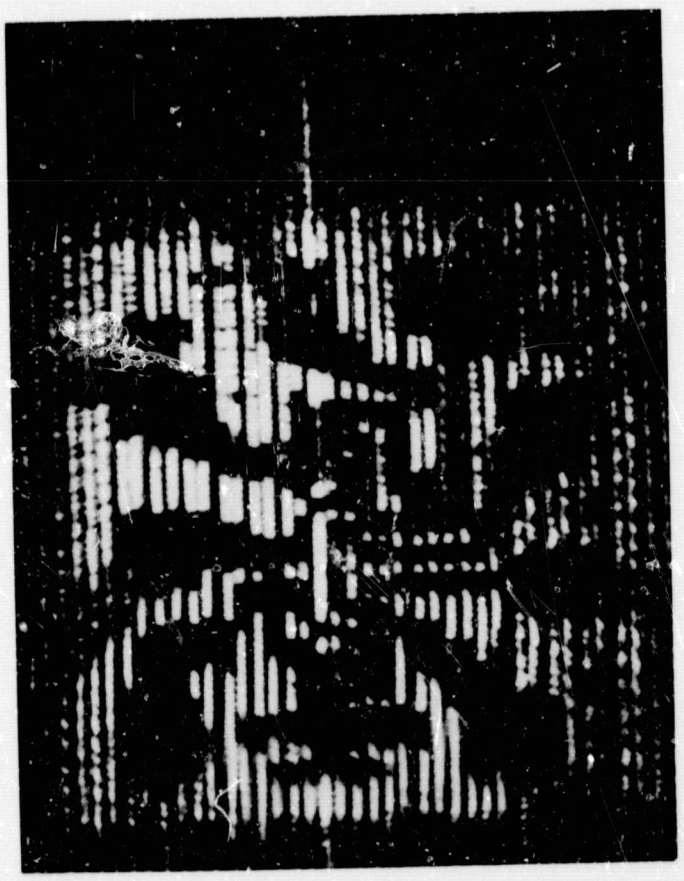


Figure 11- A color modulated infrared display showing a defect in point B.

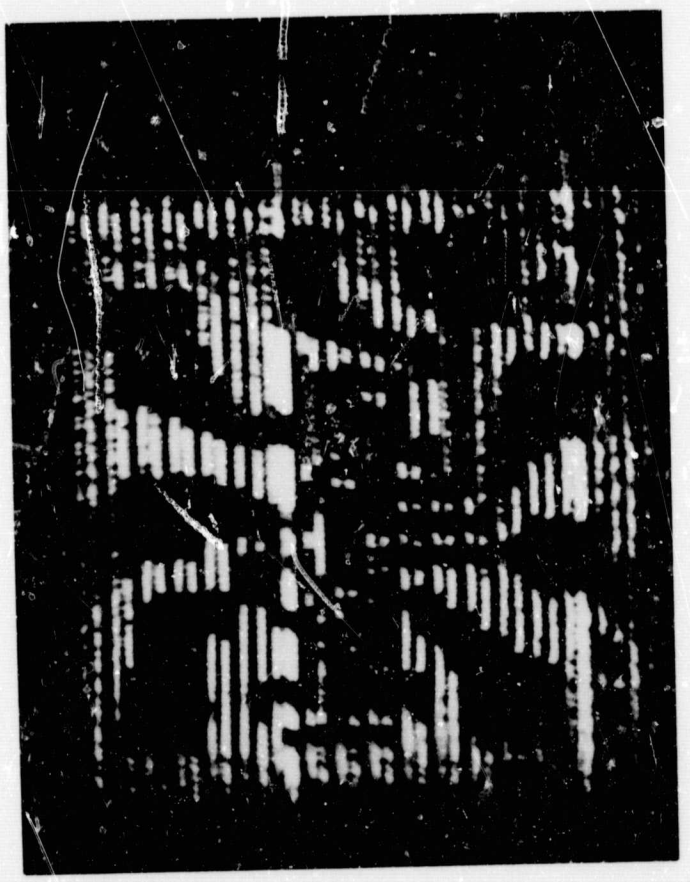


Figure 12- A color modulated infrared display of a good device.

defect at point A, the device with the defect at point B, and a normal device respectively.

2.4 COLOR MODULATED INFRARED DISPLAYS OF ELECTRICALLY GOOD AND ELECTRICALLY DEFECTIVE COMPLEX BI POLAR ARRAYS

Color modulated infrared displays of one electrically good, and three electrically defective complex bipolar array devices were generated. Each device contains 415 components interconnected with the use of bilayer metalization techniques in an RTL configuration. A block diagram of the device is shown in figure 13. The infrared displays were made during the time the devices were operating under a supply voltage of 3V and 2V, 10KHz clock. The circuit is shown in figure 14. The color displays of two of the defective devices were significantly different from the electrically good device. The color display of the third defective device was similar to the good device, but did show some slight differences in thermal characteristics. The initial evaluation of the electrical cause for failure of device #54 indicated difficulty in the 2^1 output flip flop and electrical evaluation of device #108 indicated difficulty in the 2^0 and 2^1 output flip flops. These were the two devices which showed significant differences in the infrared characteristics when compared to the electrically good device. The initial evaluation of the characteristics of device #49 was inclusive as far as the location of the defective area. Further evaluation will be made, but the differences in the thermal characteristics do not seem to be related to the electrical difficulties associated with the device.

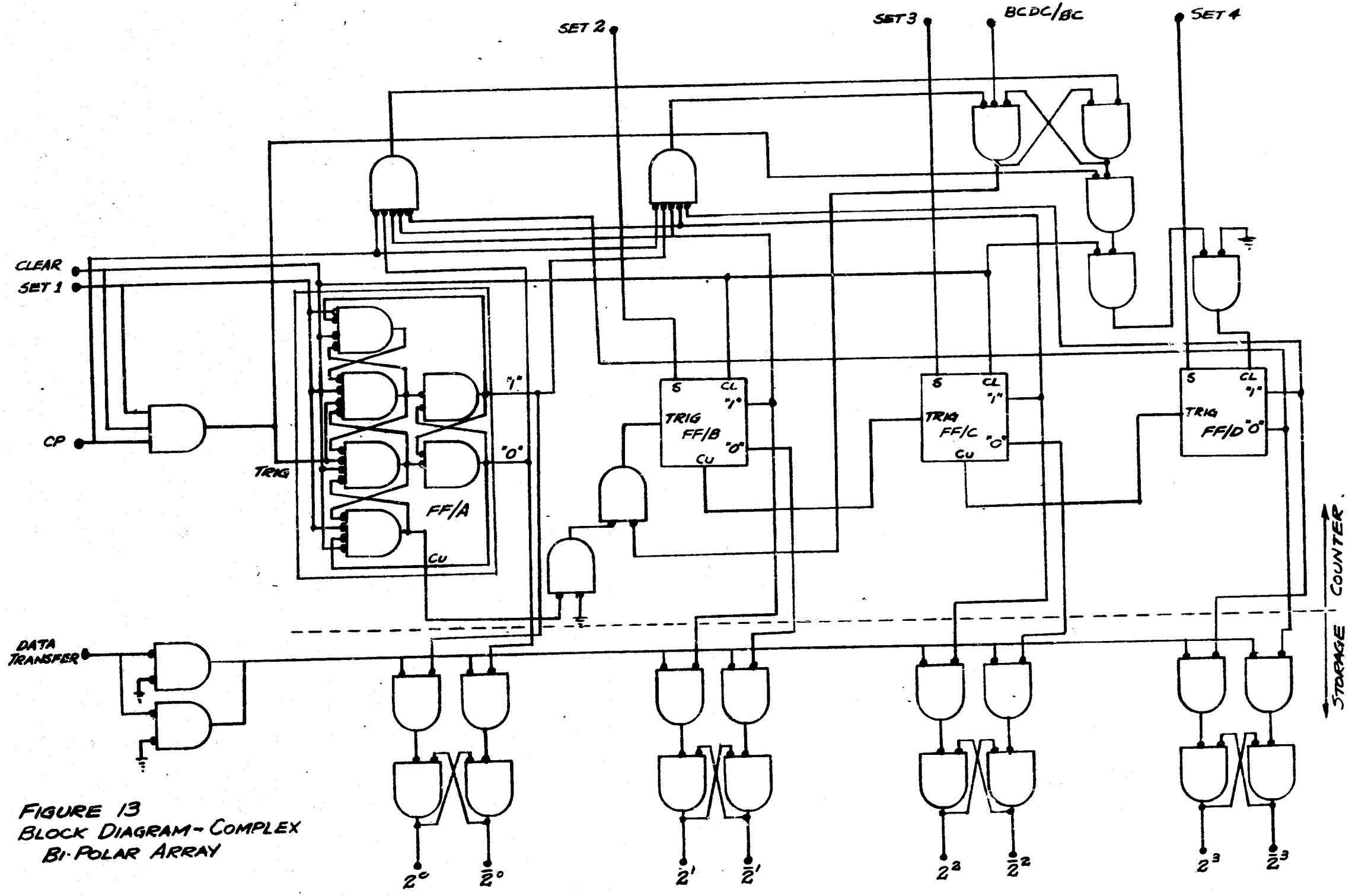
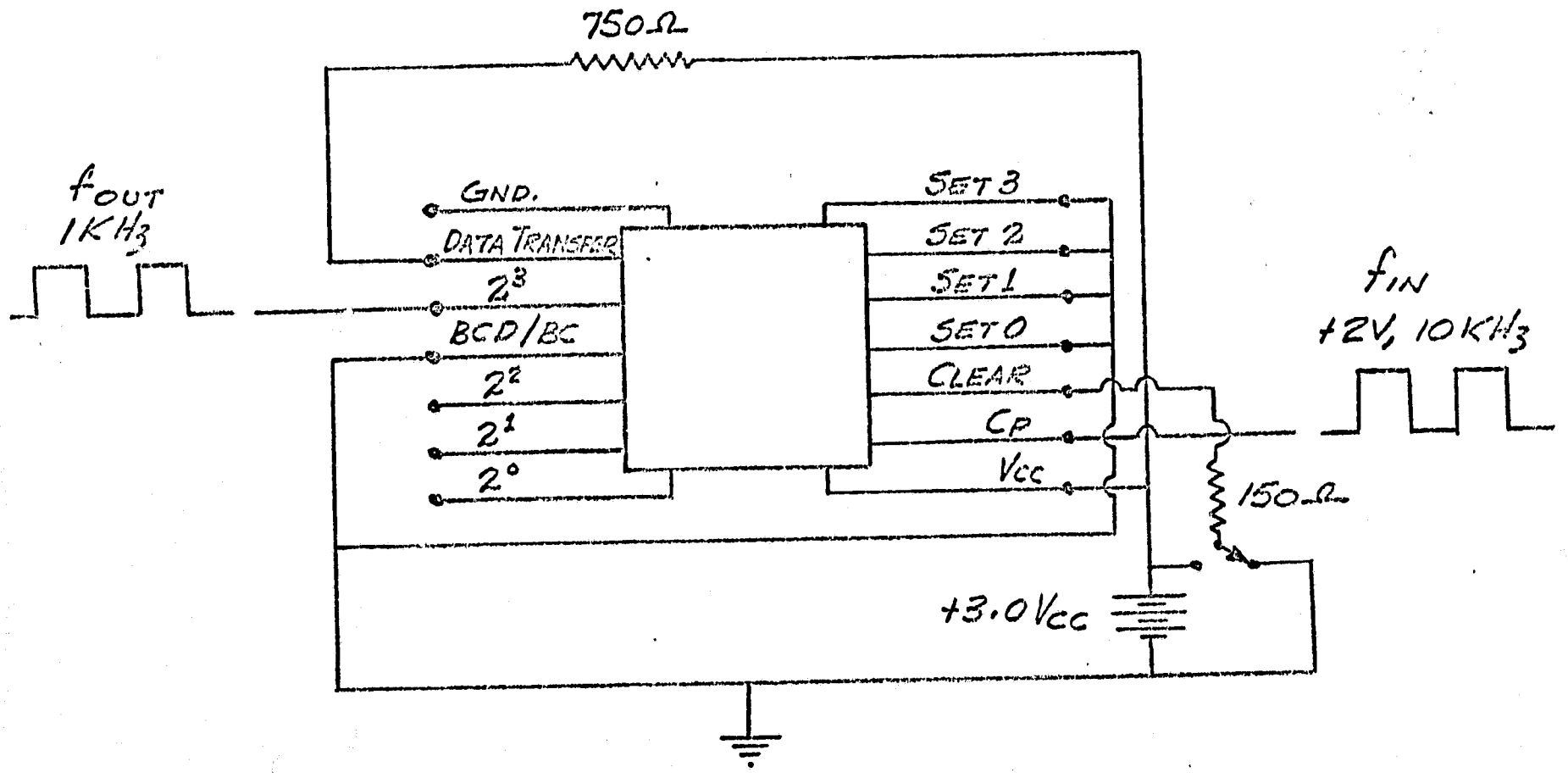


FIGURE 13
BLOCK DIAGRAM - COMPLEX
BI-POLAR ARRAY



NOTE: A POSITIVE PULSE MUST BE APPLIED TO CLEAR LINE TO INITIATE THE OPERATION OF THE DEVICE IN THE BCDC MODE.

FIGURE 14. TEST CIRCUIT FOR COMPLEX BI-POLAR ARRAY

2.5 LOCALIZED HEATING AT VIAS BETWEEN UPPER AND LOWER METALIZATION PATTERNS OF BILAYER METALIZED DEVICES

To determine if the vias which provide the electrical connection through the glass insulation layer between the top and bottom metalization patterns are a source of localized heating, evaluations utilizing two separate types of vehicles were performed. The evaluations consisted of generating infrared line scan data along the center line of metalizations that contained vias during the time the stripe was conducting current.

The initial evaluation was performed using bilayer metalized DTL devices. A photomicrograph of this vehicle is shown in Figure 1. The test circuit was arranged to cause various levels of d.c. current to flow through the via in the Vcc stripe. This particular via is 1/4 mil by 1/4 mil in cross section and approximately 12,000 Å in length. In the case of these vehicles localized heating at the via was initiated as current levels between 16 and 22 mA. At current levels of about 30 mA, considerable heating was observed at the via as indicated below:

DEVICE NO.	CURRENT mA	METALIZATION STRIPE TEMPERATURE °C	VIA TEMPERATURE °C	DELTA TEMPERATURE °C
420	31.5	97	127	30
517	31.0	103	[illegible]	22
516	29.5	97	120	23
519	30.5	94	118	24
520	31.5	85	109	24
518	30.5	97	107	10

From this data, the average increase in temperature of the via as compared to the metalization stripe is 22°C, at an average current level of 30.8 mA.

The second evaluation was performed using the test vehicle shown in figure 15.

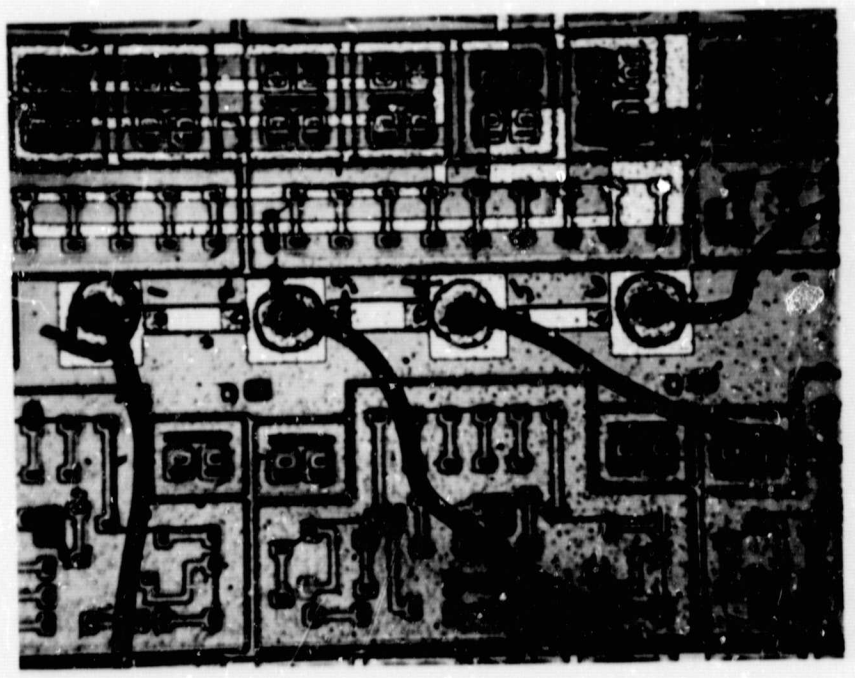


FIGURE 15. Test Vehicle for Evaluation of Localized Heating at Vias.

The vehicle consists of a series of upper and lower metalization stripes connected by vias approximately 1/4 mil by 1/4 mil in cross section and 12,000 Å in length. Line scans made along the center line of these metalization stripes on 8 different devices at current levels as high as 50 mA, did not indicate any appreciable heating at any via. Unfortunately, not all of the data obtained was usable because the location of the nail head bond obscured the infrared radiation from some of the vias.

From the data obtained during these evaluations, it appears that in the case of the bilayer metalized DTL devices, electrical resistance occurred in the vias and caused localized heating because of ohmic heating. The test vehicles used in the second part of the evaluation however, did not indicate any appreciable heating. This demonstrates that if bilayer metalization processing is properly defined and accomplished, no heating will occur in the vias, and the use of bilayer metalization techniques should not have any adverse effect on reliability.

2.6 FLIP CHIP HEATING EVALUATION

A single device of multiple flip chip construction was evaluated. The device contained four active silicon devices flip chipped onto a silicon substrate which contained the interconnecting metalization patterns. The silicon substrate was header bonded into a metal bottom flat package. The data obtained indicated that there is sufficient thermal conduction through the electrical contacts between the active chip and the silicon substrate to maintain the active chip at a reasonably even operating temperature with a relatively small gradient between the chip and the substrate. The evaluation also indicated chip to header bond voids under the silicon substrate which caused the areas above the voids to operate at a higher temperature than the areas above the well bonded portions of the substrate. This information was confirmed by radiographic techniques which indicated substrate to header bond voids in the regions that operated at higher than normal temperatures.

2.7 EVALUATION OF HEATING AND COOLING RATES OF DISCRETE COMPONENTS

In all of the studies thus far performed, we have permitted the device under evaluation to come to thermal equilibrium before initiating the infrared scanning. It was conjectured that because of the good thermal conductivity of silicon, when the device is studied in this state, the thermal effects are so spread that it is impossible to detect localized areas that operate at slightly higher or lower than normal dissipations. We therefore initiated work to determine the heating and cooling rates of discrete components, and the areas surrounding these components, when the component is subjected to pulsed power operation. The purpose of this evaluation was to determine the optimum scanning speeds and pulse rates necessary to isolate defective areas.

Figure 16 is a photograph of the test vehicle selected for this evaluation. It is a 35 X 35 mil chip containing several discrete elements and is mounted in a metal bottom flat package.

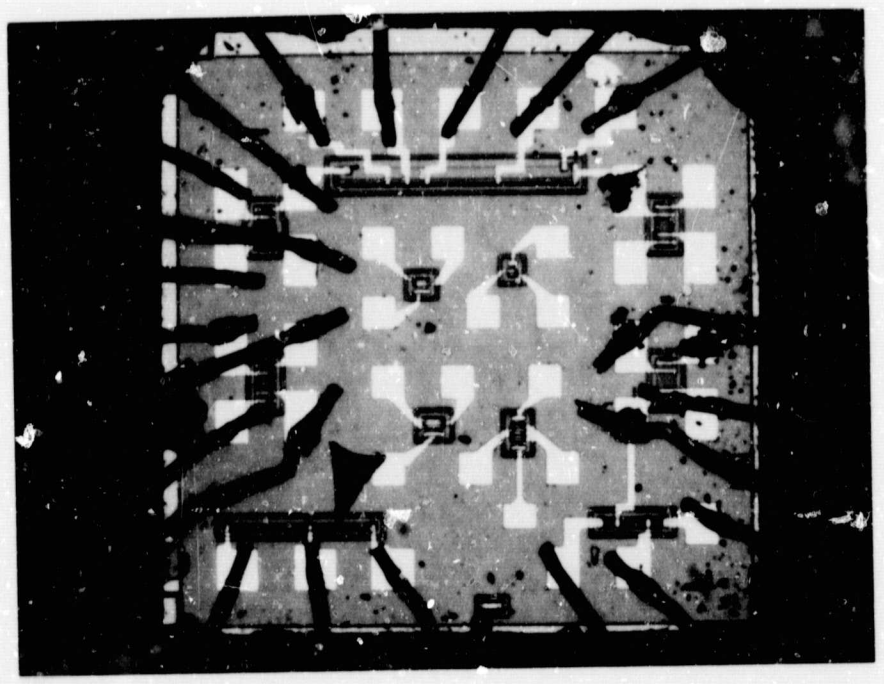


FIGURE 16. Photomicrograph of 35 X 35 Mil Chip
Utilized for heating and cooling rate evaluation.
Resistor R-8 is indicated by the arrow.

The initial evaluation consisted of pulsing D.C. power into a discrete diffused resistor (R-8 indicated by the arrow on figure 16) and measuring the rate of temperature increase and the rate of temperature decrease immediately over the resistor, 10 mils from the resistor, and 20 mils from the resistor. In this evaluation the component was supported only by its external leads and the heating and cooling rates determined are referenced to free air. The data obtained from this evaluation is shown in Figures 17, 18, and 19.

A second evaluation was performed with the same vehicle mounted on a heat sink and the data derived from this portion of the evaluation is shown in Figures 20, 21, and 22. In both of the above cases the initial heating and cooling fits an equation of the form:

$$t = A\Theta^{b}$$

where t = time in seconds after the instant power is turned on or off.

A = an experimentally derived constant

Θ = the temperature in °C

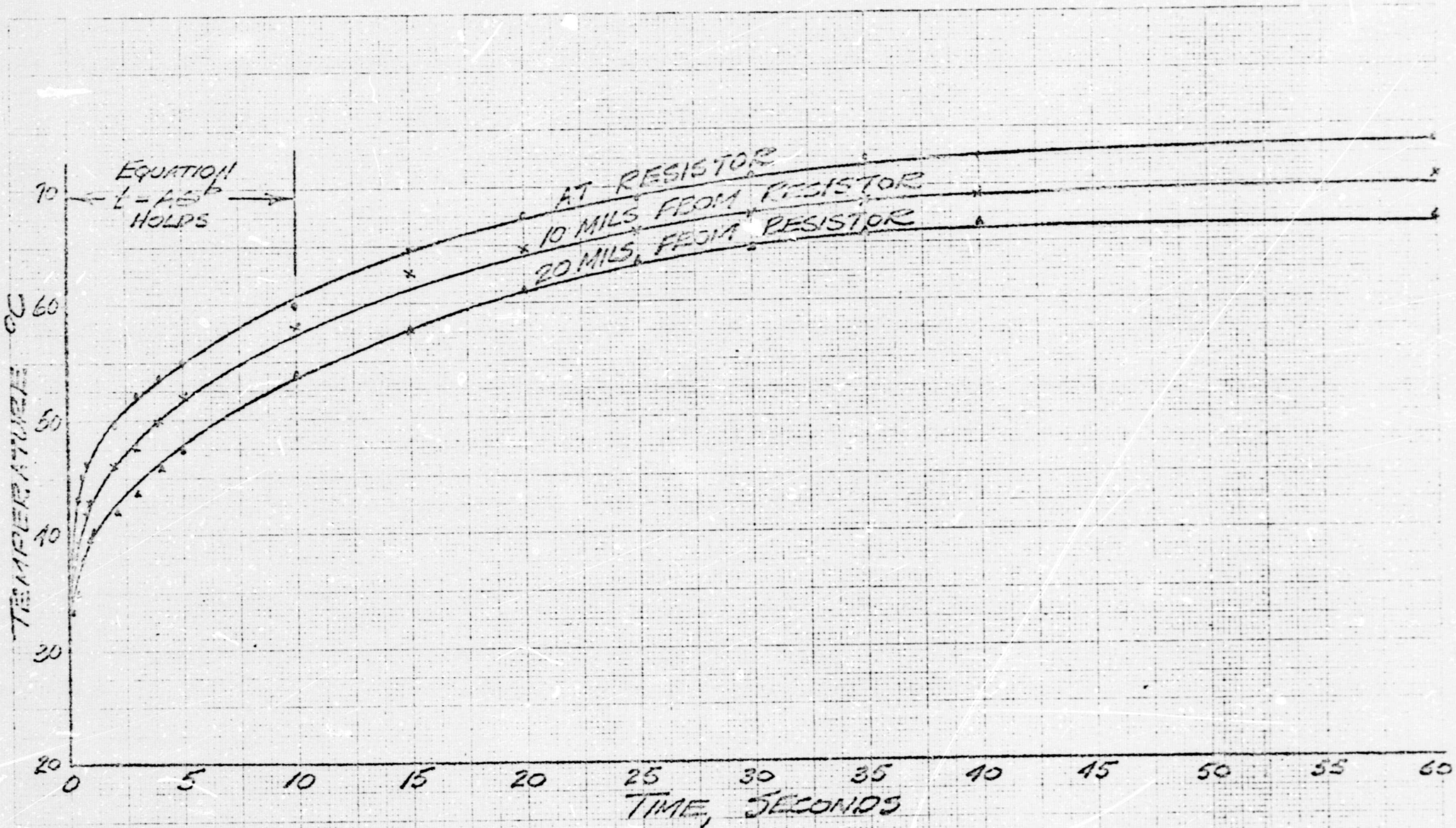
b = an experimentally derived constant in the range of 9 to 11.

After the fast initial rise or fall of temperature, the rate of change becomes very gradual and the equation fails. Figure 23 indicates the operating temperature at the three locations at various times after the turn on of the power pulse. It is observed from these curves that when the device is dissipating to free air, increased time results in "blurring" of localized hot spots, but when the device is mounted on a heat sink, increased time results in enhancement of the localized hot spot, and the time required for the device to reach its maximum temperature is much shorter than with the device dissipating to free air.

It should be noted that in the case of these measurements, the silicon chip was mounted in a metal bottom flat package, which has relatively good thermal transfer characteristics, if another package, with a higher coefficient of thermal conduction were mounted on a heat sink, enhancement of localized hot spots with time would not occur to the same extent.

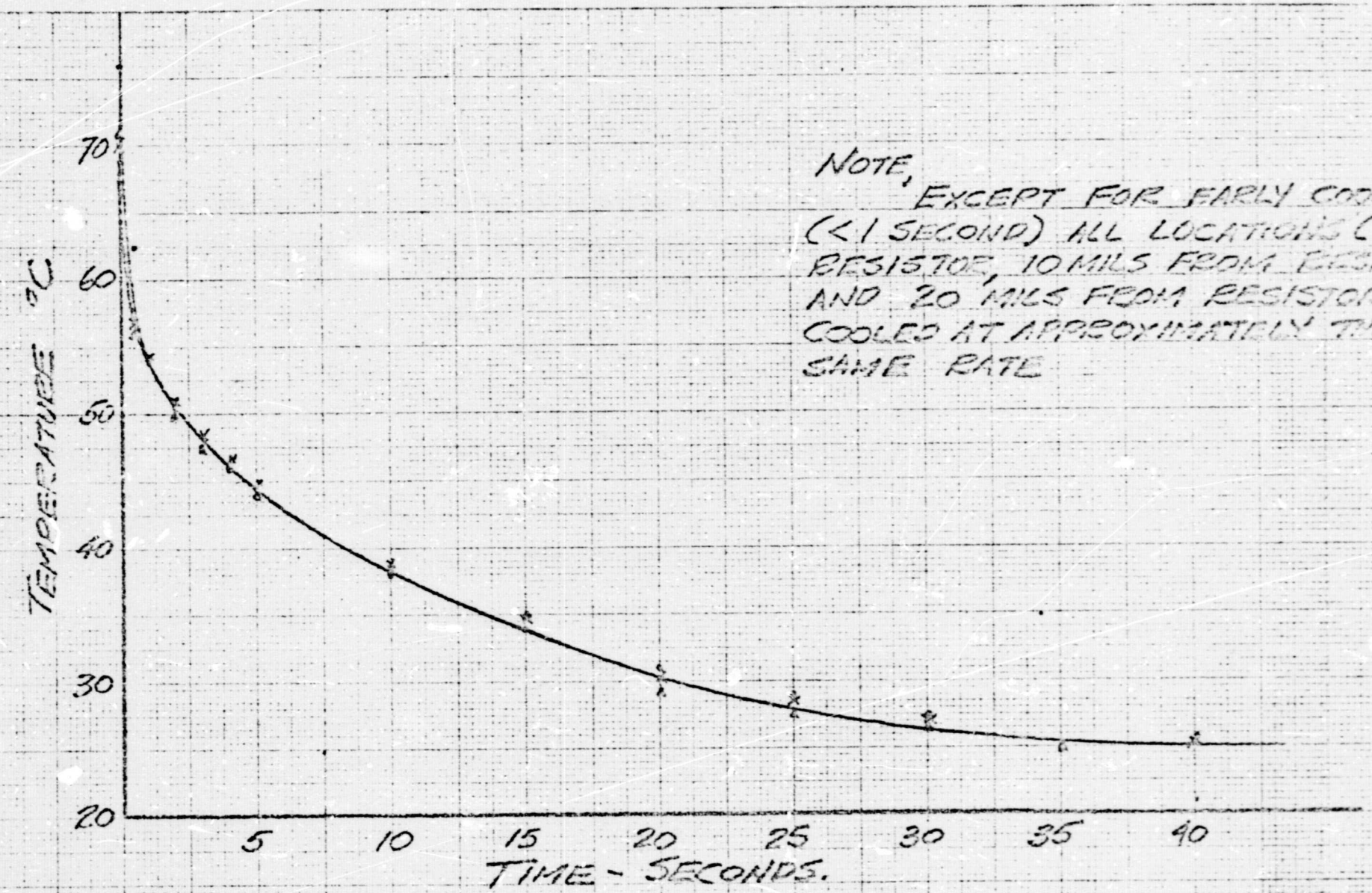
The data thus far obtained indicates that localized hot spots can be enhanced by operating the device on a heat sink. It also indicates that when the device is heat sinked the maximum operating temperature is achieved about 0.10 seconds after the application of the power pulse. The difficulty with operating the device on heat sink is that at the normal dissipation levels of most integrated circuits the operating temperature of the device is close to room temperature, the lower limit of the temperature detection capability of existing infrared equipment. However, if small localized

defects exist that cause localized high energy densities, and therefore temperatures several degrees higher than surrounding areas, the data obtained thus far in this evaluation indicates that the location of these defect areas should be enhanced by pulsed operation of "heat sinked" devices during the evaluation to verify this indication by determining the rate of rise and fall of temperature in smaller areas than resistor R-8, and to utilize the data obtained to determine the optimum power pulse width and duty cycle and the optimum scanning rate for the detection of small localized hot spots.



HEATING RATE FOR TEST VEHICLE WHEN MOUNTED IN FREE AIR DISSIPATION = 350 mW

FIGURE 17



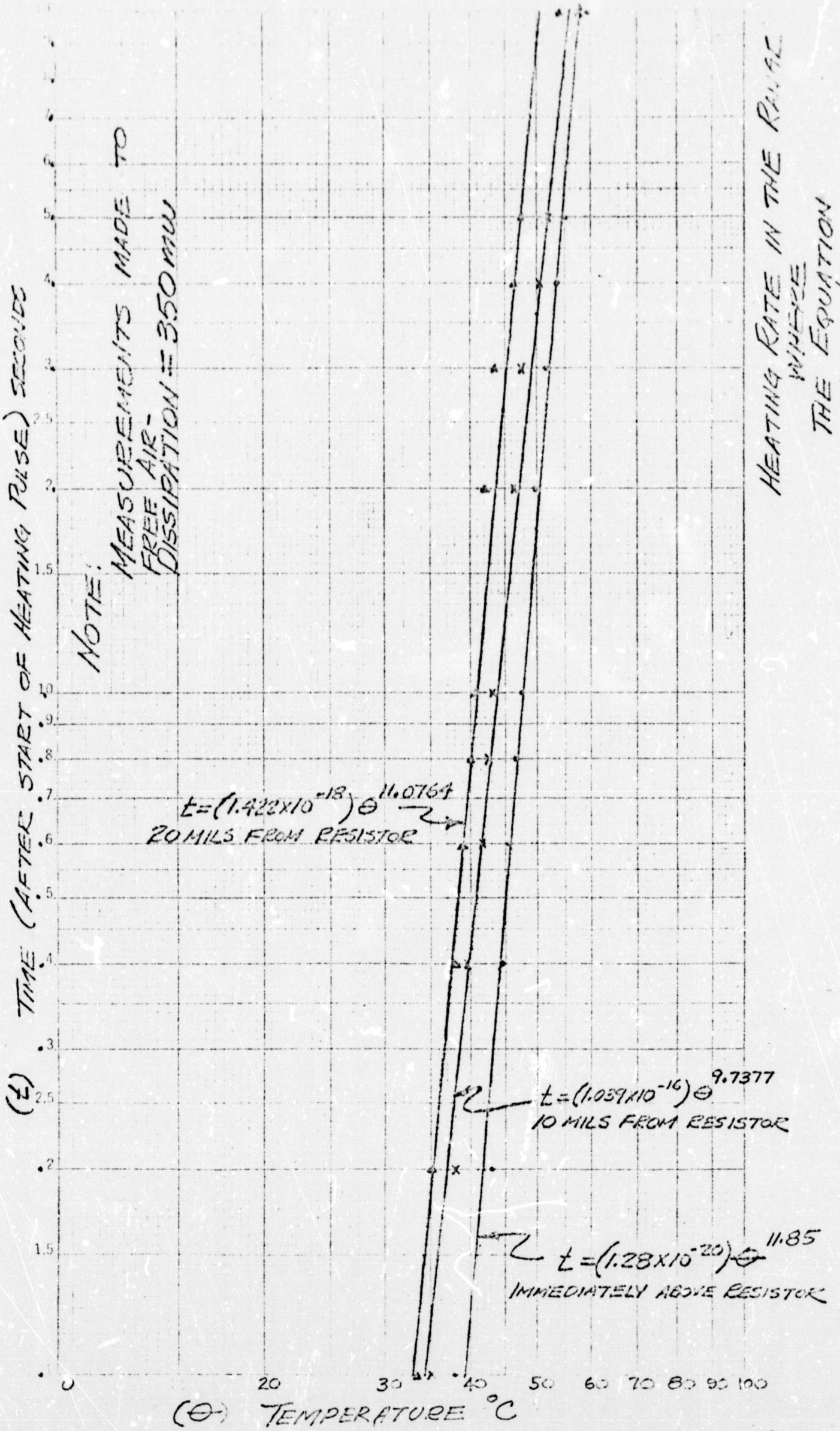
NOTE,
EXCEPT FOR EARLY COOLING (<1 SECOND) ALL LOCATIONS (I.E. AT RESISTOR, 10 MILS FROM RESISTOR AND 20 MILS FROM RESISTOR) COOLED AT APPROXIMATELY THE SAME RATE

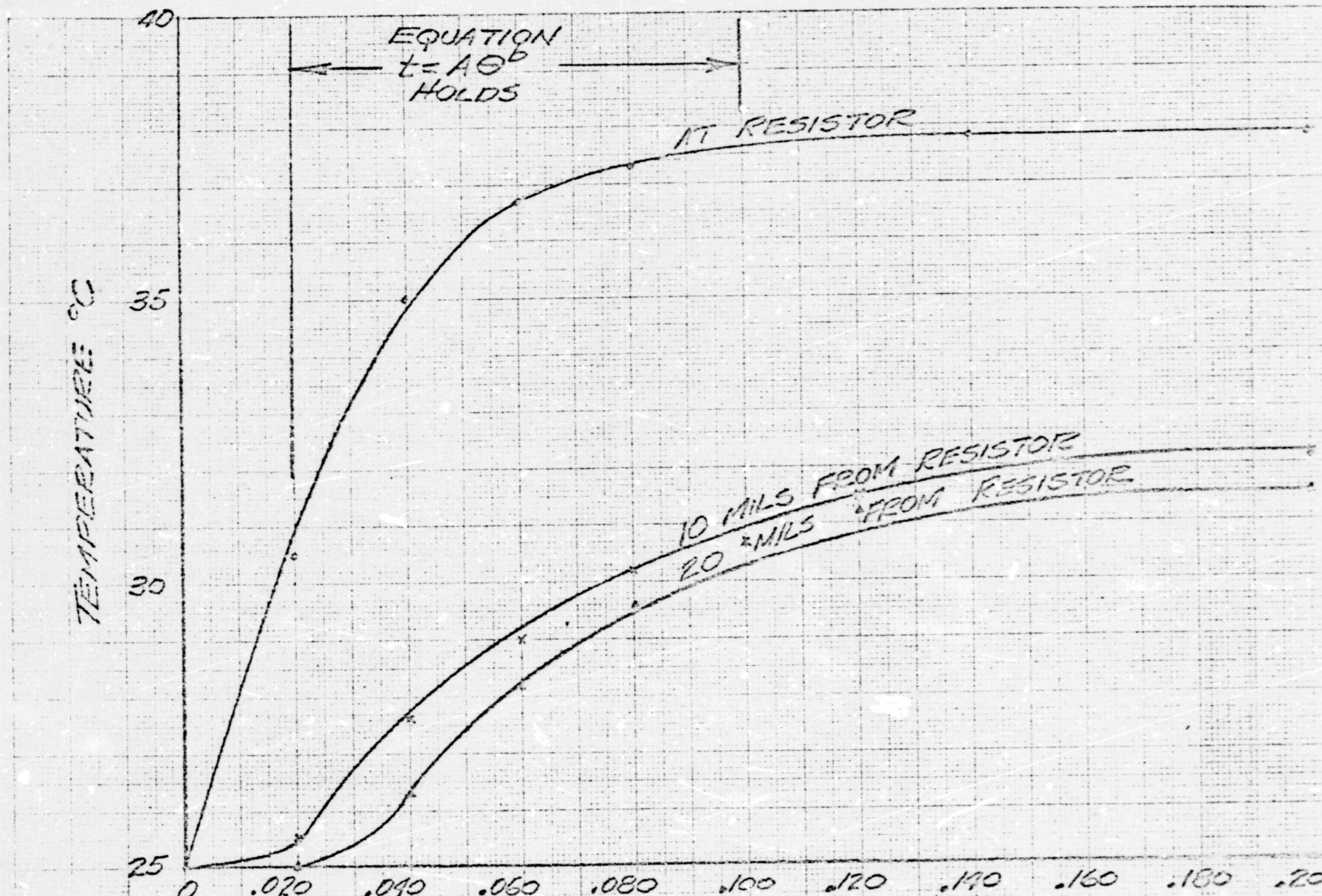
COOLING RATE FOR TEST VEHICLE WHEN MOUNTED IN FREE AIR. DISSIPATION = 350 MW

FIGURE 18

FIGURE 15

HEATING RATE IN THE PULSE MINIMUM
THE EQUATION
$t = A\theta^{\alpha}$
FOR
HOT SPOT





HEATING RATE FOR TEST VEHICLE
WHEN
MOUNTED ON HEAT SINK
DISSIPATION = 400 mW
FIGURE 20

COOLING RATE FOR TEST VEHICLE
WHEN
MOUNTED ON HEAT SINK
DISSIPATION = 400 MW.

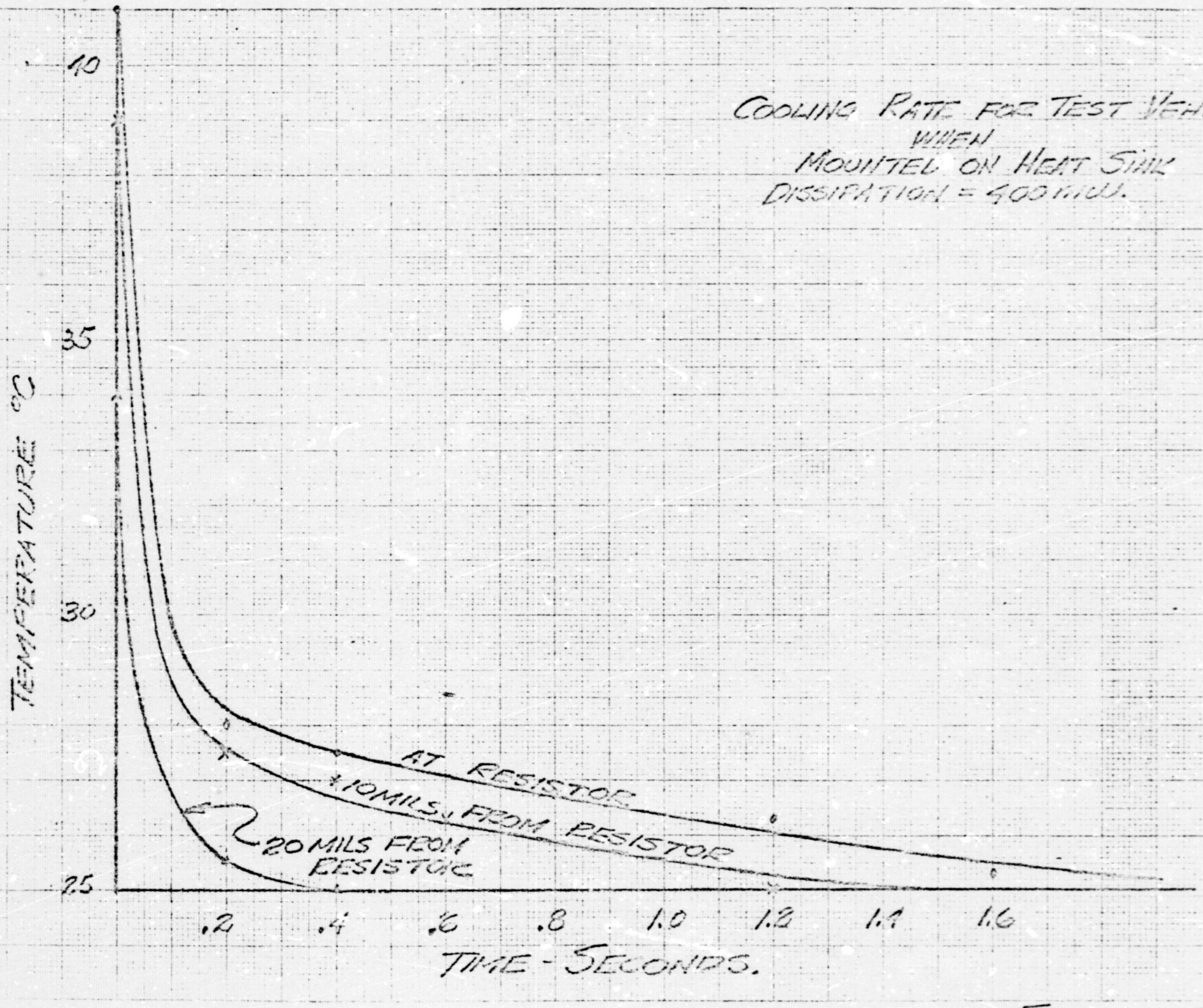
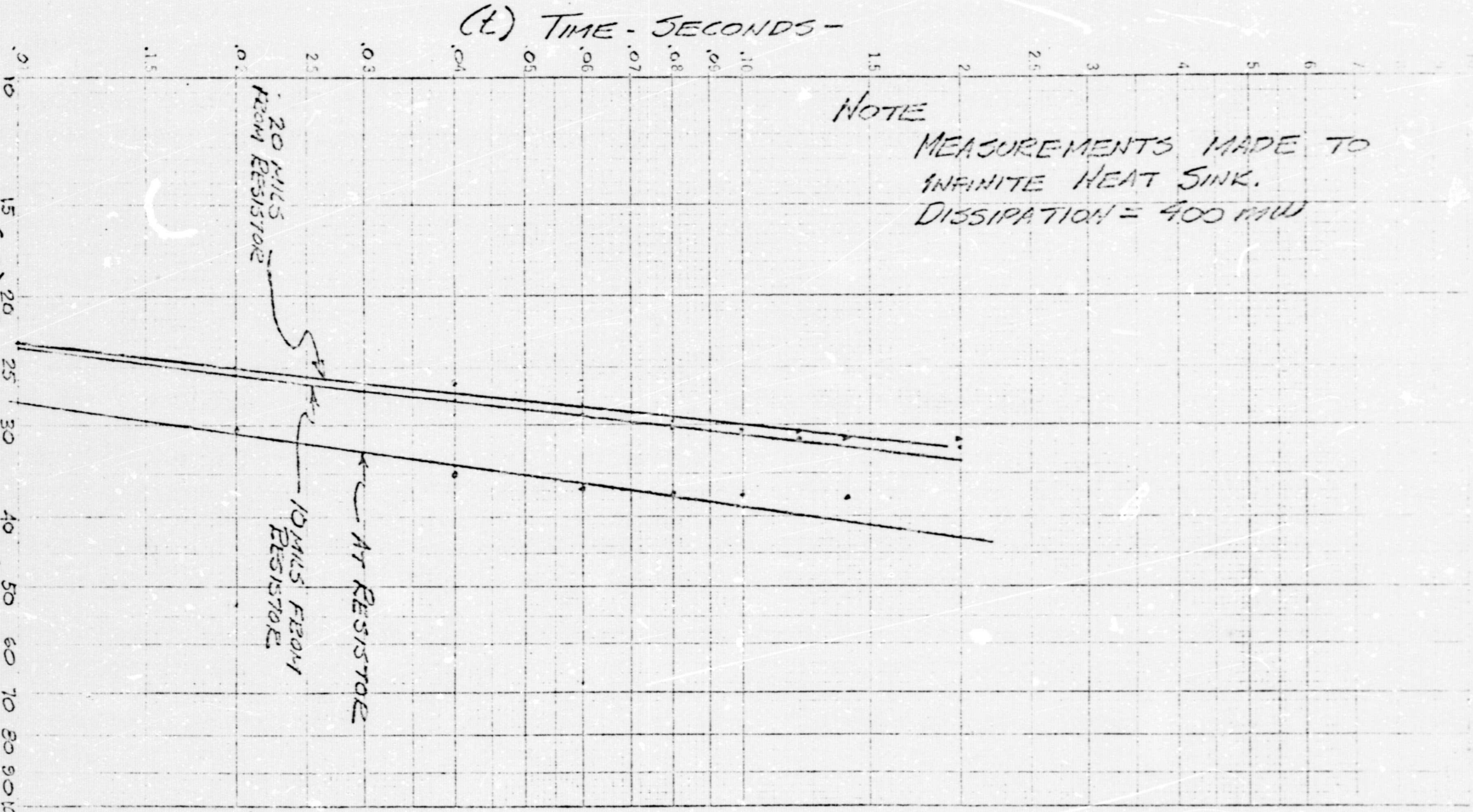


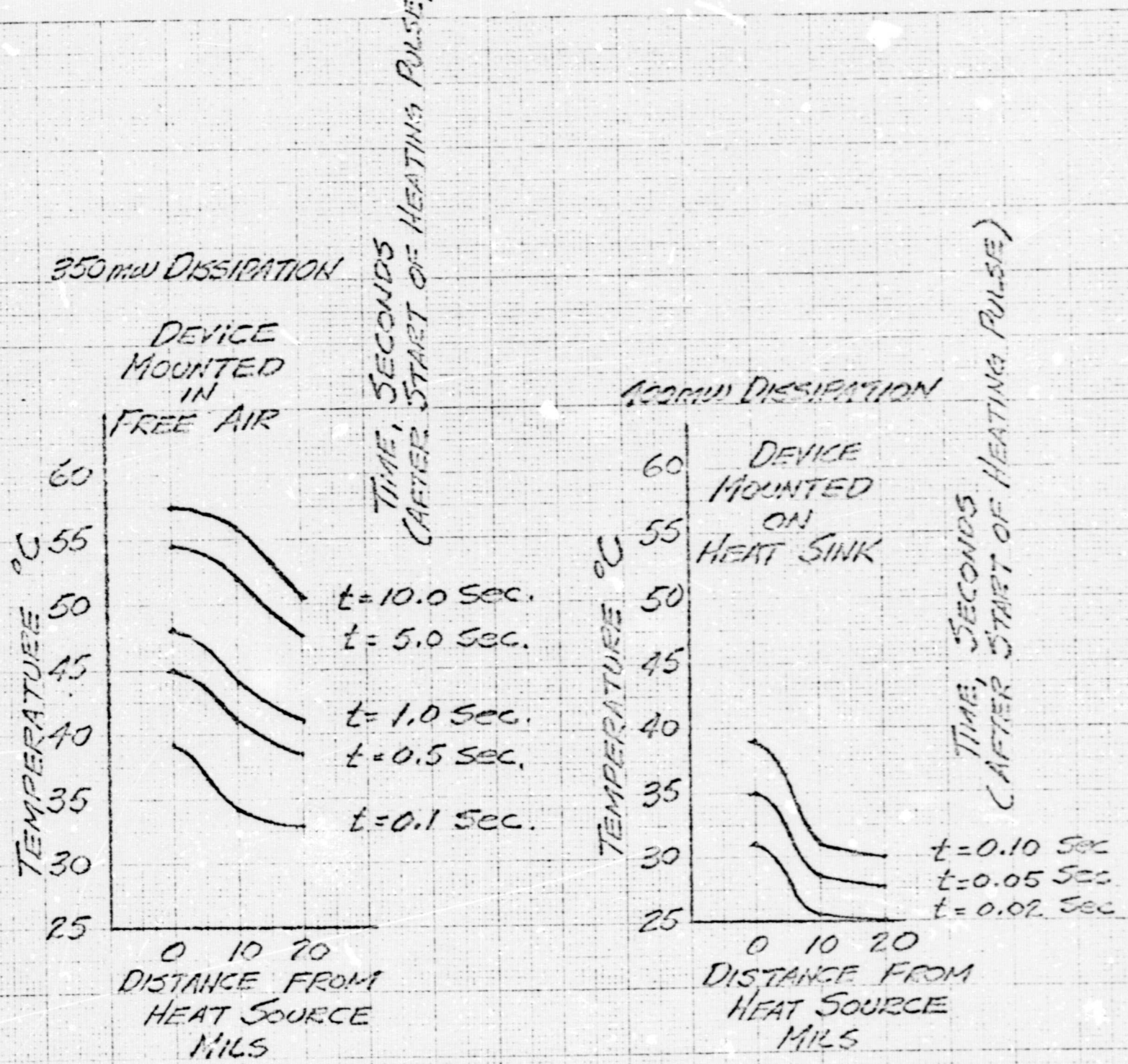
FIGURE 2.1



NOTE
MEASUREMENTS MADE TO INFINITE HEAT SINK.
DISSIPATION = 400 MW

HEATING RATE IN THE RANGE WHERE THE EQUATION $t = A\theta^b$ HOLDS

FIGURE 2.1



TEMPERATURE GRADIENT VS TIME.

FIGURE 23

Section III - FUTURE ACTION

3.0 WORK PLANNED FOR NEXT QUARTER

We will continue our efforts to determine the optimum infrared scanning conditions, through the measurement of the heating and cooling rates of discrete components. Specifically we will obtain data similar to that presented in section 2.6 for various components of various sizes, and we shall also determine the effects of the interactions when 2 or more discrete components are simultaneously energized. It is believed that this data will yield significant information concerning the types of semiconductor defects that can be observed in addition to the determination of the optimum infrared scanning conditions.

When this data is obtained we will resume our evaluation of the infrared manisfestations of gross visual defects such as oxide and diffusion faults, provided the data obtained indicates these types of defects will be observable. We also intent to complete the evaluation of the data obtained on the complex bipolar array BCDC devices, and the bilayer metalized DTL devices.

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