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FINAL TECHNICAL REPORT

DESIGN AND DEVELOPMENT OF A DIGITAL SUBSYSTEM EMPLOYING N- AND P- CHANNEL MOS FET'S IN COMPLEMENTARY CIRCUITS IN AN INTEGRATED CIRCUIT ARRAY

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FOREWORD

This quarterly technical report covers the work performed by RCA Electronic Components, Somerville, New Jersey, under Contract No. NAS 12-119 from 1 May 1967 to 30 April 1968.

SUMMARY

The past year under this program has resulted in the following developments:

a. A basic cell for the universal wafer approach was designed and fabricated. The cell, which consists of two groups of four p-channel and four n-channel devices, occupies an area 35 mils by 38 mils. The devices in the cell have a 5-mil channel width, a 0.3-mil channel length, and a 1000Å oxide thickness over the gate area. The cell design allows a ±0.5-mil tolerance for the final metalizations.

b. A process for two-layer metalization was developed. Typical contact resistance was in the range of 0.7 ohm per square.

c. Two circuits with single-layer metalization were fabricated and tested: a dual inverter circuit using one basic cell with a typical stage delay of 12 nanoseconds; and a J-K flip-flop using two cells and operated at frequencies as high as 2 megahertz.

d. A full-adder circuit with two-layer metalization also was fabricated.

e. Using the universal wafer, a four-stage counter was designed and fabricated in which 16 basic universal cells and two-layer metalization were used. This four-stage counter has a clock input, four parallel outputs, a reset, and four parallel set-inputs gated-in by a "set enable" signal. The circuit can be used as a general purpose four-stage binary counter that can be set by a logic signal into any one of the 16 different possible states in one cycle. This counter also has reset capability. A total of 120 transistors are used in the four-stage counter circuit. It occupies an area 80 mils by 150 mils. The integrated four-stage counter operates at clock frequencies up to 5 megahertz.

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SECTION I
INTRODUCTION

The program objective was to design and develop the technology required to fabricate MOS complementary logic on a "universal wafer," i.e., one that can be adapted to all MOS "true" complementary logic circuits by the design of the two final layers of metalization. This universal wafer approach was demonstrated by the fabrication of a four-stage binary counter circuit. This four-stage binary counter has a clock input, four parallel outputs, a reset, and four parallel set-inputs gated-in by a "set enable" signal. The circuit can be used as a general purpose four-stage binary counter that can be set by a logic signal into any one of the 16 different possible states in one cycle. The circuit also has reset capability.

SECTION II
TECHNICAL DISCUSSION

A. GENERAL

There are two approaches to the design of an integrated circuit (IC) that require 100-percent yield within the chip area: design the topology on the chip to meet the needs of a particular customer (tailored approach); or use a universal chip with all critical dimensions for diffusion and basic metalization masking preset, the metalized interconnections being designed by the requirements of a particular circuit (universal approach). The universal approach usually results in the use of greater chip area than the tailored approach currently being employed in the design of IC's. The universal approach, however, requires less initial cost, and the IC that subsequently is developed can be delivered much more rapidly to the customer.

For large quantities (e.g., one million units), the tailored approach will be used. A large-volume item can result from a multicustomer demand. For small to medium quantities, however, the universal approach can be practical and can achieve lower cost. The curve of Figure 1 provides a graphic illustration of the above statements. The crossover point in cost shown in Figure 1 depends upon economy of wafer area in the universal approach, relative sophistication of computer designing, and relative quantities (large to small) required by customers.

Complementary-symmetry MOS (COS/MOS) logic circuits are more practical for the universal approach than are standard bipolar or other types of MOS logic circuits. This characteristic results from the operation of micropower complementary circuits, in which MOS units are operated push-pull. In such operation, the devices do not require precise match of electrical characteristics; for example, the relative g_m among units may change by one order of magnitude or better. This statement is true only if the maximum speed capability of

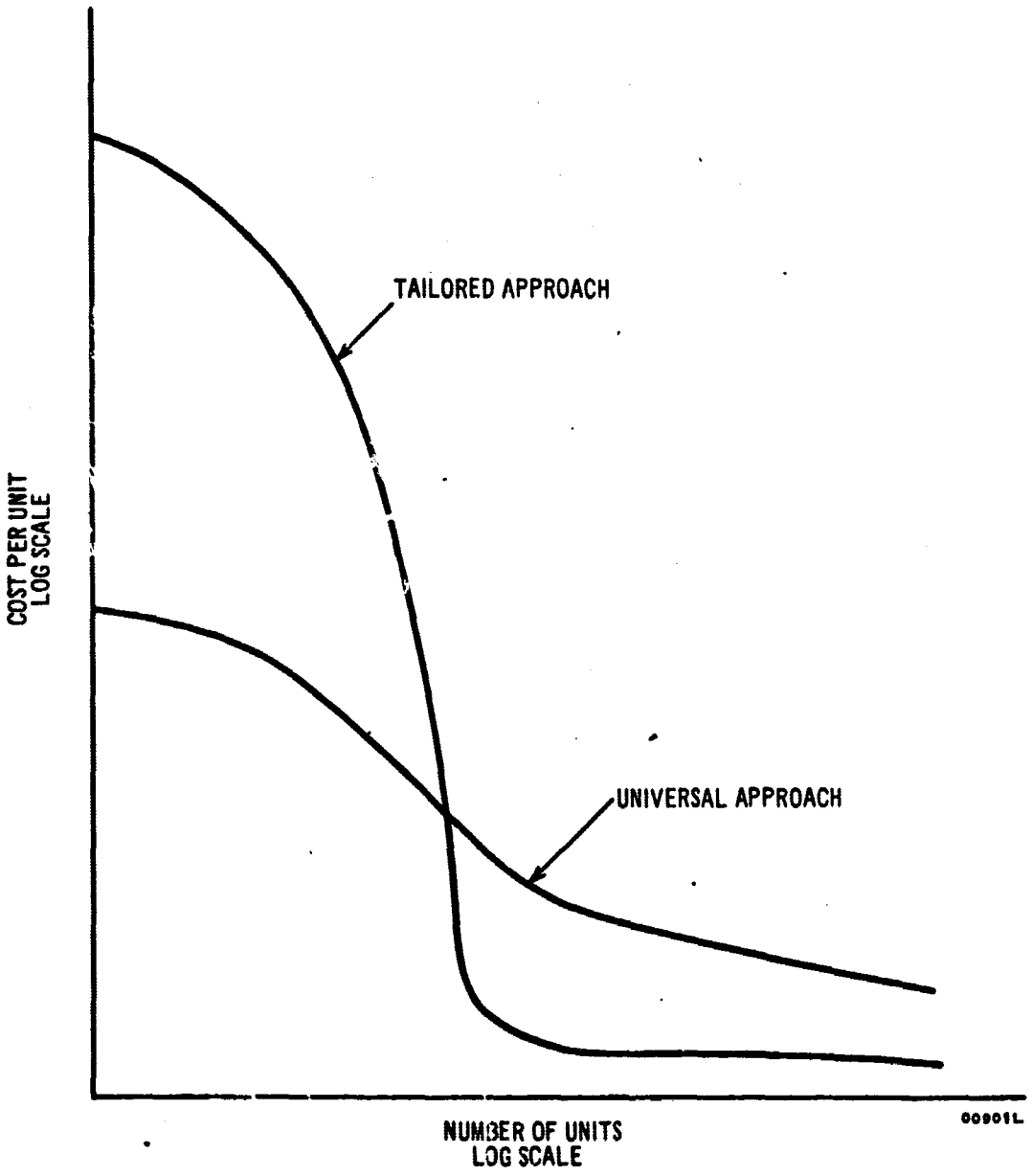

Figure 1. Comparison of Tailored Approach and Universal Approach[1]

the circuit (considering units conforming to the mean specifications) exceeds the operating speed. Rather loose tolerances for the characteristics of threshold voltages and leakage current also can be allowed in the circuit design. The circuit generally will operate unless catastrophic types of failures occur (e.g., short and open circuits).

Because of their complementary operation, many circuits can be designed from the single cell (i.e., the basic diffused pattern). Any universal wafer approach uses more silicon area than its equivalent tailored approach. The complementary MOS cell in which both n-channel and p-channel MOS units are used, however, is less wasteful of area than any other system of cells in which other types of logic are used. The cell basically consists of four n-channel and four p-channel full-gate MOS devices with common source-drain regions in doubly periodic spacing. These devices are able to interchange the electrical actions of source and drain. This interchange capability permits circuit versatility, thus minimizing wasted space. (Wasted space is an inherent disadvantage of the universal approach.) A wafer containing basic cells with one layer of metalization, including the metalized gates and metalized windows connecting to the diffused areas, would be inventoried. The chip size, with respect to yield, would be determined by the state of the art. From a circuit standpoint, the whole wafer can be used. The process is adaptable, therefore, to various sizes of arrays.

B. UNIVERSAL WAFER APPROACH

Figure 2 is a block diagram showing the complete processing cycle of the universal wafer approach. A special circuit from the customer first is designed in logic form, using the logic circuit library. The logic circuit library will contain circuits such as shift register bits, counter bits, memory cells, flip-flops, etc., in addition to a variety of gates. All circuits will be represented by logical symbols. Two sets of interconnection masks then are generated from the circuit. The computer will generate three sets of masks, using preset patterns from the library catalog and a set of interconnection algorithms. The first metalization mask is used to etch the inventoried universal wafer and form the first metalization pattern. A thick layer of oxide then is deposited over the first metalization pattern

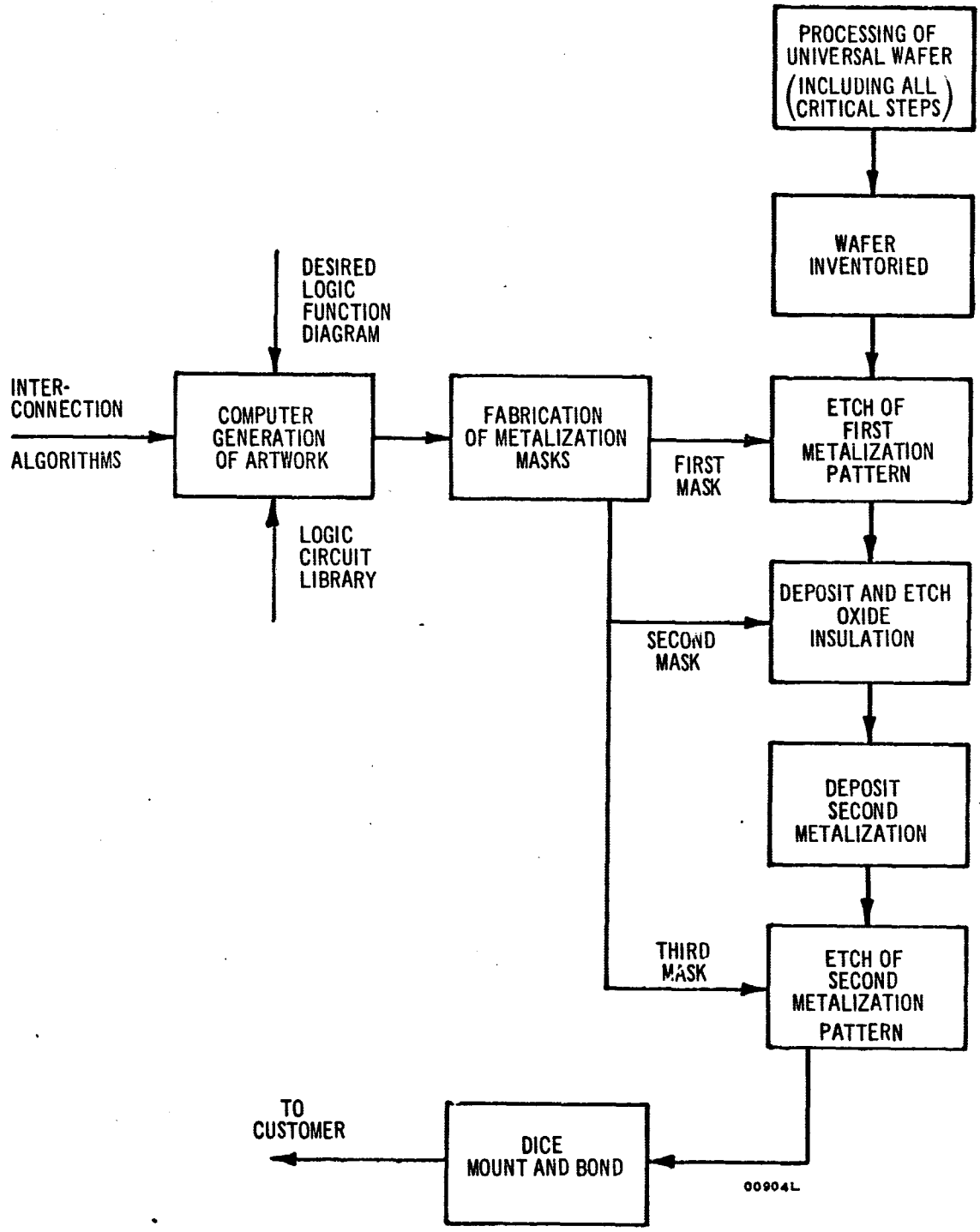

Figure 2. Block Diagram of Universal Wafer Approach

to form an insulating layer. Before depositing a second layer of metal over the oxide, the second mask is used to form contact openings by etching windows into this insulating oxide layer. A third mask is used to etch the second metalization pattern over the insulating oxide layer, thus completing circuit interconnections. The final step is to dice the wafer into individual pellets and to have these pellets mounted and bonded before delivering the circuit to the customer. Either the designer or the customer can provide the final test.

Tolerances on the dimensions of the interconnection masks are much wider than tolerances on the dimensions of the diffusion masks of the basic cell. Because of wider tolerance, interconnection masks do not require a fine step-and-repeat process, as is required for the basic cell.

C. BASIC CELL OF UNIVERSAL WAFER

The basic cell used in the universal wafer approach consists of two groups of four n-channel and four p-channel devices with common source-drain regions, as shown in Figure 3. The source-drain regions of these devices have interchangeable electrical characteristics, permitting circuit versatility and minimizing space. Wasted space is always an inherent disadvantage of a universal approach; however, this form of universal approach minimizes the wasted space.

Wafers containing the basic cells with one layer of metalization, including the metalized gates and metalized contact openings to the diffused areas, are inventoried (Figure 4). The basic cell contains 16 MOS devices and occupies an area 35 mils by 38 mils, including sufficient area to accommodate most of the complex interconnection and intraconnection patterns. Each device in the basic cell has a channel length of 0.3 mil, a channel width of 5.0 mils, and an oxide thickness of 1000Å.

D. DUAL INVERTER CIRCUIT

To evaluate the processing of the basic universal wafer cell, a group of dual-inverter circuits using a single cell and single-layer metalization were fabricated and were packaged in 12-pin TO-5 cans. The circuit and pin

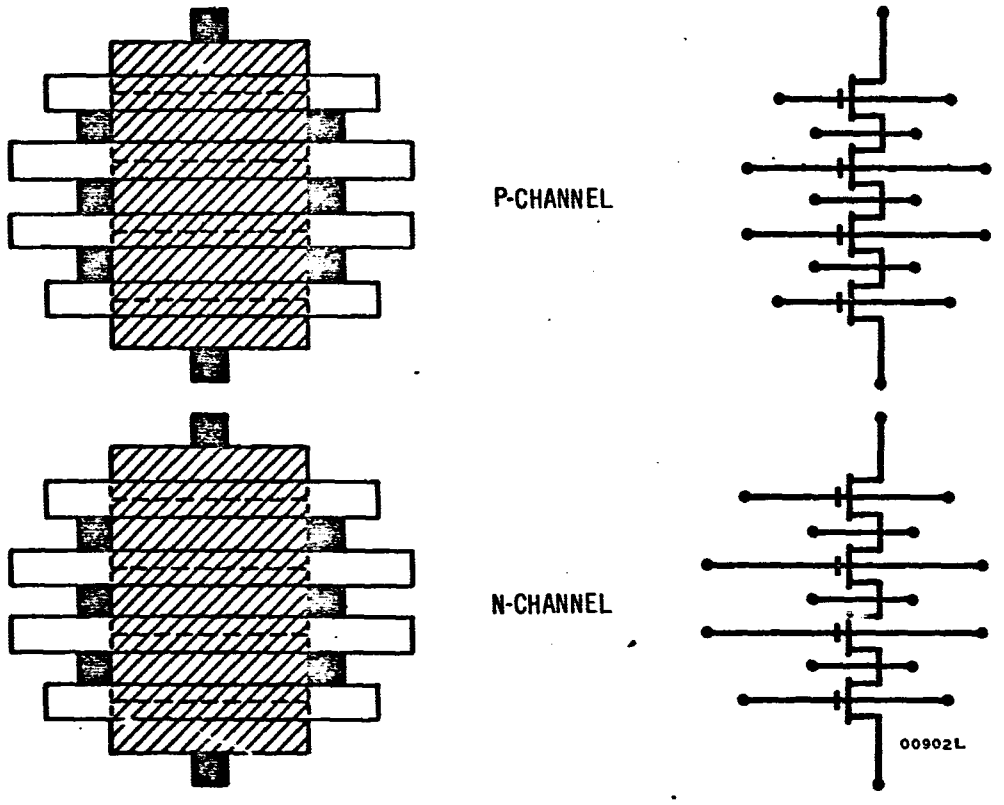

Figure 3. COS/MOS Cell

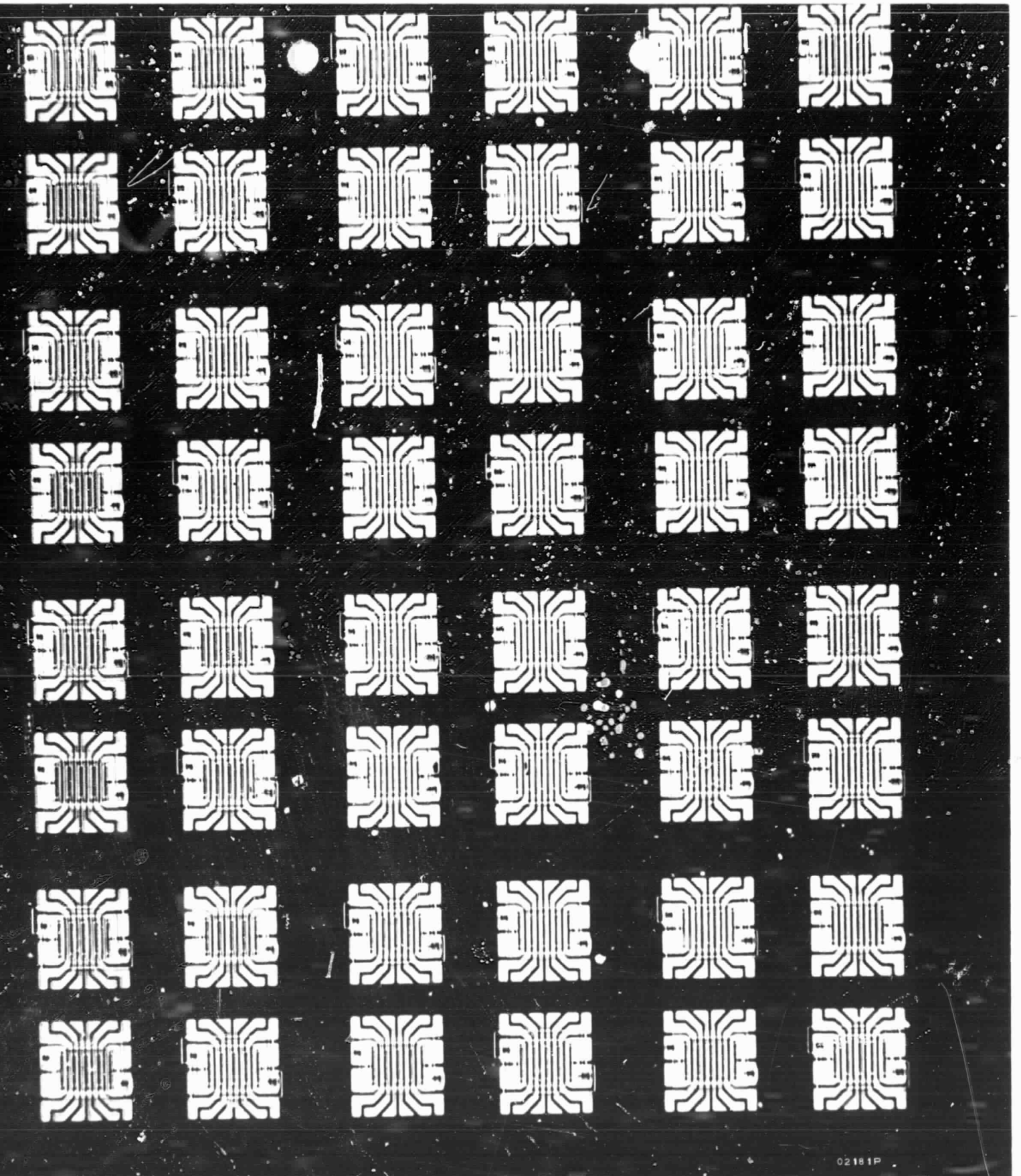

Figure 4. Inventoried Universal Wafer

arrangements of the dual inverter are shown in Figure 5. Figure 6 shows typical V-I characteristics for both p-channel and n-channel devices of a universal wafer cell. Table I contains a list of measured electrical characteristics of the universal wafer devices processed during this report period.

TABLE I. UNIVERSAL WAFER DEVICES, MEASURED ELECTRICAL CHARACTERISTICS

Characteristic	n-Type	p-Type
Inverter pair delay (ns)		24 (10 V supply)
Stage delay (ns)		12 (10 V supply)
Threshold voltage (V)	1.0-2.5	1.5-2.0
Source-drain breakdown (V)	20	10 - 20
g_m (μS)	1700	1500
Effective surface mobility (μ)(cm^2/V-s)	260	340

These measured electrical characteristics demonstrate the feasibility of the basic processing of the universal cell.

E. J-K FLIP-FLOP

A group of J-K flip-flops were fabricated in which two cells and single-layer metalization were used. Approximately one-third of the units in the bonded group were completely operational; the rest were partially operational. Some units were operated at frequencies as high as 2 megahertz. Standby power was about 20 microwatts. Figure 7 shows the metalization pattern of the J-K flip-flop.

Figure 8 shows the circuit of the J-K flip-flop. Table II illustrates the operation of this J-K flip-flop. Assume that the flip-flop is in the set state (i.e., output T is in the "1" state (+V) and output C is in the "0" state (0V). The gate of transistor N5, therefore, is charged to +V, and the gate of transistor N2 is at 0 volt. When K goes into the "1" state (+V), transistor P4 turns off and transistor N6 turns on. Since the gate of transistor N5 previously was charged to +V, this positive charge will be sustained

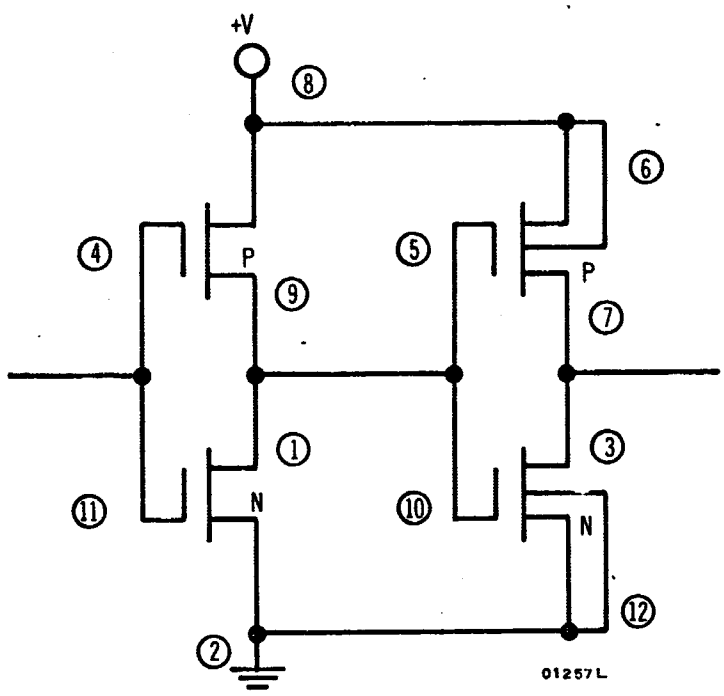

Figure 5. Dual Inverter Schematic and Pin Arrangement

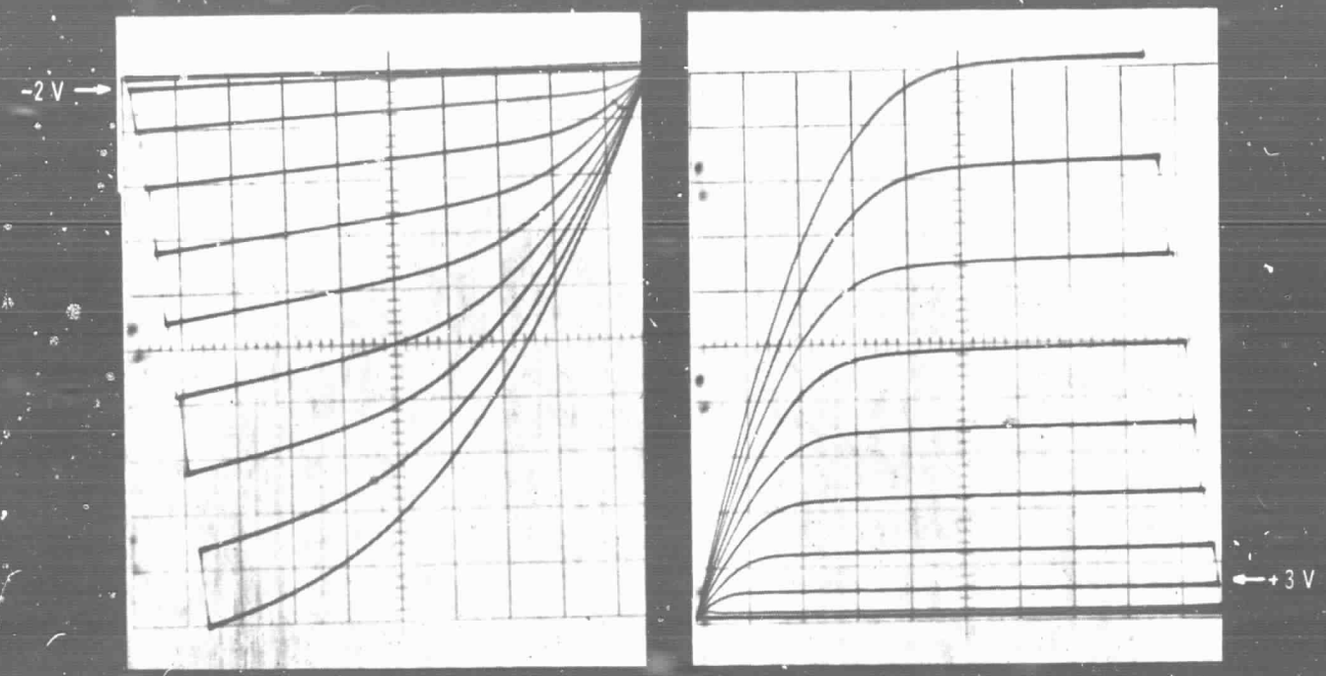

Figure 6. V-I Characteristics of Universal Wafer Devices

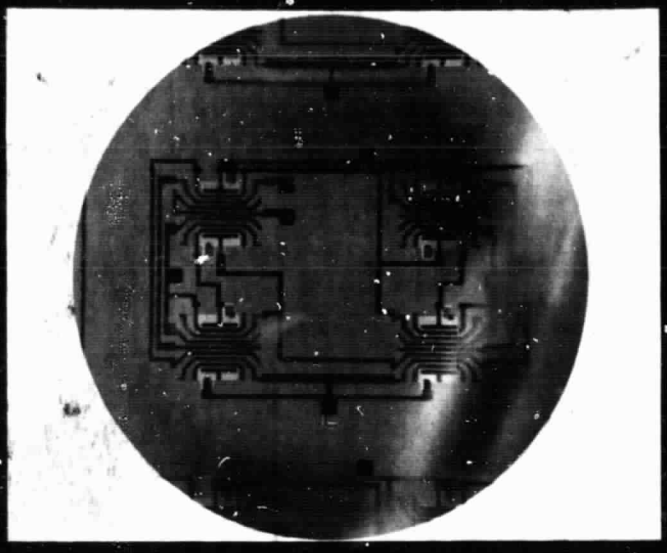

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Figure 7. Metalization Pattern of J-K Flip-Flop

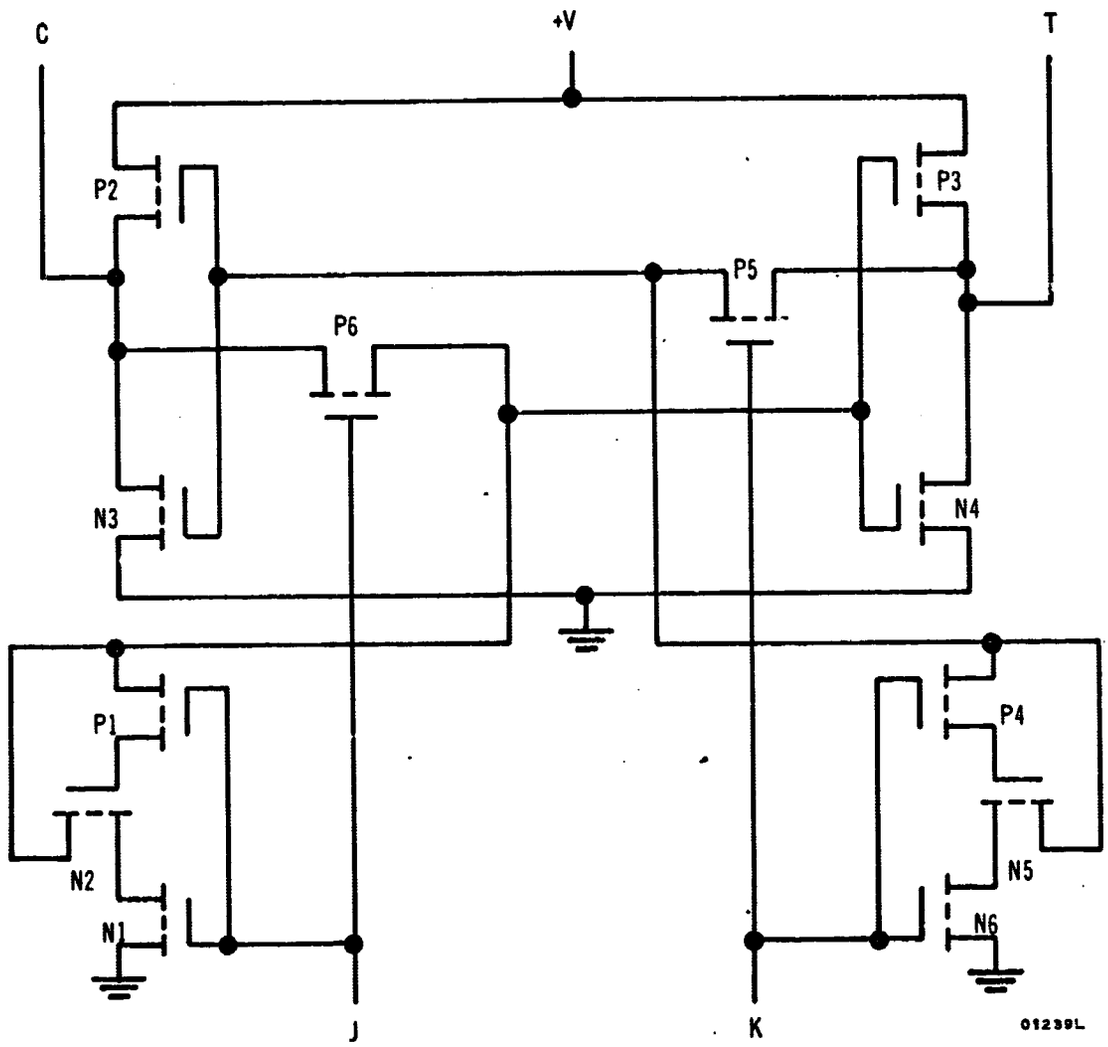


Figure 8. J-K Flip-Flop, Circuit Diagram

for a finite period of time after transistor P4 turns off. Transistor N5 will be turned on for a finite period of time, therefore, forcing output T to ground potential ("0" state) and output C to positive potential ("1" state). When J goes to the "1" state, output T similarly is forced into the "1" state and output C is forced into the "0" state. If J and K are connected together, however, a trigger flip-flop will be formed.

TABLE II

J	K	Q^{n+1}
0	0	Q^n
0	1	0
1	0	1
1	1	$\bar{Q}^n$

F. FOUR-STAGE BINARY COUNTER

The circuit developed for this program is a four-stage binary counter with a clock input, four parallel outputs, a reset, and four parallel set-inputs gated in by a "set enable" signal. The circuit can be used as a general purpose four-stage binary counter that can be set into any one of the 16 different possible states. The circuit also has reset capability. Each stage of this four-stage binary counter consists of 30 MOS transistors. The counter, therefore, has a total of 120 MOS transistors.

Figure 9 is the circuit diagram of a basic stage of the four-stage binary counter. The stage consists of two flip-flops and a number of transmission gates. Inverter P7 and N7, inverter P8 and N8, and transmission gate P6 and N6 constitute the first flip-flop. Inverter P11 and N11, inverter P15 and N15, and transmission gate P10 and N10 constitute the second flip-flop. The clock pulse controls transmission gates P9-N9 and P5-N5, either to transfer information from the first flip-flop to the second or vice-versa. If the clock pulse is at ground potential, the second flip-flop is locked, because transmission gate P10-N10 is conducting. Information, therefore, is transferred from the second flip-flop to the first flip-flop, because transmission gate P5-N5 conducts and P6-N6 is open. Information at the

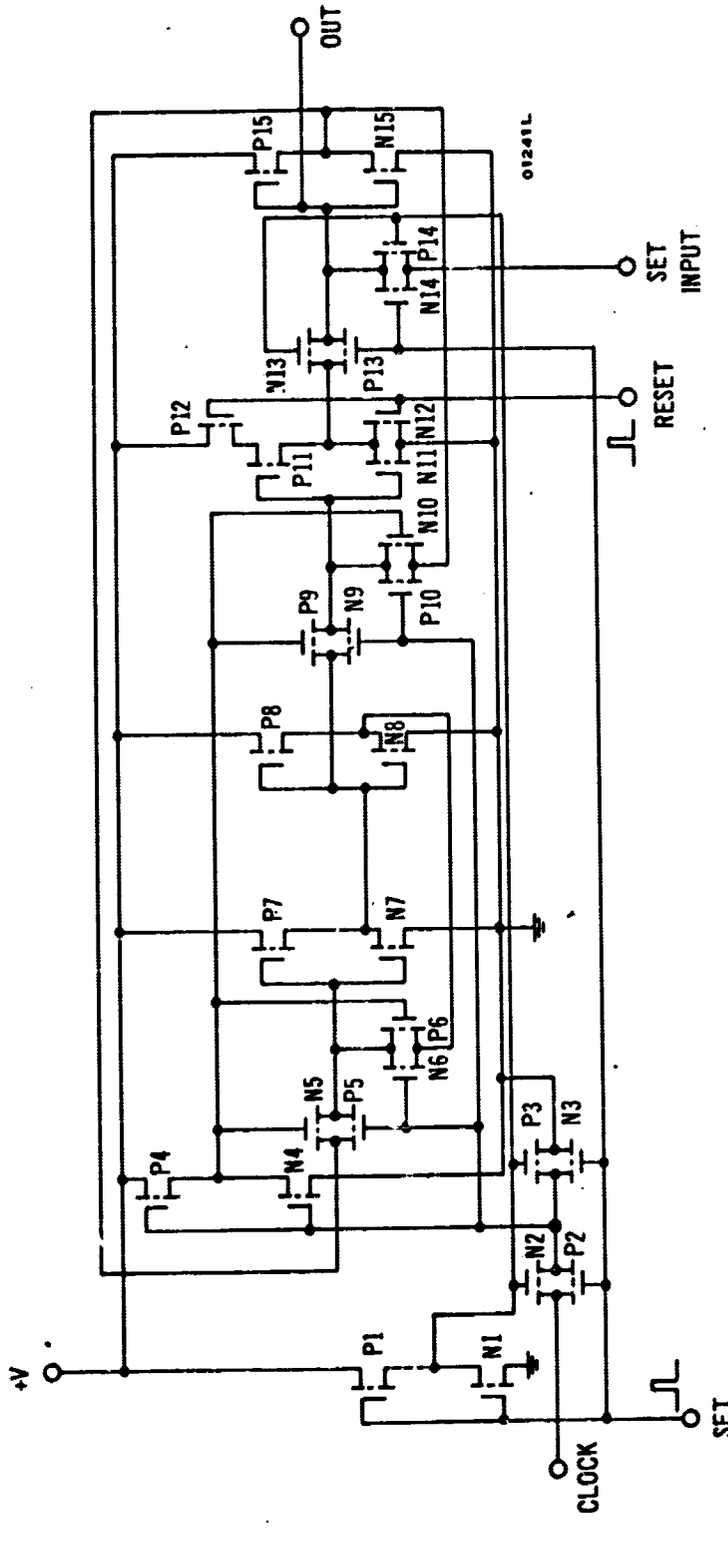


Figure 9. One Stage of Binary Counter Circuit

output of the second flip-flop also is transferred to the clock-pulse input of the following stages. When the clock pulse goes positive, the first flip-flop is locked, because transmission gate P6-N6 is conducting. Information is transferred from the first flip-flop to the second flip-flop, because transmission gate P9-N9 conducts and P10-N10 is open. As the clock pulse returns to ground potential, the information from the first flip-flop is locked into the second flip-flop. Every complete cycle of the clock pulse, therefore, sets the second flip-flop into a new state.

The "set enable" signal normally is at ground potential, and clock pulses are transmitted through transmission gate P2-N2. If the counter stage is to be set into a particular state, however, which is determined by the "set input" signal, the "set enable" signal goes to the positive potential and transmission gate P2-N2 opens; thus, clock pulses are being cut off. Transmission gate P13-N13 opens and P14-N14 conducts, which forces the output of the stage to the same potential as the "set input" signal.

Each counter stage also has two reset transistors, P12 and N12. The reset signal normally is at ground potential (i.e., P12 is on and N12 is off). When the counter stage is being reset, the reset signal goes to the positive potential: P12 is turned off and N12 is turned on. The output of each stage, therefore, is being reset to ground potential.

The four-stage counter circuit consists of 120 transistors, requiring eight basic cells. It occupies an area 80 mils by 150 mils. Figure 10 shows the metalization pattern for the four-stage counter. This counter, which has a two-layer metalization, has been fabricated successfully. The IC operates at frequencies up to the range of 5 megahertz. Figure 11 shows operational waveforms for the integrated counter operating with the "set enable" signal. Figure 12 shows the variation of circuit power dissipation as a function of operating frequency for both 10-volt and 6-volt supply operations.

The IC of the four-stage counter is packaged in a 12-lead TO-5 can. Due to the limitations of available pins on the package, the counter reset is

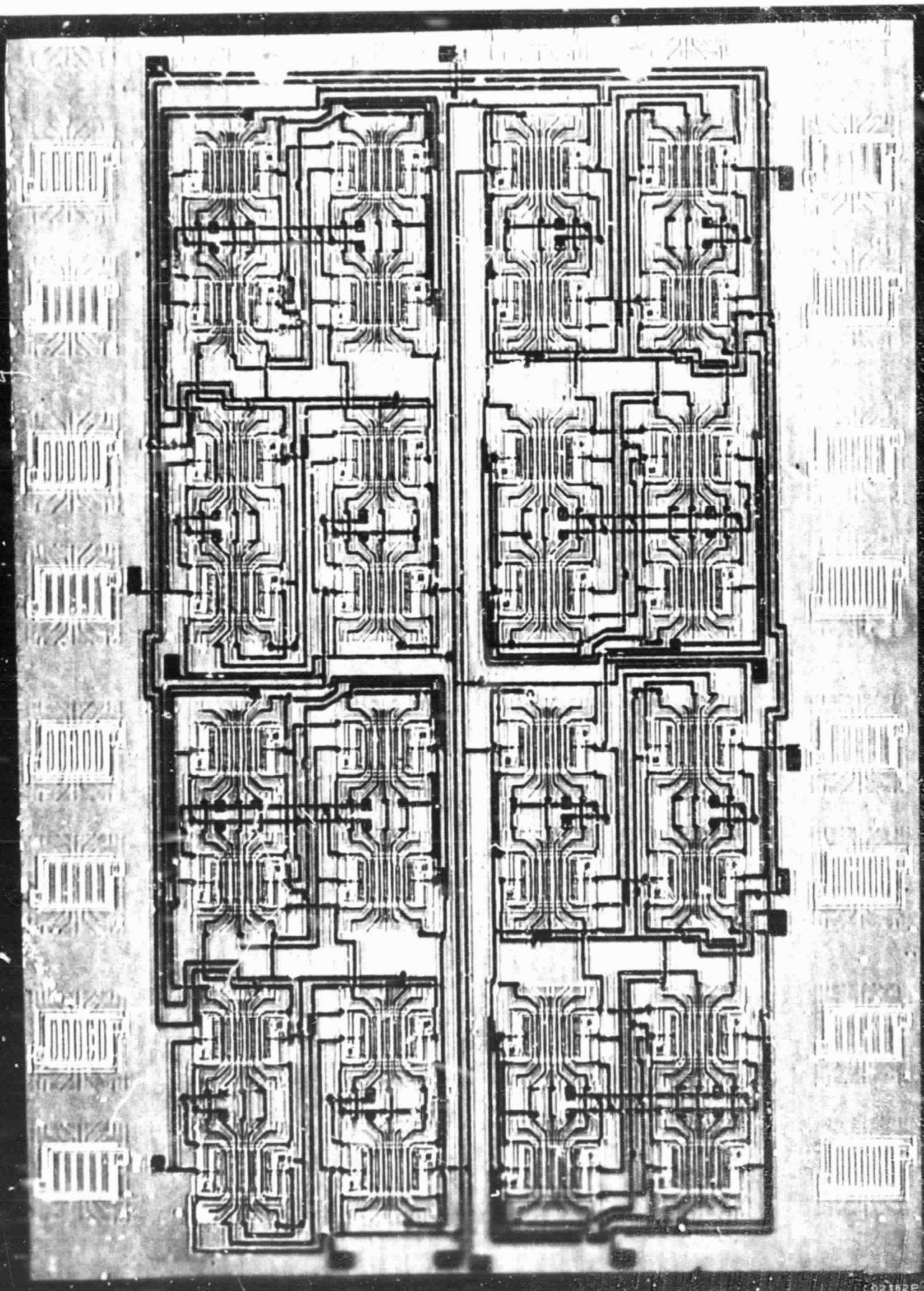


Figure [illegible] ...ation Pattern of Four-Stage Counter

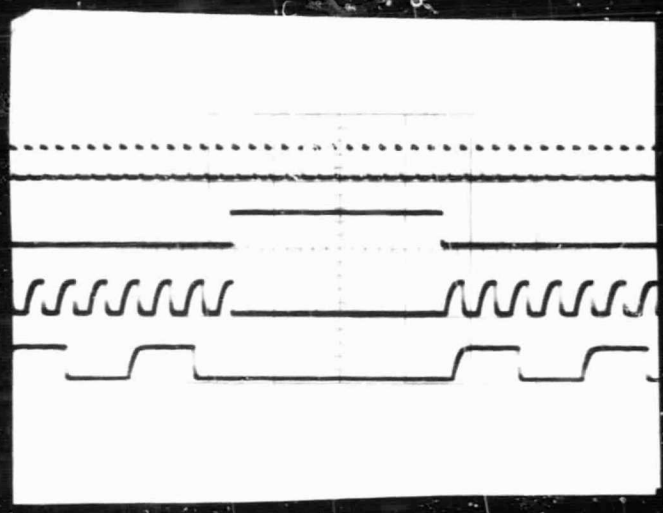


Figure 11. Operational Waveforms of Integrated Four-Stage Counter

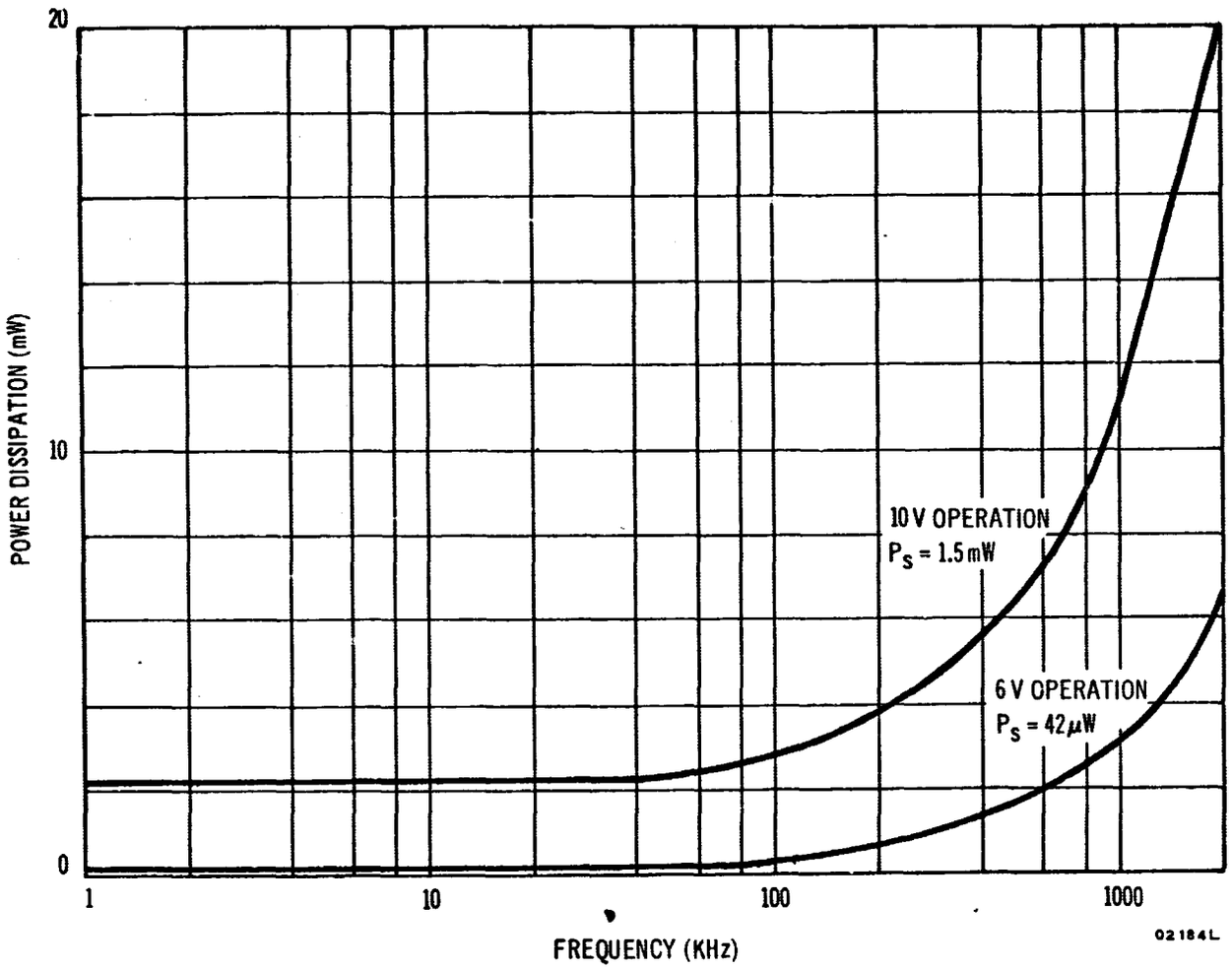


Figure 12. Four-Stage Counter, Frequency versus Power Dissipation

being grounded. Figure 13 shows the block diagram and pin arrangement of the four-stage counter.

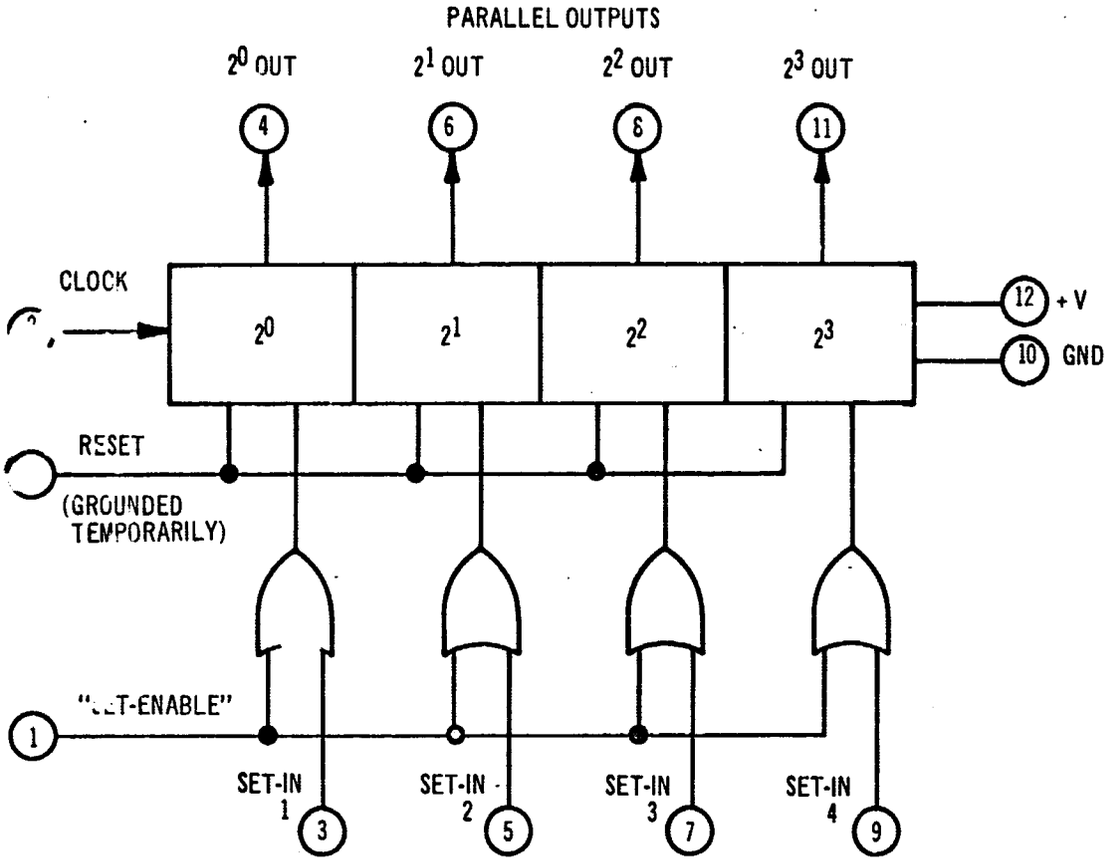
G. TWO-LAYER METALIZATION

A set of test masks was made to evaluate metallic crossovers required for the universal arrays. The test pattern was divided into two parts. One part of the mask was used to make the following evaluations of the contact between two metal layers: actual metal layers; openings in the insulator between metal layers (vias for making contact); and effects on the metal of etching and heat treatment. The second part of the mask was used to form crossovers of different sizes for evaluation of the oxide properties. The first-layer metal pattern is shown in A, Figure 14. A large bus runs down the center of the first part to facilitate contacting a series of auxiliary conductors. The auxiliary conductors vary in width from 0.1 mil to 1.0 mil. An auxiliary conductor consists of five segments that are connected together by the second-layer metal. This pattern requires eight contacts along its length to complete the conductor. The second part of the first-layer metal pattern consists of metal strips that are 0.5 mil, 1.0 mil, and 2.0 mil in width. These strips are used to form the bottom plate of a capacitor, which will be used to test the insulator that separates the two metal layers.

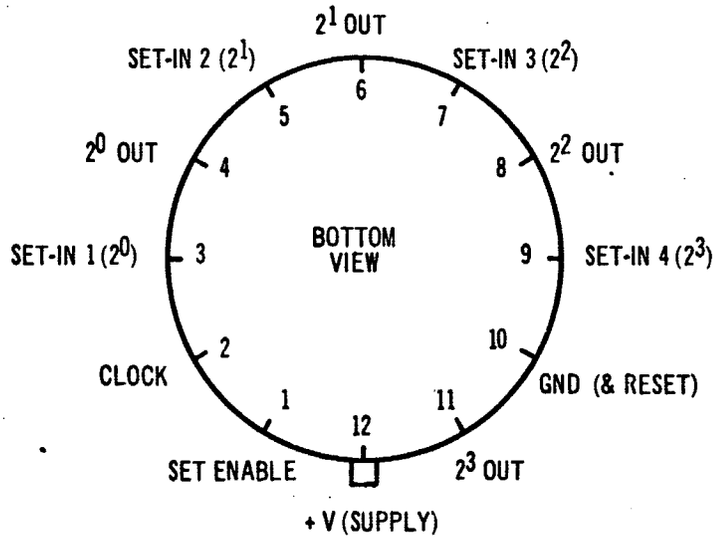
The second-layer metal pattern is shown in B, Figure 14. The upper part consists of four segments of metal in each auxiliary arm. These segments are used to join the five segments on the first-layer metal pattern. The metal strips in the lower part of the pattern form the upper plates of the capacitor for testing the insulator. The completed test pattern is shown in C, Figure 14. The completed test pattern includes the two layers of metal and the openings in the insulator. The openings are necessary for probing and contacting of the two metal layers.

The crossover test pattern was fabricated in the following sequence:

Step	Action
1	Clean wafer.
2	Grow 2000Å of oxide (thermal growth in O_2 ambient).

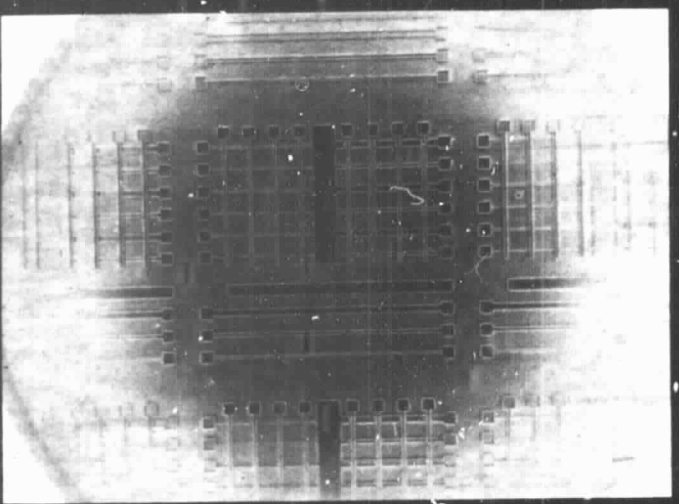


A. BLOCK DIAGRAM

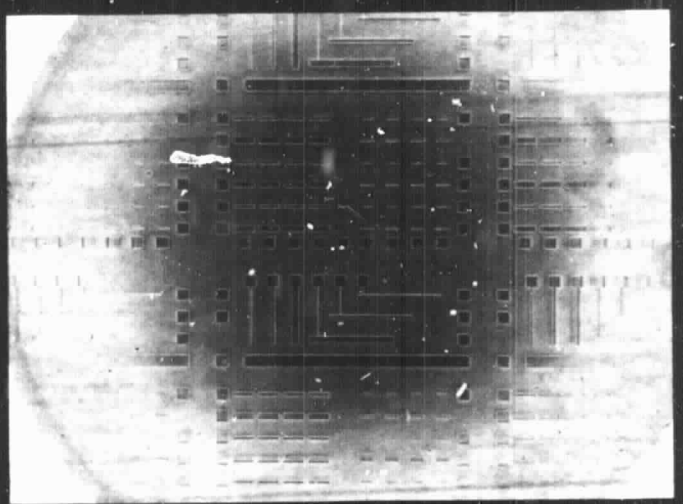


B. PIN ARRANGEMENT

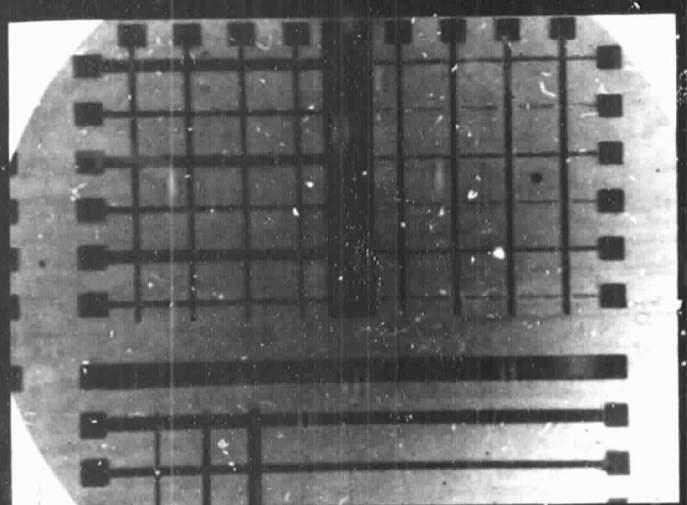
Figure 13. Four-Stage Counter, Block Diagram and Pin Arrangement



A. FIRST-LAYER METAL PATTERN



B. SECOND-LAYER METAL PATTERN



C. TWO-LEVEL METAL PATTERN

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Figure 14. Test Masks for Evaluating Crossovers

3	Evaporate 8000Å of aluminum.
4	Define and etch first-level metal pattern.
5	Deposit 4000Å of SiO_2.[1]
6	Define and open vias in oxide.
7	Evaporate 8000Å of aluminum.
8	Define and etch second-layer metal pattern.

Resistance measurements were made on the 0.5-mil segmented conductor. This size is of particular interest, because a 0.5-mil conductor is used in all circuits designed for use on the universal chip. The vias in the 0.5-mil arm are 0.4 mil by 2.5 mils. Narrower conductors were not measured because of the difficulty in reproducing reliably the contact between metal layers. Measurements along the length of the 0.5-mil segmented conductor yielded resistances from 100 to 500 ohms, or 13 to 63 ohms per via.

Metal layers separated by SiO_2 were capable of sustaining 200 volts across the oxide. Breakdown voltages above 200 volts were not determined.

The contact resistance between adjacent metal layers is believed to be caused by aluminum oxide that is formed on the surface of the first-layer metal. Postmetalization heat treatment was used in an attempt to reduce the oxide. For a 15-minute bake at 450°C in an inert atmosphere, the resistance was reduced only slightly; however, the breakdown voltage between first-layer metal and substrate was reduced, with breakdowns occurring from 120 to 160 volts. There seemed to be no correlation between linewidth and breakdown voltage. Breakdown between the two metal layers still was greater than 200 volts. It appears that the advantage of reduced contact resistance is negated by the diffusion of aluminum through the SiO_2, which reduces the breakdown voltage. Longer or higher-temperature heat treatments, therefore, would do little to improve the situation.

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[1] The deposition technique is described by Goldsmith, N. and Kern, W., "The Deposition of Vitreous Silicon Dioxide Films from Silane," RCA Review, 28, 153 (1967).

An alternate approach to reducing contact resistance was to remove the oxide from the first-layer metal. After removing oxide for the vias, the exposed metal was etched for 30 seconds in phosphoric acid (the etch used for defining metal patterns). The second layer of metal was deposited immediately. The resulting resistance was reduced, and resistance per via was in the range of 3 to 8 ohms. These values are sufficiently low to permit proper operation of the circuits designed for the universal chip. These results are summarized in Table III.

H. DESIGN OF BASIC CELL AND MASKS

The cell of the first design (A, Figure 15) consists of two blocks of four series-connected transistors. One block has four p-type MOS transistors and a contact to the n-type substrate; the other block has four n-type MOS transistors and a contact to the boron-diffused p-type substrate. The transistors have channels that are 5 mils wide and 0.3 mil long. The metalization of one block is 11 by 12 mils. The cell occupies an area 30 mils by 42 mils for eight transistors, or ~6100 transistors per square inch. The spacing was chosen to accommodate the most complex interconnection pattern; however, the spacing has been found to be overly conservative.

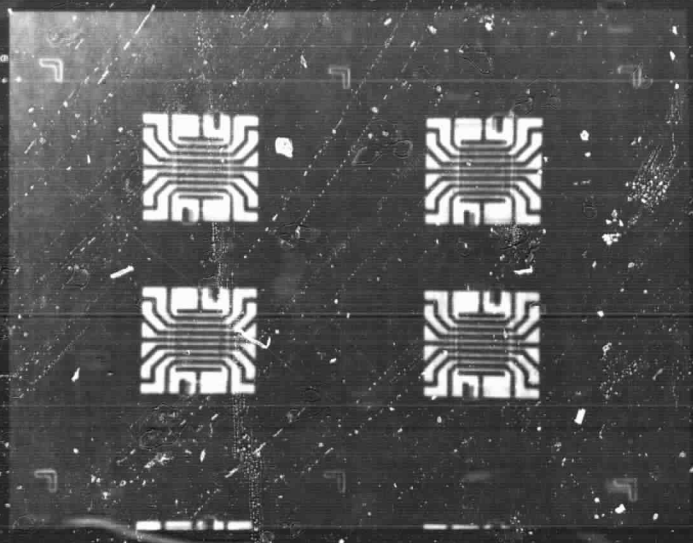
This preliminary cell was used for making breadboard units, dual inverters, and a J-K flip-flop. With the advent of successful two-layer metalization, the cell size could be reduced to use space more efficiently. A new cell was designed (B, Figure 15) in which the building blocks used were the same as the original cell, but with two blocks of four p-channel transistors and two blocks of four n-channel transistors. The transistor density of the resulting cell was increased to more than 12,000 per square inch. One other change that facilitates more efficient interconnection is the alternation of p-channel and n-channel transistors in a row. Adjacent rows of transistors in the original cell are of opposite-conductivity types. Transistors of the same conductivity type in the new cell form a checkerboard pattern. The basic cell, which now contains 16 transistors, occupies an area 35 mils by 38 mils.

A unique feature of the universal-cell approach, as opposed to custom-designed circuits, is that photomask operations for the basic cell and for the

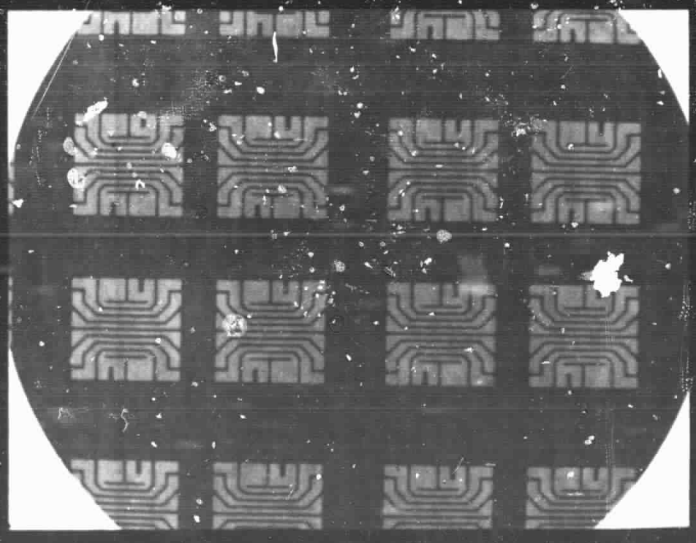
TABLE III. EFFECT OF METALIZATION TREATMENTS ON CONTACT RESISTANCE

Metalization Treatment	Resistance per Contact* (Ohms)
450°C bake in argon after second-layer metal is etched	13 to 63
Light etch of first-layer metal before second-layer metal is evaporated	3 to 8

*Resistance between two metal layers with contact area of 0.4 mil by 2.5 mils.



A. ORIGINAL LAYOUT



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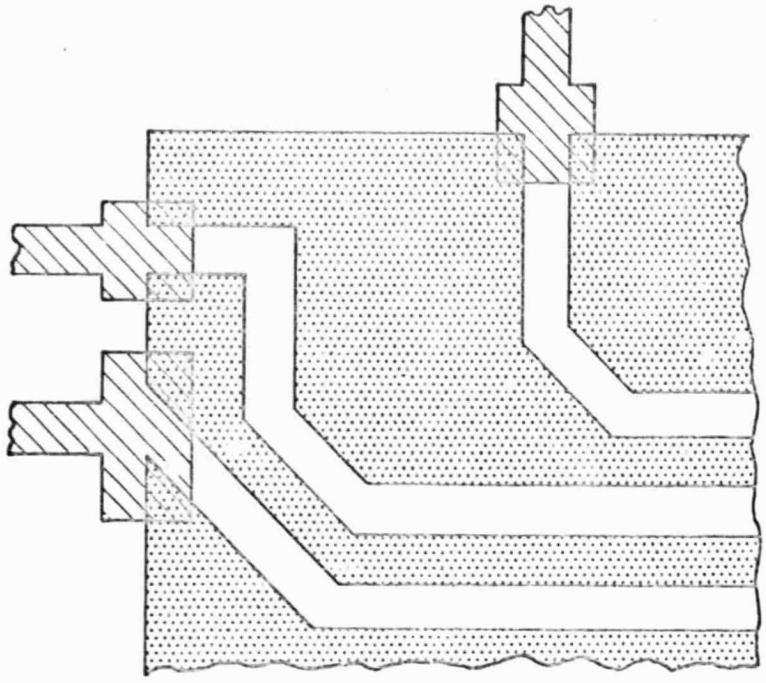
B. NEW DESIGN

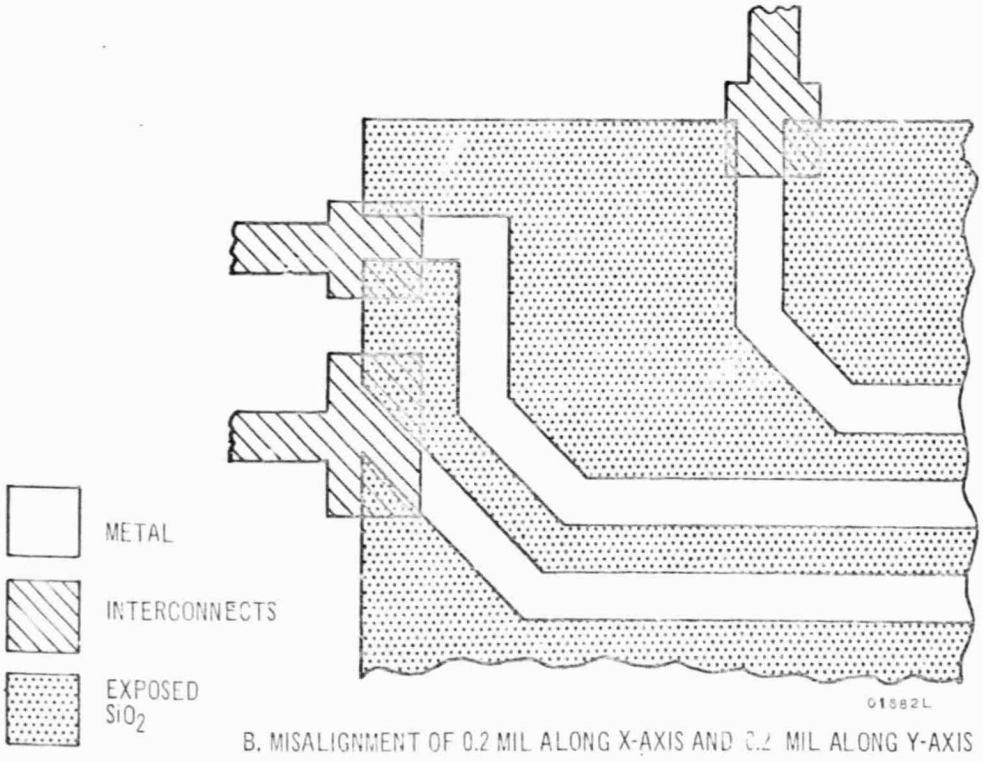
Figure 15. Basic Cell of Universal Chip

interconnections necessary to form a desired circuit are performed at different times. As a result, allowance must be made for positional errors in the interconnecting lines relative to the transistor electrodes. On a given mask, the spacing between two lines can be held easily to 0.00005 inch within a region the size of the basic cell. The positional accuracy of a given point on a pattern repeated multiple times, however, may be in error by ±0.2 mil relative to a similar pattern that is run independently. To accommodate this type of alignment error, the basic cell was designed to allow a tolerance of ±0.5 mil in the X and Y directions between corresponding connection points on the interconnect pattern and the basic cell. This tolerance is achieved by terminating an interconnection line with a metal pad that is larger than the interconnect line and by judicious placement of the leads from the transistor electrodes on the basic cell.

The basic cell with interconnecting lines overlaid is shown in A, Figure 16. The alignment is correct in this view. The same pattern is shown in B, Figure 16 with the interconnects shifted 0.2 mil along the X-axis and 0.2 mil along the Y-axis. During the first metal etch, in which the transistor electrodes are defined, the metal is removed from the region shown shaded in B, Figure 16. During the second metal etch, in which the interconnections are defined, the metal is removed from the region shown unshaded in A, Figure 16 (except the metal on the transistor). Even with this large misalignment, there is sufficient metal remaining to make proper connections to the transistors. If mask-to-mask positional accuracies are improved, the tolerance on alignment can be reduced, the size of the basic cell can be decreased, and a further space saving can be realized.



A. PROPER ALIGNMENT



B. MISALIGNMENT OF 0.2 MIL ALONG X-AXIS AND 0.2 MIL ALONG Y-AXIS

Figure 16. Alignment of Interconnections for Basic Cell

SECTION III
CONCLUSIONS

The pattern for COS/MOS universal wafer cells, including the two layers of metalization, have been developed, and reasonably successful results have been demonstrated. The basic cell consists of two blocks of four series p-channel transistors and four series n-channel transistors. These devices have a channel width of 5 mils, a channel length of 0.3 mil, and an oxide thickness of 1000Å over the gate area. Each cell occupies an area approximately 35 mils by 38 mils. A process for two-layer metalization was developed under this contract, the typical contact resistance of which was in the range of 0.7 ohm per square mil. The metalization that contacts the cell can have a ±0.5-mil tolerance with respect to the cell-interval metalization.

Two circuits were fabricated and tested with single-layer metalization: the dual inverter circuit, using one basic cell, with a stage delay of 12 nanoseconds; and the J-K flip-flop, using two cells operated at frequencies as high as 2 megahertz.

A special four-stage counter circuit was designed, fabricated, and tested for this contract. The circuit requires two-layer metalization and eight cells. The chip area is 150 mils by 80 mils. This integrated counter circuit operates at frequencies up to the range of 5 megahertz.

SECTION IV
RECOMMENDATIONS

To achieve full utilization of the program for a universal wafer, the procedure shown in the flow diagram, Figure 17, must be developed, including the generation of artwork. When the functions shown in the flow diagram have been developed fully, the resulting digital system can be used for rapid design of arrays. The vendor, therefore, can supply a particular circuit to a customer with low- and medium-quality requirements in minimum time. Some of the functions shown in Figure 17 have been developed completely or partially; other areas require intensive work.

The flow diagram of Figure 17 starts with an input, a set of logic equations restricted by the library of circuit topologies related to the logic, and the limiting design algorithms. The computer receives the input logic set, relates the logic set to the library, positions the logic set relative to the topology of cells, and determines the routing path. The routing then is tested logically and is checked against the input logic. A logic test procedure also is generated. The circuit then is analyzed for transient response. A basic problem occurs at this point if the worst-case transient response path is not acceptable. The computer can be instructed to look for another routing diagram. To use reasonable computer times and memory space, the routing algorithms usually are limited. If the transient analysis is acceptable, the artwork test program is generated and circuits are fabricated, as shown in blocks A through F and M through O.

The COS/MOS process for blocks A, M, N, and O of Figure 17 were developed during the past two years. Under the universal wafer program, a basic universal cell was designed and fabricated. Using this basic cell, circuits with both single-layer and two-layer metalization can be fabricated and tested successfully. Blocks B, C, D, E, and F of Figure 17, therefore, also were developed. Since several circuit vehicles were fabricated using the universal

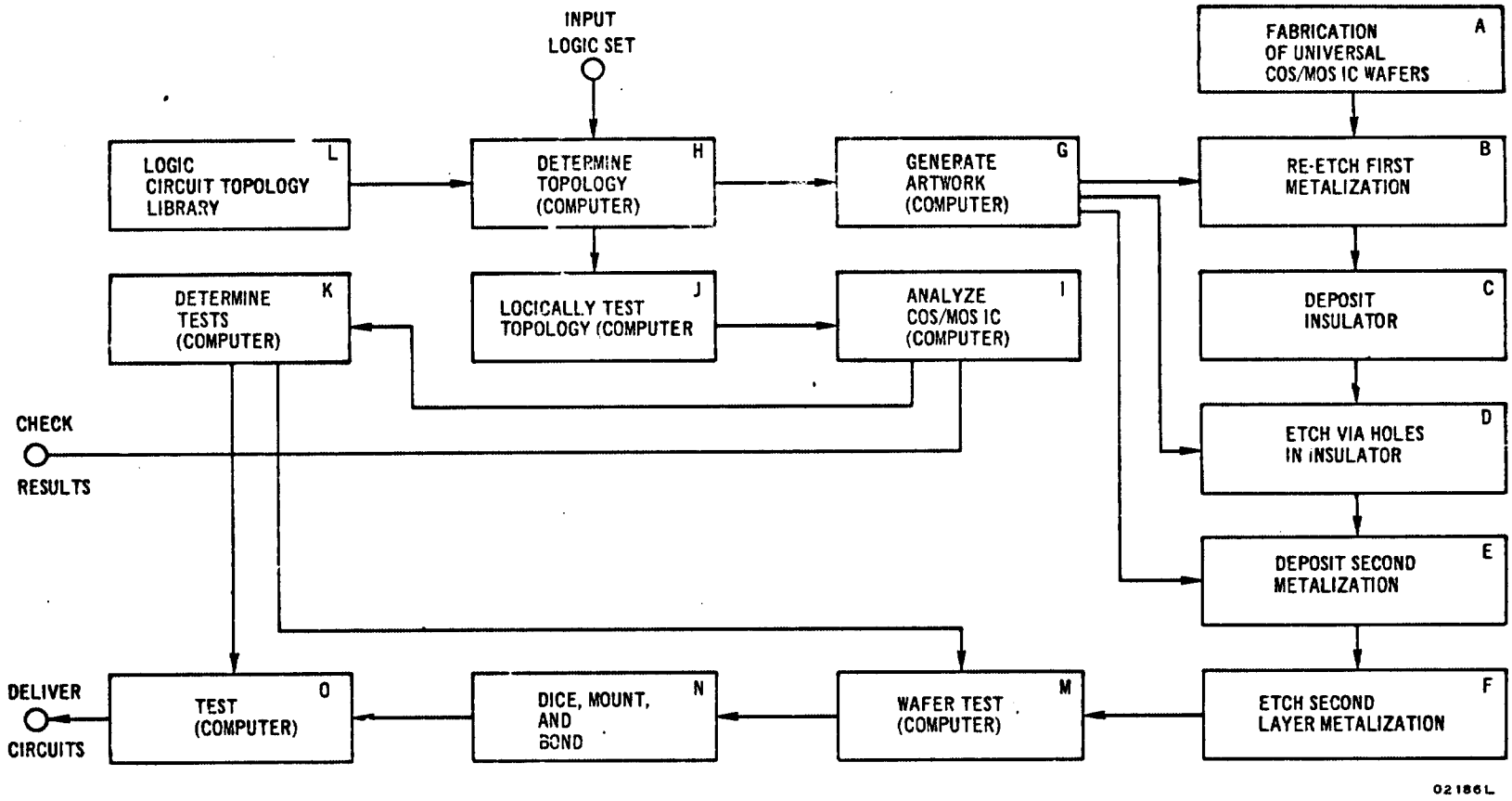


Figure 17. Flow Diagram for COS/MOS Universal Wafer Design

wafer approach, a small portion of the logic library (block L of Figure 17) has been generated. A general-purpose COS/MOS computer analysis program currently is being developed, and some of the work required for block I is in process.

Although much work has been done, the attractiveness of the universal wafer approach demonstrated that much work is required before NASA engineering personnel can make full use of the universal wafer approach. A basic library of circuit topologies first must be determined and tested, perhaps in breadboard form. The software for block H must be developed. Using the work already accomplished, artwork must be generated that is compatible with the software for block H. Compatible logic testing and COS/MOS analysis must be developed, as well as compatible hardware for testing and probing wafers. Although fabrication has been successful, it is believed that redesign of the basic cell can give greater silicon area economy because of the tighter tolerances allowed by the newer optics used in mask fabrication. In the present design, there is a wide tolerance of ±0.5 mil between the final metalization and the inventoried wafer metalization. A tolerance of ±0.1 mil is possible, however, when the inventoried wafer and the final metalizations use the same optical system and reduction ratios.

The additional work required would involve considerable effort. The following reasonable plan of action is recommended:

a. Develop a library of circuits for computer operation.

b. Based upon this library and projected optic tolerances, design the basic universal cell with less area.

c. Investigate a compatible analysis program, and demonstrate on an appropriate vehicle.

d. Investigate the computer software problem of determining topology. Recommend basic methods of developing software for routing and determining topology that are compatible with overall system objectives. This effort would include investigating areas such as the Banning approach (the DOD-sponsored program on the p-type MOS IC design system) to determine its application to this system.

APPENDIX
NEW TECHNOLOGY

COS/MOS UNIVERSAL CELL

The COS/MOS universal cell developed under this contract is described in pages 7 through 9.

COS/MOS COUNTER CIRCUIT WITH GATING

The counter circuit developed under this contract is described in pages 15 through 22.

ADDENDUM TO
FINAL TECHNICAL REPORT

DESIGN AND DEVELOPMENT OF A DIGITAL SUBSYSTEM EMPLOYING N- AND P-CHANNEL MOS FET's IN COMPLEMENTARY CIRCUITS IN AN INTEGRATED CIRCUIT ARRAY

Contract No. NAS 12-119

Tests performed by Mr. R. Lesniewski, NASA/Goddard Space Flight Center, indicated a problem in the original four-stage binary counter. This problem subsequently was confirmed by tests at RCA Electronic Components, Somerville, New Jersey.

When information was gated into the set input, the respective counter stage was set. When the set-in enable signal was removed, however, the stage changes to another state if the clock input was at the +V potential. This problem was not encountered during tests of the IC, because operating tests were limited to the following tests: counting; and set with the set-enable signal "on."

The circuit was re-examined, and the circuit design was found to be in error. Details of the problem and of the circuit redesign follow.

The original circuit (Figure 1), which is a down counter, changes state on the positive-going edge of the clock signal. During set-input operation, the set-in enable signal is on (+V); transmission gate P2-N2 opens and transmission gate P3-N3 closes, forcing the internal clock line (i.e., gates of P4 and N4) to ground potential. Transmission gate P13-N13 opens and transmission gate P14-N14 closes; therefore, the output of the counter stage is set to the state of the set-input signal. If the set-input signal is a "1" (+V) and the "1" is the clock input of the following stage, the internal clock line of the second stage (i.e., gates of P4 and N4 of the second stage) encounters a positive-going signal as the set-in enable signal returns to ground, because gate P3-N3 opens and gate P2-N2 closes. As a result, the second stage changes state; similarly, the third and fourth stages will change state if the second

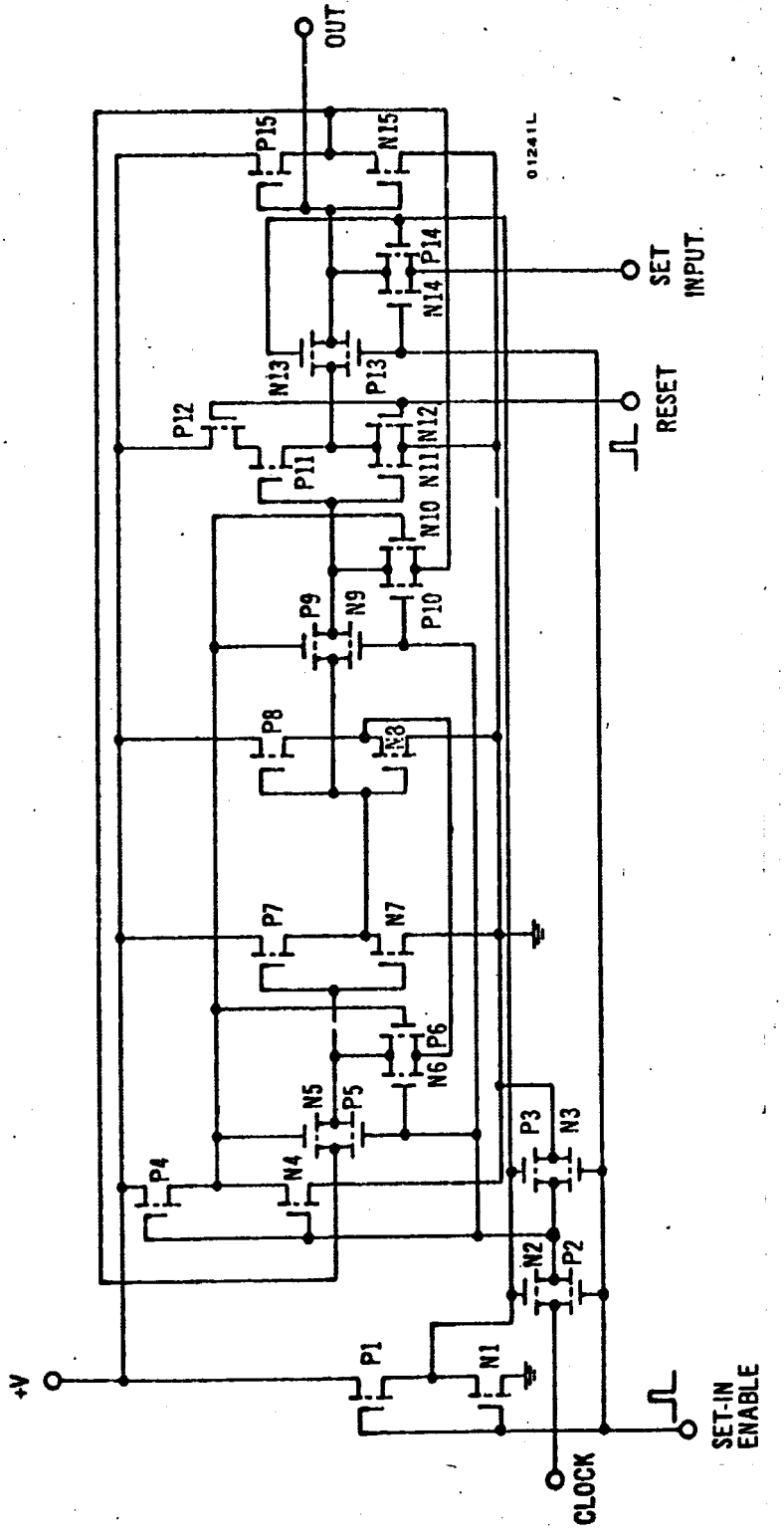


Figure 1. Original Counter Circuit

stage and third stage, respectively, were set into the "1" state. During set-input operation, therefore, the clock input of every stage must be at ground potential. The result is that this four-stage counter can be set only into the 0000 state or the 0001 state.

The redesigned counter circuit is shown in Figure 2. This counter, an up counter, changes state on the negative-going edge of the clock signal. The set-input gating circuit (P14-N14 of Figure 1 and P8-N8 of Figure 2) has been transferred from the second flip-flop to the first flip-flop. During set-input operation, the set-input signal is gated in by the set-in enable signal. When the set-in enable signal is on (+V), the internal clock line (i.e., gates of P4 and N4) again is at ground potential, because transmission gate P3-N3 is on. Transmission gate P7-N7 opens, unlocking the first flip-flop and allowing the set-input signal to be transferred into the first flip-flop through transmission gate P8-N8; then through transmission gate P12-N12 to the output. When the set-in enable signal returns to ground, the first flip-flop or the second flip-flop (depending upon whether the clock signal is at ground or +V potential) will be locked. A change of state will not occur at the counter stage output, as was true in the original design. This counter circuit maintains its set state after the set-in enable signal returns to ground, therefore, and it is independent of the potential at the clock input. In addition to the changes discussed above, two transistors were added to the reset circuit of the redesigned counter stage shown (Figure 2). The two additional transistors ensure proper reset operation of the counter.

The redesigned four-stage counter has been breadboarded. Figure 3 shows operational waveforms for the redesigned four-stage counter with a 1010 code being set into the counter by the set-in enable signal. The clock signal following the set-in enable signal (i.e., second clock signal shown in Figure 3) increments the counter by a one count to 0110, the next clock pulse sets the counter to 0111, etc.. Each redesigned counter stage contains 32 transistors; the four-stage counter has a total of 128 transistors.

An alternate version of the counter circuit of Figure 2 is shown in Figure 4. The only difference is in the set-input gating circuit. Instead of placing transmission gates P7-N7 and P8-N8 at the input of inverter P9-N9,

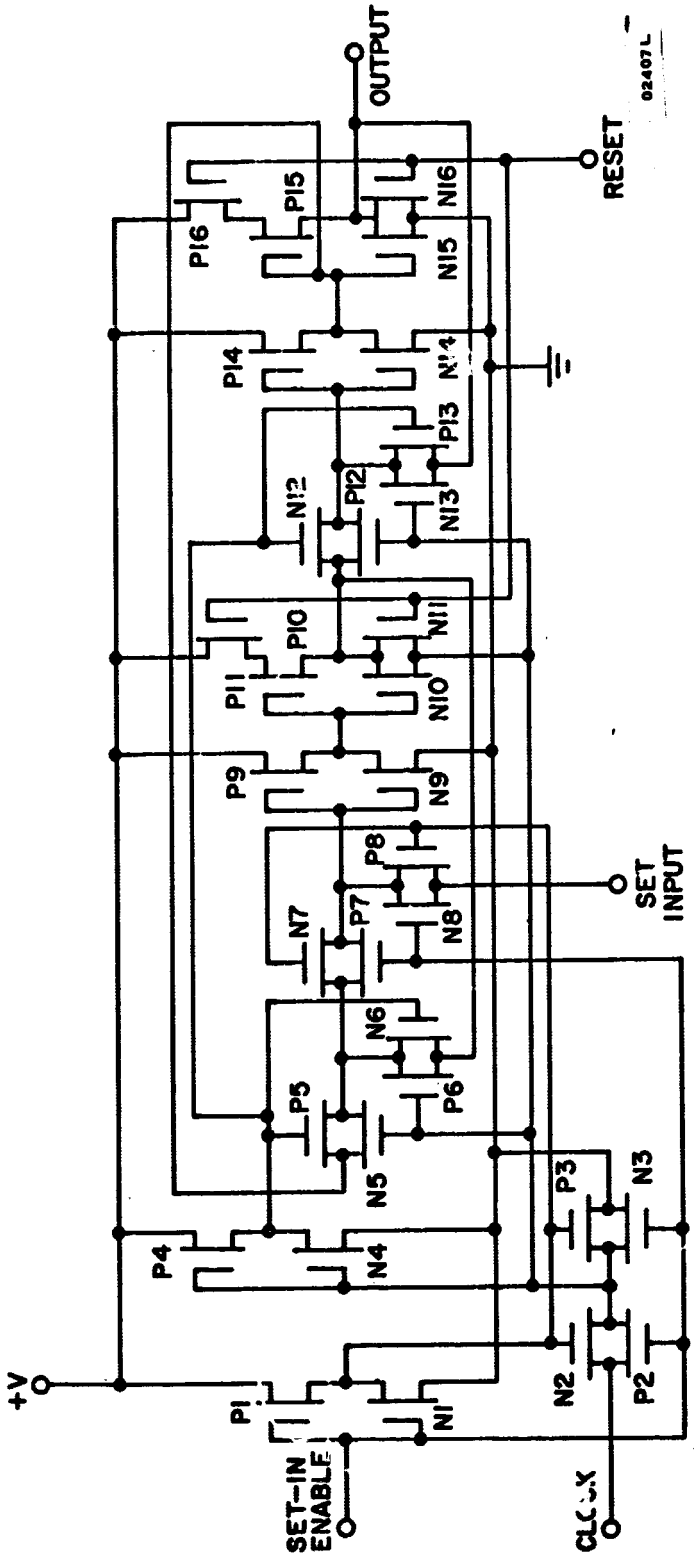


Figure 2. Redesigned Counter Circuit

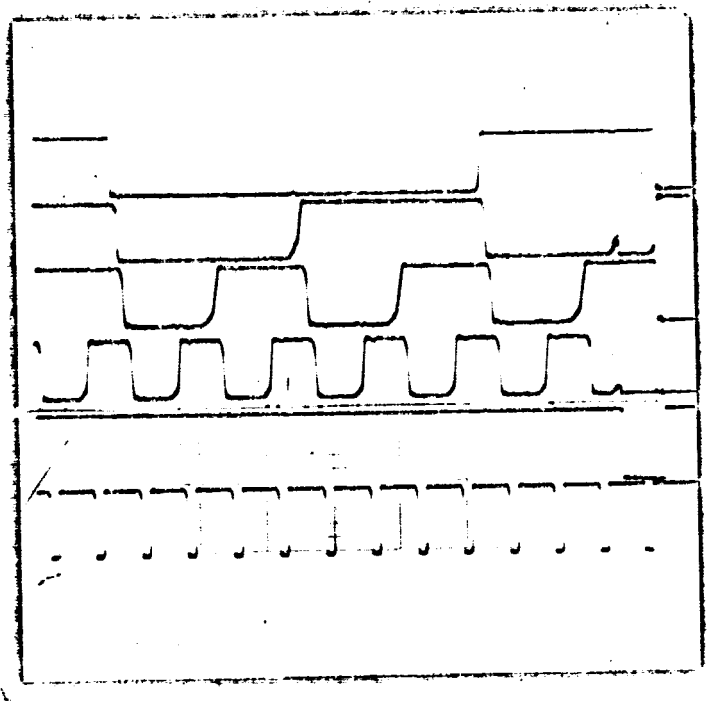


Figure 1. Operational Waveforms of Synchronous Four Stage Counter

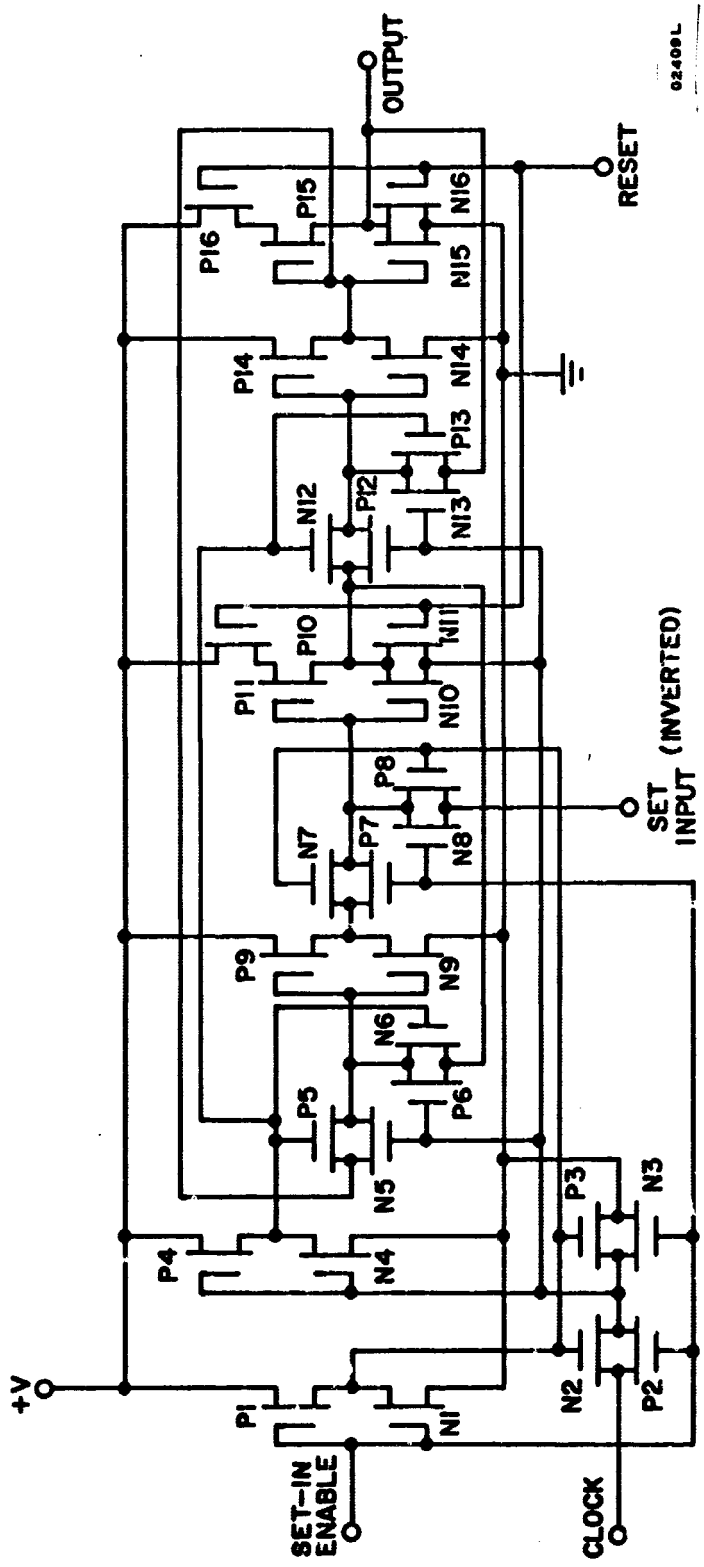


Figure 4. Alternate Version of Counter Circuit

they are placed at the output of inverter P9-N9. This configuration eliminates the arrangement shown in Figure 2 of two series transmission gates, I5-N5 and P7-N7. Two transmission gates connected in series invariably slow the circuit operation. Isolating the two transmission gates by an inverter driver improves the operational speed of the circuit. One disadvantage of the circuit shown in Figure 4 is that an inverted set-input signal is required to set the counter stage, because inversion takes places from the set input to the output of the stage.