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SUBJECT: Aerospace Digital Computer Design Trends - Case 103

DATE: January 14, 1969

FROM: D. O. Baechler

MEMORANDUM FOR FILE

Attached is a copy of "Trends in Aerospace Digital Computer Design," an article which will be published in the January 1969 issue of the Institute of Electrical and Electronics Engineers' Computer Group News.

This article updates a previous article, "State-of-the-Art of Aerospace Digital Computers, 1962-1967," which appeared in the January 1968 issue of the Computer Group News.

D. O. Baechler

1031-DOB-ml

Attachment

TRENDS IN AEROSPACE DIGITAL COMPUTER DESIGN

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INTRODUCTION

This article summarizes some of the recent trends in aerospace computer design that can be inferred from the changing characteristics of computers developed during the period 1962-1968. In an earlier paper,* characteristics of 40 computers developed during 1962-1967 were described. Since the time the earlier paper was written, at least 13 new aerospace computers have been introduced and at least 7 others are in development. This paper updates the information in the earlier paper with very little repetition. For a more detailed description and discussion of computer characteristics and how they have evolved, the reader is referred to the earlier paper.

Characteristics of the sixty computers used as a basis for this paper are given in Table 1, where the computers are listed according to their date of introduction. Table 2 provides an alphabetically listed cross-reference to Table 1. The list of computers includes those in the earlier report and is intended to be inclusive, but some computers of interest may have been omitted either because their characteristics are still considered proprietary by the manufacturer or because the information was not received from the manufacturer in time to be included.

GENERAL CHARACTERISTICS

Most aerospace computers perform parallel rather than serial operations on the computer word. Since logic hardware is built using integrated circuit (IC) techniques, the added cost of building a parallel computer becomes less important than the speed advantage that the parallel computer has over the serial computer. Therefore, general purpose machines will probably continue to be built as parallel processors, with serial machines designed only for special jobs with a low speed requirement and a need for extreme simplicity to achieve reliability.

Fixed point number representation is used in all except two of the computers listed in Table 1. As hardware

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*"State-of-the-Art of Aerospace Digital Computers, 1962-1967," D. O. Baechler, IEEE Computer Group News, January 1968.

becomes smaller, lighter and more reliable, it is likely that floating point representation will become more common since fixed point representation places a burden on the programmer and makes program validation more difficult.

There is a trend toward a larger basic instruction set, with many of the more recently designed computers having more than fifty instructions. Also, the trend is toward single address instructions with provisions for designating operand and result locations from among central processing unit (CPU) registers.

Word lengths of 12 to 32 bits have been used, with some computers using different lengths for the data word, instruction word and memory word. The trend is toward a single word length. To obtain required precision without double precision operations and to provide adequate addressing and instruction decoding, 24 or 32 bits seem to be the sizes most often used.

SOFTWARE

There is an increasing attempt to reduce the problems associated with managing large programming efforts. All of the computers have assemblers; more are also being provided with compilers, diagnostic programs and simulators that can be run on commercial machines.

There is a trend toward designing families of computers, all with the same instruction set but of different sizes and operational capability. Sometimes, the family consists of both ground and aerospace computers, and the instruction set of the aerospace computer is a subset of the ground computer's instructions.

INSTRUCTION EXECUTION TIME

The execution time for the add, multiply and divide instructions are listed in Table 1 to give an indication of machine speed. Also, add times and multiply times are plotted against calendar time in Figures 1 and 2, respectively.

Add times have decreased to a range of from 2 μsec to 5 μsec and multiply and divide times have been reduced to the point that 10 μsec to 20 μsec times are not uncommon. Figures 1 and 2 also show a tendency for the times to cluster near the low end during the most recent years, with the upper limit decreasing much more than the lower limit.

MEMORY

Computers in Table 1 have memory cycle times ranging from 0.6 μsec to 27 μsec with the range from 2 μsec to 6 μsec being the most prevalent.

While core memories are used for most of the computers in Table 1, there are two emerging technologies. A plated wire memory is offered as an option on one computer in Table 1 and it is likely that such offerings will increase.

Semiconductor memories implemented using large scale integration (LSI) techniques are used in two computers in Table 1 and their use is expected to increase. LSI memories can be implemented as read-only storage or as read-write storage, and either metal-oxide-semiconductor (MOS) or bipolar devices can be used.

INPUT/OUTPUT (I/O)

The information in Table 1 concerning I/O channels and interrupts is not uniform because not all manufacturers define "channel" in the same way and because in some cases information was taken from a computer description that did not fully explain the numbers given. Most of the computers in Table 1 have at least one external interrupt and a means for input and output of parallel digital data and discrete signals. Often a separate I/O unit is required to handle analog and serial digital inputs and outputs.

It is likely that computers will continue to be built without rigidly defined I/O, but with features that will permit the addition of I/O units designed for a particular application. Among the features that will probably be provided are direct memory access, priority interrupts with automatic multi-level program status retention, and addressed I/O to permit selection of a large number of devices.

PHYSICAL CHARACTERISTICS

Prior to 1963, the computers in Table 1 used discrete components or hybrid circuits. From 1963 until 1968, all the computers in Table 1 used bipolar silicon integrated circuits. This year represents the beginning of two changes in the hardware used. First, machines are being designed with LSI. One which is already built, the TI 2502 LSI, uses 100 to 200 gates/chip. And second, MOS technology is being used in designing a CPU. This is being done in the Autonetics D-200.

The changing hardware technology is reflected in a reduction in the characteristic size and weight of aerospace computers. An aerospace computer with an 8K memory used to be less than 1 cu. ft. in size and weighed less than 100 lbs. Now it is generally less than 0.5 cu. ft. and weighs less than 50 lbs. Characteristic power has remained at about 100 watts. It is likely that power as well as volume and weight will further decrease as LSI technology is more widely used.

RELIABILITY

In Table 1, the reliability of some of the computers is indicated by a predicted mean time between failures (MTBF). An MTBF was not available for each of the computers in Table 1, and for those MTBF's listed, the method of calculation is in most cases not described. The comments associated with Texas Instruments TI 2540 and TI 2550 begin to describe the tradeoffs in designing and building reliable equipment and also to illuminate the problem in stating an MTBF without discussing the conditions under which it was calculated. Texas Instruments builds the TI 2540 and TI 2550 for an application in which a 500 hour MTBF is adequate, and the manufacturing costs necessary to achieve this reliability result in a particular price. If high reliability--and therefore more costly--parts were used in building the computers, the calculated MTBF's would increase. If these parts were carefully screened and burned in--another costly procedure--the calculated MTBF's would increase further. And if a lower operating temperature were assumed in the calculation, the MTBF's would increase once more. While it is not difficult to predict the reliability of a system, it is difficult to meaningfully compare the reliability of several systems unless their reliabilities have been predicted under the same assumed conditions and those conditions are carefully described. Therefore, it is difficult to identify trends in reliability.

SUMMARY

A summary of the state-of-the-art in aerospace computers can be acquired from the information in Table 1. The characteristics listed below summarize the data for all the computers in the 1967, 1968 and development categories, except that serial machines are excluded as being atypical. The values for weight, size and power are for computers with an 8K memory.

CHARACTERISTIC	MINIMUM	TYPICAL	MAXIMUM
Add Times (μsec)	∿2	4-9	∿20
Multiply Times (μsec)	6	20-40	66
Divide Time (μsec)	11.4	20-60	94.5
Weight (pounds)	12	20-50	120
Size (cubic feet)	0.18	0.2-0.7	0.96
Power (watts)	20	50-200	310
Memory Size (words)	1K	4K-32K	131K

To summarize the trends in aerospace computer design, a fictitious computer of the not-too-distant future will be described based on what the author expects the trends to be. This is one of many computers that might be used to illustrate the trends. Using the format of Table 1, the description is as follows:

The manufacturer's name and nomenclature indicates that this is one of a series of machines that are available. It may even be implied in the nomenclature that it is in some way compatible with the manufacturer's ground-based computers. The date of introduction is 1971.

It is a parallel machine with floating point number representation and has 75 instructions with provisions for register-to-register operations.

The add time is 1 μsec, multiply time is 8 μsec and divide time is 10 μsec. These times are possible because of the very fast MOS memory and because of features that allow some operations to overlap.

The MOS memory has a 500 nsec cycle time. It is 4K x 32 bits and can be expanded to 32K. There is another computer in this series which has a memory that can be expanded to 131K.

There is an interrupt that has a 12-bit address associated with it to designate one of the 4096 possible interrupt sources that can be connected to the computer through a specially designed I/O unit. There are two separate channels that have direct access to the memory and there is a bus for transferring data and control words between the I/O unit and the CPU.

Bipolar LSI technology is used to implement the logic. With a 4K MOS memory, the computer weighs 20 pounds, has a volume of 0.20 cubic feet and uses 25 watts of power.

The listed MTBF is 450 days, or about 11,000 hours. It was calculated for 70° C using MIL HDBK 217B techniques but the failure rates for the LSI circuits were based on the manufacturer's own experience with these circuits. The computer also has multiprocessor capability.

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TABLE 1 - CHARACTERISTICS OF AEROSPACE COMPUTERS*

NAME DATE INTRODUCED	DATA FLOW	DATA TYPE	NO. OF INSTRUCTIONS	COMPUTING TIME, µ SEC			MEMORY						IN/OUTPUT		PHYSICAL CHARACTERISTICS				MTBF (HRS)	COMMENTS
				ADD	MULT	DIV	TYPE	WORD SIZE (BITS)	CAPACITY (WORDS) MIN	CAPACITY (WORDS) MAX	ACCESS TIME (µ SEC)	CYCLE TIME (µ SEC)	NO. OF CHANNELS	NO. OF INTERRUPTS	TYPE OF HARDWARE	WEIGHT (LBS)	SIZE (CU. FT.)	POWER (WATTS)		
1. BURROUGHS D210 PRE 1962	P	Fx	16	30	580	680	DRO CORE CORE ROPE CORE ROPE	24 16 50	256 1K 256	1K 16K 1K	 10 10	15	2	1	MAGNETIC LOGIC	19	0.25	100	7000	USES CORE NULL-DECODER REGISTERS FOR LOGIC. INSTRUCTIONS ARE 16 BITS, DATA IS 24 BITS. 50-BIT ROPE USED FOR MICROPROGRAMMING.
2. UNIVAC ADD-1000 PRE 1962	P	Fx	16	12	711	837	DRO THIN FILM NDRO THIN FILM	24 24	256 7K		3	3	16	4	DISCRETE COMPONENTS	88	1.1	262		NDRO MEMORY HAS 50 MILLISEC WRITE TIME FROM EXTERNAL EQUIPMENT.
3. ARMA MICRO COMPUTER MID 1962	S	Fx	19	27	135	324	NDRO CORE	22	2K	8K		27	2		DISCRETE COMPONENTS	20	0.4	50		REGISTERS ARE DELAY LINES. MEMORY IS TWO-APERATURE CORE
4. HUGHES HCM-201 MID 1962	P	Fx	30	6	120	120	DRO CORE OR NDRO CORE OR DRUM	24 24 24	4K 16K 1500K			6	3	1	DISCRETE COMPONENTS	51		150		CHOICE OF ONE OF THE THREE MEMORIES AVAILABLE.
5. IBM GEMINI GUIDANCE COMPUTER EARLY 1963	S	Fx	16	140	420	840	NDRO CORE	39	4K			4	5	0	DISCRETE COMPONENTS	59	1.65	85		CONCURRENT MULTIPLY/DIVIDE. 13 BITS OF MEMORY WORD ARE READ-ONLY. INSTRUCTION WORD, 13 BITS; DATA WORD, 26 BITS.
6. GENERAL PRECISION AN/ASN-24 MID 1963	S	Fx	12	624	4K	4K	DRUM	25	4K				1	0	DISCRETE COMPONENTS	100	1.2	420		HAS INDEPENDENT, PROGRAMMABLE INTEGRATOR. USES TWO ADDRESSES, OPERAND AND NEXT INSTRUCTION.
7. HUGHES HCM-202 MID 1963	P	Fx	30	6	120	120	DRO CORE NDRO THIN FILM	24 24	512 1024	4K 8K		6 6	3	1	HYBRID THIN FILM	51		150		OTHER MEMORY TYPES ARE AVAILABLE.
8. IBM SATURN IB/V LVDC MID 1963	S	Fx	14	82	328	656	DRO CORE	28	4K	32K	28		1	1	DTL HYBRID	80	2.1	138		REGISTERS ARE GLASS DELAY LINES. CONCURRENT ADD AND MULTIPLY. TWO PARITY BITS IN MEMORY WORD.
9. MIT BLOCK I AGC LATE 1963	P	Fx	11	23.4	117	210	DRO CORE CORE ROPE	16 16	1K 10K			11.4 11.4		8	DCTL IC	87	1	125		SOME I/O HANDLED THROUGH COUNTER INTERRUPTS.
10. UNIVAC 1824 LATE 1963	P	Fx	41	8	92	128	DRO THIN FILM NDRO THIN FILM	24 48	512 4K		0.7	4	8	1	DTL IC	31.5	0.47	110	10,000	DATA WORD, 24 BITS; INSTRUCTION WORD, 16 BITS.
11. BURROUGHS D84 MID 1964	P	Fx	47	6	25		DRO CORE	24	4K	32K		3			IC	166	3.6	150		WEIGHT, SIZE AND POWER ARE GIVEN FOR 4K MEMORY
12. SAAB CK 37 MID 1964	P	Fx	48	5.6	23.8	44.8	DRO CORE	26	8K		1.2	2.8	67	8	RTL IC	80	1.3	200	1850	MOST COMMON OPERATIONS USE 13-BIT INSTRUCTION WORD, WITH 13-BIT OPERAND STORED IN OTHER HALF OF THE WORD.
13. LITTON L-304 EARLY 1965	P	Fx	63	5.6	61		DRO CORE	32	4K	131K		1.8	8	1	TTL IC	34	0.26	100	2300	DATA WORD, 16 BITS; INSTRUCTION WORD, 32 BITS
14. NORTRONICS NDC-1051 EARLY 1965	P	Fx	51	8	70	176	DRO CORE	24	2K	8K	2	4	1	4	IC	29	0.5	94	8500	WEIGHT, SIZE, POWER AND MTBF ARE GIVEN FOR 2K MEMORY.
15. AUTONETICS D26J LATE 1965	P	Fx	38	8	18	18	DRO CORE	12	4K	8K		4	4	4	DTL IC	35	0.21	200	7200	24-BIT WORD OPTION IS AVAILABLE. SIZE, WEIGHT AND POWER ARE GIVEN FOR 4K MEMORY.

*SEE ATTACHED EXPLANATION OF HEADINGS

TABLE 1 - CHARACTERISTICS OF AEROSPACE COMPUTERS (CONTINUED)

NAME / DATE INTRODUCED	DATA FLOW	DATA TYPE	NO. OF INSTRUCTIONS	COMPUTING TIME, μ SEC			MEMORY						IN/OUTPUT		PHYSICAL CHARACTERISTICS				MTBF (HRS)	COMMENTS
				ADD	MULT	DIV	TYPE	WORD SIZE (BITS)	CAPACITY (WORDS) MIN	CAPACITY (WORDS) MAX	ACCESS TIME (μ SEC)	CYCLE TIME (μ SEC)	NO. OF CHANNELS	NO. OF INTERRUPTS	TYPE OF HARDWARE	WEIGHT (LBS)	SIZE (CU. FT.)	POWER (WATTS)		
16. HONEYWELL ALERT LATE 1965	P	Fx	89	4	14	32	DRO CORE	24	4K	64K	1	2	7	24	HLTTL IC	65	1.2	150	1951	AVAILABLE OPTIONS INCLUDE DRO CORE WITH 1 μSEC CYCLE TIME, AND BUFFERED I/O WITH 7 CHANNELS. ALSO DESIGNATED AN/AYK-5.
17. NORTRONICS NDC-1051A EARLY 1966	P	Fx	51	6	26	50	DRO CORE	14	8K	32K		2	2	8	DTL IC	38	0.87	225	3060	WEIGHT, SIZE, POWER AND MTBF ARE GIVEN FOR 16K MEMORY.
18. SPERRY MARK XII EARLY 1966	P	Fx	13	18	60		DRO CORE	21	6K				1		IC	64	1.5	250		MEMORY CAN BE PARTIALLY HARD-WIRED.
19. TRW MARCO 4418 EARLY 1966	P	Fx	27	10	70	73	DRO CORE	18	4K	8K		5	1	0	DTL IC	34	0.4	75		MEMORY CAN BE PARTIALLY HARD-WIRED.
20. ARMA MICRO D MID 1966	S	Fx	18	18 (12)	342 (200)	342	DRO CORE	18	4K	31K		3.3	2	1	TTL IC	5.75	0.07	30	10,000	(AVAILABLE WITH FAST CLOCK) MTBF EXCLUDES POWER SUPPLY, AT 50 C. NO ENVIRONMENTAL CONTROLS REQUIRED, -65C TO +125C
21. CDC 5360 MID 1966	P	Fx	41	12	90	90	DRO CORE	24	4K	32K	1.5	6	12	1	IC	26	0.6	95	1625	WEIGHT AND SIZE EXCLUDE POWER SUPPLY. MTBF IS FOR 8K MEMORY. MTBF IS 2425 FOR 4K MEMORY.
22. COMPUTING DEVICES OF CANADA AN/UYK-501 MID 1966	P	Fx	110	8	110	118	DRO CORE	24	4K	32K	1	2	1	64	IC	82	0.96	240	1180	WEIGHT, SIZE, POWER AND MTBF ARE GIVEN FOR 8K MEMORY. HAS ALTERABLE MICROPROGRAM.
23. SPERRY MARK XIV MID 1966	P	Fx	13	18	60		DRO CORE	21	6K				1		IC	64	1.5	250		MEMORY CAN BE PARTIALLY HARD-WIRED.
24. TI 2501 MID 1966	P	Fx	36	4	27	37	DRO CORE	32	4K	16K		2	17	32	IC	65	1.1	350		WEIGHT, SIZE AND POWER ARE GIVEN FOR 4K MEMORY.
25. UNIVAC 1830-A MID 1966	P	Fx	72	4	20	34	DRO CORE	30	4K	131K		2	32	1	IC	200	2.65	567	4500	ALSO HAS DRO THIN FILM CONTROL MEMORY AND 64-WORD CORE ROPE BOOTSTRAP MEMORY. SUCCESSOR TO 1830.
26. AC ELECTRONICS MAGIC 321 LATE 1966	S	Fx	22	15	121	323	DRO CORE	32	4K	32K		3	1	3	IC	23	0.44	120		WEIGHT, SIZE AND POWER ARE GIVEN FOR 8K MEMORY. DATA WORD, 31 BITS + PARITY; INSTRUCTION WORD, 15 BITS + PARITY.
27. AUTONETIC D26C LATE 1966	P	Fx	87	12	45		DRO CORE DRO CORE	30 30	8K 256	32K		6 1	2	8	IC	47	0.65	175	15,600	HIGH-SPEED MEMORY USED FOR SCRATCH PAD.
28. CDC 5400 LATE 1966	P	Fx	73	3.1	25	275	DRO CORE NDRO THIN FILM	24 96	4K 3K			2.5 2.5	5	16	IC	60	1.1	140	2500	4-WORD (96-BIT) READOUT FROM NDRO MEMORY TO AN INSTRUCTION LOOK-AHEAD MEMORY.
29. HONEYWELL SIGN III LATE 1966	P	Fx	53	4	24	24	DRO CORE	20	2K	16K	0.65	2.0	5	1	DTL IC	28	0.49	92	4000	HAS DOUBLE PRECISION ADD INSTRUCTION.
30. HUGHES HCM-205 LATE 1966	P	Fx	42	4	24	25	DRO CORE	18	2K	8K		2.0	1	1	DTL IC	16	0.2	110	4000	WEIGHT, SIZE AND POWER ARE GIVEN FOR 2K MEMORY.

TABLE 1 - CHARACTERISTICS OF AEROSPACE COMPUTERS (CONTINUED)

NAME / DATE INTRODUCED	DATA FLOW	DATA TYPE	NO. OF INSTRUCTIONS	COMPUTING TIME, μ SEC			MEMORY						IN/OUTPUT		PHYSICAL CHARACTERISTICS				MTBF (HRS)	COMMENTS
				ADD	MULT	DIV	TYPE	WORD SIZE (BITS)	CAPACITY (WORDS) MIN	CAPACITY (WORDS) MAX	ACCESS TIME (μSEC)	CYCLE TIME (μSEC)	NO. OF CHANNELS	NO. OF INTERRUPTS	TYPE OF HARDWARE	WEIGHT (LBS)	SIZE (CU. FT.)	POWER (WATTS)		
31. IBM 4 PI/CP LATE 1966	P	Fx	34	6.6	29.1		DRO CORE	32	8K	32K	0.9	2.5	3	5	TTL IC	57	.85	250	3000	HAS 1024-2048 WORD MICROPROGRAMMING MEMORY, 70 BITS/WORD, 155 NSEC ACCESS TIME. AVAILABLE WITH 51 OR 77 INSTRUCTIONS. AVAILABLE AS CP-2 WITH HARDWARE DECODE INSTEAD OF MICROPROGRAM.
32. IBM 4 PI/EP LATE 1966	P	FL	135	5.8	9.5	18.3	DRO CORE	36	8K	128K	0.9	2.5	3	5	TTL IC	62	0.9	303	5000	8K x 100 BITS MICROPROGRAMMING MEMORY. FLOATING POINT OPTION. 32-BIT DATA WORD. 1 PARITY BIT PER 8-BIT BYTE.
33. MIT BLOCK II AGC LATE 1966	P	Fx	34	23.4	46.8	81.9	DRO CORE CORE ROPE	16 16	2K 36K			11.4 11.4	15	10	DCTL IC	58	1.0	100	4100	HAS DOUBLE PRECISION ADD.
34. SPERRY MARK XVI LATE 1966	P	Fx	14	12	34		DRO CORE	21	8K	16K		6	4		IC	60	1.5	250		MEMORY CAN BE PARTIALLY HARD-WIRED.
35. AC ELECTRONICS MAGIC 301 EARLY 1967	S	Fx	12	24	96	280	DRO CORE	8	2K			4	2	1	IC	5.2	.08	39		MEMORY CAN BE PART HARD-WIRED. DATA WORD, 16 BITS; INSTRUCTION WORD, 8 BITS.
36. AC ELECTRONICS MAGIC 311 EARLY 1967	S	Fx	28	19	104	332	DRO CORE	13	6K	...		2.6	1	1	IC	15	0.28	87		DATA WORD, 24 BITS + 2 PARITY; INSTRUCTION WORD, 12 BITS + PARITY.
37. AC ELECTRONICS MAGIC 331 EARLY 1967	P	Fx	23	4.5	34.5	94.5	DRO CORE	16	4K	32K		3	1	1	IC	23	0.35	115		DATA WORD, 31 BITS + PARITY; INSTRUCTION WORD, 15 BITS + PARITY.
38. CDC 449 EARLY 1967	P	Fx	36	28	604		DRO THIN FILM NDRO μBIAX	24 24	256 3840				1	1	IC	12	.083	4.0		INCLUDES BATTERIES, KEYBOARD AND DIAL READOUT. 12-BIT PARALLEL, 2 BYTE SERIAL.
39. ELLIOTT MCS 920 M EARLY 1967		Fx	23	19	38		DRO CORE	18	8K	65K		5	2	0	DTL IC	30	0.61	60		WEIGHT, SIZE AND POWER ARE GIVEN FOR 8K MEMORY.
40. IBM 4 PI/TC EARLY 1967	P	Fx	54	15	51		DRO CORE	8	16K			2.5			TTL IC	27	0.48	75	7500	2 BYTE SERIAL, 8-BIT PARALLEL. MEMORY SIZE GIVEN IN TERMS OF 8-BIT BYTES. DATA WORD IS 2 BYTES AND INSTRUCTION WORD IS 1, 2 OR 3 BYTES.
41. RCA VIC-36A EARLY 1967	P	FL		9.3	66		DRO CORE DRO CORE	38 38	4K 512	32K	.650 .326	3.0 0.6	4	4	IC	120	3.0	525		SOME DISCRETE COMPONENTS USED. VARIABLE, INSTRUCTIONS CONTROL MICROPROGRAM. WEIGHT, SIZE AND POWER GIVEN FOR 4K MEMORY.
42. UNIVAC 1818 EARLY 1967	P	Fx	28	4	22	22	DRO CORE CORE ROPE	18 18	1K 4K	8K		2 2	12	10	IC	35	0.7	197	1500	WEIGHT, SIZE AND POWER ARE GIVEN FOR 8K MEMORY.
43. GPI KEARFOTT GPK-20 MID 1967	S/P	Fx	32	20	100		DRO CORE	10	4K	16K	1	4	5	1	DTL IC	25	0.35	85		HAS ADDITIONAL I/O FOR DISCRETES, PULSE RATE INPUTS. DATA WORD, 20 BITS; INSTRUCTION WORD, 5, 10, 15 OR 20 BITS.
44. NORTRONICS NDC-1060 MID 1967	P	Fx	51	6	26	50	DRO CORE	14	8K	32K	1	2	2	1	DTL IC	38	0.87	180	2367	WEIGHT, SIZE, POWER AND MTBF ARE GIVEN FOR 8K MEMORY.
45. TELEDYNE SERIES 20000 MID 1967	P	Fx	29	8	32	41	DRO CORE	20	1K	8K		4	4		IC	12	0.18	70	3999	PHYSICAL CHARACTERISTICS ARE FOR ONE IN THE SERIES.

TABLE 1 - CHARACTERISTICS OF AEROSPACE COMPUTERS (CONTINUED)

NAME / DATE INTRODUCED	DATA FLOW	DATA TYPE	NO. OF INSTRUCTIONS	COMPUTING TIME, μ SEC			MEMORY						IN/OUTPUT		PHYSICAL CHARACTERISTICS				MTBF (HRS)	COMMENTS
				ADD	MULT	DIV	TYPE	WORD SIZE (BITS)	CAPACITY (WORDS) MIN	CAPACITY (WORDS) MAX	ACCESS TIME (μ SEC)	CYCLE TIME (μ SEC)	NO. OF CHANNELS	NO. OF INTERRUPTS	TYPE OF HARDWARE	WEIGHT (LBS)	SIZE (CU. FT.)	POWER (WATTS)		
46. GPI KEARFOTT GPK-10 LATE 1967	S	Fx	32	70	1025	1055	DISC	32	16K				148	8	IC	31	0.46	100		PHYSICAL CHARACTERISTICS INCLUDE POWER SUPPLY. HAS ADDITIONAL I/O FOR DISCRETES, PULSE RATE INPUTS.
47. RAYTHEON RAC-230 LATE 1967	P	Fx	16	2.6	11.4	11.4	CORE or PLATED WIRE CORE	24 24	4K 2K			2	8	8		20	0.4	95	5000	
48. ARMA PORTABLE MICRO D EARLY 1968	P	Fx	36				CORE ROPE	18	4K				2		IC	14	0.195			ALSO CALLED CELESTIAL DATA PROCESSOR. WEIGHT AND SIZE INCLUDE BATTERIES AND I/O DEVICES.
49. NORTRONICS NDC-1070 MID 1968	S/P	Fx	53	6	8	32	DRO CORE	16	8K	64K	1	2	2	1	TTL IC					HAS DOUBLE PRECISION AND REGISTER-REGISTER OPERATIONS.
50. TI 2540 MID 1968	P	Fx	29	4	13.5		DRO CORE	32	4K	32K		2	4	16	IC	50	0.96	310	500	MTBF CALCULATED AT 71°C USING COMMERCIAL PARTS WITH NO BURN-IN; HI-REL, BURNED-IN PARTS CAN BE PROVIDED AT EXTRA COST. DATA WORD, 16 BITS; INSTRUCTION WORD, 32 BITS.
51. TI 2550 MID 1968	P	Fx	78	4	36	53	DRO CORE	32	4K	32K		2	4	16	IC	50	0.96	310	500	ALL COMMENTS FOR TI 2540 APPLY.
52. HONEYWELL H-437 LATE 1968	S	Fx	32	9	103	193	LSI ROS LSI ROS LSI	12 18 18	1K 128 32				2	2	IC	4	0.13	20	17,522	HAS HARDWARE SQUARE ROOT. MEMORY IS EXPANDABLE TO 8K. MEMORY SHOWN HAS 1K INSTRUCTIONS, 128 CONSTANTS, AND 32 SCRATCH PAD WORDS.
53. ARMA ADVANCED MICRO D DEVELOPMENT	P	Fx	36	6.6	25	25	CORE	18	4K	32K	0.7		2	1	IC	6.6	0.096	55		
54. AUTONETICS D-200 DEVELOPMENT							MOS	24	4K	32K						9	0.116	10		WEIGHT, SIZE AND POWER ARE GIVEN FOR 4K MEMORY.
55. LITTON L-3050 DEVELOPMENT	P	Fx	92	3.3	6		DRO CORE	32	8K	131K	1.6		1	64	IC	40	.33		2100	WEIGHT, SIZE AND POWER ARE GIVEN FOR 8K MEMORY. INSTRUCTION WORD ADDRESSES A MEMORY OPERAND, A REGISTER OPERAND, AND AN ANSWER REGISTER.
56. RAYTHEON ARGUS MULTIPROCESSOR DEVELOPMENT	P	Fx	55	2.4	9.4	23.7	CORE	32	8K	64K		1	16	256	TTL LSI	20	0.4	120		WEIGHT, SIZE AND POWER ARE GIVEN FOR 8K MEMORY. HALF-WORD INSTRUCTIONS USED FOR REGISTER-REGISTER OPERATIONS.
57. TELEDYNE TDY 300 DEVELOPMENT	P	Fx	42	6	22.5	230	DRO CORE	24	8K			3	7	5	IC	25	0.27	110	3240	ONE OF A SERIES.
58. TI 2502 LSI DEVELOPMENT	P	Fx	36	4	11	20	DRO CORE	32	4K	32K		2	4	12	LSI	46	0.45	200		DATA WORD, 32 BITS; INSTRUCTION WORD, 16 BITS.
59. TRW EW 20/24 DEVELOPMENT	P	Fx	48	4	29	55	DRO CORE	24	8K	32K	0.7	2	2	1						MULTIPROCESSOR. EACH 8K MEMORY MODULE CAN HANDLE PRIORITY REQUESTS AND PROVIDE A BUSY SIGNAL.
60. UNIVAC 1819 DEVELOPMENT	P	Fx	77	6	24	24	DRO CORE	18	4K	32K		2	8	1	IC	35	0.7	197		WEIGHT, SIZE AND POWER ARE GIVEN FOR 4K MEMORY.

TABLE 1: CHARACTERISTICS OF AEROSPACE COMPUTERS (CONTINUED)

*EXPLANATION OF HEADINGS:

- NUMBER: PROVIDES CROSS-REFERENCE FROM ALPHABETICAL LIST TO THIS CHRONOLOGICAL LIST.
- NAME: MANUFACTURER'S NAME, FOLLOWED BY OTHER IDENTIFYING NAMES OR NUMBERS. DATE OF INTRODUCTION IS DATE THAT MANUFACTURER HAD WORKING HARDWARE.
- DATA FLOW: S = SERIAL, OR P = PARALLEL, INDICATES THE WAY DATA FLOWS IN THE ARITHMETIC UNIT; S/P INDICATES A COMBINATION OF SERIAL AND PARALLEL, AND IS EXPLAINED IN THE "COMMENTS" COLUMN.
- DATA TYPE: Fx = FIXED POINT, FL = FLOATING POINT.
- NO. OF INSTRUCTIONS: THIS THE NUMBER OF INSTRUCTIONS IN THE INSTRUCTION SET, AND DOES NOT INCLUDE VARIATIONS OF BASIC INSTRUCTIONS.
- COMPUTING TIMES: NO MEMORY OVERLAP IS ASSUMED. ONE INSTRUCTION FETCH AND ONE OPERAND FETCH FROM MEMORY IS INCLUDED.
- MEMORY: "CAPACITY (MIN)" IS THE STANDARD MEMORY SIZE FOR THE MACHINE, AND "CAPACITY (MAX)" IS THE MAXIMUM SIZE OF DIRECTLY ADDRESSABLE MEMORY ATTAINABLE BY ADDING STANDARD MODULES.
- INPUT/OUTPUT: THESE NUMBERS WERE OBTAINED FROM MANUFACTURER'S DESCRIPTIONS. DIFFERENT MANUFACTURERS DEFINE "CHANNEL" IN DIFFERENT WAYS, AND INTERRUPTS LISTED IN SPECIFICATIONS SOMETIMES INCLUDE INTERNAL INTERRUPTS AS WILL AS EXTERNAL INTERRUPTS. THEREFORE, CARE SHOULD BE TAKEN IN USING THE NUMBERS LISTED.
- PHYSICAL CHARACTERISTICS: UNDER "TYPE OF HARDWARE" THE FOLLOWING ABBREVIATIONS ARE USED:

  MOS - METAL OXIDE SEMICONDUCTOR
  IC - INTEGRATED CIRCUITS
  DCTL - DIRECT-COUPLED TRANSISTOR LOGIC
  DTL - DIODE-TRANSISTOR LOGIC
  TTL - TRANSISTOR-TRANSISTOR LOGIC
  HL - HIGH LEVEL, AS IN HLTTL.
  LSI - LARGE SCALE INTEGRATION

  THE WEIGHT, SIZE, AND POWER REQUIREMENTS ARE GIVEN FOR A MACHINE WITH A "STANDARD SIZE" MEMORY.
- MTBF: THIS IS A FIGURE OBTAINED FROM THE MANUFACTURER. THE METHOD OF CALCULATING THE RELIABILITY MAY VARY FROM MANUFACTURER TO MANUFACTURER.
- COMMENTS: COMMENTS DESCRIBE UNIQUE OR INTERESTING FEATURES, OR FURTHER EXPLAIN AN ENTRY IN THE PRECEDING COLUMN.

TABLE 2. ALPHABETICAL LIST OF COMPUTERS

Number From Table 2	Name	Year Introduced
35	AC Electronics Magic 301	Early 1967
36	AC Electronics Magic 311	Early 1967
26	AC Electronics Magic 321	Late 1966
37	AC Electronics Magic 331	Early 1967
53	ARMA Advanced Micro D	Development
3	ARMA Micro Computer	Mid 1962
20	ARMA Micro D	Mid 1966
48	ARMA Portable Micro D	Early 1968
27	Autonetics D26C	Late 1966
15	Autonetics D26J	Late 1965
54	Autonetics D-200	Development
11	Burroughs D84	Mid 1964
1	Burroughs D210	Pre 1962
38	CDC 449	Early 1967
21	CDC 5360	Mid 1966
28	CDC 5400	Late 1966
22	Computing Devices of Canada AN/UYK-501	Mid 1966
39	Elliott MCS 920M	Early 1967
6	General Precision AN/ASN-24	Mid 1963
46	General Precision Kearfott GPK-10	Late 1967
43	General Precision Kearfott GPK-20	Mid 1967
16	Honeywell ALERT	Late 1965
52	Honeywell H-437	Late 1968
29	Honeywell SIGN III	Late 1966
4	Hughes HCM-201	Mid 1962
7	Hughes HCM-202	Mid 1963
30	Hughes HCM-205	Late 1966
5	IBM Gemini Guidance Computer	Early 1963
8	IBM Saturn IB/V LVDC	Mid 1963
32	IBM 4 PI/EP	Late 1966
31	IBM 4 PI/CP	Late 1966
40	IBM 4 PI/TC	Early 1967
13	Litton L-304	Early 1965
55	Litton L-3050	Development
33	MIT Block II AGC	Late 1966
9	MIT Block I AGC	Late 1963
14	Nortronics NDC-1051	Early 1965
17	Nortronics NDC-1051A	Early 1966
44	Nortronics NDC-1060	Mid 1967
49	Nortronics NDC-1070	Mid 1968
56	Raytheon ARGUS Multiprocessor	Development
47	Raytheon RAC-230	Late 1967
41	RCA VIC-36	Early 1967
12	SAAB CK37	Mid 1964
18	Sperry Mark XII	Early 1966
23	Sperry Mark XIV	Mid 1966
34	Sperry Mark XVI	Late 1966
45	Teledyne TDY-210	Mid 1967
57	Teledyne TDY-300	Development
24	Texas Instruments 2501	Mid 1966
58	Texas Instruments 2502 LSI	Development
50	Texas Instruments 2540	Mid 1968
51	Texas Instruments 2550	Mid 1968
59	TRW EW 20/24 Multiprocessor	Development
19	TRW MARCO 4418	Early 1966
2	Univac ADD-1000	Pre 1962
42	Univac 1818	Early 1967
60	Univac 1819	Development
10	Univac 1824	Late 1963
25	Univac 1830-A	Mid 1966

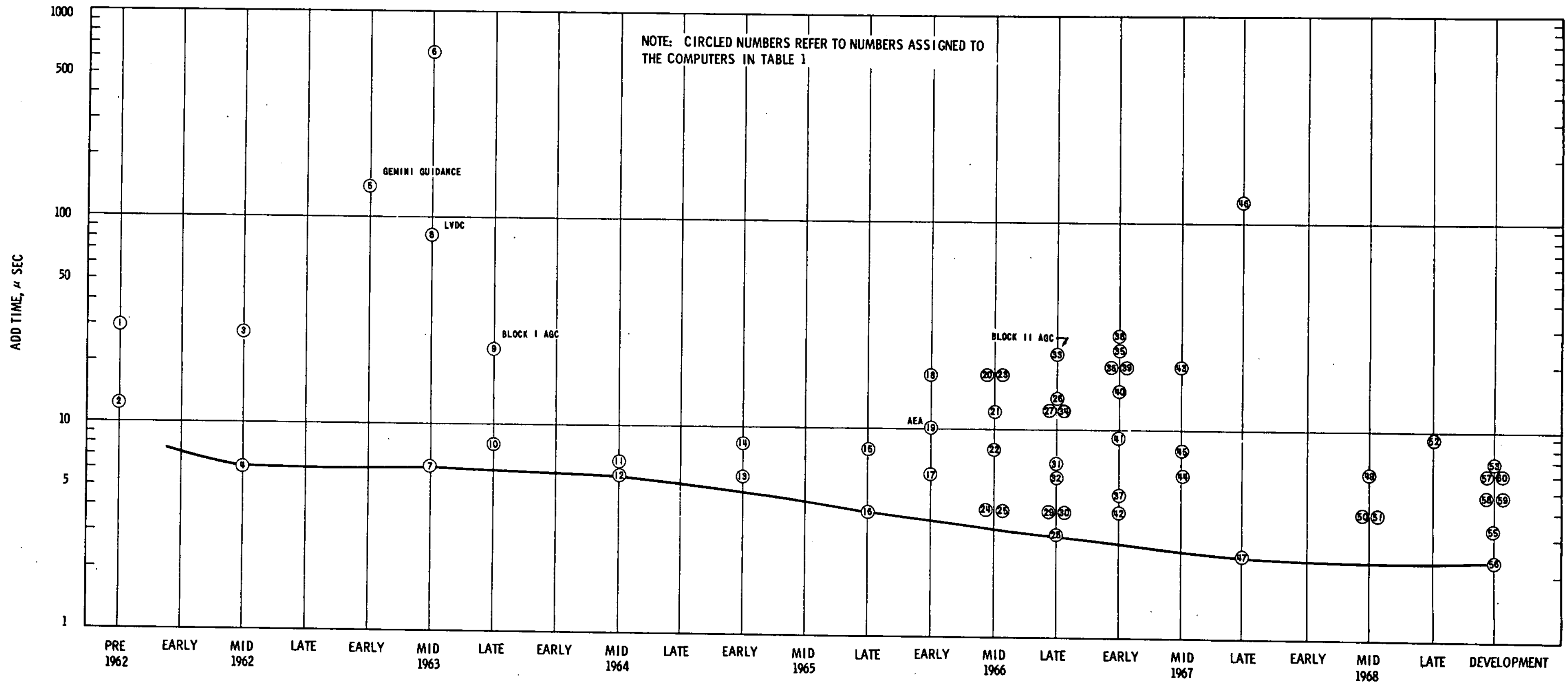

FIGURE 1 - ADD TIMES OF AEROSPACE COMPUTERS

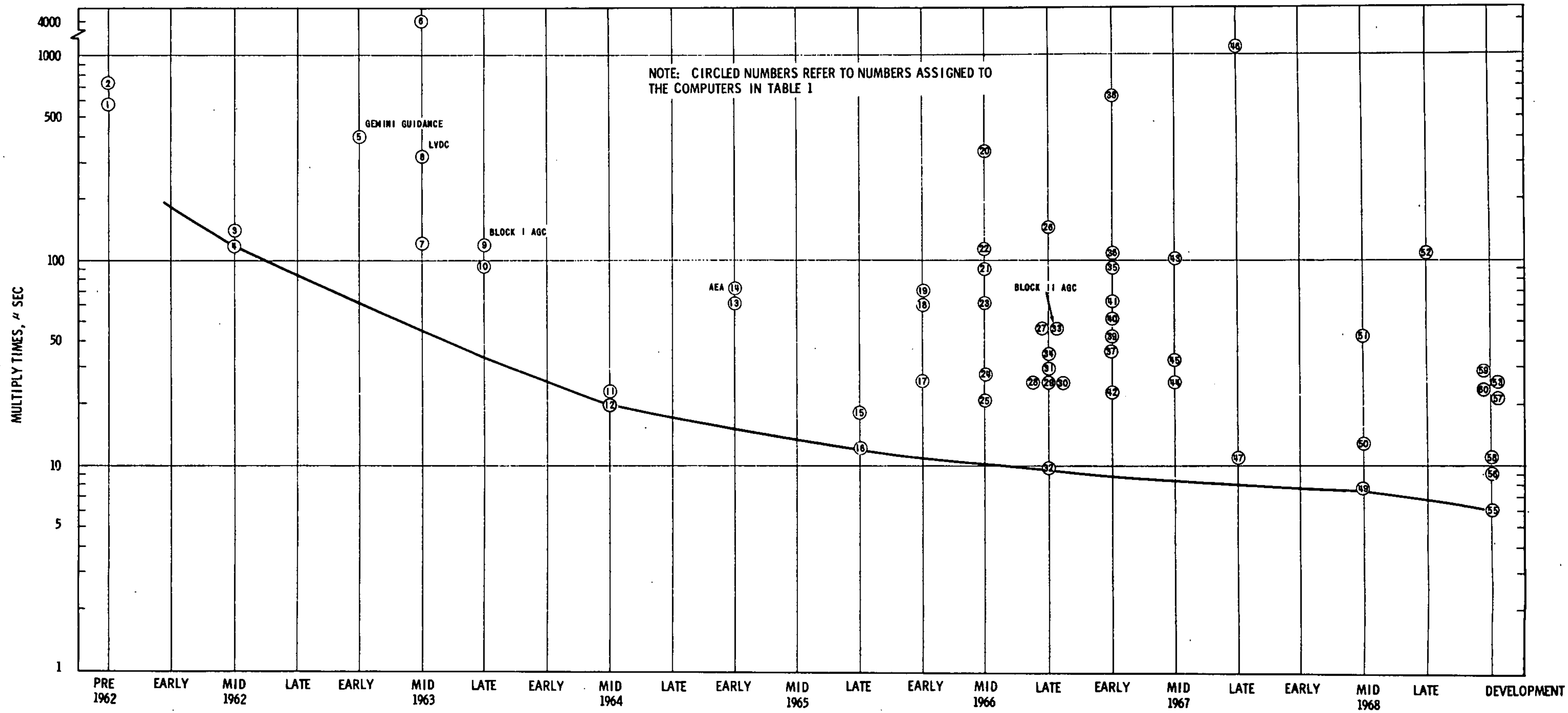

FIGURE 2 - MULTIPLY TIMES OF AEROSPACE COMPUTERS

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Subject: Aerospace Digital Computer Design Trends - Case 103

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