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PROCESS TECHNIQUES STUDY OF INTEGRATED CIRCUITS

Quarterly Report No. 13

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ABSTRACT

The purpose of this program is to investigate some of the dominant problems confronting planar technology, to seek solutions to these problems and to provide instrumental support services to NASA-ERC in the areas of failure analysis and instrumental capabilities. Areas of investigation are organized under the following categories of activity.

1. Failure Mechanisms Related to Oxide Passivation
2. Failure Mechanisms Associated with Packaging
3. Instrumental Capability Profile

Past program activities on oxide passivation have provided insights into the origin of atomic species contributing to inversion and to the origin of dielectric defects. Current activities have shown that most dielectric defects in oxide layers are developed during the cooling of wafers after oxidation and follow an exponential decay with increasing oxide thickness. Compressive stress in the oxide layers due to thermal expansion mismatch with the substrate is directly implicated as a causative factor, and the loci of defects appear to be determined by micron-size surface irregularities in the silicon substrate. Treatments designed to reduce such irregularities produce a corresponding reduction in defects.

Examination of oxide impurities is reopened with special reference to their effects on MOS-FET gate performance. Some approaches to the analytical determination of such impurities are given.

Previous packaging investigations have shown that deleterious effects of hydrogen on integrated circuits are nonexistent. A compilation of thermodynamic free energy values applicable to potential interactions of normal package components provided further corroboration of this result. No additional reportable items are presently available.

The instrumental capability profile was updated in February, 1968 (Quarterly Report No. 11), followed by an analysis of leak test methods (Interim Scientific Report No. 1). The present report considers instrumental approaches to the measurement of oxide impurities and MOS-FET gate temperatures.

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1. Failure Mechanisms Related to Oxide Passivation

A. Dielectric Defects - Mechanism Research

The occurrence of dielectric defects, or "pinholes", constitutes a significant failure mode in modern oxide passivated devices and is probably the largest remaining barrier to large scale integration. Although numerous remedial innovations in materials and process techniques have been attempted, no reliable solution to this problem has yet been found. Because of the general convenience and superiority of thermally grown oxides for most masking and passivating purposes, and because this application of silicon dioxide has been successfully optimized in most other respects, it seems important to take full advantage of these characteristics by determining the process requirements needed to remove this remaining major problem in its use. The objectives of this effort, therefore, are to discover why structural defects are produced in thermally grown oxides and to learn how they may be prevented.

Previous activity on this program has sought to relate the origin of dielectric defects to various process factors and structural considerations. These results may be summarized as follows:

(1) Factors tending to increase dielectric defects.
  a. Extended process (generally)
  b. Higher compressive stress in the oxide
  c. Embedded lapping grains in the substrate
  d. Superficial HF etching
  e. Abrupt oxide steps
  f. Thermal cycling
  g. Mechanical wiping
  h. Removal of back oxide layers

(2) Factors tending to decrease dielectric defects.
  a. Growth of oxide to higher thicknesses
  b. Chemical etch of initial wafer
  c. Pyrolytic oxide, uniformly applied and properly densified
  d. Additives tending to reduce bond strain in silica glass
  e. Addition of steam to oxidation process gas, or termination of any dry oxidation step with a wet oxidation

(3) Factors having little or no effect on defect incidence.
  a. Wafer cooling rates after oxidation
  b. Mineral content of water used as steam source
  c. Oxide growth rate
  d. Substrate doping (except high boron levels)
  e. Crystal micro-defects (dislocations, stacking faults)
  f. Some nonreactive or nonadhering particulate contaminants.

The results noted above are consistent with a compressive stress model as the principle source of dielectric defects in oxide layers. The compressive stress in the oxide layer is introduced during cooling from the oxidation temperature as a result of an approximately 10-fold mismatch in thermal expansion coefficients between substrate and dielectric. This model was confirmed in a number of subsequent experimental observations. Replicate electron microscopy of a known defect revealed oxide outcroppings suggestive of a compressive stress relief process. Measurements of the compressive stress gave values of the order of 4×10^4 psi. Quantitative comparison of oxide defect densities before and after cooling to room temperature demonstrated that the bulk of the defects (90 to 98 percent) were introduced during the cooling process. Removal of one oxide layer from a wafer introduced a significant warping of the wafer which resulted in an increase in the measured defect population in the remaining oxide layer.

Although these tests established beyond reasonable doubt the origin of the physical forces producing dielectric defects they provided no direct indication of the local factors contributing to their formation. The contribution of substrate crystal dislocations and loosely adhering particulates previously had been ruled out. Therefore additional experiments were undertaken to examine in detail the kinetics of the oxidation process. Defect densities as a function of oxide growth were found to follow an exponential decay law. This was true not only of defect densities after cooling to room temperature, but also of densities prior to cooling and of those remaining after one oxide layer had been etched off. As expected, decay factors were largest prior to wafer cooling (unstressed condition) and least after warping the wafer by removal of one oxide layer. The general nature of these results indicated the existence of latent defects in the oxide prior to cooling which were progressively strengthened and rendered less vulnerable to rupture as oxide thickness was increased. The assumed presence of such latent defects, however, implies the existence of structural or distributional irregularities in the oxide-substrate system introduced either before or during the oxidation process.

Further investigation revealed that a kinetic anomaly in oxide growth rate existed at the beginning of oxidation (during the first 300 to 600 Å) after which a square root low characteristic of a diffusion controlled process was followed. Attention, therefore, was focused on the beginning phases of oxidation in the expectation that moderation of the reaction kinetics at this point might remove an assumed distributional irregularity in the oxide and thereby reduce the latent defect density. Such a moderation was achieved (and kinetically demonstrated) by application of an oxidative pretreatment (using hot nitric acid) which developed a very thin oxide layer on the wafers prior to high temperature oxidation. A significant drop in the latent defect density (extrapolated to oxidation time zero) was observed as a result of this treatment.

It was not clear from this result whether the decrease in defect density was due solely to an attenuation of initial oxidative attack on the substrate or to an additional "cleansing effect" caused by the nitric acid

treatment. Therefore a second series of experiments was performed in which the initial thin oxide layer was introduced by slow thermal growth. In this case the wafers were "nonoxidatively" precleaned (using a swabbing technique with HF, preceded and followed by water and alcohol rinses). The resulting defect decay curve versus oxide thickness was essentially identical with the corresponding curve for the oxidatively precleaned wafers, both with respect to decay factors and to latent (ordinate intercept) defect densities.

This result was taken as potential confirmation that the assumed initial inhomogeneities associated with latent defect sites were, in fact, related to the observed kinetic anomaly at the beginning of oxidation. A number of tests were made, therefore, to modify the reaction kinetics during the first few hundred Ångstroms growth and to correlate the defect densities in these very thin oxide layers with the type of treatment used. Although the results appeared to substantiate the proposed model they did not differentiate clearly between purely kinetic effects and the possible effects of dimensional irregularities in the silicon substrate. In either case, the initial slow oxidation might provide the necessary conditions for the equilibrium distribution of either oxide or substrate material. If dimensional irregularities were the locus-determining factor, the participating physical irregularities of the oxide-substrate system, regardless of origin, would be in the submicron range, i.e., a significant fraction of the oxide layer thickness and several orders of magnitude greater than the substrate lattice parameter. The appearance of a defect in the oxide layer (after cooling) then would become a function of the particular local stress conditions associated with the radius of curvature of the presumed structural irregularity. As more oxide is grown the ratio of the radius of curvature to the oxide thickness will decrease exponentially with oxide thickness, thus accommodating the corresponding disappearance of dielectric defects.

The concept was subjected to test by applying an HCl vapor etch to wafers (four sets of four each) immediately prior to oxidation. This idea is not novel, as it has been recently learned that Semimetals (q.v., below) employs the same treatment prior to wafer oxidation. The decoration densities resulting from the inclusion of this treatment clearly showed improvement over those not so treated. Consequently additional tests were designed to maximize the redistribution of the assumed structural irregularities both in "bare" silicon and in very thin initial oxide layers using various heat-soak periods at the oxidation temperature (1180 C). Because this temperature is well above the set temperature of silica (1000 C) it was felt that the oxide would be sufficiently plastic to conform to any interfacial energy-reducing material migrations. Also included in the experimental matrix were tests of the effects of oxidative precleaning of the wafers and static and dynamic conditions of nitrogen flow during heat soak. The results showed that oxidative precleaning was not as effective as HF wiping in reducing defects and that a very slow nitrogen flow during heat-soak was superior to a rapid flow in reducing defects. In general, all the treatments designed to smooth the silicon surface produced improvements while at least two of them (HF wiping and HCl pre-etch) should have had no effect at all on the initial oxidation kinetics.

The foregoing results are a summary of work previously reported on this program and serve as a basis for the work continuing through the present period described below.

In continuing experiments all wafers were precleaned by HF wiping, as described previously, and all were exposed to a five-minute treatment with four percent dry O_2 immediately prior to a 16-hour heat-soak in nitrogen. Process variables and resulting defect counts are summarized in Table I.

TABLE I. EFFECTS OF HCl PRETREATMENT AND HEAT-SOAK ON DEFECTS

HCl pre-treatment (minutes)	N_2 Heat-Soak (hours)	Normal Oxidation (minutes)	Oxide Thickness (Angstroms)	Defects (cm^{-2})
none	16	10	2600	12.3
none	16	40	4500	6.0
none	16	80	6100	3.7
1	16	5	1900	15.8
1	16	20	3300	5.7

A log plot of the first three defect counts yields approximately 1 defect/cm^2 when extrapolated to 10,000 Å, which compares with results from TI and Fairchild wafers grown to 10,000 Å (see below). The second set of data, which includes a one-minute HCl treatment prior to the dry O_2 preoxidation, when similarly plotted yields less than 0.1 defects/cm^2 at 10,000 Å, which compares with results from Semimetals grown to this thickness. The effect of the HCl appears to be to cause a significantly higher defect decay rate with oxide thickness as a result of reducing initial wafer surface irregularities.

Increasing the HCl treatment to two minutes produced a further reduction of defect densities as shown in Table II where the effects of one-minute and two-minute treatments are compared.

TABLE II. EFFECT OF HCl PRE-ETCH ON OXIDE DEFECTS

HCl pre-treatment (minutes)	Normal Oxidation (minutes)	Oxide Thickness (Angstroms)	Oxide Defects (cm^{-2})
1	5	1900	15.8
1	20	3300	5.7
2	5	2300	6.4
2	20	3200	4.0

The results are clearly superior to those obtained with a shorter HCl pretreatment. Extrapolation to 10,000 Å again yields a defect density of the order of $0.1/cm^2$ which is comparable with oxides grown by Semimetals and superior to oxides grown by Fairchild and TI.

The HCl pretreatment, however, was distinctly less than optimum because it introduced clearly visible (at 100 X) etch pits in the wafers. Etch pit sizes lay in the micron and sub-micron range. A comparison of etch pit counts with defect counts revealed a distinct correlation as shown in Table III.

TABLE III. OXIDE DEFECTS AS A FUNCTION OF PREVIOUSLY INTRODUCED ETCH PITS

HCl Etch Pits (per wafer)	Ultimate Defects (per wafer)
72	20
77	45*
82	27
98	34
116	16*
125	40
174	58
233	115

The only anomalous results in this progression are the ones starred. This is the first known direct evidence that depressions in the silicon surface, in the micron and sub-micron range, give rise to subsequently grown oxide irregularities which are incapable of withstanding the compressive stress introduced on cooling from the oxidation temperature. It is well known that vitreous silica is remarkably resistant to compressive stress but yields readily to tension and shear. The abrupt changes in oxide curvature caused by the etch pits introduce tension and shear vectors as resultants of the existing compressive stress. Thus the oxide pinhole problem now appears to be completely defined, and the answer to this problem in terms of process techniques would appear to lie in achieving complete geometrical smoothness of silicon surfaces prior to oxidation. The usefulness of an HCl pre-etch in achieving this result already has been demonstrated. Other means of developing the requisite smoothness undoubtedly will be devised. In principle, however, the oxide pinhole problem would seem to be solved.

Future investigation should take the following courses: 1. Optimize the HCl pretreatment in order to define properly the most effective process technique for eliminating oxide defects; 2. Investigate other surface smoothing

methods of potential process applicability; 3. Evolve an analytical model quantitatively relating the development of tension and shear stresses to compressive stress and oxide radius of curvature; 4. Secure quantitative experimental evidence relating the size and shape of silicon surface irregularities to the incidence of defects over a range of oxide thickness; 5. From Items 3 and 4, draw up a material specification defining the tolerable limits of silicon surface irregularities applicable to planar processing.

B. Dielectric Defects - Vendor Survey

Defect analyses of 10,000 Å oxides prepared by three manufacturers are listed in Table IV.

TABLE IV. DEFECT LEVELS IN 10,000 Å OXIDES FROM VARIOUS SOURCES

Company	Number of Wafers	Average Defects (cm^{-2})	Wafers with zero Defects (%)	Maximum count ($wafer^{-1}$)
Semimetals				
Lot 1	10	0.040	80	1
Lot 2	28	0.057	79	2
Fairchild				
Lot 1	10	0.29	30	9
Lot 2	10	0.69	-0-	19
Lot 3	10	0.72	10	13
Texas Inst.	30	0.73	3.3	11

The superiority of the Semimetals product is clearly evident with 80 percent of the wafers having no defects at all. A Semimetals representative indicated to Autonetics that its oxidations were preceded by an HCl etch; no other vendor made this claim. In view of the results tabulated in the preceding section of this report it seems likely that neither Texas Instruments nor Fairchild employ a pre-etch with HCl.

Also of interest is the apparent lot-to-lot variance in the case of Fairchild. As expected, the lower the average defect density, the higher the proportion of wafers with zero defects and the smaller the maximum count for a single wafer. Texas Instruments did not supply separate lots but has agreed to ship two more lots in compliance with the original purchase order.

C. Oxide Impurities

Gate oxides in MOS-FET's are subject to contamination by a variety of materials, some of which may be present in the original silicon while others are introduced by processing. In the first category may be included sodium at $\sim 5 \times 10^{13}$ atoms/cm^3 as determined by neutron activation analysis (Fifth Monthly Report, September, 1965) and traces of gold, copper and manganese detected by the same means (Quarterly Report No. 3, February 15, 1966). Contaminants introduced by processing include minimally phosphorus (or boron) via diffusion steps, fluoride via etching steps and sodium via boil-off from quartz tubing during oxidation. Other trace contaminants may be introduced from additional treatments, such as clean-up steps, and may include carbon, sulfate, chromium, etc., according to the procedures used.

The role of sodium in causing MOS-FET gate instability has received considerable attention, resulting in a variety of process modifications designed to curtail its presence in oxide layers. However, no tolerable upper limit of sodium seems to have been established, nor has success been achieved in excluding its presence sufficiently to gaurantee stable gate threshold voltages. In addition, little has been done to establish the contribution of other known contaminants to gate performance. These problems exist primarily because of the analytical difficulties associated with the low levels of contamination usually involved and the small sample sizes that must be manipulated.

The objective of this investigation is to review the analytical techniques potentially applicable to this problem, to select and employ the most promising on typical gate oxides and to correlate the analytical results with gate performance so as to demonstrate the maximum tolerable limit of each contaminant chosen for study.

Initial attention will be focused on sodium, to be extended later to other contaminants as methodology is refined. Some approaches are considered below. For comparative purposes it will be assumed that a uniform sample size is available for analysis derived from the entire wafer area, less a small section containing one or more MOS-FET's for electrical characterization. The MOS-FET's can be separated from the remainder of the wafer by scribing and breaking where required by the analytical technique employed. The bulk of the wafer will be processed to gate oxide simultaneously with the MOS-FET's on the assumption that the oxide will be a true representation of that comprising the gates. It also will be assumed that the gate oxide thickness is 1000 Å, thereby yielding a total sample of $\sim 5 \times 10^{-3}$ cm^3. Finally, it will be assumed, on the basis of available literature information, that for an analytical technique to qualify for further consideration it must at least detect 10^{17} atoms of Na/cm^3 of oxide with 50 percent precision. In the available sample this amounts to a total of 5×10^{14} sodium atoms in association with 10^{20} silicon atoms and 2×10^{20} oxygen atoms.

(1) Wet Chemical Approach - Theoretically $2.5 \times 10^{-2} cm^3$ of 48 percent HF should suffice in dissolving the sample after separating the MOS-FET section from the wafer. Practically, a larger volume would have to be used, probably of the order of $0.2\ cm^3$, which could be led as a droplet over the area of the wafer by means of a probe. Tests at Autonetics have revealed that electronic grade HF contains 0.13 ppm sodium which, in $0.2\ cm^3$, would amount to 7×10^{14} atoms of sodium, approximately equal to the sodium level sought in the sample. The excessive reagent blank required in this case would have to be reduced by further purification of the HF. Assuming this can be done (Reference 1) (or that acid of higher purity is available) there are several ways of proceeding with the analysis for sodium, the most attractive being flame photometry (Reference 1) and atomic absorption spectrophotometry. These methods are roughly comparable in sensitivity but the latter is freer from interferences. The lower limit of detection of sodium by atomic absorption spectrophotometry is 0.03 ppm (Reference 2) or 1.6×10^{14} atoms of sodium in the specified sample volume. This just meets the sensitivity target earlier adopted and assumes that $0.2\ cm^3$ would be adequate volume for test. If sodium levels of $10^{16}\ atoms/cm^3$ in oxides are found to be important (a very real possibility) then the test would fail. In view of the marginal capability of this approach, and the problem of securing sufficiently pure reagents (Reference 1), it is recommended that this approach not be pursued further.

(2) Electron Microprobe - Analysis by the electron microprobe is extremely convenient and is readily adaptable to small samples. Experience developed in the application of this instrument to a variety of analytical problems at Autonetics reveals, however, that it is incapable of attaining the sensitivity required by the present problem. The limit of detection of chromium in alumina, for example, is 50 ppm. For lighter elements the instrumental sensitivity decreases rapidly and is estimated to be 1000 ppm for sodium in thick (10,000 Å) oxide layers. In 1000 Å layers the sensitivity would be a factor of ten lower. The Autonetics instrument focuses on a spot of ~ 5 microns diameter which in a 1000 Å layer would yield a sample volume of $2 \times 10^{-12} cm^3$. At 10^{17} Na $atoms/cm^3$ this would amount to a total of 2×10^5 atoms, or 10^{-17} grams of sodium. A potential additional problem is the penetration of the beam through the oxide and into the silicon. However, with a level of 5×10^{13} atoms of Na/cm^3 in the silicon this would not introduce significant error. The above figures indicate that the lower limit of detection of sodium by the electron microprobe is $\sim 10^{19}\ atoms/cm^3$ in 10,000 Å oxides and $10^{20}\ atoms/cm^3$ in 1000 Å oxides, and that this instrument would be incapable of fulfilling the analytical requirements sought.

(3) Neutron Activation Analysis - Previous work on this program (Quarterly Report No. 3, February 15, 1966) has demonstrated the feasibility and convenience of estimating sodium levels in oxide layers by neutron activation analysis. Analyses were performed on composite samples of five oxidized wafers each to insure adequate sample activities. Samples (and Na standard) were irradiated 0.5 hr at 250 KW (Mark I TRIGA reactor) in a thermal neutron flux of $1.8 \times 10^{12}\ n\ cm^{-2}\ sec^{-1}$. Oxides were stripped from the wafers by HF (to isolate the samples from activities retained in the silicon)

and concentrated by evaporation. The residue was counted in a NaI well detector using the 2.75 Mev photopeak of Na^{24} to avoid interference from Si^{31}. Sodium levels of 10^{17} to 10^{18} atoms/cm^3 were readily estimated by this technique. The total sample size, however, was about 15 times larger than that now under consideration. On the basis of previous and recent experience at Autonetics it is estimated that the lower limit of detection could be extended to a total of about 2 X 10^{14} sodium atoms by increasing the neutron dosage level and accelerating sample preparation for counting. This would correspond to a sensitivity limit of $\sim$5 X 10^{16} atoms/cm^3 in the specified sample volume. The sodium content of the HF and other reagents would not constitute an interference since only the sodium in the original oxide would be radioactive. Thus neutron activation analysis appears to be superior to the two approaches previously discussed and may well afford useful correlation data.

(4) Solids Mass Spectrometry - Autonetics recently has undertaken an investigation of the analysis of trace contaminants in SiO_2 layers by solids mass spectrometry. The instrument used is a CEC Model 21-110 located at the Bell and Howell Research Center, Pasadena, California. An integral part of the program is to compare the sensitivity of solids mass spectrometry with neutron activation analysis. It has been found that neutron activation analysis is comparable in sensitivity with solids mass spectrometry when the latter is used in the photoplate detection mode. However, when used with an electrical detector it is capable of exceeding the sensitivity of neutron activation analysis by two orders of magnitude. Moreover, the technique readily and unambiguously detects many other potential contaminating elements in silicon dioxide layers.

The technique consists essentially of vaporizing and ionizing the sample with an RF spark, followed by sorting and collection of the ionized species in a mass spectrometer. In order to maximize the sampling of thin oxide layers and minimize the sampling of silicon, successive small pulses of RF energy have been applied to different areas of the surface of the wafer. Adaptation of more advanced techniques, such as the use of a spinning sample disc, should decrease the time and effort spent in sampling and increase the amount of sample consumed.

Using photoplate detection the limit of sensitivity for sodium is 1.6 X 10^{15} atoms/cm^3 in oxide layers 1.5 microns thick. For 1000 Å layers the mass spectrometric detection limit becomes 2.5 X 10^{16} atoms/cm^3 which compares with 5 X 10^{16} atoms/cm^3 achievable by neutron activation analysis. With photoplate detection a complete contaminant spectrum is obtained; if only one or two elements are sought, electrical detection (with a lithium drifted Ge detector) becomes feasible with an increase in sensitivity by a factor of 100. For sodium this limit would be 2 X 10^{14} atoms/cm^3 oxide. Other trace elements detected and estimated included C, F, Mg, Al, P, Cl, K, Ca, Cr, Fe and Cu. In view of these results it would appear that solids mass spectrometry is the most versatile and powerful tool presently available for the detection of contaminant elements potentially inimical to the performance of MOS-FET gates.

2. Failure Mechanisms Associated with Packaging

No additional results are presently available.

3. Instrumental Capability Profile

A. Temperature Determination of MOS Structures

Thermal treatments of planar structures for the purpose of mobilizing ionic impurities in silicon dioxide layers, particularly under electrical bias, are frequently employed to achieve metastable distributions from which the density of slow states, Q_{ss}, may be deduced. In addition, the activation energies of the thermal redistribution of ionic entities provide important clues to their identities as previously investigated on this program (Quarterly Report No. 3, February 15, 1966, p. 7 ff; Quarterly Report No. 4, May 15, 1966, p. 15). The details of temperature measurement and control in such circumstances, such as in C-V measurements on MOS structures, are frequently omitted. The purpose of this study is to consider in comparative fashion various approaches to the temperature measurement of MOS structures while under electrical bias. These are enumerated below.

(1) Liquid Crystals - The use of "liquid crystals", mainly cholesteryl esters and other sterol derivatives, have come into use in recent years as color indicators of surface temperatures. At present many such compositions are on the market, spanning various temperature ranges. The materials are organic-soluble and noncorrosive; therefore they frequently are recommended for use in nondestructive testing of semiconductor surfaces. The problem of whether the organic residues can be completely removed from the surface after testing does not seem to have been thoroughly investigated. The materials generally are applied in the form of a thin film, usually by evaporation of original solvent. As temperature is raised a point is finally reached where crystal or micel alignment begins to take place, producing a birefringent effect which is observed as a distinct color. Continued increase in temperature gives rise to a complete spectrum of colors corresponding to a manifold of aggregational states in the film. The effect terminates at a temperature where molecular disorganization becomes complete. The process is reversible and may be repeated indefinitely, each color being associated with a specific temperature. Temperature identification is somewhat subjective, as well as dependent on ambient lighting, reflection angle, etc. To a large degree these factors can be normalized and quantified by obvious instrumental routes where required. Temperature spans generally cover ranges of three to 50 degrees centigrade for a single material with temperature resolution decreasing (since only one color octave is involved) as the span is increased. A three degree range, for example, gives 0.3 C resolution by ordinary microscopic observation and 0.01 C resolution with spectroscopic equipment. Cholesteryl esters are available over a -20 to 350 C range. They have been applied successfully to integrated circuit surfaces and should be applicable to MOS structures over most thermal treatment ranges of interest.

(2) Thermocouples - Although the art of thermocouple applications has been refined enormously it is doubtful if a junction can be made small enough to have a heat capacity a small fraction of that of an MOS chip and still be convenient to implement. Further doubt arises as to completeness of contact with the specimen. In view of these problems, and the relative complexity of required instrumentation (due to the high impedance source), a thermocouple technique is not recommended.

(3) Built-in Sensor - Where practical, a built-in resistive element could be vacuum deposited directly on the device chip with independent leads of T-dependence measurements. Unit calibrations probably would be needed for each specimen but, after some experience, could be done at two or three selected temperatures well below treatment temperatures or temperatures that would degrade the original ion distribution in the gate oxide. The method is recommended as an alternative to the liquid crystal approach.

(4) Thermostating - The most reliable method of controlled thermal treatment is by thermostat. Control to $\pm$ 0.01 C is readily available in a variety of instrumentation. Where time of exposure must be sharply defined mechanical arrangements for quick insertion and removal of specimens must be made. The problem is compounded if the device simultaneously must be under electrical bias. This should be achievable, however, with a well-type heater provided with a controlled vertical motion. This approach should receive top priority over the others mentioned unless presently unobvious complications would be introduced thereby.

COMPLETION INFORMATION

Approximate physical completion (current year) 69%

Approximate expenditures 68%

ACTION REQUIRED BY NASA

None

CURRENT PROGRAM CONTRIBUTORS

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REFERENCES

1. B. Yurash and B. E. Deal, J. Electrochem. Soc. 115, 1191 (1968).
2. L. Capacho-Delgado and A. J. LaPaglia, American Laboratory, October, 1968, p. 39.