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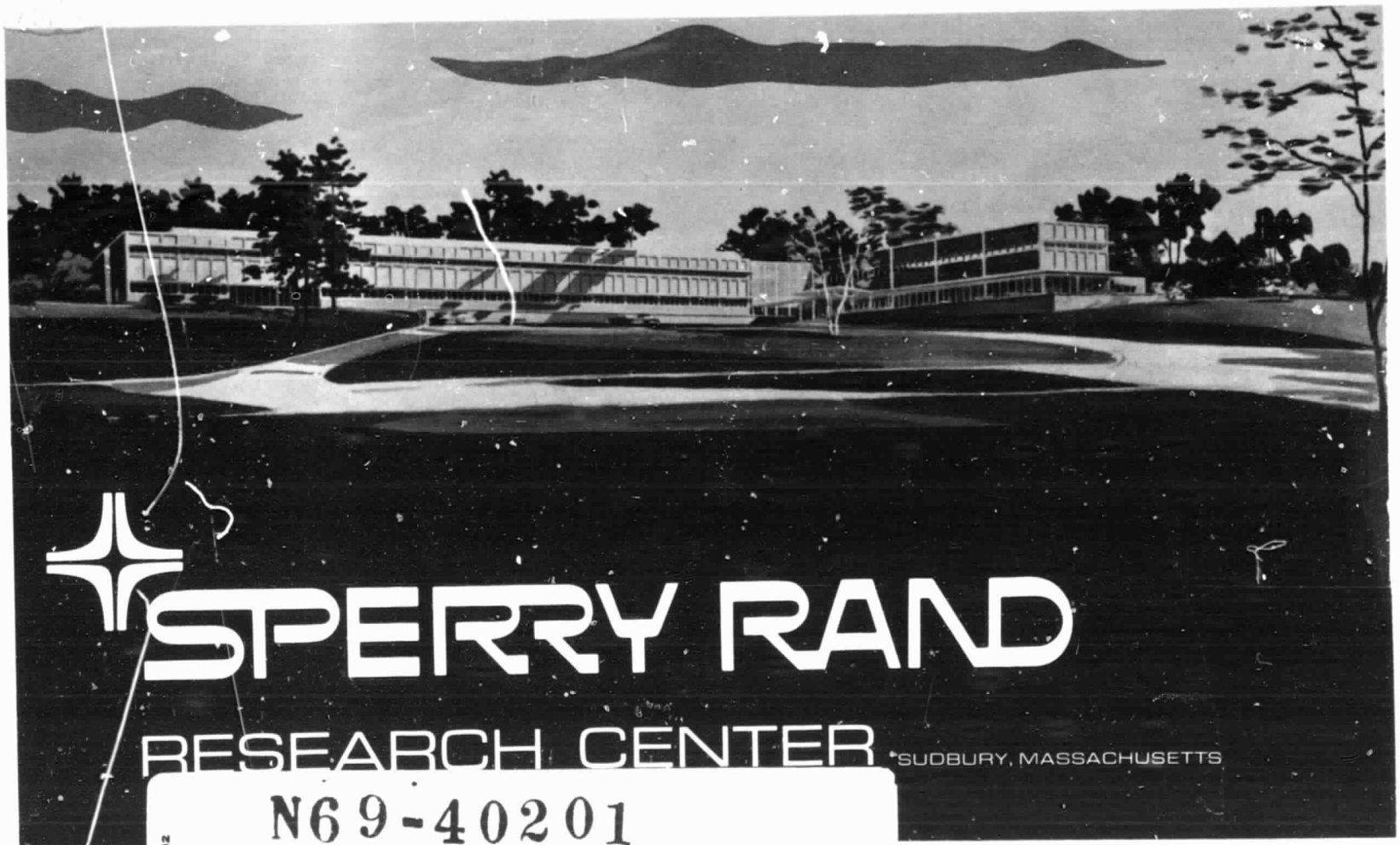

SPERRY RAND

RESEARCH CENTER

SUDBURY, MASSACHUSETTS

SPERRY RAND CORPORATION

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SECOND QUARTERLY TECHNICAL REPORT

INVESTIGATION OF NEW CONCEPTS OF ADAPTIVE DEVICES

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I. INTRODUCTION

The monthly letters to date and the first quarterly report give a detailed theoretical analysis of the charge storage behavior of an MI_2I_1S device, as well as the results of certain qualitative experiments. In the present quarterly report we include the results of several experiments, in particular J-E curves, which substantiate the theory. We will show that it is possible to predict the relationship between the applied bias to a device and the charge stored in the device (hereafter referred to as bias-storage curves). From the same data we can also quantitatively establish the charging and discharging times. These three pieces of information characterize the memory behavior of the MI_2I_1S device.

Finally, an analysis of the MI_2I_1S equivalent circuit is given, showing that with the use of a properly designed analog computer, one can extract a representation of the charging current transient. Equipment is now being checked out which will provide a visual display of this function.

II. J-E CURVE PREDICTION OF MEMORY CHARACTERISTICS

In order to determine the J-E characteristics of each layer of a two insulator device separately, a sample similar to that shown in Fig. 1 was prepared. A 10 Ω-cm n-type silicon wafer was chemically cleaned and placed in the boat in the reactor tube. The reactor was brought up to 900°C and a layer of silicon nitride approximately 1000 Å thick was deposited. This layer was "pure" silicon nitride formed by the pyrolysis of extremely pure ammonia and

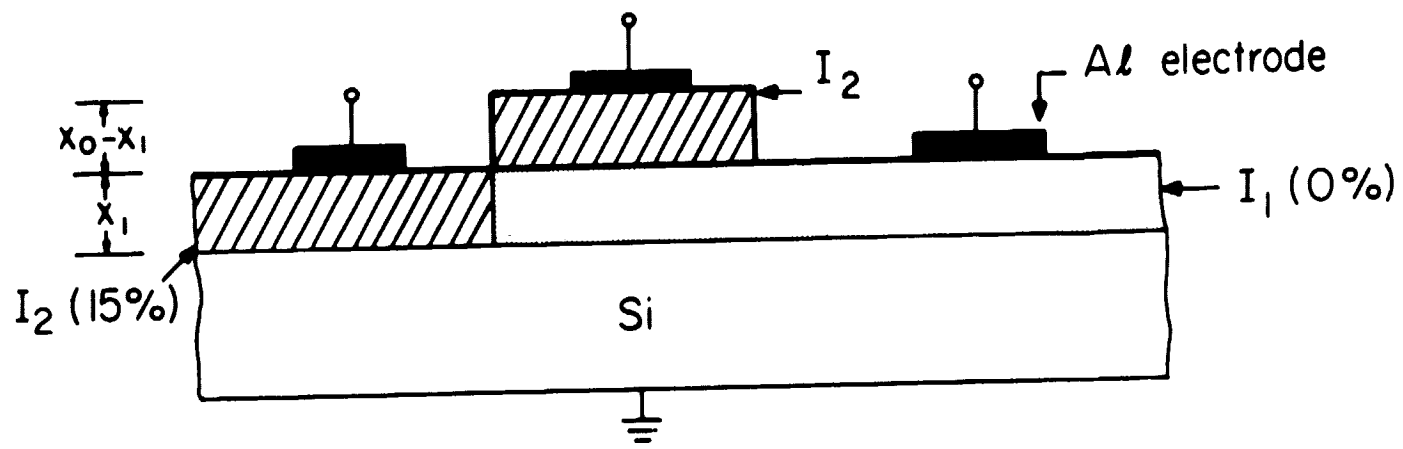

FIG. 1 Schematic representation of device fabrication.

silane with less than 2 ppm of oxygen. Since there was no deliberate injection of O_2, or compounds of O_2, the film is designated 0%. The 0%, or pure silicon nitride, is characterized by a 12 μ IR absorption, a dielectric constant of about 7, an etch rate in buffered HF of about 10 Å/min, and a low insulation resistance.

After this deposition, the silicon wafer was removed from the reactor tube and the silicon nitride was chemically etched away over an area covering about one third of the wafer. The rest of the surface was masked with black wax. The sample, with the wax removed, was then placed in the reactor again and another layer deposited. This time the film was about 850 Å thick. During deposition N_2O was injected at a rate of 15% of the overall flow rate, forming an oxynitride (designated 15%) with an IR absorption of 10.6 μ, a dielectric constant of about 5, an etch rate in buffered HF of about 150 Å/min, and an insulation resistance considerably higher than the 0%-film. After deposition the slice was removed and a portion of the 15%-film was removed, leaving the 0%-film beneath intact (see Fig. 1).

This procedure resulted in separate layers of different conductivity films as well as a composite film. Aluminum dots of 10 mil diameter were evaporated through a contact mask. Then the slice was diced and the individual capacitors mounted on headers. Voltage vs current plots were taken on these samples using a Cary Vibrating-Reed Electrometer Model 31. The volage was applied with a battery supply, and before each current reading was taken, enough time was allowed to elapse so that the current became stable with time. So far, curves have been taken only with a positive bias on the gate electrode. For the n-type substrate we are using, the positive bias on the gate electrode results in an accumulation layer of electrons.

Now these individual J-E curves and the respective dielectric constants completely characterize the two materials used in fabricating the two insulator layer device shown in Fig. 1. From this information, and from the known thickness of the layers, it is possible to predict or estimate the three parameters that describe the memory type behavior of this device, i.e., the bias-storage curve, the charging time for a given charge, and the discharge time for a given stored charge. The bias-storage curve is simply the relationship between the voltage applied to the MI_2I_1S device and the charge stored at the interface between the two insulators. The latter quantity we express as a flatband voltage, that is, the applied voltage necessary to cause the field at the semiconductor-insulator interface to go to zero. This expression, derived in the first quarterly report, is

$$V_{FB} = eN_I(x_o - x_1)/\epsilon_2$$

where eN_I is the stored charge in C/cm^2, ϵ_2 is the dielectric constant of the top layer (I_2), and $x_o - x_1$ is defined by Fig. 1. V_{FB} is a convenient measure of the stored charge since it is approximately equal to the voltage necessary to turn on a field effect transistor whose gate is a MI_2I_1S structure with stored charge eN_I.

Now to predict the V_{appl} vs V_{FB} relationship we proceed as follows. The condition for the equilibrium situation in the device is that the voltage be applied for a long enough time for all displacement currents to vanish. Initially, when a voltage is applied, the following continuity condition holds

$$\frac{dD_2}{dt} + j_2 = \frac{dD_1}{dt} + j_1 = j.$$

However, when sufficient charge builds up at the interface between I_1 and I_2,

$$\frac{dD_2}{dt} = \frac{dD_1}{dt} = 0 \text{ and}$$

$$j = j_1 = j_2.$$

If j flows in an insulating film, then the field in the film, E, must be given by the J-E curve for the material. Therefore, for any steady-state current flowing through both films, the existing fields in the films, E_1 and E_2, may be determined from the I-E plots in Fig. 2. We may therefore take sets of E_1 and E_2 for successively higher values of steady state current and from these sets construct the V_{appl} vs V_{FB} relationship. For a given set E_{1f}, E_{2f}, the accumulated charge is

$$\epsilon_2 E_{2f} - \epsilon_1 E_{1f} = eN_{If}$$

from which $V_{FB} = eN_{If}\ (x_o - x_1)/\epsilon_2$. The V_{appl} corresponding to this set is just

$$V_{appl} = E_{2f}(x_o - x_1) + E_{1f}x_1.$$

These calculations can be made for successive sets of E_{1f} and E_{2f} until the complete V_{appl} vs V_{FB} plot is constructed.

In Fig. 3, we show the calculated and experimental bias-storage curves for the combined layers, and in Fig. 4 we show the experimental curves for the individual layers. A few words of explanation are in order for these graphs. First, the positive bias and negative bias curves were taken on separate capacitors for all three configurations (MI_1S, MI_2S, MI_2I_1S), and since there were variations in the initial C-V offset voltage, there is a slight discontinuity at

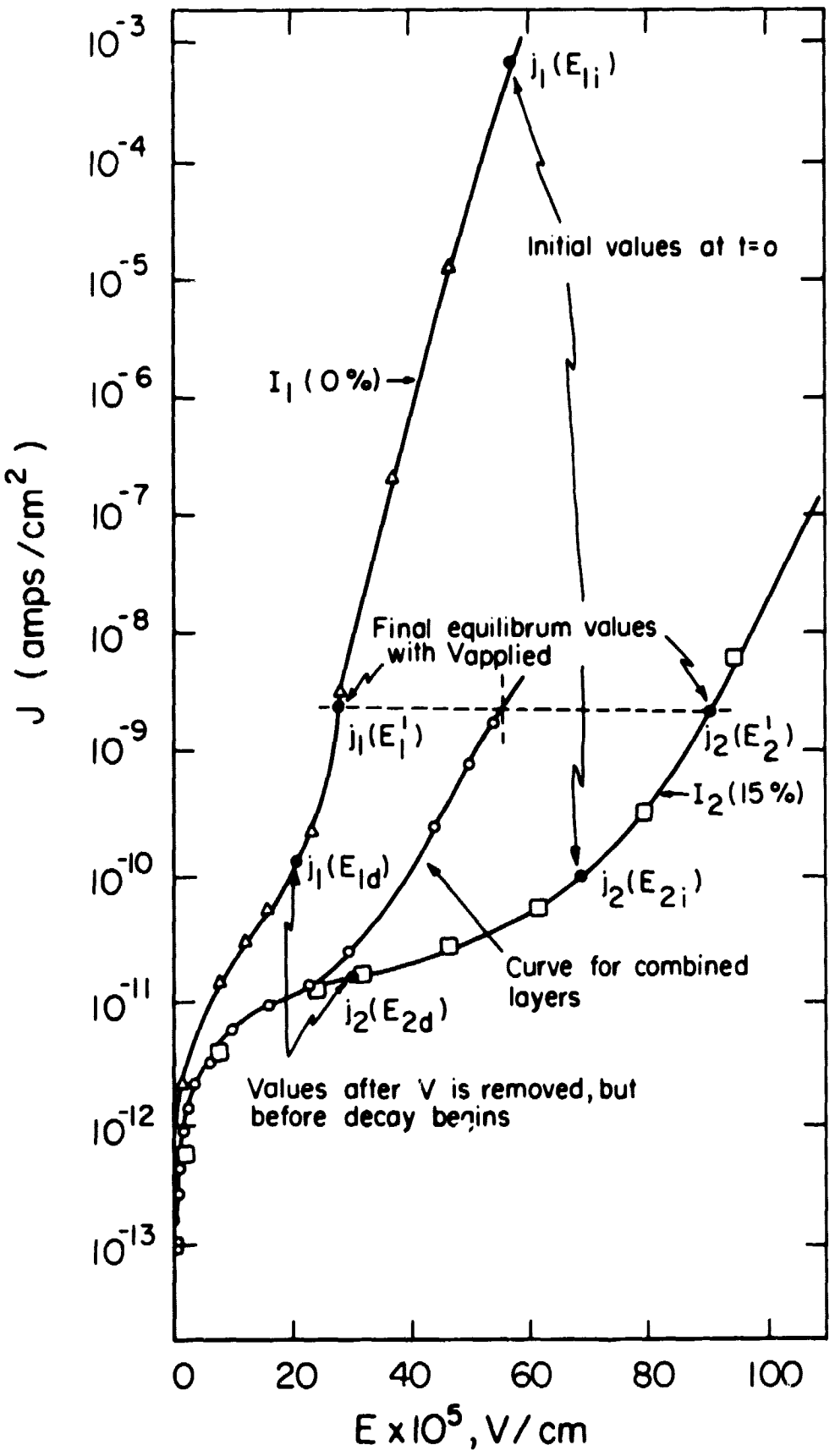

FIG. 2 Experimental J-E curves.

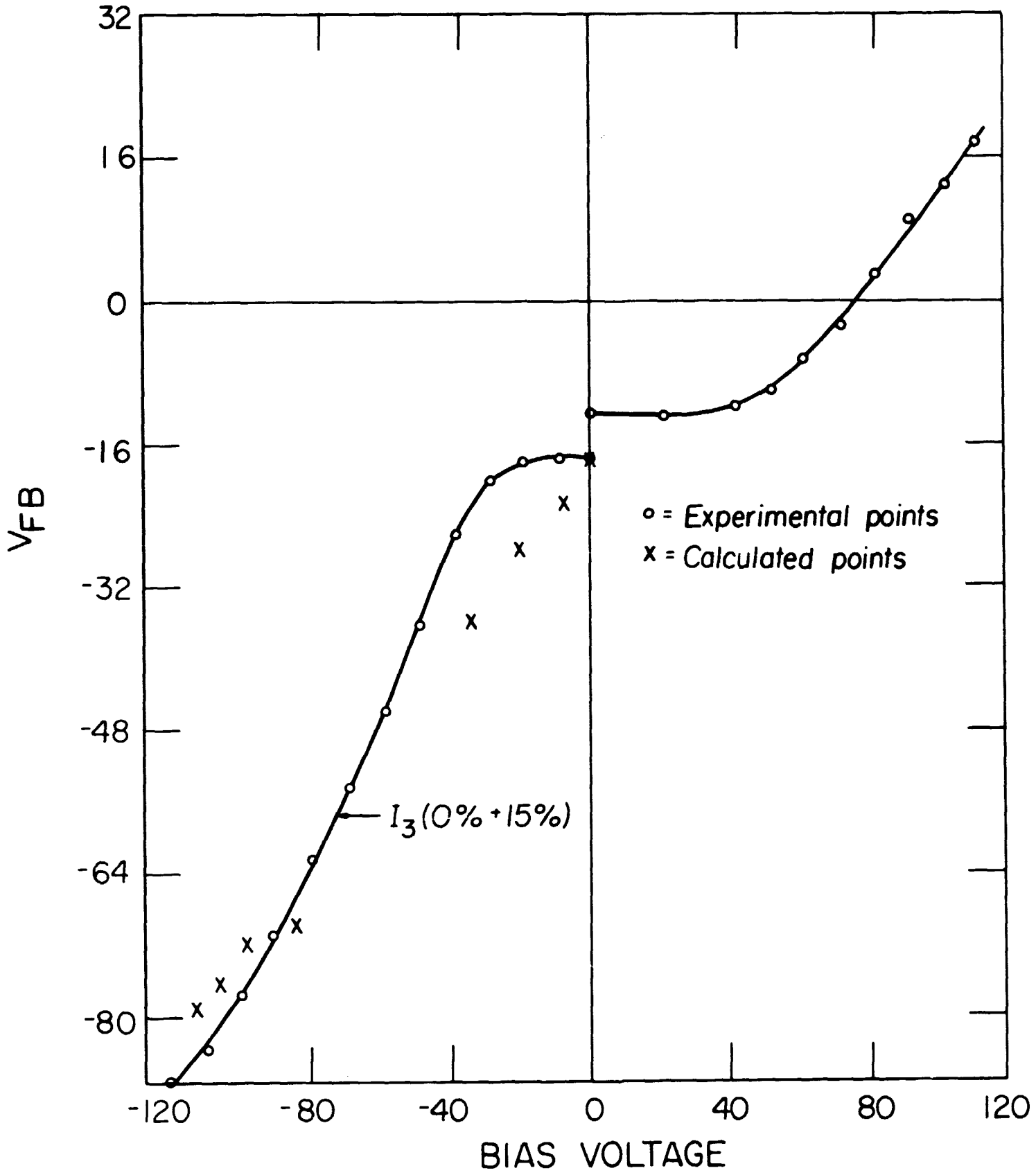

FIG. 3 Storage-bias curves for MI_2I_1S device.

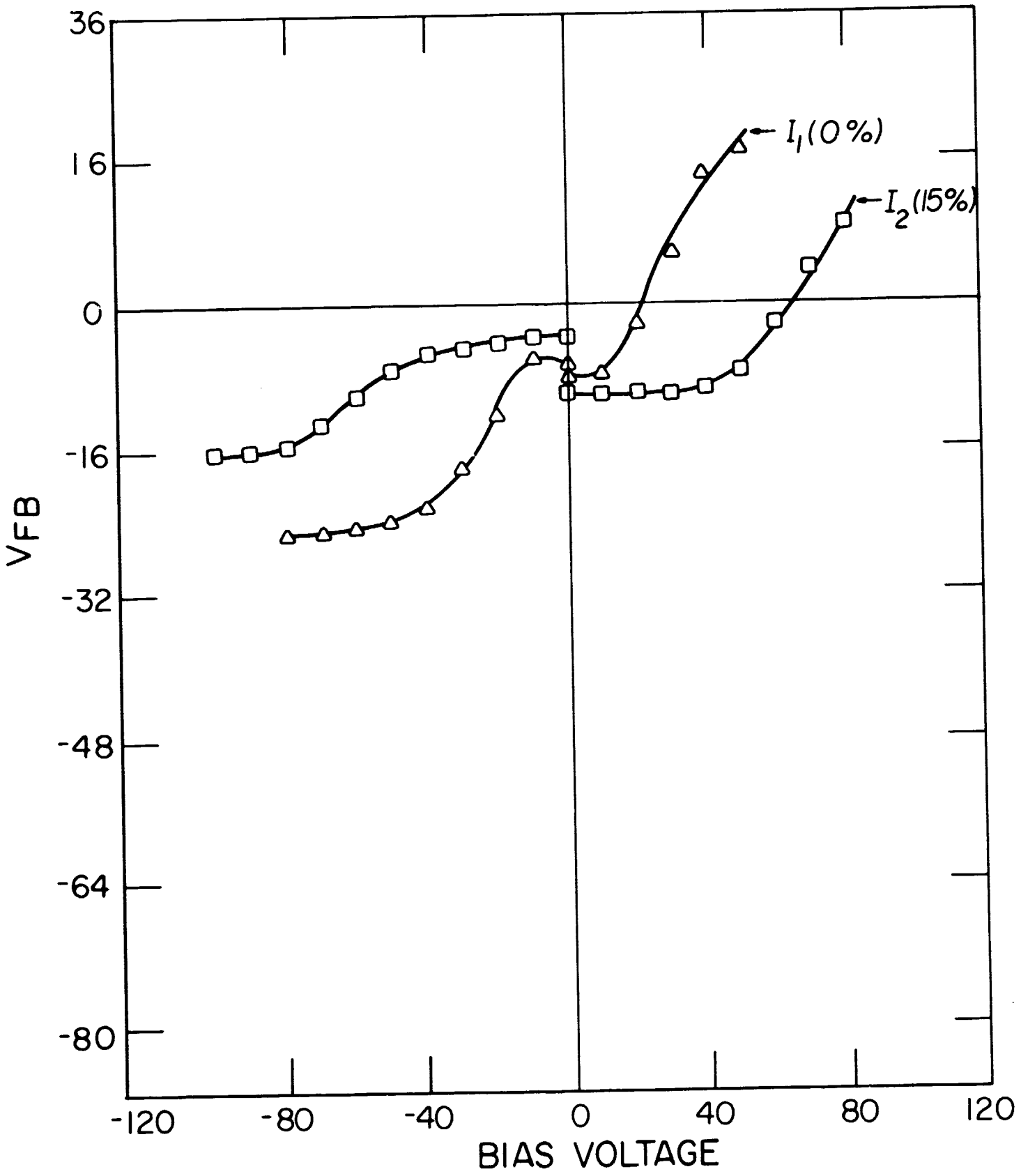

FIG. 4 Storage-bias curves for separate layers I_1 and I_2.

the V=0 line. First, consider the effect on V_{FB} of a positive bias. Both single layer samples (Fig. 4) exhibit a negative charge storage (positive V_{FB}) not considerably different from that of the composite layer (Fig. 3). Some storage effects in single layers of silicon nitride are to be expected because there is an observable gradation of certain nitride properties near the interface; in particular, the etch rate increases, implying the possibility of a silicon-rich nitride layer with a higher conductance than that of the remaining film. However, for a positive V_{appl}, the combination film (Fig. 3) does not show significantly more storage than the individual layers. At present, this phenomenon is still unexplained. For a negative applied bias, however, there is a pronounced difference between the combined layer and the single layers, indicating charge storage at the interface between I_1 and I_2. (The calculated curve showing this charge is also shown in Fig. 3.) This was determined as previously described and then corrected by adding to the combined layer V_{FBf} the V_{FBf} that had been determined experimentally for the layer I_1, using the appropriate E_1. The agreement with the experimental curve is fair, considering the approximations and assumptions that were made. The fact that the J-E curves were taken with a positive bias and the charge storage measurements were made with a negative bias may lead to some discrepancy, since we are neglecting the space charge effects mentioned earlier and also since there could be interface injection effects that depend on polarity.

Another experiment was performed independently to determine the location of the stored charge in the double layer system. This work involved storing charge in the system by application of a large negative bias, thinning the sample in steps by etching, and then measuring the C-V offset (V_{FB}) after each step. A control sample was also biased so that any decay effects with time could be

accounted for. Figure 5 shows a plot of V_{FB} measured vs the total thickness x_o of the dielectric. It is evident that a distinct change in slope occurs at a distance from the silicon that is equal to the thickness of the layer I_1. This change in slope indicates that the charge stored at the I_1-I_2 interface was localized, and therefore could be removed in one etching step. Thus the assumed distribution has, at most, a width of the thickness of this step, or about 200 Å. This justifies the simple delta function distribution of stored charge used in the development of the theory. Assuming a charge density eN_I at the interface of I_1 and I_2 and a charge density of N_{ss} at I_1 and the silicon, the relations between V_{FB} and x_o and x_1 are given by

$$V_{FB} = eN_I(x_o - x_1)/\epsilon_2 + eN_{ss}[\epsilon_2 x_1 + \epsilon_1(x_o - x_1)]/\epsilon_1\epsilon_2 \text{ for } x_o > x$$

and

$$V_{FB} = eN_{ss}x_o/\epsilon_1, \text{ for } x_o < x.$$

The slope M_I is the differential dV_{FB}/dx_o of the first expression, the slope M_{ss} that of the second. In terms of the slopes M_I and M_{ss}, the ratio of the stored charges becomes

$$\frac{N_I}{N_{ss}} = \frac{M_2\epsilon_2 - M_1\epsilon_1}{M_1\epsilon_1} \approx \frac{M_2 - M_1}{M_1} = 5.$$

Approximately the same estimate is obtained from the storage-bias curves.

It is appropriate now to discuss the subject of charging and discharging times. It is in this area that the essence of the memory behavior requirements must be met, i.e., a rapid charge time and a slow discharge time.

These requirements are met by using materials with appropriately nonlinear J-E characteristics such as displayed in Fig. 2. We can estimate the charging time as follows:

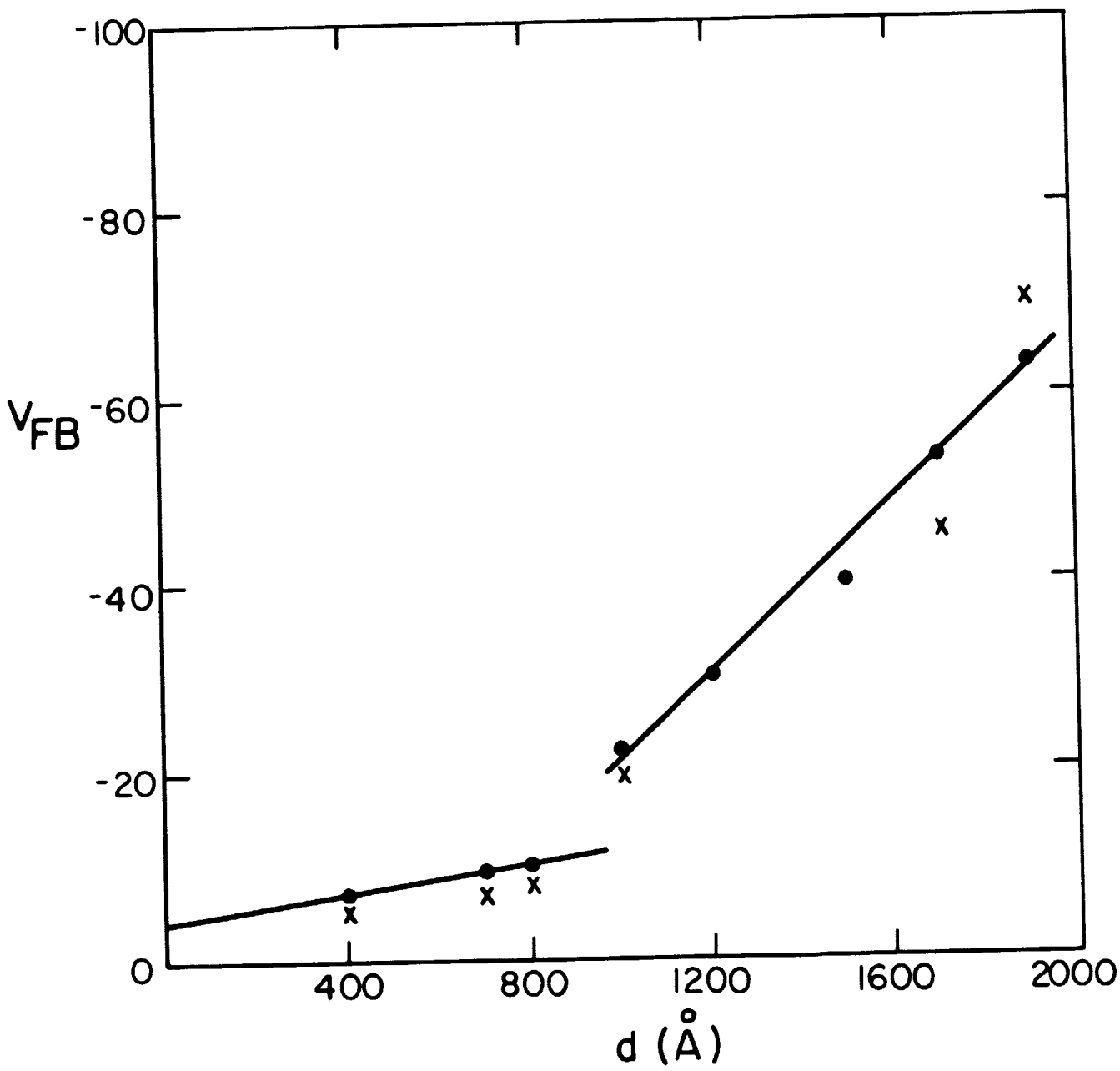

FIG. 5 V_{FB} vs thickness for step-etched sample.

First, we assume that there is negligible series resistance in the charging circuit, so that at the application of a voltage V_{appl}, the external capacitor plates are fully charged before internal charging begins. At t = o, no charge has accumulated at the interface so that the initial fields E_{1i} and E_{2i} are given by the conditions

$$\epsilon_2 E_{2i} - \epsilon_1 E_{1i} = 0,$$

and

$$E_{2i}(x_o - x_1) + E_1 x_1 = V_{appl}.$$

Solving for E_{1i} and E_{2i} gives

$$E_{1i} = \frac{\epsilon_2 V_{appl}}{(x_o - x_1)\epsilon_1 + \epsilon_2 x_1}$$

$$E_{2i} = \frac{\epsilon_1 V_{appl}}{(x_o - x_1)\epsilon_1 + \epsilon_2 x_1} \quad .$$

For V_{appl} = 100 v, and using the appropriate parameters for the devices, $E_{1i} = 5.81 \times 10^6$ and $E_{2i} = 6.98 \times 10^6$. These values are shown in Fig. 2. Immediately after t = o, charge will begin to build up such that j_1 and E_1 will decrease as given by the J-E curve for I_1, and j_2 and E_2 will increase according to the J-E curve for I_2. Finally, the two currents will become equal so that $j = j_1(E_1 f) = j_2(E_2 f)$. Now according to the equation of continuity,

$$\frac{dD_2}{dt} - \frac{dD_1}{dt} = \frac{d(eN_I)}{dt} = j_1 - j_2$$

$$\Delta t = \frac{\Delta eN_I}{j_2 - j_1} = \frac{\epsilon_2 \Delta V_{FB}}{(x_o - x_1)(j_2 - j_1)} \quad .$$

To calculate Δt as a function of stored charge increment, we must know over what range E_{1i} and E_{2i} change to give ΔV_{FB}. Then the appropriate j_1 and j_2 may be estimated from the experimental J-E curves. We assume a ΔE, and from this calculate a new E_1, a new E_2, and therefore, a ΔV_{FB}. Then we repeat the process and calculate Δt as a function of ΔV_{FB} from the last expression. The results of such a calculation, along with experimental points, are shown in Fig. 6. The initial V_{FB} for this curve is 17.5 v. The agreement is excellent.

Estimating the decay or discharge time presents somewhat more difficulty. Immediately after the removal of the applied voltage V_{appl}, the fields E_1 and E_2 take on new values E_{1d} and E_{2d}, depending on eN_I and on the conductance laws. The instantaneous values of E_{1d} and E_{2d} after the removal of V_{appl} and before discharge conduction starts are given by

$$E_{1d} = \frac{-eN_I(x_o - x_1)}{\epsilon_2 x_1 + (x_o - x_1)\epsilon_1} = \frac{-V_{FB}\epsilon_2}{\epsilon_2 x_1 + (x_o - x_1)\epsilon_1}$$

$$E_{2d} = \frac{\epsilon N_I x_1}{\epsilon_2 x_1 + (x_o - x_1)\epsilon_1} = \frac{V_{FB}\epsilon_2 x_1/(x_o - x_1)}{\epsilon_2 x_1 + (x_o - x_1)\epsilon_1}$$

The values have been calculated from the eN_I due to an applied voltage of 100 V, and are shown in Fig. 2 (E_1 is negative, but it is plotted on Fig. 2, and it is assumed that the J-E curves are symmetrical). The stored charge eN_I effectively will now be shared by two capacitors in parallel with the charges on one capacitor given by $\epsilon_1 E_{1d}$, and on the other by $\epsilon_2 E_{2d}$. They will dissipate via currents j_1 and j_2, which are, of course, interdependent. With these instantaneous fields established after the removal of V_{appl}, the instantaneous currents are $j_1(E_{1d})$ and $j_2(E_{2d})$. A rough estimate of the time to reduce V_{FB} to $V_{FB}/2$ is given by

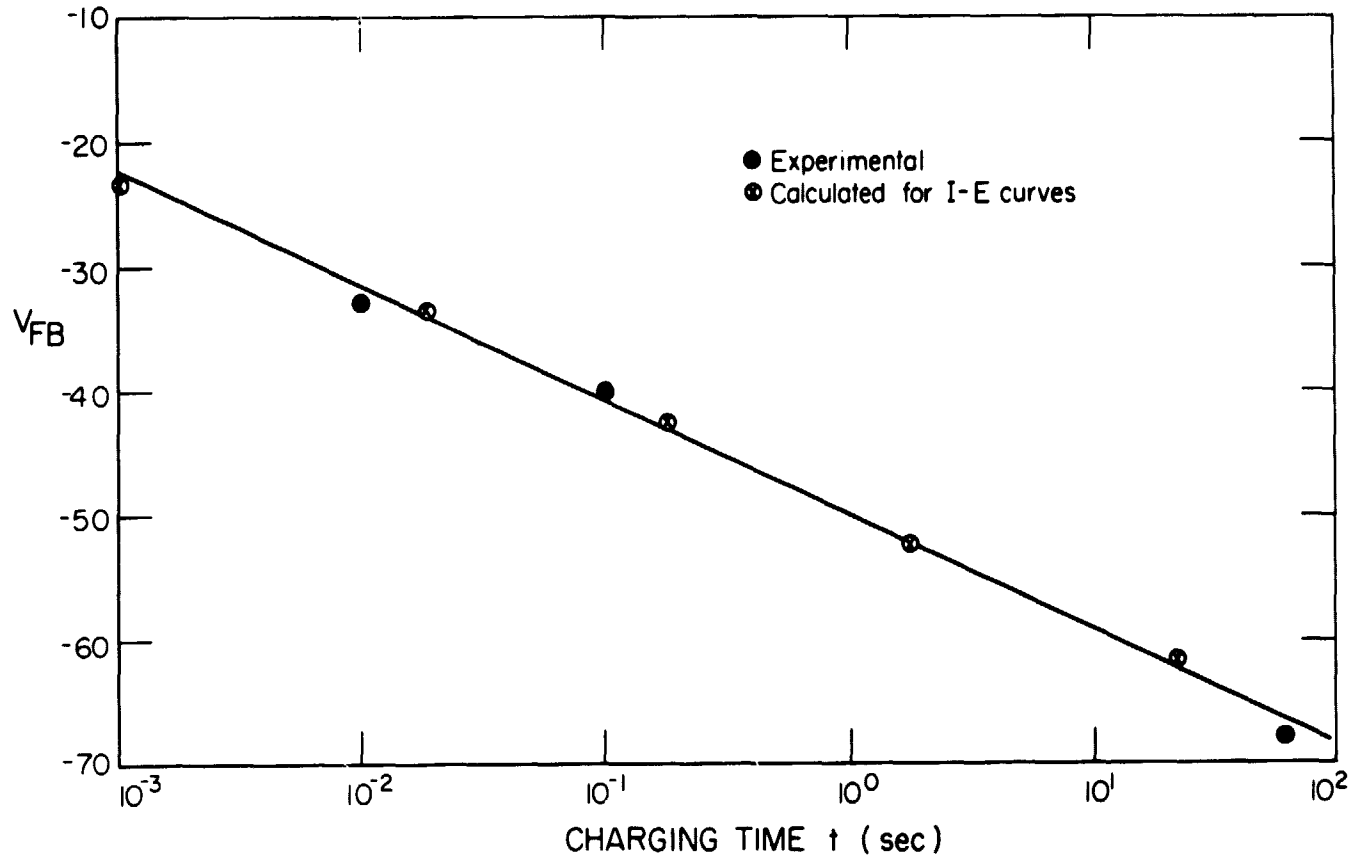

FIG. 6 Charging time vs V_{FB} (for V_{appl} = 100 V).

$$\Delta t = \frac{\epsilon_1 E_1 d/2}{j_1(E_1)} \simeq 80 \text{ min.}$$

Since $j_1(E_1) \gg j_2(E_2)$ this will be the controlling mechanism. (This calculation, of course, assumes a charge removal only by conduction processes. See the first quarterly report for discussion of other possibilities.)

The experimental discharge curve is given in Fig. 7, covering a range up to 30 minutes. In this time period, V_{FB} loses about one third of its value, agreeing qualititatively with predictions that the charge across I_1 decays to half its value in 80 minutes.

III. AN EQUIVALENT CIRCUIT OF THE MI_2I_1S CAPACITOR WITH CHARGE STORAGE

The physical structure of an MI_2I_1S capacitor is shown in Fig. 8. The unique feature of this structure is that the rates of charge flow through these insulators are not equal. With an external bias it is therefore possible to accumulate excess charge at the interface between the two insulators.

This charging process may be represented by the equivalent electrical circuit shown in Fig. 9. The capacitors C_1 and C_2 represent those of the first and second insulators, respectively. The different rates of charge flow through insulators I_1 and I_2. It is also evident that several additional elements have been included in this generalized equivalent circuit. The capacitor C_{SC} is the space charge capacitance associated with a depletion layer in the semiconductor. The resistor R has been added in series with the MI_2I_1S capacitor so that the net charging current i can be observed via a probe with an input capacitance of C_0.

In the present form, the charging terms i_1 and i_2 cannot be separated. It is necessary to construct a device in which only one of the charging terms is

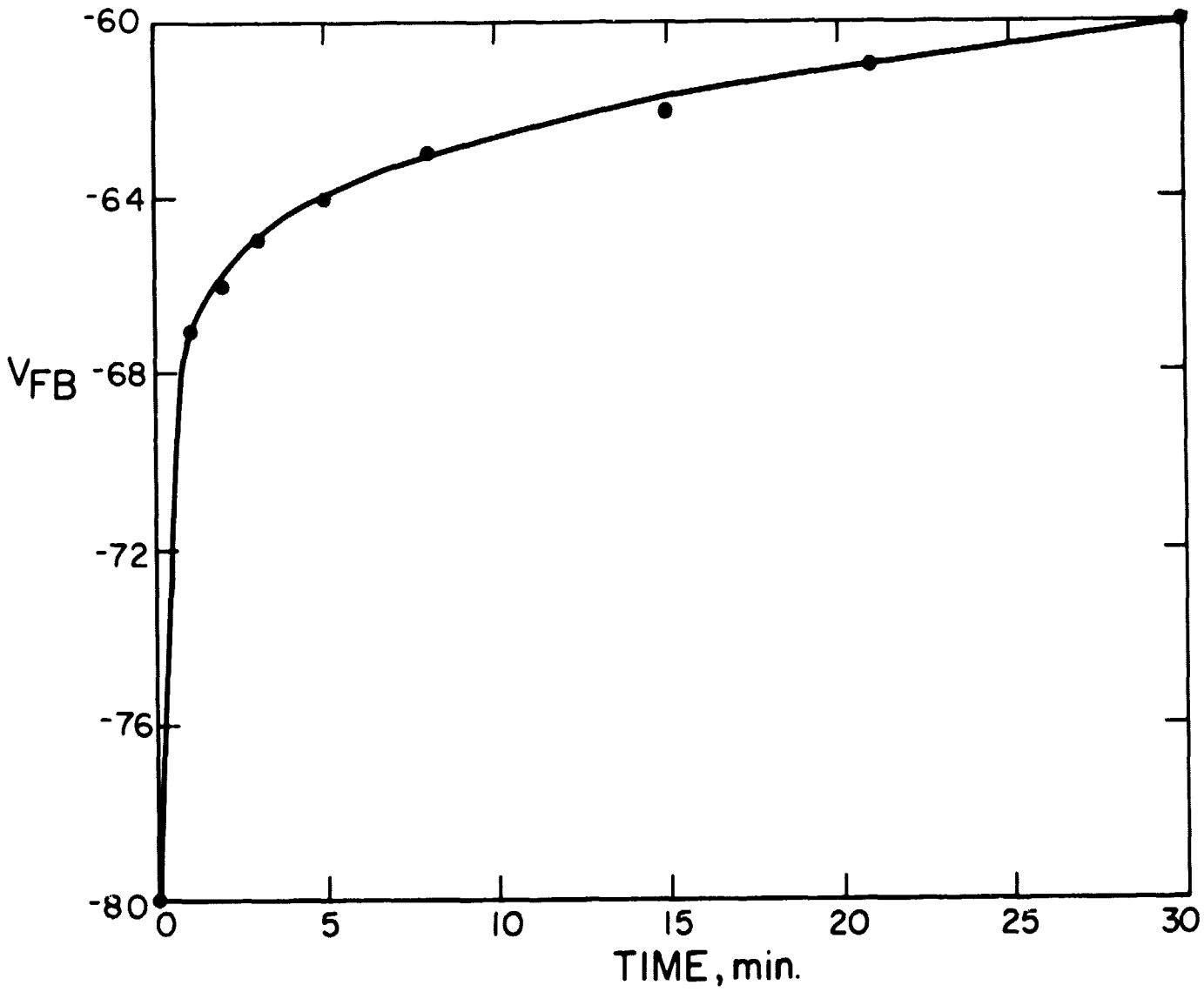

FIG. 7 Decay of V_{FB} with time.

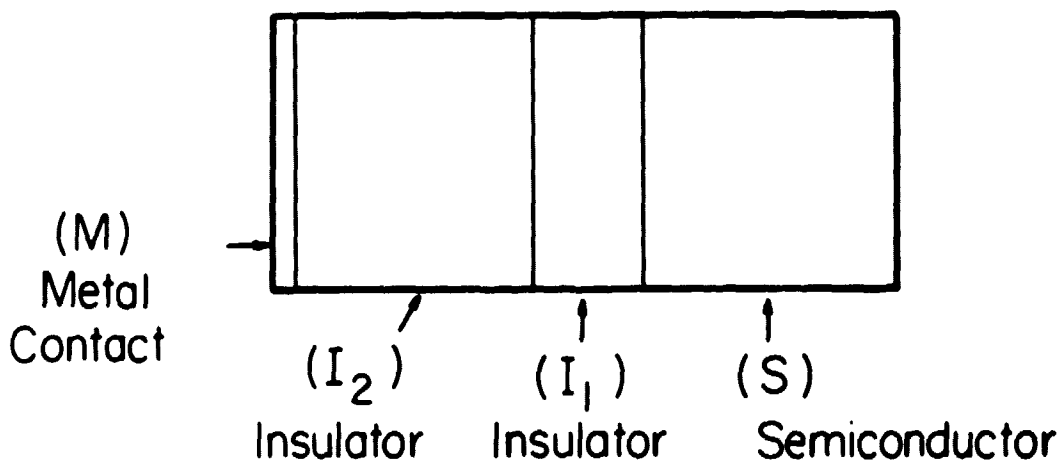

FIG. 8 Physical structure of MI_2I_1S capacitor.

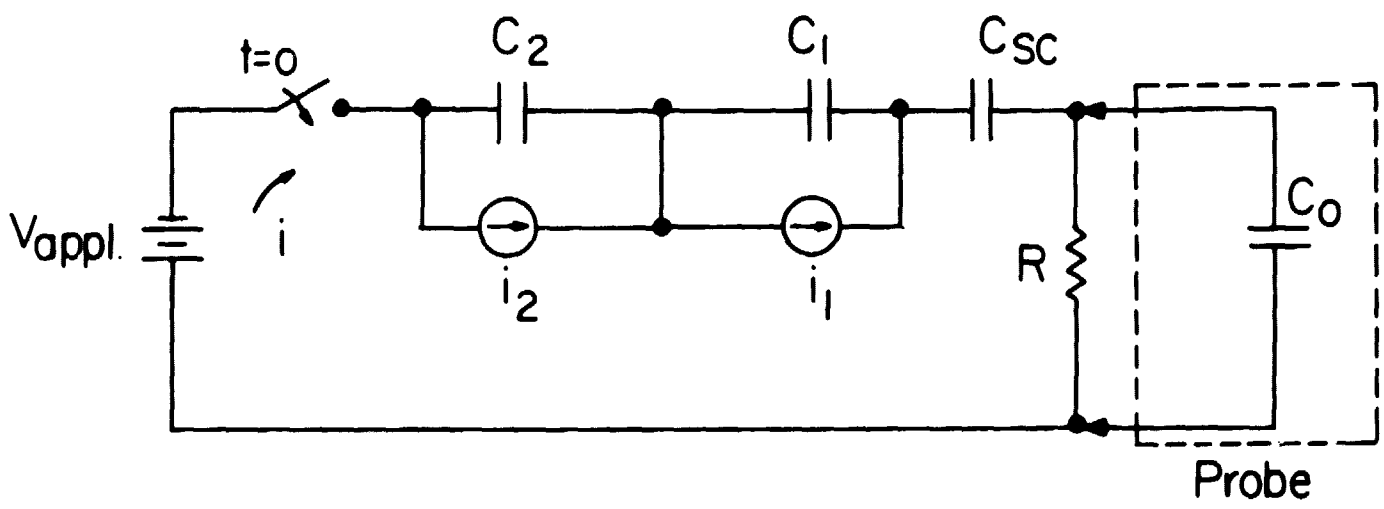

FIG. 9 Complete electrical equivalent circuit of MI_2I_1S capacitor.

dominant, e.g., i_1. The non-linear capacitor C_{SC} may also be eliminated by charging the device so that the semiconductor surface is accumulated and thus behaves as a metal plate. If these two conditions are achieved then the equivalent circuit shown in Fig. 10 is applicable.

In this form it is possible to solve for i_1 and v_1 as functions of time in terms of the measurable node voltage v. The circuit equation is as follows:

$$\text{let } C_1 = \frac{C_1 C_2}{C_1 + C_2}.$$

Then, for $t \geq 0$,

$$C_I \frac{d}{dt}\left[V_a + \frac{1}{C_1}\int i_1 dt - v\right] = \frac{v}{R} + C_o \frac{dv}{dt}.$$

From this equation i_1 may be found to be,

$$i_1 = C_1 \left[\left(1 + \frac{C_o}{C_I}\right)\frac{dv}{dt} + \frac{v}{RC_I} - \frac{dV_{appl}}{dt}\right]. \tag{1}$$

The voltage across insulator I_1 is,

$$v_1 = \frac{1}{C_1}\int i dt - \frac{1}{C_1}\int i_1 dt. \tag{2}$$

In terms of the circuit elements and the measurable parameter v, this becomes,

$$v_1 = -\frac{1}{R}\left(\frac{1}{C_I} - \frac{1}{C_I}\right)\int v dt - \left(1 + \frac{C_o}{C_I} - \frac{C_o}{C_1}\right) v + V_{appl}. \tag{3}$$

The capacitances C_1 and C_2 may be determined from the device geometry. All that is necessary to display the charging current and voltage is an analog computer that will perform the indicated mathematical operations.

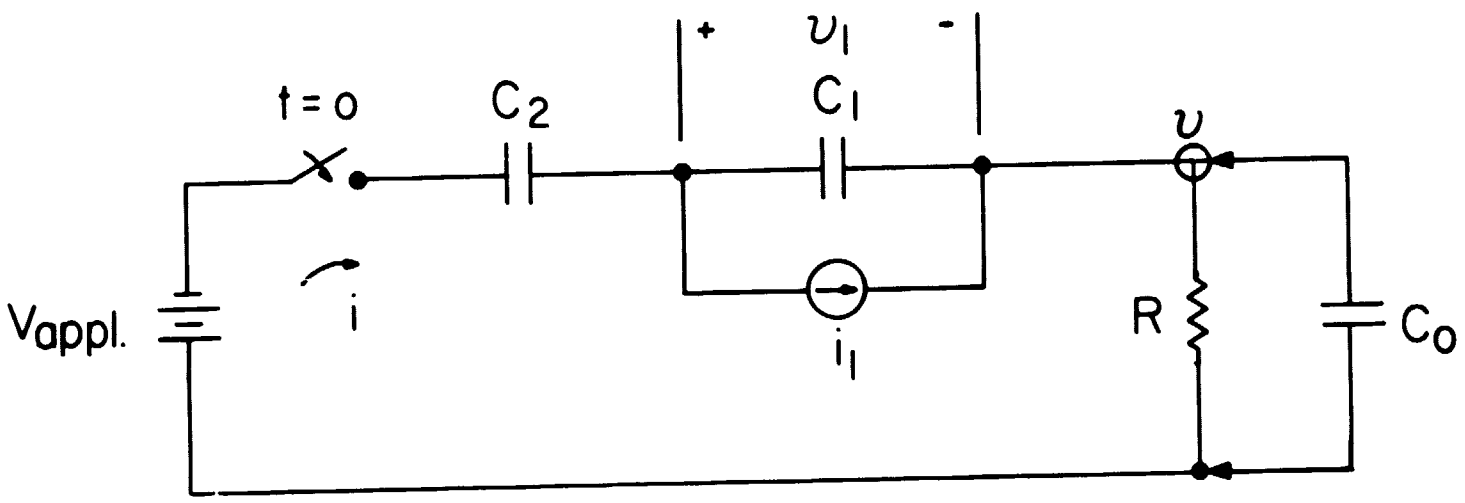

FIG. 10 Simplified electrical equivalent circuit of MI_2I_1S capacitor.

IV. AN ANALOG SOLUTION FOR TRANSIENT CURRENT i_1

A system using wide-band operational amplifiers has been designed that will solve the differential equations for i_1 and v_1 and display them visually on a CRT. This system is shown in Fig. 11.

A generalized operational amplifier arrangement is shown in Fig. 12. The output voltage, V_o, is related to both inputs, V_1 and V_2 by the equation,

$$V_o = - V_2 \frac{Z_f}{Z_2} + V_1 \frac{Zg}{Z_1 + Zg} (1 + \frac{Z_f}{Z_2}),$$

provided the open loop gain of the amplifier, A, is very large.

The following discussion will outline the functions performed by each amplifier in the analog solution shown in Sketch 3. The first amplifier in the diagram is an input stage that senses the voltage, v, in the test circuit of Fig. 10. The input impedance of this stage is 33 megohms in parallel with 6 picofarads. Therefore, the input resistance presents a negligible load on the test circuit, but the input capacitance is comparable to that of the device. This capacitance is included in the test circuit as C_o. The output of the first stage is

$$v_A = (1 + \frac{R_2}{R_1})v, \tag{4}$$

R_2 and R_1 may be chosen so as to amplify the signal. This may be desirable since the remaining operations to be performed will then be immune to noise considerations.

The response of the circuit that is generating i_1 is given by the following expressions:

$$v_c = - \frac{R_6}{R_5} (1 + \frac{R_2}{R_1}) \int v dt + \frac{R_9 R_4}{R_8 R_3} (1 + \frac{R_2}{R_1}) v + \frac{R_9}{R_7} V_a \tag{6}$$

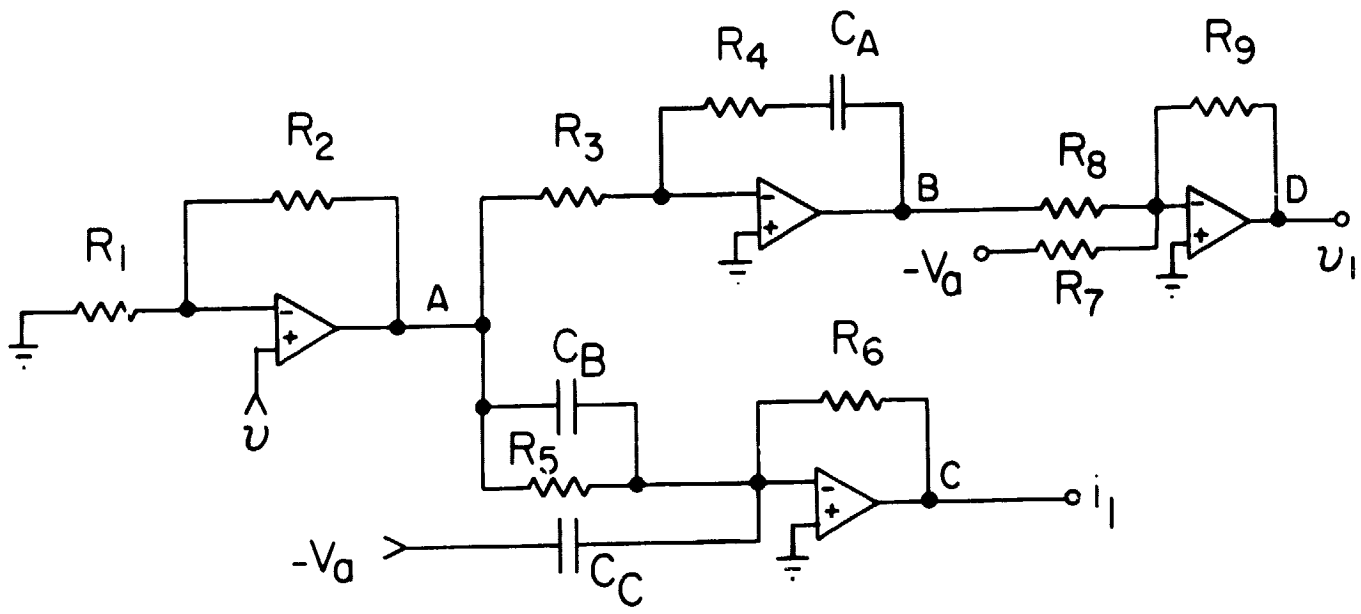

FIG. 11 Analog solution for i_1 and v_1.

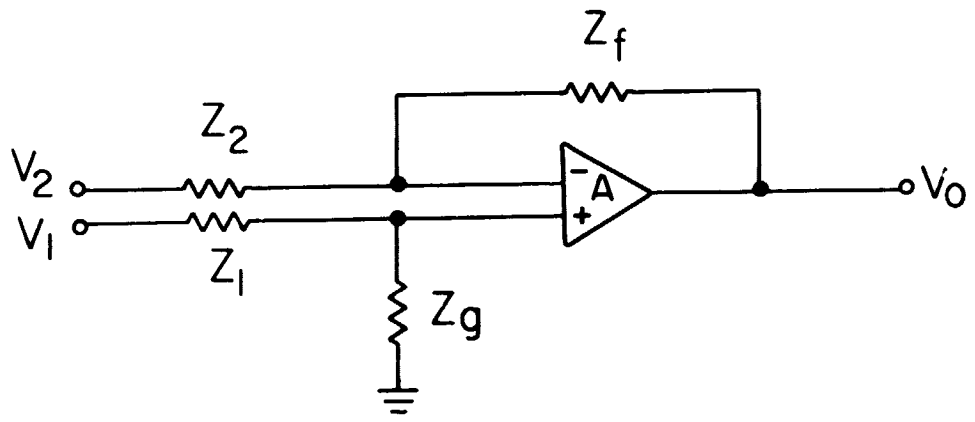

FIG. 12 Generalized operational amplifier.

The form of Eq. (6) is equivalent to that of v_1. Again, as for the expression for $-i_1$, these coefficients may be adjusted to give any multiple of v_1.

This analog computer has been assembled with elements that generate $-200\ i_1$ and $2v_1$. The voltage V_{appl} will be supplied by a function generator that controls the response time. The complete system is in the process of being adjusted and checked out.

V. SUMMARY

In conclusion, we find that the memory properties of the MI_2I_1S structure depend entirely on the electrical conductivity properties of the separate insulating layers and on their dielectric constant and thickness. In addition, we have shown that by proper circuit design, it will be possible to display a dynamic I-V curve for a composite device. This will be useful for comparison with the static curves. In the following months, we intend to accumulate extensive data on an entire series of oxynitride, from which the memory characteristics may be optimized, and put into operation the special analog computer.

NEW TECHNOLOGY APPENDIX

Utilization of Two Modifications of Silicon Nitride in the Formation of Memory Structures

On pages 1 and 2 of this report, the two layers of different conductivity required by the memory device theory were both formed from silicon nitride. The layer of high conductivity was fabricated from silicon nitride containing no oxygen, the layer of lower conductivity was fabricated from silicon nitride formed in the presence of 15% N_2O during deposition.