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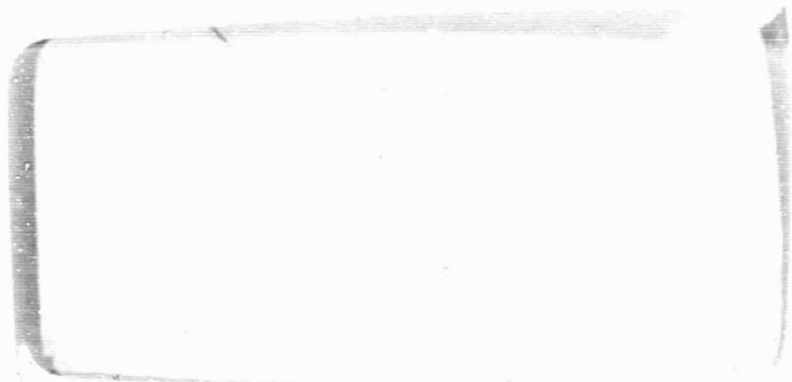

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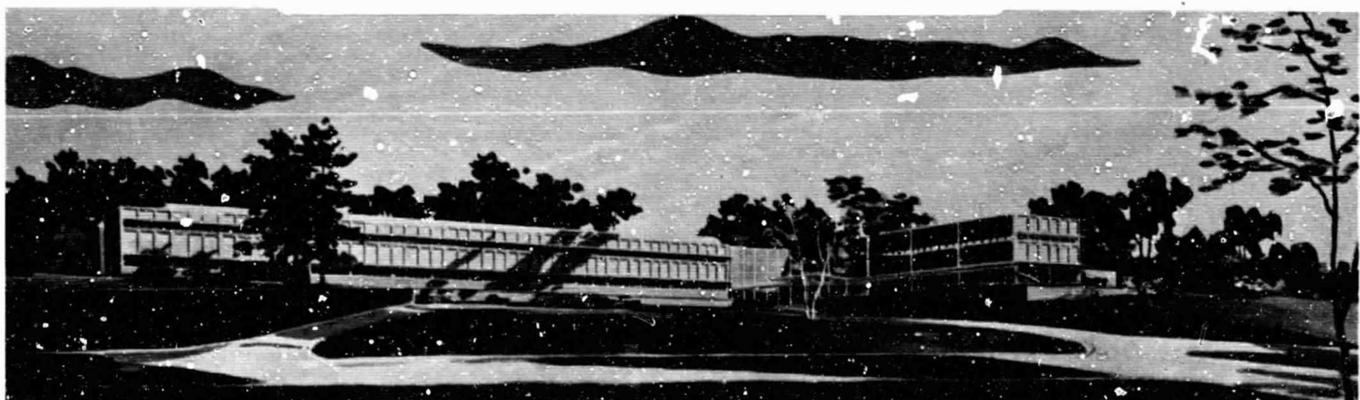

SPERRY RAND

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SUDBURY, MASSACHUSETTS

SPERRY RAND
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FIFTH QUARTERLY TECHNICAL REPORT

INVESTIGATION OF NEW CONCEPTS OF ADAPTIVE DEVICES

Contract No. NAS 12-570

Period Covered:
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Prepared for

NASA Electronics Research Center
Cambridge, Massachusetts

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I. INTRODUCTION

The overall goal of the present work is to achieve a more complete understanding of the MI_2I_1S memory device. Such an understanding should yield a thorough knowledge of all the participating conduction mechanisms to the point of device predictability. Five conduction mechanisms are probable in this structure (two bulk and three interface mechanisms). With a thorough knowledge of the various conduction laws, the chemical constituents can be modified for optimum performance characteristics. The effects of external stimulants such as heat and light will also be studied as to their perturbations on the conduction properties and, hence, the charge storage characteristics.

This first report discusses the results obtained on silicon wafers that were subjected to high temperature surface treatments prior to the deposition of silicon nitride and the effect of light on the charge storage properties of the silicon nitride memory capacitor.

The surface treatments consisted of exposing silicon surfaces to hydrogen and ammonia ambients at $1250^{o}C$ prior to the deposition of silicon nitride. The deposition was performed in hydrogen at $900^{o}C$. This approach resulted in a different surface and revealed some interesting features on interface conduction mechanisms.

The effect of light on the charge storage properties of a memory capacitor was studied and shown to be related to a space charge layer in the silicon adjacent to the insulator. With a relatively intense light directed on the surface of the device this space charge layer can be practically eliminated.

II. EFFECT OF SILICON SURFACE TREATMENTS ON THE CHARGE STORAGE CHARACTERISTICS

A. Introduction

A series of silicon wafers were subjected to various high temperature surface treatments prior to the pyrolytic deposition of silicon nitride. These treatments consisted of exposing the surfaces of silicon wafers to a hydrogen ambient and to various concentrations of ammonia in hydrogen at 1250°C for 30 minutes. The nitride deposition was then performed in hydrogen after reducing the temperature to 900°C.

The reason for these high temperature treatments was to attempt to obtain an oxide-free silicon surface. In the present form of the memory device, two physically distinct insulators in series with silicon have been utilized for the establishment of a layer of charge. This layer would exist at the interface between the two insulators. When no special attempt is made to remove the silicon surface oxide prior to the deposition of silicon nitride, the resulting insulator structure would consist of a thin layer of silicon oxide (30 to 50 angstroms) followed by a predetermined thickness of silicon nitride. This is then referred to as an MI_2I_1S structure. If the two layers have different conduction characteristics, charge will accumulate at their interface which can be expressed by

$$\sigma = \epsilon_1 E_1 - \epsilon_2 E_2 \tag{1}$$

In an actual two layer structure there are a maximum of five conduction laws to consider. Three of these are due to interface conduction mechanisms and two are due to bulk conduction mechanisms. The interfaces exist between the silicon and the first insulator, the first and second insulator,

and the second insulator and the metal. The bulk regions are those of the two insulators. A representation of this is shown in Fig. 1. Note that the arrows representing the direction of the current across each interface have different magnitudes. This is done to account for the possibility of directional electronic energy barrier differences. An analog to this would be the rectification property inherent in a Schottky barrier diode or a semiconductor junction diode.

If the bulk conduction mechanisms are dominant then the charge storage can be determined from a knowledge of only the insulator conduction laws. However, if this is not the case, and one or more of the interface conduction mechanisms are dominant, then both the bulk conduction laws and the dominant interface conduction laws must be considered in a charge storage analysis.

When one of the insulator layers has been successfully removed then the conduction representation shown in Fig. 2 is applicable. It is noted that there are now only three possible conduction mechanisms. If there are no significant interface energy barriers then this device should not be capable of storing charge. In fact, this structure is very useful for isolating the insulator-silicon interface, since any charge stored in the insulator near the metal-insulator interface has almost no effect on the flatband voltage, which is the parameter used to indicate the existence of charge storage. Its effect would be that of a non-linear resistor. The analysis presented in Section 3 shows that this non-linear resistance is relatively small such as to be analytically negligible.

B. Experimental Results

From the various "oxide-free" silicon-silicon nitride wafers formed by the processes described above, capacitors were constructed for transient and

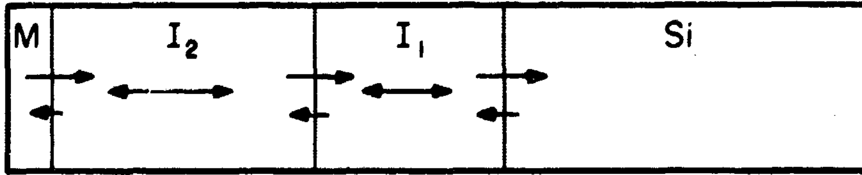

FIG. 1 Representation of conduction mechanisms in MI_2I_1S memory device.

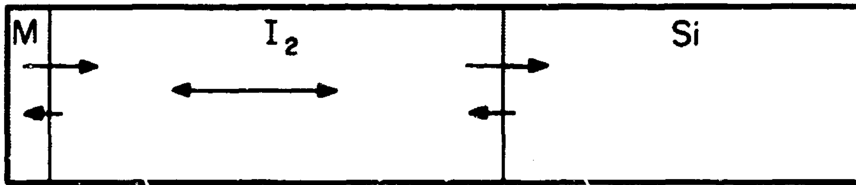

FIG. 2 Representation of conduction mechanisms in MI_2S memory device.

static measurements. Initial pulse measurements on these capacitors indicated that a large amount of charge was being stored in the insulator structure. With the aid of an analog computer it was ascertained that the location of the charge center varied between 20 and 50 angstroms. When these results are compared to those obtained from wafers that were not surface treated prior to the deposition of silicon nitride, it is apparent that the charge center is appreciably closer to the silicon surface. For untreated wafers the center of charge was between 50 and 100 angstroms away from the surface of the silicon and did not shift appreciably with variations in the magnitude of the charging pulse. As the pulse amplitude was increased on the capacitors formed from treated wafers, the center of charge increased in distance from the silicon surface. The results of the analog computer solution for the center of charge on two devices are shown in Table I. One of these devices had an in situ oxide while the other presumably did not. The pulse sequence is one that has been described in an earlier report. It consists of a negative reset pulse followed by a positive truncated ramp. During the application of the ramp the analog computer generates a function that is proportional to the location of the center of charge. By varying the magnitude of the truncated ramp, the amount of charge being transferred is changed. For the case of an in situ oxide layer, a physically distinct insulator-insulator interface exists where charge may accumulate. When this layer has been removed, any charge storage in the remaining insulator must occur in electronic trapping centers. Since there is a finite density of such centers, as more charge is being introduced into the traps, it must occupy a greater volume of the insulator. Therefore, the charge center will move away from the silicon. This is evidenced in the experimental results.

TABLE I

PULSE	CHARGE CENTER
(-80)(+30)	52Å
(-80)(+40)	50Å
(-80)(+50	51Å

(a)

PULSE	CHARGE CENTER
(-80)(+40)	19Å
(-80)(+45)	23Å
(-80)(+50)	37Å

(b)

ANALOG COMPUTER SOLUTION FOR CENTER OF CHARGE

(a) Device with insitu oxide.

(b) Device with high temperature surface treatment.

From these initial observations it was possible to infer that the surface treatments were having a strong effect on the surface oxide. At present, however, it is not possible to conclude whether the oxide was completely removed, greatly reduced in thickness or possibly converted to another chemical species.

1. Analysis of Conduction Laws

In the present theory of the memory device a necessary condition for the accumulation of charge in the insulator is the existence of two different conduction laws. Therefore, by using Eq. (1), the static I vs E_2 characteristic of the nitride, and the static flatband voltage for corresponding fields, it is possible to calculate the I vs E_1 characteristic of the necessary silicon-silicon nitride interface conduction curve.

The calculation of the I vs E_1 conduction characteristic begins by first establishing the I vs E_2 characteristic for the silicon nitride. This is obtained through the use of Ohm's Law.

$$V = E_1 x_1 + E_2 x_2 \tag{2}$$

Since $x_1 \ll x_2$, then it is possible to approximate Eq. (2) as

$$V \approx E_2 x_2 \tag{3}$$

Therefore, for each static voltage applied across the device structure a value for E_2 may be calculated. The thickness of the silicon nitride layer deposited on the surface treated wafer presently being considered was 900 angstroms. Table II shows the calculated value of E_2 and the corresponding static current.

For each static voltage applied the amount of injected charge was determined through a measurement of the flatband voltage. This measurement

TABLE 11

Calculation summary for [illegible] vs E_1 characteristic of interface between silicon and pyrolytically deposited silicon nitride.

I(amps)	V(volts)	E_2(V/m)	V_{FB}(volts)	[illegible](coul/m^2)	E_1(V/m)	$1/E_1 (V/m)^{-1}$
4.3×10^{-13}	+30	3.33×10^{8}	0	0	3.33×10^{8}	3.0×10^{-9}
2.4×10^{-11}	+40	4.44×10^{8}	+ 6	-3.72×10^{-3}	3.84×10^{8}	2.6×10^{-9}
9.3×10^{-10}	+50	5.55×10^{8}	+10.2	-6.33×10^{-3}	4.53×10^{8}	2.21×10^{-9}
2.1×10^{-8}	+60	6.66×10^{8}	+13.3	-8.24×10^{-3}	5.33×10^{8}	1.88×10^{-9}
1.5×10^{-7}	+70	7.77×10^{8}	+13.7	-8.5×10^{-3}	6.40×10^{8}	1.56×10^{-9}

was performed rapidly so as to minimize a loss of stored charge. The stored charge, σ, is related to V_{FB} by the equation,

$$\sigma = -\frac{\epsilon_2}{x_2} V_{FB} \tag{4}$$

In this calculation the value for the permittivity is that of silicon nitride, i.e. $\epsilon_2 = 6.2 \times 10^{-11}$ farads/meter.

Now, by using Eq. (1), where ϵ_1 is replaced by ϵ_2, since an oxide interface is assumed not to exist, the calculation of E_1 is obtained.

$$\sigma = \epsilon_2 E_1 - \epsilon_2 E_2 \tag{1}$$

$$E_1 = E_2 + \frac{\sigma}{\epsilon_2} \tag{5}$$

The results of these calculations are shown in Table II along with the reciprocal of E_1. The plots of I vs E_2 and I vs E_1 are shown in Fig. 3.

For comparison, the same calculation was performed on a device having an untreated surface. The results of this are shown in Table III and plotted in Fig. 5. Since an oxide is known to exist between the silicon and the silicon nitride, an oxide dielectric constant was used. The nitride thickness in this case was 600 angstroms.

Since it has been inferred in previous correspondence that the transfer of charge between the silicon and the nitride might be taking place via a Fowler-Nordheim tunnelling mechanism, a plot of I vs $1/E_1$ might reveal this. This plot for the treated wafer is shown in Fig. 4. The linearity of this plot is exceptional. A simplified Fowler-Nordheim expression is shown in Eq. (6).

$$I = I_0 \varepsilon^{-E_0/E} \tag{6}$$

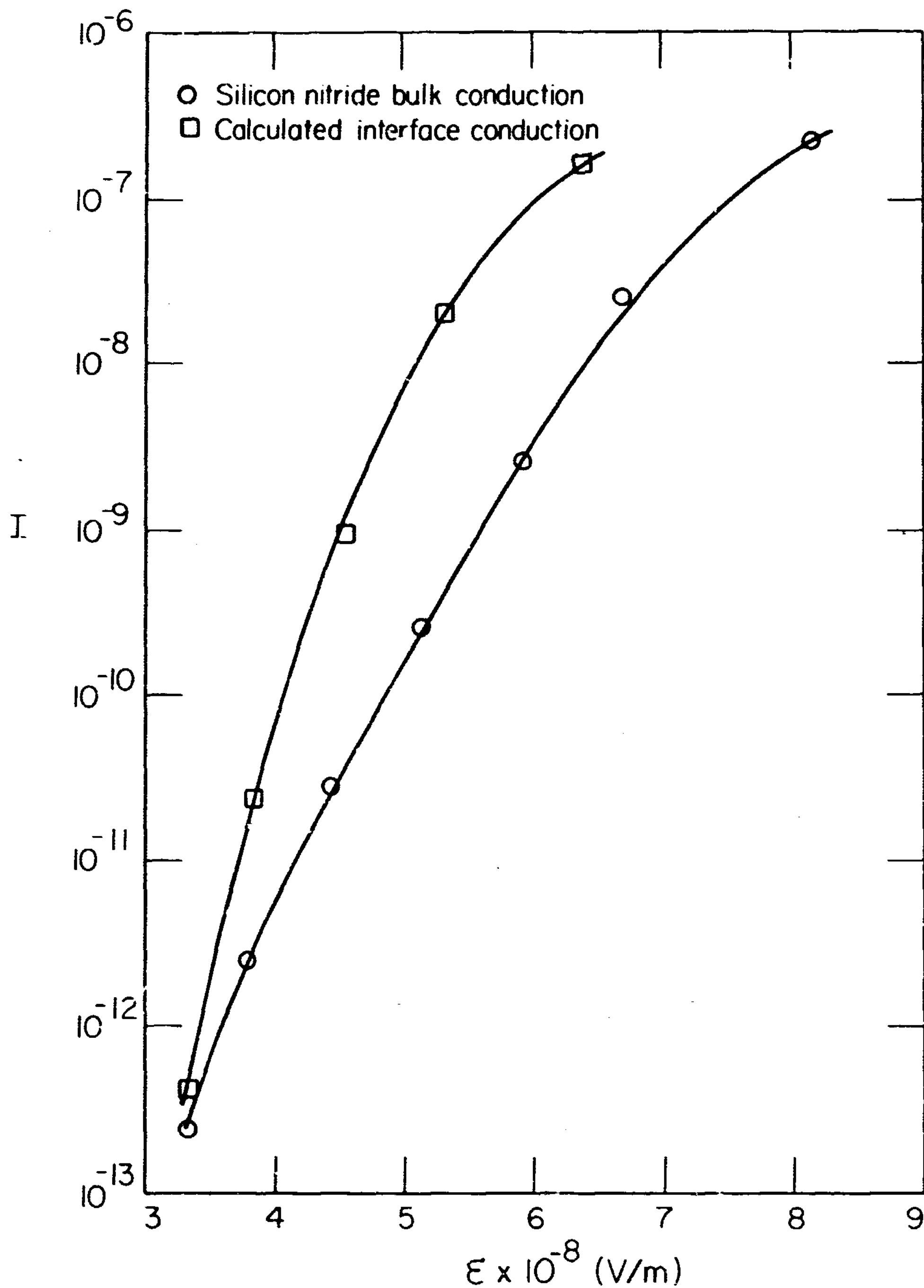

FIG. 3 Current vs field characteristics of conduction mechanisms in a memory device fabricated by pyrolytically depositing silicon nitride on a surface treated silicon wafer.

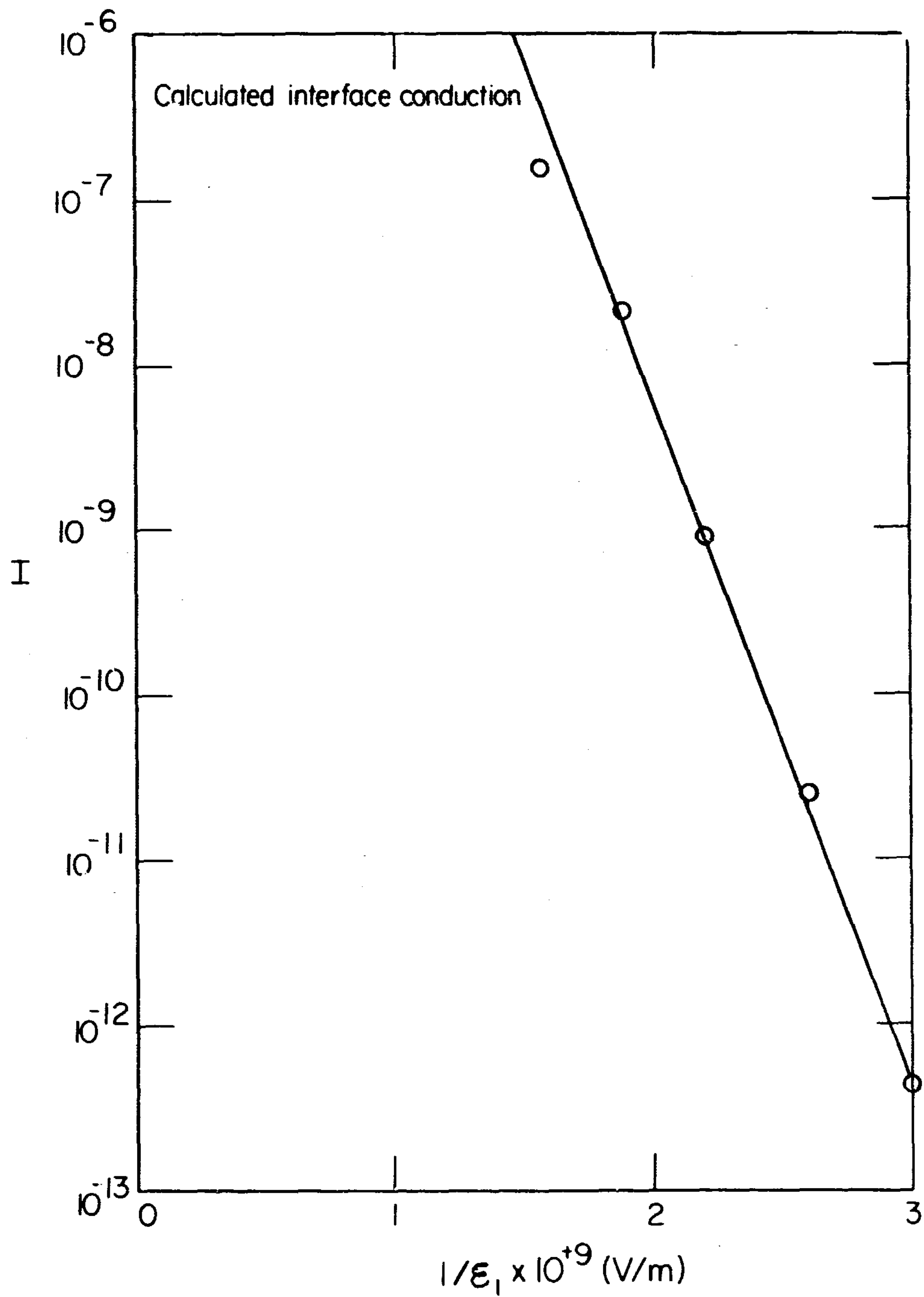

FIG. 4 Current vs reciprocal field for the calculated interface conduction mechanism in a surface treated memory device.

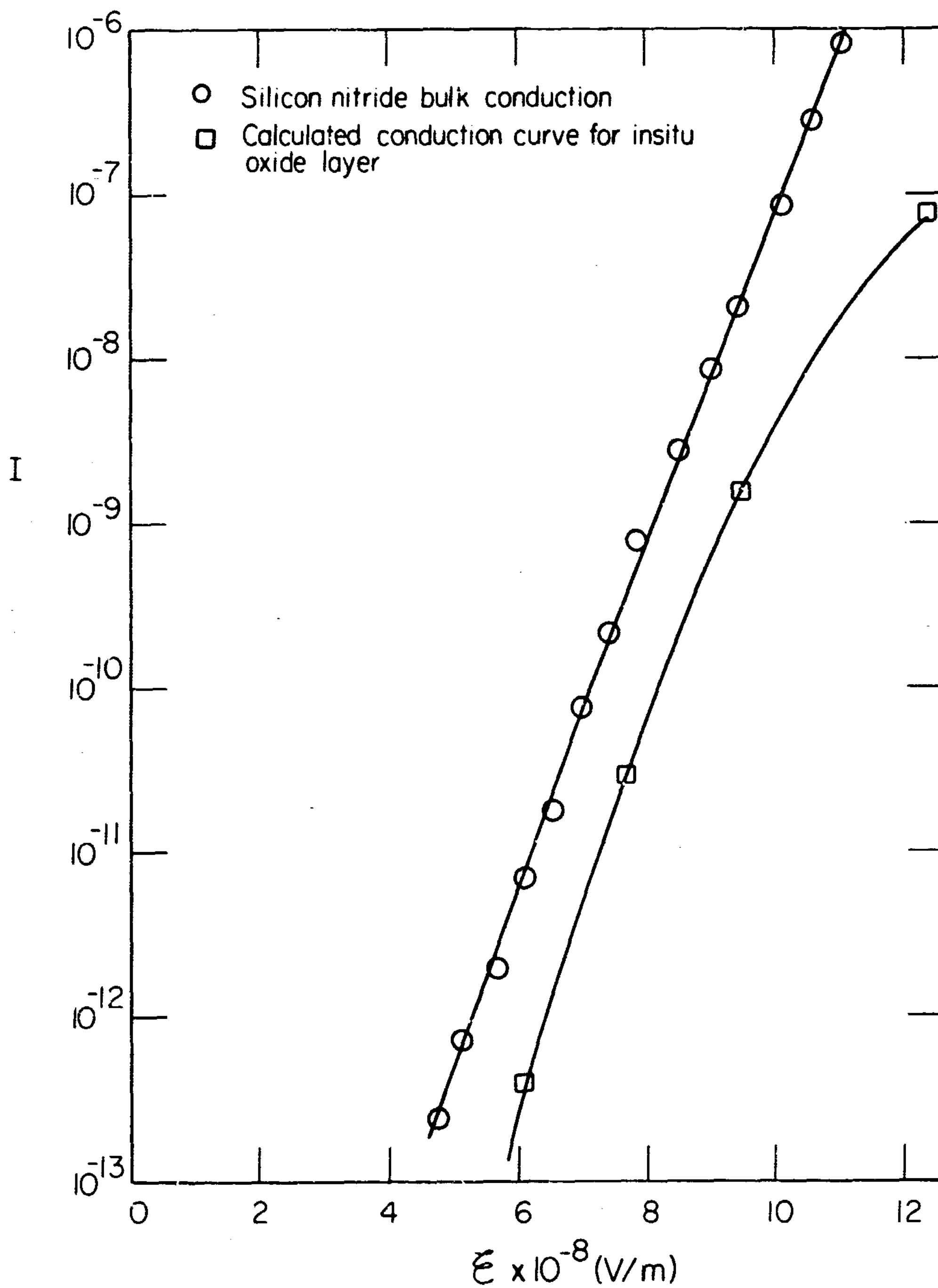

FIG. 5 Current vs field characteristics of conduction mechanisms in a memory device fabricated by pyrolytically depositing silicon nitride on a silicon wafer having an insitu oxide layer.

TABLE III

Calculation summary for I vs E_1 characteristic of interface oxide between silicon and pyrolitically deposited silicon nitride.

I (amps)	V (volts)	E_2 (V/m)	V_{FB} (volts)	-(coul/m^2)	E_1 (V/m)	$1/E_1$ $(V/m)^{-1}$
4.0×10^{-13}	+30	5.0×10^{8}	+ 9.0	-9.26×10^{-3}	6.1×10^{8}	1.64×10^{-9}
3.0×10^{-11}	+40	6.67×10^{8}	+13.5	-13.9×10^{-3}	7.7×10^{8}	1.3×10^{-9}
1.5×10^{-9}	+50	8.33×10^{8}	+17.0	-17.5×10^{-3}	9.5×10^{8}	1.05×10^{-9}
7.5×10^{-8}	+60	10.0×10^{8}	+17.0	-17.5×10^{-3}	12.4×10^{8}	0.81×10^{-9}

where

$$E_o = \frac{4}{3} \frac{\sqrt{2m^*}}{hq} (\Delta e_c)^{3/2}.$$

m^* = carrier effective mass

Δe_c = barrier energy .

Since the effective mass of the carriers is not known, the rest mass of the electron was used in order to calculate Δe_c from the slope of the line in Fig. 4. The value derived for Δe_c is 1.24 eV. This is very close to the theoretical value of 2 eV for the difference in energy between the conduction band of silicon nitride and that of silicon. By using an electron effective mass of 0.24 m_o the theoretical value of 2.00 eV for Δe_c is obtained.

For comparison, a plot of I vs $1/E_1$ is shown in Fig. 6 for an untreated wafer that has an in situ oxide layer. A calculation of the barrier energy, Δe_c, for this wafer using the rest mass of an electron yields 1.75 eV. By using the same effective mass that was used in the previous calculation (i.e. $m^* = 0.24\ m_o$) one obtains a value for Δe_c of 3 eV. This energy is near the theoretical value for the energy difference between the silicon oxide conduction band and that of silicon.

From these results it can be inferred that the basic conduction mechanism is that of tunnelling. For the case of a silicon wafer that has been heat treated in hydrogen or ammonia prior to the deposition of silicon nitride, the assumption of an oxide free interface is possible. This assumes that charges are introduced into the nitride through a surface barrier which can be described by a Fowler-Nordheim relation. Charge storage occurs because the bulk conduction in the nitride (following a Poole-Frenkel law) is smaller than the surface barrier tunnelling described. For the case of an oxide interface, tunnelling occurs through the oxide layer into the silicon nitride.

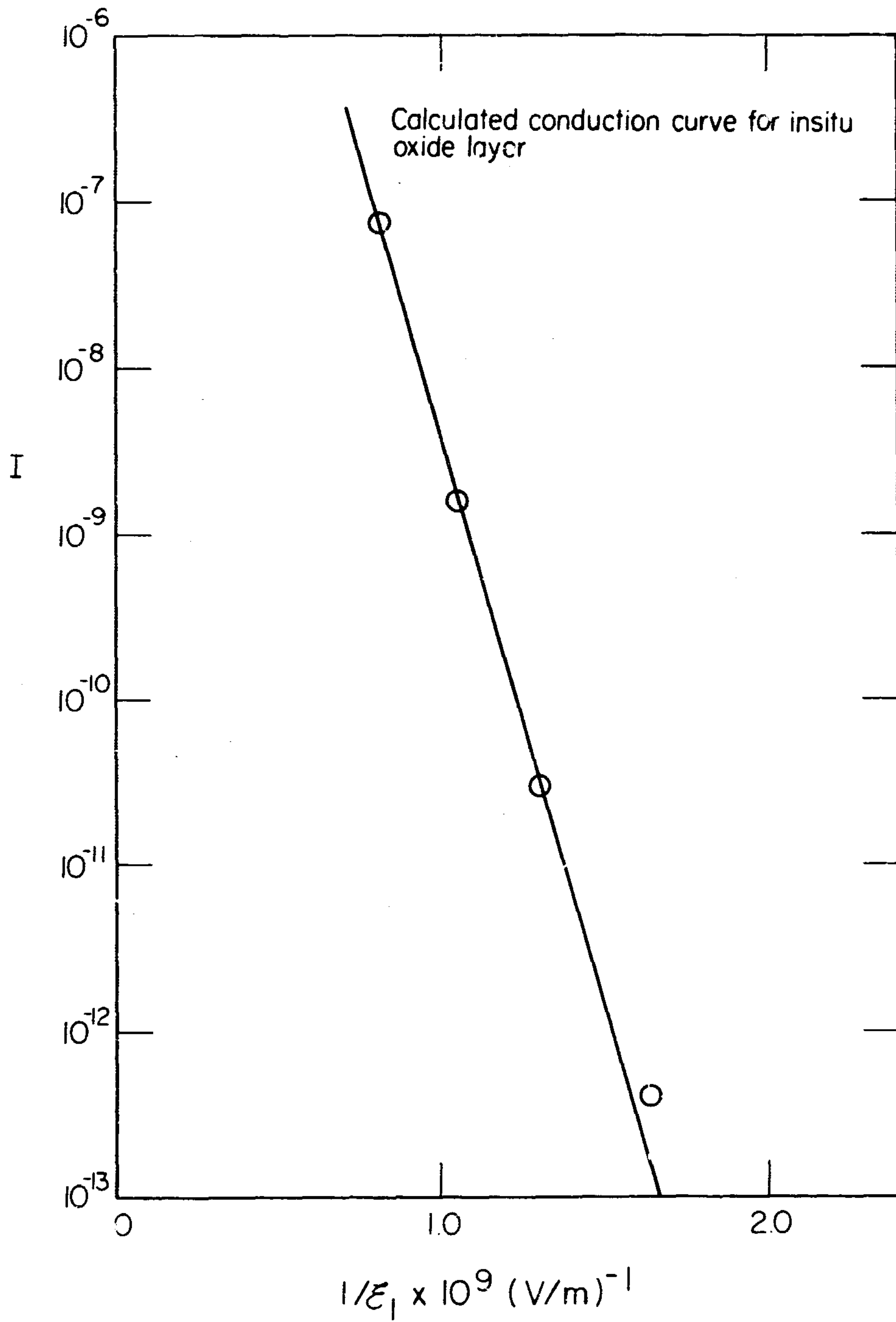

FIG. 6 Current vs reciprocal field for the calculated oxide layer conduction mechanism in a memory device having an insitu oxide layer.

Charge is then stored at the interface between the two insulators.

Additional experiments are being planned to further substantiate these results. A more detailed analysis of data obtained via transient measurements is presently being pursued.

III. OPTICAL EFFECTS ON THE CHARGE STORAGE CHARACTERISTICS OF THE MEMORY CAPACITOR

A. Preliminary Remarks

It had been noticed during the wafer probing of memory capacitors that a significant enhancement in charge storage occurred when the light from a microscope lamp was directed onto the surface of the wafer concurrently with the application of a negative charging pulse on the gate electrode. There was no enhancement when a positive charging pulse was applied. This effect was later observed on all memory structures that were fabricated on n-type silicon wafers. An initial correlation between this effect and the light modulation of the semiconductor space charge was postulated.

B. Analysis of Memory Device with Negative Gate Voltage

The current vs negative gate voltage characteristic of a memory capacitor was recorded both with light and without light directed on the surface of the device. This is reproduced in Fig. 7. With light on the device, the generation of electron-hole pairs in the silicon is great enough to cause a collapse of the space charge layer adjacent to the insulator. This space charge layer results from the depletion of electrons from the surface of the silicon when a negative voltage is applied to the gate electrode. This depletion continues as the bias voltage becomes more negative because the rate of charge flow through the silicon nitride exceeds the generation-recombination (g.r.) rate of carriers in the silicon space charge region. In

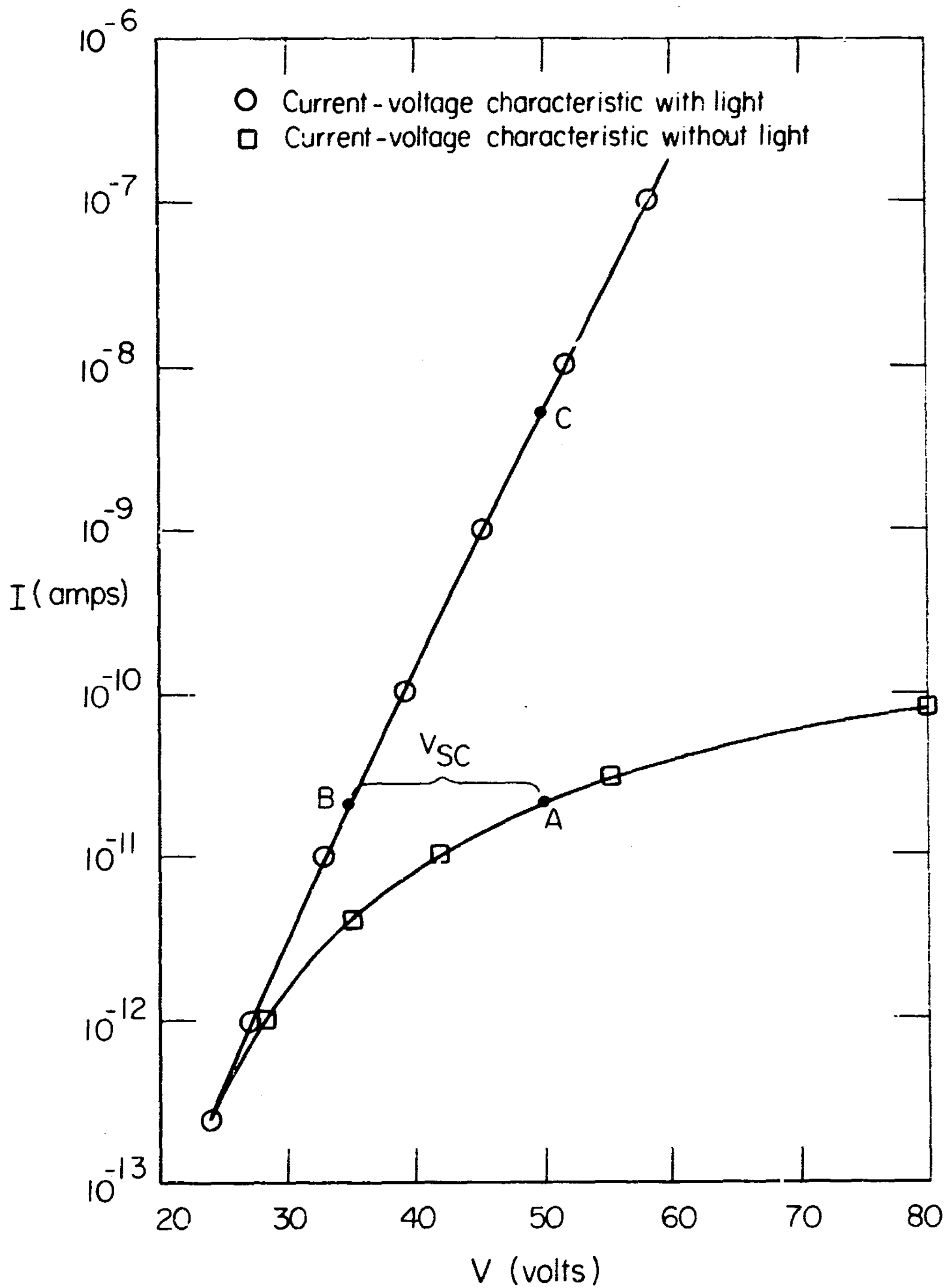

FIG. 7 Current vs negative gate voltage characteristics of a memory capacitor with and without the presence of light.

order to have an increased current, the number of g.r. centers must increase. This is achieved by the extension of the space charge region deeper into the silicon. The net result is a large increase in the voltage dropped across the silicon.

Consider the points A and B shown on the curves in Fig. 5. Point A is on the curve taken in the absence of light, while Point B is on the curve taken in the presence of light. When a negative 50 V is applied to the gate electrode in the absence of light, the actual drop across the insulator is 35 V and the drop across the space charge layer is 15 V. If this bias is applied to the sample in the presence of light then the current and voltage corresponding to Point C would be achieved. In this case approximately the full 50 V would be across the insulator. Therefore, a greater charge transfer would occur when the device is pulsed in the presence of light than in the absence of light. This has been confirmed quantitatively. For a dc setting voltage of -50 V the charge stored in the insulator of a capacitor without light (Point A in Fig. 7) was equal to that stored in the insulator of the same device when -35 V was applied with light (Point B in Fig. 7). A detailed analysis of the silicon surface space charge will be performed in order to develop a predictable current-voltage characteristic.

With modifications in the silicon nitride conductivity and the insulator structure this effect can be optimized to form the basic principle of an image storage device. This investigation will be continued and innovating features will be reported in future correspondence.

IV. FUTURE WORK

Although a model has been proposed and investigated for the transfer of electrons from the silicon into the insulator, a model for the reverse

process still remains to be established. The tunnel barrier will consist of the trap energy in the silicon nitride for the case of an oxide free interface and the trap energy plus the oxide-nitride energy barrier for the case of a device possessing an in situ oxide layer. The spatial distribution of these charges has been partially explored, but their redistribution with time still awaits investigation.

Injection effects occurring at the metal-insulator interface will also be investigated. The approaches to be used will incorporate variations in electrode materials (hence work functions) and methods by which "ohmic" contacts can be formed.

The silicon nitride growth parameters will be varied and the resulting layers investigated to determine any changes in the electronic microstructure. Such changes as electronic trap energies, trap density and possibly macroscopic conduction mechanisms will be of particular interest.

The light sensor effect described in this report will be explored further as to its utility and possible optimization. The thermal effects on charge storage will also be investigated.