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INVESTIGATION OF NEW CONCEPTS OF ADAPTIVE DEVICES

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I. INTRODUCTION

This report deals with a new type of device that has both adaptive and memory characteristics. It has the structure of a typical silicon planar p-channel enhancement insulated-gate field-effect transistor (IGFET). The mode of its operation is illustrated in Fig. 1, which shows the memory cell as an inverter and its output current as a function of applied gate voltage. Information is stored by setting the threshold voltage (V_T) of the IGFET to a high (V_{TH}) or a low (V_{TL}) value. Interrogation is accomplished by applying a gate voltage intermediate to the threshold voltage extremes. A current I_D will flow between source and drain if the recorded threshold voltage is less negative than the interrogating gate voltage (V_I); none will flow if the recorded threshold voltage is more negative. A high (negative) threshold voltage is written by applying a pulse of -50 V for a duration of 1 msec or less between gate and substrate. A low threshold voltage is similarly obtained with a positive 50 V pulse. The persistence of stored information has been demonstrated for periods of at least several months.

The operational feature that makes this IGFET an adaptive device is the possibility of making the threshold voltage larger or smaller in a reproducible manner. Once the threshold voltage has been set to a predetermined value, it operates very much like a fixed-threshold IGFET.

Thus, all the relationships of device parameters (e.g., transconductance, etc.) to device geometry are valid. As indicated in Fig. 1, the read-out step is a normal operation of an IGFET. Read-out speed is

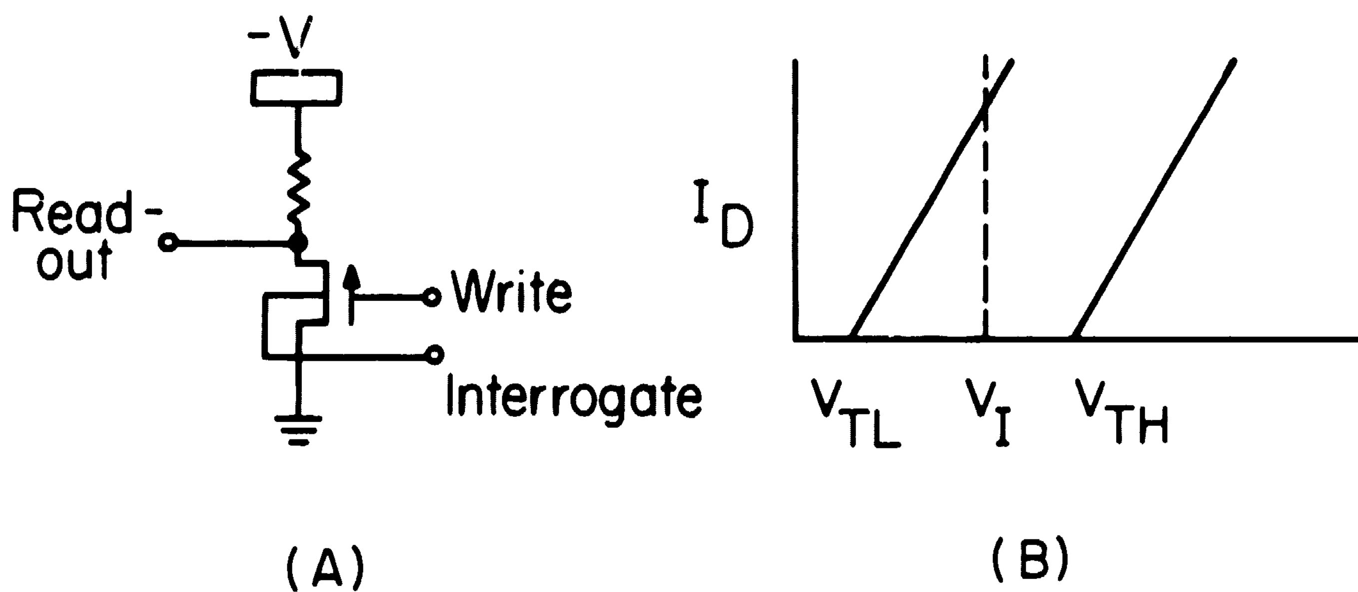


FIG. 1 (a) Memory cell used in inverter configuration.
(b) Idealized drain current vs. gate voltage characteristics of memory cell for low threshold voltage V_{TL} and high threshold voltage V_{TH}. V_I is the interrogation voltage applied to the gate to determine the state of the memory cell.

therefore determined by the f_T of the device and the interrogation circuit configuration. Given the limits of device geometry, which are determined by manufacturing technology, the read-out speed depends on the circuitry employed. The property of the device that is entirely new is its information storage capability. The phenomena relating to this property are the area of investigation covered by the reported work.

The switching characteristic, which is meant to be the relationship of the induced threshold voltage changes with the sign and amplitude of the applied voltage, is summarized in a short section. Work done since the beginning of this contract has not indicated any changes in the general character of these initial results. However, the data on temperature dependence of the switching characteristic are new.

Much work has been done on the measurement of write-in time. Methods of recording the current transient giving rise to the writing-in phenomenon have been established. Transient times ranging from 10 msec to 1 μsec were recorded, depending both on device structure and circuit parameters.

Initial data on the persistence of the information indicated a storage time of the order of 10 to 10^2 days. Now the change of the stored voltage with time and temperature has been studied in more detail. The results indicate a storage time of the order of a few months at room temperature, and of about a month at a temperature of 175°C.

More insight in the device physics was obtained from step-etch experiments which located the stored charges within 100 Å of the device interface. The mechanism of rapid charge transfer undoubtedly involves tunneling, as has been indicated by another set of experiments. Finally, it was determined that both the nature of the nitride composition and the oxide layer thickness affected the device characteristics.

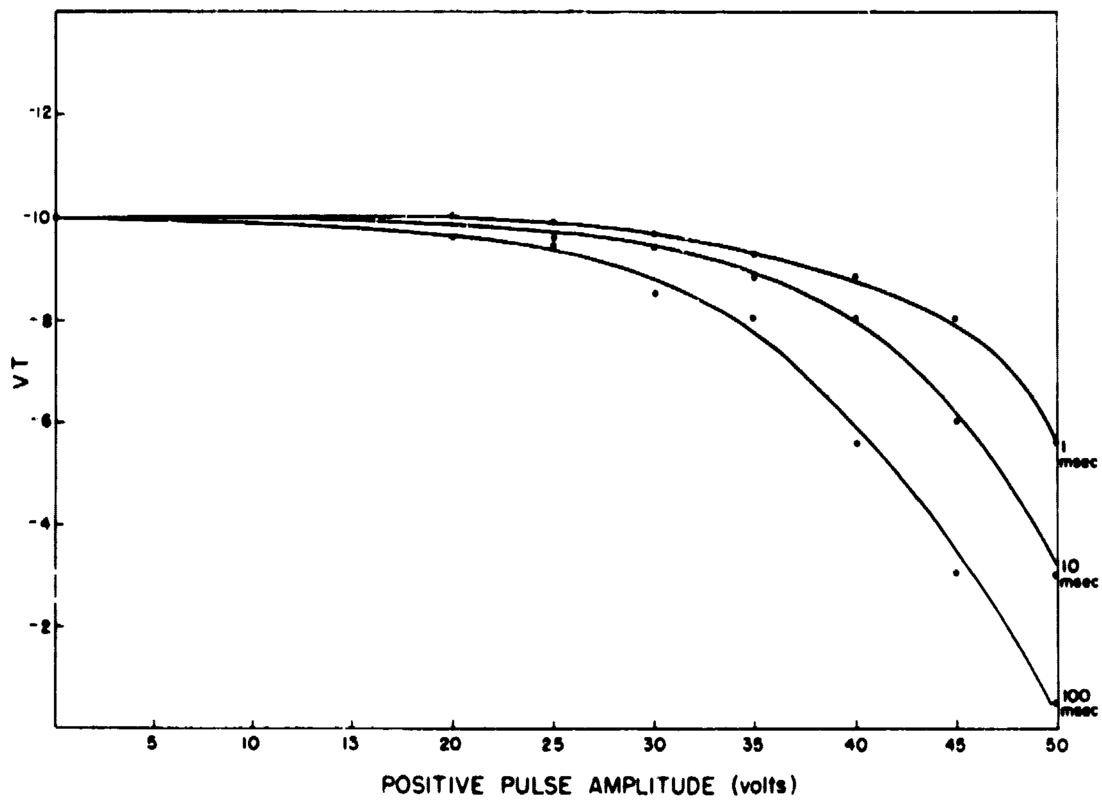
The greatest advance has been made in the theoretical understanding of the device. This is based on the existence of two coplanar regions having mutually independent conductance laws. With the help of Poisson's equation and the condition of current continuity, all device characteristics can be derived. Since the stored quantity consists of charges in the dielectric of the gate of the IGFET, the switching characteristic deals with the amount of charge stored. The study of write-in time is concerned with a determination of the rate of charge transfer. The persistence of information really depends on how long the charges are stored. The theoretical work ties all of these threads together in a model of the movement of charges in a solid state device as a function of applied voltage and the physical and geometrical parameters of the device. The model agrees with the experimental data in a qualitative way and awaits detailed measurements for complete confirmation. The work during the next period will be concentrated on the design and performance of experiments that permit an evaluation of the proposed theory.

II. EXPERIMENTAL RESULTS

A. Switching Characteristics

The threshold voltage of the memory device is changed by the application of a voltage pulse between its gate and substrate. The relationship between the amplitude of the applied voltage pulse, the width of the pulse, and the threshold voltage induced by that pulse is indicated in Figs. 2(a) and (b).

The curves in Fig. 2(a) were obtained by setting the device to a low threshold voltage by a positive pulse of 50 V. This was followed by a



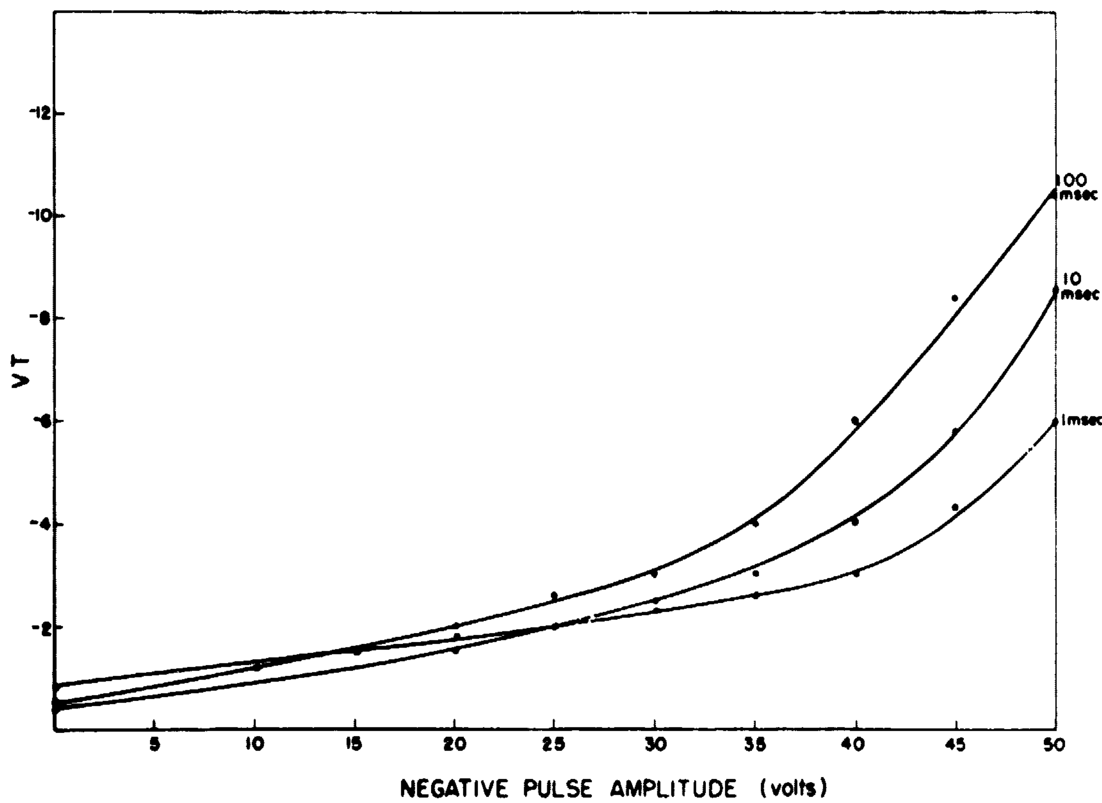


FIG. 2 (a) Threshold voltage V_T of MNS-VTT as a function of positive pulse amplitude and length.
(b) Threshold voltage V_T of MNS-VTT as a function of negative pulse amplitude and length.

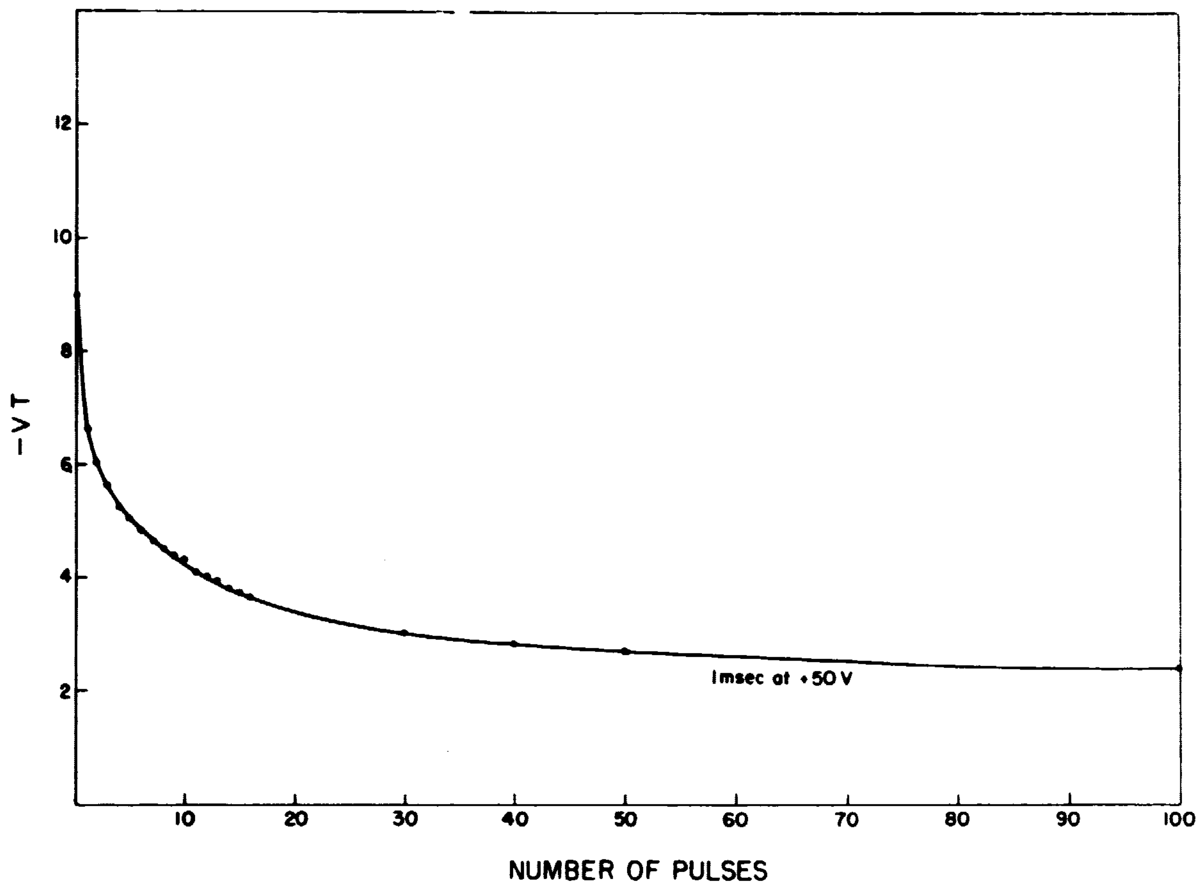


FIG. 3 Threshold voltage V_T of MNS-VTT as a function of the number of positive pulses of +50 V amplitude and 1 msec length.

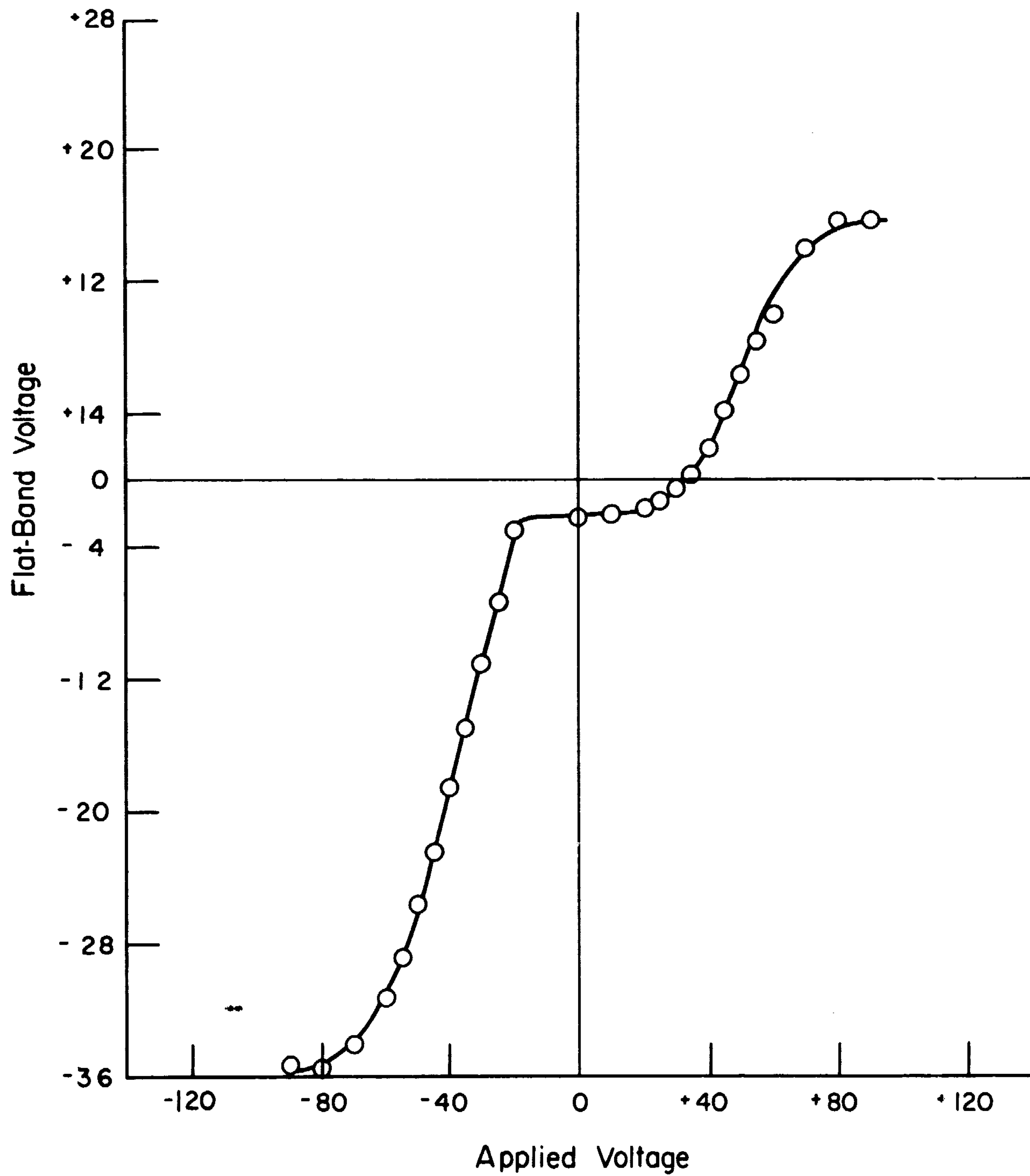


FIG. 4 Saturated values of flatband voltage as a function of applied voltage.

negative pulse of desired amplitude and width. The threshold voltage obtained from this negative pulse was recorded. Then a 50 V positive pulse was again applied to the gate, followed again by a negative pulse of another width or amplitude. In this way, all the points in Fig. 2(a) were obtained. Those in Fig. 2(b) were derived in an analogous manner, except that the signs of the alternating pulses were reversed.

It is clear that the amount of shift depends both on the amplitude and the width of the pulse. There is, however, a saturation pulse width beyond which no further increase in threshold voltage occurs for a given pulse amplitude. This saturation effect is typified by Fig. 3. A plot of the saturation voltage vs both positive and negative applied voltage is shown in Fig. 4. The curve was obtained by applying a dc voltage across the device, for as long as ten minutes, so that saturation was achieved. The most noteworthy feature of this curve is the fact that there is a minimum absolute voltage below which no shift in threshold voltage occurs in either direction. As long as this minimum voltage is larger than the interrogation voltage used to determine the content of the storage element, the process of interrogation will not change the information stored in the transistor. This is a necessary requirement for a nondestructive read-out (NDRO) device.

An interesting temperature dependence of the amount of threshold voltage shift was found. First, between 25°C and 100°C no temperature dependence was observed at all. Above this temperature, low pulse amplitudes (50-70 V) resulted in an increase in the amount of shift with increasing temperatures. For pulse amplitudes between 70 and 80 V, little change with increasing temperature occurred. For pulse amplitudes above 80 V, the threshold voltage change actually decreased with temperature, increasing above 100°C.

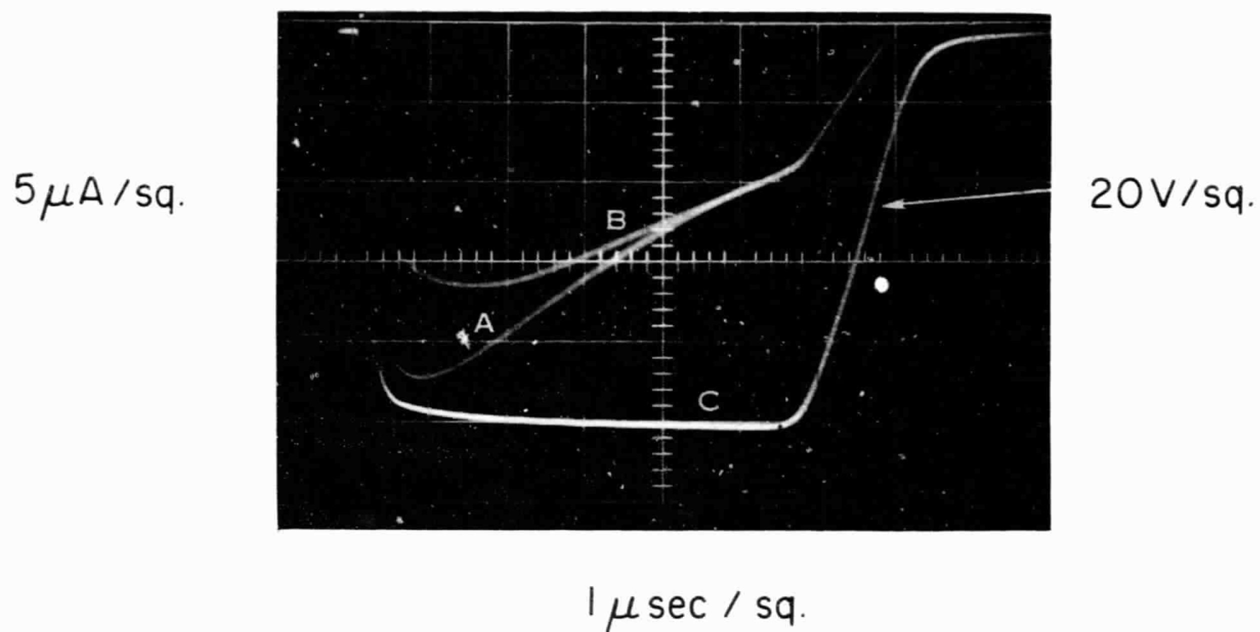


FIG. 5 An oscilloscope trace of: (a) the current pulse which represents the charge going into storage plus the displacement current, (b) the current pulse described the displacement current alone, and (c) the incoming voltage pulse.

All ΔV_T vs ^oC curves appear to approach a common value near 300^oC. The explanation of this behavior requires the assumption of a charge transfer mechanism that is dependent on temperature.

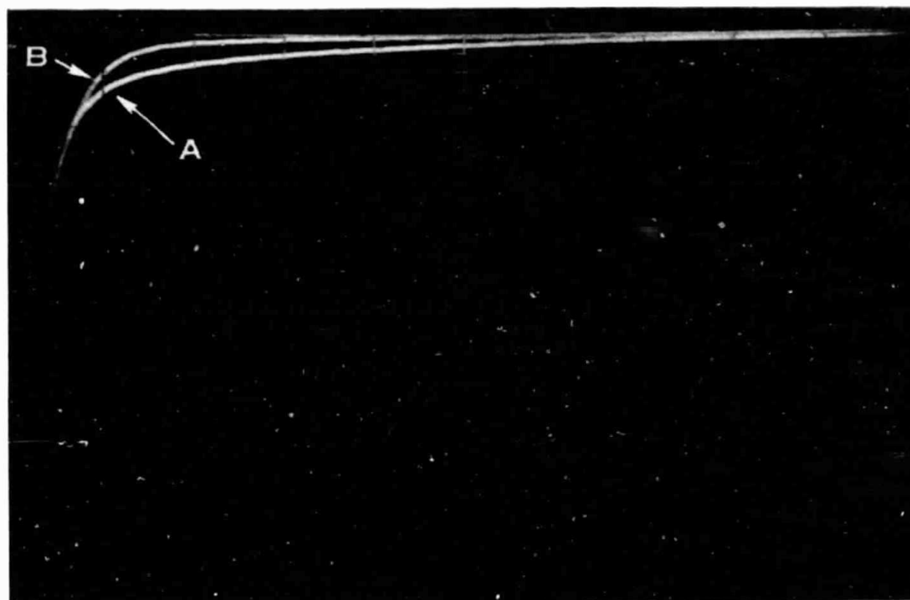
B. Write-in Time

Simple electrostatics require that the change in threshold voltage induced in the transistor must have resulted from the injection of charges into the dielectric. An increase in the (negative) threshold voltage must be due to a buildup of positive charges, and a decrease in the (negative) threshold voltage must be due to a loss of positive charges. These charges then must be transported by a transient current that goes to zero as the induced threshold voltage reaches its saturation value.

Our initial attempts to record this current on transistors met with difficulty, since the currents were too small to give sufficiently accurate results. However, capacitor structures similarly fabricated, with areas fifteen times larger than the transistor gates, permitted definitive values to be recorded. An example is given in Fig. 5. In this oscilloscope trace, the horizontal scale is in units of 1 μsec per division. The large trapezoid is the trace of the applied voltage pulse. Its amplitude is -100 V to produce a readily measurable current.

The two other traces are transient currents, at a scale of 50 μA per division. They were recorded across a resistor in series with the device. The larger amplitude transient resulted when the device was pulsed once after it had been set to a low threshold voltage. The smaller transient resulted when the device was pulsed a second time with the same voltage value as the first pulse. Further pulsing resulted in repeated tracings of the lower amplitude transients. The first and larger current transient arises from

5μ A/sq.



50 μsec/sq.

FIG. 6 The difference between trace A and trace B is the amplitude of the conduction current into the dielectric.

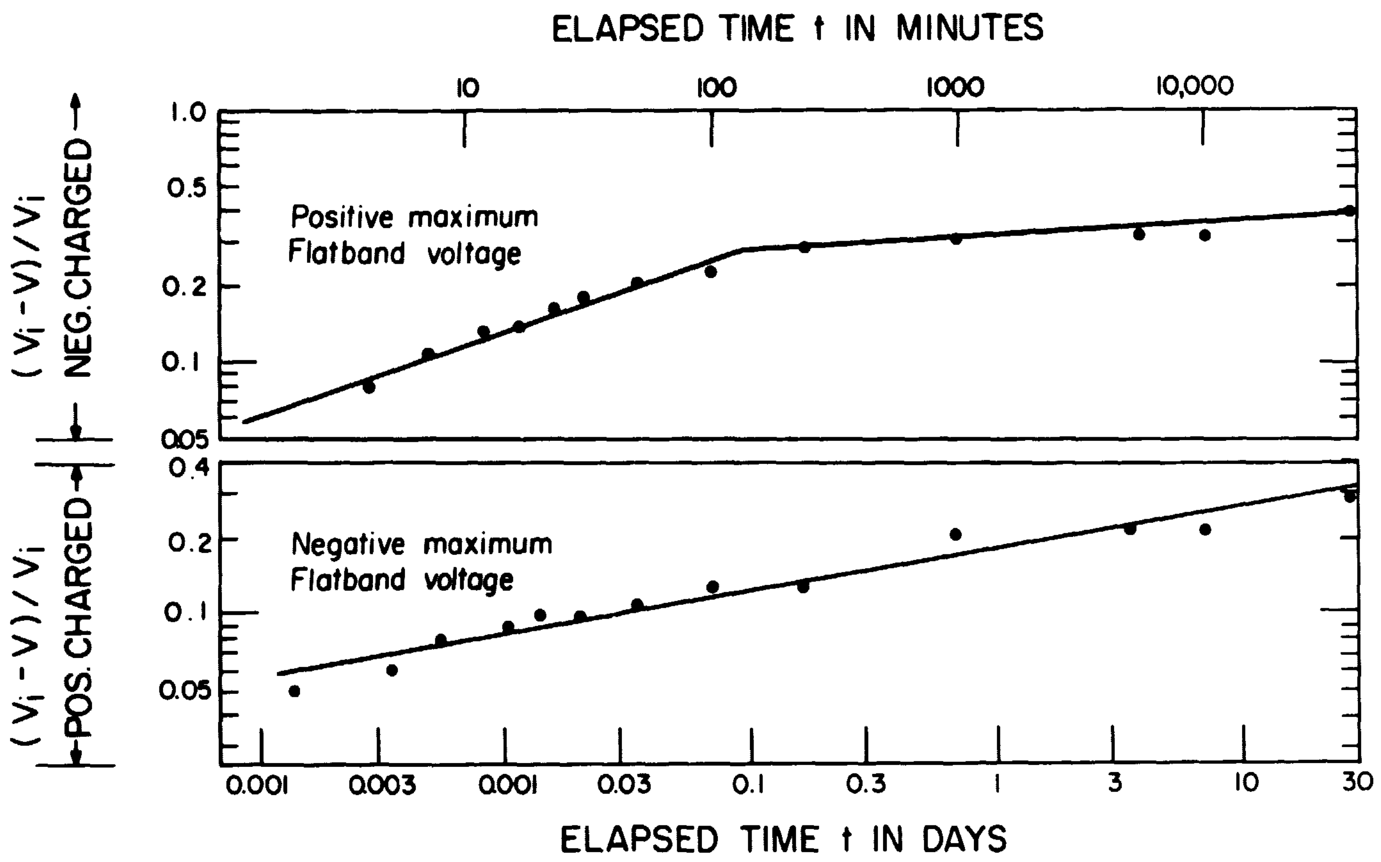


FIG. 7 Typical storage-life test results for a positively shifted capacitor and a negatively shifted capacitor.

the sum of the currents that transport the charges into the dielectric, and the displacement current charging up the device capacitance. The second current transient is due to the displacement current alone.

It is clear from the trace that, for this structure, all charge storage occurred during the time interval when the displacement current was quite large. For the results shown in Fig. 5, the saturation write-in time was about 7 μsec. Since the displacement current is determined only by the capacitance of the structure and its series resistance, the write-in time of a configuration should really depend only on the series resistance in the writing circuit. In a further experiment the values of such resistors were changed from 1MΩ to 100 kΩ, and then to 10 kΩ resistors, and the predicted dependence on the RC constant was confirmed. With some nitride structures, write-in times of the order of 1 μsec were observed. Other structures, made by a different fabrication process, showed very much longer write-in times. A typical example is given in Fig. 6. Here the difference between the first and the second pulse is very small, indicating a small current carrying charge into the dielectric. Very fast and very slow write-in's are discussed in more detail in section III.

C. Persistence of Stored Information

The storage life of the information is a parameter of considerable importance, since it determines the types of application which are possible. Initial tests on transistors were carried out over periods of the order of 200 hours. The transistors were shifted to high and low threshold voltages and then stored at room temperature and at 125°C, both with zero bias and -5 V bias during storage. All transistors exhibited a small change in threshold voltage, ranging between 0.1 and 1 V, over the first two hours. For the remainder of the test period the changes were essentially negligible. Another

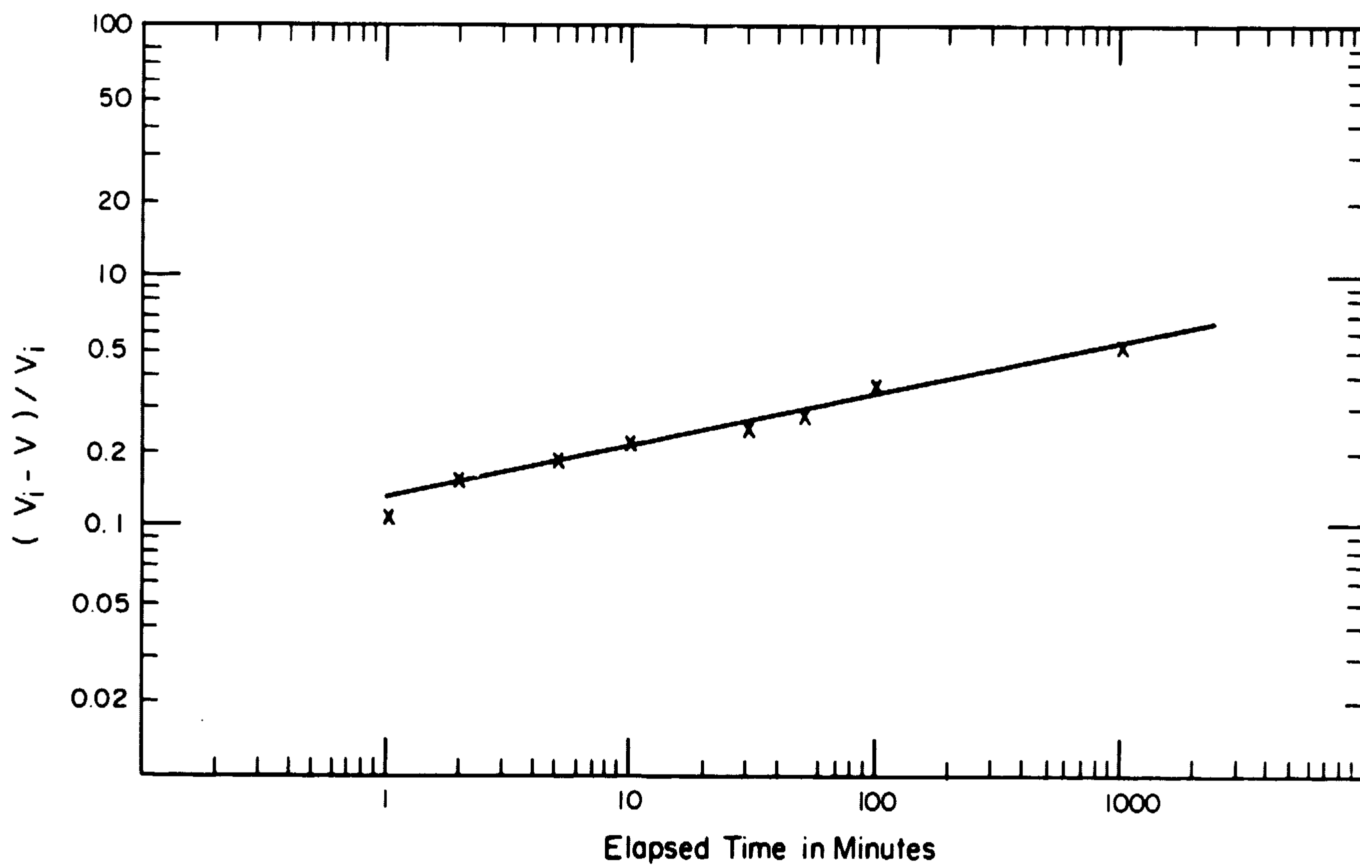


FIG. 8 Decay of stored charge at 150°C; V_i = - 16 V.

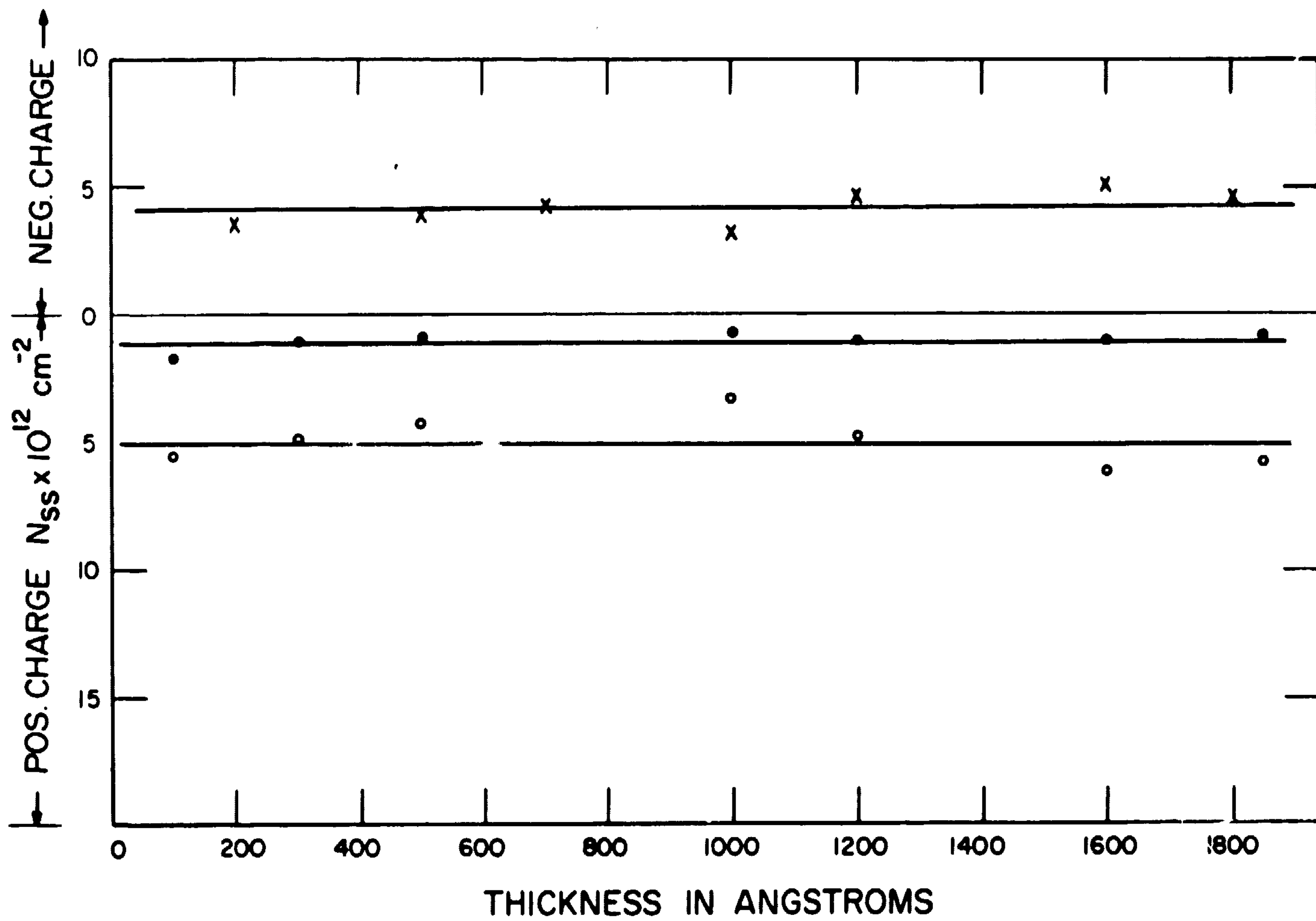


FIG. 9 The step-etch results for the capacitors: (1) subjected to positive pulses prior to test, (2) not subjected to pulses, and (3) subjected to negative pulses.

early test involving four transistors under constant interrogation indicated no important change in the stored information after a period of three months.

Since these early measurements, charge decay has been studied in more detail. An example of a typical experiment is given in Fig. 7. The study was carried out with two identical capacitors that had been shifted to +21 V and -43 V flatband voltages by the application of 140 V, 1 msec pulses with the correct polarity. Their original threshold voltage was -10 V. These capacitors were observed over a period of a month. The curves in Fig. 7 exhibit an initial rapid decay that progressively slows down. At present the decay law is not known,but it is convenient to use a log-log display of the data. Extrapolating from these data indicates that it would take about a year for one-half of either a positive or a negative charge to decay. This is probably a low estimate, since the decay is undoubtedly field dependent. At the lower charge densities, corresponding to lower threshold voltages, the fields due to the charges will be lower and decay should proceed at a slower rate.

The effect of temperature is indicated in Fig. 8. It indicates that at sufficiently elevated temperatures there is an increase in the decay rate of capacitors similar to those used in Fig. 7. If a relationship between time constants of charge decay is assumed to have the form $\tau = \tau_0 \exp(e\varphi_t/kT)$, then Figs. 7 and 8 permit a calculation of the trap depth φ_t. The value found is 0.25 eV.

D. Experiments of a Basic Nature

It is clear that it is charges stored in the dielectric which are giving rise to changes in threshold voltage in the memory device. The exact location of these charges is of some importance to both understanding

the device and in controlling its fabrication. In order to determine this parameter, MIS structures were made and shifted to high negative and positive flatband voltages. The metal plates were then removed and the insulator was removed in small increments by etching. After each removal the flatband voltage of the structure was measured with a mercury probe. In this way, a relationship between flatband voltage and insulator structure was established. From both sets of values, the surface charge density in the dielectric was calculated and plotted as a function of insulator thickness. The data in Fig. 9 indicate that down to about 100 Å, the smallest thickness that could be estimated, there was no discernible change in surface charge density. The charges were therefore located within 100 Å of the insulator-silicon interface.

In order to gather information on the mechanism of charge transfer, the transient current produced during the pulse that changed the flatband voltage of a capacitor was recorded as a function of temperature of that capacitor. Table 1 shows the results, which indicate that the charge transfer mechanism is independent of temperature at least between $25^{o}C$ and $100^{o}C$. This suggests a mechanism involving either tunneling of conduction electrons through a barrier or tunneling of electrons from isolated states into a conduction band. It is necessary to assume that electrons are doing the tunneling from the dielectric into the silicon. The transfer of holes from silicon into the dielectric appears unimportant, since during the charge transfer the hole concentration at the dielectric-silicon interface is still of the order of that of the minority carriers, namely $\sim 10^{20}/10^{15}$ or 10^{5} holes/cm^3. The temperature independence of the current pulse is further evidence that the positive charges in the dielectric were formed by electrons leaving neutral states. The density of neutral states in the dielectric is clearly

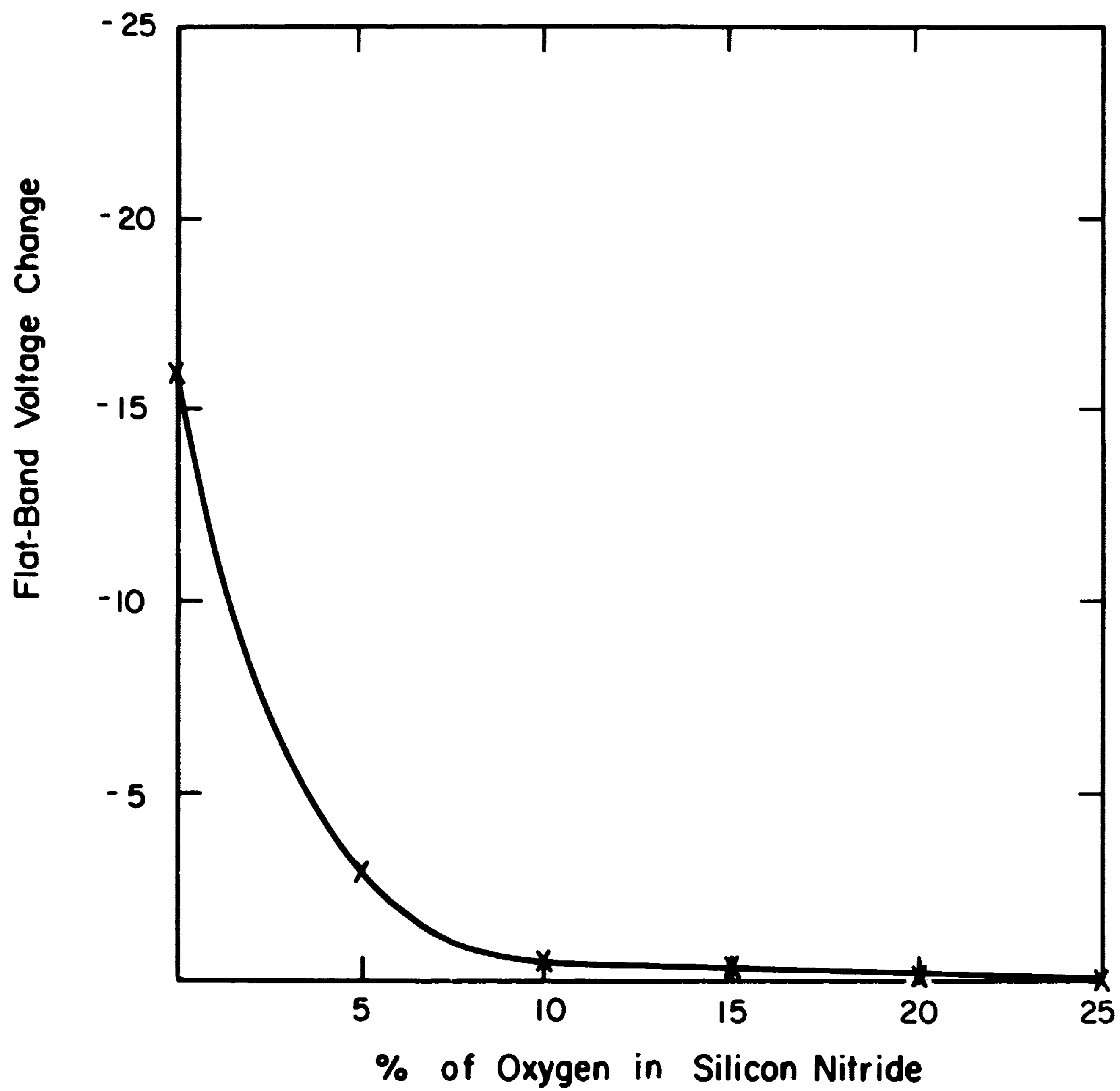


FIG. 10 Shift in flatband voltage for capacitor structure of 100 Å silicon oxide and 1000 Å silicon nitride, as a function of oxygen concentration in silicon nitride. Voltage pulse: - 100 V, 1 msec.

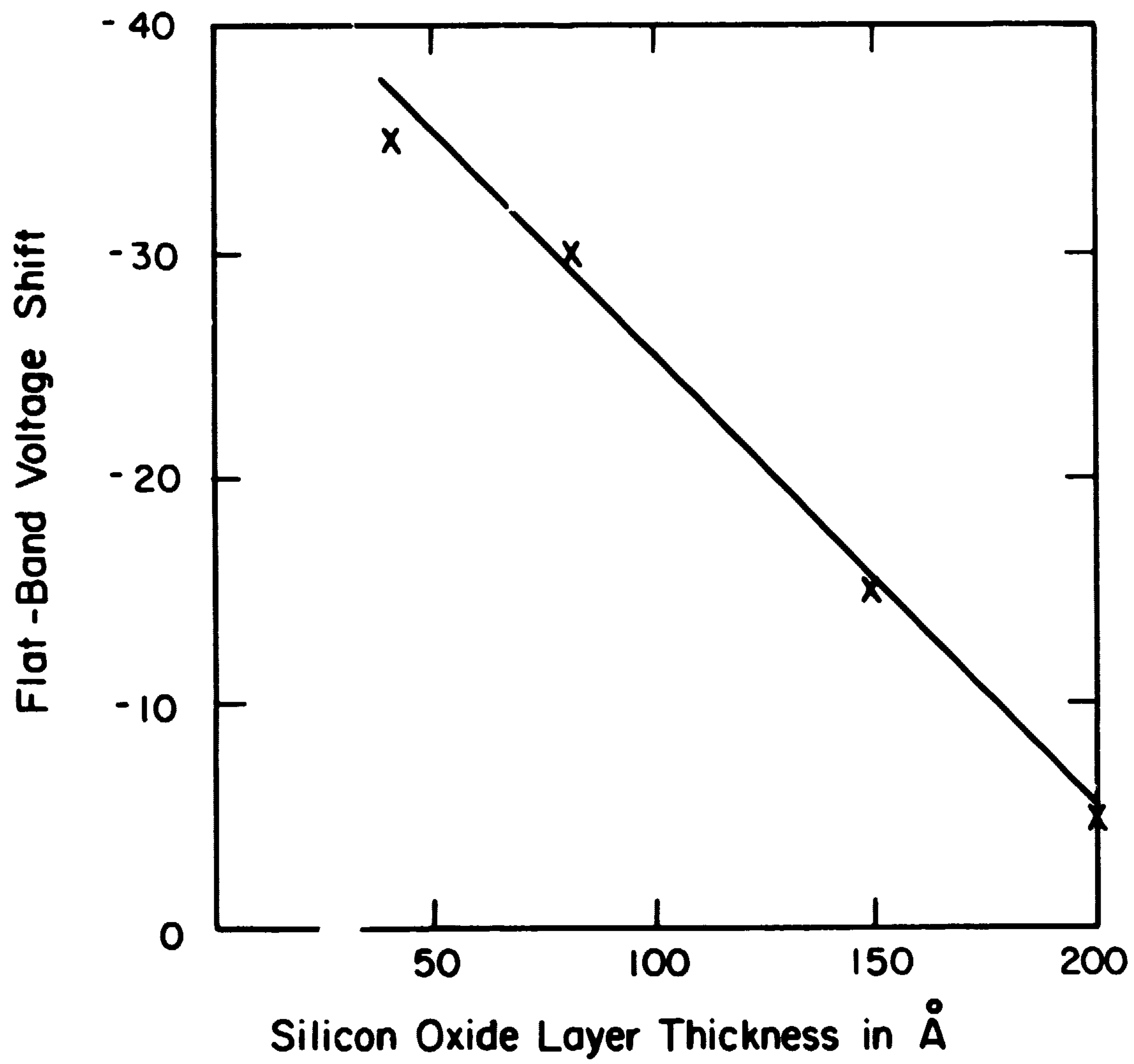


FIG. 11 Effect of silicon oxide layer thickness on flatband voltage shift in capacitors having 1000 Å of oxygen-free silicon nitride over the oxide layer. Voltage pulse: - 100 V, 1 msec.

independent of temperature. In contrast, the density of holes in silicon at 300^0C would be much higher than that at 25^0C. If the positive charges in the dielectric had been the result of the trapping of holes injected from the silicon, the maximum amplitude of the transient current would have been larger at 300^0C than at 25^0C. As described in part A of this section, the magnitude of the change of the threshold voltage was temperature dependent. Therefore, there must be several processes at work simultaneously, with only one of them temperature independent. This will be clarified in section III.

TABLE 1

Effect of Temperature on Duration and Peak Current of Charging Transient

Temperature	Transient Time	Peak Current
25^0C	1.2 μsec	2.0 mA
100^0C	1.3 μsec	1.9 mA
150^0C	1.2 μsec	1.8 mA
200^0C	1.2 μsec	2.0 mA
300^0C	1.4 μsec	1.6 mA

Finally, the effect of the macroscopic structure of the dielectric was investigated in two series of experiments. In the first, a number of capacitors were formed having a silicon-oxide layer of constant thickness and a 1000 Å thickness of nitride. The concentration of oxygen in the nitride was varied from 0 to about 30 %. Figure 10 shows a plot of the flatband voltage change for a constant pulse amplitude and width as a function of the oxygen concentration of the silicon nitride. It is clear that the amount of shift is critically dependent on the oxygen concentration.

In the second series of experiments, capacitors which had a varying thickness of the oxide layer, but a constant thickness and composition of the nitride, were studied. Again, a clear-cut correlation with flatband voltage

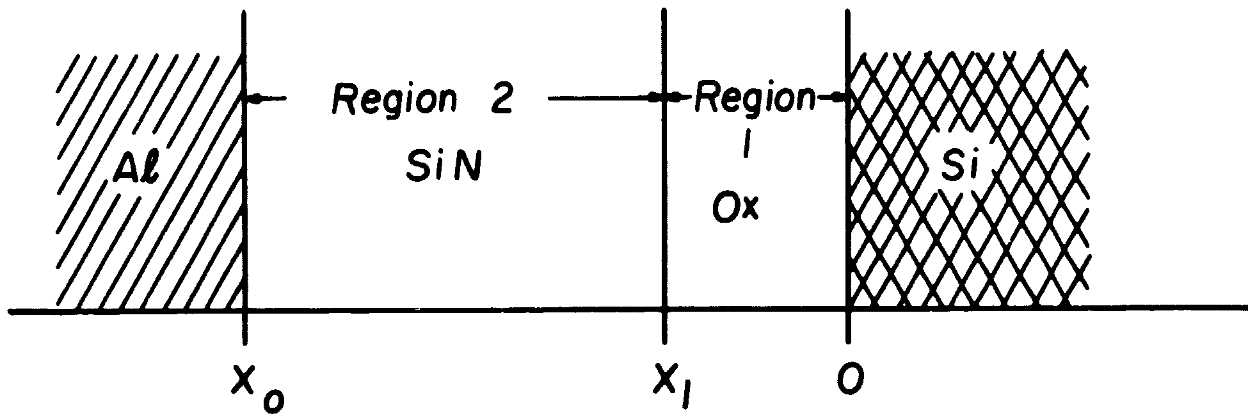


FIG. 12 Structure of memory capacitor.

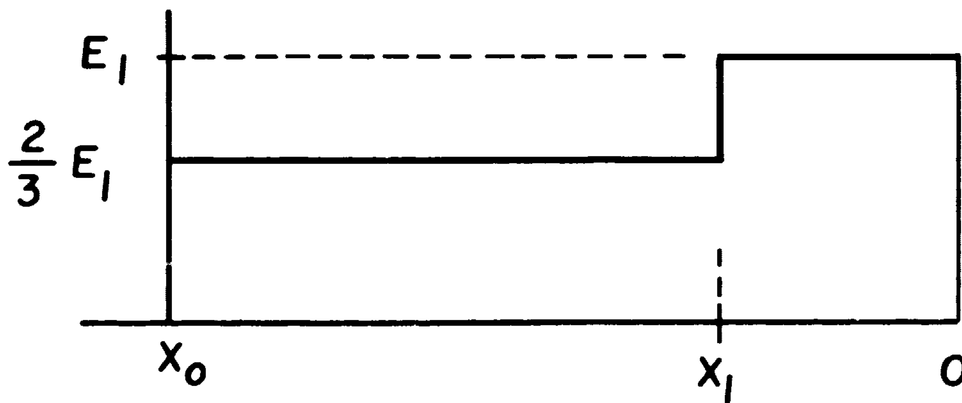


FIG. 13 Initial field distribution in memory capacitor.

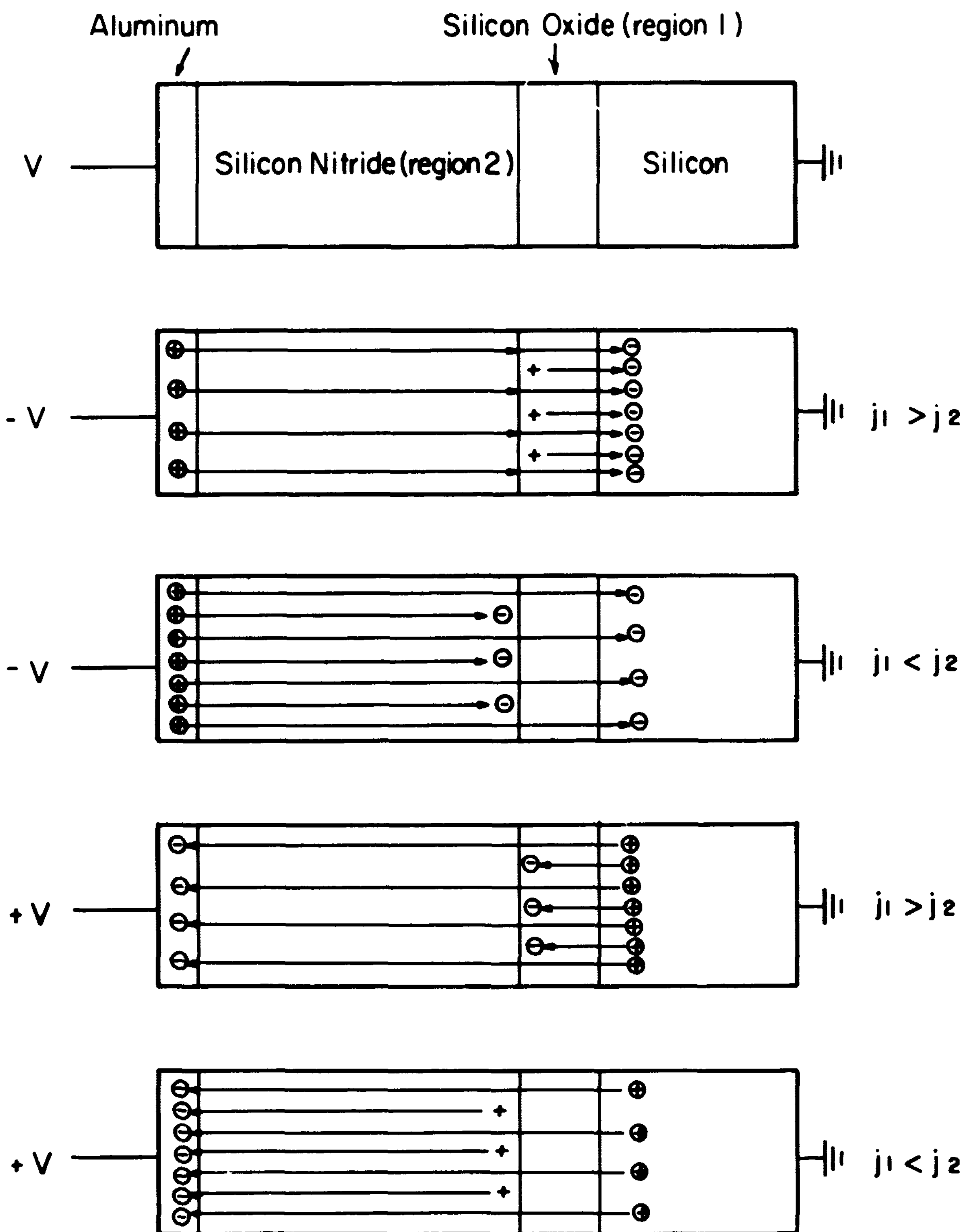


FIG. 14 Effect of the polarity of the applied voltage and the relative magnitude of j_1 with respect to j_2 on the polarity of the charge sheet built up at the insulator-insulator interface.

shift per applied pulse can be seen, as displayed in Fig. 11. Evidently the amount of shift is inversely related to the thickness of the oxide.

III. THEORY OF MEMORY DEVICE

A. Basic Mechanism

The basic structure in which all action takes place is that of an MIS capacitor. At present, its top electrode is a metal plate and its bottom electrode is n-type silicon. Its most important feature is the fact that the insulator consists of two layers with different conductance properties.

Keeping close to the structure of the present memory element, the thinner region at the silicon interface (region 1) is designated silicon oxide, and the thicker region at the aluminum interface (region 2) is designated silicon nitride. A one-dimensional sketch of this structure is given in Fig. 12. The current density in region 1, J_1, is controlled by the field across region 1, E_1, according to the conductance law $J_1 = f(E_1)$ appropriate for this insulator. The current density in region 2, J_2, is controlled by the field across region 2, namely E_2, according to the conductance law $J_2 = f(E_2)$, appropriate for the insulator in region 2.

When a voltage V_{appl} is applied across the plates of this MI_2I_1S structure, the displacement vectors D_2 (across region 2) and D_1 (across region 1) are identical. The fields are then $\epsilon_2 E_2$ and $\epsilon_1 E_1$ in those regions, respectivly, where ϵ is the permittivity of each region. We assume for the present that there are no charges in either insulator region, so that the fields are constant in each.

Region 2 consists of silicon nitride, $\epsilon_2 = K_{SiN}\epsilon_0$, where $K_{SiN} = 6$; and region 1 consists of silicon oxide, $\epsilon_1 = K_{0x}\epsilon_0$, where $K_{0x} = 4$.

At the instant after application of the dc voltage step V_{appl},

$$D_1 = D_2 \text{ or } E_1\epsilon_1 = E_2\epsilon_2, \tag{A1}$$

and

$$E_2 = E_1\frac{\epsilon_1}{\epsilon_2} = E_1\frac{K_{Ox}}{K_{SiN}} = \frac{2}{3}E_1 \tag{A2}$$

We can therefore describe the initial field across the MI_2I_1S capacitor by Fig. 13. Immediately after this first instant, the fields in each region will start conductance; each independently in its region, according to the fixed $J_1 = f(E_1)$ and $J_2 = f(E_2)$ laws. It is clear that, given different conductance laws and fields, the charges in each region will be transported at different rates. We will assume that transport across the electrode-insulator interfaces does not affect the conductance laws (i.e. these electrodes act as ohmic contacts). Since the current densities effecting charge transport are different in each region, a charge pile-up will occur at the interface between region 1 and 2. The effects of the sign of the applied voltage, and the relative levels of the instantaneous currents in region 1, namely j_1, and in region 2, namely j_2, are sketched in Fig. 14.

Figure 14 (a) provides the labels for the different regions shown. Figure 14 (b) indicates the effect of a negative voltage on the metal plate for $j_1 > j_2$. Since more electrons leave region 1 than are entering it, a positive charge is left behind at the boundary between the insulators. Figure 14 (c) depicts the case for $j_1 < j_2$ at a negative applied voltage. Now fewer electrons are leaving region 2 than are entering it, so that a negative charge is left at the insulator-insulator boundary. Figure 14(d)

shows the condition for a positive applied voltage and $j_1 > j_2$. Fewer electrons are leaving region 1 than are entering it, again leaving a negative charge at the insulator-insulator boundary. Finally, in Fig. 14(e) the condition is given for a positive applied voltage and $j_1 < j_2$. Since more electrons are leaving region 2 than are entering it, a positive charge is left behind. Thus, depending on the individual conductance laws in each region, positive and negative applied voltages can result in both positive and negative charge accumulation at the insulator-insulator interface.

Whatever the sign of the charge accumulating at the interface, it will give rise to a field which opposes that in existence in the more highly conducting region. The field due to the accumulating charge will at the same time add to that in existence in the lowly conducting region. All charge accumulation will stop when the effective field across the high conductance region has been lowered to such an extent that its current density is equal to that passing through the low conductance region, whose field has been increased by accumulated charge. The end point of charge accumulation is therefore obtained when the conduction currents across both regions are equal. The same model is valid if we have the same insulator I throughout the dielectric instead of an insulator I_1 different from I_2. But then there must be a thin region 1 where conduction is controlled by a different mechanism, giving rise to a current law $J_1 = f(E_1)$ in a thin region of characteristic thickness x_1 having a field E_1 across it. Such a situation would exist when an interface or barrier controlled current (emission limited) crosses the silicon-insulator interface, while the conduction in the insulator is controlled by bulk limited mechanism $J_2 = f(E_2)$.

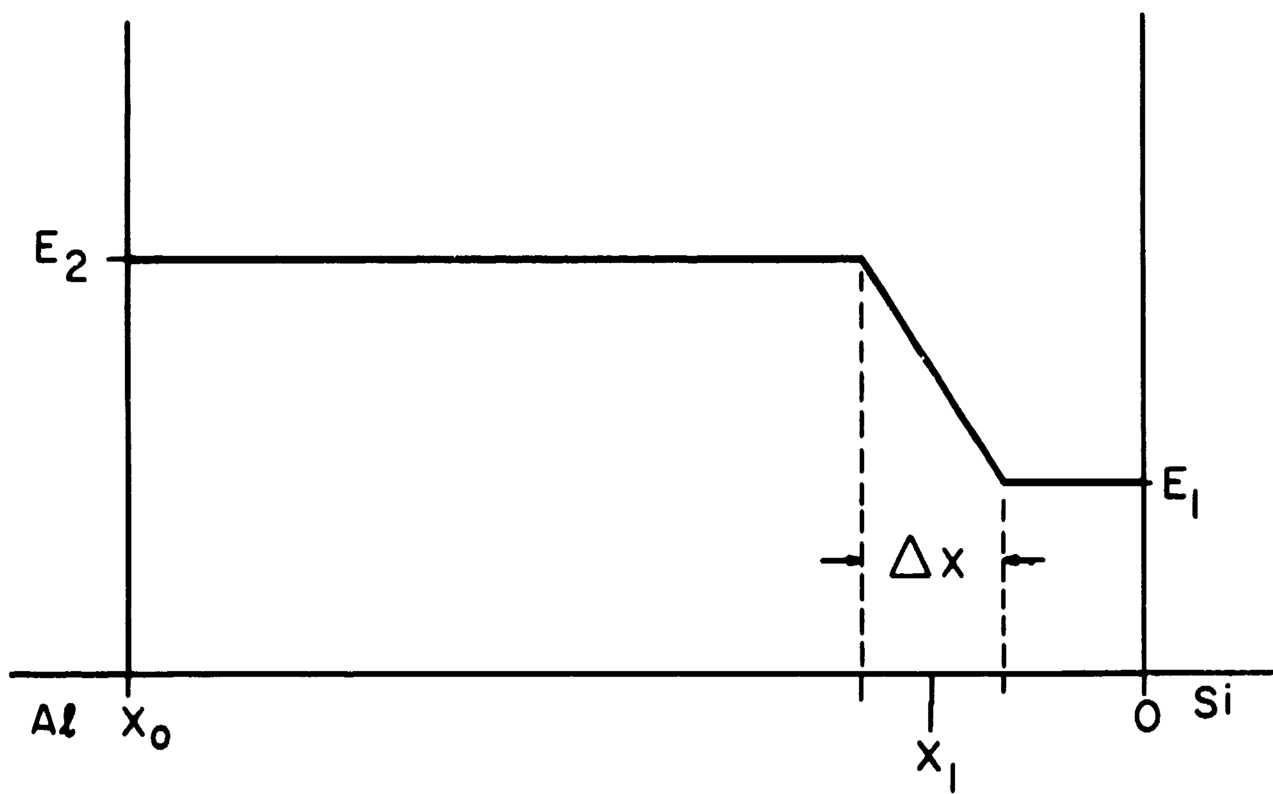


FIG. 15 Steady-state field distribution in memory capacitor.

B. Conductance Laws

Following C. A. Mead, Physical Review 128, 2088-2093 (1962), we can expect that the conduction current densities in the thick insulator formed by silicon nitride are bulk controlled. In that case, the current density j obtained for an applied field E may be the sum of three current contributions, i.e.,

$$j = j_{PF} + j_{IFE} + j_{H}. \tag{B1}$$

The quantity j_{PF} is the current arising from an internal Schottky emission (of trapped electrons into the conduction band) known as the Poole-Frenkel effect and is given by

$$j_{PF} = \sigma_{PF} E \exp\{ - e[\varphi_T - (eE/\pi\, \epsilon_0 \epsilon_d)^{1/2}]/kt\}, \tag{B2}$$

where e is the electronic charge, φ_T is the barrier height for the electron traps, e_0 is the permittivity of free space, e_d is the dynamic dielectric constant, k is the Boltzmann constant, and T is the absolute temperature. The constant σ_{PF} is a function of trap density.

The quantity j_{IFE} is the current arising from internal field emission of electrons from traps into the conduction band. It is essentially a tunneling effect described by the expression

$$j_{IFE} = SE^2 \exp(E_{IFE}/E), \tag{B3}$$

where S is a function of effective mass and trap density, and E_{IFE} is a function of effective mass and trap depth.

The current j_H arises from the hopping of thermally excited electrons between isolated states. It has an ohmic characteristic, but

is dependent on a thermal activation energy φ_H, i.e.

$$j_H = \sigma_H E \exp(- e\varphi_H/kT) \tag{B4}$$

The thin silicon oxide layer may have bulk conduction properties of the same nature as those described for silicon nitride. In addition, however, it is probable that tunneling through it occurs. Schottky emission at either of its interfaces is also a possibility. The exact mechanism therefore is hardly predictable and depends on its thickness and many factors arising from the details of its formation process.

C. Steady-State Characteristics

In this section we will examine the effect of an applied voltage on the charge accumulated after a steady-state condition has been reached, that is, when $j_1(E_{1f}) = j_2(E_{2f})$. In order to yield a maximum of insight for a minimum of manipulation, it is assumed that the accumulated charge is spread over an infinitesimal distance Δx, so that it may be treated as a delta function distribution. This assumption appears well justified in view of the fact that step-etch experiments have established that the stored charge must lie within about 100 Å of the silicon-insulator interface.

At steady state, the field distribution in the insulator is given in Fig. 15. This is expressed by Poisson's equation

$$\nabla \cdot D = \rho \tag{C1}$$

where the displacement vector $D = \epsilon E$, and ρ = volume charge density in coulombs per cubic centimeter. Integration with respect to x yields

$$D_2 = D_1 + \int^{\Delta x} \rho dx, \tag{C2a}$$

or

$$D_2 = D_1 + eN_I, \tag{C2b}$$

where N_I is the sheet charge density in cm^{-2}, and e is the electronic charge in coulombs (1.6×10^{-19} coulombs).

The division of the applied voltage V_{appl} across the insulator is given by

$$V_{appl} = E_1 x_1 + E_2 (x_0 - x_1). \tag{C3}$$

In this formulation, the voltage drop across the narrow region Δx is neglected. Substituting $\epsilon_1 E_1$ for D_1, and $\epsilon_2 E_2$ for D_2 in (C2b), and eliminating E_2 from (C3) with this form of (C2b) results in

$$V_{appl} = E_1 \left(\frac{\epsilon_1}{\epsilon_2}\right) \left[(x_0 - x_1) + \left(\frac{\epsilon_2}{\epsilon_1}\right) x_1\right] + \frac{eN_I}{\epsilon_2} (x_0 - x_1). \tag{C4}$$

The applied voltage that causes the field E_1 at the insulator-silicon interface to go to zero is called the flatband voltage V_{FB}, i.e., $V_{appl} = V_{FB}$ when $E_1 = 0$. This causes (C4) to become

$$V_{FB} = \frac{eN_I}{\epsilon_2} (x_0 - x_1). \tag{C5}$$

When steady state conditions have been reached, the field at the insulator-silicon interface has reached a final value E_{1f}, and the flatband voltage has reached a final value V_{FBf}. At steady state, then,

$$E_{1f} = (V_{appl} - V_{FBf}) \left(\frac{\epsilon_2}{\epsilon_1}\right) \Big/ \left[x_0 - x_1 + \left(\frac{\epsilon_2}{\epsilon_1}\right) x_1\right]. \tag{C6}$$

If we now eliminate E_1 from Eq. (C3), again using (C2b) expressed in terms of $\epsilon_1 E_1$ and $\epsilon_2 E_2$ and going through the same manipulations to arrive at E_{2f},

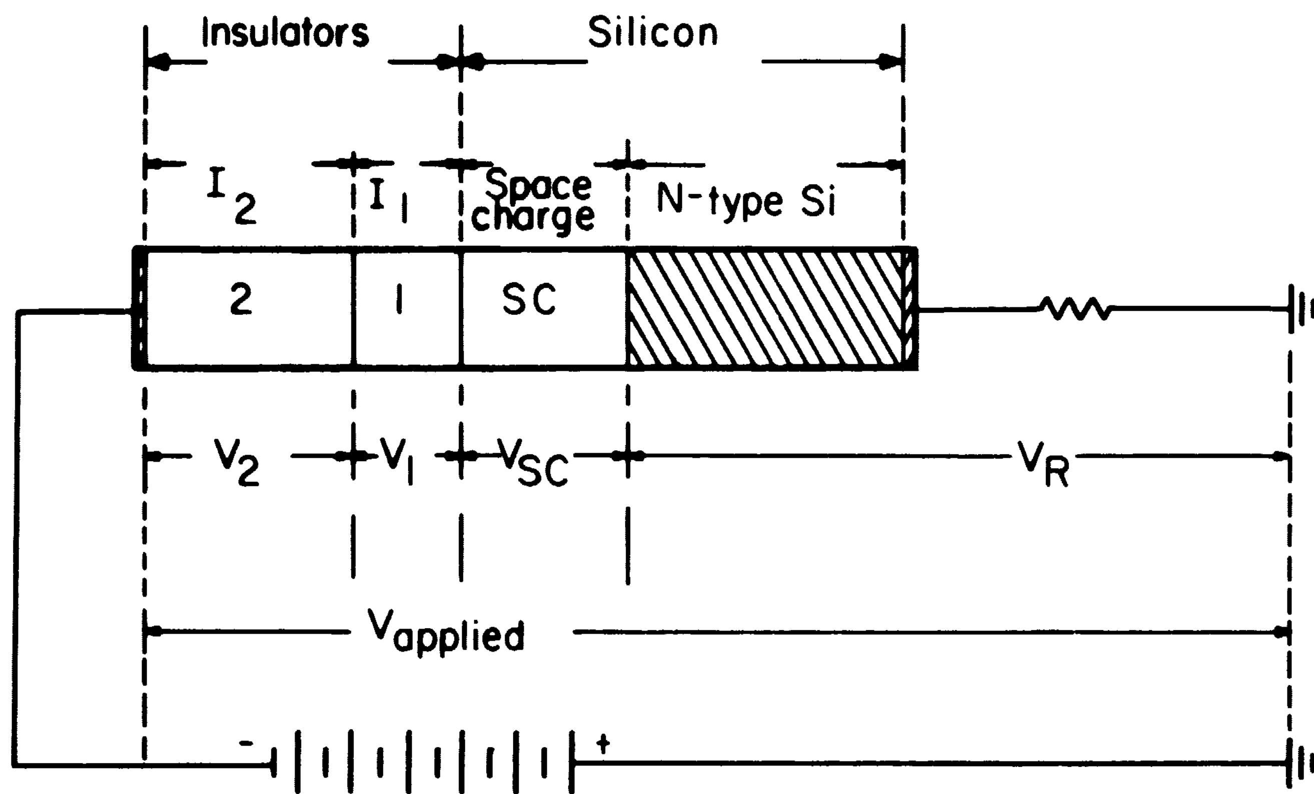


FIG. 16 Potential drops across $RC_{MI_2I_1S}$ circuit.

we find

$$E_2 = \left[V_{appl} + V_{FBf}\left(\frac{\epsilon_2}{\epsilon_1}\right)\left(\frac{x_1}{x_0 - x_1}\right)\right] \Big/ \left[x_0 - x_1 + \left(\frac{\epsilon_2}{\epsilon_1}\right)x_1\right].$$

Equation (C4) can be simplified to read

$$V_{appl} = V_{min} + V_{FBf}, \quad \text{(C8)}$$

where

$$V_{min} = E_{1f}\left(x_0 - x_1 + \frac{\epsilon_2}{\epsilon_1} x_1\right)\left(\frac{\epsilon_1}{\epsilon_2}\right).$$

The quantity E_{1f} is, of course, the field across region 1 and E_{2f} is the field across region 2, at which the density of the conduction current is equal in both regions, i.e.,

$$j_1(E_{1f}) = j_2(E_{2f}).$$

The actual value of $E_1 f$, and therefore of V_{FBf}, the final value of the flatband voltage, depends very much on the details of both the $j_1(E_1)$ and the $j_2(E_2)$ relationship, aside from the dependence on x_1, x_0, ϵ_1, ϵ_2, and V_{appl}. An instructive example of the role of these relationships is given in the last section.

A short postscript should be added with respect to real MI_2I_1S structures. These have a flatband voltage that is due to the presence of surface states, ionic charges in the dielectric, and the semiconductor-metal work function difference, before any charges were introduced into the dielectric by conduction. It is clear that the ionic charges will act much like the injected charges, except that their location is not as clearly defined. It can be assumed, however, that their effect simply

adds to or subtracts from the induced charges. The effect of the work function difference is operative regardless of the number of injected charges, and it generally is so small that it can be disregarded altogether. Surface states, however, may alter the whole picture. These states are charges at the silicon-insulator interface, so that they disturb the field distribution in region 1 to a great extent. They undoubtedly also affect the conduction mechanism in region 1 very severely, so that it is important to reduce them to a level much below that of the charges to be stored in the dielectric.

D. Transient Conditions

We will start by recalling that the charge density accumulated at the insulator-insulator boundary is assumed to be distributed over such a small distance that it can be considered a delta function distribution. As the charge accumulates, then, it does not vary with respect to distance, but only with respect to time. We can therefore write

$$eN_I = \int j_I dt. \qquad \text{(D1)}$$

The most important condition during the time that such a current j_I flows is that of current continuity across both regions 1 and 2. This is expressed by

$$\frac{dD_1}{dt} + j_1 = \frac{dD_2}{dt} + j_2 = j \qquad \text{(D2)}$$

where j is the total current flowing into and out of the MI_2I_1S capacitor electrodes, $\frac{dD_1}{dt}$ and $\frac{dD_2}{dt}$ are the displacement currents due to the charge build-up across regions 1 and 2, respectively, and j_1 and j_2 are the conduction currents flowing in regions 1 and 2.

In the exploration of the current vs time relationships that follow, the functional dependence j_I vs E_I will not be specified; the formulations from section II (conductance mechanisms) can be inserted when it becomes practicable. The structure we will consider is an MI_2I_1S capacitor with the silicon having n-type conductivity. A resistor will be placed in series with it. We will, for the present, assume that the initial flatband voltage of the capacitor is zero. When we apply a negative bias to this capacitor we have the added complication that a space charge region forms in the reverse-biased n-type substrate. We will start by allocating potential drops across the various parts of the circuit indicated in Fig. 16. . . We can write

$$V_{appl} = V_2 + V_1 + V_{SC} + V_R \tag{D3}$$

where $V_1 = E_1 x_1$, $V_2 = E_2(x_0 - x_1)$, and $V_R = iR = jAR$, where A is the area of the MI_2I_1S capacitor.

We will now derive V_{SC} in terms of E_1. D-vector continuity at the silicon-insulator interface demands that:

$$\text{(a)} \quad D_1 = D_{SC} \text{ and } E_{SC} = E_1 \frac{\epsilon_1}{\epsilon_{Si}}. \tag{D4}$$

(b) The space charge region in the silicon obeys Poisson's equation

$$\frac{dE_{SC}}{dx} = \frac{eN_D}{\epsilon_{Si}},$$

where N_D is the excess donor density in the silicon substrate.

(c) Integrating, we find

$$E_{SC} = \frac{e}{\epsilon_{Si}} \int_0^w N_D dx = \frac{eN_D}{\epsilon_{Si}} w,$$

where w is the width of the space charge region.

(d) Integrating again to obtain V_{SC}, we obtain

$$V_{SC} = \int_0^w \int_0^x \frac{eN_D}{\epsilon_{Si}} \, dx = \frac{eN_D}{2\epsilon_{Si}} w^2 .$$

(e) Substituting (c) into (d) to eliminate w, we find

$$V_{SC} = \frac{eN_D}{2G_{Si}} \left(\frac{E_{sc}\epsilon_{Si}}{eN_D} \right)^2 = \frac{E_{SC}^2 \epsilon_{Si}}{2eN_D} .$$

(f) From (a), $V_{SC} = \dfrac{E_1^2 \epsilon_1^2}{2 \epsilon_{Si} eN_D}$.

To express j in terms of E_1 we will make use of the continuity condition, Eq. (D2). To express E_2 in terms of E_1 we also make use of the continuity equation:

$$\frac{dE_2}{dt} = \frac{j_1 - j_2}{\epsilon_2} + \frac{\epsilon_1}{\epsilon_2} \frac{dE_1}{dt} , \text{ so that} \tag{D5}$$

$$E_2 = \int \frac{j_1 - j_2}{\epsilon_2} dt + \frac{\epsilon_1}{\epsilon_2} E_1$$

Now we can express everything in terms of E_1, except that the dependence of $j_2 = f(E_2)$ results in the fairly cumbersome

$$j_2 = f\left[\frac{\epsilon_1}{\epsilon_2} E_1 + \left(\frac{j_1 - j_2}{\epsilon_2} \right) dt \right] .$$

Going back to Eq. (D3), and expressing everything in terms of E_1, we find

$$V_{appl} = E_1 x_1 + \frac{j_1 - j_2}{\epsilon_2} dt + \frac{\epsilon_1}{\epsilon_2} E_1 \quad (x_0 - x_1) +$$

$$+ E_1^2(\epsilon_1^2/2\epsilon_{Si}eN_D) + (j_1 + \epsilon_1 \frac{dE_1}{dt}) AR . \qquad (D6)$$

In order to eliminate the integral sign, this equation can be differentiated with respect to time. This results in a nonlinear, inhomogeneous equation of second order in E_1, which up to now could not be solved.

The term containing E_1^2 is important only if the total transient takes less than about 10 msec in capacitors; in transistors even shorter transients make it unimportant. Any longer time will permit the formation of an inversion layer at the semiconductor-insulator interface, with the attendant partial disappearance of the carrier-free space charge region.

For positive applied voltage, the same steps leading to Eq. (D6) are applicable, except that instead of a space charge region, an accumulation region forms at the silicon-insulator interface. This means that in (D6) the term containing E_1^2 is again zero. Therefore, for a positive applied voltage:

$$V_{appl} = E_1 x_1 + \left(\int \frac{j_1 - j_2}{\epsilon_2} dt + \frac{\epsilon_1}{\epsilon_2} E_1 \right) (x_0 - x_1) \qquad (D7)$$

$$+ (j_1 + \epsilon_1 \frac{dE_1}{dt}) AR$$

This equation presents nearly the same difficulties as (D6), and has not been solved to date.

We can, however, obtain information about the time dependence of the total transient current j by realizing that it consists of a displacement current that simply charges up the capacitor and a conduction current that transfers charge into the insulator.

Let us assume first that the conduction current into the insulator is very high for any given E_1, so that as the voltage builds up across the

MI_2I_1S capacitor the conduction current into the insulator keeps pace, so that, instantaneously, the temporary voltage across the capacitor V_{appl} fulfills the condition (C8):

$$V'_{appl} = V'_{FBf} + V'_{min} \tag{C8}$$

The final V_{FBf} will then be reached at once when the MI_2I_1S capacitor has been completely charged. Therefore, the shortest time to build up V_{FBf} is that determined by the $RC_{MI_2I_1}$ time constant.

For a positive bias, with no space charge region formed in the silicon, the transient current simply follows the trivial

$$i = \frac{V_{appl}}{R} \exp(-t/RC) \tag{D8}$$

For a negative bias, the space charge region complicates matters. We can use Eq. (D6), setting currents j_1 and j_2 equal to zero. Then

$$V_{appl} = E_1\left[x_1 + \frac{\epsilon_1}{\epsilon_2}(x_o - x_1)\right] + E_1^2\left(\epsilon_1^2/2\epsilon_{Si}eN_D\right) + \epsilon_1 AR\frac{dE_1}{dt}. \tag{D9}$$

Clearly, the variables can be separated to form

$$\int\frac{dE_1}{V_{appl} - E_1x_o' - E_1^2\beta^2} = \frac{t}{\epsilon_1 AR} + \text{constant} \tag{D10}$$

where

$$x_o' = x_1 + \frac{\epsilon_1}{\epsilon_2}(x_o - x_1),$$

$$\beta^2 = \epsilon_1^2/2\epsilon_{Si} \cdot eN_D,$$

which can be converted into

$$\int \frac{dE_1}{E_1 + B^2E_1^2 - E_A} = - \frac{t}{RC} + \text{constant} \tag{D11}$$

where

$$B^2 = \beta^2/x_0',$$

$$C = \frac{\epsilon_1 A}{x_0'},$$

$$E_A = \frac{V_{appl}}{x_0'}.$$

This can be solved with a standard solution from a table of integrals and from the condition that $E_1 = 0$ when $t = 0$. The solution is

$$E_1 = \frac{1}{2B} \left[\frac{K(1 + M\exp(-Kt/RC)}{1 - M\exp(-Kt/RC)} - 1 \right], \tag{D12}$$

where

$$K = (4E_AB + 1)^{1/2}$$

$$M = (1/K)\ \ln \left[(1 - K)/(1 + K)\right]$$

From this equation, the build-up of other fields or voltages can be derived. The transient current is of course $i = \epsilon_1 A \frac{dE_1}{dt}$, which results in

$$i = \frac{x_0'}{R} \left(E_A - \frac{1}{4B} \left\{ \left[\frac{K(1 + M\exp(-Kt/RC)}{1 - M\exp(-Kt/RC)} \right]^2 - 1 \right\} \right). \tag{D13}$$

Let us assume now that the current density due to conduction in the dielectric is very low, so essentially all charge transfer occurs only

when the MI_2I_1S capacitor has charged up long ago. In that case, the iR drop due to the series resistor can be neglected, and we can write

$$V_{appl} = E_1 x_1 + \left(\int \frac{j_1 - j_2}{\epsilon_2} dt + \frac{\epsilon_1}{\epsilon_2} E_1 \right) (x_0 - x_1), \tag{D14}$$

which can be differentiated with respect to d/dt and rearranged to form

$$\int_{E_{1f}}^{E_A} dE_1 / \left[j_1(E_1) - j_2(E_1) \right] = t / \left(\frac{\epsilon_2 x_1}{x_0 - x_1} + \epsilon_1 \right) \tag{D15}$$

for positive bias. For negative bias, similar manipulations result in

$$\int_{E_{1f}}^{E_A} \left[1 + E_1 \epsilon_1^{2} / \epsilon_{Si} e N_D x_0 \right] dE_1 / \left[j_1(E_1) - j_2(E_1) \right] = t / \left(\frac{\epsilon_2 x_1}{x_0 - x_1} + \epsilon_1 \right) \tag{D16}$$

by setting the last term in (D6) equal to zero.

When we apply these equations to a real structure, we have to consider the presence of a charge already present in the MI_2I_1S structure, which can be expressed as a flatband voltage V_{FB}. If V_{FB} is negative and V_{appl} is negative, the capacitor will behave as a simple MI_2I_1S capacitor until E_1 is zero; that is, for a short time t' defined by

$$V_{FB} = V_{appl}[1 - \exp(t'/RC)].$$

Then depletion sets in, and Eqs. (D6), (D9), or (D12) apply, with V_{appl} in those equations replaced by $V_{appl} - V_{FB}$.

If V_{FB} is negative and V_{appl} is positive, both fields add to E_1, and we can replace V_{appl} in Eqs. (D7), (D8) and (D11) by $(V_{appl} + V_{FB})$. If V_{FB} is positive and V_{appl} is negative, both fields again add to form E_1.

But since we started from a static condition, an inversion layer has already formed that neutralizes the field due to V_{FB}. Therefore Eqs. (D6), (D8), and (D12) can be used without modifying V_{appl}. Finally, if V_{FB} is positive and V_{appl} is positive, Eqs. (D7), (D8) and (D11) can be used in replacing V_{appl} with $(V_{appl} - V_{FB})$.

E. Charge Decay

The decrease in an existing charge density can be brought about by a migration of those charges away from their original site or by the removal of charges through neutralization by carriers of the opposite sign. The rate of charge density decrease has the dimensions of a current density. There can be two limiting mechanisms that control this rate. Assuming purely electronic conduction, the first is that the rates of negative charge removal by conduction away from the trap, or positive charge removal by electron currents towards the traps, are slower than the rate of thermal activation of negative charges into the conduction band, or the rate of recombination of conduction electrons with positively charged traps. For this case, the $j_I = f(E_I)$ laws should determine the rates of carrier transportation. If, instead, thermal activation of negative charges and electron-trap recombination of positive charges are rate-determining, the decay laws will depend on the respective activation energies and on the density of charged traps. The effective activation energies would depend on the charged trap density due to the field set up by the charges, and the recombination rates of the positive traps would depend on charge density in controlling the density of electrons available for recombination.

If current transport is the rate limiting step, the whole problem is really a special aspect of the equations derived in sections 3 and 4.

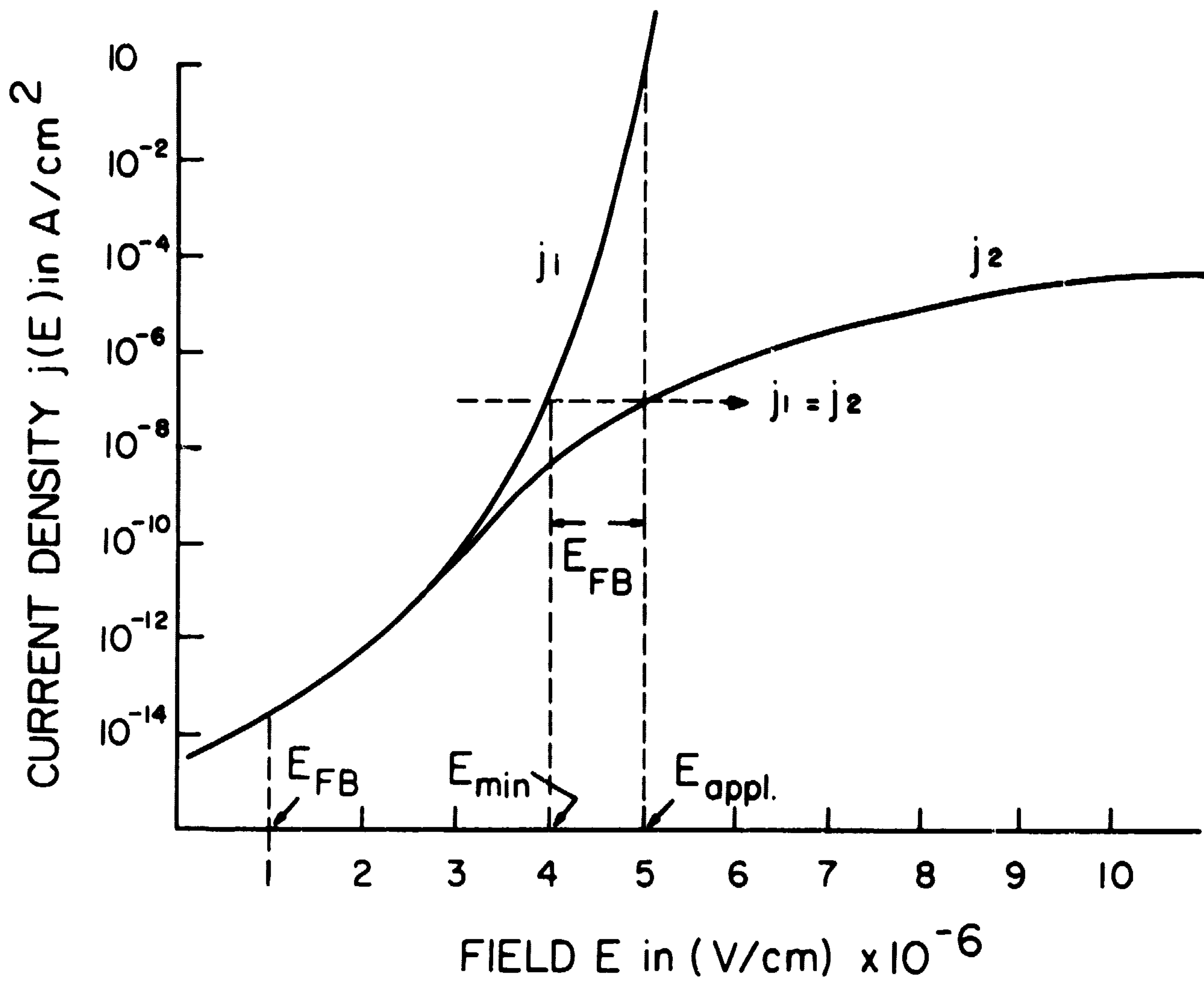


FIG. 17 Plot of idealized current density vs field for dielectrics I_1 and I_2 .

The only difference is that V_{appl} is either zero or, at any rate, below V_{min}. Recalling Eqs. (C6) and (C7) and setting $V_{appl} = 0$ we find that

$$E_1 = - V_{FB} \frac{\epsilon_2}{\epsilon_1} \Big/ \left(x_0 - x_1 + \frac{\epsilon_2}{\epsilon_1} x_1\right), \text{ and} \tag{E1}$$

$$E_2 = + V_{FB} \frac{\epsilon_2}{\epsilon_1} \; \frac{x_1}{x_0 - x_1} \Big/ \left(x_0 - x_1 \frac{\epsilon_2}{\epsilon_1} x_1\right) \tag{E2}$$

Since E is a vector quantity, E_1 and E_2 must have opposing signs because they originate from the same charge distribution at x_1, but point in opposite directions. This is seen for the case of $V_{appl} = 0$ in Eq. (C3):

$$E_1 x_1 = - E_2 \; (x_0 - x_1). \tag{E3}$$

Finally, Poisson's equation is still valid, i.e.

$$D_2 = D_1 + eN_I \tag{E4}$$

which, differentiated, yields

$$\frac{dD_2}{dt} = \frac{dD_1}{dt} + e \frac{dN_I}{dt} \tag{E5}$$

The rate of charge density change is equal to the sum of the conduction currents j_2 and j_1,

$$e \frac{dN_I}{dt} = j_2 + j_1, \tag{E6}$$

so that

$$\frac{dD_2}{dt} = \frac{dD_1}{dt} + j_2 + j_1 \tag{E7}$$

Substituting (E3) into (E7) and eliminating $\frac{dE_2}{dt}$ results in

$$\int dE_1/[j_2(E_1) + j_1(E_1)] = -t/[\epsilon_1 + \epsilon_2 \left(\frac{x_1}{x_0 - x_1}\right)] \tag{E8}$$

This integral can be solved at least numerically. Since

$$-eN_I = \left[\epsilon_2 \left(\frac{x_1}{x_0 - x_1}\right) + \epsilon_1\right] E_1, \tag{E9}$$

the decay law calculated in (E8) will give the charge density decay with the help of (E9) and the flatband voltage decay from (C5).

Considering a decay mechanism that is limited by the rate of escape of the charges from their traps, we assume again the material is an electronic conductor. Negative trapped charges must escape by themselves and drift away to result in a reduction of charge density. Positive trapped charges must be neutralized by electrons with the proper activation energy. Negative charges in traps would set up a field that would repel other carriers. Simultaneously, this field would lower the activation energy of the trapped charges much as in the Poole-Frenkel effect. Intuitively then,

$$\frac{dN_I}{dt} = -k_- N_I \exp\{-e[\varphi_t - (eE/\pi\epsilon_0\epsilon_d)^{1/2}]/kT\} \tag{E10}$$

Integration of (E10) will result in an expression of the form:

$$\frac{Pt}{2} = \text{Const} - \log N_I^{1/2} + \frac{\alpha N_I^{1/2}}{1 \cdot 1!} - \frac{\alpha^2 N_I^{2/2}}{2 \cdot 2!} + \frac{\alpha^3 N_I^{3/2}}{3 \cdot 3!} - \cdots$$

where P and α are constants.

Positive charges in traps would attract electrons, so that local charge neutrality would exist. However, since this is a two-particle process,

and since detailed neutrality is assumed, the decay rate would be proportional to the square of the existing charge density. However, this neutrality would prevent the operation of a Poole-Frenkel mechanism. Therefore,

$$\frac{dN_{I+}}{dt} = - k_{+}(A-N_{I+})^{2} \exp(- e\varphi_{t}/kT). \tag{E12}$$

This equation can be integrated to result in

$$Kt = \frac{N_{I+}}{A(A - N_{I+})} \tag{E13}$$

where K and A are constants.

It is clear that either rate limiting mechanism may become important during different periods of the decay of the same accumulated charge.

F. Summary

In the preceding sections the details of the memory characteristics of the variable-threshold-voltage IGFET have been explained. They are based on the elements of an MIS capacitor whose dielectric has two coplanar regions of different conductivity. This difference may arise from the fact that there are two different materials, or it may be due to two conduction mechanisms operating in the same material, one at the surface and one in the bulk. The theoretical model is the same for either structure. As a matter of fact, in the course of experimentation both have been realized. When a voltage is placed across this $MI_2 I_1 S$ capacitor, both regions transport electrons, but at different rates, so that charge accumulation must occur at the interface.

This accumulating charge lowers the field across the more highly conducting region, so that its conduction progressively decreases. Charge accumulation ceases when the currents in both regions have become equal. The current laws in thin film insulators all require the existence of traps (see section III 2), so that the storage of the accumulated charge in traps does not require additional assumptions. The rate of decrease of the stored charge may be controlled simply by the charge transport mechanisms active in the structure at the low fields generated by the stored charge. It may also be controlled by an activation process even slower than charge leakage. In that case, additional deep traps, due to doping or the existence of an interface, must be postulated. The possibility of this slight complication will be ignored to give unity to the following discussion.

All memory characteristics of the device, steady-state, transient, or storage characteristics, are dependent on the relative relationships of the two conductance laws $j_1(E_1)$ and $j_2(E_2)$. The high field characteristics determine the write-in speed, the relative magnitudes of j_1 and j_2, and the amount of charge stored, while the low field characteristics determine the rate of charge decay. In order to obtain the observed write-in time of about a microsecond and a charge decay time of the order of a few months, the current density range must extend over thirteen orders of magnitude for applied fields ranging from 5×10^5 to 5×10^6. This will be illustrated in the following examples. As an aid, idealized plots of currents j_1 and j_2 have been drawn as a function of field in Fig. 17. In order to ease the discussion, it is assumed that $x_1 = 0$ and $\epsilon_1 = \epsilon_2$, so that, from Eq. (C7), $E_2 f = V_{appl}/x_o = E_{appl}$, and from Eq. (C6), $E_1 f = (V_{appl} - V_{FBf})/x_o = E_{appl} - E_{FBf}$. At the instant when E_{appl} appears across region 1, a large current j_1 flows

until the accumulating charge density at the interface between region 1 and 2 has built up an opposing field E_{FB}. When $j_1 = j_2$, no further change in field occurs. When the switching field E_{appl} is removed only the field E_{FB} due to the interface charge remains, and it starts to decay (assuming conduction mode decay) at a rate given by the current at that field.

Assuming that $x_0 = 1000$ Å, we can calculate all pertinent characteristics, since $V_i = E_i \times 10^{-5}$. A plot of V_{appl} vs V_{FB} is derived by finding the value of j_2 at E_{appl} and then finding the field $E_{1f} = E_{min}$ (see Eq. (C8)) at the same current density on the j_1 curve. The difference between E_{appl} and E_{min} is E_{FB}. The specific values indicated in Fig. 17 are $V_{appl} = 50$ V, $V_{min} = 40$ V; V_{FB} is therefore 10 V. Conduction current equality exists at a current level of 10^{-7} A/cm^2.

An estimate of the switching time can be obtained by utilizing a simplified form of Eq. (D5). It is obtained by setting $j_2 = 0$ and otherwise utilizing $\epsilon_2 = \epsilon_1$ and $x_1 = 0$ (which makes $\Delta E_2 = 0$). Then,

$$\Delta t = \epsilon_1 \Delta E_1 / j_1 = \epsilon_1 E_{FB} / j_1 .$$

Using $\epsilon_1 = 3.5 \times 10^{-13}$ and j_1 at $E_{appl} = 1$ A/cm^2, we find Δt for write-in is 0.4×10^{-6} sec.

For the decay time, we can use the same expression except that ΔE_1 is now ΔE_{FB}, which we will assume to be 5×10^6 V/cm and j_1 at $E_{FB} - 1/2\Delta E_{FB} \simeq 10^{-14}$ A/cm^2. The decay time Δt for loss of one-half the flatband voltage is calculated from this to be 1.8×10^7 sec, or about seven months.

It should be pointed out that the j vs E relationships in Fig. 17 were drawn to illustrate the theory. Both curves have not yet been fully established by experiment, although the data in existence indicate that the whole range of current levels shown is in error by probably less than two orders of magnitude.

This exercise shows clearly that all steady-state and transient charge build-up relationships can be derived from a knowledge of the j vs E relationships in both regions of the insulator. It is quite sufficient that this knowledge is only empirical, although theoretical relationships will naturally be of interest.

The behavior of the device characteristics as a function of temperature can also be predicted on the basis of j vs E curves taken at the appropriate temperatures. The low field j vs E curves represent at least the upper boundary of the decay of the stored charge. Experiments will decide this question.

IV. FUTURE WORK

In the previous section it was established that all device characteristics should be predictable from j vs E plots of properly constructed MI_2I_1S capacitors. Only the dependence of the charge decay rate on these plots is at this moment not established. The work in the next two months will be concentrated on proving out all aspects of this theory. This will be accomplished by constructing MI_1S and MI_2S capacitors, finding their j vs E plots, and then forming an MI_2I_1S capacitor and measuring its E_{FB} and $j_1 = j_2$ conditions as a function of applied voltage. Ideally, the j_1 vs E_1 and j_2 vs E_2 plots determined with the MI_1I_2S capacitor will agree exactly with those measured separately in MI_1S and MI_2S capacitors.

The next step will be a detailed investigation of the charge decay mechanism using the same approach of MI_1S, MI_2S and MI_1I_2S capacitor construction. These studies will be repeated at several temperatures. After this, a program will be put into effect to optimize switching sensitivity, write-in speed, and charge storage by controlled modifications of the material properties in regions 1 and 2.

NEW TECHNOLOGY APPENDIX

After a diligent review of the work performed under this contract, no new innovation,discovery, improvement or invention was made.

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