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STUDY OF SEMICONDUCTOR HETEROJUNCTIONS OF ZnSe, GaAs and Ge

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ABSTRACT

The fabrication problems and device characteristics of Ge-GaAs and ZnSe-GaAs heterojunctions are being studied.

The quality of the ZnSe layer grown on GaAs, using a close-spaced HCl process, has been investigated as a function of the substrate orientation. The best layers have been obtained for GaAs substrates oriented 5° off (111) and low HCl concentrations. Various techniques for diffusing Zn into the ZnSe layer to reduce its resistivity and through it to form the base region of an nZnSe-pGaAs-nGaAs transistor have been studied. Process control is quite critical in this technology in order to obtain useful transistor performance.

The low-temperature iodine system has been used to grow Ge on GaAs. Preliminary measurements on the resulting diodes showed considerable improvement in their forward i-^{v} characteristics and no trace of cross-diffusion.

The solar-cell efficiency of ZnSe-GaAs, GaP-Si, ZnSe-Ge and GaAs-Ge heterojunctions have been computed and compared with Si and GaAs homojunction cells. The performance potential of ZnSe-GaAs cells is shown to exceed that for both Si and GaAs cells if interface recombination losses are small.

I. INTRODUCTION

The investigations during this quarter on our grant have been concerned with the fabrication of ZnSe-GaAs heterojunction transistors, the low temperature growth of Ge-GaAs heterojunction transistors and a theoretical study of the expected performance of heterojunction solar cells.

The studies of the ZnSe-GaAs transistor are concerned with the dependence of the quality of the grown layer on the substrate orientation, the techniques for fabricating ZnSe-GaAs transistors with low resistivity ZnSe and suitable GaAs base widths and methods for obtaining heavily doped ZnSe layers. The study of Ge-GaAs heterojunctions has concentrated on the low temperature growth of Ge on GaAs using low temperature iodine transport in order to reduce cross doping between the Ge and GaAs and improve the device characteristics.

The solar-cell study has been conducted in order to compare the efficiency of the most promising heterojunction cells with the performance of Si and GaAs homojunction cells.

2. STUDIES OF THE GROWTH OF ZnSe UPON GaAs

In the last quarterly report ZnSe growths on various major orientations of GaAs were studied using the HCl close-spaced vapor transport growth system. The results revealed that ZnSe grew smoothly on or near the (100) orientation but not on (111) orientations where structured surfaces (of pyramids and hillocks) occurred. Growth rates were typically 2-6 μm/hr depending on HCl concentrations and growth temperatures. Smooth growths are particularly desirable for heterojunction planar diffused transistor fabrication. So during this quarter, growth studies on misoriented (100) and (111) GaAs were continued, with the hope that misoriented (111) seeds might produce smooth growths. Misoriented (111) material may have some advantage in the reduced number of interface states, expected from lattice mismatch considerations, in the (111) plane relative to the (100) plane. This is a consideration in transistor work where interface states can reduce gain.

Growths were made upon GaAs planes misoriented 5° off the (100) plane (toward (111) plane) and 5° off the (111) plane (toward the (100) plane). Growths on 5° off (100) GaAs were mirror smooth. Growths on 5° off (111) GaAs resulted in high densities of 1 μm high pyramids if the HCl concentration was above .05%. For low HCl concentrations (.02-.05%) only a slight ripple can be seen on the grown ZnSe surface. High HCl concentrations penetrate the protective SiO_2 on the GaAs side and bottom surfaces not grown upon. This causes As and Ga compound formation which may lead to pyramids on the growth face. Growth rates of smooth ZnSe layers grown on 5° off (100) and (111) GaAs substrates are about 3.5-4.0 μm/hr for standard growth conditions (Source Temp = 760°C; Seed Temp = 640°C; .04% HCl; and total H_2 flow = 200 cc/min). These results look encouraging and in the near future transistors will be made from ZnSe grown upon 5° off (111) n type GaAs.

3. ZnSe-GaAs TRANSISTORS

During this quarter better methods of making transistors were developed using Zn diffusion through ZnSe into GaAs to form thin p-type base regions. ZnSe resistivity (ρ_{ZnSe}), base surface carrier concentration (C_{SB}), and base width (W) are all controlled simultaneously during the Zn diffusion step and are therefore dependent on each other through the diffusion temperature (T_D), diffusion time (t_D), and ZnSe thickness (d_{ZnSe}). The ideal ZnSe-GaAs transistor would appear to have a low ZnSe resistivity (low emitter resistance, high frequency response), high C_{SB} (high drift field to favor injection), and small base-width W (to prevent base recombination since the lifetime is 10^{-9} - 10^{-10} sec. in GaAs). High T_D favors low ρ_{ZnSe} and high C_{SB} while producing base widths too large. Low T_D produces moderate ρ_{ZnSe}, low C_{SB} and small base widths. Consequently T_D, t_D, and d_{ZnSe} must be optimized. Using the Zn vapor-diffusion closed-ampoule quenching technique the highest gain transistors ($\beta \approx 50$) were obtained with the following parameters.

T_D = 650°C - 700°C

t_D = 5 min - 60 min

d_{ZnSe} = 3-4 μm

ρ_{ZnSe} = 10^5 - 10^6 Ω-cm

C_{SB} = 10^{18} cm^{-3}

W = .2 - .5 μm

It was always necessary to have the ZnSe resistivity large (say 10^5 instead of 10^3 ohm-cm) to obtain the highest gain. Similar behavior has been experienced in ZnSe-Ge transistors and is tentatively explained if wide depletion widths in the ZnSe have the effect of reducing the defect current at the ZnSe-Ge interface. This may also occur in ZnSe-GaAs transistors. Consequently, in transistor fabrication ρ_{ZnSe} and W will be made low while C_{SB} is made high by using reasonably high temperatures, short times, and small ZnSe thicknesses. Then ρ_{ZnSe} can be increased by heating at moderate temperatures (where C_{SB} and W are not affected) to adjust the transistor for proper gain or frequency response. It should be noted here that the ZnSe resistivity affects not only gain but also emitter resistance so that in increasing ρ_{ZnSe} one trades off low emitter resistance, good frequency response, and small offset voltage for increased gain.

The method of closed tube Zn diffusion followed by quenching is capable of simultaneously producing ρ_{ZnSe} as low as 10^3 Ω-cm and C_{SB} as high as 5 x 10^{18} cm^{-3} with base widths down to .5 μm. However this process is unreliable because the ZnSe resistivity depends on a quenching step, and is not repeatable. The reason for this is that Zn outdiffuses from ZnSe so fast at the quenching temperature (650°C-700°C) that a few microns of ZnSe is easily converted to semi-insulating material before the temperature can drop sufficiently. Thicker ZnSe layers (5 μm or more) which would not all be converted to high ρ, crack from the quenching step and also reduce C_{SB}. The quenching process cannot be controlled accurately enough to guarantee low ρ_{ZnSe} (10^3 Ω-cm) more than 20% of the time. Thus, alternative methods of transistor fabrication were tried.

The first alternate method tried was evaporating Zn layers on grown ZnSe, sealing the evaporated sample with a small amount of Zn in an evacuated ampoule, heating slowly to the diffusion temperature, diffusing, cooling slowly to room temperature, and removing the Zn layer. The small amount of added Zn provides an equilibrium Zn vapor pressure to suppress Zn evaporation from the sample during heating. This method allows the sample to be temperature cycled slowly so that any interface strain can be annealed out and produces base widths from .1 - .5 μm with gains as high as 50. However the ZnSe resistivity obtained was never lower than 5 x 10^4 Ω-cm because the evaporated Zn layers always cracked off during heating. The method was abandoned because the cracking problem was associated with the Zn-ZnSe interface properties, and no protective coating (Ni and Cr were tried) could alter the problem.

Another method tried was closed-tube vapor diffusion of Cd into grown ZnSe followed by quenching. Cd is a Group II element, and it should replace Zn (fill up Zn vacancies) in ZnSe. Cd diffusions in high resistivity (10^8 ohm-cm) Ga doped bulk ZnSe have produced 10 ohm-cm ZnSe (Zn treatment produces 0.1 ohm-cm ZnSe) showing that the method is feasible. Diffusion of Cd in ZnSe may be slower than Zn, and it was hoped that outdiffusion of Cd during quenching would be slow enough to prevent the ZnSe from becoming high resistivity. However when ZnSe-GaAs structures were heated in Cd vapor to 650°C for 20 min. and cooled, the grown ZnSe layer was found to have been completely removed by the Cd vapor. Doped p-layers of .1 - .2 μm were formed in the unattacked GaAs indicating that Cd was effective as a p-type base formation dopant.

Cd attack of grown ZnSe layers prompted using a thin protective layer of SiO_2 pyrolytically deposited on grown ZnSe at 430°C. Either Cd or Zn can diffuse through this layer reaching the ZnSe at reduced concentrations preventing attack. The SiO_2 has the advantage of preventing the outdiffusion of Cd or Zn during the quenching step since Zn and Cd diffuse much slower through SiO_2 than ZnSe. Its disadvantages are that higher temperatures or longer times are necessary to achieve necessary base widths and that C_{SB} is lowered due to a reduced Zn concentration produced by the SiO_2. Therefore, the SiO_2 thickness

must be made small enough to allow good base width control and yet thick enough to prevent Zn or Cd outdiffusion and attack. With these ideas in mind a 500-1000 Å layer of SiO_2 was grown upon a 4 μm ZnSe grown layer (on GaAs). Zn was used as a diffusant since it produces two orders of magnitude lower ρ_{ZnSe} than does Cd under identical conditions. Table I summarizes the diffusion results. Samples were quenched from the diffusion temperature.

Run #	d_{SiO_2}	d_{ZnSe}	T_D	t_D	ρ_{ZnSe}	W
TR-13-B	500Å	3.5μm	700°C	60min	$10^3\Omega$-cm	25μm
TR-13-C	500Å	3.5μm	650°C	20min	$10^3\Omega$-cm	1μm
TR-13-D	1000Å	3.5μm	630°C	10min	$10^4\Omega$-cm	.1μm
TR-14-100	1000Å	4μm	625°C	30min	$5\times10^3\Omega$-cm	.25μm

Table I ZnSe-GaAs Transistor Fabrication Using SiO_2 Mask and Zn Vapor-Quenching Process((100) GaAs, $n = 1 \times 10^{16}cm^{-3}$)

Although emitter base and collector-base V-I characteristics were very good for all of these devices, little to no transistor action was seen. One sample of TR-14-100 showed a gain of unity. TR-14-100 has ideal transistor parameters, but its low gain indicates that either the ZnSe-GaAs interface properties are preventing injection, C_{SB} is too low, or the GaAs electron lifetime is too low. Material from only one boule of GaAs was used for the SiO_2 experiments, and it is believed that its lifetime is too low to make transistors. New material has been ordered. In the interval before it arrives, thinner oxides will be tried to increase C_{SB} and see whether this is responsible for low gain. The higher ρ_{ZnSe} of TR-13-D and TR-14-100, where the SiO_2 thickness is higher, indicates that the Zn concentration is low making C_{SB} low. Figure 1 shows a typical emitter-base (ZnSe-GaAs) V-I characteristic for a Zn diffused SiO_2 protected transistor. Note that an exponential current variation, $I \propto e^{qV/\eta kT}$ occurs with $\eta = 1.45$ for $I < 10^{-4}$ A whereas

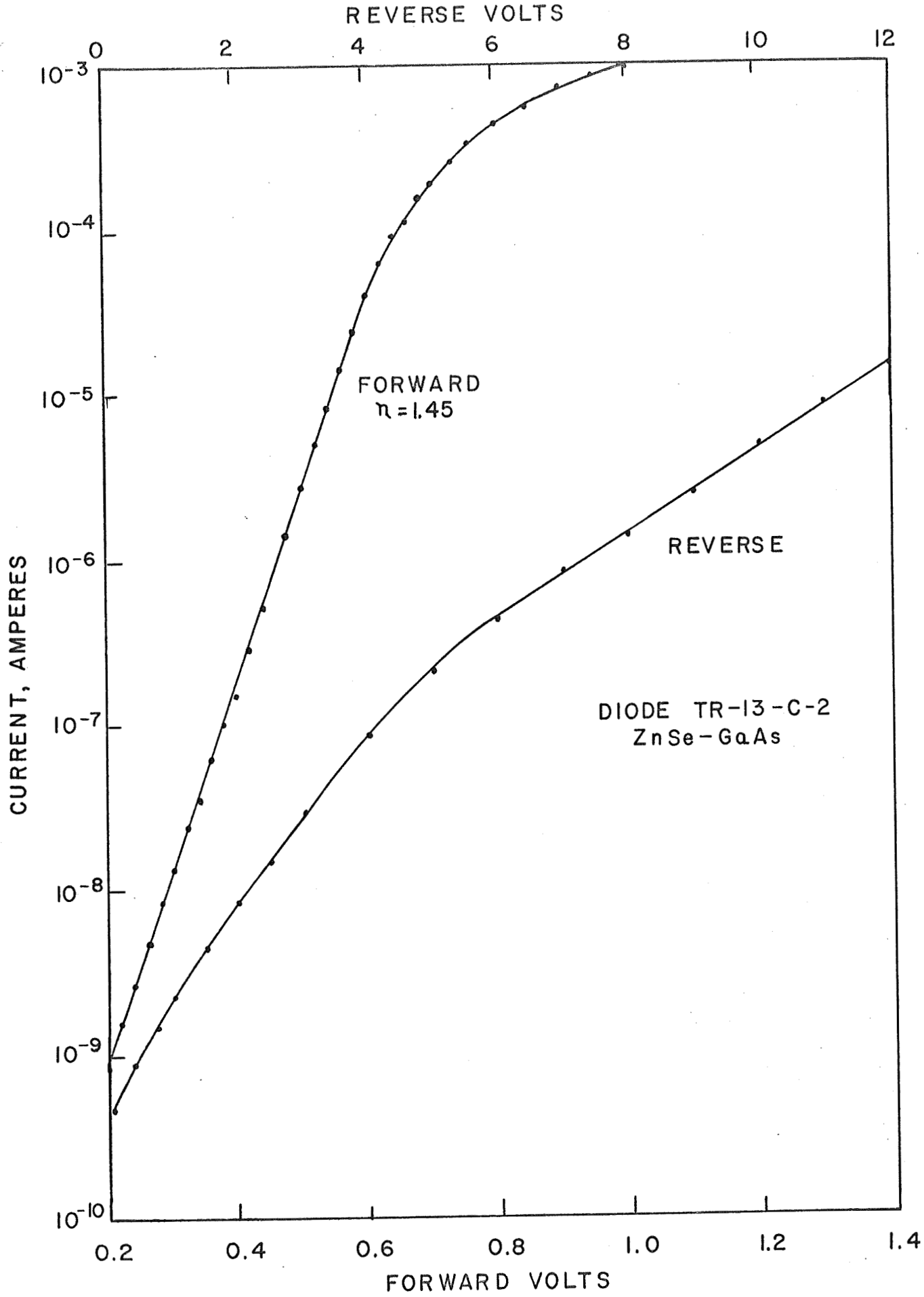

Fig. 1 ZnSe-GaAs Emitter-Base
V-I Characteristic

previously made emitter-base diodes always yielded a power low characteristic, $I \propto V^n$. There is a chance that the ZnSe resistivity is less than 10^3 Ω-cm, and that the heterojunction is not being masked by space charge effects in the ZnSe. The exact ρ_{ZnSe} has yet to be measured with any accuracy because there is always significant current conduction through the thin p layer in the GaAs. The "bending over" of the forward curve above 10^{-4} A is not understood at this time. Measurements were taken using the two contact technique that eliminates series resistance so that the bending cannot be attributed to series resistance unless there is significant lateral flow between contacts. The reverse characteristic does not follow a power law and appears to be exponential above 5×10^{-7} A. The collector-base junction has an exponential forward characteristic $I \propto e^{qV/\eta kT}$ where $\eta = 2.4$ for $2 \times 10^{-7} A < I < 5 \times 10^{-4}$ A and tends to $\eta = 4$ for higher currents. The reverse breakdown is hard at 12-15 volts (typically $I = 10^{-7}$ A at 12 volts).

4. PROGRESS IN OBTAINING HEAVILY DOPED n ZnSe p GaAs

Some recent experiments have been successful in providing us with lower resistivity ZnSe layers than ever before. The procedure adopted is to grow the layer in the normal way on GaAs, and then induce the n type doping by Se vacancy generation. The nZnSe-pGaAs structures after growth are completely coated on all faces with SiO_2 and heated in Zn vapor at 900°C. The vapor pressure of Zn at this temperature is about one atmosphere, and Se diffuses out quite rapidly and the Se vacancies act as donors provided the Zn vacancies are suppressed. The method produces 0.1 ohm-cm n type ZnSe when bulk ZnSe is used. When layer structures are used direct measurement of the ZnSe resistivity is not easy but the resistance has certainly been considerably lowered from the usual 10^3 - 10^5 ohm-cm range. The role of the SiO_2 coating is to prevent Zn attack of the GaAs and rapid Zn vacancy creation in the ZnSe. Se diffuses through SiO_2 much faster than does Zn, so that there should be no problem in diffusion through the oxide at 900°C. This method is presently not capable of producing ZnSe-GaAs transistors because base widths would be too large at 900°C. But ZnSe layers of low resistivity on heavily doped p type GaAs should give useful information about the ZnSe-GaAs interface, now unobtainable because ρ_{ZnSe} is too large.

Such heavily doped ZnSe-GaAs diodes may also be efficient light emitters.

The 900°C Zn treatment was applied to two samples of ZnSe grown upon .01 Ω-cm p-type GaAs. The samples were slowly heated to 900°C, diffused for 1/2 hour, cooled slowly to 650°C, and then quenched. One sample was attacked by the Zn presumably because of an imperfect SiO_2 coating but the other survived. The survivor showed signs of interface strain when lightly etched. Several diodes were easily fabricated. Fig. 2 shows the V-I characteristic of such an nZnSe-pGaAs diode. There are several exponential regions the most interesting of which is the region 10^{-4} A $< I < 10^{-2}$ A where η is less than unity. This behavior is not easily explained and will require more experimental work. The resistivity of the ZnSe was estimated at about .5 Ω-cm from series resistance measurements. These results look promising in that space charge effects and high series resistance have been eliminated. The reverse characteristic follows a power low of $I \propto V^{4.5}$ from 10^{-8}A $< I < 10^{-4}$ A. Breakdown is soft at about 10 volts. Fig. 3 compares the V-I curve of a typical ZnSe-GaAs emitter-base diode diffused through SiO_2 at 650°C with the curve of the 900°C treated ZnSe-GaAs diode. We are hopeful that these promising new characteristics will enable us to make a study of the nZnSe-pGaAs interface that may be useful with respect to both optical device and transistor performance.

5. LOW TEMPERATURE GROWTH OF Ge ON GaAs BY IODINE TRANSPORT

Work this quarter included the fabrication of an inverting seed holder, replacement of a length of dopant carrying tubing, alteration of the dopant introduction tip, growths of undoped and p-type layers using the inverting seed holder, and some preliminary evaluation of grown heterodiode devices.

In an effort to promote full transport of dopants (particularly the p-type dopant boron tri-iodide) from their sources into the deposition region, the length of pyrex tubing connecting the sources to the quartz dopant introduction fitting has been replaced with capillary tubing. Such replacement produces a reduction in cross section of about twenty times with a corresponding increase in dopant carrier flow velocity.

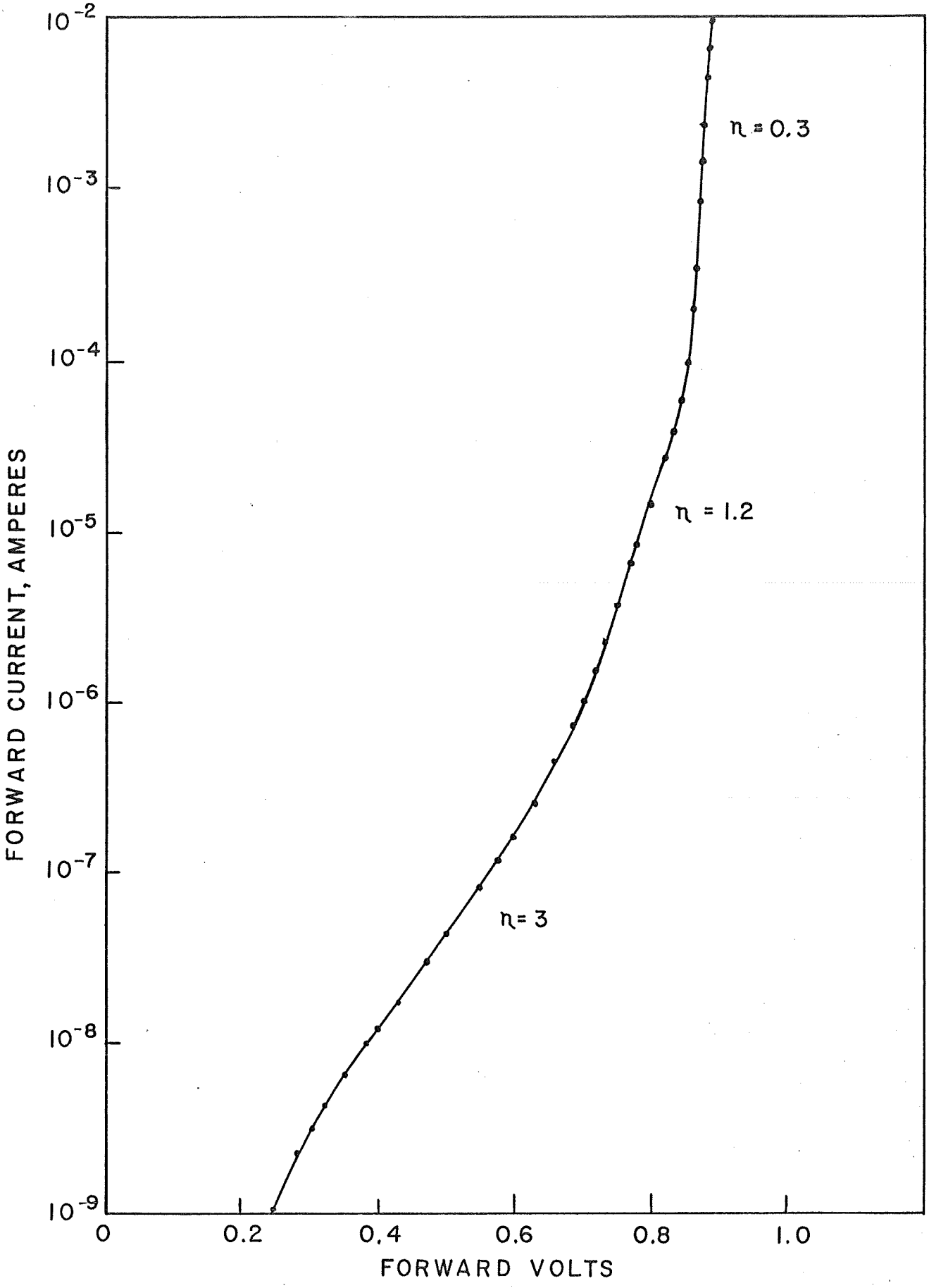

Fig. 2 nZnSe-pGaAs Junction Forward Characteristic
After 900°C Zn Vapor Treatment

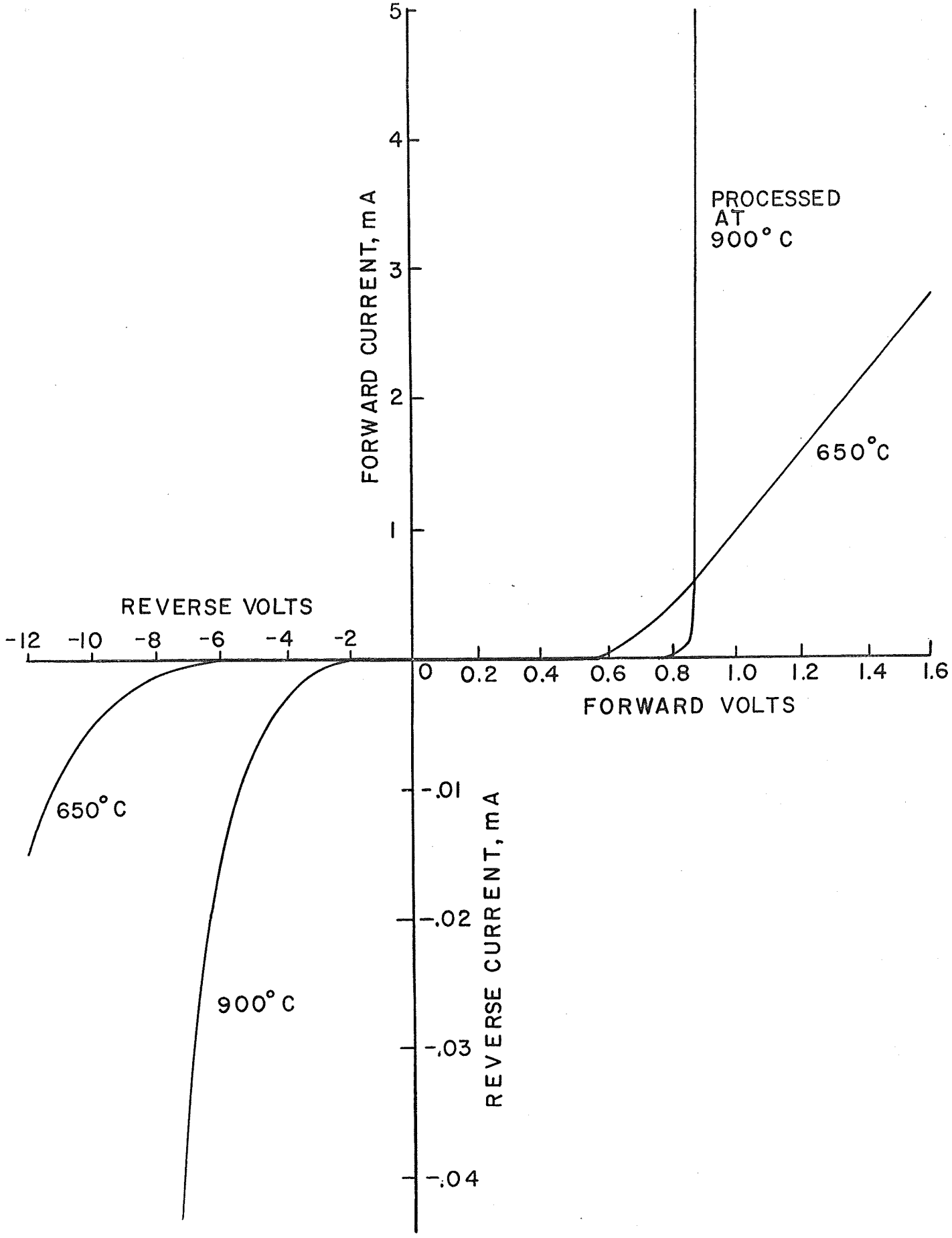

Fig. 3 Comparison of ZnSe-GaAs V-I Curves of Diodes, With Different Zn Vapor Treatments at 900°C and 650°C

This effect is especially important when small amounts of dopants are to be introduced or when dopant types are to be changed in forming multi-layer structures. In previous attempts to grow high resistivity p-type germanium with low boron tri-iodide carrier gas flow rates, no dopant has transported to the seed area resulting in n-type growths.

A new clear quartz substrate holder has been fabricated to allow seeds to be inverted in the deposition region. Seeds loaded in the retainer slots are suspended by the holder from the dopant introduction tubing during system loading. Inversion of substrates is an attempt to eliminate the triangulated surface of growths which is thought to be due to germanium particles which fall onto the surface of non-inverted seeds from the liner tube walls. Smooth layers are necessary for junctions, introduced by change of dopants, to be plane-parallel to the heterojunction interface.

A first run using the inverting seed holder quickly revealed the need for allignment modification of the dopant introduction tubing. This was done using the holder as a jig. The holder itself was a tight fit inside the liner tube causing repeated loss of the seed from its slots during loading. This was corrected by cutting away a thin section of the holder edge for a looser fit in the liner.

A technique has been developed for making mesa devices which permits the final step to be etching of the mesas with several mesas per 50 by 50 mil die. Previous devices consisted of a single large mesa per die and used contact alloying as the final step which always degraded the junction characteristics. Some difficulty was experienced in evaluating devices which had probe contacts with resistance of more than several hundred ohms. Contact is now alloyed into each mesa to overcome this.

In making mesa devices from the last five growths from the previous quarter, it was found that three growths were on high resistivity GaAs and therefore unsuitable for devices. A room temperature V-I plot of a device made from one of the other two growths has been made using a tungsten probe to pass current and a small alloyed contact as a potential probe. This plot is very encouraging in that it yielded a semi-log slope value of about $\eta = 1.10$ with the near linear region extending over two decades. This is much better than has been seen in earlier devices.

Two undoped runs were made using the new inverting seed holder. The first gave a somewhat irregular surface due to seed surface scratches

and polishing irregularities and the second showed a much smoother growth. Neither growth showed the triangular features which are characteristic of all previous growths with seeds face-up.

A series of p-doped runs were then made on some newly polished GaAs seeds using the inverting holder for comparison with runs made under nearly identical conditions in the previous face-up position. Growth thickness measurements show a growth rate in the inverted position of 0.7 times that of the face-up position, perhaps due to fewer surface sites from which growth may proceed. These growths have been diced and are now being made into van der Pauw samples for resistivity and mobility measurements and into mesa diodes.

6. HETEROJUNCTION SOLAR-CELL CALCULATIONS

The work in this area during the quarter has been formalized in terms of a paper to be submitted for publication. A copy of the paper with the above title accompanies the report.

In this paper solar-cell efficiencies are computed for feasible semiconductor heterojunction cells of ZnSe-GaAs, GaP-Si, ZnSe-Ge and GaAs-Ge. The analysis includes the loss in efficiency because of reflection, incomplete collection and internal series resistance. Optimum antireflection films are also calculated. The results are compared with the performances expected of Si solar cells and GaAs homojunction cells.

ZnSe-GaAs cells are shown to have the potential for exceeding the efficiency of both Si and GaAs cells, if interface recombination losses are small. The output voltage, voltage regulation and temperature performance should be superior to that of Si cells. The window effect in the heterojunction cell may also provide some inherent resistance to determination under radiation conditions.

7. PUBLICATIONS AND PAPERS PENDING

During this quarter a paper entitled "Autodoping Effects at the Interface of GaAs-Ge Heterojunctions" was presented at the AIME Conference on Defects in Electronic Materials for Devices, August 24-27, 1969 in Boston and accepted for publication in the March 1970 issue of the Transactions of the Metallurgical Society.

The paper "Performance Potential of High Frequency Heterojunction Transistors" was also accepted for publication in the IEEE Transactions on Electron Devices.

8. CONTRIBUTORS

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