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FINAL REPORT

Contract Number: NAS-5-21012

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SOLID STATE SCIENTIFIC INC.
MONTGOMERYVILLE, PENNA.

TABLE OF CONTENTS

INTRODUCTION

This final report covers the accomplishments made during the performance of the investigation into the combination of Complementary MOS and Complementary Bipolar circuits on a monolithic silicon chip. The results of this effort clearly demonstrates feasibility. The data shows that enhanced electrical performance can be expected with this new technology.

Study Program

The development program was devided into two work phases. Phase I consisted of the design and fabrication of a special engineering photo-resist mask set and an investigation of the wafer processing techniques required to determine initial feasibility. Phase II consisted of the fabrication of read/write buffer circuits using a second set of masks. This new technology has been named "Complementary-squared" or simply "C^2".

Complementary-squared (C^2) PROCESSING:

The diffusion development effort centered around the fabrication of a compatible high beta PNP. Both a "lateral" PNP and a "substrate" PNP approach were eliminated as candidates for C^2. The final structure used is the familiar vertical planar PNP. Additional investigations to determine the minimum fabrication steps and the processing reproducibility were also completed during Phase I. Figure #1 shows a cross-sectional view of the C^2 structure. The process requires only two additional steps versus that of C MOS only. The bipolar transistor process was specially designed to achieve the high emitter-base reverse breakdown voltages required for the read/write buffer circuits. Typical electrical characteristics are shown in Figure #2 for both the bipolar and C MOS devices.

PHASE I ELECTRICAL RESULTS:

The mask set of Phase I was designated SD 5610. The first group of wafers completely processed using these masks clearly demonstrated the feasibility of C^2. The dynamic performance showed that with a capacitive load of greater than 470 pico-farad, speeds in excess of one megahertz could be achieved. The static power consumption achieved with these circuits was typically much less than 100 nano-watts.

The successful completion of Phase I marked the beginning of an entirely new and exciting technology.

PHASE II

The circuits developed during phase II are shown in Figure #3 and #4. These devices are designated SD 5615-2 and SD 5615-3 respectively. A simple inverting output buffer was evaluated as shown in Figure #5 (SD 5615-1). Ten samples of each circuit have been furnished to NASA for further evaluation. The wiring diagrams are shown in Figure #6. Table I shows the data for the SD 5615-1 device.

BI-DIRECTIONAL DRIVER PERFORMANCE:

The data collected on circuits # SD 5615-2 and SD 5615-3 is represented in tables II and III. The high leakage currents associated with these devices are a result of the low BV_{CEO} of the PNP devices. The BV_{CEO} values were a result of extremely narrow base-widths for these devices. It has already been shown in Phase I that these high leakage levels are not inherent in the C^2 process, and identical dynamic performance for low leakage devices (nano-amperes) would be experienced.

C MOS versus C^2

The evaluation of the dynamic characteristics clearly shows the advantages of C^2 over that of C MOS.

C MOS versus C^2 (Cont'd)

This is represented graphically in Figure #7. Here, the rise and fall times are plotted versus load capacitance for the case of V_{dd} = +10Volts (SD 5615-2). The C MOS inverter used for this graph has w/l ratio equal to 100 for both the N and the P channel devices. It is apparent from this data that a ten to one speed improvement can be realized by using the C^2 technology.

BUFFER CIRCUIT EVALUATION

The two bi-directional driver circuits were compared dynamically in both the input and output modes of operation. In the output or driving mode the SD 5615-3 circuit exhibits extremely long fall times. This is due to the fact that the bases of the bipolar devices are not turned off thru MOS devices. Rather, the bipolar device that should be off (depending upon the input state), is left "floating" such that current can continue to flow until the device capacitances are discharged. The fact that only the fall time is affected indicates that the NPN charge storage time is much greater than that of the PNP. The SD 5615-2 circuit does not suffer from this problem due to the "push-pull" effect achieved by driving the bipolar bases from a common C MOS inverter. In the input or data acceptance mode the SD 5615-2 circuit has an undesireable property. This circuit loads down the output as expected due to the fact that the bipolar devices are not turned off as is the case with the SD 5615-3 device. The loading effects of both circuits were evaluated by using a C MOS inverter to drive into the bipolar output and then measuring transition times. These times were in turn translated into effective capacitances. The SD 5615-2 represented a load from 200 to 1000 pico-farads and the SD 5615-3 represented essentially zero load to the C MOS inverter.

BUFFER CIRCUIT EVALUATION - Cont'd:

The circuit comparisons show that an optimum design can be achieved by combining the best aspects of these two circuits. This optimum design is shown in Figure #8, and it will result in the fastest switching response and minimum output loading.

LOW VOLTAGE OPERATION

Circuit #SD 5615-2 was evaluated at a supply voltage equal to +5 volts. The results of these tests are extremely significant in that no degradation of dynamic performance was observed under high loading conditions in terms rise and fall times. Figure #9 shows a comparison of C MOS and C^2 in terms of switching response versus supply voltage.

The fact that the C^2 fall time increases at higher supply voltage indicates that the effective series collector resistance increases due to current saturation. However, the supply range from +5 to +10 volts is of prime importance. In this voltage range the speed advantage of C^2 versus C MOS varies from a factor of ten (at 10 volts) to a factor of approximately twenty-five (at 5 volts).

The fact that the switching speed of C MOS at low voltage is quite poor, has inhibited its usefulness as an interface with standard TTL logic. The new C^2 technology offers the user direct TTL interface at high speeds.

C^2 GEOMETRY CONSIDERATIONS

Three MOS inverter geometries (w/l ratios) and two bipolar geometries were evaluated in terms of dynamic performance.

The SD 5610 device contained three C MOS inverter sizes, which were; W/L = 100, W/L = 50, and W/L = 25. These devices were evaluated in terms of driving capability

for the bipolar outputs. The results of this investigation is shown in Figure 10. The plotted parameters are propagation delay plus transition time versus inverter size for both logic states. The conditions were V_{DD} = +10 volts and C_L = 120 pico-farads.

The results show that the larger inverter sizes increase the maximum operating frequency as expected. Thus, the minimum inverter size required of any new circuit designs will be a function of the requirements in terms of dynamic performance.

The bipolar devices were evaluated similarly using a constant inverter size of W/L = 100. The two bipolar sizes (total area for both the NPN and the PNP) were 212 mil^2 and 408 mil^2. The results of this investigation is plotted (Figure #11) in terms of propagation delay plus transition time versus capacitive load for both buffer sizes, (V_{DD} = +10 volts). The results show that there is very little difference in terms of maximum operating frequency. This suggests that perhaps even smaller bipolar sizes could be used in future designs.

CHIP AREA TRADE-OFFS

This study program shows that both a speed improvement and a chip size improvement can be achieved with the new C^2 technology.

The area consumed by a typical output C MOS inverter (W/L = 100) is 176 mil^2. The bipolar output buffer of the SD 5610 device is only 212 mil^2. The increase in area of the bipolar devices is very minimal considering the tremendous gain in dynamic response. This very small increase in area makes C^2 very attractive for use as output buffers and also internal buffers such as clock line drivers.

CONCLUSION

The successful completion of this study program has lead to the following conclusions:

1) Both high speed and low leakage can be obtained using C^2.

CONCLUSION - Cont'd

2) Only two additional process steps are necessary for the fabrication of C^2 versus C MOS alone.

3) Both types of bi-directional buffer circuits functioned electrically and pointed the way to a newer optimum design.

4) The SD 5615-3 represented nearly zero load in the input mode of operation.

5) C^2 offers a dynamic performance improvement from 10 to 25 times that of C MOS.

6) The observed high speed performance at +5 volts is compatible with conventional TTL circuits.

7) Chip area is not appreciatably increased by using C^2.

SCL 5615-1

TABLE #1

STATIC CHARACTERISTICS: V_{DD} = 10.0V, V_1 = 10.0V, V_0 = 0.0V

Units Serial #	I_{DD} @ V_1 μA	I_{DD} @ V_0 μA	V_{OH} @ V_0 Volts	V_{OL} @ V_1 Volts
1	0.0005	250	9.41	0.00
2	0.11	0.003	9.57	0.00
3	3.0	0.09	9.58	0.01
4	48	0.45	9.58	0.46
5	6.4	4.0	9.54	0.01
6	4.6	4.6	9.57	0.01
7	60	0.0003	9.96	0.55
8	0.0005	0.0005	9.56	0.00
9	34	47	9.58	0.01
10	2.1	0.04	9.57	0.01

DYNAMIC CHARACTERISTICS: V_{DD} = 10.0V, V_1 = 0.0 V, C_L = 92 pf

Units Serial #	T_r n Sec	T_f n Sec	T_{p0} n Sec	T_{p1} n Sec
1	54	188	44	56
2	60	218	46	60
3	60	204	53	62
4	52	272	37	58
5	66	252	69	66
6	60	182	55	62
7	64	196	48	64
8	60	146	38	62
9	58	358	94	60
10	63	218	47	62

SCL 5615-2

TABLE II

STATIC CHARACTERISTICS: V_{DD} = 10.0 V, V_1 = 10.0V, V_0 = 0.00 V

INPUT CONDITIONS	IDD V_0 V_0	V_1 V_0	V_0 V_1	V_1 V_1	V_{OH} V_1 V_0	V_{OL} V_0 V_0	Data Write
Units	μA	μA	μA	μA	Volts	Volts	
Serial #							
1	6.7	2450	0.0008	0.003	8.53	0.01	
2	0.025	310	0.025	310	9.44	0.00	
3	1650	950	950	1000	9.58	0.07	
4	1300	1700	0.0003	0.0003	9.34	0.18	
5	0.60	730	0.0005	0.0005	9.38	0.00	
6	470	950	1100	0.0012	9.32	0.01	
7	510	2000	0.0002	0.0002	9.35	0.00	
8	0.0005	670	21	0.0011	9.37	0.00	
9	1.0	150	0.19	0.20	9.44	0.40	
10	30	270	34	34	9.99	0.50	

DYNAMIC CHARACTERISTICS: @ V_{DD} = 10.0 V

CONDITIONS	T_r ϕ V_0	T_f ϕ V_0	T_{p0} ϕ V_0	T_{p1} ϕ V_0	Ce0 V_0 V_1 V_{OL}	Ce1 V_0 V_1 V_{OH}	Data Write Output
	C_L=1.4pf <———			———> C_L=1.4pf			
Units	n Sec	n Sec	n Sec	n Sec	pF	pF	
Serial #							
1	30	48	46	35	150	870	
2	29	56	50	34	380	740	
3	36	38	48	35	290	700	
4	30	48	54	38	350	740	
5	29	48	48	34	390	800	
6	33	40	44	35	200	870	
7	30	62	54	34	280	400	
8	33	46	52	46	360	860	
9	29	46	50	35	470	770	
10	35	42	50	45	260	550	
CONDITIONS	25pf	25pf	25pf	25pf			C_L
Units	n Sec	n Sec	n Sec	n Sec			
Serial #							
1	36	50	50	44			
2	36	80	56	43			
3	43	42	57	46			
4	37	54	58	47			
5	34	58	52	43			
6	40	46	48	45			
7	36	110	58	43			
8	39	52	56	56			
9	34	60	56	44			
10	45	70	58	56			

Continued.....

DYNAMIC CHARACTERISTICS: Cont'd

CONDITIONS	92pf	92pf	92pf	92pf	C_L
Serial #					
1	47	90	60	59	
2	52	140	72	59	
3	61	92	62	65	
4	48	100	68	62	
5	44	112	66	57	
6	52	78	56	62	
7	47	220	84	57	
8	55	94	68	72	
9	47	126	72	60	
10	72	156	78	35	

CONDITIONS	300pf	300pf	300pf	300pf	C_L
Serial #					
1	91	228	108	96	
2	88	250	154	92	
3	107	240	127	103	
4	87	240	127	95	
5	80	296	142	89	
6	93	200	96	97	
7	83	600	216	89	
8	99	235	128	113	
9	85	350	160	93	
10	132	430	192	122	

SCL 5615-3

TABLE III

STATIC CHARACTERISTICS: V_{DD} = 10.0V, V_1 = 10.0V, V_0 = 0.00 V

		I_{DD}				V_{OH}	V_{OL}
INPUT	V_0	V_1	V_0	V_1	V_1	V_0	Data
CONDITIONS	V_0	V_0	V_1	V1	V_0	V_0	Write
Units	μA	μA	μA	μA	Volts	Volts	
Serial #							
1	0.0017	3500	500	500	9.30	0.00	
2	0.020	900	200	200	9.36	0.00	
3	100	600	100	100	9.37	0.00	
4	0.001	2200	0.001	0.001	9.31	0.00	
5	0.0006	200	0.0055	0.0055	9.42	0.00	
6	6.0	650	6.0	6.0	9.40	0.00	
7	15	3500	600	600	9.33	0.00	
8	0.0011	4000	0.001	0.001	9.26	0.00	
9	4.0	300	110	110	9.40	0.00	
10	110	110	110	110	9.58	0.00	

DYNAMIC CHARACTERISTICS: @ V_{DD} = 10.0V

	T_r	T_f	T_{p0}	T_{p1}	C_{e0}	C_{e1}	
CONDITIONS	O	O	O	O	V_0	V_o	Data
	V_o	V_o	V_o	V_o	V_1	V_1	Write
C_L	1.4pf	1.4pf	1.4pf	1.4pf	V_{OL}	V_{OH}	Output
Units	n Sec	n Sec	n Sec	n Sec	pf	pf	
Serial#							
1	24	2000	630	34	O	O	
2	22	2400	720	32			
3	30	1100	80	34			
4	30	1200	90	34			
5	22	1500	70	34			
6	20	2600	590	28			
7	20	2600	870	30			
8	44	1300	270	36			
9	26	1800	350	34			
10	20	1600	70	30			

CONDITIONS	25pf	25pf	25pf	25pf	C_L
Units	n Sec	n Sec	n Sec	n Sec	
Serial #					
1	28	2000	660	40	
2	24	2300	670	36	
3	32	1100	100	38	
4	32	1200	100	38	
5	24	1300	70	38	
6	22	2500	550	34	
7	22	2700	850	34	

Continued

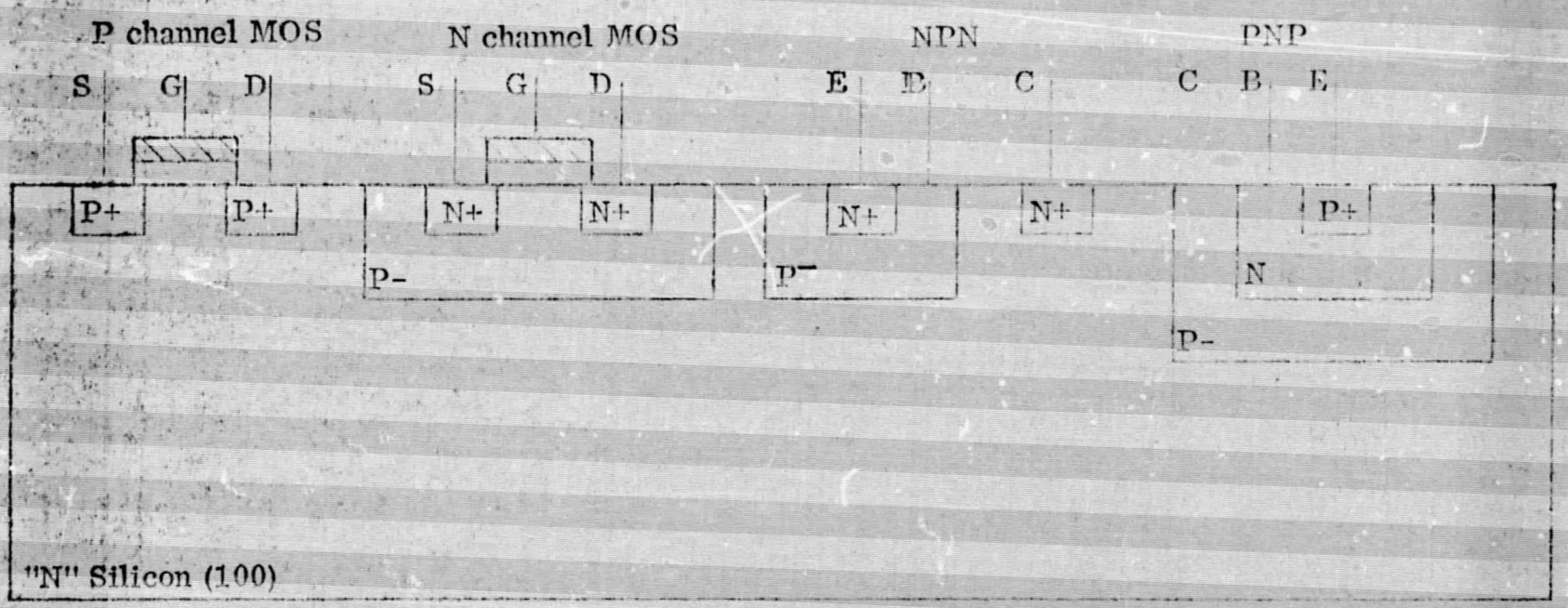
TABLE III Cont'd

CONDITIONS Cont'd	25pf	25pf	25pf	25pf
Units	n Sec	n Sec	n Sec	n Sec
Serial #				
8	38	1300	260	41
9	30	1800	340	40
10	22	1600	90	36

CONDITIONS	92pf	92pf	92pf	92pf
Serial #				
1	38	2000	1000	48
2	32	2300	590	45
3	40	1100	130	48
4	44	1200	130	48
5	34	1300	100	48
6	32	2500	410	42
7	30	2700	750	42
8	48	1300	250	52
9	40	1800	290	50
10	32	1700	130	44

CONDITIONS	300pf	300pf	300pf	300pf
Serial #				
1	60	2100	240	72
2	56	2500	230	66
3	66	1200	210	70
4	68	1300	230	72
5	58	1700	200	70
6	54	2800	480	62
7	50	3200	770	62
8	72	1400	300	76
9	66	1900	310	74
10	56	2100	290	66

REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED



A cross-section view of one fabrication approach of complementary MOS and complementary bipolar on the same substrate.

(Figure #1)

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES	DRAWN	DATE	SOLID STATE SCIENTIFIC CORP. MONTGOMERYVILLE, PENNSYLVANIA 18936
	CHECKED		
MATERIAL	APPROVED		C^2 - CROSS SECTION
	APPROVED		SIZE A / CODE IDENT NO.
	APPROVED		SCALE / WEIGHT / SHEET

DIETZGEN Phila. 198M 10354

COMPLEMENTARY-SQUARED

ELECTRICAL CHARACTERISTICS

BIPOLAR devices

DEVICE	BV_{CBO} @ 10 μA	BV_{EBO} @ 10 μA	BV_{CES} @ 10 μA	V_{CE} I_C = 1 mA I_B = 0.1 mA	BETA I_C = 10 mA
PNP	60V	30V	60V	0.5V	150
NPN	80V	50V	80V	0.15V	50

MOS devices

DEVICE	V_T @ 10 μA	BV_{DSS} @ 10 μA	I_{DSS} @ 10 V
P Channel	2.3V	50V	1 nA
N Channel	1.9V	30V	1 nA

FIGURE #2

REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED

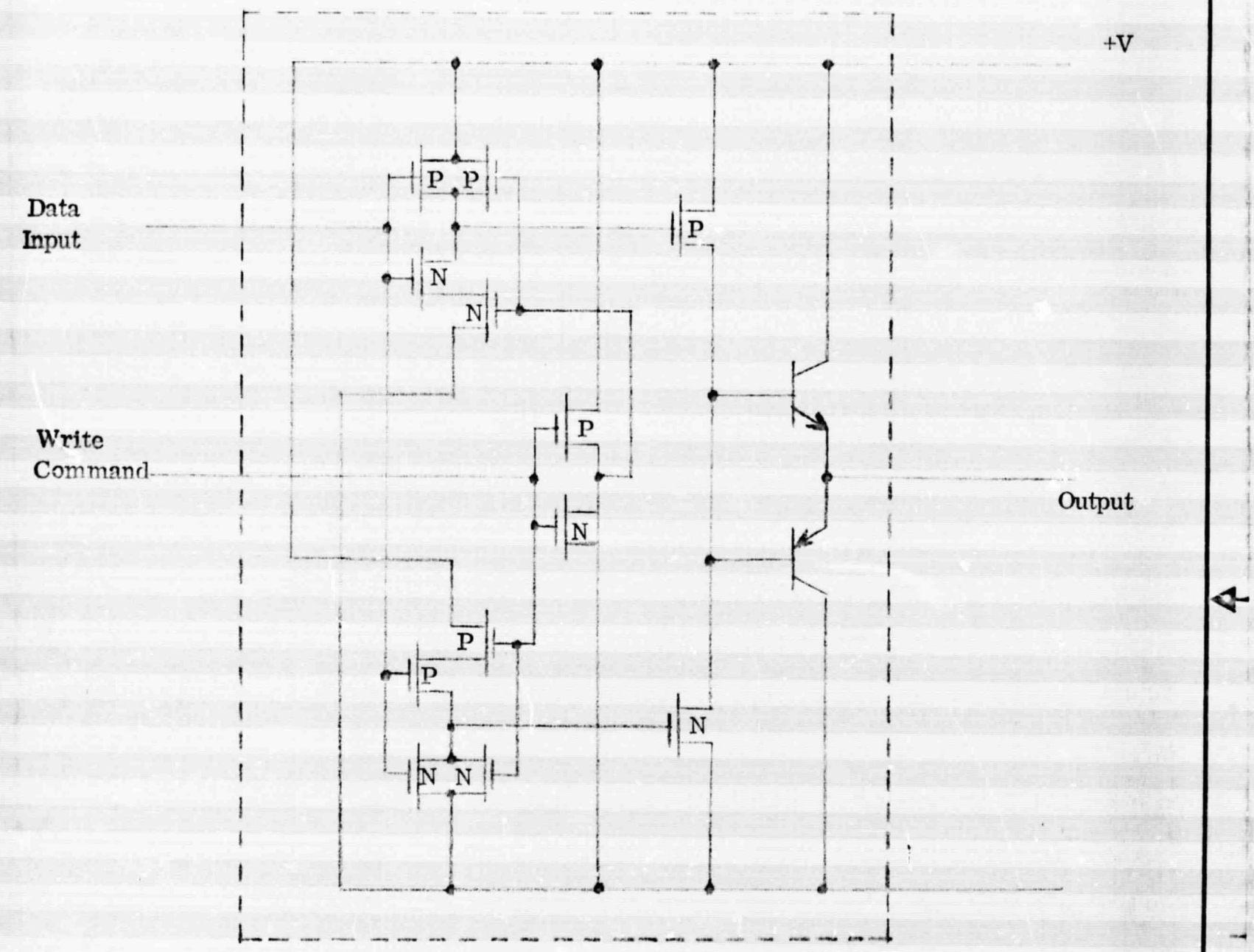
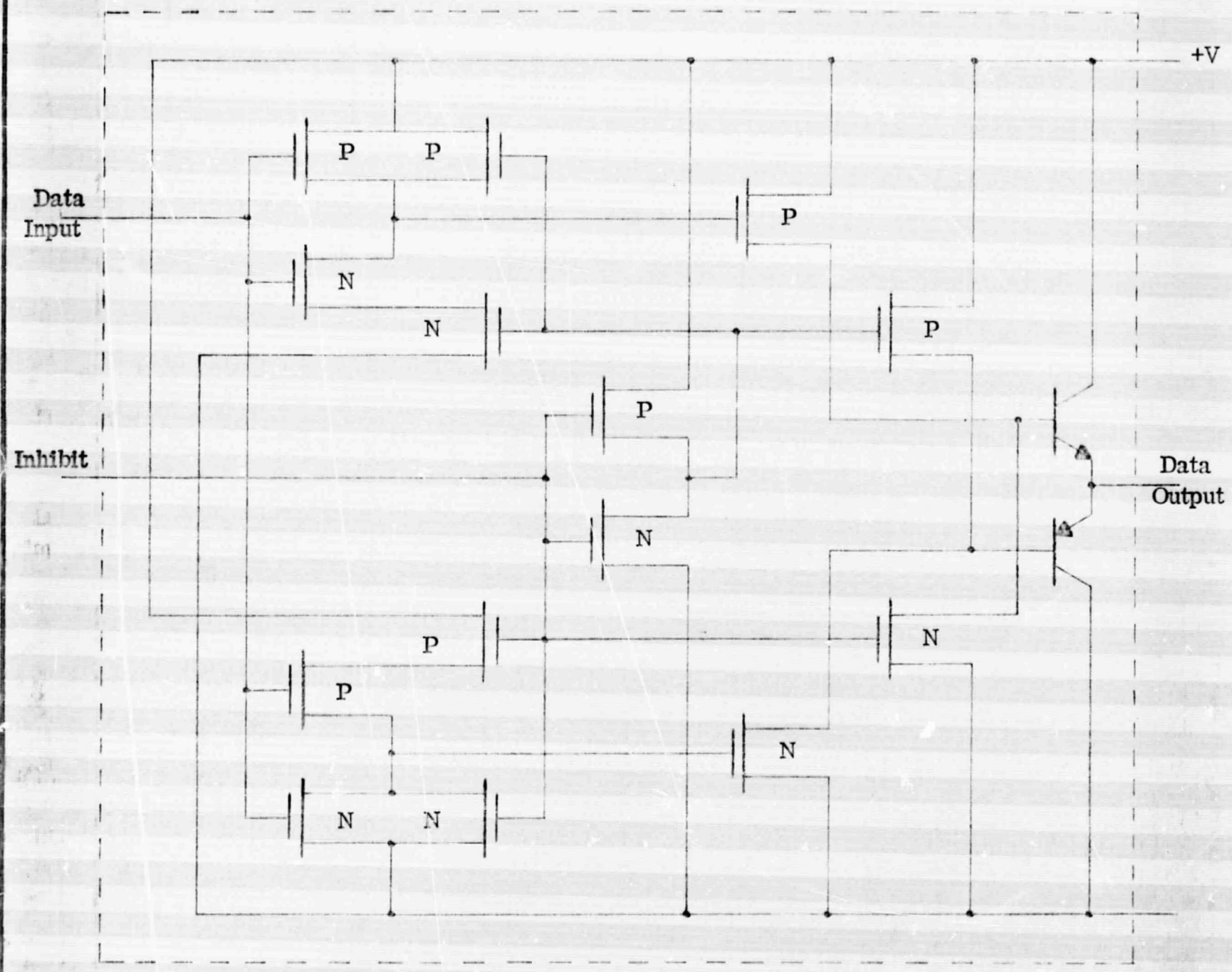


Figure #3

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES	DRAWN	DATE	SOLID STATE SCIENTIFIC CORP. MONTGOMERYVILLE, PENNSYLVANIA 18936
	CHECKED		
MATERIAL	APPROVED		BI-DIRECTIONAL DRIVER SD 5615 - 2
	APPROVED		SIZE A / CODE IDENT NO.
	APPROVED		

REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED



NOTE: The output is open circuited when Inhibit is high. (Figure #4)

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES	DRAWN	DATE	SOLID STATE SCIENTIFIC CORP. MONTGOMERYVILLE, PENNSYLVANIA 18936
	CHECKED		
MATERIAL	APPROVED		BI-DIRECTIONAL DRIVER SD 5615 - 3
	APPROVED		SIZE A / CODE IDENT NO.

REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED

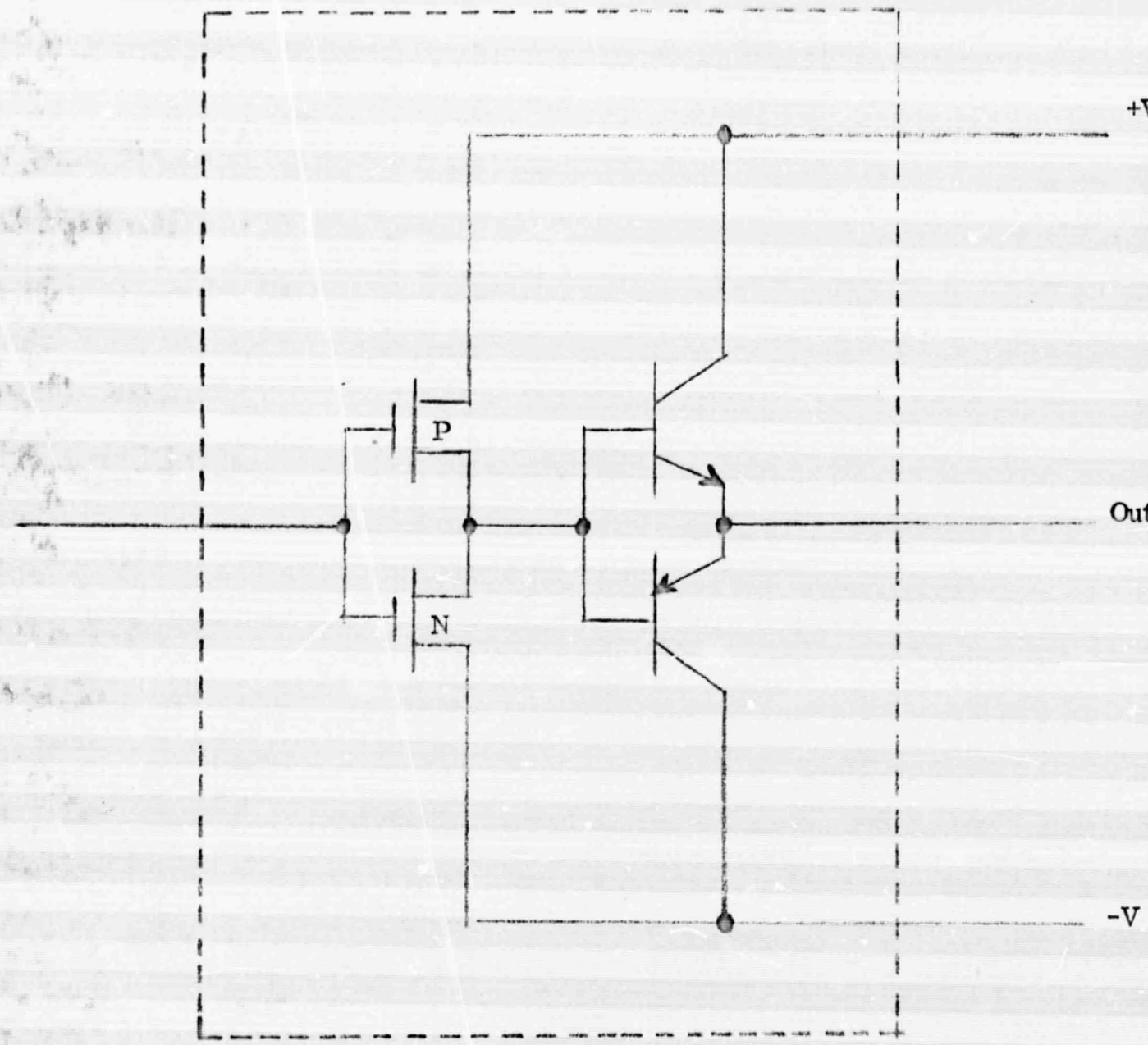
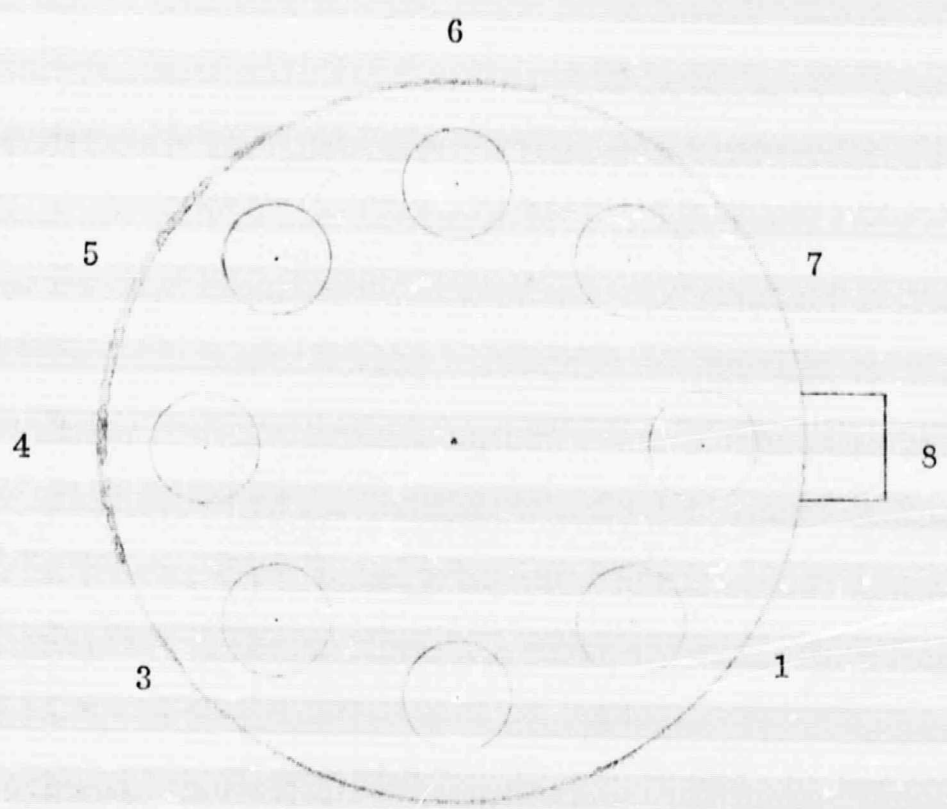


Figure #5

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES	DRAWN [illegible]	DATE 10/24/69	SOLID STATE SCIENTIFIC CORP. MONTGOMERYVILLE, PENNSYLVANIA 18936
MATERIAL	CHECKED [illegible]	[illegible]	INVERTING BUFFER SD 5615-1
	APPROVED [illegible]	[illegible]	
	APPROVED		SIZE A / CODE IDENT NO.
	APPROVED		SCALE / WEIGHT / SHEET



BOTTOM VIEW

PIN#	SCL 5615-1	SCL 5615-2	SCL 5615-3
1	INPUT	+V	+V
2	+V	---------	---------
3	-------	OUTPUT	DATA
4	OUTPUT	---------	---------
5	-------	WRITE	WRITE
6	-------	DATA	-V
7	-V	---------	---------
8	-------	-V	OUTPUT

FIGURE #6

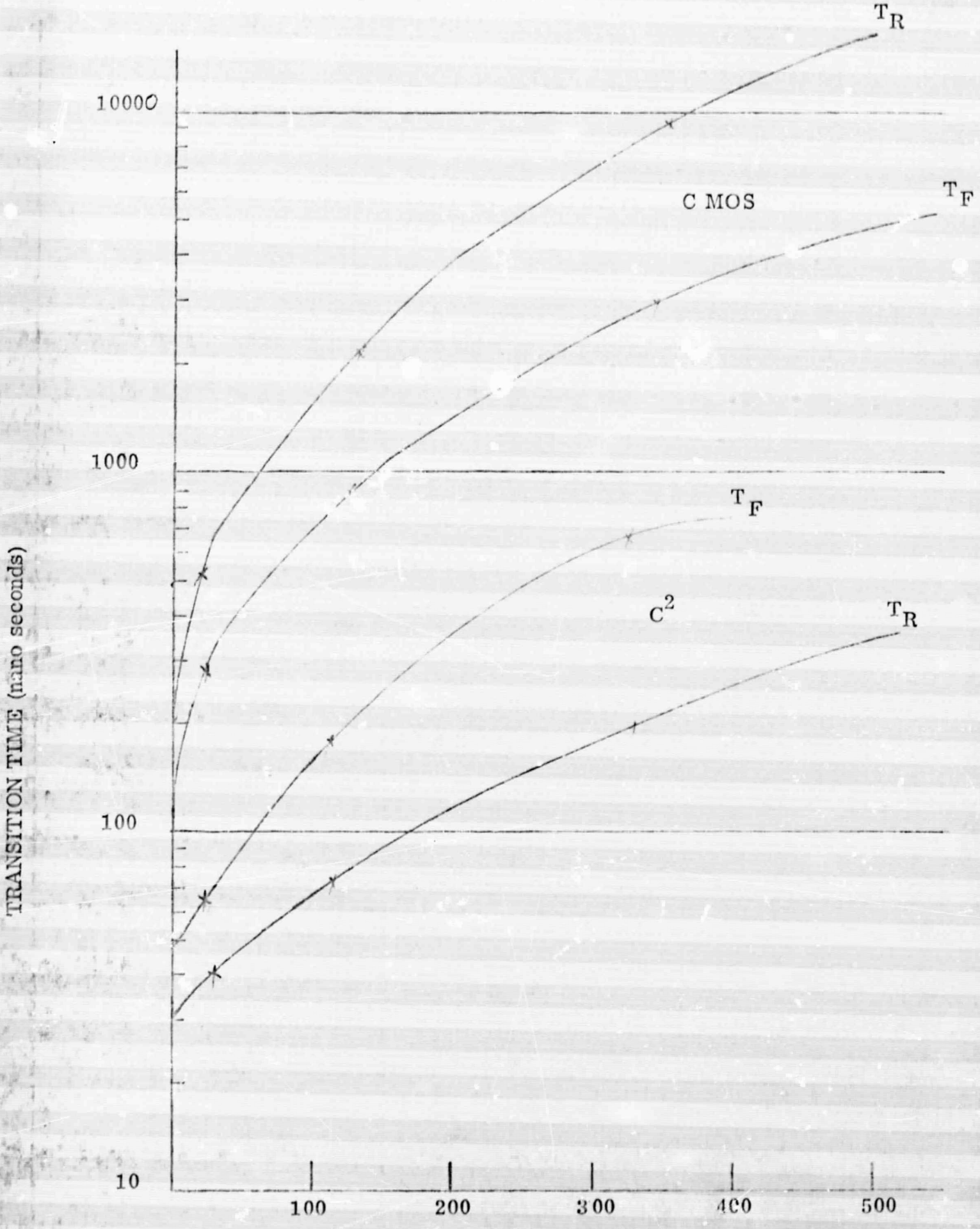


FIGURE #7

REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED

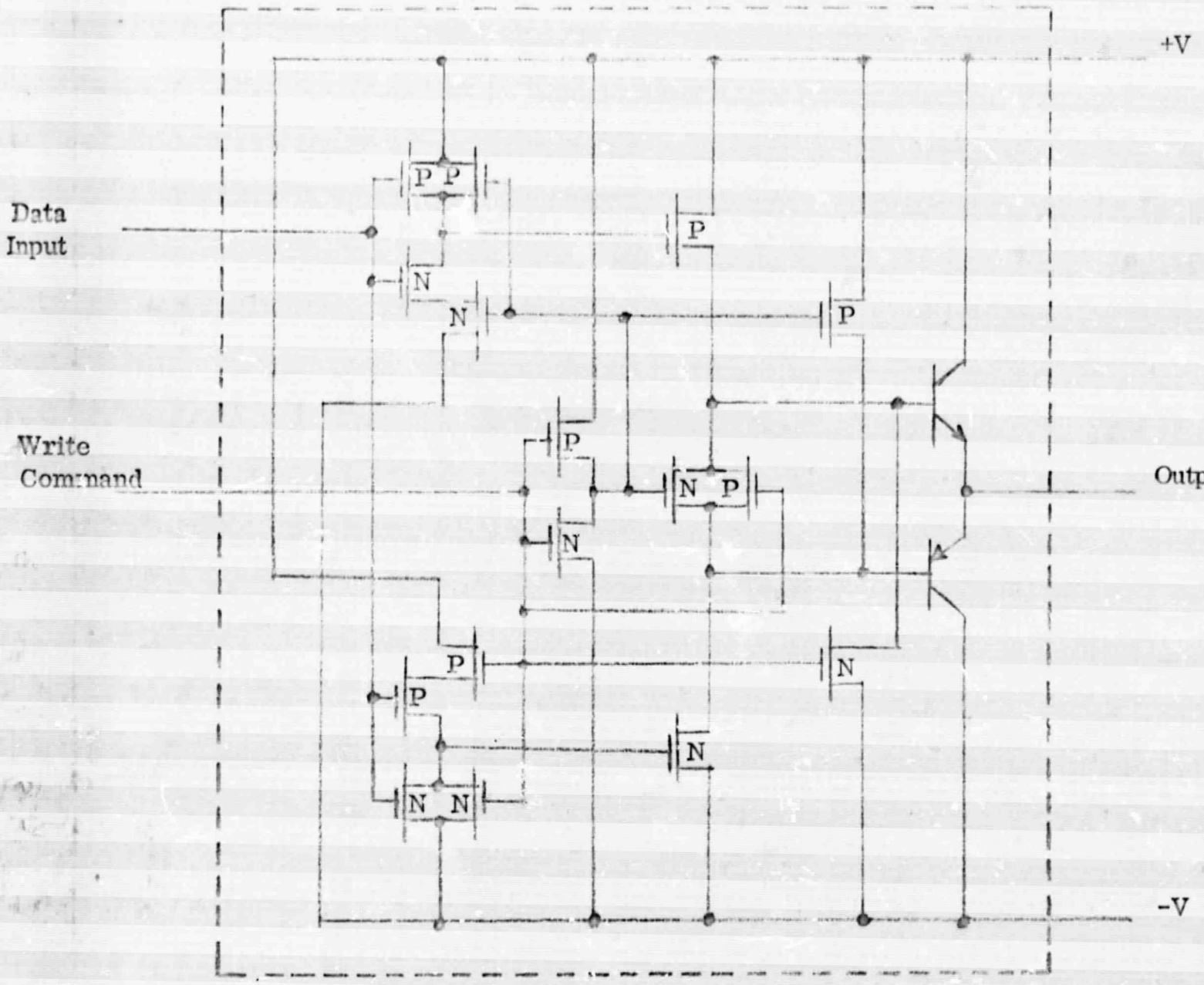


FIGURE #8

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES	DRAWN	DATE	SOLID STATE SCIENTIFIC CORP. MONTGOMERYVILLE, PENNSYLVANIA 18936
	CHECKED		IMPROVED READ/WRITE OUTPUT BUFFER WITH PULL-UPS
MATERIAL	APPROVED		
	APPROVED		SIZE A / CODE IDENT NO. / SCALE / WEIGHT / SHEET

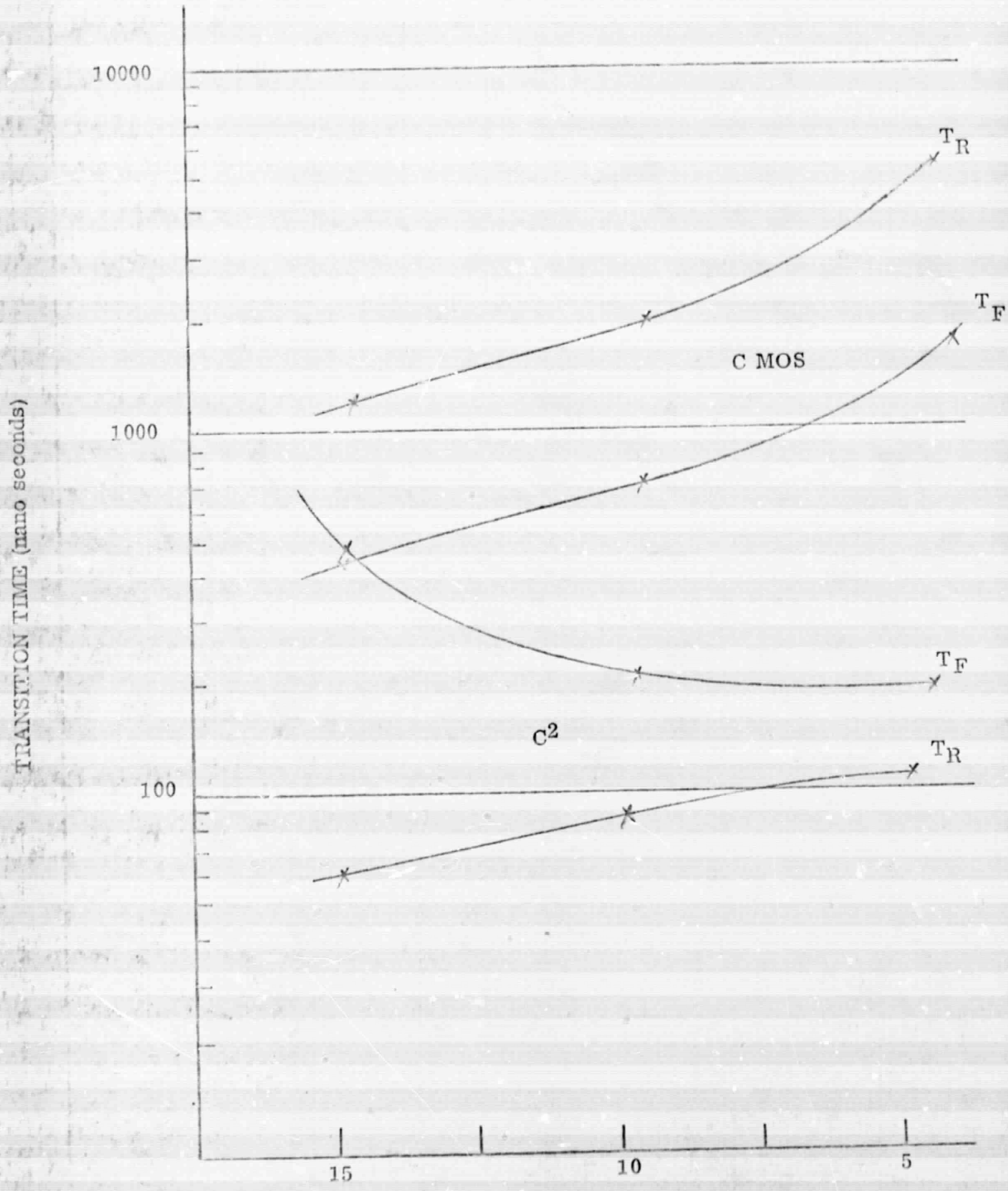

10000
1000
100
TRANSITION TIME (nano seconds)
T_R
T_F
C MOS
T_F
C^2
T_R
15
10
5
SUPPLY VOLTAGE

FIGURE #9

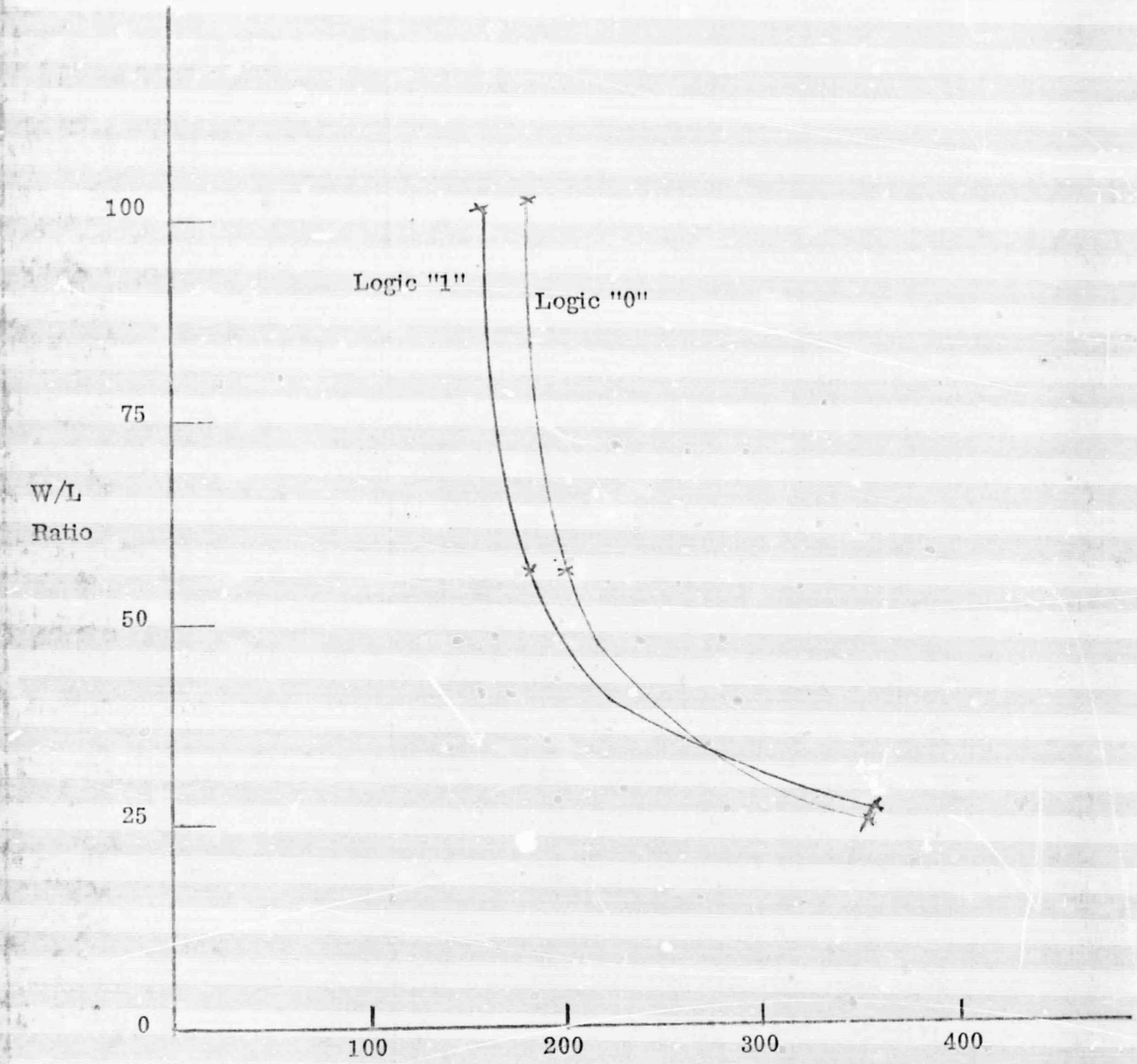

100
75
W/L
Ratio
50
25
0
Logic "1"
Logic "0"
100
200
300
400
SWITCHING TIME (nano seconds)

FIGURE # 10

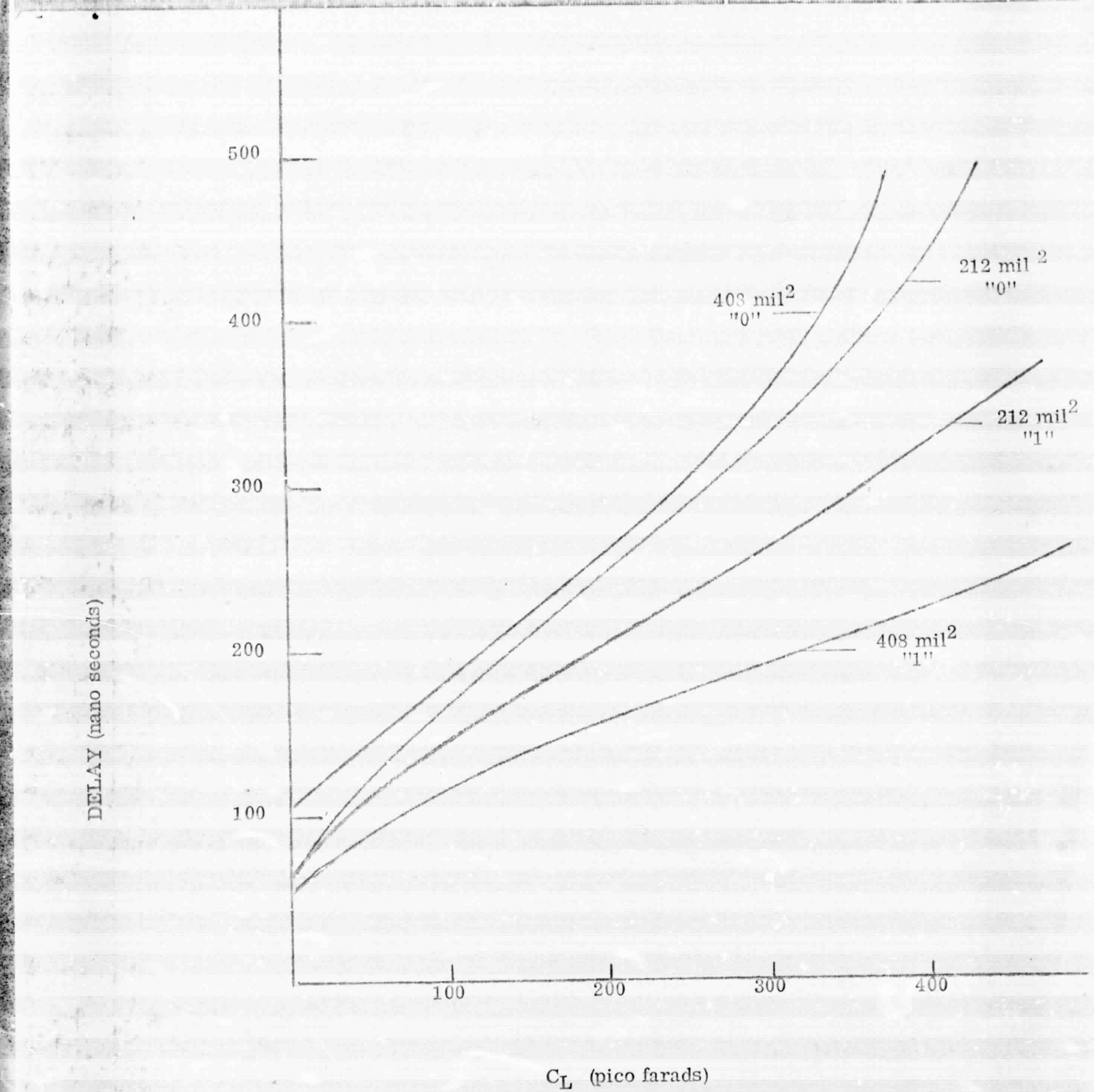
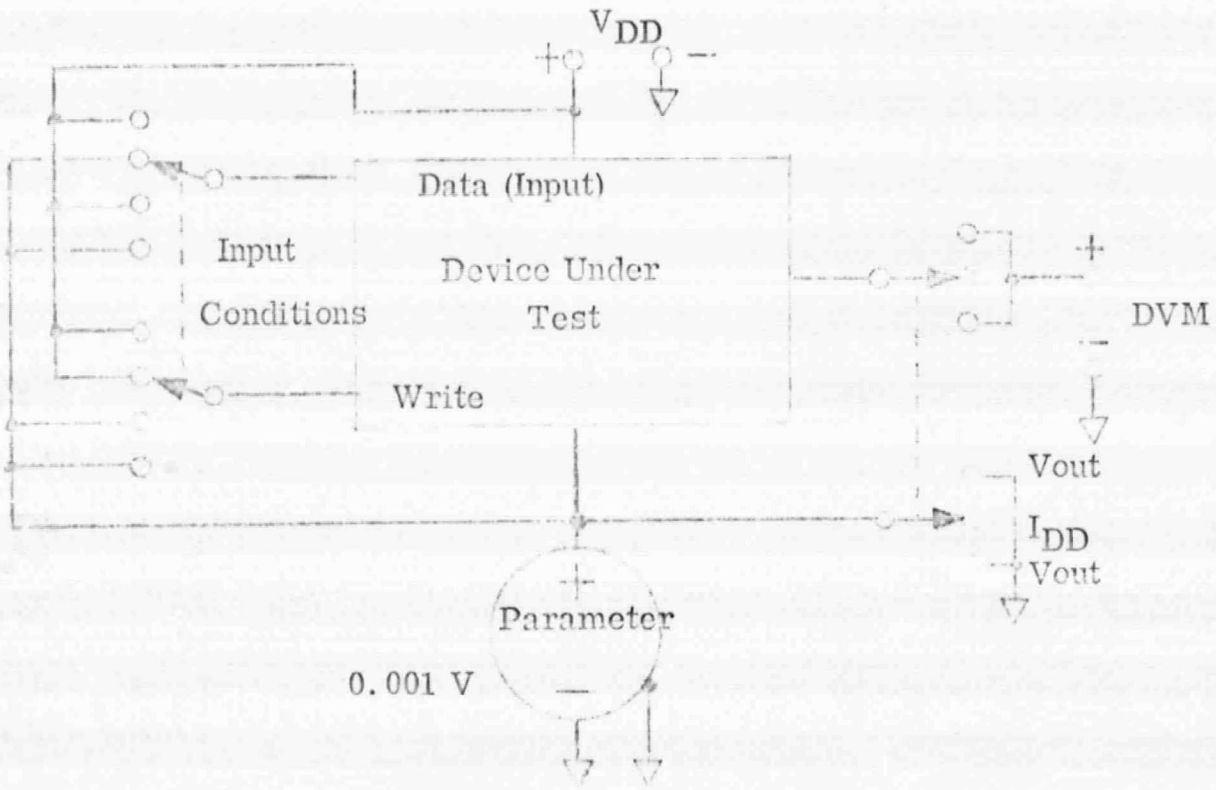
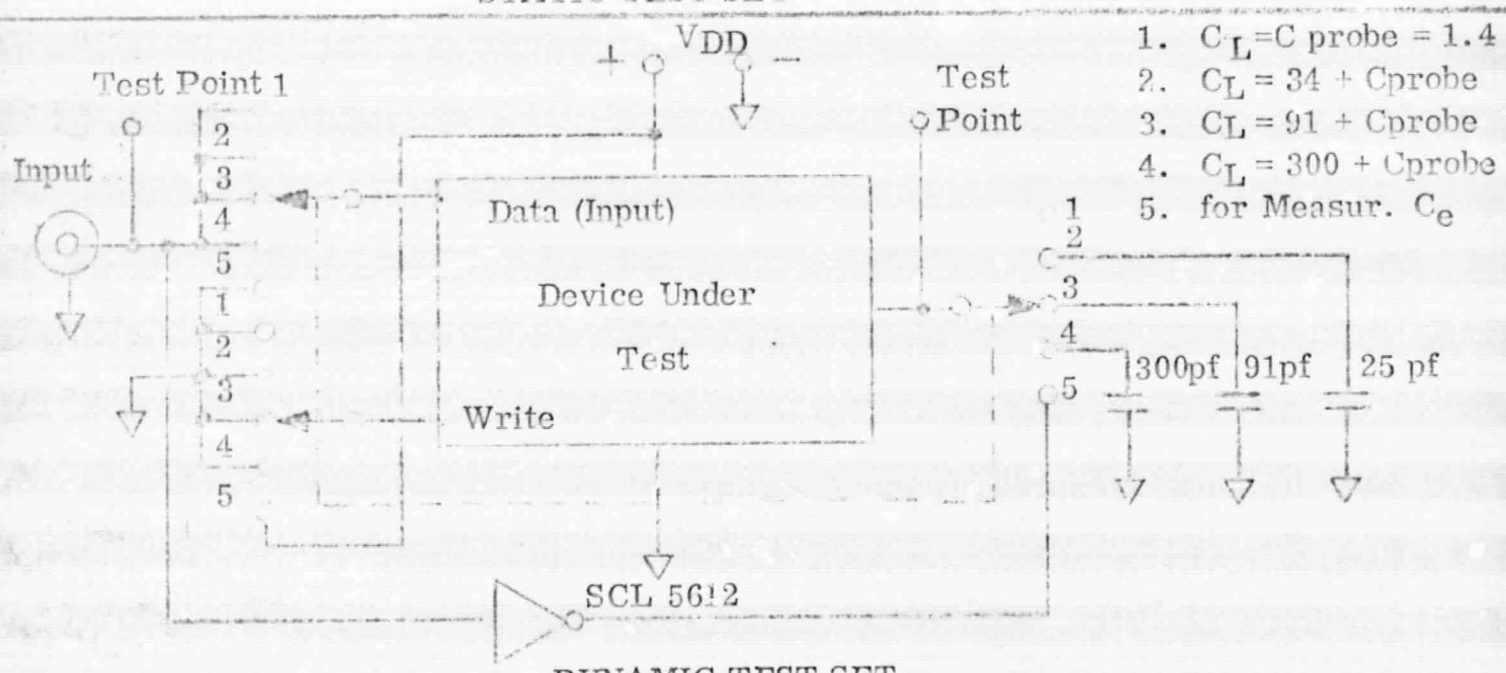

DELAY (nano seconds)
500
400
300
200
100
100
200
300
400
408 mil2
"0"
212 mil 2
"0"
212 mil2
"1"
408 mil2
"1"
CL (pico farads)

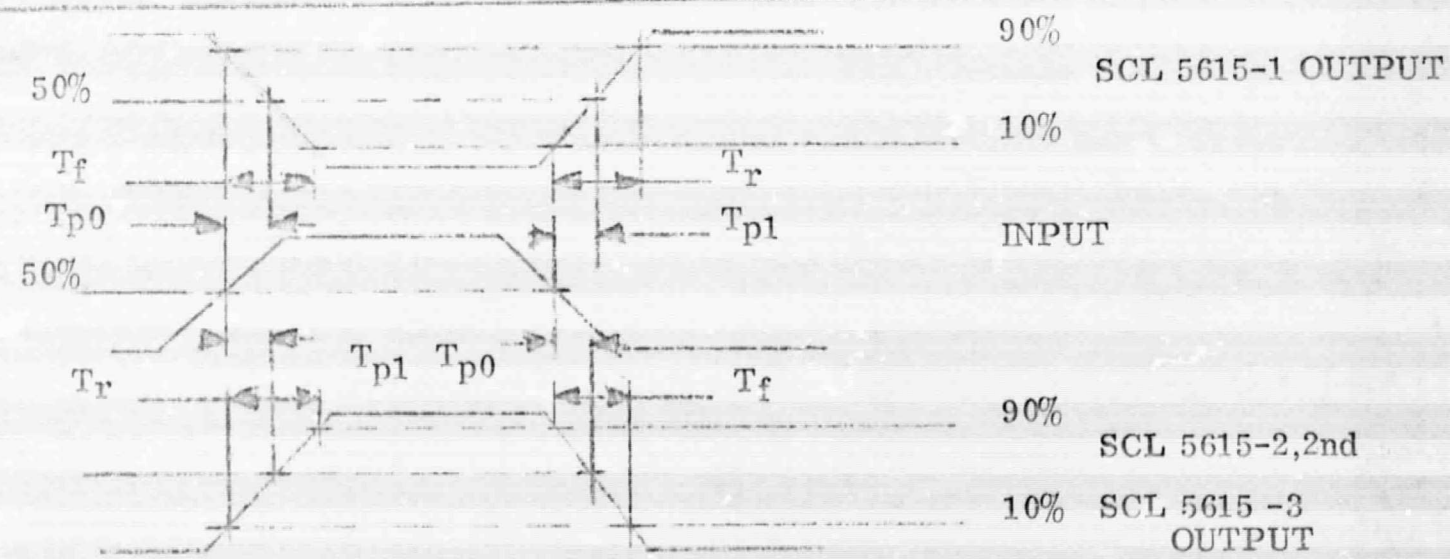
FIGURE # 11



STATIC TEST SET



DYNAMIC TEST SET



TYPICAL DYNAMIC WAVEFORMS

FIGURE #12