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CR 86291

INVESTIGATION OF REFRACTORY DIELECTRIC FOR INTEGRATED CIRCUITS

By V.Y. Doo, P.J. Tsang, and P.C. Li

February 1969

Prepared under Contract No. NAS 12-667 by

INTERNATIONAL BUSINESS MACHINES CORPORATION

Hopewell Junction, New York 12533

ELECTRONICS RESEARCH CENTER

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1.0 INTRODUCTION

This is the third quarterly report on contract No. NAS 12-667, describing the work performed from December 1, 1968 to February 28, 1969. The objective of this contract is to conduct research and development on refractory dielectrics leading to integrated circuits application. Progress in this quarter included (1) measurements of V_{FB} and N_{FB} of Na contaminated MAOS samples, (2) continuous study of the effect of inert gases on film growth and C-V characteristics, (3) study of the effect of post deposition heat treatment and other pertinent factors on N_{FB} and V_{FB} of MAS and MAOS samples, and (4) preparation of integrated circuits using newly developed composite films of Al_2O_3-SiO_2 as the gate insulator for test IGFET devices.

2.0 V_{FB} and N_{FB} OF Na CONTAMINATED MAOS SAMPLES

Two samples consisting of composite films of Al_2O_3-SiO_2 were prepared. One sample designated as 12 Al has 4500 Å thermal SiO_2 and 1000 Å Al_2O_3 and the other, 7 Al has 800 Å thermal SiO_2 and 1200 Å Al_2O_3. These samples were then deposited by NaCl vapor so that the surface concentration of Na contamination was approximately 10^{13} atoms/cm^2. This was done by first evaporating 0.5 ml of 0.0005 mole NaCl solution in a tungsten boat and then vacuum vaporizing the salt onto the films. Finally the MAOS samples were prepared using Al metallurgy as done by standard methods. The V_{FB} and N_{FB} of these samples were calculated from the measured C-V curves under temperature bias treatments. Results were presented in Table I. Data indicated that these Na contaminated samples tend to increase the negative V_{FB}, independent of the film thickness. As compared with the data from non-contaminated samples prepared in runs 10 Al and 5 Al-2 having comparable film thickness as 12 Al and 7 Al, respectively, the increment of negative V_{FB} of these Na contaminated samples is approximately 3 volts. Consequently there is an increase of negative surface charge at the silicon surface of about 6×10^{11} charge/cm^2. It is further noticed that both V_{FB} and N_{FB} of these Na contaminated samples did not show any substantial change even

TABLE I. V_{FB} and N_{FB} of Na-Contaminated Samples.

A. Sample 12 Al, 1000 Å Al_2O_3 + 4500 Å Thermal SiO_2

No. of Test Sequence	Temp. - Bias Test (in dry N_2) Temp./Time	Bias	V_{FB} (V)	N_{FB} (charge/cm^2)	ΔV_{FB} (V)	ΔN_{FB} (charge/cm^2)
1	As Received and Na Contaminated		-6.5	-3.14×10^{11}	-3.2*	-4.4×10^{10} *
2	200°C/30 min.	0	-6.0	-2.74×10^{11}	+0.5**	$+4.0 \times 10^{10}$ **
	200°C/30 min.	+5	-7.8	-3.56×10^{11}	-1.8	-8.2×10^{10}
3	200°C/30 min.	0	-6.0	-2.99×10^{11}	-0.0**	-2.5×10^{10}**
	200°C/30 min.	+30	-9.0	-4.49×10^{11}	-3.0	-15.0×10^{10}
4	200°C/30 min.	0	-6.0	-2.79×10^{11}	-0.0**	-0.5×10^{10}**
	200°C/30 min.	-5	-6.0	-2.79×10^{11}	-0.0	-0.5×10^{10}
5	200°C/30 min.	0	-6.0	-2.79×10^{11}	-0.0**	-0.5×10^{10}**
	200°C/30 min.	-30	-6.0	-2.79×10^{11}	-0.0	-0.5×10^{10}
6	200°C/150 min.	0	-7.8	-3.56×10^{11}	-1.8**	-8.2×10^{10} **
	200°C/150 min.	+30.0	-7.8	-3.56×10^{11}	0.0	0.0
7	200°C/150 min.	0	-7.8	-3.56×10^{11}	0.0**	0.0**
	200°C/150 min.	-30.0	-6.0	-2.79×10^{11}	+1.8	$+8.2 \times 10^{10}$

*Compared with the V_{FB} and N_{FB} of Non-Na contaminated Sample 10 Al which has V_{FB} and N_{FB} of -3.3V and -2.7×10^{11} charge/cm^2, respectively.

**Compared with the corresponding values of those of as received Na-contaminated sample.

B. Sample 7 Al 1200 Å Al_2O_3 + 800 Å Thermal SiO_2

1	As received No T-B Test		-4.2	-7.03×10^{11}	-3.16*	-5.03×10^{11}*
2	200°C/30 min.	No	-4.0	-6.34×10^{11}	+0.2**	$+6.9 \times 10^{10}$ **
	200°C/30 min.	+5	-4.2	-6.8×10^{11}	-0.2	-5.4×10^{10}
3	200°C/30 min.	No	-3.7	-6.06×10^{11}	+0.5**	$+9.7 \times 10^{10}$
	200°C/30 min.	+30	-5.1	-8.37×10^{11}	-1.4	-2.3×10^{11}
4	200°C/150 min.	No	-4.2	-7.00×10^{11}	0.0**	$+3.0 \times 10^{9}$ **
	200°C/150 min.	+30	-5.5	-8.79×10^{11}	-1.3	-1.79×10^{11}

*Compared with the V_{FB} and N_{FB} of Non-Na contaminated Sample 5 Al-2, which has V_{FB} and N_{FB} of -1.04 V and 2.0×10^{11}, respectively.

**Compared with the corresponding values of those of as received Na-contaminated sample.

after prolonged heat treatments, indicative of excellent film stability. After these samples were under temperature bias treatments (applied voltages ranging from $\pm$ 5 to $\pm$ 30), the thin composite film (7 Al) was found to have a maximum V_{FB} shift of - 1.4V and the thick composite film (12 Al) - 3.0V. The change of surface charge density, $(-\Delta N_{FB})$, for both samples were in the order of 10^{11} charge/cm^2. Results from above measurements strongly suggest the low mobility and high retaining ab ility of Na ions in Al_2O_3 film. These results confirm previous finding in the Na isotope diffusion experiment (Tung et al. ECS Fall Meeting 1968, Boston, Mass.).

3.0 EFFECT OF INERT GASES

Continuous study was conducted on the effect of inert gases on the growth and C-V characteristics of Al_2O_3 films. The effect of A gas as main carrier gas in Al_2O_3 film deposition was presented in the second quarterly report. This quarter, the effect of He on Al_2O_3 film was investigated. It was found that the film growth rate decreases linearly with increasing He content in the main carrier gas. Results are shown in Fig. 1, in which the He content was varied from 10% to 90% and the respective growth rate varying from 95 to 40 Å/min. The film quality appears poor and non-uniform when the He content exceeded 90%. Refractive index is approximately 1.745 independent of He content in the carrier gas. Study on C-V characteristics of these films is in progress. Preliminary measurements reveal that the C-V characteristics are more or less similar to those prepared in H_2 carrier gas. However films from high He content carrier gas exhibit low resisistivity varying from 10^{13} to 10^6 Ωcm.

4.0 EFFECT OF POST DEPOSITION HEAT TREATMENT

The objective of post deposition heat treatment is to make the film more homogeneous, to reduce the surface state charge and to minimize the space charge density. In some instances the chemical stoichiometry might even be improved and the lattice defect can be reduced. This has been demonstrated

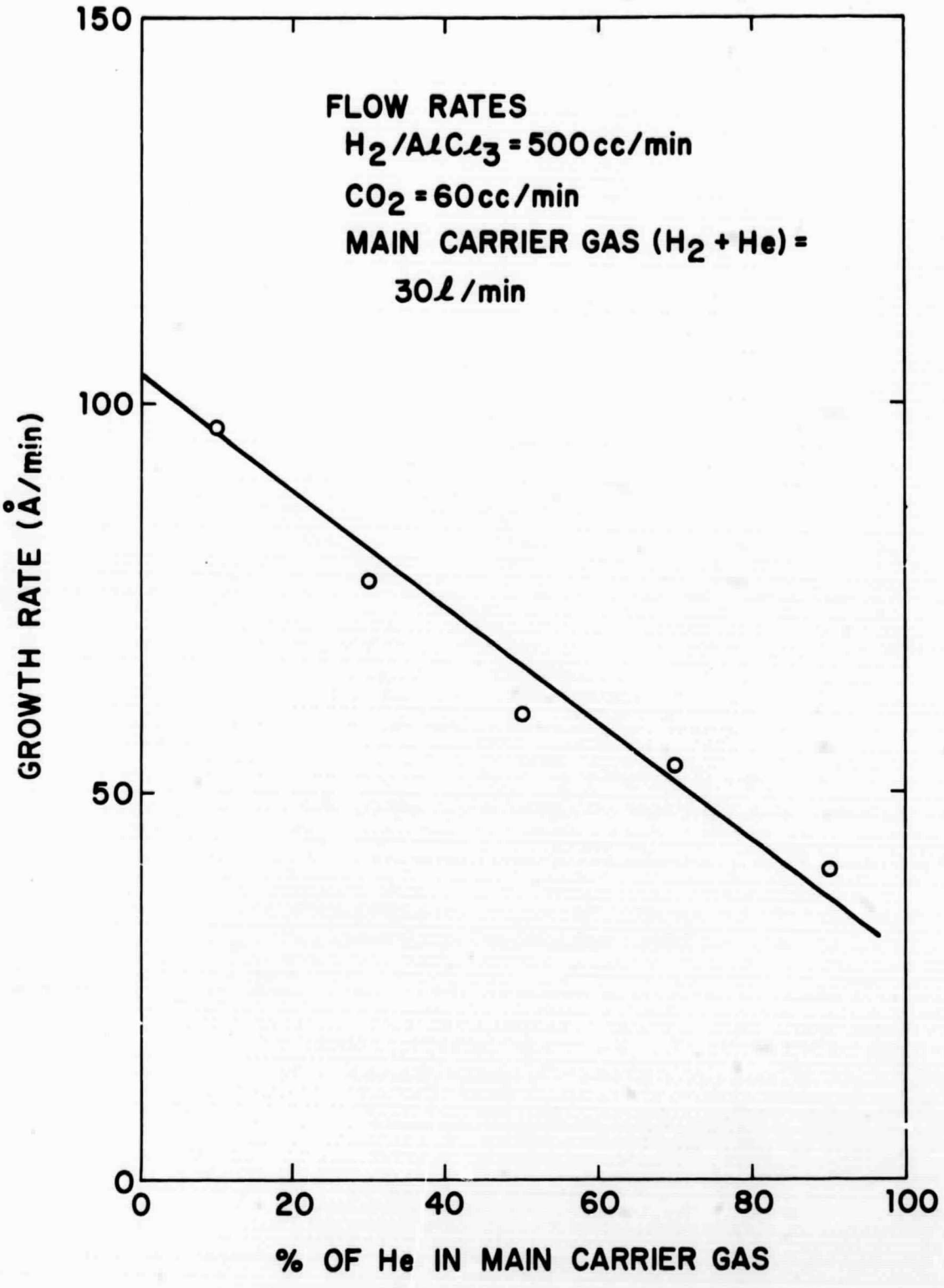

Fig. 1. Effect of substituting of He for H_2 as main carrier gas on the growth rate of the Al_2O_3 film.

in the case of thermally grown SiO_2 layer on silicon.[1,2] In Al_2O_3 - SiO_2 composite film the interfacial structure as well as its stability becomes extremely important. Thus we have conducted some limited experiments studying the effects of V_{FB} and N_{FB} resulting from past deposition heat treatment. Results will be ready in the next report.

5.0 PREPARATION OF TEST INTEGRATED CIRCUITS USING COMPOSITE Al_2O_3-SiO_2 FILMS AS GATE INSULATOR

In order to investigate the actual performance and merrits of Al_2O_3-SiO_2 gate insulator in integrated circuits applications, a test device of one-bit shift register, n-channel FET circuit[3] has been designed. Each circuit is located 0.032" apart, and consists of six FET, essentially of a flip-flop type. The circuit is so designed that each FET can be individually tested. The circuit has an overall size of 0.018" x 0.020". Figure 2 shows the circuit diagram and Fig. 3 represents its actual layout.

In preparation P^- ⟨100⟩ silicon wafers from chemical-mechanical polishing were used for the devices. These wafers have resistance of 2 Ω-cm. Approximately 5000 Å SiO_2 were first thermally grown on the well cleaned wafers, and the source and drain window patterns were carefully opened by conventional photo-etch methods. Phosphorus diffusion for the source and drain was conducted in an open tube. The junction depth of source and drain was controlled at approximately 1.5 μ and the sheet resistance after phosphorus diffusion was approximately 5 Ω/□. As indicated in the 2nd quarterly report, thin composite film of Al_2O_3-SiO_2 has low surface charge density and low turn-on voltage of less than 1.0V. Therefore, in the initial study of composite film of 500 Å Al_2O_3 over 500 Å SiO_2 was arbitrarily chosen for gate insulator in the intended IGFET device preparation.

We have nearly completed the first batch of two n-channel FET wafers using Al_2O_3 over in-situ grown SiO_2 as gate insulator. So soon as the final metallization is completed, they will be ready for performance testing. For

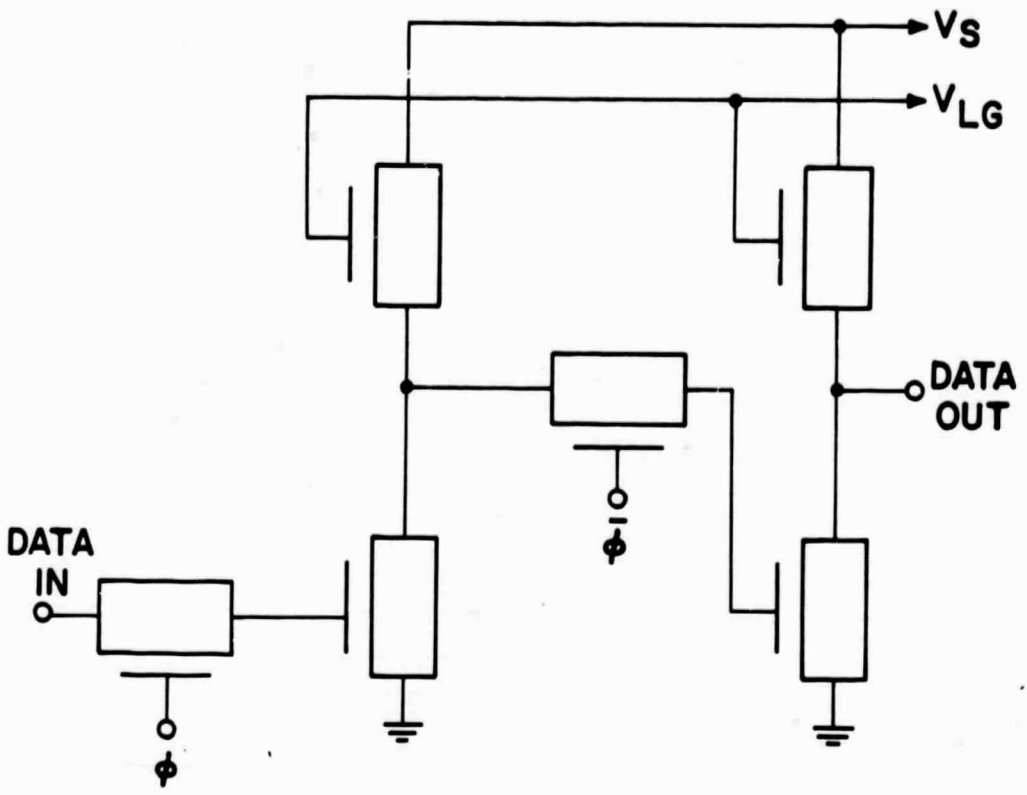

Fig. 2. Circuit diagram of one-bit shift register circuit.

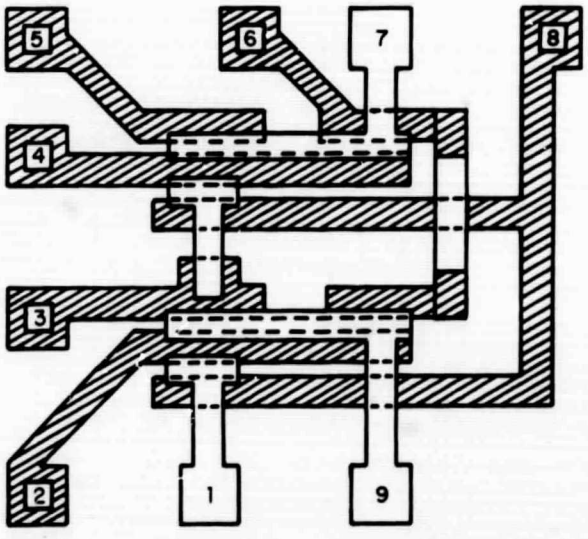

Fig. 3. Mask layout for one-bit shift register circuit.

the purpose of comparison a study on composite film of Si_3N_4 over SiO_2 as gate insulator is also under the way.

A testing system for the prepared devices is being set-up. Primarily we are intending to measure the turn-on voltage and transconductance of each FET in the shift register circuit. For testing the circuit both dc and low frequency ac are being used.

6.0 NEW TECHNOLOGY APPENDIX

After a diligent review of the work performed under this contract, no new innovation discovery improvement or invention was made.

7.0 FUTURE WORK

The future work for the remaining contractual period will include the following:

1. To complete the study on the effect of post deposition heat treatment on the surface charge characteristics.
2. To complete the test device preparation.
3. To test and evaluate the prepared IGFET device including composite films of Al_2O_3/SiO_2 and Si_3N_4/SiO_2 as gate insulators.

8.0 ACKNOWLEDGEMENTS

The authors wish to thank Messrs. Joseph C. Hollis and Arthur G. Smith for their valuable contributions to this work.

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