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RESEARCH INTO THE FEASIBILITY OF THIN METAL AND OXIDE FILM CAPACITORS

by

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June 1969

Prepared Under Contract No. NAS 12-551 by

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for

Electronics Reseach Center

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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SECOND INTERIM SCIENTIFIC REPORT

RESEARCH INTO THE FEASIBILITY OF THIN METAL AND OXIDE FILM CAPACITORS (U)

by

M. E. Browning
G. V. Jorgenson
and
W. H. Graves

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NORTH STAR RESEARCH AND DEVELOPMENT INSTITUTE
Minneapolis, Minnesota

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SECOND INTERIM SCIENTIFIC REPORT

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SUMMARY

Two deposition techniques, low energy radio frequency (rf) sputtering and vacuum evaporation, were utilized in a continuing investigation of the feasibility of producing thin metal- and oxide-film capacitors. Dielectric material systems examined in the development work included SiO_2, Al_2O_3, TiO_2, and lead zirconate titanate.

SiO_2 gave the best results even with its lower dielectric constant because it had higher deposition rates and more stable electrical characteristics than the other materials. In most cases, deposited aluminum was used as the electrode material.

Electrical test characteristics of thin film dielectric capacitors were excellent at temperatures up to 300°C and for frequency ranges of 200 to 100,000 Hertz. The capacitors remained functional at 500°C, but with some deterioration in characteristics. A number of test systems were made up with multiple layers of dielectric film and metal-film electrodes, including systems containing as many as ten capacitive layers.

Deposition techniques were developed to permit control of thickness of both the dielectric layer and the electrode material. Interferometric examination of dielectric surfaces, deposited in thickness ranges between 2,000 and 5,000 angstroms, revealed a thickness variation of less than

five percent over the area of the capacitor. Tests for shorts in the capacitors indicated that more than 90 percent of the dielectric films were free of pinholes when deposited, and there was no change after baking at 250°C for more than 100 hours.

A number of modifications were made to the combination of the Ultek ultrahigh vacuum system and R. D. Mathis rf sputtering module, and this equipment was installed in a new Class 100 clean room. With this arrangement, SiO_2 can be sputtered from a five-inch-diameter target at rates that give values greater than five microns per hour for the product of deposition rate and dielectric constant. Capacitance-per-volume of deposited material has been increased from 190 μF per cm^3 for AH series capacitors[(1)]* using Al_2O_3 to 300 μF per cm^3 for lower-dielectric-constant SiO_2 capacitors.

Life testing has shown that Al_2O_3 capacitors require some thermal conditioning before they become stable. A bakeout for approximately 200 hours at 250°C is sufficient. No such conditioning step is required with SiO_2 capacitors, which remain very stable throughout life tests.

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*Superscripts refer to references at the end of the report.

Conventionally, thin film cicrocapacitors do not require high breakdown strengths, nor do they need to handle high power. In most situations, the problem is reduced to one of employing a capacitor with sufficiently high capacitance and insulation resistance for its application. The dielectric constants for the usual dielectrics lie between three and ten. At any specific dielectric constant, reduction of the thickness of the dielectric is the only means of obtaining higher capacitance per volume. As an example, a capacitor fabricated from a material with a dielectric constant of ten and a thickness of 2000 angstroms would have a capacitance of 0.044μF per cm^2 whereas, if the thickness was 500 angstroms, it would have a capacitance of 0.176μF per cm^2 in only one-fourth the volume of the dielectric. The fabrication of capacitors with dielectrics as thin as 500 angstroms is difficult because discontinuities and voids are more prevalent, and because film resistance and breakdown voltage -- both dependent on film thickness -- suffer as films become thinner. However, with a uniform film of 2,000 angstroms, the resistivity can approach 10^{15} ohm-cm, and 50 volts dc can be maintained readily without breakdown.

Techniques used to date to prepare thin film capacitors include such procedures as vacuum evaporation of metals with <u>in situ</u> oxidation[2], sputtering of a metal with subsequent anodic treatment to form the dielectric oxide[3], evaporation of silicon monoxide[4], or reactive sputtering, where the dielectric is developed by sputtering metal in an oxygen-rich plasma[5]. As an example, silicon monoixde has been frequently evaluated as a candidate dielectric material for thin film capacitors using vacuum evaporation procedures[6,7]. Silicon monoxide is a misnomer in this case, as the composition of the deposit is dependent upon evaporation parameters; insufficient vacuum tending to promote unpredictable higher-oxygen-containing SiO_x deposits[8]. Silicon dioxide, more desirable because of its stability, is, however, very difficult to deposit by vacuum evaporation procedures.

Until recently, the available deposition technology was not amenable to producing thin films of the desired dielectrics. Vacuum evaporation was exploited by numerous investigators, including Siddall[9], whose

studies of the use of SiO capacitors are representative. Problems usually found in this type of system are that the dielectric film is frequently porous, and is subject to stresses induced during evaporation and to lifting in moist air[10]. This produces an unstable capacitor, usually with a low dielectric constant varying between 2.5 and 3[11].

The technique of low energy rf sputtering is attractive for insulator films because of excellence in the control of stoichiometry and film thickness[12,13]. The technique as presently developed also yields high film density and permits a high degree of freedom from pinholes. Improved adherence is also obtained, because particles being deposited arrive at the substrate at much higher velocities than they do, for example, in vacuum evaporation[14].

Thin film inorganic capacitors that can withstand high-temperature environments up to 500°C and that have higher energy storage capability per unit volume than do presently available inorganic capacitors are of particular interest to the National Aeronautics and Space Administration for applications near energy converters, especially near nuclear reactors. Work undertaken by North Star Research and Development Institute to develop thin film metal oxide capacitors utilizing advanced deposition procedures is a large step toward this goal.

EXPERIMENTAL WORK

The experimental work in development of thin film dielectric capacitors involves studying both the optimum arrangement of deposition equipment and the actual deposition variables for the dielectric layers and the deposited electrodes.

Equipment Modification

Deposition equipment used in the initial study[1] was employed in the early laboratory work reported here. During the current reporting period, design studies and fabrication work were directed toward completing a new facility. The new test facility design incorporated an R. D. Mathis sputtering module and power supply, and an Ultek ultra-high vacuum (UHV) system. A specially designed substrate holder and mask changer were considered for use with the new unit. Operating procedures were established for operation of equipment in a new horizontal laminar-flow clean room (Class 100).

Capacitor development work was accomplished during the initial portion of this project year using the R. D. Mathis sputtering module on a North Star vacuum stand (Figure 1) or with a Consolidated Vacuum Corporation CVE-14 vacuum stand. A substrate holder and mask changer (Figure 2) were designed and fabricated for use with this system. Although completely operational, the substrate holder and mask changer could not be adapted to the ultimate arrangement in the Ultek unit. Hence, it was not employed further in the capacitor development studies.

Capacitor development work being performed in the plasma (indicated in Figure 3) was initially carried out in a six-inch-high, 18-inch-diameter glass cylinder mounted on the CVC vacuum stand (oil diffusion pumped). The sputtering module and cylinder were subsequently mounted on the Ultek base flange (combination base plate-metal chamber flange). This is shown in the sketch (Figure 4) illustrating the first ultra-high vacuum facility set-up. In this arrangement, steel bars were bolted to three lugs inside the sublimation well. These bars

supported a rod holding the six-inch-diameter substrate table in the center of the system. The electromagnet was at the level of the target-substrate combination. With this arrangement, an argon plasma could be produced using a dynamic system (continual flow of argon through the system). The principal drawback to the system (shown previously in Figure 4) was the fact that plasma filled the entire sublimation well. This occurred when the sublimator was off, but was even more of a problem when the sublimator was on. All the added electrons from the sublimator filament increased the plasma density in the well. The electromagnet could not maintain the plasma between the target and substrate except at very low power levels.

The first attempt at keeping the plasma out of the sublimation well was by increasing the diameter of the substrate table to one inch less than the inside diameter of the glass cylinder. This would leave about 30 square inches open for pumping out the upper space. This approach met with only partial success. The plasma was less dense below the substrate table, and the system could be operated at slightly higher power without plasma developing in the lower region. This power level was too low to produce useful films in reasonable times. A second 750-turn electromagnet was then added to the system in a manner such that the bottom of the upper magnet was positioned approximately in the plane of the target, and the top of the lower magnet in the plane of the substrate. These magnets, circular and positioned around the cylinder, were connected in series with 2.4 amps supplied to produce a 3600-ampere-turn system.

This significantly increased the plasma density, but some plasma penetrated below the substrate table. A screen (conventional aluminum window-screen material) was positioned on the substrate table around the outer edge of the table and bent down along the glass wall. It prevented the rf field from developing below the substrate table and maintained plasma exclusively above the table. However, this arrangement does not lend itself readily to the substrate holder and mask changer described earlier, or to a "Ferris wheel"-type jig, where

the dielectric is sputtered at the top and electrode material is evaporated at the bottom. Present considerations favor an approach where both the dielectric and the electrodes are sputtered. After an electrode has been deposited through an appropriate mask, the mask can be changed for dielectric deposition. A dielectric target is then swung into place in front of the metal target and in contact with it. With minimal retuning to match this load to the transmitter, dielectric sputtering can be accomplished without breaking vacuum.

A Class 100 horizontal laminar-flow clean room was designed and constructed for installation of the Ultek ultrahigh vacuum system. The clean room was equipped with a workbench, sink, and equipment storage facilities to handle mask changers and other peripheral capacitor fabrication equipment. Air conditioning was added to maintain temperature and humidity requirements and to permit more exacting working conditions. The filter and air-handling equipment were designed to process 6½ air changes per minute. Figure 5 shows the Ultek sputtering system and service modules as they are presently located in the clean room. Currently, operating equipment uses a second circular magnet, described previously.

Deposition Variables

The major emphasis during the development work on thin film capacitors was placed on the dielectric materials, and particularly the sputtering procedures. Detailed consideration was given to such deposition variables as vacuum system operation, arrangement and performance of the sputtering module, and effect of heating the substrate, increasing plasma density, and changing substrate materials. The vacuum evaporation of aluminum and the deposition of tantalum or titanium (where used) was typically conventional, and a limited examination of deposition variables for these procedures revealed no dramatic or significant effects either on the dielectric material or the electrode metal being deposited.

In investigating the ultrahigh vacuum system (Ultek UHV unit described previously), the operating procedure was reviewed in detail to ascertain whether optimum deposition conditions were being maintained.

The system could be conveniently pumped down (sorption roughing stage, the sorption and titanium sublimation stage, and finally sublimation and ion pumping stage) into the 10^{-8} Torr range. In routine practice, the ion pump was valved off, the sublimator was left on at low setting, argon was bled into the system through a 1^{o} leak valve, and the roughing system was cracked open to one liquid nitrogen-cooled sorption pump. This approach was used because it was easier to maintain a constant pressure in a dynamic system. To maintain constant pressure in a static system (no pumping), only as much argon must be introduced as is being lost because of sputtering. The sublimator was allowed to operate continually in order to remove any impurities released by plasma action or introduced with the tank argon.

A typical operating cycle for the preparation of the thin film dielectrics using the Ultek facility is as follows:

1. Substrates are loaded into the 18-inch ring vacuum chamber on the Ultek ultrahigh vacuum system (up to four at one time).

2. The system is then evacuated to a pressure of approximately 8×10^{-8} to 1.5×10^{-7} Torr. These pressures are about two orders of magnitude lower than the background pressure formerly used in our oil diffusion pumped system.

3. The titanium sublimator is then turned on for continuous operation at 35-38 amps; the ion pump valve is now closed.

4. Argon is then fed into the vacuum chamber through a 1^{o} needle valve opened to 0.62 turns.

5. At this point, one of the sorption pumps has been evacuating the sorption pump manifold. When the argon pressure in the chamber rises higher than the pressure in the manifold, the valve between the two is opened about 3-1/3 turns (this same valve position is maintained each time).

This combination of sublimation and sorption pumping gives the following advantages:

a. The sublimation pump will readily remove any impurities from the argon, and equally important, remove the impurities that may be desorbed from walls and fixtures resulting fro... the action of the plasma.

b. The sorption pump permits a slow pumping of the argon to maintain a dynamic system inasmuch as this makes constant pressure control much easier.

6. In two to three minutes after the valve to the sorption pump manifold is opened, the deposition system attains a steady state pressure. The dielectric material is now ready to be sputtered.

In rf sputtering, power densities of approximately 2.5 watts/cm^2 have been reported to give deposition rates of 50-60 angstroms per minute of SiO_2 [15]. In the present North Star arrangement with the R. D. Mathis sputtering module and a five-inch-diameter target, deposition rates of 235 angstroms per minute are obtained at power densities of 2.2-2.5 watts per cm^2.

Effect of Heating the Substrate. In examining the effect of heating the substrate, titanium dioxide was used as the dielectric material. Substrate temperatures were varied from 125°C to 350°C. At the lower temperature, test capacitors as thin as 915 angstroms were produced and examined. The following favorable test results are typical of those obtained:

Capacitance	Dissipation Factor	Dielectric Constant
18,223 pf	0.0197	27
23,508 pf	0.0093	31

TiO_2 films deposited at 350°C were subject to extensive crazing, making it impossible to measure their electrical characteristics. Because of difficulties in sputtering TiO_2 (as discussed later), this work was not continued at other temperatures.

Increasing Plasma Density. To examine the effect of increased plasma density, two new electromagnets were fabricated. Two Helmholtz coils of 250 turns each were placed on either side of the vacuum chamber fitted with the R. D. Mathis unit so that the magnet axes passed across the center of the target face. When the magnets were turned on with a current of ten amperes, there was a definite increase in plasma density (thinner dark sheath). The magnets were not capable of operating at ten amperes continuously, so new 1,000-turn magnets were specially fabricated. The new magnets were wound on narrow, almost elliptical reels, as opposed to the old circular magnets, to achieve a planar geometry in the magnetic field. The design was expected to produce a narrow sheet of high-density plasma near the target without too much plasma near the substrate.

However, the elliptical magnets were only partially successful; they produced a rather thin plasma sheet in the deposition chamber except in the area near the center of the target, where the high-density plasma dipped down to the substrate table. The problem in this regard is that the substrate is placed in the central area because that is where the highest deposition rate and greatest uniformity are obtained. Emphasis, therefore, shifted back to using circular magnets with their axes parallel to the target-substrate table axis. Two circular magnets, presently employed, produce a sufficiently high-density plasma for high-quality SiO_2 deposition.

Dielectric Materials Examined. Four different insulators (SiO_2, Al_2O_3, TiO_2, and lead zirconate titanate) were examined as candidate thin film dielectrics. In all tests, low energy rf sputtering was used, but target size and spacing (target-to-substrate table) varied somewhat. Capacitor configuration varied during the conduct of the program, ranging from a simple dot with extending side tabs to a grid arrangement (shown in Figure 6). Test capacitor series were labeled with letters primarily for work performed in vacuum systems using oil diffusion pumps (e.g. AH-AL and BA-BQ), but Roman numerals were used for test series developed in the Ultek UHV system. Systems differed in series designation depending upon type of dielectric used, electrode material deposited, and thicknesses of deposited layers.

Thickness Uniformity

A study of thickness uniformity of deposited film in the R. D. Mathis system was carried out by making steps at various places on a substrate and measuring the depths of the steps interferometrically. The steps were made by placing small pieces of quartz cover glass on the quartz substrates prior to sputtering. The film was then deposited on the unmasked area. The position of each measured step was noted with respect to the center of the target.

The results for a five-inch-diameter fused quartz target on a 3.5-inch-diameter target electrode are plotted in Figure 7. The zero on the abscissa denotes the center of the system, and the other numbers are distances from the center in centimeters. The units on the ordinate are relative, with 1.0 being the thickest film. The film is thickest at the center and begins to drop off very near the center. The region in which the thickness remains within ten percent of maximum is a circle of 2.0 cm radius in the center of the system when the target-to-substrate distance is 5.1 cm (curve a). When the target-to-substrate distance is reduced to 3.8 cm, the radius of the circle with ten percent maximum deviation is about 3.1 cm (curve b).

SiO_2 Multilayer Capacitors

Several series of SiO_2 multilayer capacitors (0.950 cm in diameter) were prepared by vacuum evaporation and sputtering for additional testing and electrical characterization. In this particular group, all multilayer capacitors were prepared using the sputtering system with the oil diffusion pump and using SiO_2 dielectric layers between 2500 and 4800 angstroms in thickness. Prepared capacitors were checked for shorts and tested at elevated temperature. All were found to be satisfactory. Aluminum electrodes were deposited in thicknesses varying between approximately 1,000 and 1,400 angstroms. All capacitors representing these series (AH-AM) were found to possess high parallel resistance.

Using the values of thickness, area, and bulk resistivity, the dc resistance can be computed:

$$\text{Resistance} = \frac{(\text{Resistivity})\ (\text{Length})}{\text{Area}}$$

While it is recognized that the thin film resistivity may be significantly different from bulk value, the bulk resistivity was available and was used to compute the dc resistance at various temperatures. Typical calculated results are given in Table 1. Values of dissipation factor are also given for three of the temperatures. As would be expected, the dissipation factor increases with decreasing film resistance.

Deposited thin film and bulk SiO_2 were compared for selected electrical properties. These data are presented in Table 2. Advancements in deposition techniques are presumably responsible for property improvements, noted in sources 2 and 3.

Representative of electrical test characterization of a typical SiO_2 capacitor, fabricated with aluminum electrodes and prepared by sputtering in the R. D. Mathis unit with oil diffusion pumping, is a series of property curves prepared for Series AH Al-SiO_2 capacitors. Layer thicknesses varied from 3,500 to 4,800 angstroms.

TABLE 1

COMPUTED VALUES OF CAPACITOR RESISTANCE

Temperature ^{o}C	SiO_2 Purity	Resistivity (Bulk Value) ohm-cm	Computed Value of Capacitor Resistance (ohms) using bulk value of resistivity	Average Selected Measured Values of Dissipation Factor at 1 kHz
25	(96%)	10^{17}	10^{12}	7.5×10^{-4}
250	(96%)	5×10^{11}	6.7×10^{6}	5×10^{-3}
277	(99.8%)	4.5×10^{9}	6×10^{4}	-
350	(96%)	4×10^{9}	5.4×10^{4}	20×10^{-3}
477	(99.8%)	2.1×10^{7}	2.8×10^{2}	-

TABLE 2

COMPARISON OF SELECTED ELECTRICAL PROPERTIES OF SiO_2 (DEPOSITED AND BULK)

Data Source	Dielectric Constant	Unit Capacitance ($\mu F/cm^2$)	Temperature Dependence of Capacitance ($ppm/^{o}C$)	Dissipation Factor
1. Schwartz & Berry[11]	2.5-3.0	0.018 (3000 Å)	+100 to +400	0.01 to 0.1*
2. Pratt[16]	3.94	0.011	-57	0.0007 (below 5500 Å ~0.001)**
3. North Star Research	3.5	~0.009	+20	0.001 to 0.002**
4. General Electric (bulk material)	3.75	-	-	<.0001***

* audio
** 1 kHz
*** 1 MHz

Plots of capacitance versus frequency for various temperatures from 22° to 512°C are shown in Figures 8 and 9. It is of interest that capacitance values are essentially constant (varying within 1.5 percent) at temperatures to the 300°C level, and at frequencies between 0.5 and 100 kHz.

As can be seen in Figures 10, 11, and 12, the variation of dissipation factor with temperature is the smallest at the higher frequencies. Data plots at various frequencies for multilayer systems are typical of Al-SiO_2 single-layer capacitors examined previously. Figure 10 covers the effect at the temperatures of 22° and 134°C. Figure 11 shows curves for temperatures of 213° and 314°C, while Figure 12 shows curves for temperatures of 409° and 512°C.

The electrical properties of double-layer Al-SiO_2 capacitors made with the R. D. Mathis unit in the oil diffusion pumped system were characterized to examine the effect of frequency and temperature on dissipation factor. The reliability of typical capacitors at different temperature ranges is shown for Series BN capacitor systems in Figures 13 and 14. The effects of frequency and temperature on capacitance are illustrated in Figure 14. Thicknesses of the dielectric material were 2,950 and 3,200 angstroms. Typical test values obtained for this system are capacitance of approximately 16,500 pF and dielectric constant approaching 4. The dissipation factor at 1,000 Hz is approximately 0.002.

Other double-layer capacitors (Al-SiO_2 systems) were deposited on eight- to ten-mil-thick quartz substrates. Electrical characterization of this series (B) gave results of 18,380 pF using the 3/8-inch-diameter configuration. Dissipation factor value for this series was 0.0015. The effect of frequency and temperature are shown in Figure 15.

Temperature tests from approximately 23°C and 300°C show that both Series BN and BO have almost identical percent capacitance change at a frequency of 200 Hz. Figure 16 shows curves illustrating the uniformity in capacitance viewing the effect of temperature and frequency variations.

The effect of temperature of dc resistance for the Al-SiO_2 multilayer system is shown in Figure 17. The resistance begins to decrease very rapidly above 400°C. The shape of the curve indicates that the film begins to lose its insulating character as the temperature approaches 500°C.

Typical of electrode and dielectric thicknesses deposited for these four-layer Al-SiO_2 capacitors is the profile for the system AM:

Electrode (Al) -- 995 to 1,460 angstroms
Dielectric (SiO_2) -- 4,200 to 4,820 angstroms

Laboratory work was continued in developing SiO_2 dielectric capacitors using the R. D. Mathis sputtering unit mounted on the Ultek ultrahigh vacuum unit. Facilities for these continuing studies were operated in the new Class 100 clean room. Typical dielectric deposition conditions during these sputtering runs included:

Substrate-to-target spacing	1 - 1½"
Voltage	1000 V
Ionizing gas	Argon*
Dielectric thickness	3,000-3,500 angstroms

The sputtering was accomplished with electromagnet coils operating at 2.4 amps. Reflected rf power was measured and found to be below the maximum level prescribed for best operation of the R. D. Mathis unit. In most of the SiO_2 deposition work, the substrate table was used without supplemental cooling. Aluminum electrodes were deposited to approximately 1,000 angstroms thick. The sputtering target was a fused quartz disk (General Electric Type 101), five inches in diameter and one-eighth inch thick.

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*One test run was made with Argon -- five-percent oxygen

The best values that have been achieved for product of dielectric constant and deposition rate of SiO_2 are approximately 5.7 μ per hour. This is for a SiO_2 deposition rate of 290 angstroms per minute and dielectric constant of 3.3. A typical deposition rate is 235 angstroms per minute, with a dielectric constant of 3.5, giving a product of 4.9 μ per hour.

A number of multilayer Al-SiO_2 capacitors (possessing six or more capacitive layers) were fabricated for electrical property studies. The Series III capacitor was a nine-layer capacitor system (nine SiO_2 layers and ten Al layers). The total dielectric thickness is 28,600 angstroms and total Al thickness is approximately 12,000 angstroms. The capacitance of 30,000 pF is considerably less than would be expected from this 0.71 cm^2 stack. However, there were a number of small shorts in various layers, and these were burned out and deposition continued. Apparently, one of the results of having to burn out shorts is that capacitance decreases, and it decreases more than would be indicated by the area that is lost in the burn-out procedure. The capacitor's high temperature characteristics of capacitance do not seem to be affected by curing the shorts. Figure 18 shows electrical test results for the effect of frequency on dissipation factor of typical Series III multilayer capacitors examined at temperatures ranging from 21° to 248° C. The change in slope of the curve at the higher temperature and lower frequency is as expected.

Figure 19 is a plot of capacitance versus frequency for Series III capacitors in the same temperature range. The rapid rise in capacitance at frequencies above 10,000 Hertz is uniform for all test temperatures, and has previously been witnessed at lower capacitance values with SiO_2 (Reference 1, Figure 28).

Series IV and Series V capacitors are both six-layer capacitors. They both have approximately 26,000 angstroms of SiO_2 and approximately 8,500 angstroms of Al. These capacitors were essentially free of shorts and have more capacitance per layer than Series III. Capacitances of approximately 31,600pF and 30,600pF respectively would be higher except that both capacitors have one very thick dielectric layer (7,000 angstroms), and one layer of over 5000 angstroms.

Figure 20 shows a curve of dissipation factor versus frequency between 24° and 251°C for Series IV six-layer capacitors. Variation in dissipation factor at lower frequencies and the higher temperature is not unexpected.

Figure 21 depicts the change in capacitance of typical Series IV Al-SiO_2 multilayer capacitors as a function of temperature and frequency. The very small percentage variation in capacitance between 24° and 251°C indicates high thermal stability in the dielectric/electrode layer deposition.

The effect of elevated temperature (from 24° to 244°C) on dissipation factor of Series V capacitors as a function of frequency is shown in Figure 22. These six-layer capacitors have very little sensitivity-to-temperature differences except at very low frequencies. At frequencies from 1,000 Hz to 100,000 Hz, the curves are exceptionally parallel.

Capacitance change as it relates to frequency at four test temperatures (from 24° to 244°C) for Series V multilayer capacitors is seen in Figure 23.

The dissipation factor curves for Series III, IV, and V as a function of frequency and temperature are nearly the same. The bulk value of the dissipation factor for fused quartz at a frequency of one kHz and a temperature of 200°C is approximately 2×10^{-3}. Measured values on the three series are within the expected dissipation factor range. Series III has a higher dissipation factor at 100 kHz than Series IV and V. This may be due to the number of small shorts that were burned out in various layers.

The capacitance characteristics of all three Series behave in nearly an identical manner. The change in capacitance at 1,000 Hz for Series III, IV, and V is 1.1, 1.05, and 1.27 pF per °C. The variations of capacitance are less than one percent for an average temperature change of approximately 220°C. These small variations are expected and compare favorably with the SiO_2 system that has been measured previously.

A number of capacitors (Al-SiO_2) have been fabricated in the Ultek system and were heated to 200°C in air for approximately 150 hours. The dissipation factor and the capacitance increased with temperature by only a very small amount. When the capacitors were returned to ambient temperature, dissipation factor and capacitance dropped to values lower than those originally recorded. Capacitances before and after thermal conditioning are normally close, varying by less than one percent. Dissipation factor measurements show the same tendency for being lower after heat conditioning, but there is less consistency between capacitors. Typical of capacitors before and after 150 hours of thermal conditioning in air at 200°C are the following results:

Capacitance-5094 pF before -- 5081 pF after thermal conditioning
Dissipation factor—0.001 before -- 0.0008 after thermal conditioning

Al_2O_3 Multilayer Capacitors

Studies were initiated for the preparation of stacked multilayer Al_2O_3 capacitors, using deposition procedures established for the Al-SiO_2 systems. In attempting to produce a four-layer capacitor, it was observed that shorts in the dielectric were so numerous by the time the third layer was deposited that conventional healing techniques would not work effectively. Examination of the surfaces revealed a "crazing" condition, rather that pinholes. This indicated that the problem was created by stresses in the Al_2O_3 that are probably related to differences in thermal expansion.

The initial Al-Al_2O_3 multilayer systems utilized a first-layer dielectric (Al_2O_3) of 3,450 angstroms thickness, but the thickness of the first layer in the subsequent trial was increased to 6,000 angstroms to eliminate pinholes. In the latter systems, the finished capacitors had smooth, continuous surfaces, and electrical tests showed them to be free of shorts.

System AQ represents four-layer Al-Al_2O_3 capacitors of approximately 16,650 angstroms total dielectric thickness, and approximately 8,500 angstroms total electrode thickness. The area of the capacitor is 0.71 cm^2. The capacitance at room temperature at one kHz was approximately .036 μF, which gives a capacitance per volume of deposited material of 200 $\mu F/cm^3$. This is considerably improved over 70 $\mu F/cm^3$ obtained for Al-SiO_2 four-layer capacitors produced in the first phase of the project.

Elevated temperature tests of this series disclosed that failure began to occur somewhere between 284° and 330°C. Cooling to room temperature and further examination revealed persistent low resistance in the system.

Life Test Studies

Initial standardization life test measurements were made on Al-Al_2O_3 thin film capacitors. Tests were made using the three-eighth-inch-diameter configuration and the high-temperature test unit described in the First Interim Scientific Report[1].

A number of Al_2O_3 dielectric capacitors with aluminum electrodes were prepared and examined under life testing conditions. Electrical testing of a typical Al-Al_2O_3-Al capacitor with 3,700-angstrom-thick dielectric revealed a room temperature capacitance (C) of 7,333 pF, and the dissipation factor (DF), 0.0026. When the capacitor was heated to 250°C, these values increased to 7,760 pF and 0.0094, respectively. Figure 24 shows the effect of time and exposure to 250°C on capacitance and dissipation factor. The test was terminated at 222 hours when it appeared that equilibrium had been reached in the electrical properties at C = 7,640 pF and DF = 0.0072. When the capacitor was returned to

27°C, the electrical values had changed to C = 7,220 pF and DF = 0.0020. Changes in electrical properties in this capacitor on initial heating demonstrate the necessity for a conditioning step (thermal treatment) prior to performance testing.

Examination of a similar type capacitor employing a thinner dielectric layer (2,840-angstroms dielectric) gave 27°C test values of C = 6,890 pF and DF = 0.022. The capacitor was baked at 400°C for several hours, then returned to 27°C. Electrical properties were then found to be C = 6,685 pF and DF = 0.002. The order-of-magnitude decrease in DF indicates that some fault in the system was improved during the bakeout. The treated capacitor was then life-tested for 165 hours at 250°C. The capacitance and dissipation factor remained at 7,070 pF and 0.0100, respectively, as shown in Figure 25. When cooled to 23°C, the values were C = 6,675 pF and DF = 0.0020, indicating that the high-temperature thermal treatment had definitely improved capacitor performance.

To further examine the effect of varying dielectric and temperature, an Al-SiO_2-Al capacitor of the same configuration was life-tested at 250°C. This capacitor had a dielectric thickness of 3,440 angstroms, and, at 23°C, gave test results of C = 4,600 pF and DF = 0.0010. This unit was not thermally pretreated before life testing. The results of baking at 250°C during the test are shown in Figure 26. Note that capacitance is slightly higher than room temperature value, but did not change with time at elevated temperature. Dissipation factor also changes with temperature, and the increase from 0.0026 to 0.0030, revealed in the lower curve of Figure 26, is not readily explained. This phenomena has not shown up in other tests. The elevated temperature exposure appeared to have very little effect because the 23°C readings after the life test were C = 4,570 pF and DF = 0.0010.

Surface Defect Studies

Previous problems in Al_2O_3 dielectric-film deposition, especially relating to the Ta-Al_2O_3 capacitor system, were studied using temperature-sensitive liquid crystals. Experimental work indicated that the contact

tab area becomes the weaker part of the capacitor where the tabs have to cross over steps left by previous depositions. The liquid crystal solution used on the subject test capacitors was LC-130 from Pressure Chemical Company, having a color sensitivity from 30.2° to 32.2°C. Variations in conductivity (or resistance) in the capacitor create different temperature zones and are seen in the liquid crystal indicators as color changes.

Figure 27 shows a multilayer Ta-Al_2O_3 capacitor coated with liquid crystal. A dc potential was applied to the contacts, and it can be seen that color changes began at the tab areas and progressed inward. Thus, the tab areas are the highest conductivity areas of this capacitor. Indications are that this capacitor system has defect regions, rather than a few pinholes, causing its low electrical resistance.

Additional tests were initiated to examine a specially prepared capacitor possessing known shorts. Trials with this type of material using Al-Al_2O_3 systems were unsuccessful because the shorts were healed during the testing with liquid crystals. It is of interest to note that potential regions of capacitor weakness were found during this study rather than specific pinholes or clusters as were originally anticipated.

Emphasis was shifted back to SiO_2 as the dielectric material after the work with Al_2O_3 because the lower deposition rate for Al_2O_3 (approximately one-half to one-third that of SiO_2) and the higher temperature coefficients of capacitance and dissipation factor more than offset the improvement obtained in dielectric constant.

TiO_2 Capacitor Systems

The requirement for high capacitance per unit volume and also for high value for the product of dielectric constant and deposition rate led to a rather extensive investigation of TiO_2 as the dielectric. Its bulk dielectric constant of about 100 made it very appealing, compared to SiO_2 at about 3.75 and Al_2O_3 at about 9.6.

A four-inch diameter x one-fourth-inch-thick TiO_2 target was obtained from Cerac, Inc. In early sputtering trials, it was found that there was considerable arcing at the three points of contact where clips held the target to the target electrode (arcing did not occur with SiO_2 or Al_2O_3). Thin slabs of Al_2O_3 (~.030 inch thick) were placed between the clips, and the TiO_2 target, and this reduced the arcing considerably. With this arrangement, sputtering voltages were slowly increased until, at ~1,600 volts, the target shattered. It appeared that this failure may have been due to the high thermal gradient. Cerac, Inc., supplied a replacement target of lower density that might reduce thermal stresses. This target was mounted with a one-half- to one-mm space between it and the water-cooled electrode, thus reducing the thermal gradient in the target. This target cracked at ~1,100 volts. The fracture line ran through two of the areas where it was fastened by the clamps, suggesting that hot spots were still being produced at these points. The target was re-assembled from the pieces and found usable. It was limited to use at only very low voltages, and even at these conditions it cracked further. Additional attempts to sputter TiO_2 reproducibly were made by examining different mounting schemes. One scheme was to place a one-fourth-inch thick Al_2O_3 target between the rf electrode and the TiO_2. Another was to bond the TiO_2 directly to the rf electrode with a high-temperature -- low-vapor-pressure adhesive, eliminating the need for clips. These techniques also failed to produce the desired results. A second replacement target was supplied by Cerac, Inc., but it also fractured. This target had been given a special stress relief treatment not normally used in producing these targets. The target fractured while operating at ~1,400 volts.

A number of TiO_2 capacitors were made during this period. Dielectric constants of these capacitors ranged from 27 to 60, with most in the 30 to 35 range. This would be a satisfactory dielectric constant, but deposition rates were very low. Values for the product of dielectric constant and deposition rate were lower for TiO_2 dielectric than for SiO_2. Capacitors made with TiO_2 having dielectric constants of from

30 to 40 had sputtering rates so low that the best value obtained was 4.45 μ/hr. Until some way can be found for improving these rates (generally about ten angstroms per minute with highs of ~20 angstroms per minute), TiO_2 is limited in its application for thin film capacitors.

Lead Zirconate Titanate Capacitors

In an attempt to produce capacitor films with higher dielectric constants, a disk of lead zirconate titanate (PZT-4 type) was obtained for sputtering trials. This material has a dielectric constant reportedly greater than 1,000. Sputtering trials were made with the PZT-4 specimen attached to the front of a standard four-inch-diameter Al_2O_3 target in a central position. The area of the titanate was approximately one-third that of the alumina, creating a situation where both materials would be deposited simultaneously.

To prevent breaking of the titanate target, power was applied at gradually increasing levels, finally sputtering at 1,000 volts. An experimental capacitor 7,350 angstroms thick was deposited in five hours using our three-eighths-inch-diameter capacitor configuration (shown in Figure 28).

Electrical tests revealed a capacitance of 11,500 pF (dielectric constant of 13.5), higher than our previous measurements for sputtered Al_2O_3, but not a significant improvement. The film structure may have been affected by being deposited on a cool substrate and by the presence of significant amounts of Al_2O_3. Use of a hot substrate should promote larger grain size in the deposit, with a resulting higher dielectric constant, but a larger lead zirconate titanate target must be obtained before additional tests can be made.

Surface and Microstructure Characterization

A brief examination of surface characteristics was initiated in an attempt to learn more about pinhole formation. Al_2O_3 and SiO_2 were reviewed for possible gross imperfections. The Al_2O_3 dielectric

layers appeared to present considerable pinhole problems in early work. This situation occurred more frequently in the CVC system than in the Ultek system, and was more prevalent in Al_2O_3 than in SiO_2. In laboratory work with SiO_2, dielectric layers deposited in high or ultrahigh vacuum conditions, the pinhole problem seems to have diminished considerably. As an example, a large Al-SiO_2-Al capacitor system was examined for pinholes, both with optical and electron microscopy, without detecting pinhole areas. Figure 29 shows two views of an Al-SiO_2-Al capacitor system. The upper view reveals a typical area of the capacitor (electrode surface) at 500 X while the lower view depicts a section magnified by electron microscope to 7,000 X. The aluminum electrode surface reveals the characteristics of a smooth substrate, sputtered SiO_2 in this case, and its freedom from pinholes. While it is acknowledged that some pinholes will be present in nearly all sputtered dielectrics, special handling procedures and clean room operation clearly permit a higher quality in capacitor fabrication and a reduction in pinhole probabilities.

CONCLUSIONS AND RECOMMENDATIONS

Thin film multilayer capacitors were fabricated using both low energy rf sputtering and vacuum evaporation techniques. Of the dielectric materials examined, including SiO_2, Al_2O_3, TiO_2, and lead zirconate titanate, the silicon dioxide dielectric material produced capacitors that gave the highest values for capacitance-per-volume (300 μF per cm^3 of deposited material). Capacitors made with Al_2O_3 were of moderate interest, but deposition techniques were not sufficiently developed to permit the reliability and pinhole freedom required for quality capacitors. Deposition studies of TiO_2 were of interest because of the high dielectric constant in the deposited dielectric layers (dielectric constants of up to 60 were obtained). However, problems appearing to reside in the target material and the attendant continual cracking or chipping experienced throughout the deposition studies suggested that improved fabrication techniques for sputtering targets of TiO_2 may be necessary before additional work is warranted.

Aluminum was preferred as the electrode material because it was conveniently deposited by evaporation and was amenable to healing shorts in dielectric films where pinholes existed. Other electrode materials, such as titanium and tantalum, were also of interest; Ti because it would match well with TiO_2 films and Ta because its thermal expansion coefficient matches well with Al_2O_3. These metals vaporized at such high temperatures that shorts resulting from pinholes in the dielectric films could not be "healed" by the usual techniques.

The use of North Star's new Class 100 clean room has shown a significant improvement in the electrical properties of capacitors made in the Ultek UHV system. Highest values achieved for dielectric constant times deposition rate for SiO_2 were approximately 5.7 microns per hour. This reflected the improved deposition rate of 290 angstroms per minute for depositing a material with a dielectric constnat of only 3.3. Typical deposition rates obtained near the conclusion of this report period show SiO_2 deposited at approximately 235 angstroms per minute with a dielectric constant of approximately 3.5.

It is recommended that additional work be conducted to develop reliable methods for obtaining thin film multilayer capacitors with a much larger number of capacitive elements. Techniques for interconnecting the electrodes to form a single thin film capacitor of the order of one μF need to be investigated. Additional work is needed to reduce the thickness of the substrates. Because initial investigations of materials that had higher dielectric constants than SiO_2 and Al_2O_3 looked promising, it is recommended that some continuing investigation into the feasibility of thin film capacitors with such materials be instituted.

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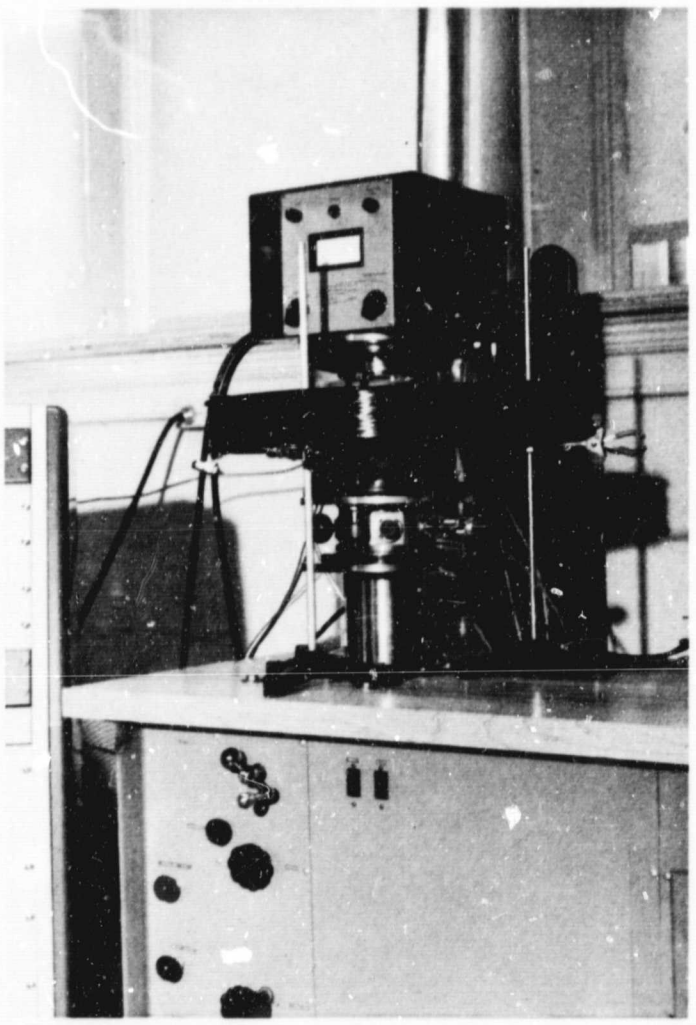


FIGURE 1. R.D. MATHIS SPUTTERING MODULE ON NORTH STAR RESEARCH VACUUM STAND

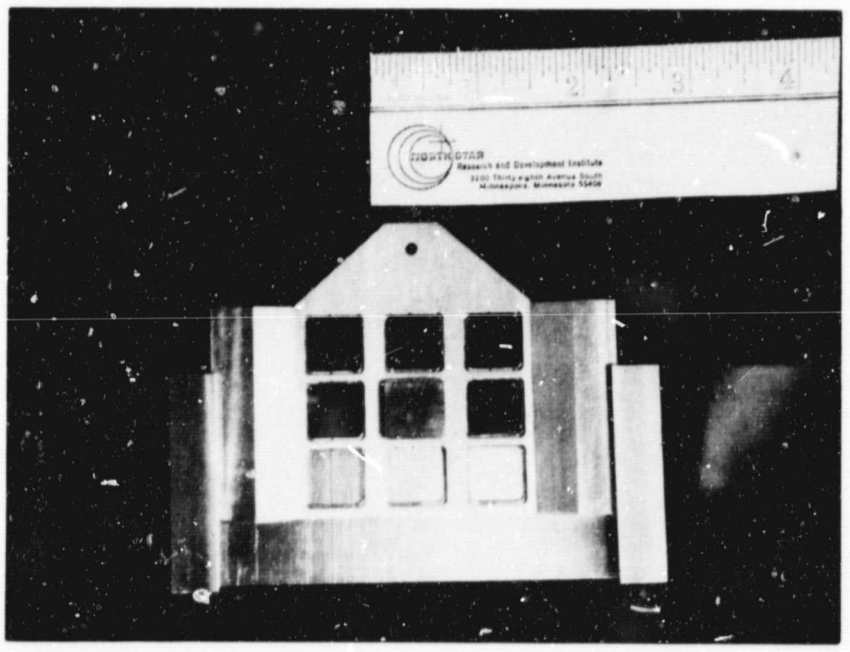


FIGURE 2. SUBSTRATE HOLDER AND MASK CHANGER FOR CAPACITOR DEPOSITION

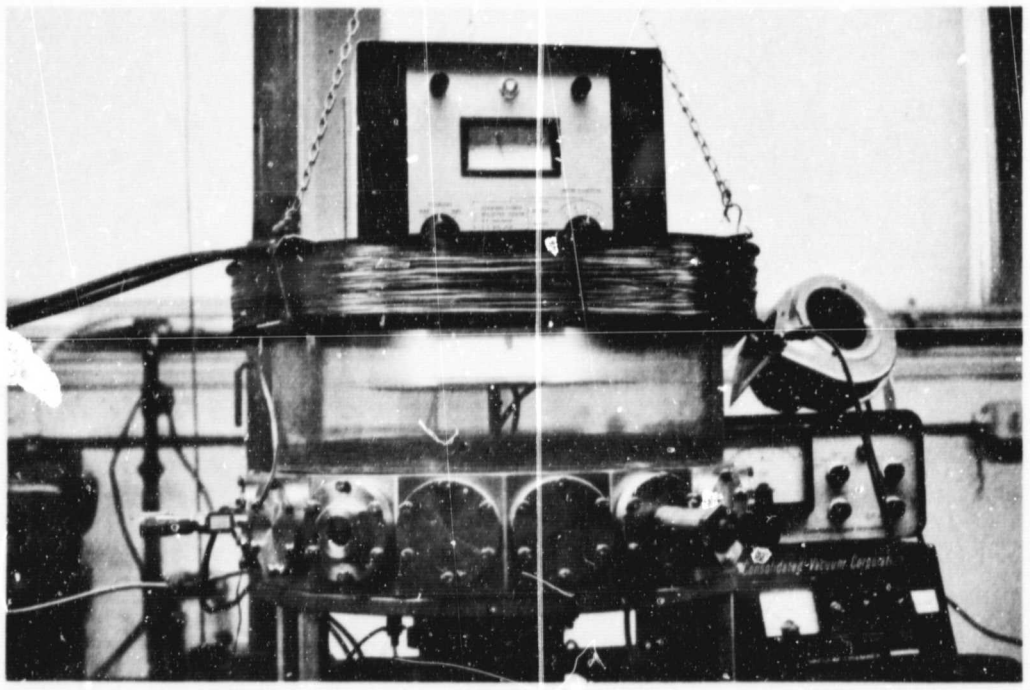


FIGURE 3. THIN FILM CAPACITOR FABRICATION IN PLASMA DEPOSITION CHAMBER. UNIT MOUNTED ON CVC VACUUM STAND (OIL DIFFUSION PUMP)

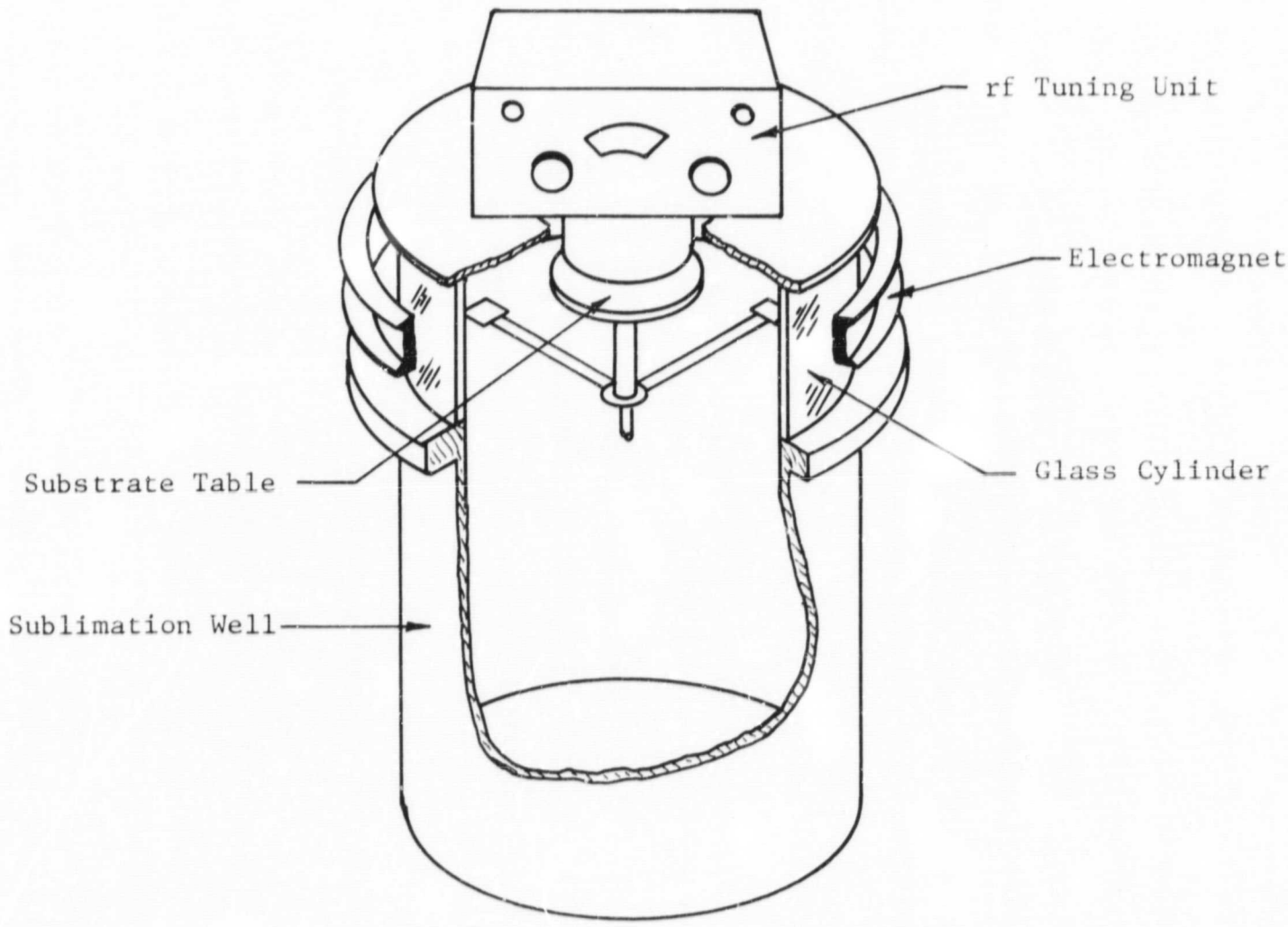


FIGURE 4. CUT-AWAY VIEW OF VACUUM SYSTEM AND SPUTTERING MODULE SHOWING SUBSTRATE TABLE AND SUPPORTS (ULTEK UHV FACILITY).

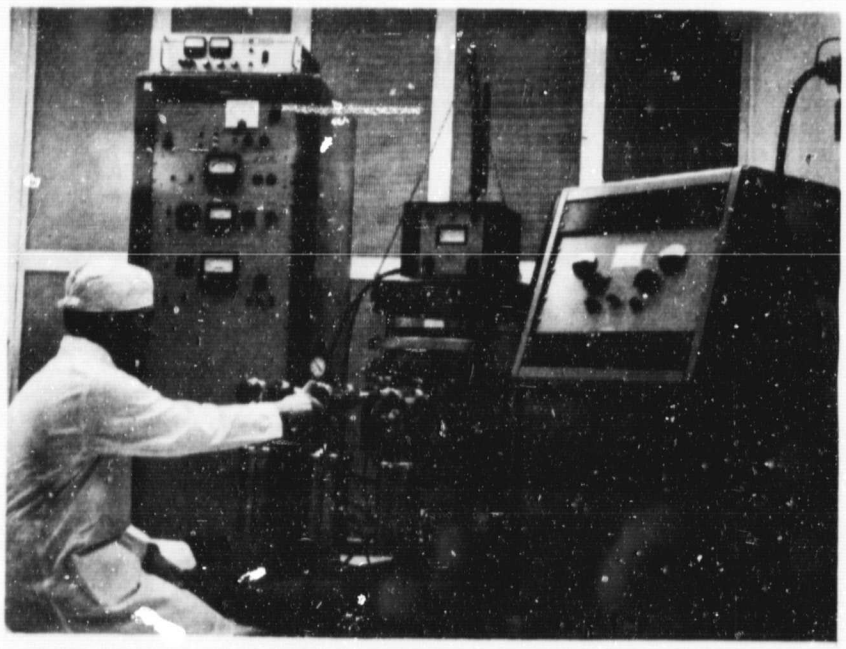


FIGURE 5. SPUTTERING SYSTEM FOR THIN FILM CAPACITOR DEVELOPMENT

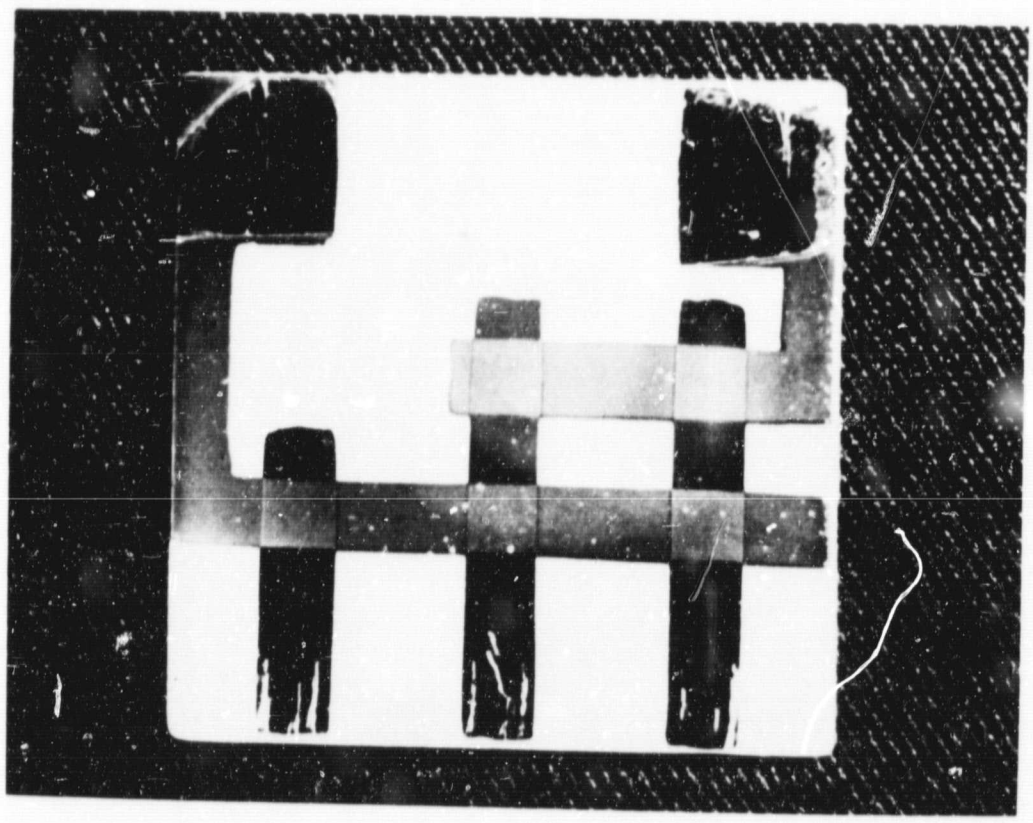


FIGURE 6. EXPERIMENTAL FIVE-CAPACITOR CONFIGURATION

Target-to-Substrate Distance: Curve a = 5.1 cm.
Curve b = 3.8 cm.

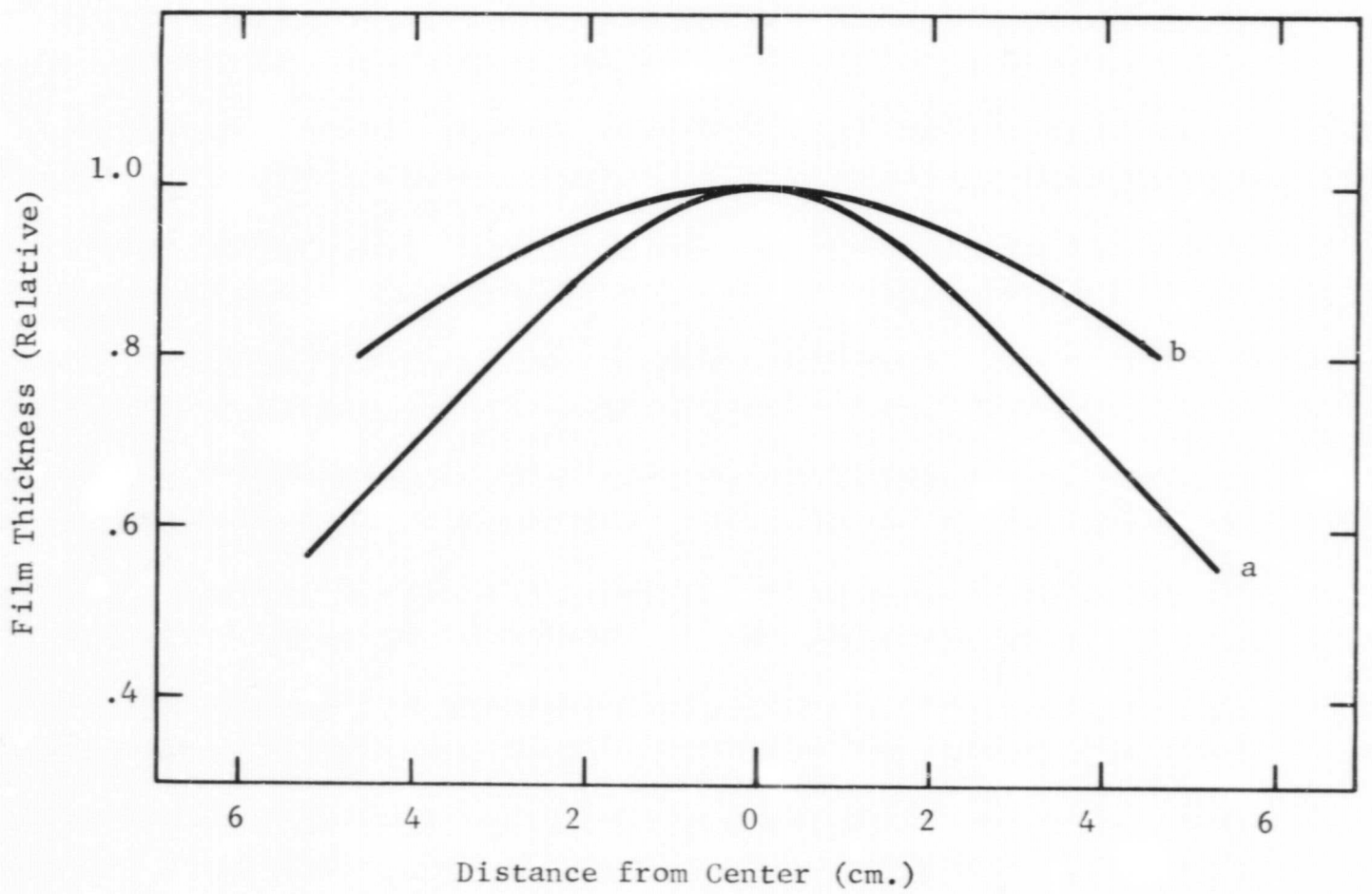


FIGURE 7. VARIATION IN SPUTTERED FILM THICKNESS ACROSS DEPOSITION SURFACE

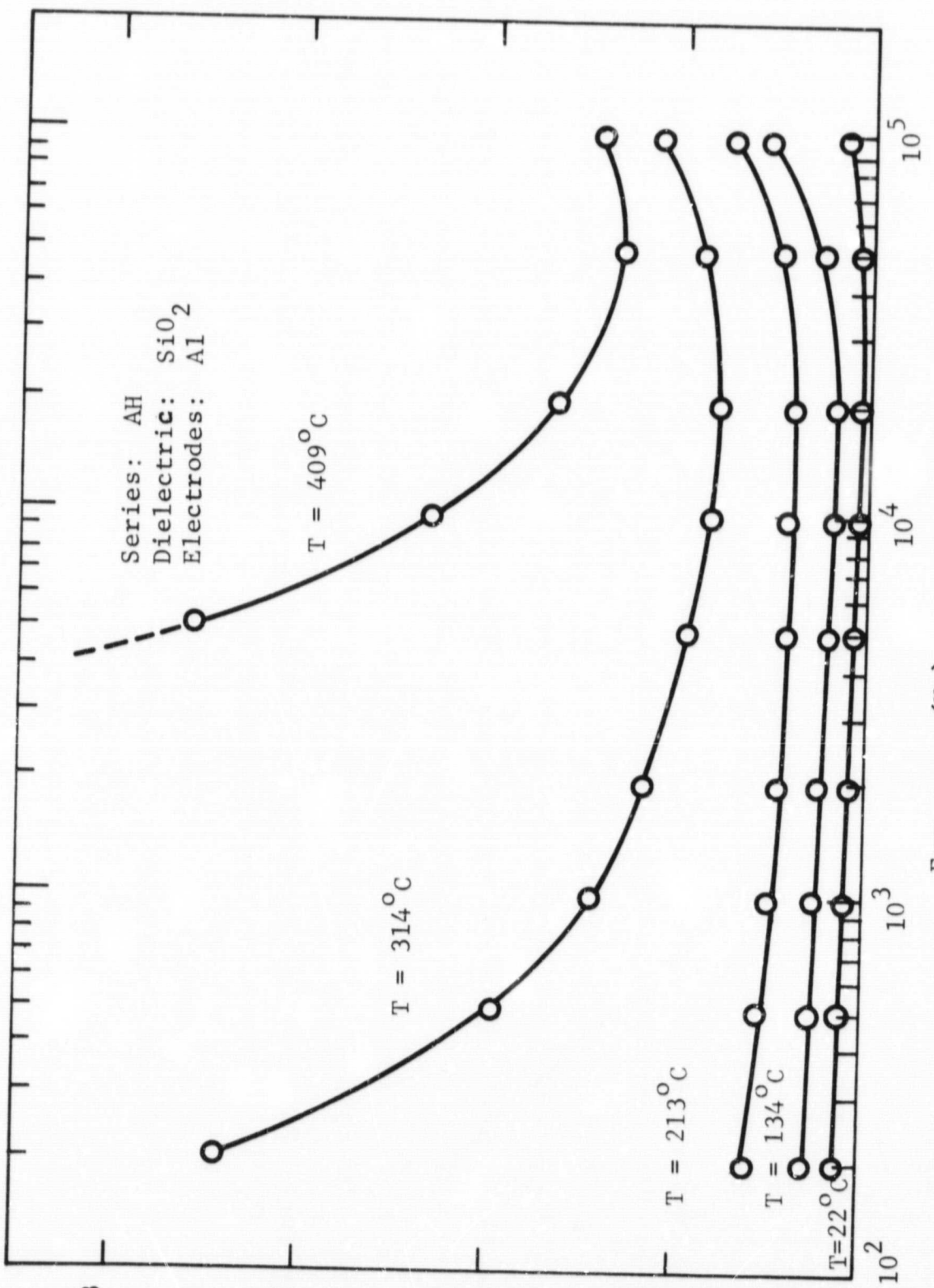


FIGURE 8. EFFECT OF TEMPERATURE ON CAPACITANCE VERSUS FREQUENCY RELATIONSHIP FOR Al-SiO_2 MULTILAYER CAPACITORS

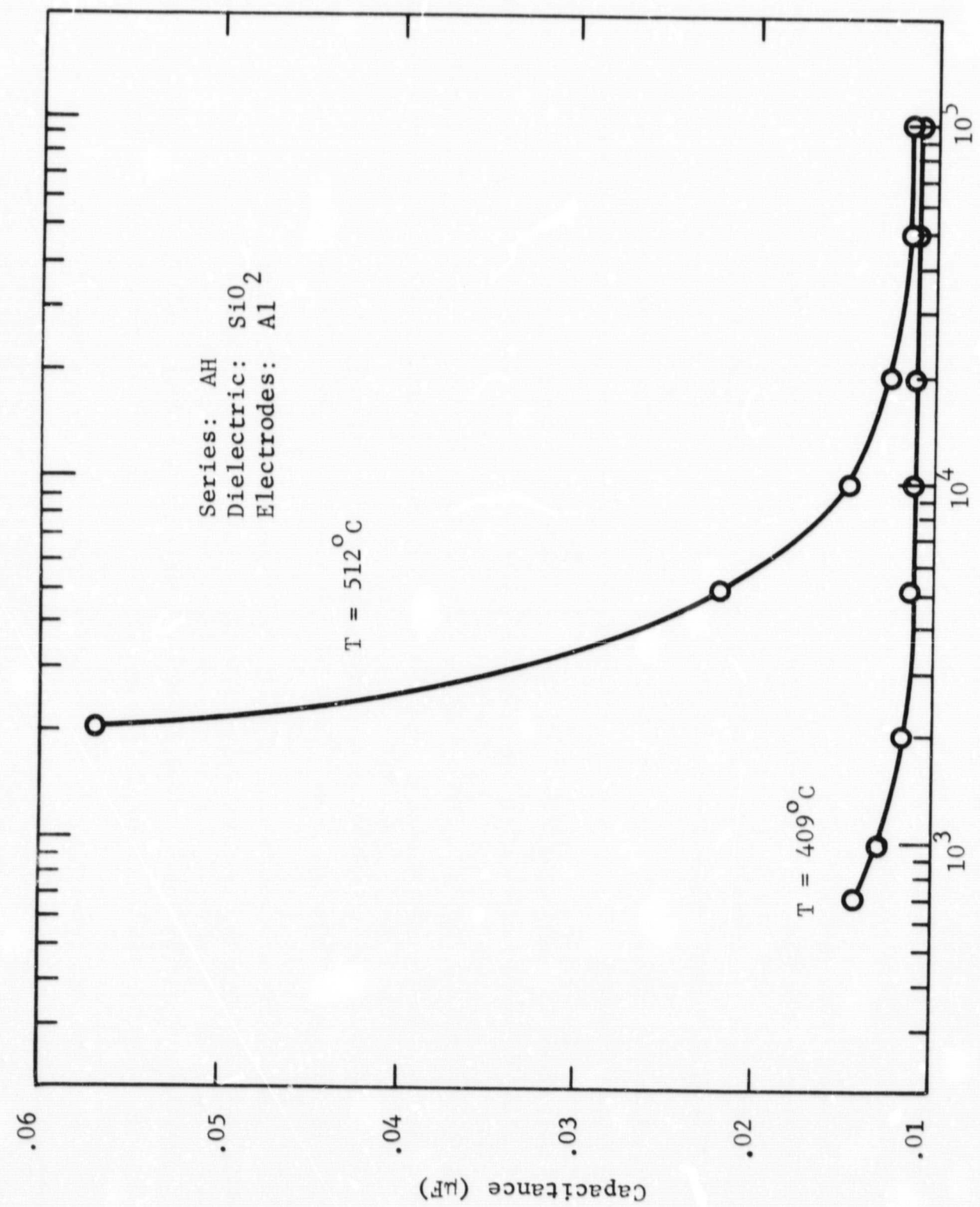


FIGURE 9. EFFECT OF TEMPERATURE ON CAPACITANCE VERSUS FREQUENCY RELATIONSHIP FOR Al-SiO_2 MULTILAYER CAPACITORS

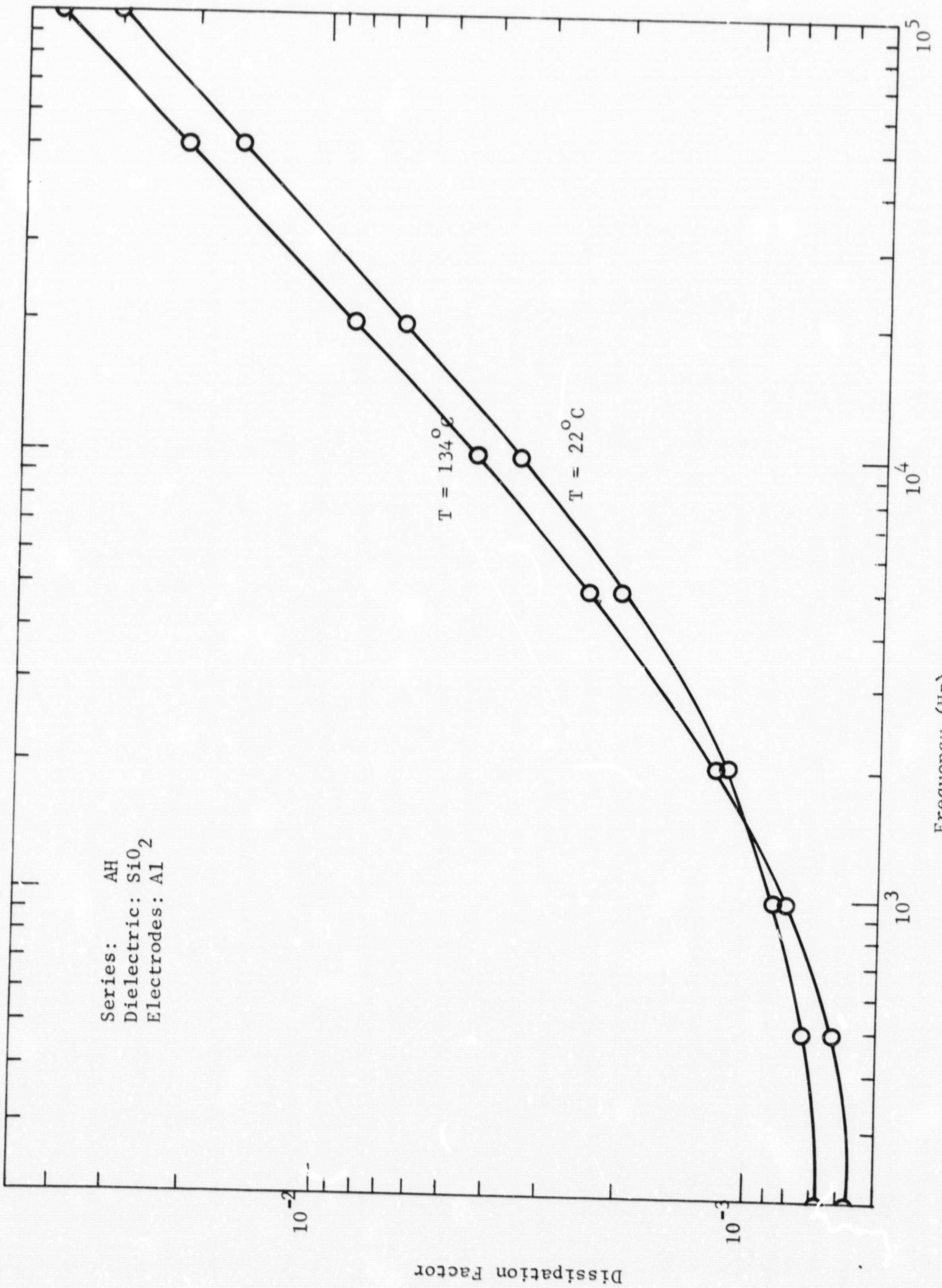


FIGURE 10. EFFECT OF FREQUENCY ON DISSIPATION FACTOR FOR Al-SiO_2 MULTILAYER CAPACITORS AT 22° and 134°C

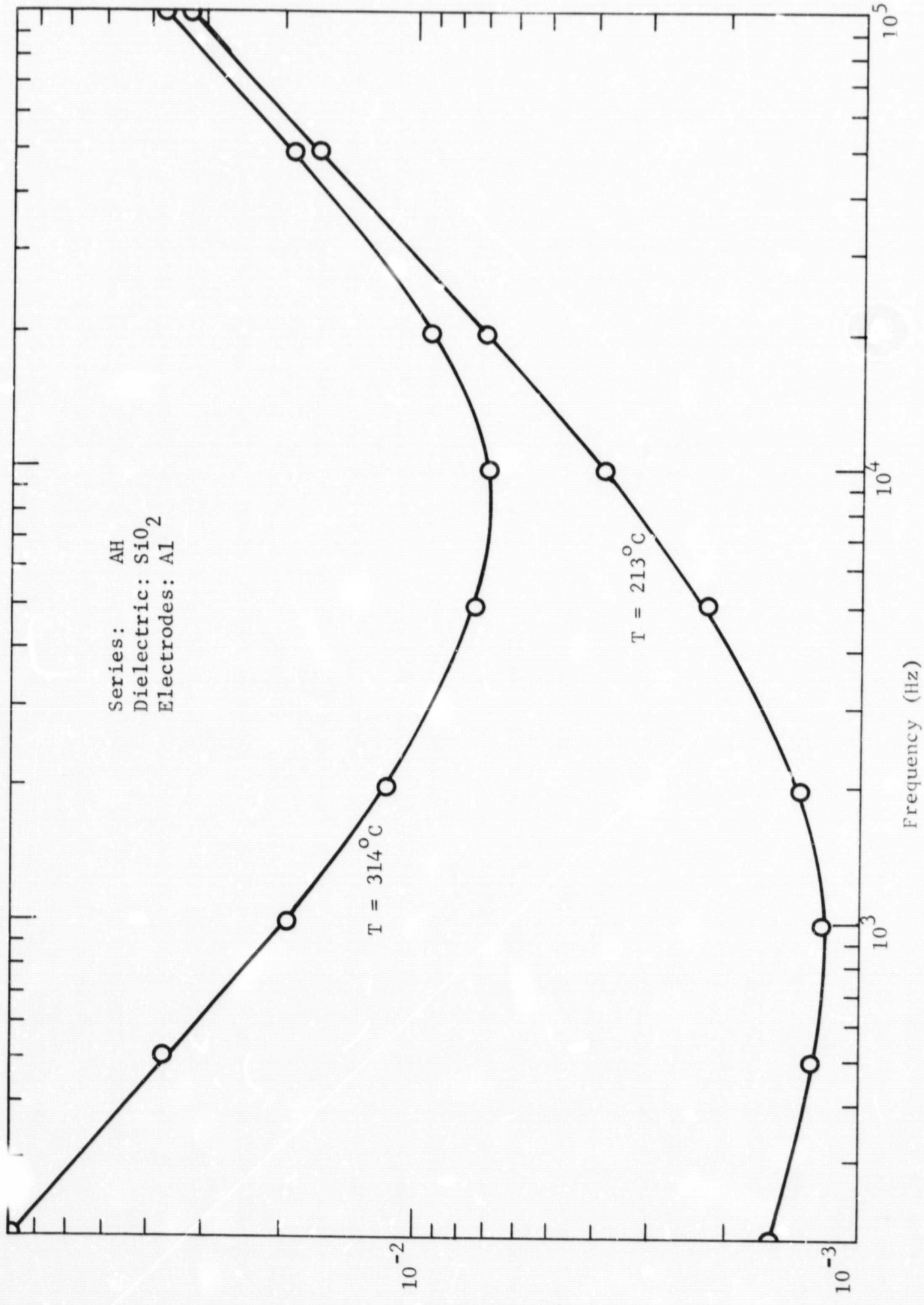


FIGURE 11. EFFECT OF FREQUENCY ON DISSIPATION FACTOR FOR Al-SiO_2 MULTILAYER CAPACITORS AT 213° and 314°C

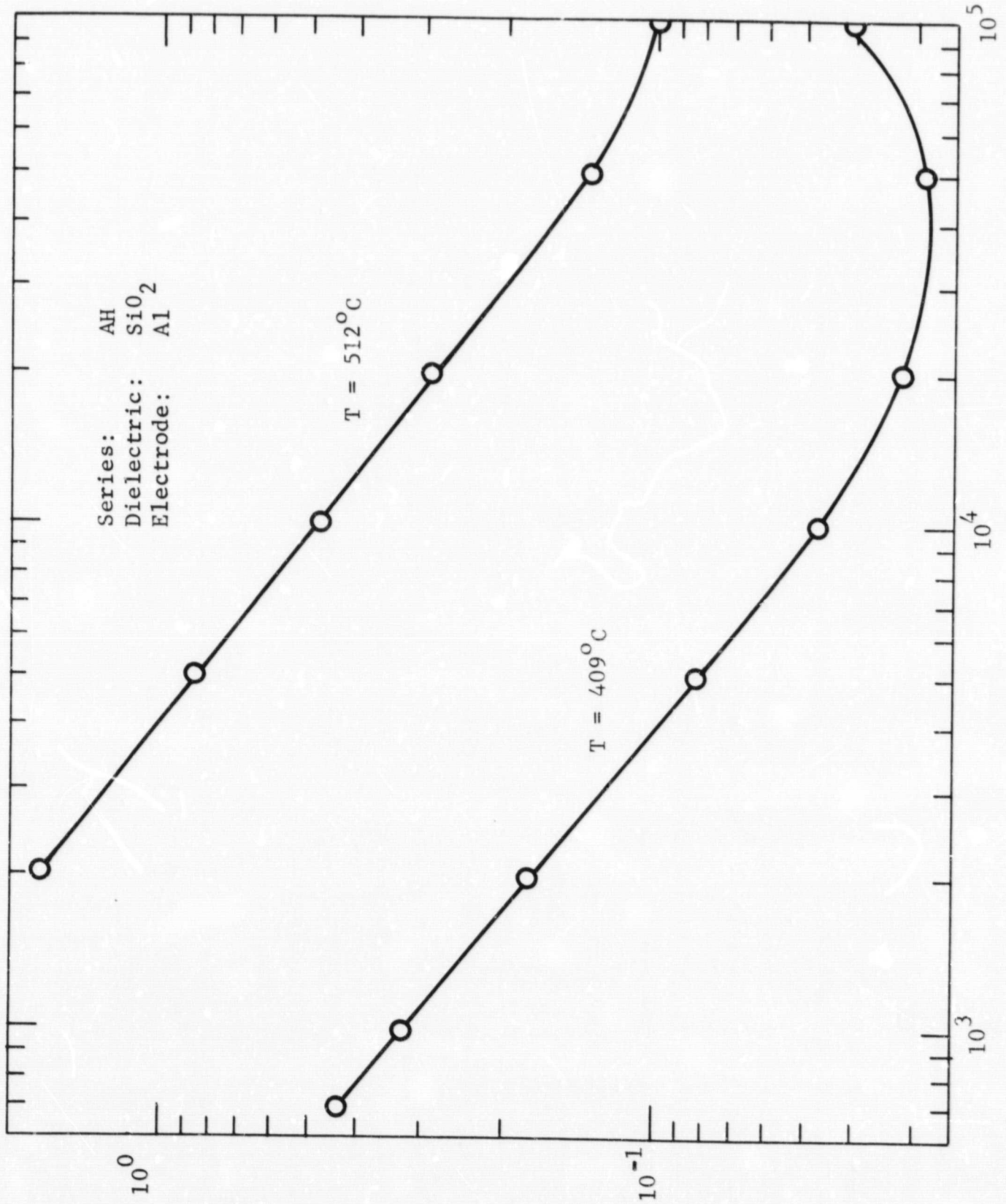


FIGURE 12. EFFECT OF FREQUENCY ON THE DISSIPATION FACTOR FOR Al-SiO_2 MULTILAYER CAPACITORS AT 409^o and 512^oC.

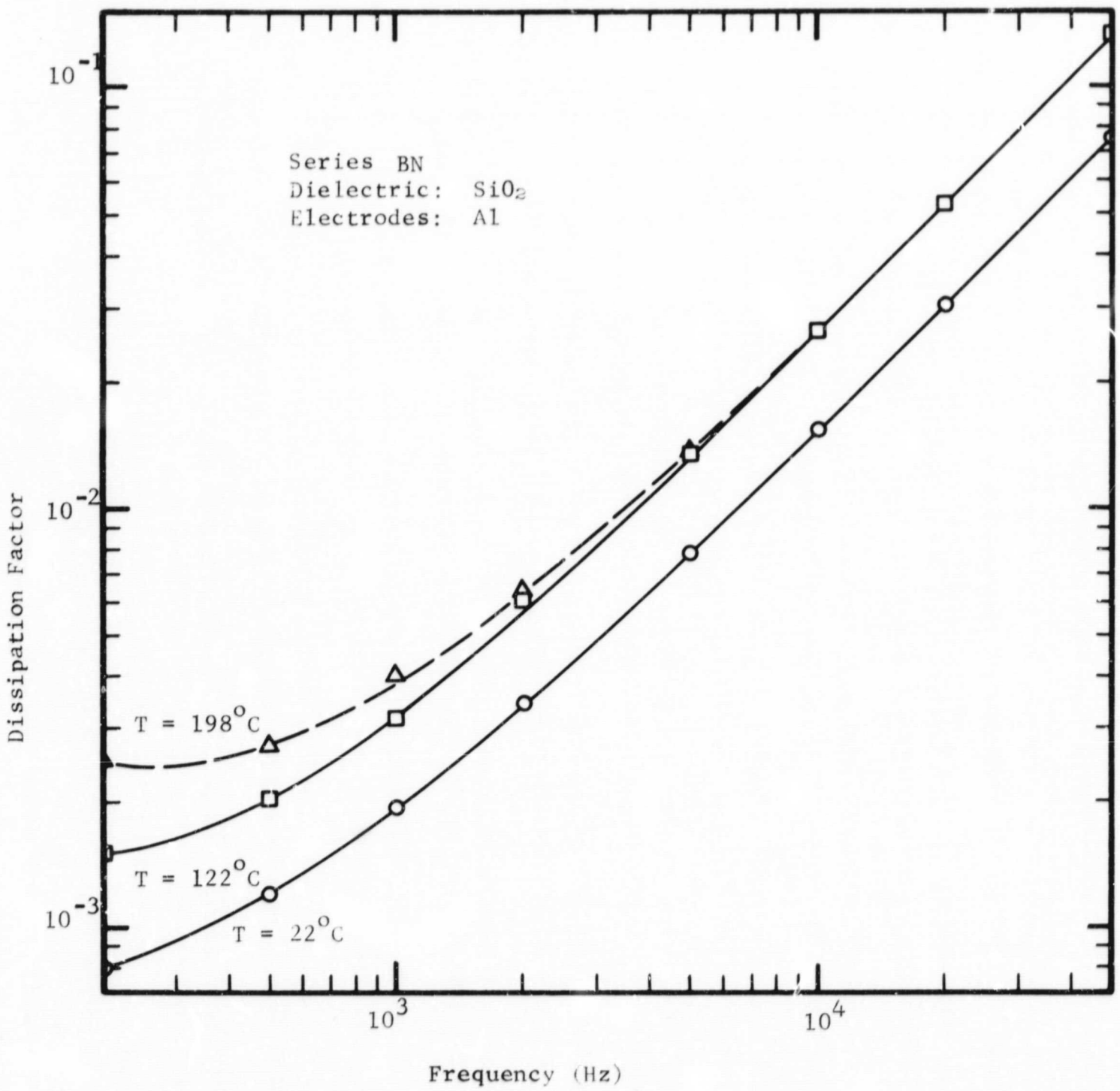


FIGURE 13. EFFECT OF FREQUENCY AND TEMPERATURE ON THE DISSIPATION FACTOR OF SERIES BN MULTILAYER CAPACITORS

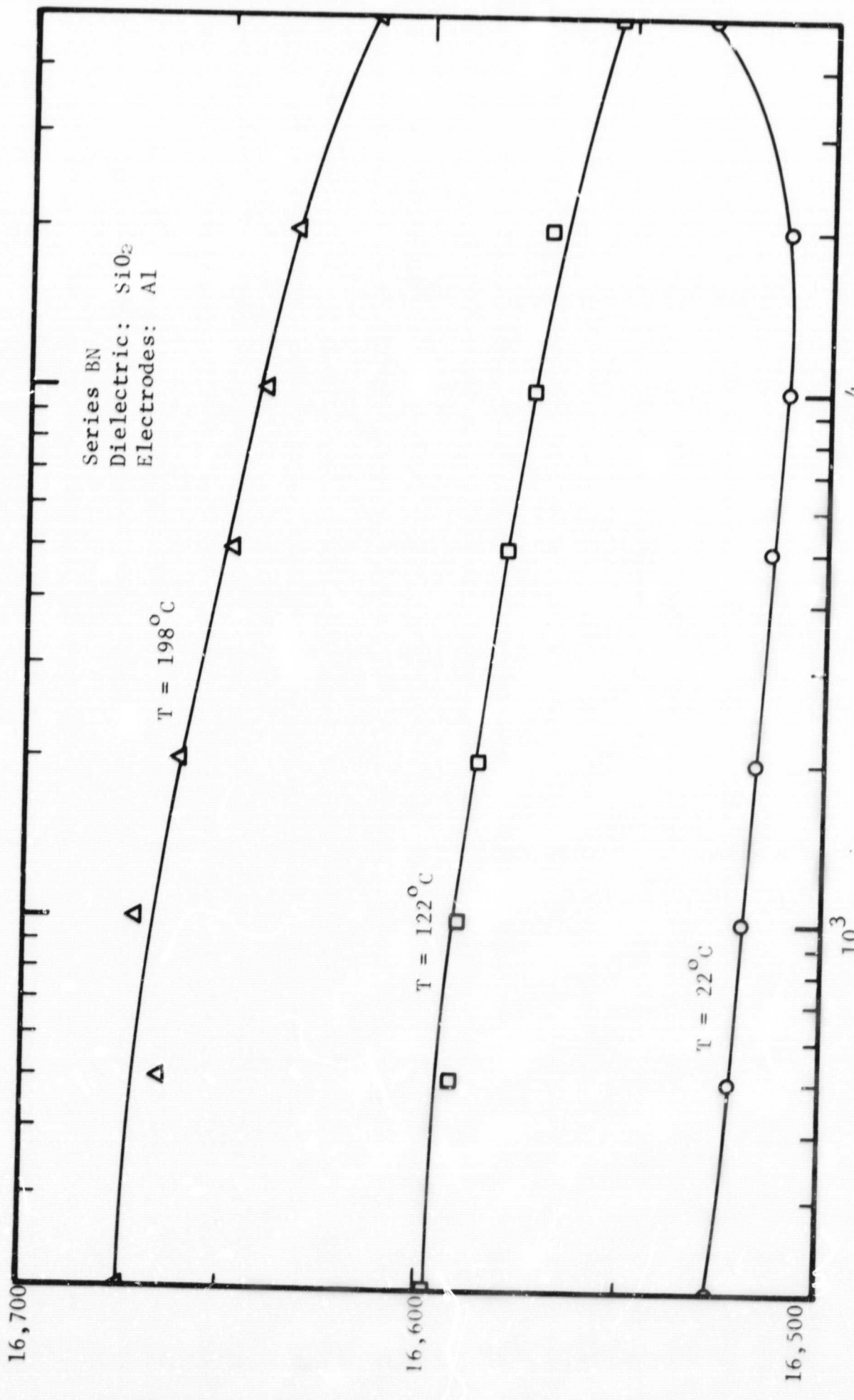


FIGURE 14. EFFECT OF FREQUENCY AND TEMPERATURE ON CAPACITANCE OF SERIES BN MULTILAYER CAPACITORS

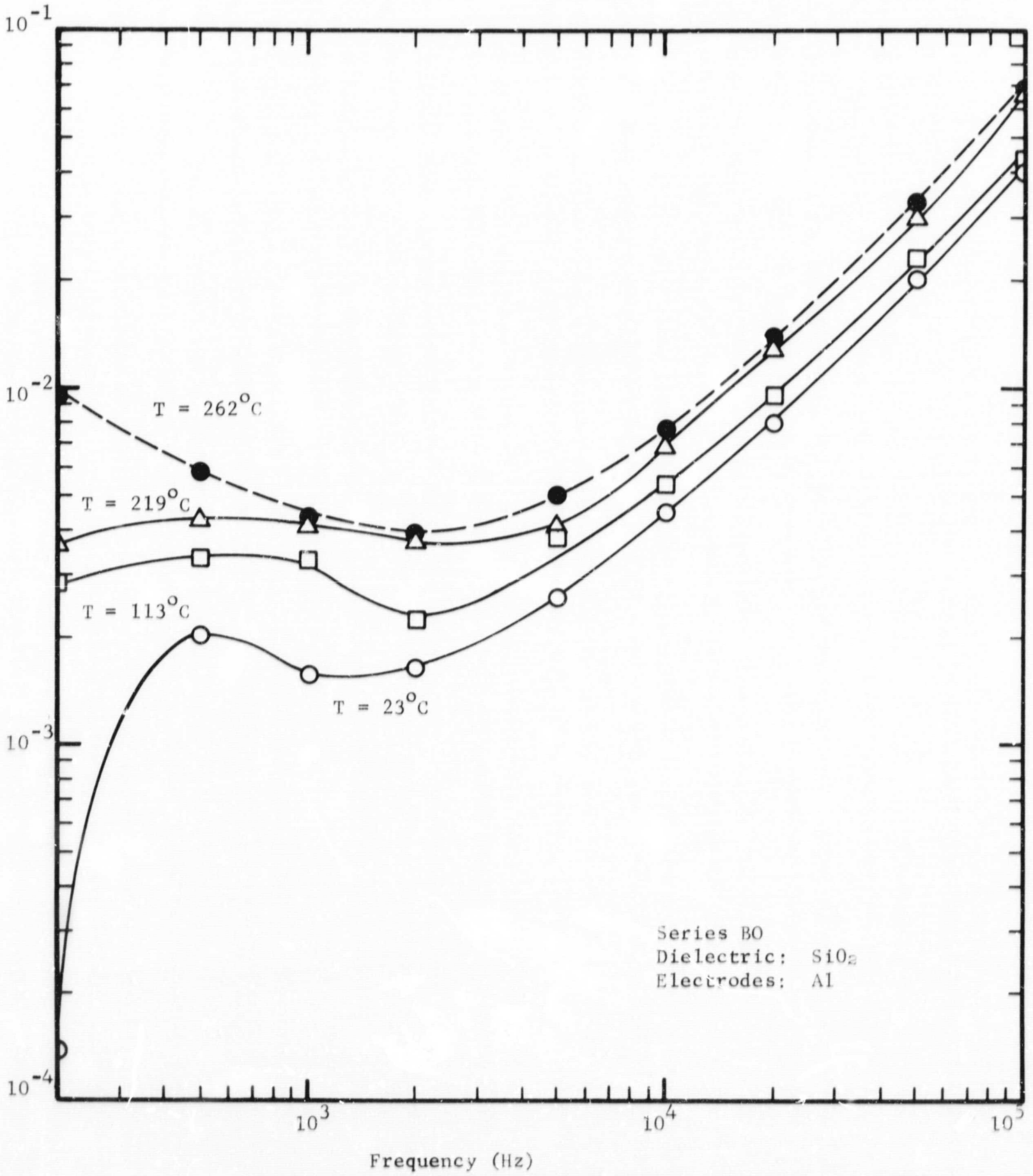


FIGURE 15. EFFECT OF FREQUENCY AND TEMPERATURE ON THE DISSIPATION FACTOR OF SERIES BO THIN FILM CAPACITORS

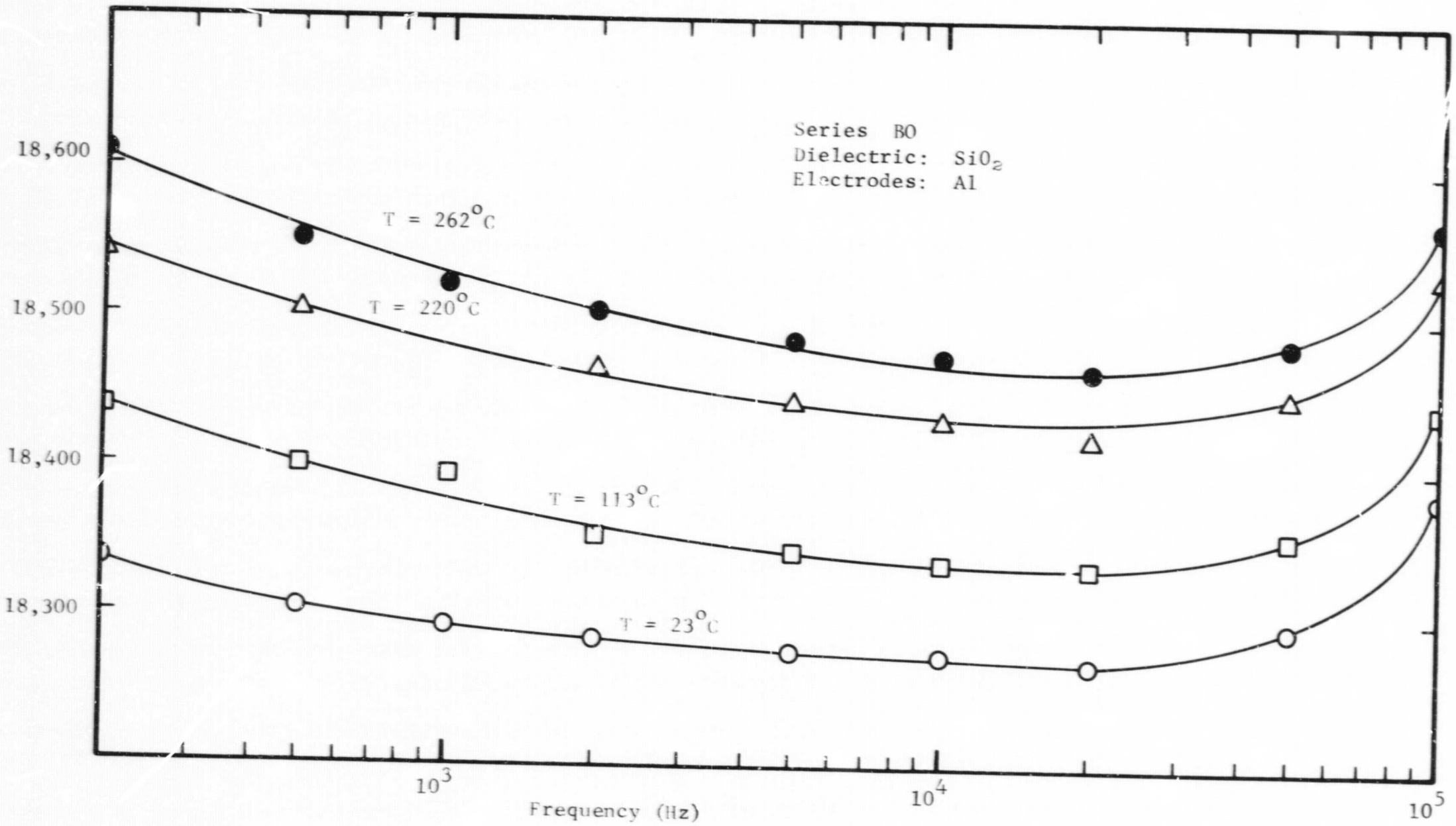


FIGURE 16. EFFECT OF FREQUENCY AND TEMPERATURE ON CAPACITANCE OF SERIES BO THIN FILM CAPACITORS

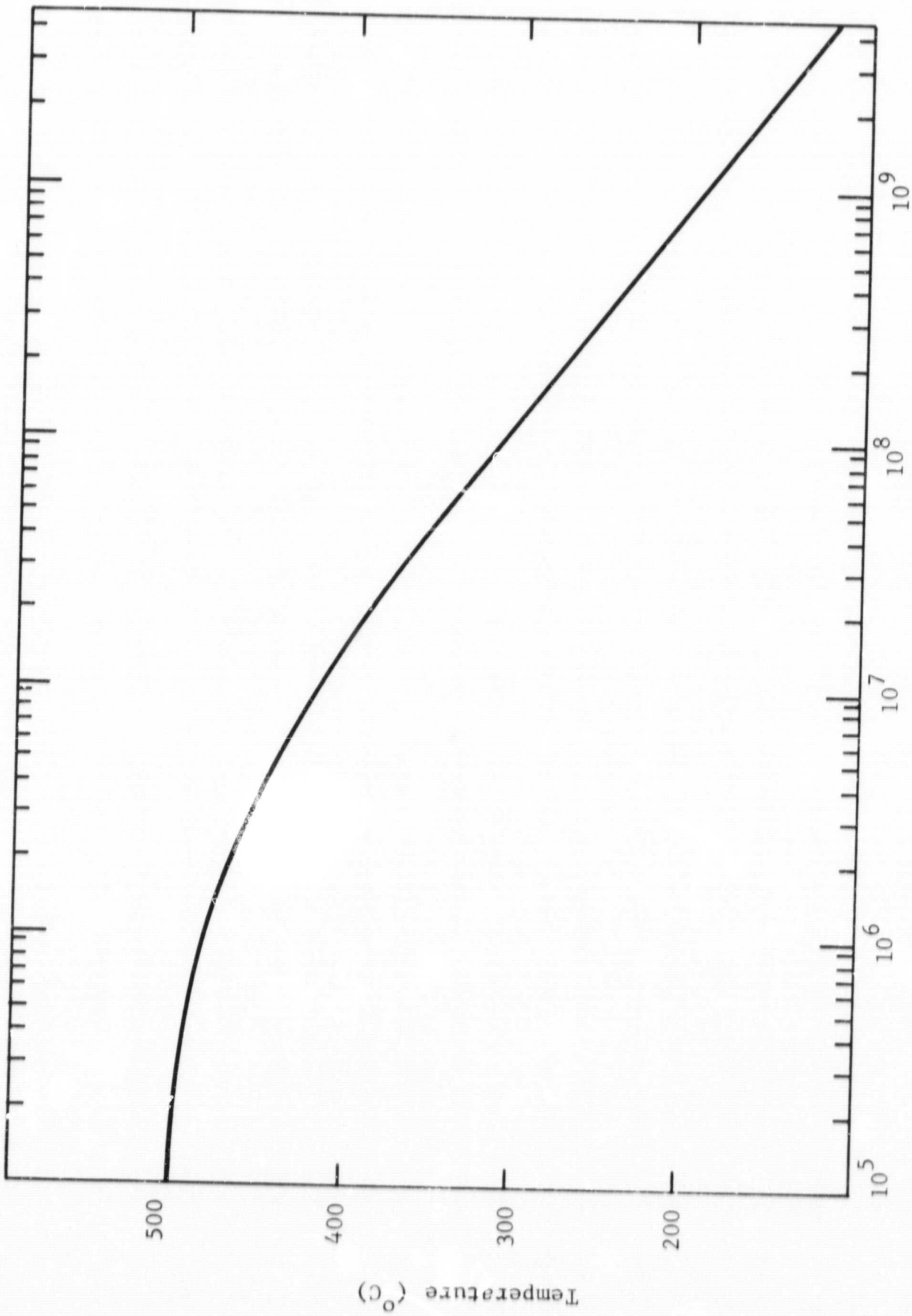


FIGURE 17. EFFECT OF TEMPERATURE ON dc RESISTANCE FOR Al-SiO_2 MULTILAYER SYSTEM

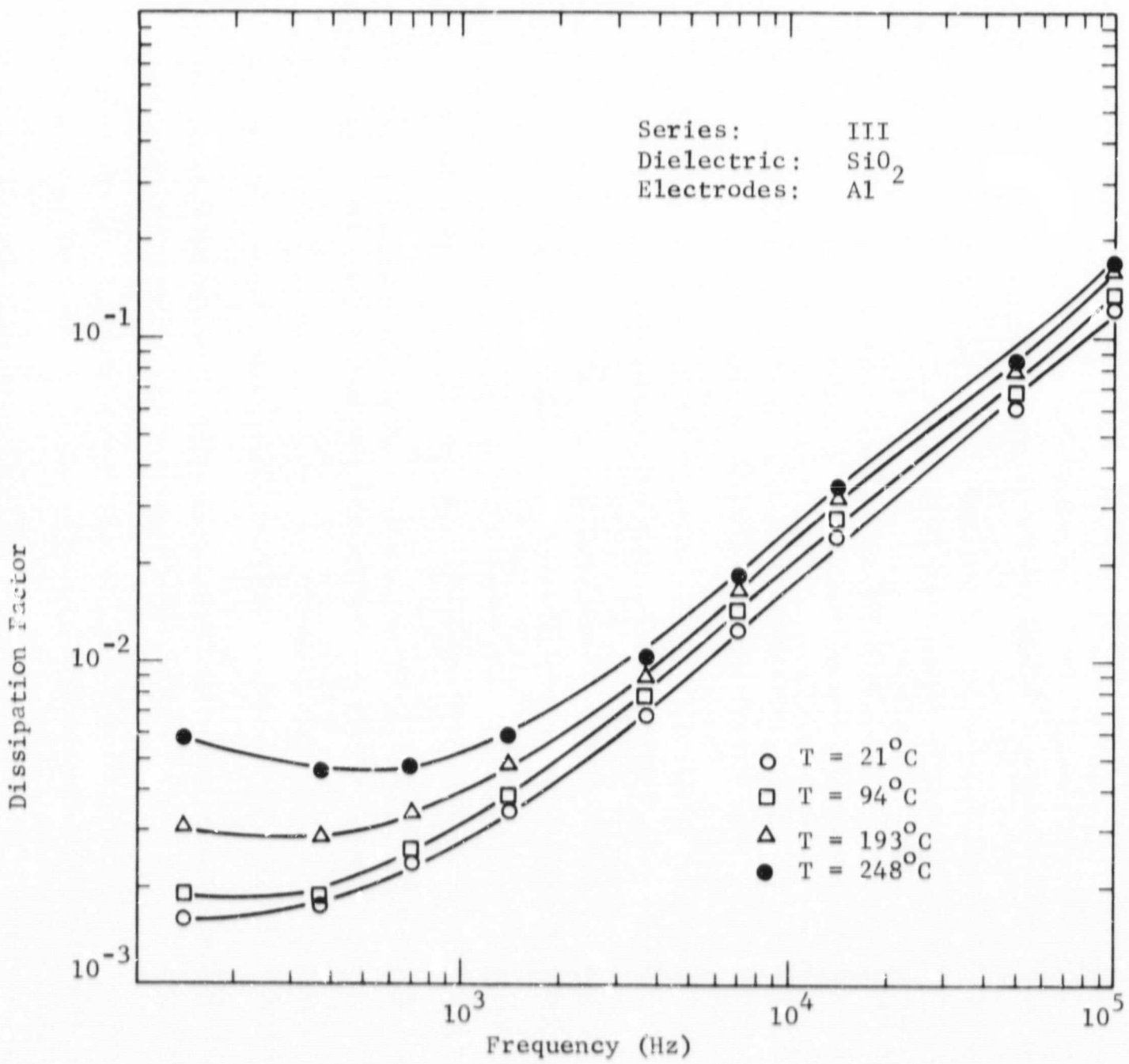


FIGURE 18. EFFECT OF TEMPERATURE AND FREQUENCY ON DISSIPATION FACTOR OF SERIES III THIN FILM CAPACITORS

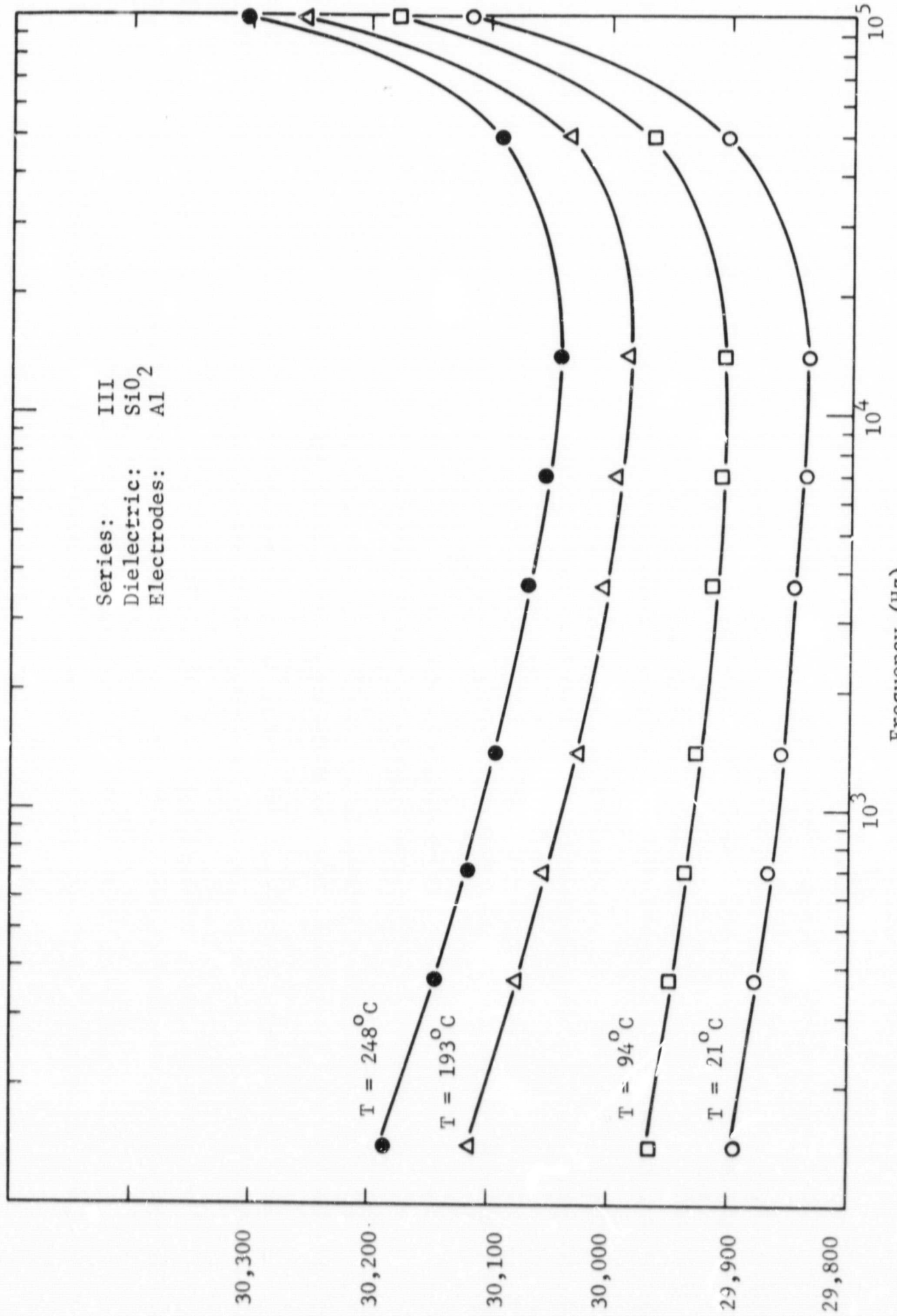


FIGURE 19. EFFECT OF TEMPERATURE AND FREQUENCY ON CAPACITANCE OF SERIES III THIN FILM CAPACITORS.

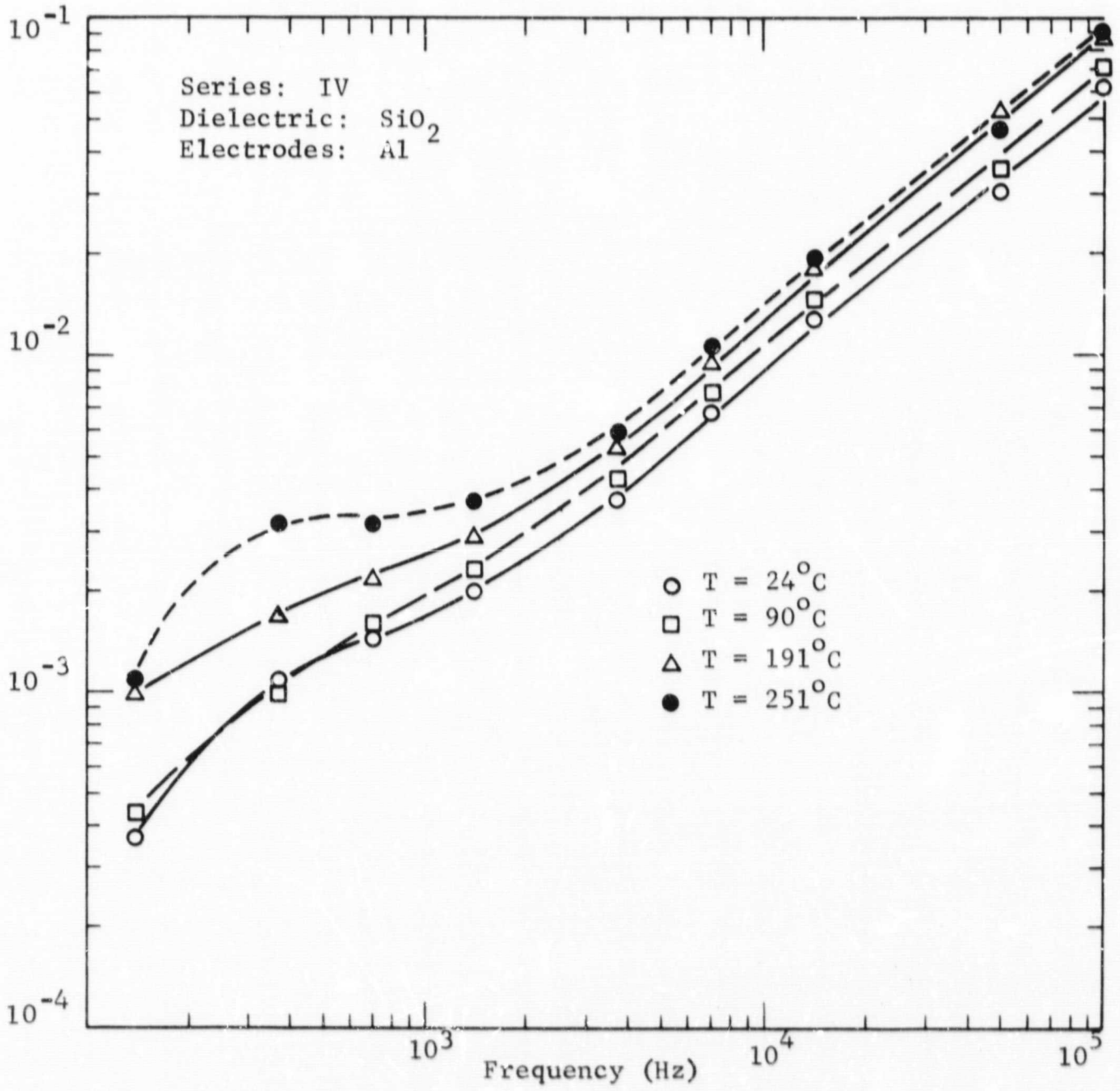


FIGURE 20. EFFECT OF FREQUENCY AND TEMPERATURE ON THE DISSIPATION FACTOR OF SERIES IV THIN FILM CAPACITORS.

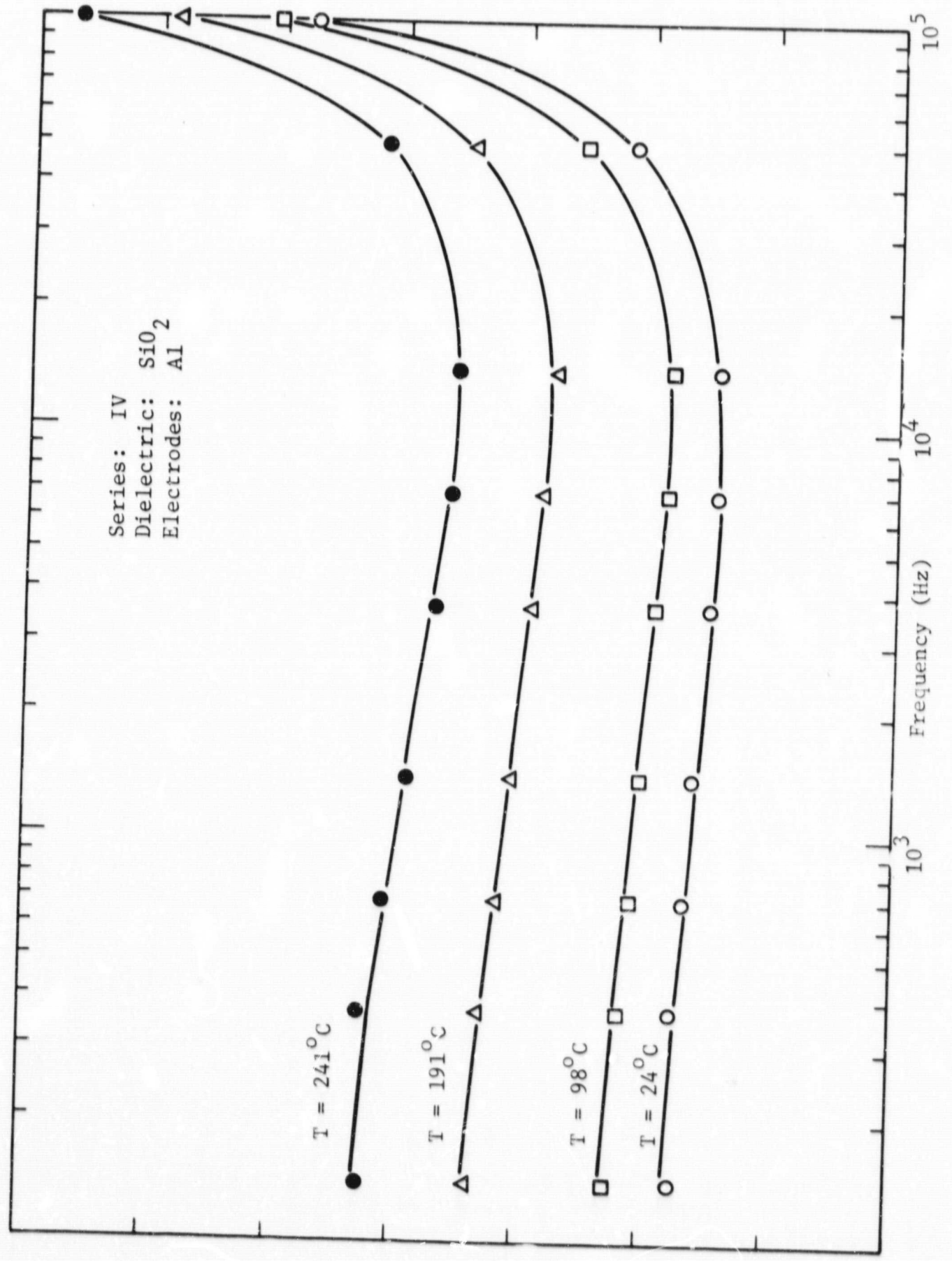


FIGURE 21. EFFECT OF FREQUENCY AND TEMPERATURE ON CAPACITANCE OF SERIES IV THIN FILM CAPACITORS.

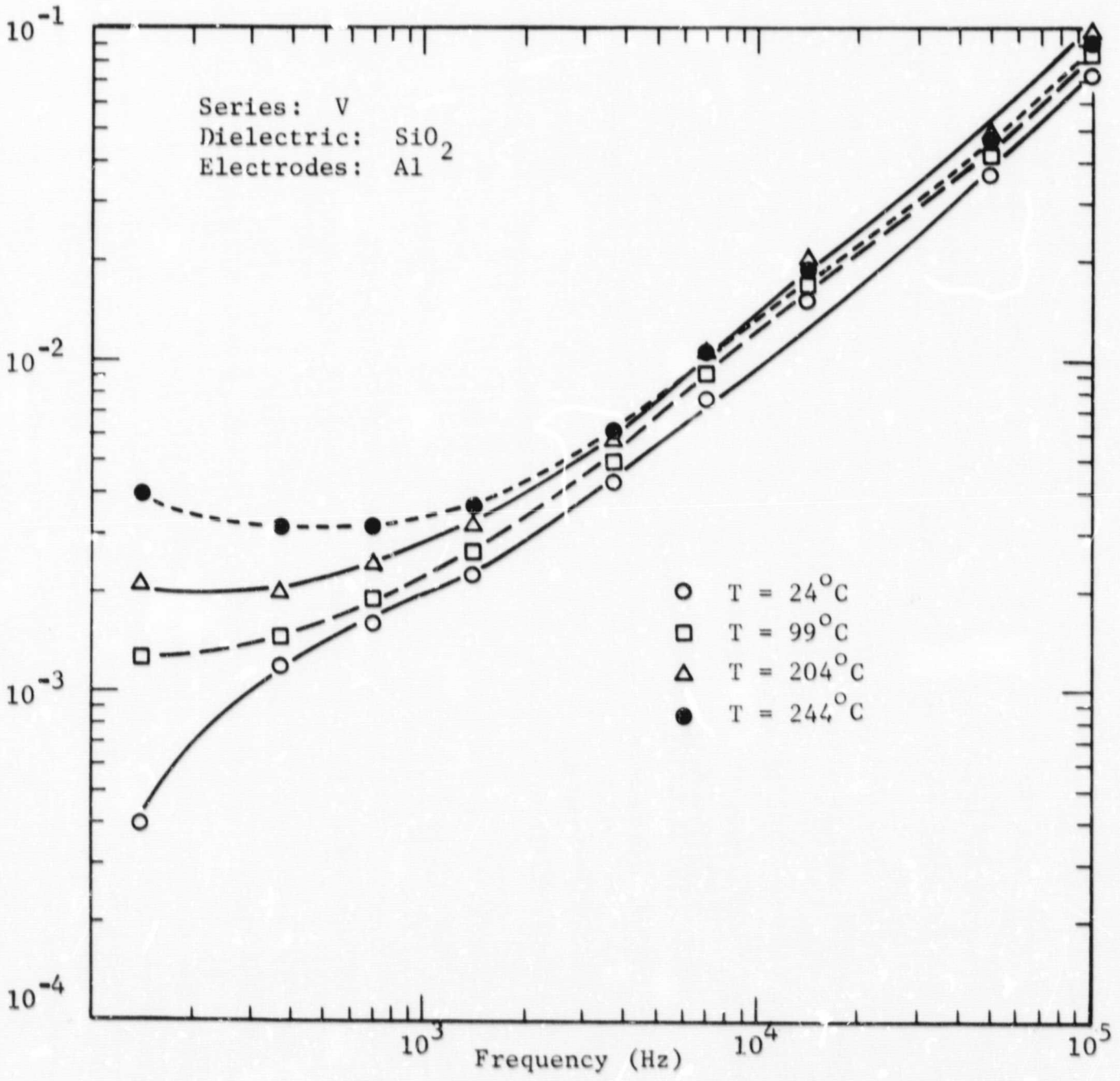


FIGURE 22. EFFECT OF FREQUENCY AND TEMPERATURE ON DISSIPATION FACTOR FOR SERIES V THIN FILM CAPACITORS.

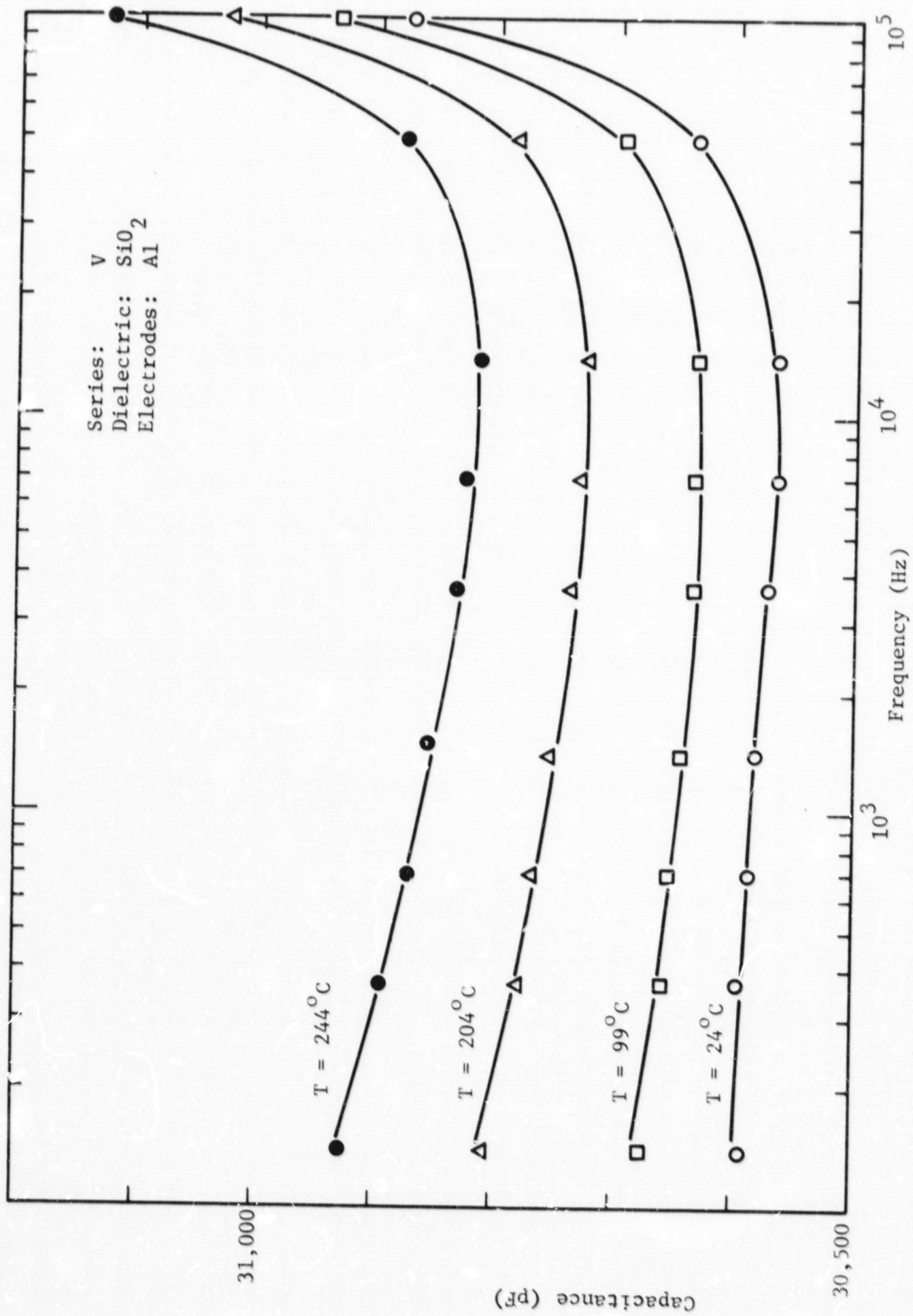
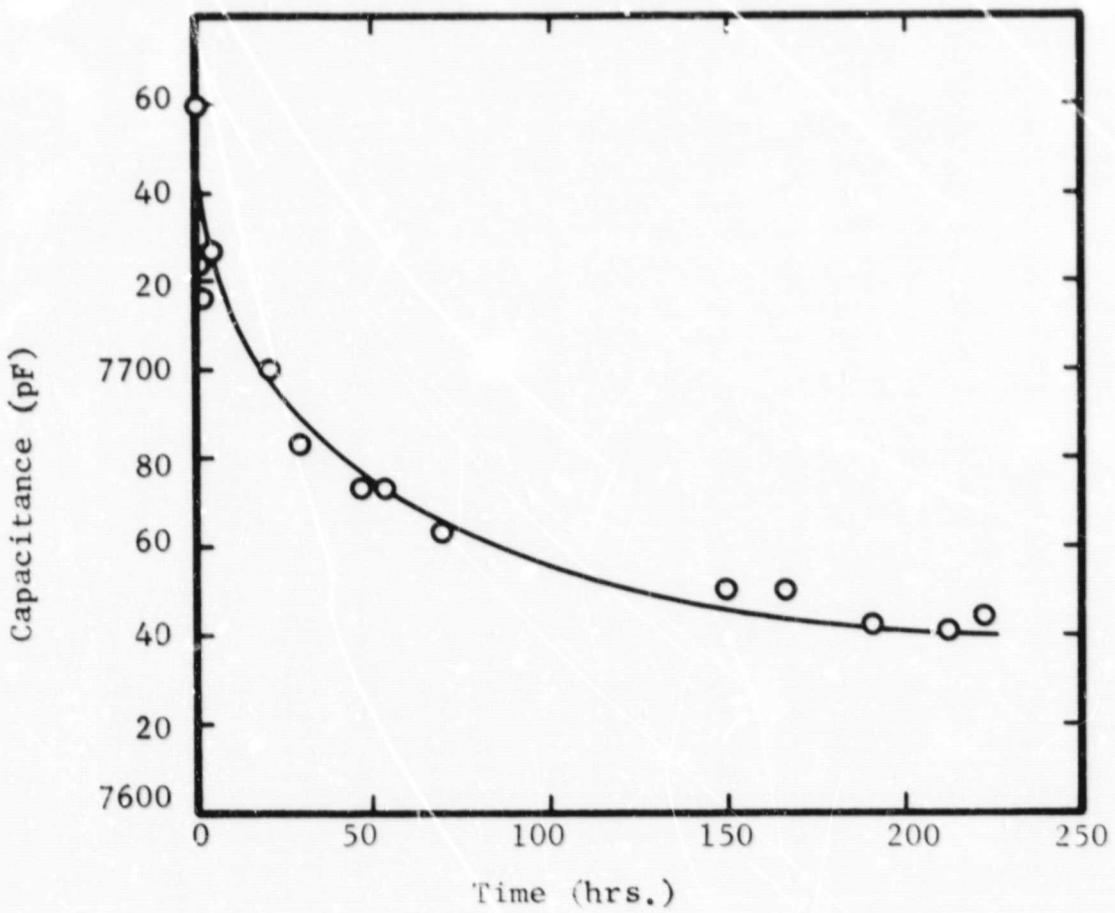


FIGURE 23. EFFECT OF FREQUENCY AND TEMPERATURE ON CAPACITANCE OF SERIES V THIN FILM CAPACITORS.



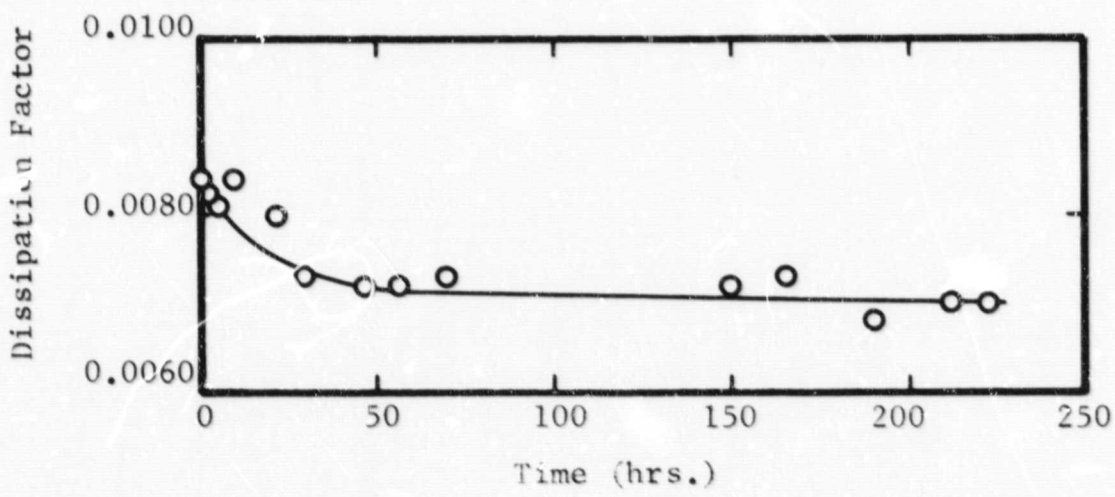
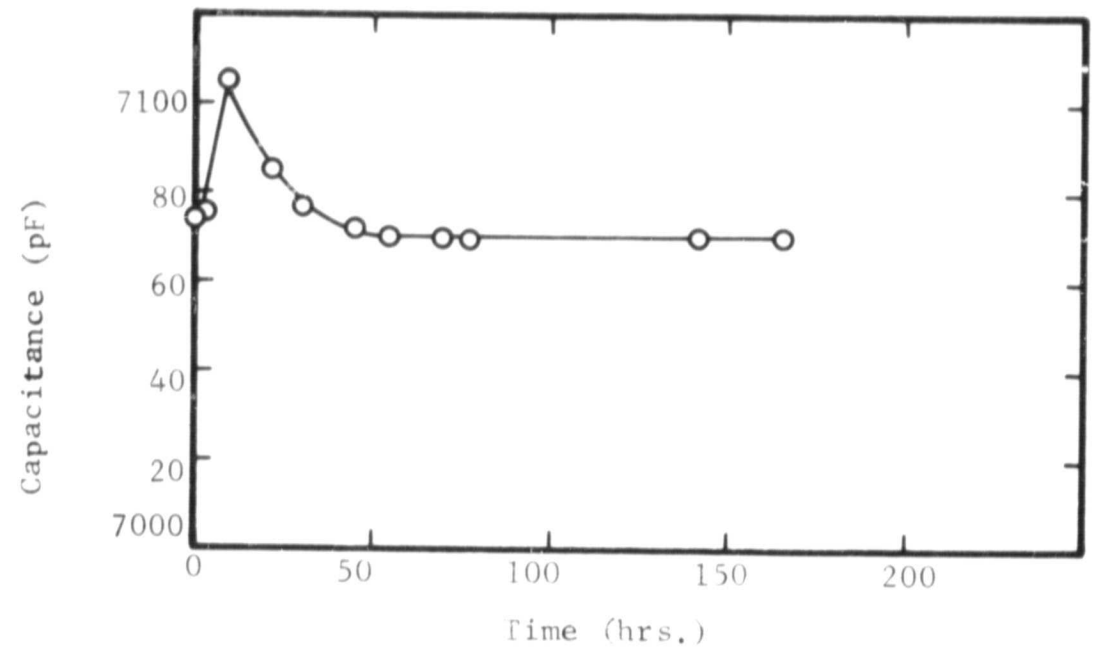


FIGURE 24. LIFE TEST CHARACTERISTICS AT 250°C OF Al-Al_2O_3-Al CAPACITORS WITH 3700 Å DIELECTRIC



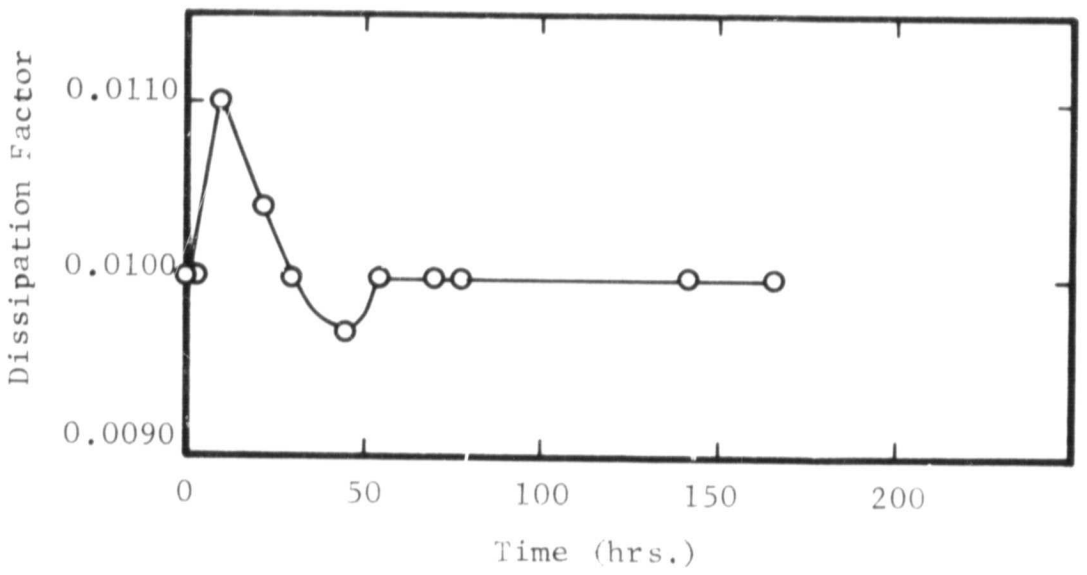
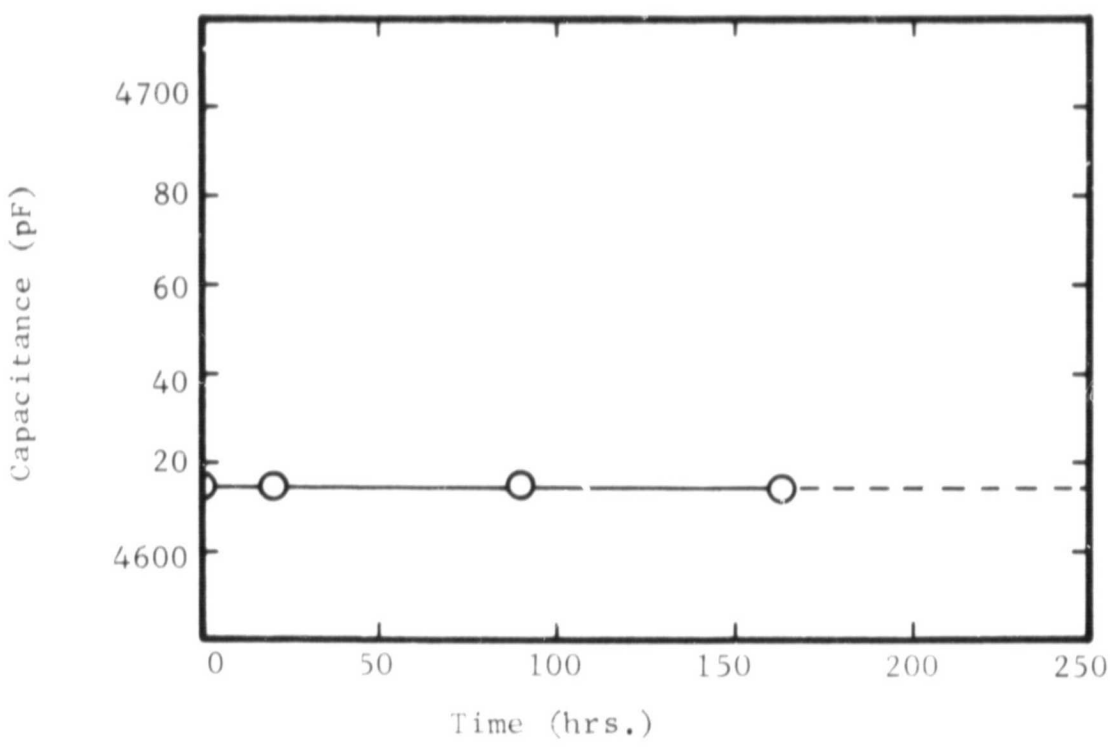


FIGURE 25. LIFE TEST CHARACTERISTICS AT 250°C OF Al-Al_2O_3-Al CAPACITORS WITH 2850 Å DIELECTRIC



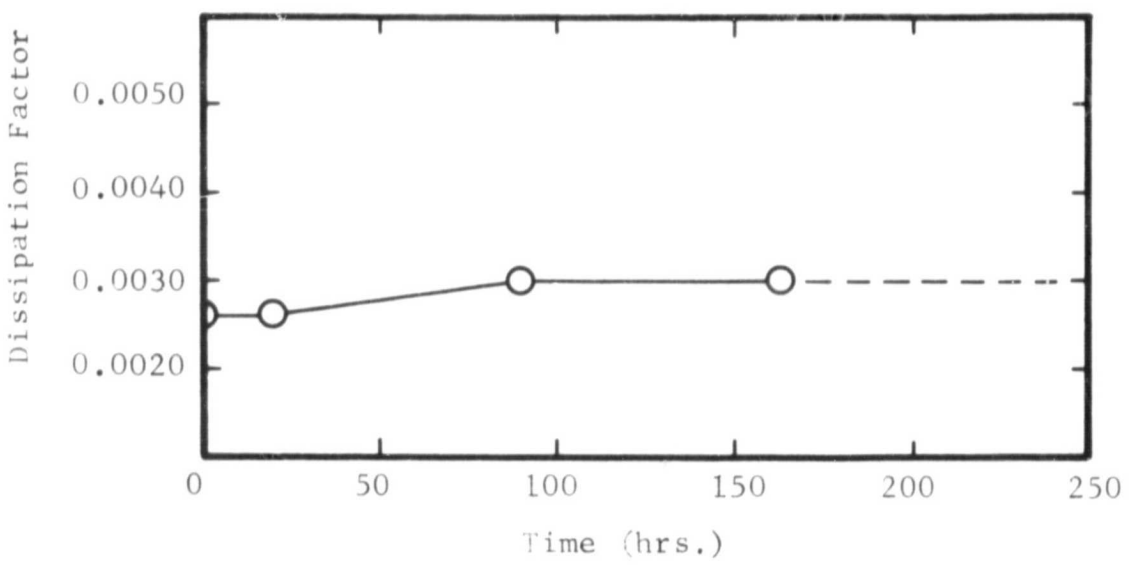


FIGURE 26. . LIFE TEST CHARACTERISTICS AT 250°C OF Al-SiO_2-Al CAPACITORS WITH 3440 Å DIELECTRIC

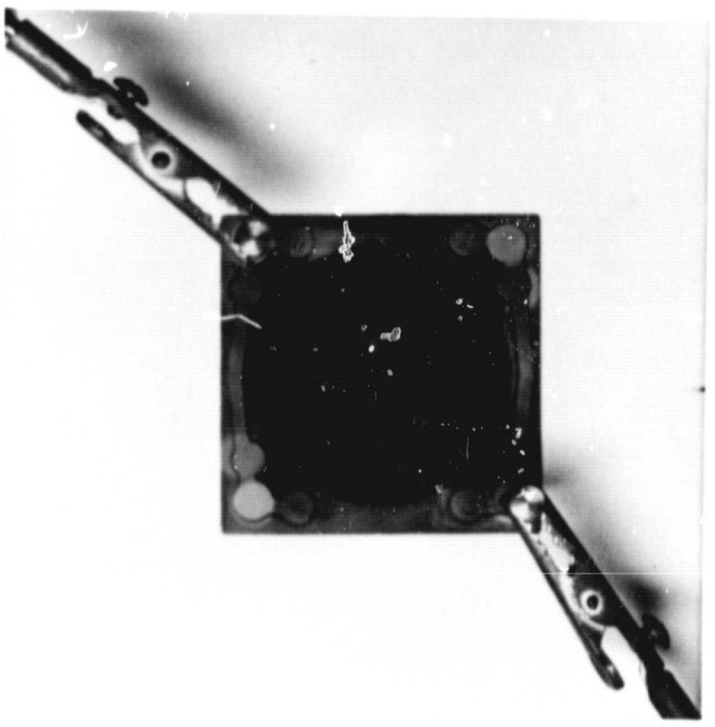


FIGURE 27. COLOR PROFILE OF LARGE Ta-Al_2O_3 CAPACITOR AFTER LIQUID CRYSTAL TREATMENT.

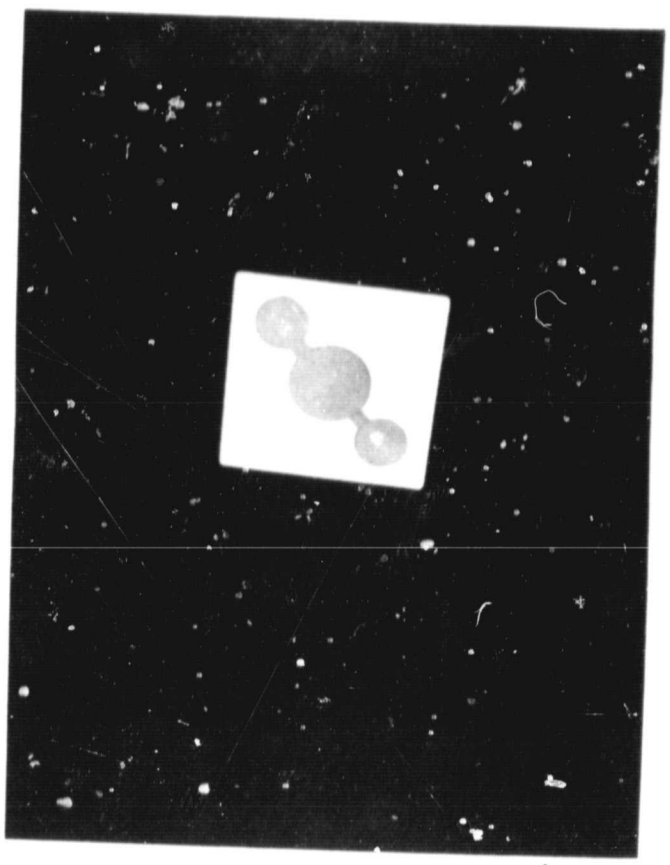
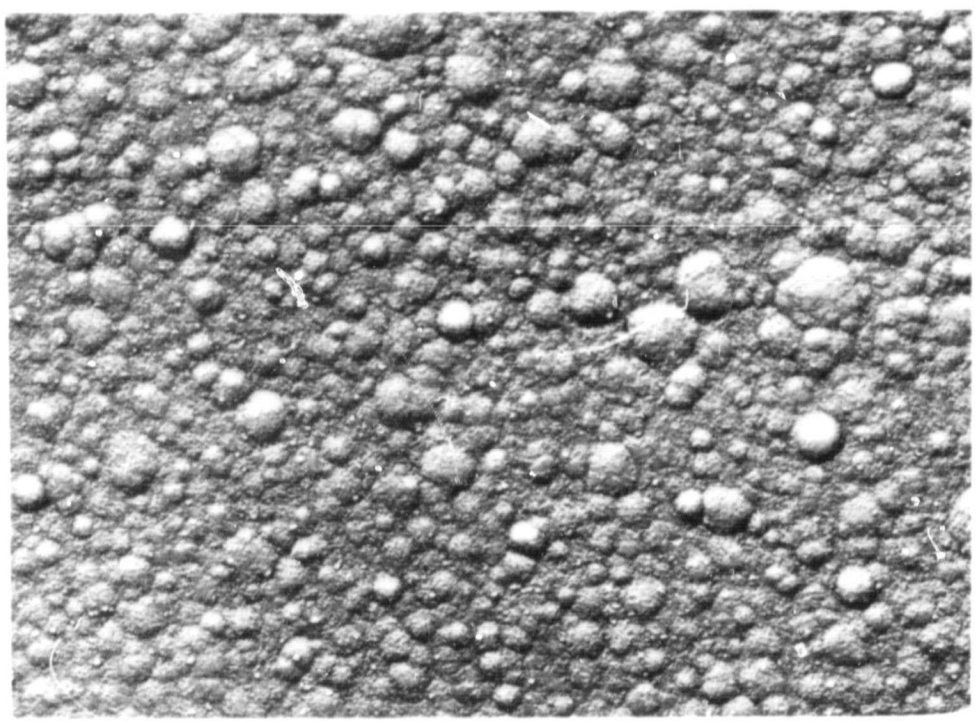


FIGURE 28. EXPERIMENTAL CAPACITOR ELEMENT USING PZT-4 TYPE DIELECTRIC AND ALUMINUM ELECTRODE

500X



7000X

FIGURE 29. SURFACE AND MICROSTRUCTURAL CHARACTERIZATION OF Al-SiO_2-Al CAPACITOR (TYPICAL ELECTRODE SECTION)

APPENDIX

NEW TECHNOLOGY APPENDIX

"After a diligent review of the work performed under this contract, no new innovation, discovery, improvement, or invention was conceived worthy of special reporting at the time of publication."

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JUNE 1969

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