General Disclaimer

One or more of the Following Statements may affect this Document

- This document has been reproduced from the best copy furnished by the organizational source. It is being released in the interest of making available as much information as possible.

- This document may contain data, which exceeds the sheet parameters. It was furnished in this condition by the organizational source and is the best copy available.

- This document may contain tone-on-tone or color graphs, charts and/or pictures, which have been reproduced in black and white.

- This document is paginated as submitted by the original source.

- Portions of this document are not fully legible due to the historical nature of some of the material. However, it is the best reproduction available from the original submission.

Westinghouse

ELECTRIC CORPORATION

NASA CR 108484

Final Report

For

Task 6 - Development of MNOS Technology

NAS 9-6636

WEC GO HS - 51431

March 20, 1970

Prepared by

WESTINGHOUSE DEFENSE AND SPACE CENTER
Systems Development Division
Baltimore, Maryland 21203

For

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
Manned Spacecraft Center
Houston, Texas 77058

Table of Contents

1.0 Introduction and Summary

The objective of this task was to develop pyrolytic silicon nitride-on-silicon dioxide technology and to correlate the deposition parameters with physical and electrical characteristics of metal-nitride-oxide-semiconductor (MNOS) structures (amplifying and memory).

The theory and physical models of charge storage in MNOS structures is described in terms of the Fowler-Nordheim tunneling currents, Poole-Frenkel field enhanced thermal currents, ohmic currents and ionic currents. Two limiting cases based on the presence or absence of deep traps at the nitride-oxide interface are shown to have significant effects on the magnitude of the flatband shift and charge retention.

The experiments are all limited to thermally grown silicon dioxide in oxygen with temperature and partial pressures as variables. It has been shown that on ⟨100⟩ silicon that the data extrapolates to an initial oxide thickness X_i of 65 Å. The most significant experiments showed that there are large differences in both oxidation rate and conductivity caused by the presence of diffused boron regions. The conclusion is that then thermal oxides should not be used on p channel MNOS transistors because of the anomolous behavior produced.

From the transient analysis and computer aided calculations it has been shown that the charging time and retention is a predictable and reproducible phenomena. Flatband shifts of about 8 volts for ±55 volts, 10 microsec pulses have been achieved on n channel transistors and correlated with the theory. Retention decay rates of 0.3 to 0.5 v/decade have been measured which indicate that the retention is poorer than for other oxide types. To show that much faster charging times may be achieved, thin oxide - thin nitride n channel structures,

were built that exhibited a 2 volt shift with $\pm$ 20 volt, 100 nanosec pulses.

From a consideration of the optimum conditions for nitride-oxide passivated structures it has been determined that thin oxides with thicker nitrides provide maximum transconductance and minimum flatband voltage shifts if precautions are taken to limit the applied fields to less than 2×10^6 v/cm. Other more conservative combinations are possible that permit larger fields to be applied.

The use of MNOS transistors in memory systems is described. A four bit breadboard was delivered to demonstrate the memory operation.

2.0 TECHNICAL DISCUSSION

2.1 Theory and Physical Models

2.1.1 Charge Storage in MNOS Devices

The storage of charge within Metal-Nitride-Oxide-Semiconductor (MNOS) structures is dependent on the difference in current density of the two insulators. The oxide current density has been shown to be mainly governed by tunneling (Fowler-Nordheim effect)[1,2] at the silicon-oxide or nitride-oxide interface while the nitride current density has been shown to be mainly governed by field enhanced thermal exitation of charge trapped within the bulk of the material.[3] (Poole-Frenkel effect)

2.1.2 Limiting Cases

Two limiting-case physical models have been presented in the literature to explain the observed features of MNOS charge storage memory devices. In the first[4,5], the current through the insulators is affected by deep traps located near the nitride-oxide interface as shown by the schematic band diagram shown in figure 1. In the second[6,7], the deep traps are assumed to be negligable in density such that they have little affect on the insulator currents.

To illustrate these differences several simplified extreme cases are listed in Table 1 for applied electric fields less than the point at which the flatband voltage saturates.

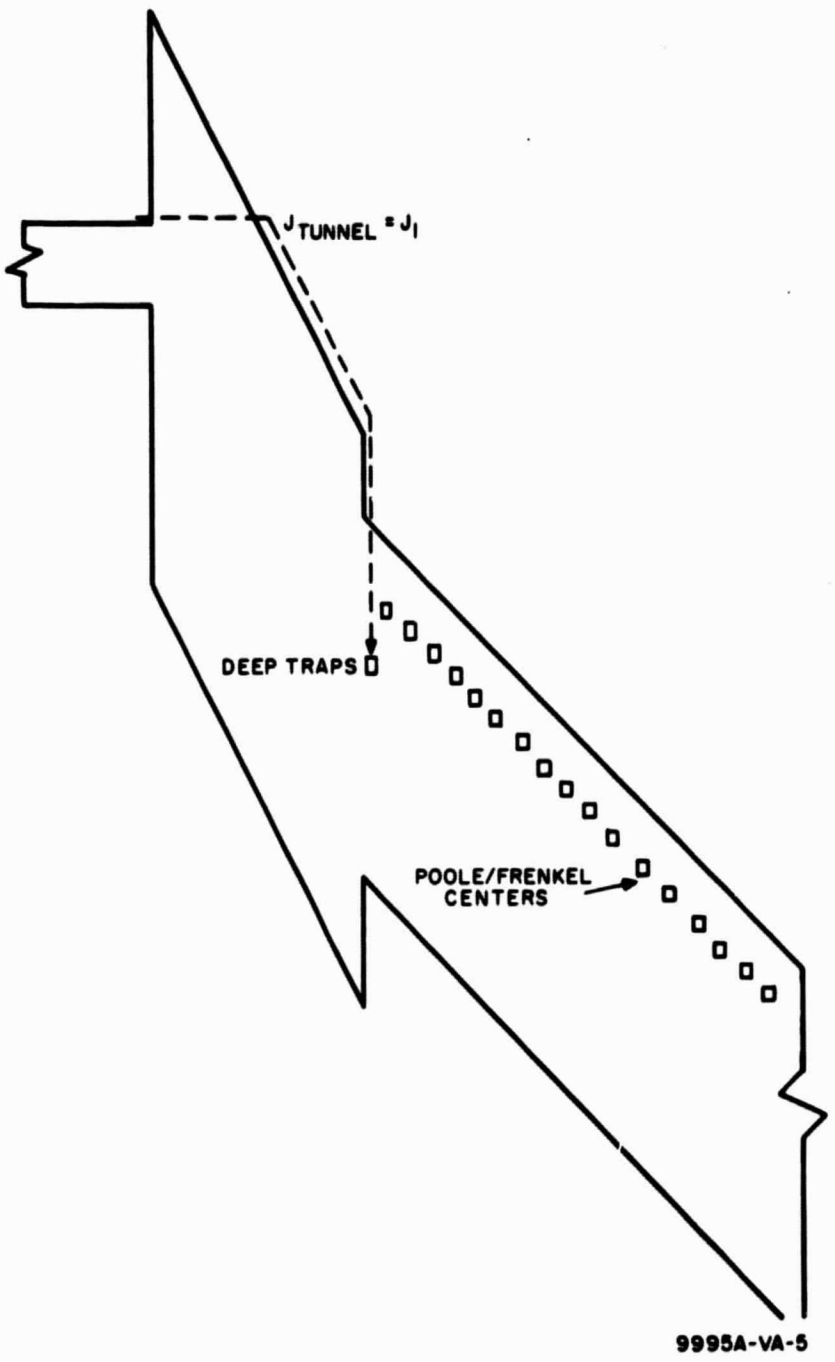


Figure 1. Schematic Band Diagram for Tunneling Trapping in MNOS Structures.

Table 1

	Dominant Current	Deep Trap Assumption	J Sensitivity to Field Direction	Direction of $\Delta V_{FB}/E_A$	Relative Shift ΔV_{FB} (E_A)
1)	$J_N > J_G$	no	$J_N(+) \simeq J_N(-)$	-	$\Delta V_{FB}(+) \simeq \Delta V_{FB}(-)$
2)	$J_G > J_N$	no	$J_G(+) \simeq J_G(-)$	+	$\Delta V_{FB}(+) \simeq \Delta V_{FB}(-)$
3)	$J_N > J_G$	yes	$J_N(+) < J_N(-)$	-	$\Delta V_{FB}(+) < \Delta V_{FB}(-)$
4)	$J_G > J_N$	yes	$J_G(+) > J_G(-)$	+	$\Delta V_{FB}(+) > \Delta V_{FB}(-)$

In case 1, the nitride current density J_N is assumed to be much greater than the oxide current density J_G, and that no deep traps at the nitride-oxide interface are present. The nitride current density for a given electric field is not very different for positive and negative applied electric fields. Note that for a positive applied field, the flatband voltage shift is negative. The shift from the flatband condition is about equal for positive and negative fields. The charge retention is determined only from the bulk nitride current term for the given field conditions.

In the fourth case, it is assumed that the oxide current is much greater than the nitride current and that deep traps are present at the oxide-nitride interface. By assumption, all the charge tunneled from the silicon into the oxide conduction band under positive bias is trapped in relatively deep centers. Because of the energy level of the deep traps the oxide current density for negative oxide field is much less than for a positive oxide field. The direction of flatband shift is positive with an applied positive field. Also the flatband shift for positive applied fields is larger than for negative applied fields because of the polarity sensitivity of the current term. The

retention of charge stored for this case can be far greater than for a structure such as example 1 if the traps are sufficiently deep to have negligable low rates of emission into either the nitride Poole-Frenkel centers or the oxide conduction band.

2.1.3 Basic Model and Theory

A simplified schematic representing the basic structure of the analytical model used to study the MNOST characteristics is shown in figure 2 together with a physical cross-section of a typical MNOST included for reference. This model is used to analyze the vertical components of the electrical phenomena taking place in the MNOST. Therefore, fields and currents that appertain to the structural sequence proceeding from the gate metal electrode, through the nitride, through the oxide, and to the semiconductor substrate electrode, are analyzed while the activity proceeding from the source to drain terminals is not treated explicitly, but is related to the analysis through the treatment of the flatband voltage. The model is established on a per unit area basis in order to lend flexibility in its utilization and in the interpretation and correlation of the results. It consists in the assignment of a capacitance per unit area (C_N) to the nitride layer corresponding to determinations made as to the relative dielectric constant (ϵ_N) of this material and to the thickness (X_N) of this material & a capacitance per unit area (C_G) to the oxide layer and its corresponding dielectric constant (ϵ_G) and thickness (X_G). A voltage controlled conductance for high-field conditions is represented by the current generator (J_N); and a low-field conductance represented by the resistor (R_N). Similar circuit elements are also assigned to the portion of the model representing the oxide layer. The model is completed by the inclusion of a voltage generator

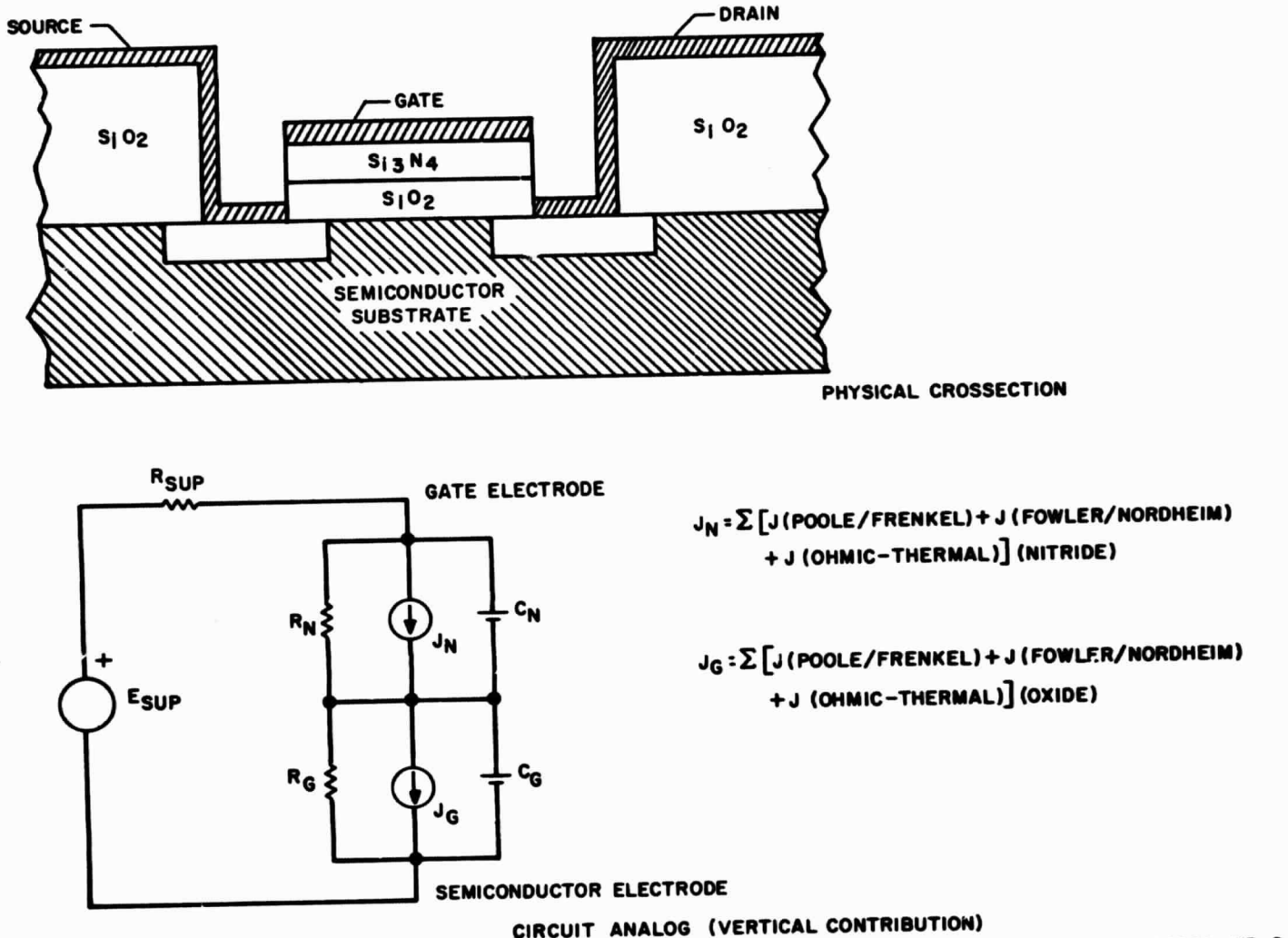


Figure 2. Circuit Model for Transient Analysis

UNCLASSIFIED

($V_{sup} = V_A$) which provides the applied voltage to the metal electrode and a resistor (R_{sup}) to represent the output impedance of this driver. The value of this resistor (R_{sup}) is adjusted so as to obtain a time constant of approximately 10 nsec for the pulse driver for the computer aided transient analysis. The capacitive elements (C_N and C_G) in the model provide for the storage of electrical energy within their respective layers of material and, furthermore, specifically serve to establish the presence of charge at their interface by considering the discontinuity in the dielectric displacement vectors. The current generators (J_N and J_G) are multi-functional conductance elements which serve to characterize the field dependent conductivities of their respective layers at high values of electric field intensity. Conduction mechanisms specifically considered in the analysis include:

a) Field enhanced thermal excitation with trapping centers (Poole-Frenkel effect)

$$J = C_1 E \exp\left(-\frac{q}{kT}\right)\left[\phi_{PF} - (q E/\pi \epsilon_o \epsilon)^{\frac{1}{2}}\right]$$

b) Charge carrier tunneling (Fowler-Nordheim effect)

$$J = C_2 E^2 \exp(-E_2/E)$$

c) Thermally excited charge carrier conduction (ohmic effect)

$$J = C_3 E \exp(-q \phi_3 kT)$$

d) Thermally excited ionic conduction

$$J = (C_4 E/T) \exp(-q \phi_4 kT)$$

The theory of the MNOS charge storage and retention is based on the integrity of the summation of electric potential, the charge/dielectric displacement continuity and the conduction current continuity. These are expressed as:

$$X_G E_G + X_N E_N = V_A \qquad \text{(Electric potential summation)} \quad (2\text{-}1)$$

$$\epsilon_o(\epsilon_G E_G - \epsilon_N E_N) = Q \qquad \text{(charge/dielectric displacement continuity)} \qquad (2\text{-}2)$$

$$Q = \int_o^t (J_N - J_G)\, dt \qquad \text{(current continuity)} \qquad (2\text{-}3)$$

Equations 2-1 and 2-2 may be solved for the electric field intensity pertaining to each material layer to obtain

$$E_G = \frac{\epsilon N}{\alpha} V_A + \frac{X_N}{\epsilon_o \alpha} Q_I \qquad \text{(oxide field intensity)} \qquad (2\text{-}4)$$

$$E_N = \frac{\epsilon G}{\alpha} V_A - \frac{X_G}{\epsilon_o \alpha} Q_I \qquad \text{(nitride field intensity)} \qquad (2\text{-}5)$$

where

$$\alpha = (\epsilon_G X_N + \epsilon_N X_G). \qquad (2\text{-}6)$$

Since the flatband condition ($E_{si} = 0$) is achieved in the semiconductor when the oxide field is zero, the flatband voltage V_{FB} may be written in terms of the effective sheet of charge per unit area stored at the oxide-nitride interface Q_I from equation 2-4 as

$$V_A = V_{FB} = -\frac{X_N}{\epsilon_o \epsilon_N} Q_I$$

$$= -\frac{Q_I}{C_N} . \qquad (2\text{-}7)$$

Where a net effective surface state charge (Q_{ss}) exists at the silicon-silicon dioxide interface

$$\epsilon_o \epsilon_G E_G = \epsilon_o \epsilon_{si} E_{si} - Q_{ss}. \qquad (2\text{-}8)$$

Then for $E_{si} = 0$, $V_{FB} = V_A$ and $E_G = \frac{Q_{ss}}{\epsilon_o \epsilon_G}$ from equation (2-4) flatband voltage is

$$V_{FB} = - \left[\frac{X_N}{\epsilon_o \epsilon_N} Q_I + \frac{\alpha}{\epsilon_o \epsilon_N \epsilon_G} Q_{ss} \right]$$

$$= - \left[\frac{Q_I}{C_N} + \frac{Q_{ss}}{C_T} \right] \qquad (2\text{-}9)$$

where C_T is the total effective series capacitance per unit area of the oxide and nitride layers.

2.1.4 Charging Time Analysis

Solutions for the charging time for the cases where the nitride current is dominant have been derived from the relationship

$$t_c = C_N \int_{\infty}^{V_{FB}} \frac{1}{J_N - J_G} \, d V_{FB} \qquad (2\text{-}10)$$

For the nitride current dominant[8]

$$J_N - J_G \simeq J_N = J_o \exp G E_N^{\frac{1}{2}} \qquad (2\text{-}11)$$

and

$$t_c = t_o \{ \exp - G\beta_1(\gamma_1 V_A - V_{FB})^{\frac{1}{2}} [G\beta_1(\gamma_1 V_A - V_{FB})^{\frac{1}{2}} + 1]$$

$$- \exp - G\beta_1(\gamma_1 V_A)^{\frac{1}{2}} [G\beta_1(\gamma_1 V_A)^{\frac{1}{2}} + 1] \} \qquad (2\text{-}12)$$

where $t_o = \frac{2}{J_o G^2} \left[\frac{X_N}{X_G} \epsilon_G + \epsilon_N \right]$

$$\beta_1 = \frac{\epsilon_N \epsilon_G}{X_N (\epsilon_N X_G + \epsilon_G X_N)}$$

$$\gamma_1 = \frac{\epsilon_G X_N}{\epsilon_N X_G}$$

For the oxide current dominant where tunnelling is the principal mechanism

$$J_N - J_G \simeq - J_G = - C_3 E_G^2 \exp \frac{-C_4}{|E_G|} \qquad (2\text{-}13)$$

The charging time then for this case is

$$t_c = \frac{\beta_2}{\gamma_2}\left[\exp\left(\frac{\gamma_2}{V_A - V_{FB}}\right) - \exp\left(\frac{\gamma_2}{V_A}\right)\right] \qquad (2\text{-}14)$$

where

$$\beta_2 = \frac{\epsilon_o \alpha^2}{\epsilon_N X_N C_3}$$

$$\gamma_2 = \frac{C_4 \alpha}{\epsilon_N}$$

$$\alpha = \epsilon_G X_N + \epsilon_N X_G$$

For some thermal oxide cases, it has been found empirically that for pulse conditions the oxide current has a form

$$J_G = C_1 \exp C_2 \; E_G^{\frac{1}{2}}. \qquad (2\text{-}15)$$

The charging time then for the case for this type of dominant oxide current is

$$t_c = \frac{2A}{B^2}\left[\frac{B\,(V_A - V_{FB})^{\frac{1}{2}} + 1}{\exp B\,(V_A - V_{FB})^{\frac{1}{2}}} - \frac{B\,(V_A)^{\frac{1}{2}} + 1}{\exp B\,(V_A)^{\frac{1}{2}}}\right] \qquad (2\text{-}16)$$

where

$$A = \frac{\epsilon_o \epsilon_N}{X_N C_1}$$

$$B = \frac{C_2 \epsilon_N^{\frac{1}{2}}}{\alpha^{\frac{1}{2}}}$$

$$\alpha = X_N \epsilon_G + X_G \epsilon_N .$$

2.2 Experiments and Results

2.2.1 Silicon Oxidation Techniques

There are several types of silicon dioxide films such as thermally grown from steam; thermally grown from oxygen; thermally grown from nitrious oxide and by the pyrolytic decomposition of silane that have been used in combination with silicon nitride. In this study the experiments were restricted to thermally grown silicon dioxide from oxygen. Several variations of this type of thermally grown oxide were studied to determine the effect of oxygen partial pressure and silicon dopant concentrations on the characteristics of MNOS devices.

The oxidation rates of silicon have been shown to be dependent on the oxygen partial pressure[9], the crystal orientation[10] and the concentration and type of dopant elements in the silicon at the surface[11].

For example, it has been shown[9] that the linear oxidation rate constant A is not affected, but the parabolic rate constant B is linearly proportional to the equilibrium concentration of the oxidant in the oxide which in turn is related to the partial pressure of the oxidant gas.

On the other hand, it has been shown[10] that the linear oxidation rate constant A is increased for ⟨100⟩ oriented silicon as compared to ⟨111⟩ oriented silicon while the parabolic rate is not changed much. Further, it has been shown[11] that for heavily doped silicon ($C > 10^{18}$) for either phosphorous or boron that the parabolic rate constant B can be increased by a factor of 1.5. The effect of temperature and time has also been determined[12]. Of particular importance is the approximation for short time oxidations which is

$$X_G = \frac{B}{A} t + X_i$$

The oxide thickness X_G for thermally oxidized silicon with oxygen gas as the oxidant is linearly dependent on time; however, the silicon initially appears to oxidize very rapidly such that the linear extrapolation of data yields an initial oxide thickness X_i at $t = 0$. This has been reported to be typically 200 Å for ⟨111⟩ silicon.[12]

Since the understanding of the thin oxide case is of primary importance for the fabrication of polarizable MNOS transistors and generally for the fabrication of oxides with low surface state density Q_{ss}, several experiments were carried out to further characterize this case. First, it was decided that the possibility of an initial oxide, X_i, would be minimized by elimination of chemically formed surface oxides by a final HF rinse leaving the surface hydrophobic. The silicon wafers are then reduced in H_2 in the oxidization system (reactor or furnace) to minimize the effect of fluorine retention on the silicon surface. The silicon material used was primarily ⟨100⟩ 2 to 8 ohm N type phosphorous doped and the same type of ⟨100⟩ crystal diffused with boron to yield a P type surface concentration of 5×10^{16} to 2×10^{17} per cm^3. Oxidation on P+ and N+ diffusions were also carried out. The oxidations were either in 100% O_2 or with the oxygen flow reduced to about 10% of the nitrogen carrier gas flow.

The silicon nitride was formed by the pyrolytic decomposition of silane (SiH_4) in ammonia (NH_3) premarily at 900°C with nitrogen as a carrier gas. The ammonia/silane ratio was greater than 200 for all experiments.

2.2.2 Characterization of MNOS Devices

Electrical measurements of the current density (J) vs electric field (E) relationship, capacitance-voltage measurements (C-V) under temperature bias stress and N and P channel transistor drain current (I_d) vs applied voltage (V_A) have

been used to characterize the nitride-oxide films fabricated. Also optical and physical measurements of film thicknesses have been used with the capacitance measurements to determine the dielectric constants.

The first type of measurements that were made were to characterize the grown silicon diocide films and the deposited silicon nitride films individually. The typical dielectric constants measured were $\epsilon_N = 6.5$ and $\epsilon_G = 3.9$. The dielectric constant of the very thin oxide films is uncertain because of the difficulty in measuring the oxide thickness; however, reasonably good agreement of the capacitance and current-field relationships for different thicknesses in the same range (100-200 Å) was obtained by using the dielectric constant of the thicker oxide films.

Typical silicon nitride and thermally grown silicon dioxide single layer current density vs electric field relationships are shown in figure 3. The current measurements were made down to 10^{-14} amperes. Comparison of these characteristics with the double layer nitride-oxide films provides some insight into the interaction of the nitride deposition conditions on the oxide formation and vice versa.

The most significant MNOS device experiment performed involved the simultaneous fabrication of N and P channel MNOS transistors and capacitors. The C-V measurements of the two types of capacitors are shown in figure 4. It should be noted that while the thermal oxidations were performed simultaneously the nitride depositions for these samples were done in two different runs to accommodate other test wafers used in the experiment. The measured thicknesses for the samples were:

	X_N	X_G	C_{max}
da-1	900	190	5.91 pf (P- Diff & N+ Diffusion)
CX 62	660	100	8.65 pf (N type and P+ Diffusion

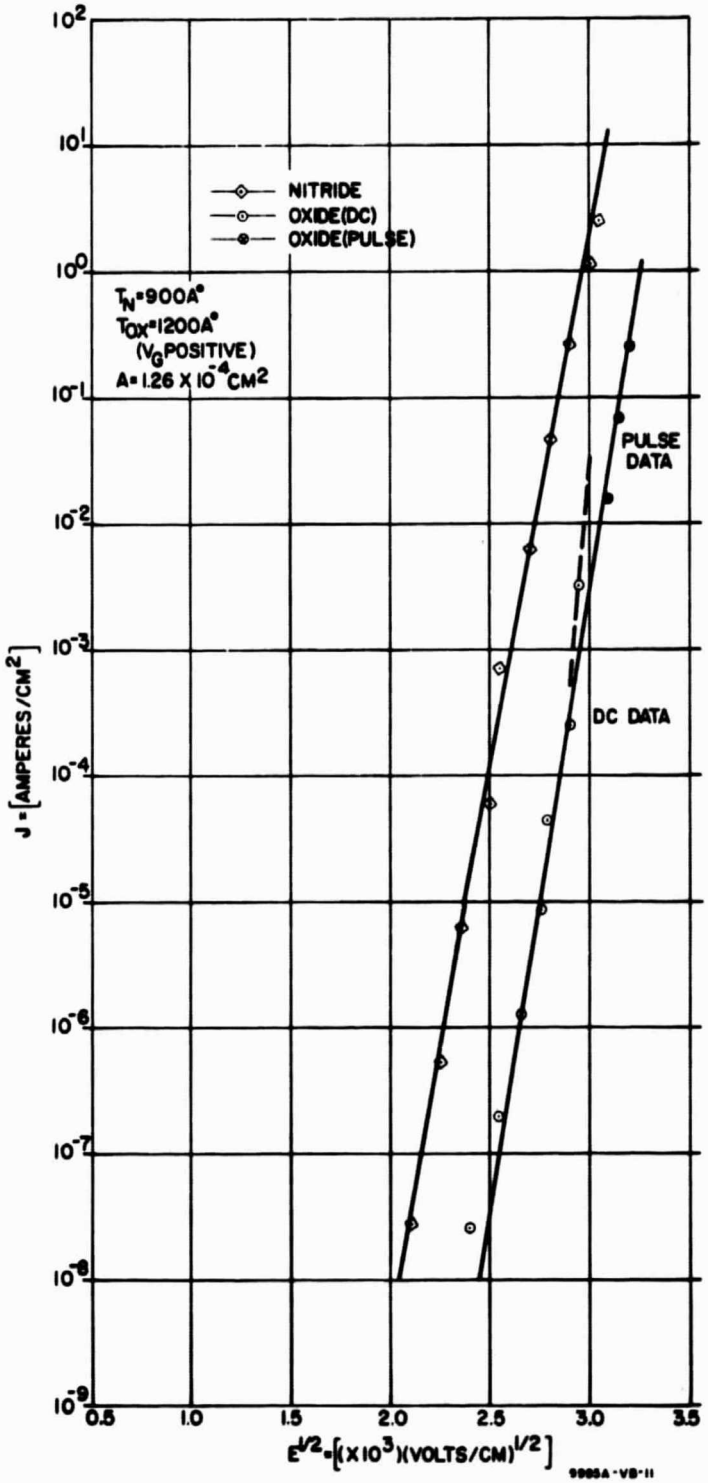


Figure 3. Insulator Current Density (J) vs. Electric Field ($E^{\frac{1}{2}}$) for Separate Oxide and Nitride Films.

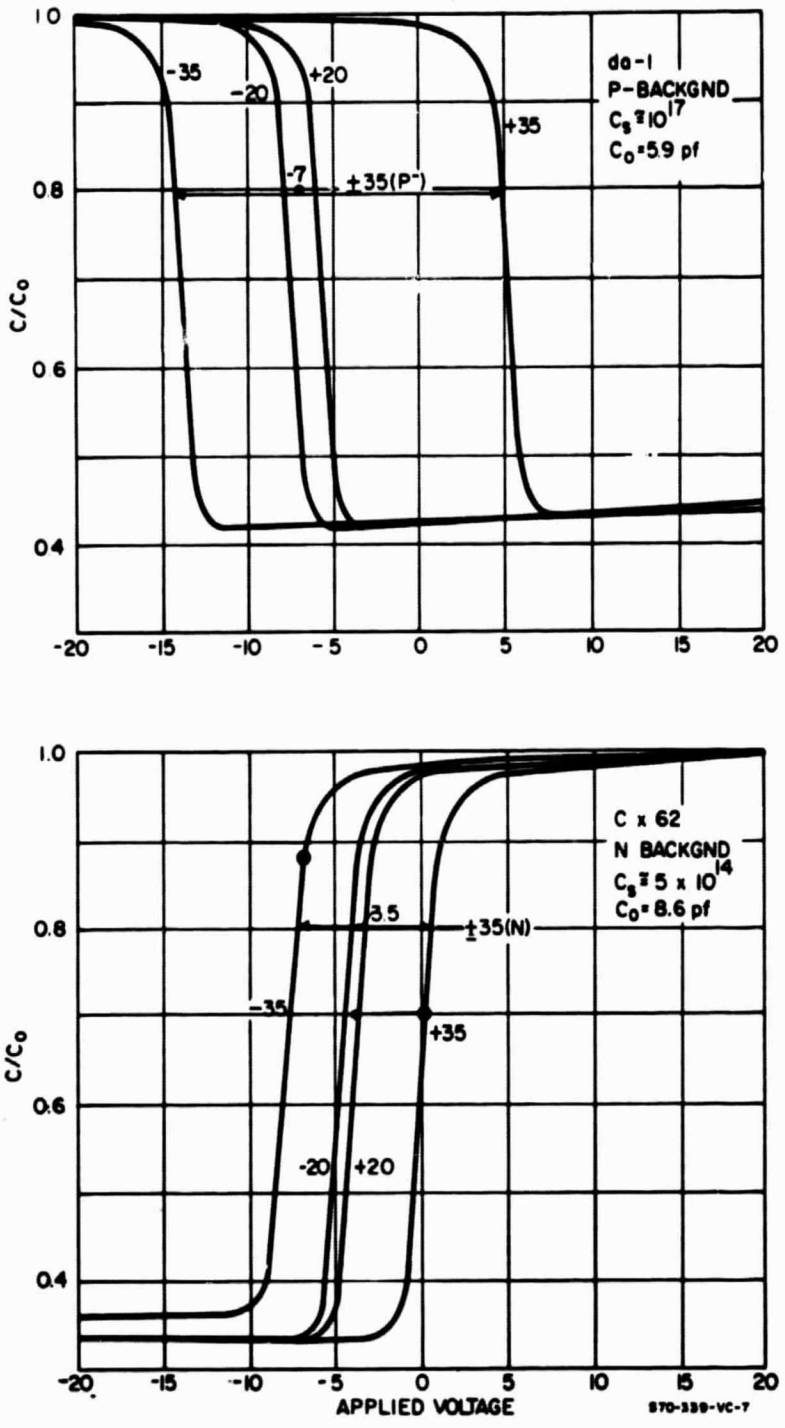


Figure 4. C-V Curves for Thermally Oxidized N and P Type Wafers.

	X_N	X_G	C_{max}
BS 13	660	100	- (N type Capacitors only)

It can be seen from the C-V curves of figure 4 that the ΔV_{FB} for a given applied dc voltage (V_A) is much greater for da-1 than for CX 62 even though the field in the oxide of da-1 is much less than for CX 62. It is concluded that not only is the oxidation rate of the P- diffusion (da-1) almost twice that of the N wafer, but also the conductivity of the thicker film on the P- wafer must also be greater than for the N wafer. Note also that the ΔV_{FB} for $\pm V_A$ is almost symetrical indicating that deep traps are not significant for these oxidation conditions.

The J vs $E^{\frac{1}{2}}$ relationships shown in figure 5 for the oxide and nitride films on these two wafers were calculated from the measured current through the composite MNOS capacitor and the fact that

$$J_N (E_N) = J_G (E_G)$$

in equilibrium. The equations 2-4 and 2-5 were used to calculate E_N and E_G.

It can be seen that the nitride J vs E characteristics for the two films are nearly the same as should be, but that the current density for the oxide film on the P- diffused wafer is much greater than for the oxide on the N type wafer as predicted from the C-V measurements, i.e.,

$$J_G (\text{da-1}) > J_G (\text{CX 62})$$

for a given field.

An additional factor observed is that the oxide - J vs E - relationship does not seem to be like Fowler-Nordheim tunneling. The presence of other field

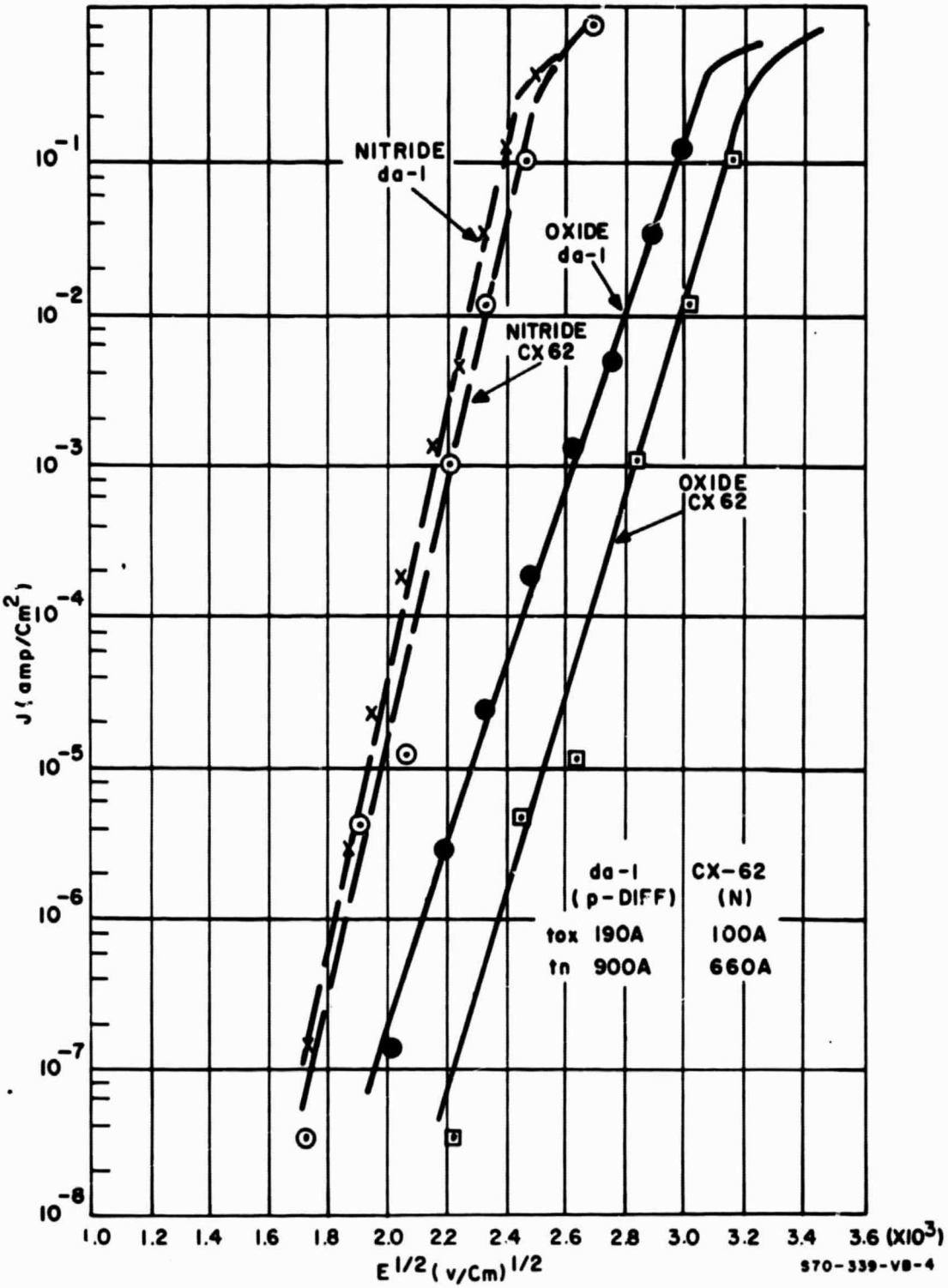


Figure 5. Current Density (J) vs. Electric Field ($E^{\frac{1}{2}}$) for MNOS Capacitors.

dependent currents is probably masking the pure tunneling characteristic.

Finally the initial value of V_{FB} for the samples that included the MNOS transistors (CX 62 and da-1) was much greater than for the capacitor only wafer BS13. This indicates some contribution to Q_{ss} from the previous processing steps. The efficacy of the hydrogen reduction step was proven by the fact that BS13 and other similarly processed wafers had initial flatband voltages of about 1 volt indicating low net effective Q_{ss}. If it is assumed that the initial interface charge Q_I is zero, then from equation 2

$$N_{ss} = \frac{C_T}{q} \left[\Delta V_{FB} - \phi_{ms} \right]$$

$$N_{ss} \simeq 2 \times 10^{11} \text{ cm}^{-2}$$

This represents about the lowest limit of N_{ss} for the thermally oxidized samples measured. Also there were no significant differences between the oxides thermally grown in the reactor and the oxides thermally grown in the resistance heated furnaces.

The oxide thickness for thermally oxidized N type ⟨100⟩ control wafers fabricated along with da-1, CX 62 and the others where the partial pressure of O_2 was about 0.1 of atmospheric is shown in figure 6. Note that $X_i = 65$ Å for these conditions is much less than that reported previously ($X_i = 200$ Å).[12] The oxidation rate ratio (B/A) calculated from this data is lower by a factor of two as compared to the oxidation theory and previously determined rate constants for thicker oxides[9, 10, 11, 12]. The uncertaintly in the thin oxide measurements may be contributing to this error.

N channel MNOS transistors made on wafer da-1 were tested and shown to have characteristics very similar to the capacitors on the same wafer. The drain

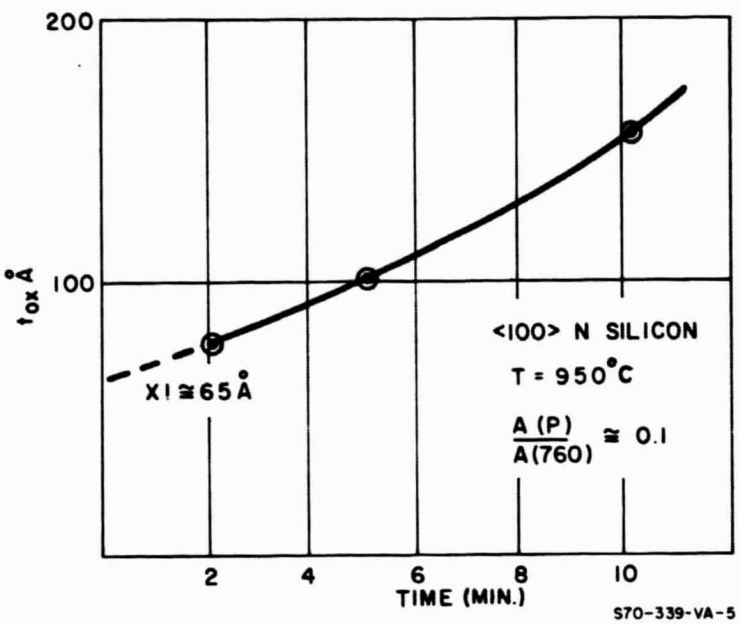
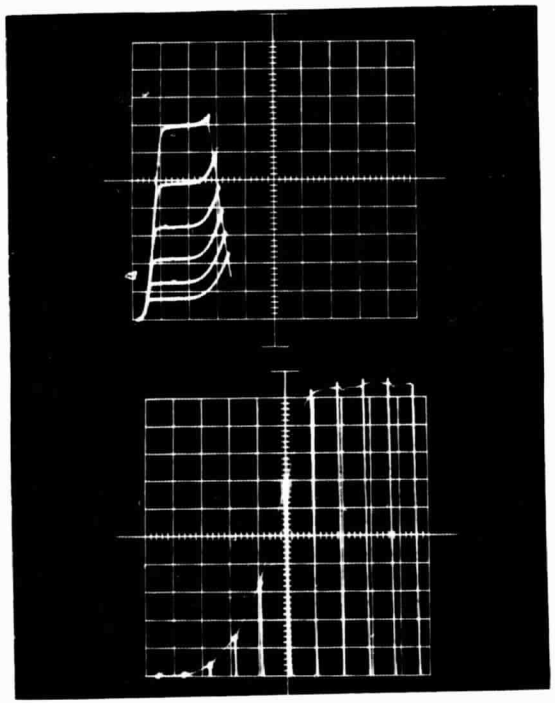


Figure 6. Thin Thermal Oxide Thickness vs. Oxidation Time (low partial O_2 pressure)

current vs drain voltage (I_d vs V_d) and drain current vs gate voltage (I_d vs V_g) characteristics are shown in figure 7. The P channel MNOS transistors on CS 62; however, exhibited anomolous behavior. It was found that at low electric field for long periods of time some correlation between the MNOS transistors and capacitors was obtained. At higher fields, however, the direction of the transistor threshold voltage, V_T, shift was reversed compared to the capacitors. Since P channel transistors require a P+ source and drain diffusion and it has been shown that the oxides over boron diffused (P type) regions are much more conductive, it is believed that the reversal of the direction of ΔV_T is caused by a larger and opposite polarity of charge being stored near the source junction as compared to the charge stored over the N type material where the channel is formed. This points to the conclusion that thermally grown thin oxide for MNOS P channel transistors is undesirable.

2.2.3 Charging and Retention Time Response

In addition to the simplified solutions to the charging response time of MNOS devices listed in section 2.1, computer aided transient analysis using Sceptre[13] has been used. The basic circuit transient analysis program has been modified to include a number of defined functions which are used to describe the conduction mechanisms in the nitride and oxide layers based on empirically derived data. The model of figure 2 is the basic circuit model used for the transient analyses. The simulation of the N channel transistor case described in the previous section has been accomplished and the results are shown in figures 8, 9 and 10. The correlation with the measurements is reasonably good. Figure 8 depicts the waveshape corresponding to the conduction current density through the oxide, and it can be seen that it is three orders of magnitude greater at its



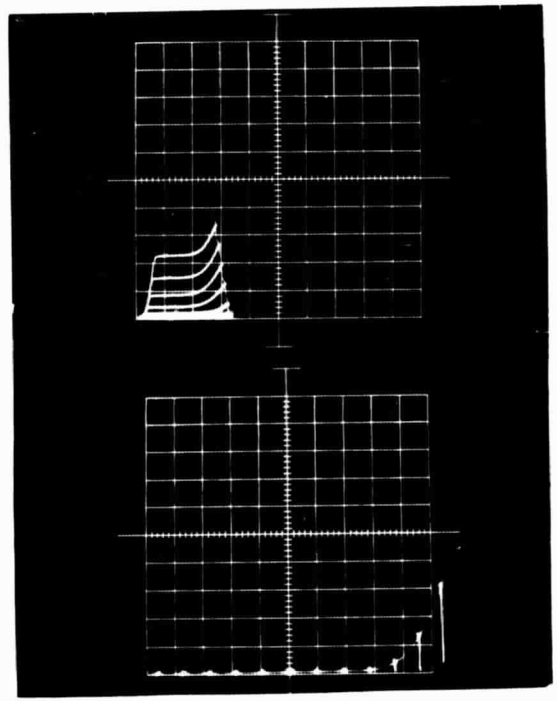
TOP: I_D VS V_D
HORIZ: 0.1 MA/DIV
VERT: 5 V/DIV

$I_D = 0$

LEFT PHOTO:
V_G = −0.5 V/STEP
RIGHT PHOTO:
V = +0.5V/STEP

$I_D = 0$

BOTTOM: I_D VS V_G
HORIZ: V_G = 1V/STEP
VERT: I_D = 0.1 MA/DIV



$-V_G$ 0 $+V_G$

AFTER −55V, 10 μSEC
V_T = −4V
V_T (SAT) = −9V

$-V_G$ 0 $+V_G$

AFTER +55 V, 10 μSEC
V_T = +4
V_T (SAT) = +6 V

9995A-VA-12

Figure 7. MNOS Transistor Drain Current vs. Drain Voltage and Gate Voltage Showing Threshold Voltage Shift

UNCLASSIFIED

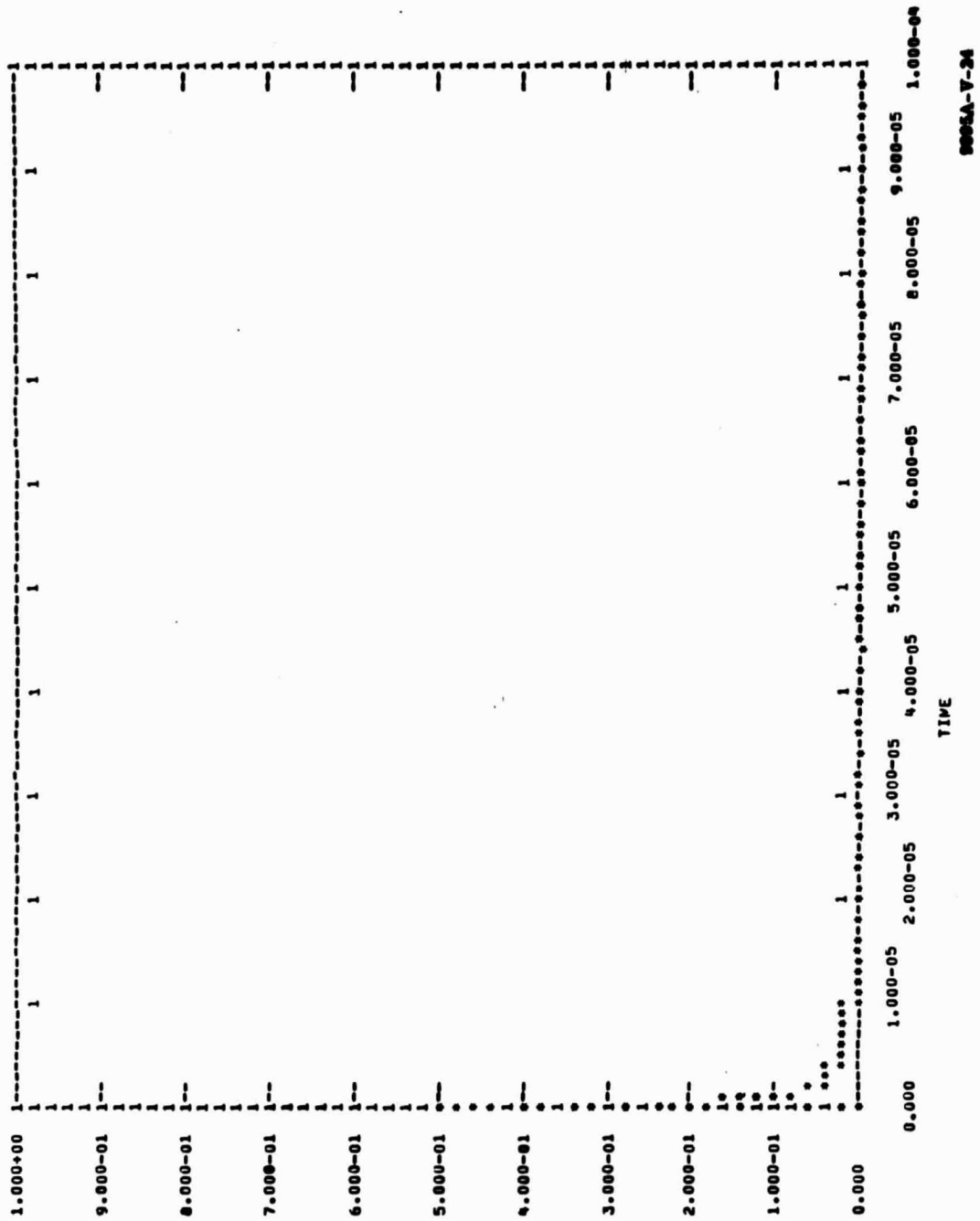


Figure 8. Computer Print Out of J_G vs. t

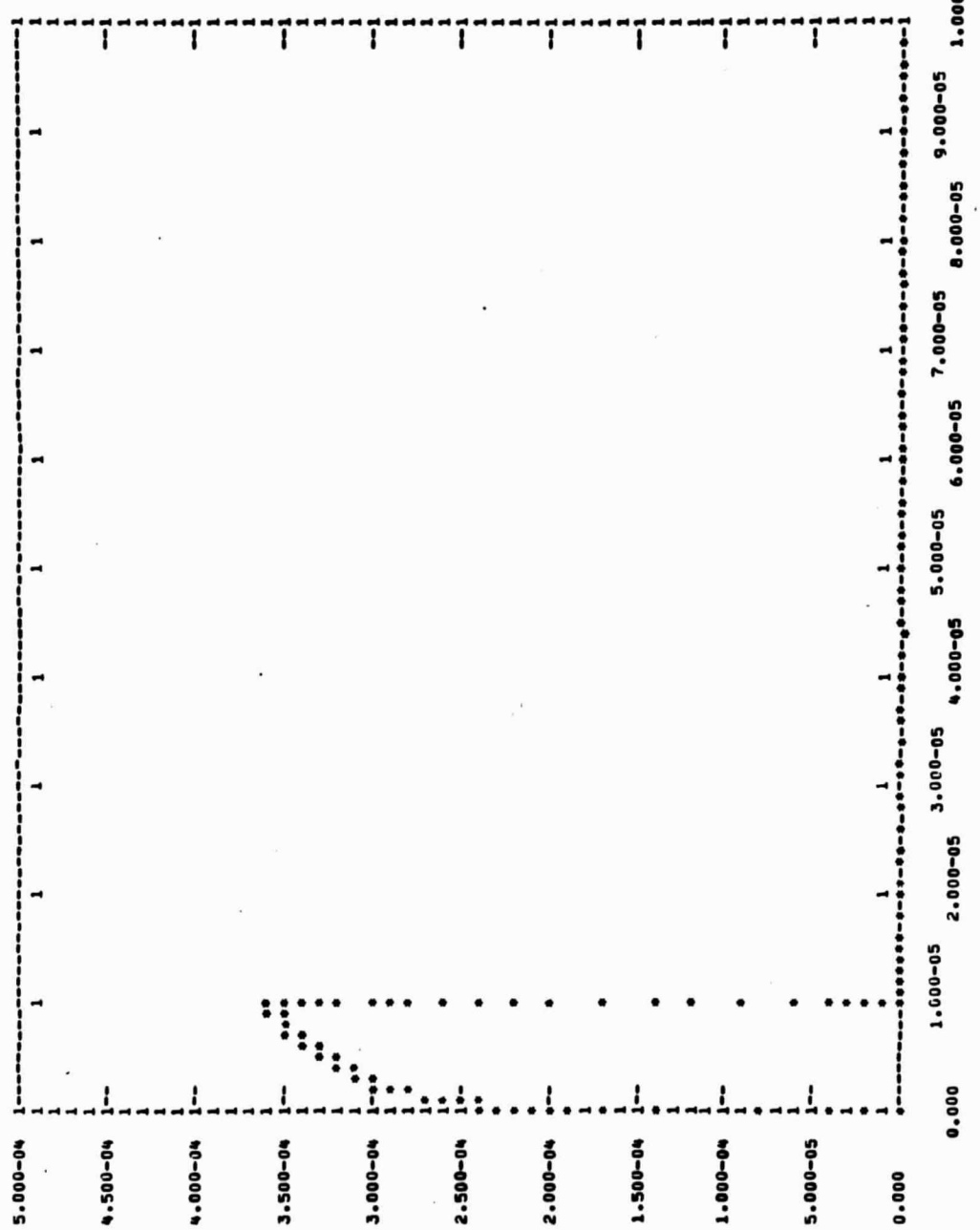


Figure 9. Computer Print Out of J_N vs. t

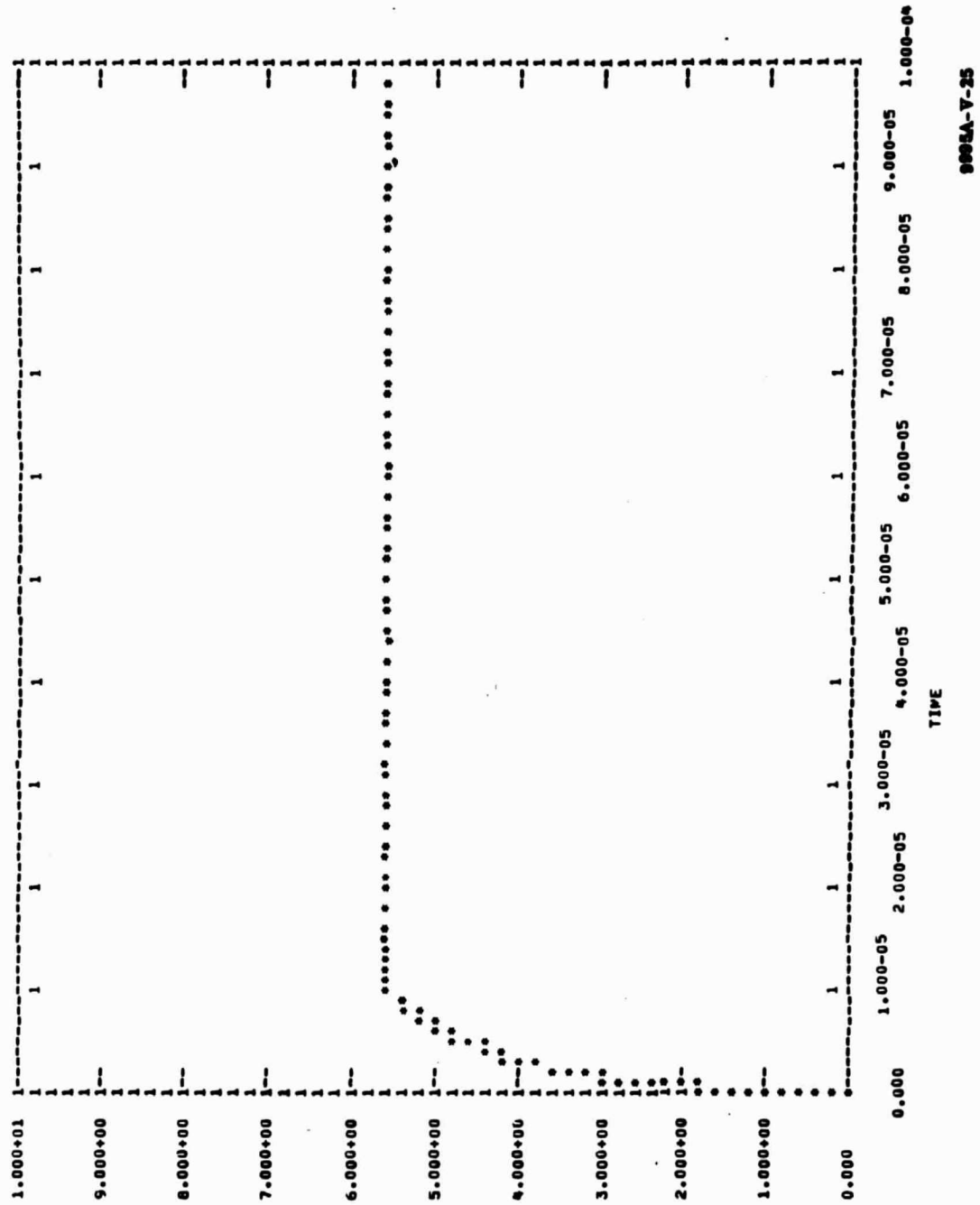


Figure 10. Computer Print Out of V_{FB} vs. t

peak in relation to the peak nitride current density shown in figure 9. The waveshape of J_N clearly defines the turnoff for the 55 volt driving pulse of 10 microseconds width. The flatband voltage waveshape is shown in figure 10. This is seen to reach 5.6v within 10 microsec and is seen to persist after the driving pulse has been turned off.

The P channel capacitors formed on wafer BS13 which are similar to those on CS 62 were also pulse tested to determine the flatband voltage shift vs the applied voltage and pulse width. The data is shown in figure 11. Note that the flatband voltage shift is nearly symetrical for negative and positive applied fields taking into account the effect of V_{FB} on the fields. This indicates that deep electron traps at the interface of the insulators are not present in any large amount. The retention time for this type of MNOS device was measured at V_A = 0v and is shown in figure 12. The rate of decay is a function of the total V_{FB} shift. The decay is logrithmic and a characteristic rate of decay is 0.3 to 0.5 v/decade from saturation. This is not as good as measured for samples that have been shown to have deep traps where the rate of decay is less than 0.1 v/decade.

To illustrate the high switching speed limits for thermally oxidized MNOS transistors, N channel MNOS transistors were fabricated with a thermal oxide grown at 850°C in a partial pressure of oxygen and with a nitride film of about 350 Å. The C-V curve of the gate capacitance which gives a low frequency characteristic is shown in figure 13. The curves illustrate that a 2.2 volt V_{FB} shift is possible with a +20 and a -15 v, 100 nanosec pulse. The decay rate was typical of the thermally grown oxides previously discussed.

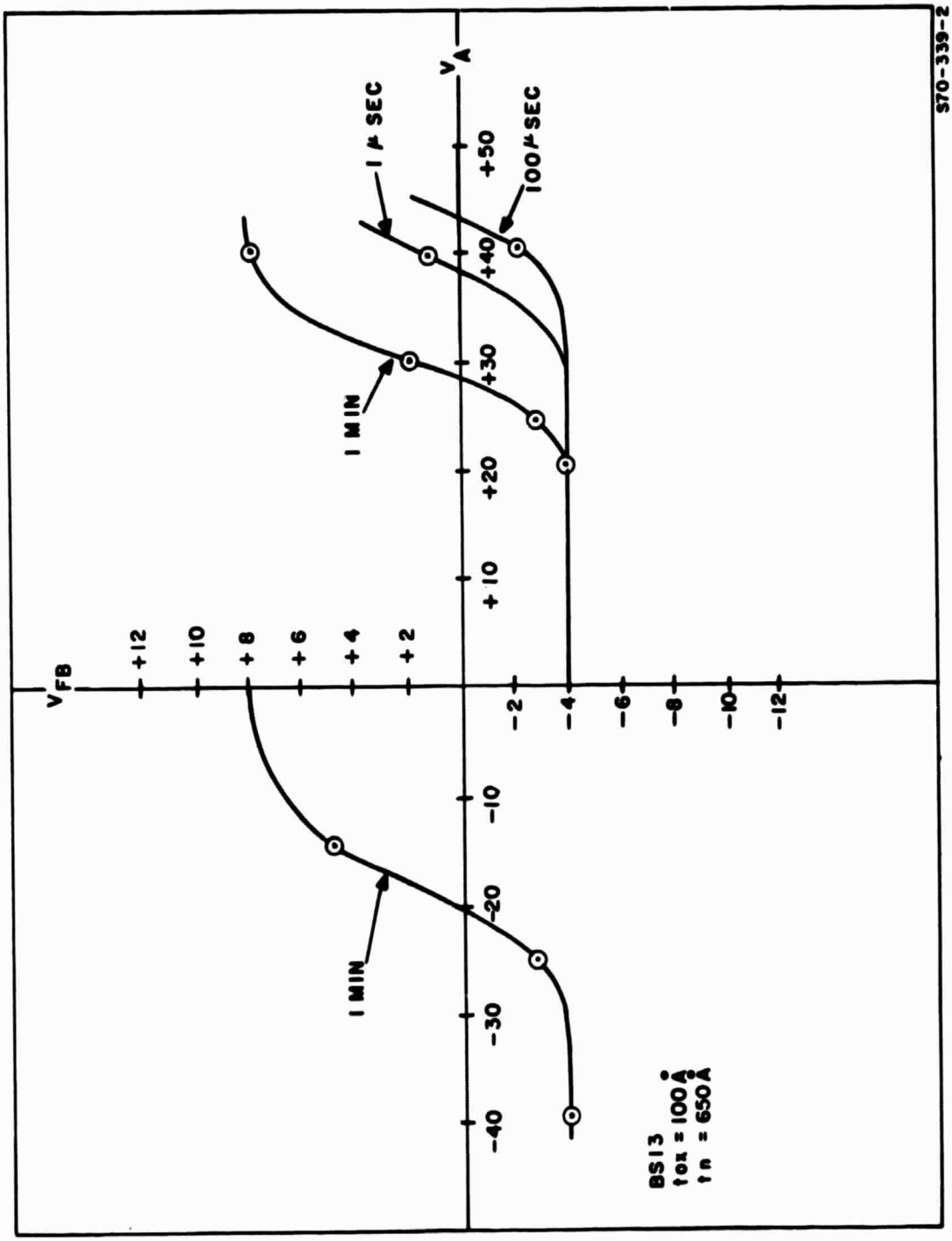


Figure 11. Flatband Voltage vs. Applied Voltage for Different Times

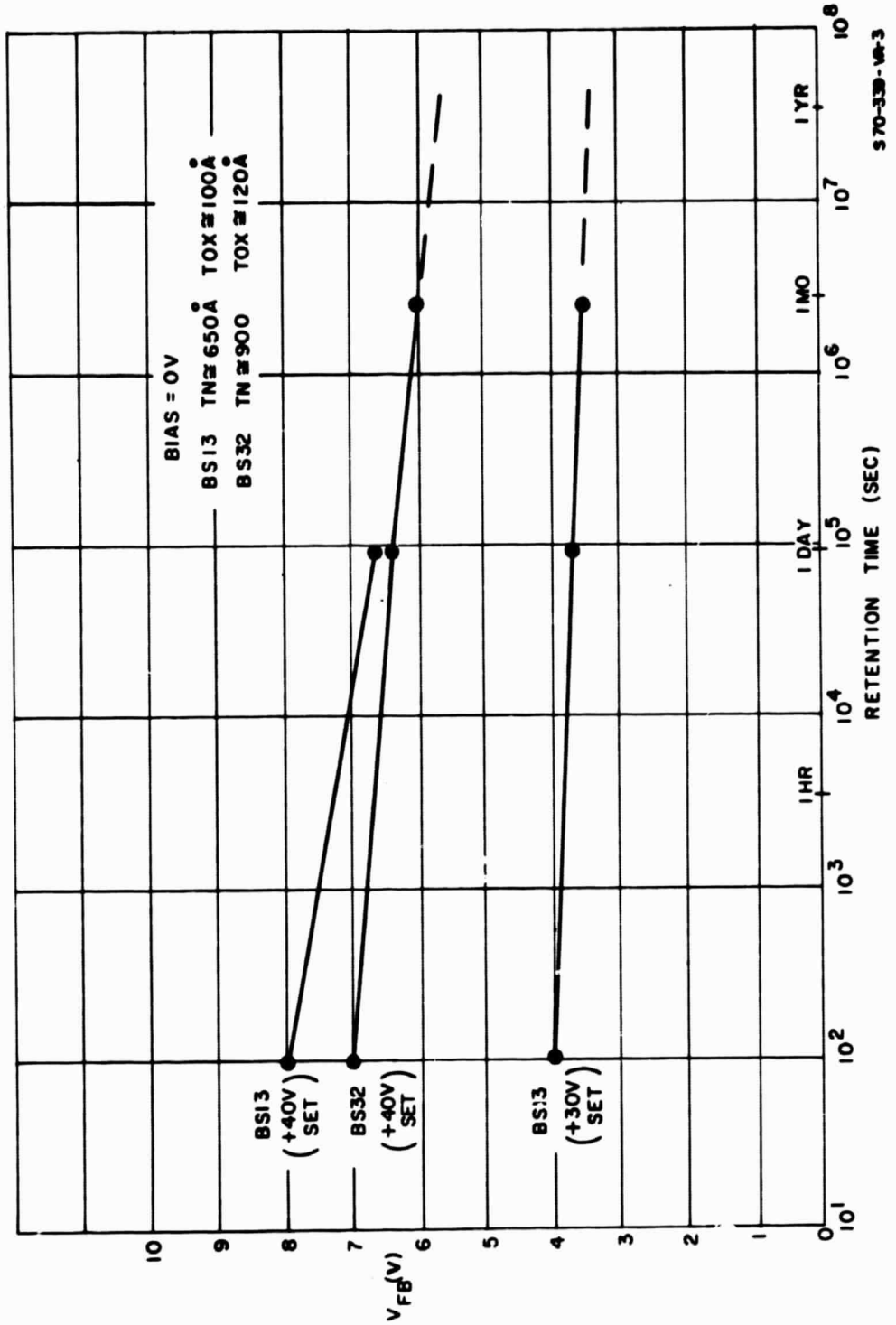


Figure 12. Retention of Charge

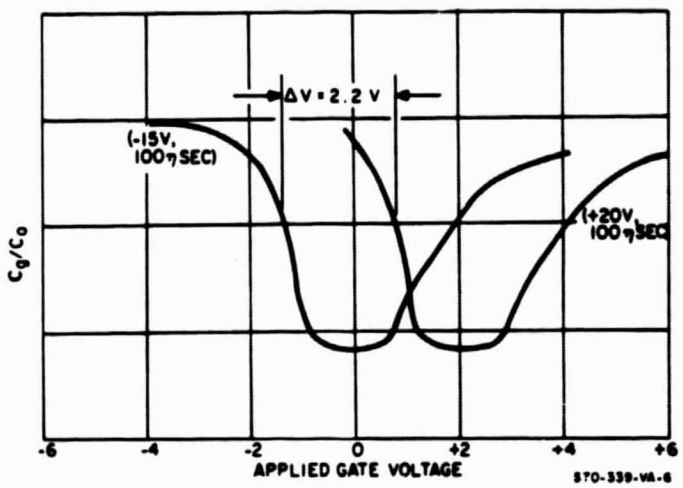


Figure 13. C-V Curve Showing N Channel Transistor Flatband Voltage Shift for 100 Nanosec Pulses.

2.2.4 Nitride-Oxide Passivation

The factors involved in optimizing nitride passivated devices are the initial level of Q_I and Q_{ss} that can be achieved, the long term accumulation of Q_I at the operating fields, the change in Q_I and Q_{ss} for a given temperature bias stress, the maximum electric field protection provided and finally the extent to which the MNOS transistor transconductance (where $g_m \sim C_T$) is to be maximized. Where shielding is not provided radiation sensitivity is also a factor to be considered.

To illustrate the range of possibilities consider the following list of cases where the total effective series capacitance per unit area C_T is kept constant. The flatband voltage is derived from equation 2-9, i.e.,

$$V_{FB} = \frac{1}{C_T} \left[\frac{C_T}{C_N} \quad Q_I + Q_{ss} \right] .$$

Case	Relative Thicknesses	Relative Capacitance	ΔV_{FB}
1	$X_G < X_N$	$C_N \cong C_T$	$-\frac{1}{C_T} [Q_I + Q_{ss}]$
2	$X_G = X_N$	$C_N \cong 2.7\ C_T$	$-\frac{1}{C_T} [0.37\ Q_I + Q_{ss}]$
3	$X_G > X_N$	$C_N > C_T$	$-\frac{1}{C_T} [Q_{ss}]$

Therefore, to minimize the effect of Q_I build up, it appears at a first glance that the nitride thickness should be minimized. There are, however, two additional factors that must be considered. One is that the masking ability of the Si_3N_4 tends to decrease as its thickness is decreased. Second, but more important, is the consideration of a dipole electric moment

that has been observed in SiO_2 after the Si_3N_4 deposition. It is suspected that the dipole is caused by the presence of hydrogen during the Si_3N_4 deposition. A similar list of cases for thick and thin nitride films again where C_T is a constant and where ΔV_{FB} is also a function of the dipole charge $Q_P(V_A)$ in the oxide in this manner,

$$\Delta V_{FB} = -\frac{1}{C_T} \left[\frac{C_T}{C_N} (Q_I - Q_P) + (Q_{ss} + Q_P)\right]$$

is shown below:

Case	Relative Thickness	Relative Capacitance	ΔV_{FB}
1	$X_G < X_N$	$C_N \cong C_T$	$-\frac{1}{C_T}[Q_I + Q_{ss}]$
2	$X_G = X_V$	$C_N \cong 2.7\ C_T$	$-\frac{1}{C_T}\left[.37\ (Q_I - Q_P) + Q_{ss} + Q_P\right]$
3	$X_G > X_N$	$C_N > C_T$	$-\frac{1}{C_T}[Q_{ss} + Q_P]$

The result is that the dipole charge effect can be minimized for a given C_T with a thin oxide. This reduction of the dipole effect has been observed for thinner oxides. Also the magnitude of Q_P can be affected somewhat by the total amount of NH_3 present during the nitride deposition.

Another hysteresis effect that has been observed which has the opposite sense to hysteresis caused by dipole moments is caused by interface charge transport across either the nitride-metal interface, the nitride-oxide interface or the oxide semiconductor interface. For any of these cases a space charge tends to remain at the interface after the applied bias because of the interface barrier.

This space charge is then imaged in the semiconductor producing a flatband voltage shift. The significant aspect of this interface charge transport affect is that the direction of V_{FB} shift is positive for a positive applied voltage. Note that either ionic drift or dipole moments in the insulators always produce a negative V_{FB} shift for a positive applied voltage and therefore, may be separated from the hysteresis caused by interface charge transport. This space charge effect is minimized by increasing the total effective capacitance C_T. The magnitude of ΔV_{FB} for samples with 900 Å of nitride and 100 Å of oxide is about $\pm$ .2v for $\pm$ 15v bias.

The conclusion based on the above factors is that for fields of less than 2×10^6 v/cm that the case where $X_G < X_N$ is the preferred and more stable case since at low fields Q_I remains small, Q_P is minimized, and the maximum C_T can be obtained for a given nitride thickness.

A very conservative case of where both a thick oxide and thick nitride of equal thicknesses are used to minimize the magnitude of the electric fields is shown in figure 14. A bias of $\pm$ 20 volts was used giving fields of less than 2×10^6 v/cm in both the nitride and oxide films. The temperature of the test was 150°C and the time was 16 hours for each bias. The initial threshold voltage at 1 micro-amp was about -3.1v. Note that for a positive bias little shift occured, but for a negative bias about a -0.6v shift occured. A shift of +0.4v occured after the positive bias was occured leaving a net shift of -0.2v. The direction of the shift with bias (+ ΔV with + V_A) is indicative of the interface charge transport and the net -ΔV shift is indicative of either redistribution of ionic charge in the oxide or some nitride conduction resulting in an increase of positive insulator interface charge Q_I.

2.2.5 Processing Manual for Pyrolytic Silicon Nitride Deposition

A manual describing the nitride processing details used for this task entitled "Pyrolytic Silicon Nitride Deposition" has been delivered under separate cover.

2.3 MNOS Transistor Memory System

A memory array using MNOS transistors has been designed. The memory operation depends on gate-to-source biasing for polarization or inhibiting of polarization. This is also known as channel shielding. The three modes of operation of the polarizable MIS transistor for gate-to-source polarization which is required in clear (erase)--write systems are shown in figure 15.

In the clear mode, a sufficiently large negative bias ($V_{SS} = -V_P$) applied to the n-type pocket provides a positive gate-to-source bias which shifts the threshold voltage positive. In the inhibit mode, a negative bias

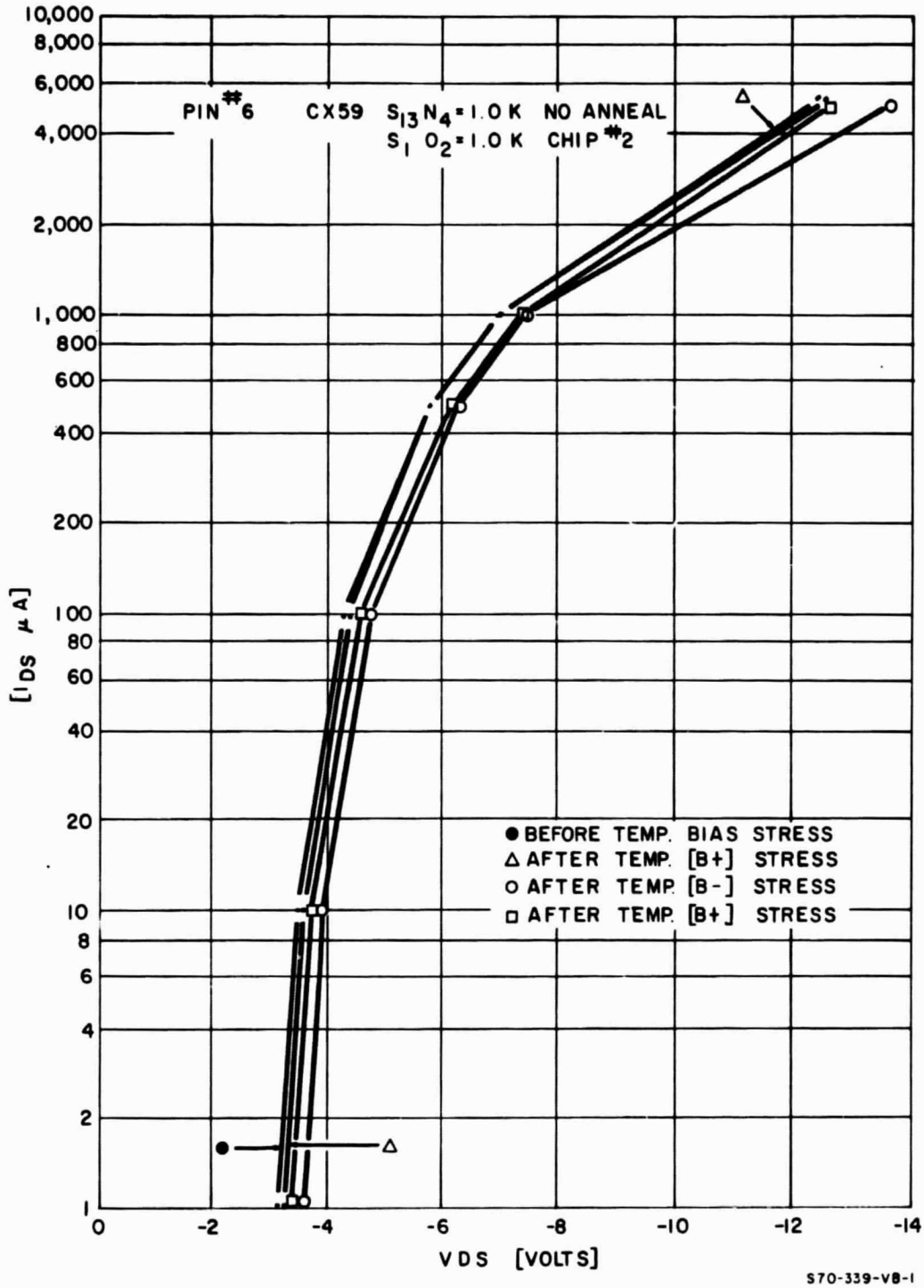


Figure 14. MNOS Transistor Curves for Temperature Bias Stress (V_A = ± 20v and $E_N \simeq \pm 0.8 \times 10^6$ v/cm, $E_G \simeq 1.3 \times 10^6$ v/cm)

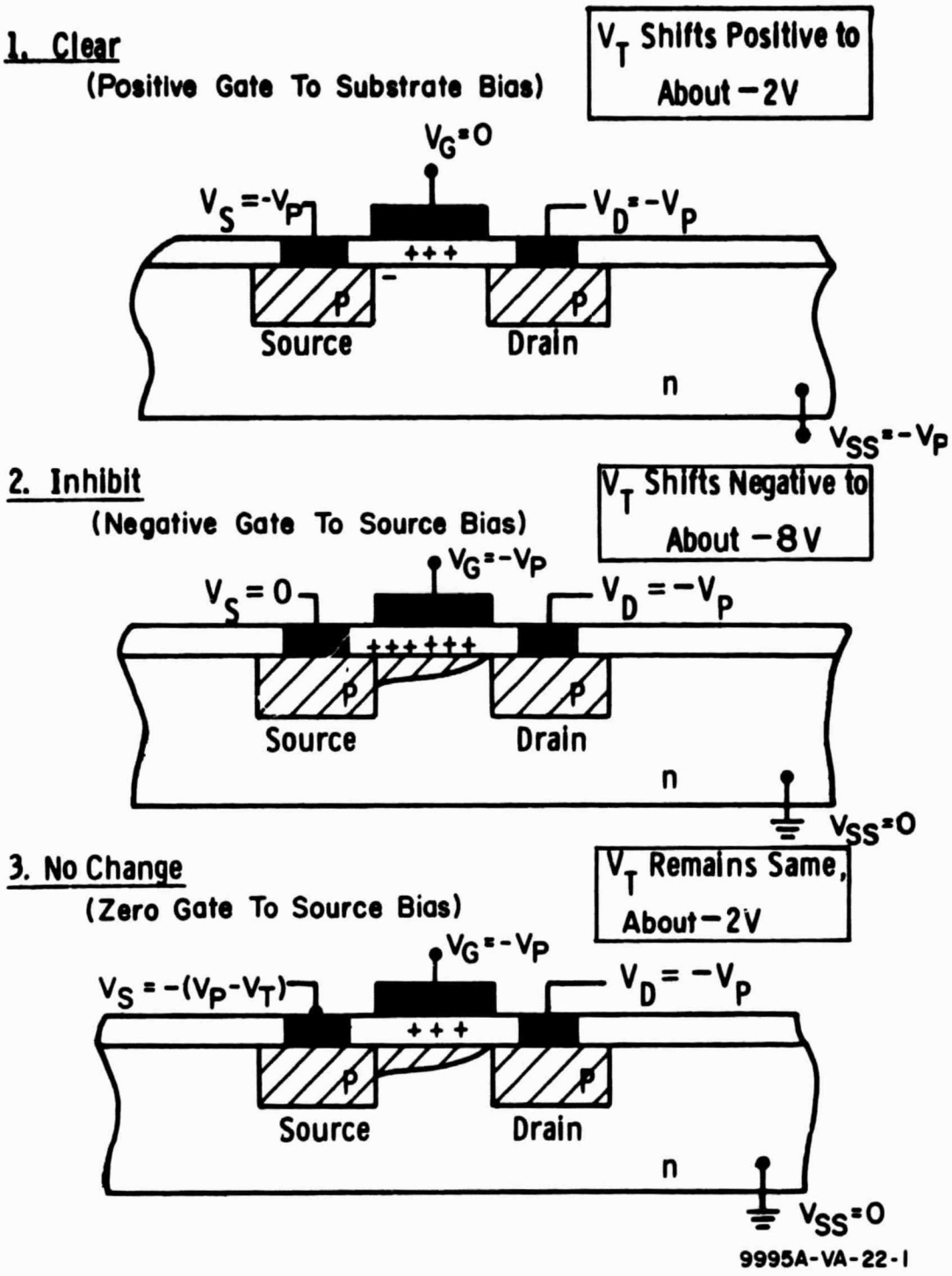


Figure 15. Gate to Source Polorization (Channel Shielding) Modes of Operation.

is applied ($V_G = -V_P$) with respect to the source ($V_S = 0$). Under this condition, notice that the p-channel MIS transistor is turned on such that a p-type surface channel exists. In the inhibit mode, the threshold voltage is made to shift negative. If the threshold voltage is made more negative than the read sense voltage, then the device will not turn on during the read operation. In the last mode of operation, shown in figure 15 the source voltage is made about equal to $-V_P$ when the gate polarizing voltage ($V_G = -V_P$) is applied. Since the gate-to-channel voltage is only about a threshold voltage V_T, the device is not polarized and the threshold voltage V_T remains the same.

A breadboard of a 4 bit read/write memory array has been fabricated, and delivered for this task. The operation of the breadboard memory is based on a memory word clear (erase) period followed by a write period. A schematic of a Westinghouse read/write MNOS memory system including timing waveforms is shown in figure 16. The breadboard memory represents a four bit segment of this type of memory. The addressing and read/write logic is achieved with switches in the breadboard. Four transistors are bonded together in each package to form the MNOS memory.

The timing and voltage waveforms for operation of the decoder/driver and memory array sections are also shown on the memory schematic, figure 16. The basic drain supply voltage V_{DD} common to both decoder/driver and memory array varies between -30V during the clear (erase) and write periods and -15V during the read period. The inverter-load-device gate supply voltage V_{gg} varies between -30V during the clear and write periods and -20V during the read period to provide maximum current drive and thus faster response times. Also, the output voltage of the memory output drivers is then the full value of the V_{DD} supply voltage since $|V_{gg} - V_T| \geq |V_{DD}|$ The nominal logic levels

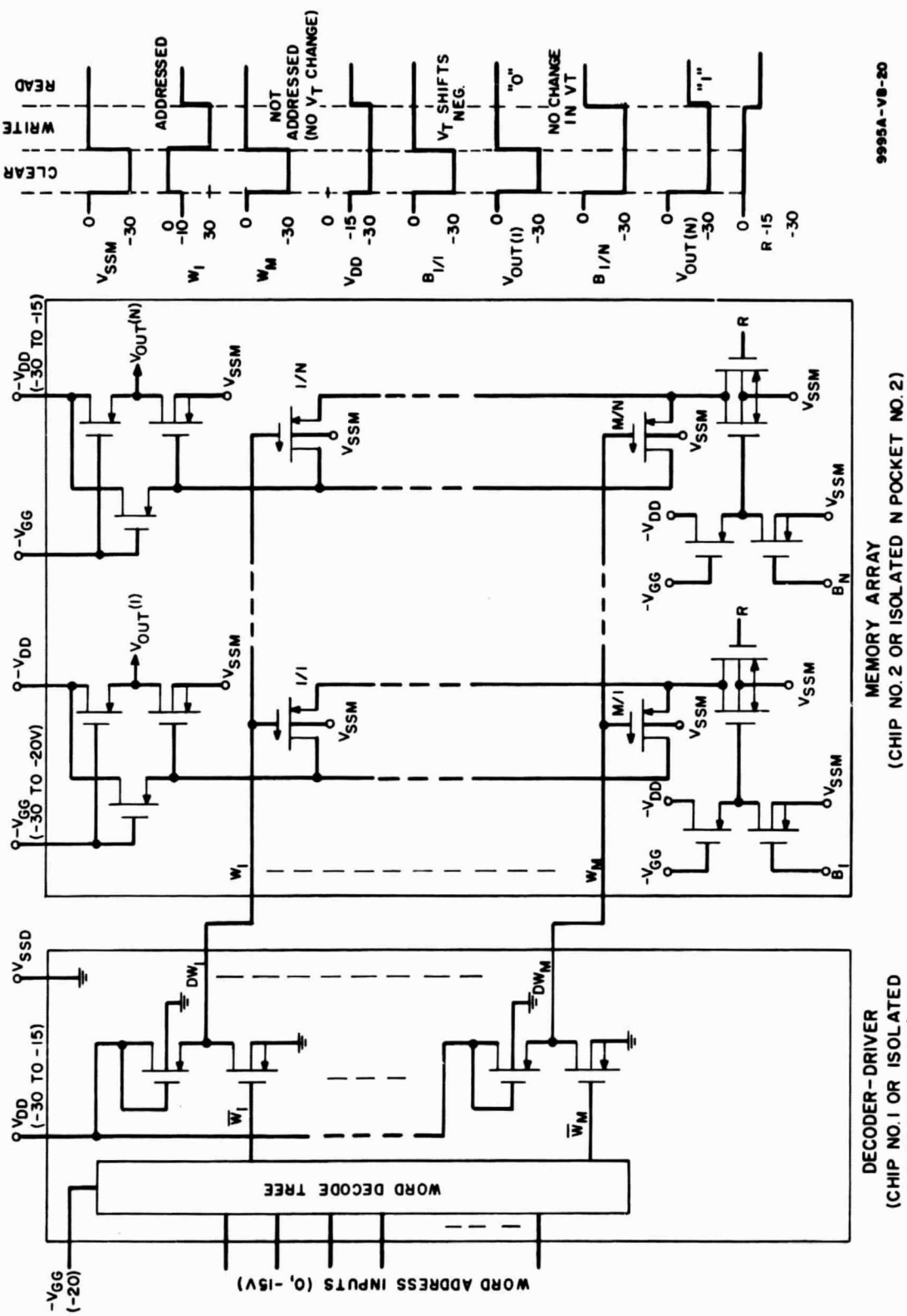


Figure 16. Array Schematic Diagram and Waveforms

for the address inputs, address decoder, bit-line inputs and memory outputs are "1" = -15V and "0" = 0 V, thus all of the input/output levels are compatible with p-channel logic design. Internally, the logic levels for the word lines W_1 through W_M are 0 or -30V during the clear and write periods and are 0 V and $-(15V-V_T) \cong -10V$ during the read period.

The most significant feature of this array design is that the positive clear (earse) bias of the gate with respect to the substrate is achieved by pulsing the memory array substrate (V_{SSM}) to -30V while grounding the word line that is to be cleared (erased). The nonaddressed words have the word line voltage also at -30V to prevent loss of stored charge. These cases are illustrated in the timing diagram in figure 16. The advantages of this approach is that the word driver and all of the associated address decoder is not required to switch between +3- and -30V and all of the input/output voltage levels remain compatible. Also, no junction or gate ever sees more than a 30V bias.

When the bit line is a logical "0" = 0V during the write period such as for $B_{1/1}$ in the timing diagram, the source of each memory device on bit line 1 also goes to 0V. Thus, since word line 1, W_1 is at -30V, the gate-to-chennel bias is nearly 0 V and no threshold voltage shift occurs. The non-addressed memory devices (W_N =0) remain in the off condition, the gate-to-substrate bias is 0 V, and no threshold voltage shift occurs.

During the read period, the read signal R is biased to -15v; thus, the source of each memory device is essentially at ground potential. In the case of memory device 1/1, assume the threshold voltage has been shifted to a negative value of about -10v. When the word line W_1 for the read period is -10v the memory device is off making the memory device drain voltage negative which in turn makes V_{OUT} (1) = 0 V. It is easy to adjust the read (or sense) value

of W_1 to be about the value of the most negative threshold voltage of the memory devices to make this case valid.

In the case of N^{th} bit of word one, the threshold voltage has been shifted to its most positive value, but not to depletion mode for the values of supply voltage shown. If the devices are shifted to the depletion mode, then the substrate voltage of the decoder (V_{DSS}) called the offset voltage and the logical "0" voltage level of all of the address inputs must be shifted from 0 to a slightly more positive voltage; (i.e., from 0 to +4 V). This is possible because the substrate of the decoder/driver is isolated from the memory array. It has been observed that oxides thermally grown on p channel MNOS transistors exhibit a lower gate breakdown voltage than capacitors on the same wafer. This is attributed to different oxide characteristics for the oxide over the P+ diffused source and drain regions. N channel transistors; however, do not exhibit the same problem. The lower gate breakdown of the p channel transistors limits the switching speed that can be achieved with thermally grown oxides.

3.0 Conclusions

Experiments have shown that thermally grown oxides with reduced O_2 partial pressure are capable of producing oxides less than 100 Å thick. These thin thermal oxide nitride structures do not appear to have deep traps at the insulator interface, and thus have poorer retention than comparable deposited oxide structures. Because of the higher conductivity of the oxide, however, it is possible to achieve switching and storage with 20v, 100 nanosec pulses. N channel transistors are the preferred type using the thin thermal oxide because of the anomolous behavior exhibited by the p channel MNOS transistors which is related to the conductivity of the thermal oxide over the P+ source and drain diffusions. Passivated MNOS devices are optimized with respect to maximum trans-conductance and stability when the oxide is much less than the nitride thickness provided the voltages applied do not produce fields greater than 2×10^6 v/cm. Other, more conservative options that trade off transconductance for lower fields are possible. These processes are predictable and reproducable; and therefore, the MNOS devices may be readily used in nitride passivated arrays or charge storage memory arrays.

REFERENCES

1. J. R. Szedon and T. L. Chu. "Tunnel Injection and Trapping of Electrons in Al-Si_3N_4-SiO_2 Silicon (MNOS) Capacitors," IEEE Solid State Device Research Conference, Santa Barbara, Calif., June 1967.

2. M. Lenzlinger and E. H. Snow. "Fowler-Nordheim Tunneling into Thermally Grown SiO_2," Journal Appl. Phys., Vol. 40, p. 278, Jan. 1969.

3. S. M. Sze. "Current Transport and Maximum Dielectric Strength of Silicon Nitride Films," Journal Appl. Phys., Vol. 38, p. 295, June, 1967.

4. T. L. Chu, J. R. Szedon, and C. H. Lee. "The Preparation and C-V Characteristics of Si-Si_3N_4 and Si-SiO_2-Si_3N_4 Structures," Solid State Electronics, X, (1967), p. 897-905.

5. J. R. Szedon and T. L. Chu, Ibid.

6. F. A. Sewel, Jr., H. A. R. Wegener, and E. T. Lewis. "Charge Storage Model for Variable Threshold FET Memory Element," Appl. Phys. Letters, Vol. 14, p. 45, 15 Jan. 1969.

7. D. Frohman-Bentchkowsky and M. Lenzlinger. "Charge Transport and Storage in Metal-Nitride-Oxide-Silicon (MNOS) Structures," Journal Appl. Phys., Vol. 40, No. 8, July 1969, pp. 3307-3319.

8. H. A. R. Wegener, F. A. Sewell, Jr., "MIS Transistor for Use as a Non-volatile Digital Storage Element," AFAL-TR-69-187, July 1969, p. 12.

9. B. E. Deal and A.S. Grove, Journal Appl. Phys., 36, 3370, (1965).

10. W. A. Pliskin, E.B.M. Journal, 10, 198, (1966).

11. B. E. Deal and M. Sklar, J. El. Chem. Soc., 112, 430, (1965).

12. B. E. Deal and A. S. Grove, SAP 36, 3770, (1965).

13. SCEPTRE, AFWL-TR-67-124.