A DESCRIPTION OF THE TIME INTERVAL MEASUREMENT AND LASER CONTROL CIRCUITRY FOR THE LUNAR RANGING EXPERIMENT

by

C. A. Steggerda

Technical Report No. 70-049

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UNIVERSITY OF MARYLAND
DEPARTMENT OF PHYSICS AND ASTRONOMY
COLLEGE PARK, MARYLAND

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College Park, Maryland

ABSTRACT

The laser control and time interval measurement circuits when combined with a detector package, a laser and an astronomical telescope form the McDonald Lunar Ranging System. This system is designed to measure the time of flight of a light pulse to a lunar retro-reflector and back to an accuracy of 1 nanosecond with a precision of 100 picoseconds. The range is computed by adding an analog measurement of the time between the outgoing laser pulse and an initial frequency standard clock pulse, subtracting a similar analog measurement between the return pulse and a final frequency standard clock pulse and counting the number of frequency standard pulses between initial and final pulses.

To prevent the system from measuring random photons, a window pulse is provided to activate the final Time to Pulse Height converters some time delata before the laser pulse is due to return. The Lunar Ephemeris, recorded on magnetic tape and read by a Varian Data Machines 620/i computer, is used to generate this window pulse.

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ACKNOWLEDGMENTS

The author wishes to acknowledge the assistance given by Drs. Carroll Alley, Douglas Currie and Sherman Poultney in developing this equipment.

The original concept of timing the flight of a laser light pulse to and from the moon using a computer, time to pulse height converters and clocks was developed by Dr. Poultney in consultation with Dr. Robert Detenbeck and Dr. Douglas Currie. The author is responsible for collecting the ideas and converting them into Circuits and with the assistance of Dr. Poultney writing specifications for purchasing commercial equipment.

Acknowledgment is due Dr. Robert Glasser, Don Day, and John Rayner for discussions on the basic timing philosophy and computer logic. The author wishes to thank Dr. Eric Silverberg for interrupting work on his thesis to build the Logic Control Circuit. Mr. Steve Silverman of Computer Operations Inc. and Mr. Jerry Felper of Astrodata contributed to the project's success by supplying special equipment on very short notice. Particular recognition is due Mr. John Mullendore who acted as project manager and co-ordinator.

The author wishes to thank Mr. Larry Pharr who did the drafting and Miss Carol Tabb who typed this report.

INTRODUCTION

A computer controlled system has been devised to operate an earth-based laser and time measurement system to accurately measure the time of a flight of a laser beam to and from a reflector on the moon.

This report deals with the computer system which controls the laser and records and displays the data, and the time interval measurement equipment which measures the time interval between a pulse generated by a photo diode monitoring the laser and a pulse generated by a photo multiplier monitoring the return from the moon.

A report dealing with the photomultipliers and the detector package has been written by S. K. Poultney[1]. The time keeping system with VLF receivers and WWV calibration procedures is reported by S. K. Poultney[2]. The programming for the computer, computer operation and peripheral equipment operation is described in a report by J. Rayner[3].

The equipment described in this report is constructed using Ortec[4] and Eldorado[5] commercial components modified to suit the purposes of the experiment. Additional special equipment is supplied by Astrodata[6] and Computer Operations[7]. The computer used is a standard 620/i by Varian Data Machines[8] and the recorders are manufactured by Digi-Data[9]. A complete list of all of the discrete boxes appears in Appendix A. The reader should become

familiar with the characteristics of each unit by obtaining the instruction manuals. Diagrams of all modifications to each of the discrete boxes are given in the appendices. Because of the modular nature of the equipment, due to the extremely short time in which the equipment was developed, improvements or changes can be made easily.

The main body of the report is divided into three sections. The first section describes what is required of lunar ranging equipment and how these measurements can be made. This section compares and contrasts several methods for control of the laser and measuring the lunar ephemeris. The second section describes in detail how the Maryland lunar ranging system operates. The third section describes a number of tests that can be made to determine correct operation.

The appendices contain a description of what changes are made to commercial units. However, because it is not practical to reproduce the instruction manuals of the commercial equipment, these appendices are meant to complement rather than replace the commercial manuals. Appendix A contain a picture of the system, a description of the components, a list of all the cables with their lengths, and a check list of all the switch positions for normal operation.

There have been questions asked as to why the Hewlett Packard type 5360 counter[10] was not used instead of developing new circuits. The answer is that at the time this system was being built, Hewlett Packard had just announced the new counter on an experi-

mental basis. The author had a lengthy discussion with Gilbert Reeser, the development engineer of the 5360A unit. It was decided that we could build a unit with at least as good accuracy and precision and have much more capability for analysis of data, including the ability to analyze more than one stop pulse. In addition, if the Hewlett Packard unit were used, many other items would still be necessary such as a gating system to select pulses near the expected time of arrival including tape reading and writing equipment.

References

1. S. K. Poultney Maryland Report #70-021

2. S. K. Poultney Maryland Report #957

3. J. Rayner Maryland Report #70-064

4. Ortec, Inc., a division of E G and G
   100 Midland Road
   Oak Ridge Tennessee 37830

5. Eldorado Electronics
   601 Chalomar Road
   Concord, California 94520

6. Astrodata Corporation
   E. Palais Road
   Anaheim, California

7. Computer Operations, Inc.
   10774 Tucker Street
   Beltsville, Maryland

8. Varian Data Machines
   2722 Michelson Drive
   Irvine, California 92664

9. Digi-Data Corporation
   4315 Baltimore Avenue
   Bladensburg, Maryland 20710

10. Hewlett Packard Corporation
    1501 Page Mill Road
    Palo Alto, California 94304

SECTION I

PHILOSOPHY OF THE MEASUREMENT

There are two basic tasks that the equipment in this experiment must perform. The first task is to generate a laser light pulse whose absolute time of generation is known to one or two microseconds. The second task is to measure the time interval between the laser light pulse leaving the telescope and returning from the reflector on the moon to an accuracy of one or two hundred picoseconds. There are several ways that these measurements can be made. This section discusses some of the methods of measurement, the problems associated with each and indicates the procedures used in the McDonald Observatory System.

A. Laser and Photomultiplier Activation Control

The equipment must either fire a laser so that the resultant light pulse leaves the telescope at a precisely predetermined time or be able to measure the time of light pulse generation precisely. The accuracy of the timing of the laser pulse depends on the accuracy of the clock and how well it is synchronized to the basic time standard. Regardless of the accuracy of the measurement, the precision should be one microsecond and synchronized to the system time of day clock. Then, as time standards and synchronized methods become more sophisticated, the system will not be limited by its precision.

It is also necessary to know within a few microseconds

when the pulse is due to return so that a receiving window may be opened to receive the returning light pulse while rejecting all other noise and ambient light. At the beginning of these lunar ranging experiments the uncertainty of the lunar ephemeris was three microseconds. Thus, to ensure that the gate is not opened too late, it is expeditious to open a 6 microsecond window 3 microseconds early. This early opening allows many noise pulses to be accepted, especially when viewing a bright moon. As the lunar ephemeris is improved, the window may be opened closer and closer to the return pulse thereby eliminating noise. It is hoped to eventually open the window ten nanoseconds before the lunar return is expected thus requiring nine decimal digits of ephemeris. Two methods for achieving the laser control and window opening are discussed below.

If the laser light pulse can be synchronized to particular one second pulses of an atomically synchronized clock, then the ephemeris can be pre-calculated and stored on magnetic tape. This synchronous system has the advantage that all of the calculations necessary are done in a large computer capable of solving the ephemeris equation with twelve decimal digit accuracy without resorting to multiple precision routines in the small control computer. The laser firing process is a two-stage affair in which first the flash lamps are fired, then, after an interval of typically one millisecond, the Pockel cell is triggered. The time interval between the two is dependent on many factors such as energy of the light pulse and age of the flash lamps. In the synchronous mode the computer controlled

circuitry is required to make the small adjustments necessary for efficient operation of the laser.

If the time of light pulse generation is not in synchronism with the one second pulses of the clock, it must be measured. The computer must calculate the expected time of each laser return. While this puts a burden on the small computer if very precise calculations are to be made, there are several advantages. First, the laser power supply electronics need not be modified. Secondly, the computer can store all of the necessary constants for the lunar ephemeris equation in core, thus eliminating the need to read tape. The third advantage is that the rate of laser firing can be changed to suit the laser conditions and is not fixed by the firing times precalculated on magnetic tape. The procedure for determining the time of laser pulse generation is to measure the time interval between the laser light pulse and a known time from the precision clock such as a millisecond pulse.

The design as originally conceived would have used the non-synchronous approach using the computer to solve an interpolation series. The computer would store the lunar ephemeris for intervals of every half hour and calculate from this the range at any time. However, because the 620/i is a small computer and high precision accuracy would have to be done using double or greater precision, rather ingenious programs would have had to be developed to do the computations in the required three seconds. Because of the lack of programming time, the synchronous mode of operation was chosen in which the lunar ephemeris is precalculated

on magnetic tape for every three seconds.

In actual operation, the Space Rays laser could not be fired more often than every six seconds, and using the Korad laser it was found that the flip mirrors limited the rate to every four seconds. It is probable that the computer could have been programmed to provide the range ephemeris for each shot.

B. Time Interval Measurement

There are many systems for measuring time interval. The number of methods decreases sharply when the time interval to be measured is in the order of seconds and the precision required is 100 picoseconds.

Most systems use a combination of digital and analog circuits, the digital circuits to count an atomically synchronized clock used for determining precise intervals during the seconds interval and analog circuits to measure the time between the known clock pulses and the system start and stop pulses. Two of these combination systems are considered below.

Using System X, an analog sweep is started with the start pulse generated by a photo diode or other Laser monitor. In addition, this start pulse opens the gate for a high speed digital counter which counts a precision clock. The first counted clock pulse stops the analog sweep. The voltage thus present on this sweep represents the time interval between the laser pulse and the precision clock pulses. The high speed counter then counts to a fixed number just short of when the pulse is expected from the reflector and opens a gate to receive the incoming pulses and at the same time starts a second sweep. The successful return pulse stops the sweep. The sweep voltage is a measure of the time between a known clock pulse and the return pulse from the reflector. The total time interval between leaving and returning laser pulses is the time equivalent of the sum of the two sweep voltages plus the high speed counter reading minus one clock period.

Method X is straightforward and would work well provided the range ephemeris is known to several hundred nanoseconds and if the range window, whose resolution is determined by the clock frequency, could be opened at fixed points. If the clock is 20 MHz, then the window may be opened on any fifty nonosecond step.

The disadvantage of Method X is that if the range is not known precisely, then the window must be opened tens of microseconds early and the sweep range on the final verniers must be changed so that the sweep operates when the return pulse arrives. As the precision of the ephemeris increases, the window may be moved closer to the return pulse, and the final vernier may be correspondingly reduced. The disadvantage arising from this procedure is that a number of sweeps of different slopes must be used. Each must be separately calibrated and accurate records kept when data is collected to indicate which sweep was used.

Method Y is similar to Method X for the initial verniers but is altogether different for the final vernier sweep. Method Y uses the return pulse from the reflector to start the final vernier sweep and stop a counter. The first clock pulse that the counter does not count is used to stop the final sweep. In Method Y, the time interval is measured by the high speed counter reading plus the difference of the two verniers; the final sweep being subtracted from the initial. Method Y is not as straightforward and uses more equipment. However, only one sweep range is ever needed for the final vernier and because an extra window opening control is needed, the window opening can be controlled to a few nanoseconds. No changing of sweep ranges is necessary,

thus eliminating a possibility of error. Method Y makes it possible to use the same sweep circuit and photo detector for the initial and final vernier because the start pulses for the sweep always come from the photomultiplier or photo diodes while the stop pulses are always clock pulses.

The circuit chosen uses the concepts of Method Y with the exception that the initial and final sweep circuits are independant. An additional provision is made to receive two return signals from the same outgoing laser pulse. This feature is desirable if several photons are received from different portions of the laser return pulse. With very little modification a third photomultiplier channel could be added.

C. Choice of Clock Frequency

The higher the clock frequency the smaller the amount of time that the sweep circuits must operate. However, as the clock frequency increases, the digital control circuitry becomes more difficult to operate correctly. 20 MHz was chosen as a compromise in which the digital and analog circuits both work well. Probably 10 MHz would work equally well and simplify programming by making the basic time interval 100 nanoseconds instead of 50 nanoseconds.

D. The McDonald Observatory System

The McDonald Observatory system uses the synchronous method of laser control in which the laser pockel cell is fired from a known one second clock pulse. Two milliseconds before the Pockel cell firing, the Varian 620/i computer initiates a series of delay circuits enabling the laser flash lamps to fire the required time before the Pockel cell.

To prevent the system from measuring random photons, a window pulse is provided to activate the final Time to Pulse Height converters just before the laser pulse is due to return. The lunar ephemeris is precalculated for specific one second intervals and stored on magnetic tape. The computer reads this tape, synchronizes it with the Time of Day Clock, subtracts a fixed time called delta from the lunar ephemeris, and loads the ephemeris into the Time Delay Generator. The Time Delay Generator is started by the laser light pulse, as sensed by a photo diode, to provide a window pulse to activate the Time to Pulse Height converters at the appropriate time.

The precision ranging electronics uses the concepts of method Y as previously outlined. The range is computed by taking an analog measurement of the time between the outgoing laser pulse and an initial frequency standard pulse, doing a similar analog measurement between the return pulse and a final frequency standard pulse and counting the number of frequency standard pulses between initial and final pulses.

The analog and digital measurements with the time of day of the measurement are then recorded on a second magnetic

tape system by the computer. The computer simultaneously converts the analog voltages and the number of frequency standard pulses to a time interval of 100 picosecond precision and types the number.

The McDonald system uses a light sensing photo diode to sense the outgoing laser light pulse and two photomultipliers to detect photons from the return pulse. This system, using the two photomultipliers with independent Time to Pulse Height converters, permits measurement of the time of flight of two photons in the laser pulse.

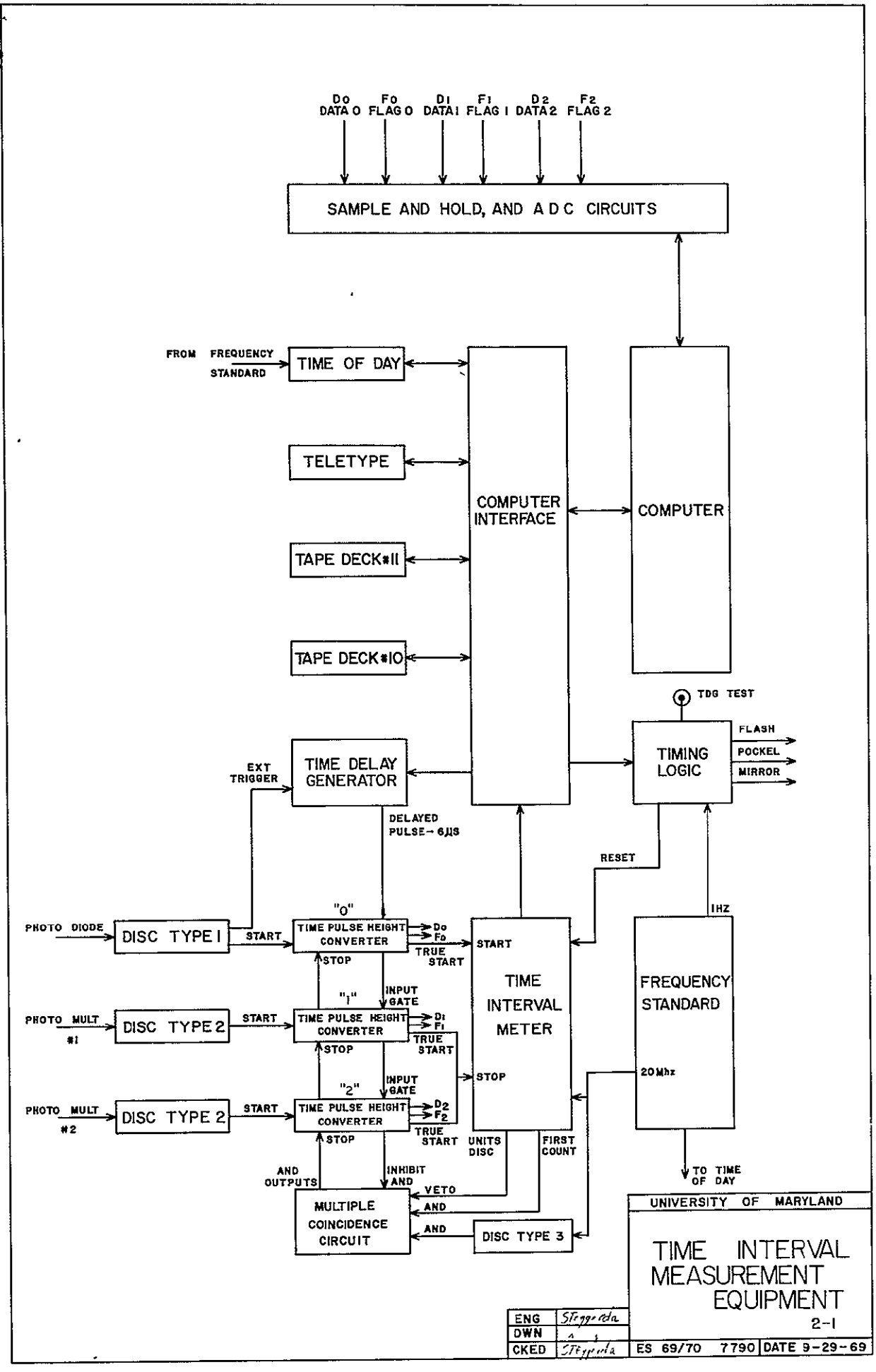
SECTION II

DESCRIPTION OF THE CIRCUITS

A block diagram of the laser control and timing electronics is shown in figure 2-1. The mode of operation is as follows.

A magnetic tape of the lunar ephemeris with the date and Greenwich time has been recorded for every 4 second interval in which the moon is above the horizon. The system computer reads this tape via a Digi-Data Model 1300 tape recorder and compares the current time read from an Astrodata Model 7190 time of day clock. Tape is reeled forward until the time information on the tape is in synchronism with the time of day clock at which time the computer reads a record containing all the ephemeris predictions for a 1 minute interval. The number of warmup (flash tube only) shots that are desired, the number of complete shots (laser firing) and finally the delta, meaning the number of nanoseconds to be subtracted from the ephemeris, are all typed on a model ASR-33 teletype and read by the computer. The computer routine is initiated by typing G and carriage return.

Two milliseconds before each 4 second pulse for which the ephemeris has been calculated, the computer sends an EXC 060 computer command pulse to the Eldorado model 650 Time Delay Generator (TDG) to strobe ephemeris information to the TDG. In addition, the computer sends a pulse via computer command

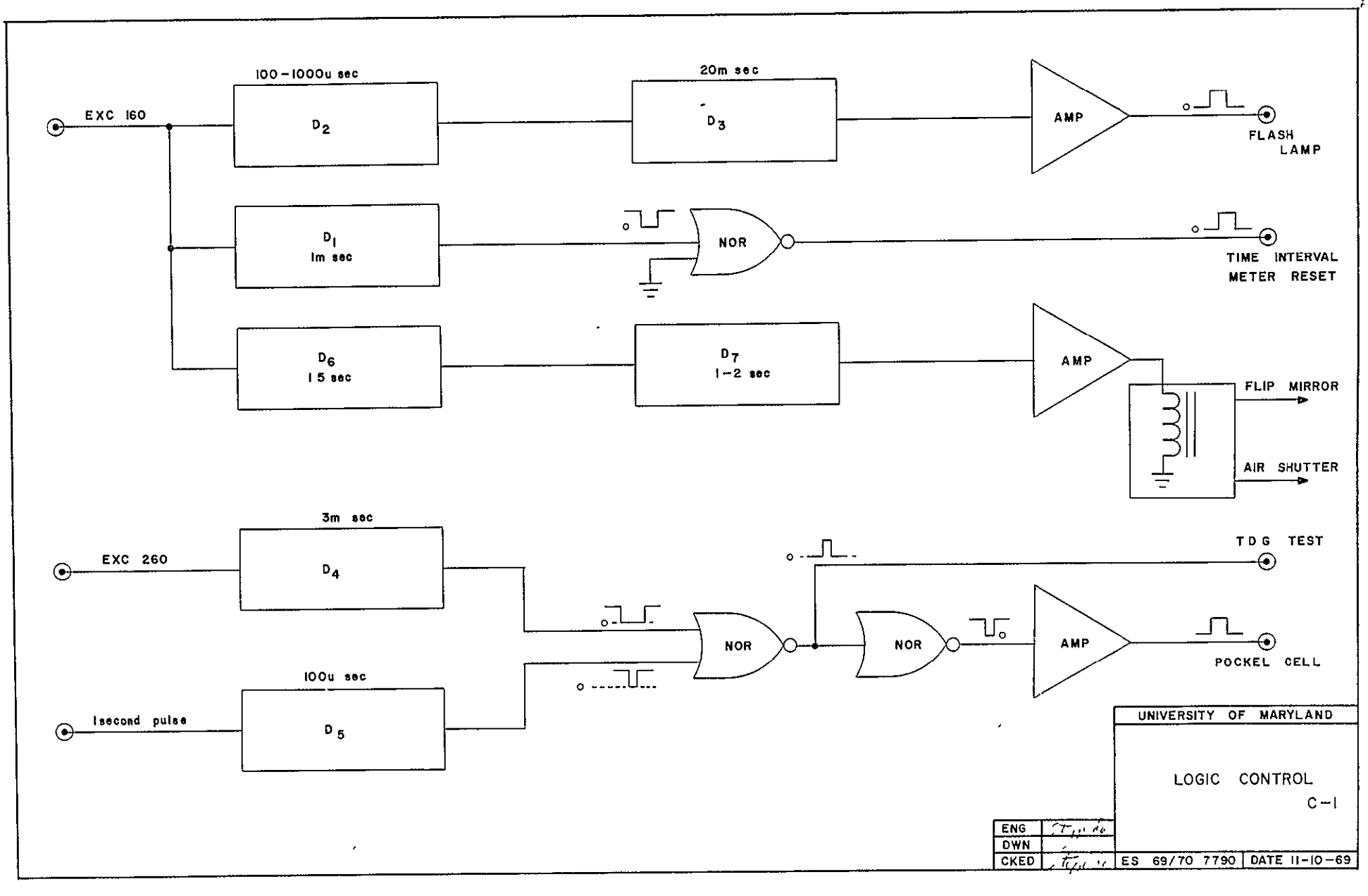

D0 DATA 0
F0 FLAG 0
D1 DATA 1
F1 FLAG 1
D2 DATA 2
F2 FLAG 2
SAMPLE AND HOLD, AND A D C CIRCUITS
FROM FREQUENCY STANDARD
TIME OF DAY
TELETYPE
TAPE DECK#11
TAPE DECK#10
COMPUTER INTERFACE
COMPUTER
TDG TEST
TIMING LOGIC
FLASH
POCKEL
MIRROR
EXT TRIGGER
TIME DELAY GENERATOR
DELAYED PULSE→ 6μs
RESET
"0"
PHOTO DIODE
DISC TYPE 1
START
TIME PULSE HEIGHT CONVERTER
D0
F0
TRUE START
STOP
START
TIME INTERVAL METER
1HZ
FREQUENCY STANDARD
"1"
INPUT GATE
PHOTO MULT #1
DISC TYPE 2
D1
F1
20Mhz
"2"
PHOTO MULT #2
DISC TYPE 2
D2
F2
UNITS DISC
FIRST COUNT
AND OUTPUTS
INHIBIT AND
VETO
AND
MULTIPLE COINCIDENCE CIRCUIT
DISC TYPE 3
TO TIME OF DAY
UNIVERSITY OF MARYLAND
TIME INTERVAL MEASUREMENT EQUIPMENT
2-1
ENG
DWN
CKED
ES 69/70 7790
DATE 9-29-69

EXC 160, to the logic control circuitry, shown in block diagram in Figure C-1, to start a delay "one-shot" of approximately 1020 microseconds simultaneously with a reset pulse for the Eldorado Time Interval Meter. 980 microseconds before the one second clock pulse, the flash lamps are fired. This sequence is repeated until the warmup cycle is complete.

The main sequence in which the laser is fired occurs when both the EXC 160 and EXC 260 pulses are sent to the logic control circuit. The EXC 260 pulse fires a one shot D-4 which asserts one half of a NAND gate. The one second clock pulse from the Astrodata 7190 clock arrives at time zero and asserts the second half of the NAND gate via one shot D-5. The output from the NAND gate fires the pockel cell after suitable polarity changes and amplification. (Please note that while figure C-1 shows a NOR module, inverted logic is used causing the module to act as a NAND module).

The EXC 160 pulse starts a series of one second one-shot delays which prepare the mirror to flip from the transmit to the receive mode and open a shutter. Two seconds after the laser fires, the mirror flips to the receive mode and the photomultiplier protective shutter opens. The schematic diagram for the logic control is shown in Appendix C, diagram C-2.

3.25 microseconds after the selected clock pulse has been sent to the Pockel cell, a return pulse arrives from the photo diode indicating the laser has fired. The Korad photo diode, described in the Korad KD1 manual, sends a very fast positive pulse to a type one discriminator, described in Appendix H. The output of the type one discriminator is


EXC 160
100 – 1000u sec
D2
20m sec
D3
AMP
FLASH LAMP
D1
1m sec
NOR
TIME INTERVAL METER RESET
D6
1 5 sec
D7
1–2 sec
AMP
FLIP MIRROR
AIR SHUTTER
EXC 260
3m sec
D4
TDG TEST
NOR
NOR
AMP
POCKEL CELL
1second pulse
100u sec
D5
UNIVERSITY OF MARYLAND
LOGIC CONTROL
C–1
ENG
DWN
CKED
ES 69/70 7790
DATE 11-10-69

used to start an Ortec Model 437-A Time to Pulse Height Converter and to start the Eldorado Model 650 Time Delay Generator. In addition, the Eldorado Model 783G Time Interval Meter gate is opened so that it may start counting clock pulses. Logically, it is desirable to start the TIM with one of the negative .70 volt three nanosecond pulses from the type one discriminator. It was found, however, that these pulses were not of sufficient power, and, consequently, the true start pulse from the 437-A is used. The true start pulse is modified to be of negative output, and the normal 27 nanosecond delay is reduced to 10 nanoseconds. The modifications to the 437-A are shown in Appendix B.

Approximately eight nanoseconds after receiving the true start pulse from TPHC #0, the input gate of the TIM is opened allowing the TIM to count pulses derived from the 20MHz sine wave from the frequency standard.

As can be seen from fig. 2.1, the 20 MHz sine wave is applied to both the input of the TIM and a delay cable leading to a Type 3 discriminator. The internal circuits of the TIM discriminate the sine wave and cause the counter to shift in synchronism with the 20 MHz source. The units digit of the TIM is a set of five flip flops connected in a ring. When the first count is registered, the number one flip flop changes state causing the first count output to shift from zero to minus one volt. This output is connected to the EG&G C104AN multiple coincidence circuit #4 AND circuit. The #3 AND input coincidence is connected to the Type 3 discriminator which supplies the delayed clock

pulses. The delay is necessary to establish gate levels before the Delayed Clock pulse arrives. The first count level and the Delayed Clock pulse are used in coincidence to form an AND pulse which is used to stop all three TPHCs, however during the initial vernier calculations, only TPHC #0 is in operation. The TPHC sweep is started by the photo-diode pulse and stopped by a Delayed Clock pulse. The TPHC gives a pulse whose amplitude is proportional to the time interval. The normal TPHC has been changed to accommodate the Astroverter ADC system as is shown in Appendix B. The Data pulse is 5.5 microsecond duration instead of the normal 1 microsecond doublet. A 4 microsecond pulse is generated whose leading edge is co-incident with the data pulse. The sample and hold circuit of the ADC samples the analog output for 4 microseconds and holds the value when the read pulse disappears. The data pulse, whose amplitude contains the initial vernier sweep information, is sampled after 4 microseconds.

The sampling process sets a flag notifying the computer that data is present on one of three channels. The computer acknowledges the flag and sends an EXC 065 pulse to the Astroverter, causing the multiplexer to connect #0 channel to the digital converter and initiate the conversion process. An EXC 165 pulse would connect the #1 TPHC to the ADC etc.

When conversion is complete, the Astroverter sets a flag indicating that a number can be read from the output buffer. The number read is a coded octal representation of the voltage from the TPHC. A calibration, which is discussed later, is necessary to convert this voltage to a time interval. A discussion

of the Astroverter modifications is supplied in Appendix G.

To review what happened:

The computer has synchronized the magnetic tape ephemeris with the time of day clock so that every six seconds an ephemeris is sent to the TDG. The laser has been warmed and in due course fired by a clock pulse from the frequency standard. A pulse has been received from the photo diode indicating the laser has sent a light pulse. The photo diode pulse was shaped by a discriminator and used to start a TPHC and the TDG. The true start pulse from the TPHC opened the input gate of the TIM and allowed the counter to count the clock pulses. The first counted clock pulse was used to open a coincidence gate. A Delayed Clock pulse was then allowed through the gate to stop the TPHC. The computer and Astroverter then read a voltage pulse from the TPHC and convert this pulse to a time interval of 100 picosecond resolution.

At this time the TIM is counting clock pulses, and the computer is free to update range information or other tasks as described in J. Rayner's article.

Two seconds after the laser is fired, the logic control circuit sends a pulse to the flip mirror and the shutter to position the detector package for receiving the return.

At the range ephemeris minus delta, the TDG sends a positive 6 microsecond pulse to the input gates of the two receiving TPHCs. The TPHCs then can receive a signal from the photomultipliers and their respective discriminators during this window pulse. Normally, the window is set to open a few microseconds early so that there is no possibility of losing a return.

The true start outputs of the two final vernier TPHCs are ORed together so that if either channel receives a return pulse it can be used to close the input gate of the TIM. The final sweep vernier starts with this return pulse, the problem is to stop the sweep with either the last clock pulse counted or the first clock pulse not counted. The methods used to determine either of these particular stop pulses are similar; they require having a circuit which reacts as soon as the counter stops counting. At low frequencies, any number of integrating circuits work, but in this case the circuit delay time after the last counted pulse must be about 25 nanoseconds. The circuit capable of this requirement is the Maryland Units Discriminator (MUD) described in Appendix E. Every time one of the five flip flops in the units counter changes state, a twenty nanosecond negative pulse is generated and sent to the VETO input of the Multiple Coincidence circuit. If the VETO level is present, the Delayed Clock pulses are blocked and cannot stop the sweep. As soon as the VETO is not present, signifying that the TIM is stopped, the following Delayed Clock pulse stops the sweep in the final TPHCs.

The 6 microsecond window pulse is used to inhibit the #4 AND circuit of the coincidence circuit. To see the necessity for this, remember that the #4 AND is connected to the output of the first flip flop in the units decade of the TIM. Half of the time this flip flop is in the "1" state and half of the time in the "0" state. During the "0" time, the Delayed Clock pulses are eliminated in the AND circuit. This makes it possible never to receive a stop pulse from the coincidence should the counter stop on counts five through nine. For this reason, during the final vernier, the #4 AND is inhibited so that only the Delayed Clock pulses and the VETO system are in operation. A logic diagram of the coincidence circuit is shown in Appendix D, figure D-1.

It may logically be asked; if a VETO pulse is produced for every unit count of the TIM, why is it possible to receive an initial vernier stop pulse?

From the previous discussion we note that the first counted pulse from the TIM enables the #4 AND gate in the multiple coincidence circuit and allows the Delayed Clock pulses through the AND section. This same first counted pulse is expected to generate a VETO pulse which blocks the Delayed Clock. In the initial design a special "Inhibit the VETO" circuit was added to kill the VETO capability during the initial vernier. This circuit was found unnecessary however because the units discriminator needs a few pulses to become operational. When the units discriminator is started, it always neglects the first 2 counts, thus, the VETO pulse is absent for the first count allowing a

stop pulse to occur.

Delayed Clock. The reasons why the Delayed Clock is necessary are now discussed. In any non-synchronous gating system, such as occurs in the TIM with the 20 MHz clock and the non-synchronous laser start and return pulses, there are always some pulses which are of reduced amplitude due to turning on or off the gate during a clock pulse. The reduced amplitude pulses have amplitudes ranging from zero to a normal pulse and they may or may not trigger the counting flip flops. Worse yet, a pulse may be of an amplitude such that the flip flop operates in an analog mode giving a pulse output rather than changing state. When this effect occurs at the first count, a pulse is sent to the MUD circuit while the counter remains in the zero state. If this false first count pulse is used, an error occurs and leads to a range being 50 nanoseconds too short.

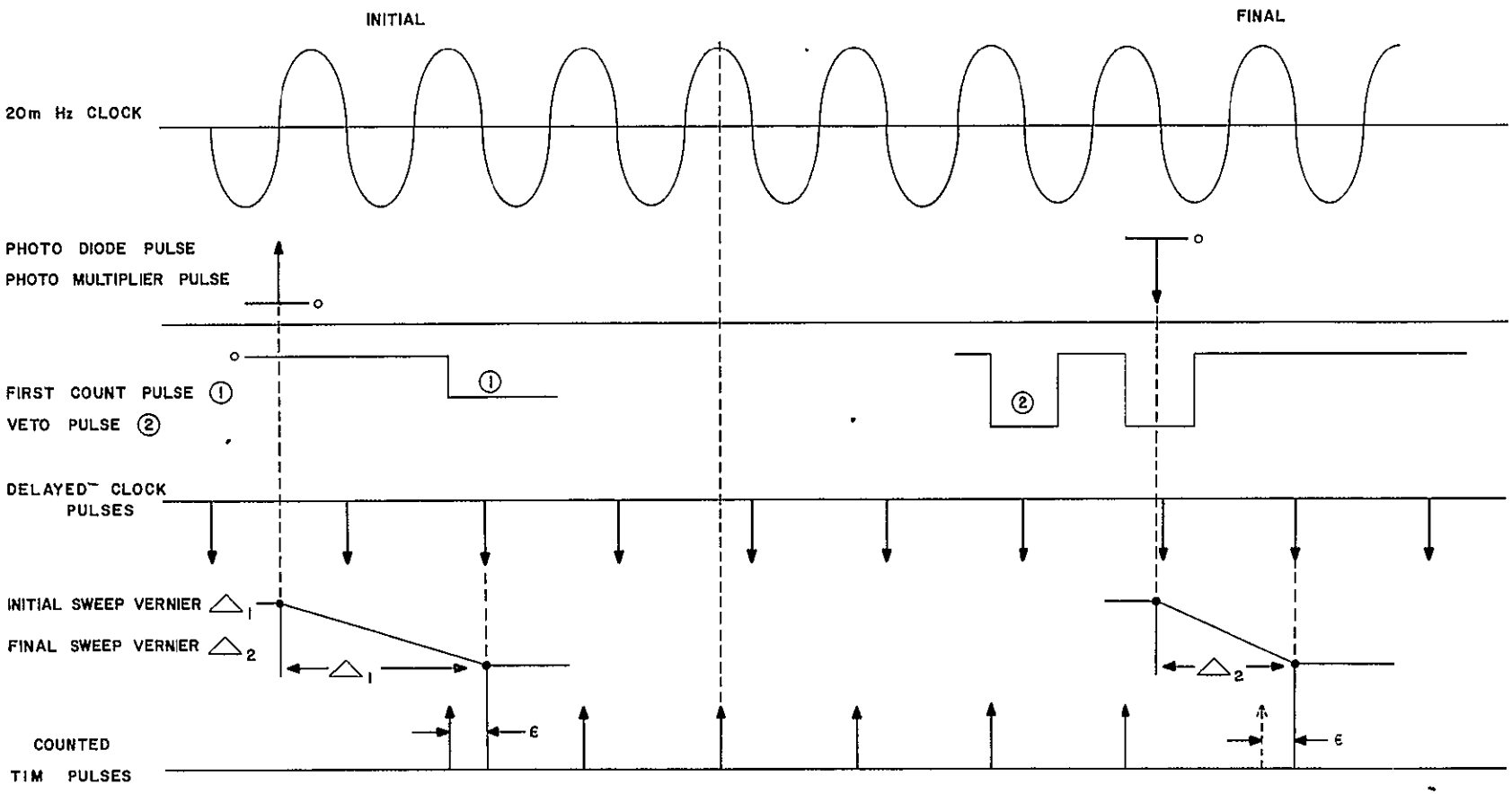
Fortunately, these transient pulses, when the flip flop changes state only to return, occur during an interval of about 10 nanoseconds. If the delayed clock occurs about 25 nanoseconds after the undelayed clock, these false pulses are ignored and only true transitions from "0" to "1" are identified.

Similarly, during the end vernier process, closing the TIM input gate during a clock pulse could cause a substandard pulse which would cause the counting flip flops to increment the count only to fall back causing the MUD and VETO circuitry under the right conditions to respond to this false count. However, because the false count is of less than 10 nanosecond duration, the VETO level disappears before the Delayed Clock

pulse, thus permitting a valid stop pulse to be generated. The adjustment for the delay cable and the discriminator is made so that when the Delayed Clock pulses and VETO pulses are both present, there shall be no output from the coincidence circuit.

If a return pulse arrives in the proper window it starts a TPHC sweep and stops the TIM. The next Delayed Clock pulse that the TIM does not count stops the TPHC. If both of the photomultipliers are triggered, the earliest of the two pulses stops the TIM and the final verniers of the two pulses are read by the two TPHCs. The TPHCs which are labeled #1 and #2, each control a sample and hold circuit in the Astroverter. The computer Astroverter system reads the output to the computer in the same manner as was described for the initial vernier.

The TIM output is read to the computer using device addresses 63 and 64. The number represented is the number of clock pulses counted between opening and closing of the input gate. Figure 2-2 shows how the initial and final verniers and TIM count may be combined to determine the time interval. From this figure it can be determined that the total range in nanoseconds is 50 [N] + (Δ_1 - Δ_2) where Δ_1 is the initial vernier, Δ_2 is the final vernier and N is the number of counts registered on the TIM. In Figure 2-2, ε denotes the time delay between when the TIM counts and the Delayed Clock. For diagram purposes, the TIM is shown changing state at the vertex of the 20 MHz sine wave.



N COUNTS

N-1 50 n second INTERVALS

$D = (\Delta_1 - \epsilon) + (N-1)(50) + (50 + \epsilon - \Delta_2)$ nano seconds

$D = (\Delta_1 - \Delta_2) + 50N$ nano seconds

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TIMING DIAGRAM FOR INITIAL AND FINAL VERNIERS AND TIM 2-2			
ENG	Stroppa		
DWN	L		
CKED	Stroppa	ES 69/70 7790	DATE 11-11-69

SECTION III

1. TESTS TO ASSURE SYSTEM PERFORMANCE

This section describes tests that are performed on the ranging electronics to ascertain if the components work as planned. Some of the tests do not use the computer but simulate pulses from the computer and the laser by the use of two Rutherford Model B16 pulse generators. For these tests it is essential to use an oscilloscope and camera similar to the Tektronix Model 454*. Those tests that involve the computer include the tests of the Astroverter, the TIM, TDG, Time of Day Clock and various tape units and teletype. Regerence must be made to J. Rayner's report[3] for a listing of the test programs.

The tests not involving the computer can be divided into three parts, those tests involving the Initial Vernier System, the final vernier system and finally a check of both verniers with TIM circuitry.

A calibration system which produces 3 nanosecond identical pulses--the time separation of which is known to 100 picoseconds--is described in the last part of this section. A method for producing an extremely short light pulse using an avalanche transistor is in the process of development. This light pulsing circuit and an integral system calibration are only in a planning stage at the time of writing. Further modification is probable.

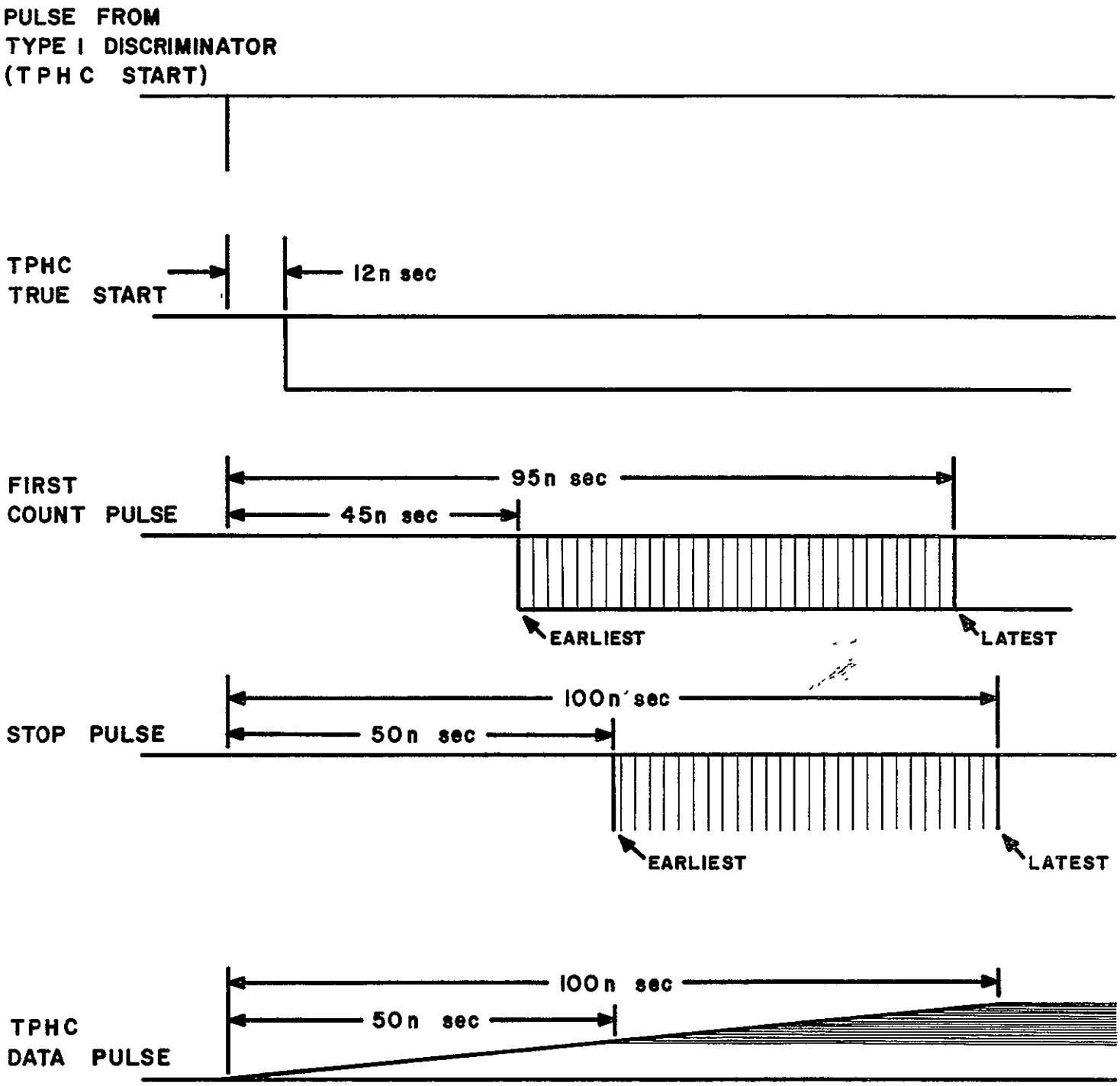
* Tektronix Corporation
P.O. box 500 Beverton, Oregon 97005

A computer assisted calibration is described in the last part of this section.

A. Measurements of the Initial Vernier System

Tests of the initial vernier system are made to determine if the TPHC sweep is started by a photo diode pulse and stopped by the Delayed Clock pulse associated with the First Count pulse. Errors that might occur are that the sweep is stopped by a pulse other than the correct Delayed Clock pulse or the stop pulse applied to the TPHC is not in synchronism with the Delayed Clock. Figure 3-1 below shows the timing sequence of the initial vernier. A description of a test circuit is given below.

A Rutherford Model B16 pulser is used to generate a positive sync. pulse simulating the photo diode pulse, and a positive 10 microsecond 3 volt pulse to drive the reset line on the TIM. The pulse delay is set for 10 milliseconds and the pulse repetition rate is 20 pulses per second. The oscilloscope is triggered using one of the negative outputs from the Type 1 discriminator. Normally, channel #1 of the oscilloscope is used to trigger and display the pulse. The #2 channel can then be used to view the true start pulse from the initial TPHC, normally delayed 10 nanoseconds; the delay to the first count pulse, normally 25 to 75 nanoseconds; the delay to the first stop pulse, normally 50-100 nanoseconds, and finally the flag and data pulses from the TPHC. The sync pulse from the B16 is not in synchronism with the 20 MHz clock. If the scope is triggered on the sync pulse, any pulses that are in synchronism with the clock appear to jitter



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INITIAL

VERNIER

TIMING

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by 50 nanoseconds.

When performing the measurements, it is essential that identical length, 50 ohm terminated cables are used on channels #1 and #2 on the oscilloscope. The exception to this rule is when measuring the TPHC Analog and Flag pulses in which case the 50 ohm termination is removed and the scope triggering is on "normal".

The measurements are made at the output terminals of each unit, (ie. the First Count pulses are measured at the output terminal of the TIM, etc.) The TPHC stop pulses are monitored at either one of the three AND outputs or on the NAND output, in which case the pulse is inverted, of the coincidence network. The Delayed Clock pulses are monitored at the output of the Type 3 discriminator. There is normally a 5 nanosecond delay in the coincidence circuit and 1 nanosecond delay in the cable between discriminator and coincidence network. The camera with a time exposure of 30 seconds is used when viewing the stop pulses or the data pulse from the TPHC. An examination of the photograph of the TPHC data pulses should reveal all possible pulse heights corresponding to delays of 50-100 nanoseconds with no one delay predominating.

B. Measurement of the Final Vernier System

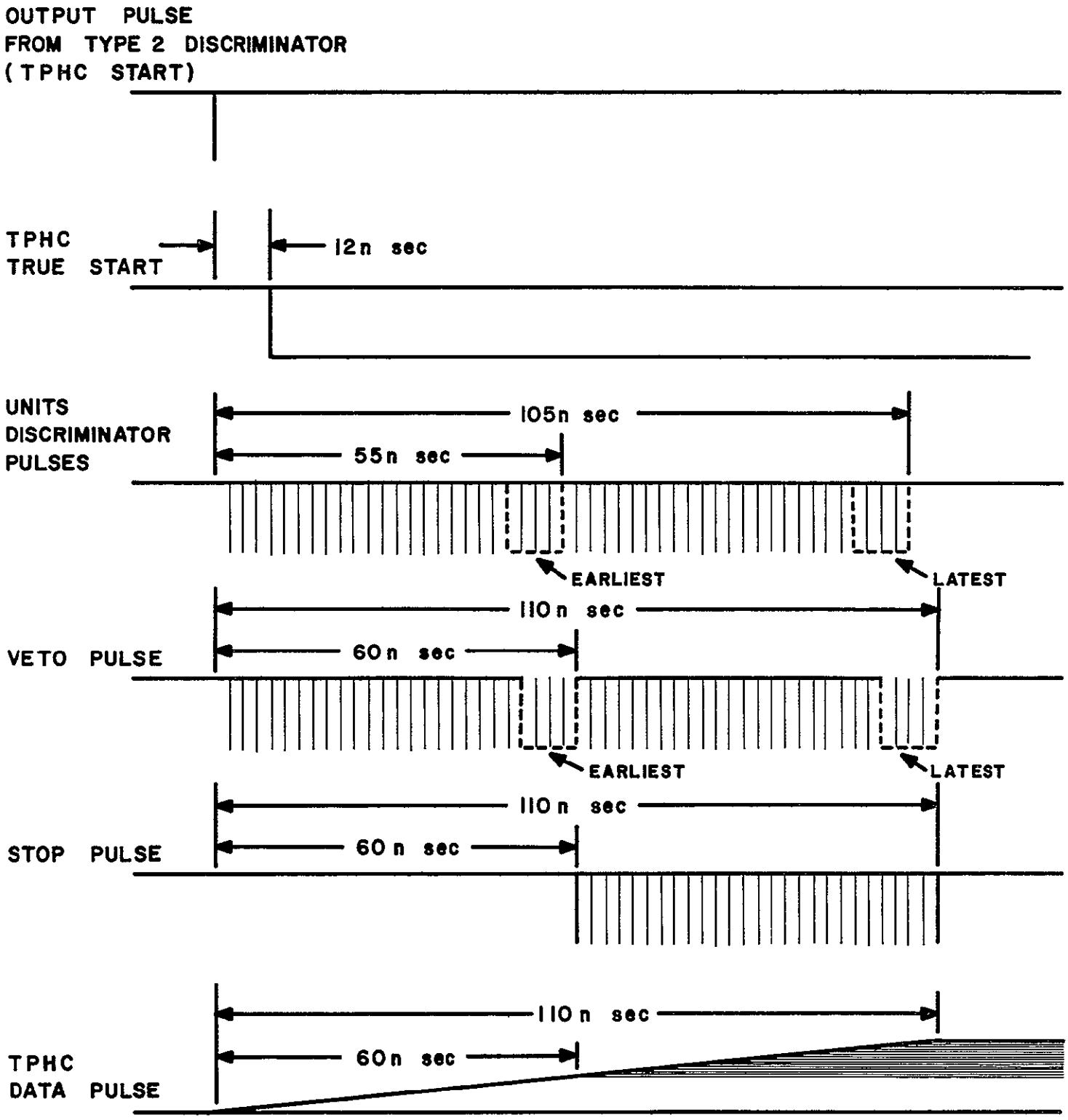
Tests of the final vernier system are made to determine if the final TPHC sweeps are started by a Photomultiplier pulse and stopped by the Delayed Clock pulse associated with the first non-counted clock pulse. A detailed timing diagram is shown

below is Figure 3-2.

Errors that could occur are that the Delayed Clock pulse is incorrectly positioned so that the VETO pulse does not inhibit, or that the TPHCs are stopped by other than the correct Delayed Clock pulse or the stop pulse is not in synchronism with the Delayed Clock. A description of a test circuit is given below.

The TDG is set for local operation, controlled by a knob on rear panel, so that the thumb wheel switches activate the delay. The TDG delay is set for perhaps 500 nanoseconds and the trigger for internal trigger of about 20 pps. The output 6μ sec. window pulse is used to trigger a B16 pulser by removing the 50 ohm termination from the window pulse line and attaching a cable leading to the B16 and re-terminating the cable at the B16. A negative sync pulse from the B16 is used to trigger the Type 2 discriminator and a positive 10 microsecond 3 volt pulse of 10 millisecond delay from the B16 is used to reset the TIM. Oscilloscope channel #1 is used to trigger the sweep, while viewing one of the negative outputs of the Type 2 discriminator.

The output from the Type 2 discriminator is referred to as time zero and delays are measured from this point. The true start pulse is delayed 10 to 12 nanoseconds, the MUD pulses, which have a midvalue width of 10 to 15 nanoseconds,stop as soon as 55 nanoseconds and as late as 105 n.sec. The veto circuit and interconnecting cables delay the VETO pulse about 5 n.sec. so that the earliest that a stop pulse may appear from the output of the



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FINAL

VERNIER

TIMING

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coincidence circuit is 60 nanoseconds and the latest 110 nanoseconds. The TPHC output has an output pulse corresponding to 60 to 110 nanoseconds.

C. Adjustment of Delayed Clock Pulse

The Delayed Clock pulse train delay is adjusted by the length of cable between the 20 MHz input to the TIM and the input to the Type 3 discriminator, and the discriminator setting. The delay is adjusted such that with just the VETO pulses and Delayed Clock pulses present there is no output from the Multiple Coincidence circuit. This adjustment is made by removing the reset cable from the TIM so that units discriminator pulses are constantly produced and removing the #4 AND condition by putting the #4 AND switch in the "out" position. The oscilloscope is used to monitor either the AND or NAND output of the Multiple Coincidence. The Type 3 discriminator setting should be set for a value such that no pulses are observed at the coincidence output.

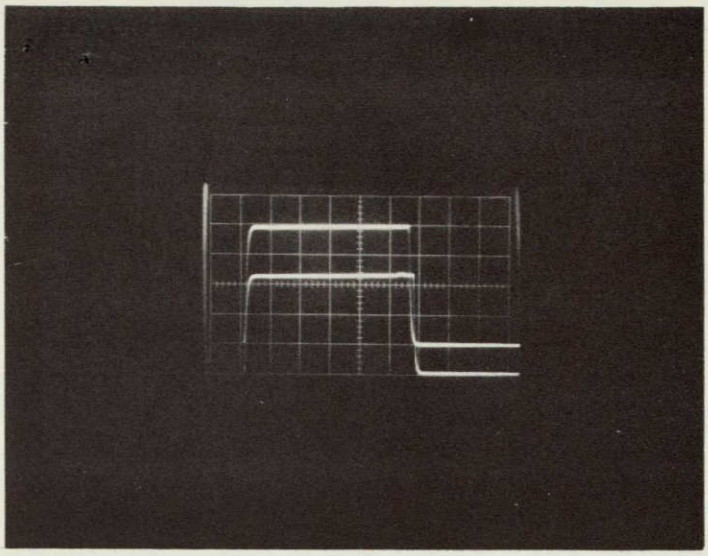
It is desirable to minimize the delay so that the output pedestal on the TPHCs data pulse is minimal. However, too small a delay will result in a non-valid stop pulse for the final vernier.

D. System Measurement

If the initial and final verniers appear to function as planned, the two systems working with the TIM should be tested. While it is more accurate and efficient to use the computer, this test is included because it checks the precision timing system without the computer. If a malfunction occurs in the Computer Astroverter system, this test may help pinpoint the problem.

In operation, the test simulates one photo diode pulse using a B16 pulser in the manual trigger mode, and a second B16 pulser simulating the photomultiplier pulse is triggered using the window pulse from the TDG. The TDG is set manually to about 2.5 seconds and the oscilloscope is set to view the data pulses from the initial and final vernier TPHCs. Using the scope in alternate sweep mode, with normal positive triggers, it is possible to photograph the initial and final vernier data pulses on one picture frame. The procedure is to open the camera shutter, manually trigger the photo diode simulating pulser, wait for the TIM to stop counting and close the shutter. This method permits making a photo of the values of the initial and final verniers and reading the TIM. To repeat the test, reset the TIM manually and start.

If the driven B16 pulser is set for minimum pulse width and delay, the time interval between the start pulse measured at the initial TPHC input and the stop pulse measured at the final TPHC input is 129 nanoseconds, plus the number of nanoseconds dialed into the TDG. This delay measurement is made by setting the TDG to zero and measuring the delay between the outputs of the Type 1 and Type 2 discriminators then adding the cable delays that connect the discriminator to the TPHCs. The initial data pulse baseline is positioned one reticle mark from the bottom of the picture and the final data pulse is started on the bottom. The TPHCs are set for 200 nanoseconds, 10 volts full scale and the oscilloscope sensitivity is 1 volt/cm on the ordinate and 1μ sec/cm for the abscissa. For the tests shown below, the TDG thumb wheel switches are set for a delay of 2489953633 nanoseconds. With the system delay of 129 nanoseconds, the total delay is 2489953762 nanoseconds, a typical lunar range.



Δ_1 = 78 n sec

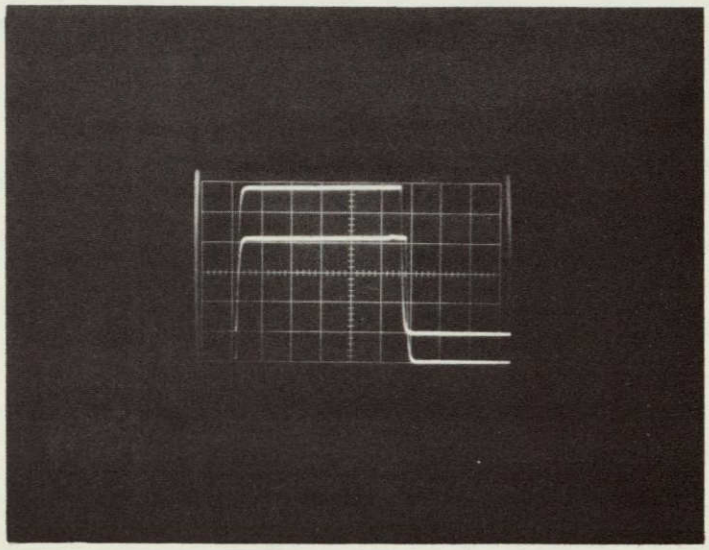
Δ_2 = 66 n sec

$\Delta_1 - \Delta_2$ = 12 n sec

N = 49799075

D = (49799075)50 + 12 =

2489953762 n sec



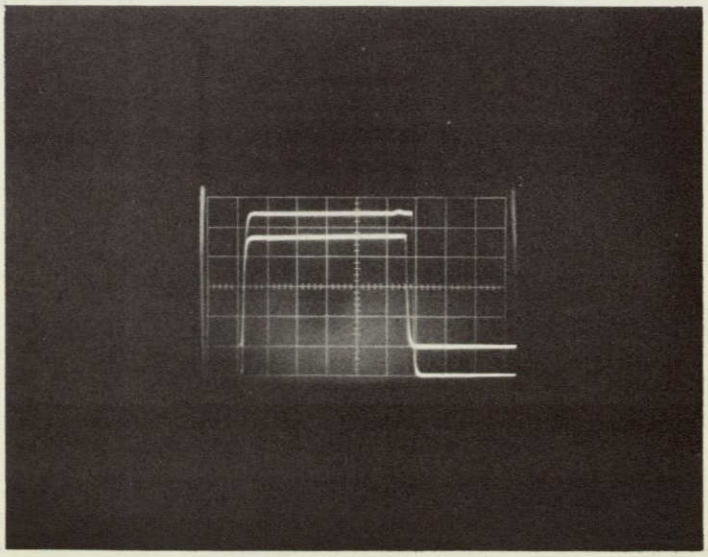
Δ_1 = 96 n sec

Δ_2 = 84 n sec

$\Delta_1 - \Delta_2$ = 12 n sec

N = 49799075

D = 2489953762 n sec



Δ_1 = 72 n sec

Δ_2 = 108 n sec

$\Delta_1 - \Delta_2$ = -36 n sec

N = 49799076

D = 2489953764 n sec

The equation for calculating the delay in nanoseconds is $D = 50\ N + (\Delta_1 - \Delta_2)$ where N is the count on the TIM and Δ_1 and Δ_2 are the initial and final vernier delays.

The results of this test show that the TPHC sweeps and the TIM readings can be correlated to give a reading of the time delay to an accuracy of several nanoseconds. The accuracy is no better than several nanoseconds because of the following:

1. The TDG may have an error of two nanoseconds and a jitter of one nanosecond when the total delay is 2 seconds.

2. There may be non-linearity in the TPHC and it is impossible to read the photograph more accurately.

The main contribution of this test is to prove that the system does lose or gain one 50 nanosecond interval.

TPHC Calibration. The linearity and a rough measure of the accuracy of the TPHC can be obtained using the TDG in the local mode using the internal trigger at perhaps 20 pps. Identical length cables connect the negative 50 n.sec. pulses from the TDG to the start and stop inputs of the TPHC. The output data pulse from the TPHC is observed with the oscilloscope and camera while the delay on the TDG is advanced from 50 to 110 nanoseconds in 10 nanosecond increments. Using a photograph of the test it is possible to calibrate the photograph of the TPHC data pulses and determine the range of the time measurement.

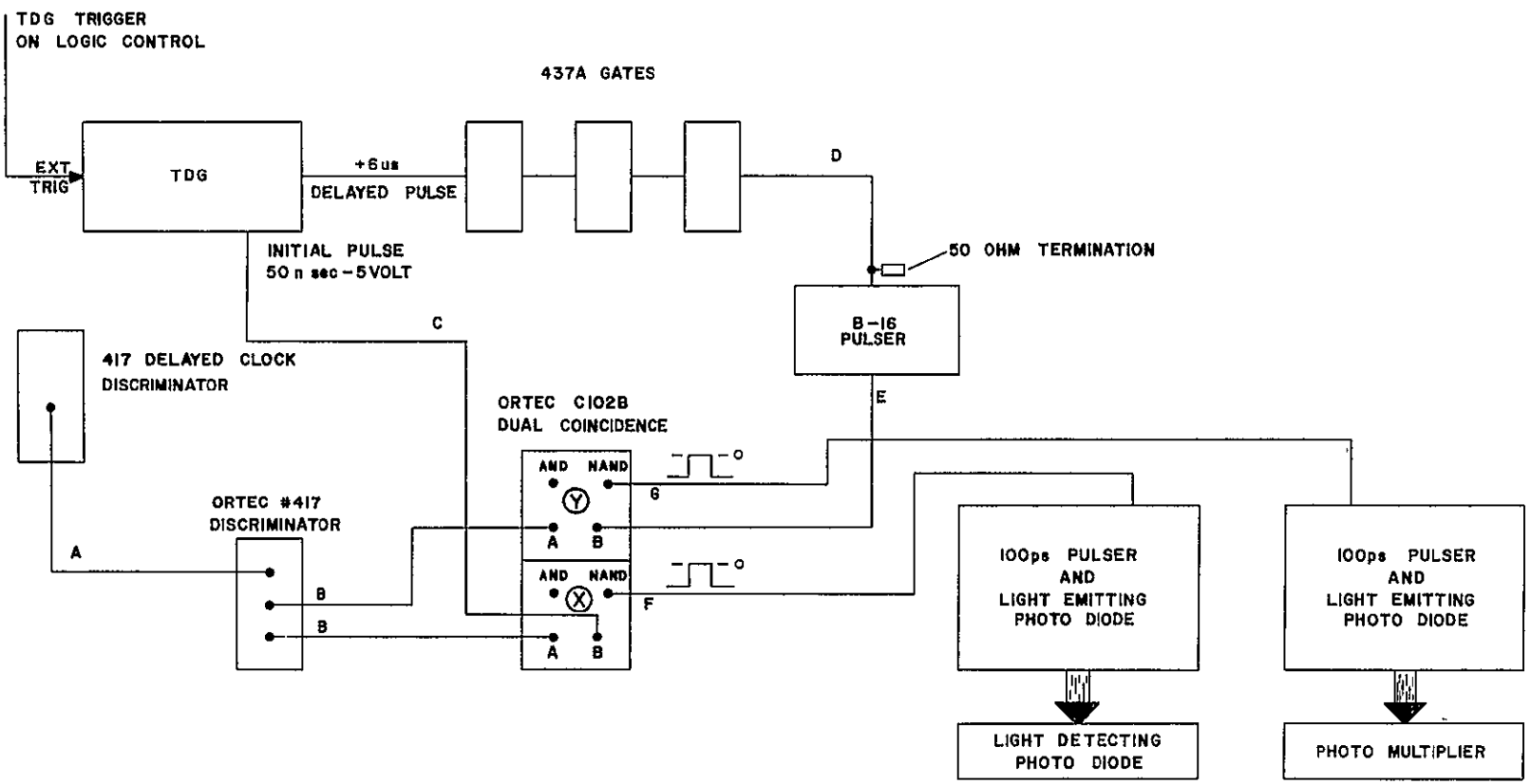
2. COMPUTER CONTROLLED PRECISION CALIBRATION SYSTEM

This section describes a test system, primarily for use with the computer, capable of producing two NIM standard pulses (negative .7 volt 3 n.sec.) whose time separation is known to 100 picoseconds. The basic accuracy of the calibrating system is determined solely by the 20 MHz clock and precision delay cables. The calibration system uses one additional Ortec type 417 Discriminator, an Ortec type C102B dual two-fold AND/NAND gate, a model B16 pulser and the TDG. Avalanche transistor amplifiers and photo diodes currently in development are required to test the photomultipliers and detecting photo diode in an integral manner.

The calibration procedure is divided into three parts; the first describes the entire system, the second describes a method for making precision delay cables, and the third describes a systematic calibration procedure.

A. Calibration Equipment

A block diagram of the calibration equipment is shown in Figure 3-3. Note that the trigger for the TDG is taken from the TDG output test jack on the Logic Control circuit. Output #2 of the Delayed Clock discriminator is used to drive cable A, of the known delay, which drives an Ortec type 417 discriminator. The fast outputs of the model 417 drive cables whose length is adjusted to provide coincident pulses to the "A" inputs of an



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PRECISION TIMING CALIBRATION 3-3			
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Ortec model C102B dual AND gate. The TDG initial pulse is adjusted to give a 50 nanosecond negative pulse which is used to drive one of the C102B "B" inputs. The delayed pulse from the TDG which is the normal 6μ sec positive window pulse, is used to trigger a B16 pulser on the end of the window pulse chain. The B16 pulser is programmed to give a 50 nanosecond, one volt, negative pulse with minimum delay (75 nanoseconds) to drive the "B" input of the remaining AND gate.

Using an oscilloscope, adjust the length of a cable A so that the initial TDG pulse and the Delayed Clock pulse are coincident when measured at the entrance terminals of the initial model C102B AND gate. An adjustment of the TDG delay, in the manual dial setting mode, assures coincidence between the Delayed Clock and the pulse from the B16 pulse generator. The output pulses from the two model C102B AND gates are separated by a precise multiple of 50 nanoseconds since they are simply selected Delayed Clock pulses.

The C102B module has both AND and NAND outputs and while each pulse is about 3 nanoseconds long, since they are identical pulses, identical parts of each pulse can be used to calibrate systems to 100 picoseconds using precision delay cables.

The exact number of 50 nanosecond intervals between the pulses from X and Y can be calculated by figuring the delay from the TDG, cables D and E and the B16 pulser, minus the delay in cable C. This number represents the time of opening of the Y pulse gate and should be adjusted so that ambiguity does not exist.

As the TDG is varied the Y pulse moves in units of 50 nanoseconds. Cables F and G may be arranged to give a pulse of any intermediate delay to the initial and final TPHCs or to the avalanche transistor amplifiers which convert the NIM pulse to a light pulse for use in driving the photomultiplier and light detecting photo diode.

B. Cable Calibration

The calibration requires cables, including BNC connectors, with accurately known delay characteristics. The cable used is RG 58 c/u, the connector plugs are King connector number KC 59-78 and the jacks are King connector KC 39-26 or equivalent.

The advertised propagation speed for RG 58 c/u is 0.65 c. The procedure for determining the exact number is to make three cables using KC 59-78 plugs on both ends, two of which are identical; the third having a 50 nanosecond longer delay. Connect the identical cables to the negative outputs of the Delayed Clock discriminator (Type 3) and terminate each cable with a BNC "tee" (UG 274 a/c) and a 50 ohm load at the input of the 454 oscilloscope. Using the 50 nanosecond/cm sweep with 10x multiplier, trigger the scope on channel 1 and use the alternate sweep mode. The two traces should coincide in all configurations, that is, it should be independent of which cable is connected to #1 or #2 discriminator outputs or oscilloscope inputs.

Disconnect one of the cables and replace it with the 50 nanosecond longer cable. If cut correctly, the pulses again coincide. The delay of the first cable can be expressed by the equation

$$2X + KL_1 = D_1$$

where $2X$ = delay in the two BNC connectors (nanoseconds)

K = propagation constant (nanoseconds/centimeter)

L_1 = cable length (centimeters)

D = delay (nanoseconds)

The equation for the longer cable is

$$2X + KL_2 = D_1 + 50$$

solving the two equations, we find

$$K = \frac{50}{(L_2 - L_1)}$$

Using the new constant for the cable propagation delay and assuming about .1 nanoseconds for plug delay, construct a 50 nanosecond cable using a plug on one end and a jack on the other. Connect this new cable in series with one of the delay cables in place and trim the cable length so that the pulses coincide. By measuring the length of the cable so adjusted, it is possible to determine the delay characteristics of a jack and plug from the equation

$$2X = 50 - KL_3$$

where L_3 = measured length of adjusted cable

K = previously calculated constant

2X = delay of a jack and plug. (Jack and plug delays are assumed equal.)

From these equations, it is possible to make a series of delay cables of any desired delay to an accuracy of 100 pico-seconds, which for this cable corresponds to a length of about 2 centimeters.

3. PRECISION CALIBRATION PROCEDURE

A. Verniers

Connect the time interval measurement equipment for normal operations but use Computer Test Program #2, which reads the TPHCs via the Astroverter system and types the voltage read from the A-D converter. Connect the precision timing calibration circuit to the main system as is shown in Figure 3-3 with the exception that the delayed pulse from the TDG is connected directly to the Ortec model C102B Coincidence circuit "B" input instead of the model B16 pulser. The TDG is programmed to give a negative 50 nanosecond pulse with a delay of 50 nanoseconds.

Using two identical cables, connect the AND output of the X gate to the start terminal of the TPHC under test and the AND output of the Y gate to the stop terminal. The coincidence-anticoincidence switch on the TPHC must be in the anticoincidence position.

When the computer starts the TDG, two pulses separated by exacly 50 nanoseconds are sent to the TPHC. The TPHC converts the delay to an analog voltage which is then converted into a coded octal number by the Astroverter and read into the computer, which in turn types the number. Add a 20 nanosecond delay cable, constructed following the procedure outlined in the cable calibration chapter, to the stop line to derive a precise 70 nanosecond delay. Remove the delay cable from the stop line and connect it to the start line for a 30 nanosecond delay. In each case the computer reads and types the voltage of the data pulse from the TPHC.

Using this procedure, an infinite number of points can be observed on the TPHC delay-voltage curve. A suitable compromise would be to use 10, 20 and 50 nanosecond delay cables to measure the curve at the 30, 40, 50, 60, 70, 80, 90, 100 and 110 nanosecond delay points. When graphed, these points should lie. on a staight line. The ultimate equation is limited only be the ingenuity and patience of the programmer. Al three TPHCs are calibrated in this fashion.

B. System

Connect the Precision Timing Calibration equipment to the system as is shown in Figure 3-3 with the exception that the start inputs for the initial and final vernier TPHCs are driven via equal length cables from the C102B AND outputs X and Y instead of the Type 1 and 2 Discriminators. Using Computer Test Program #3 with an accurate time-voltage equation for each TPHC, monitor the delay between the pulses from X and Y.

The time delay between the two pulses X and Y is a multiple of 50 nanoseconds accurate to 100 picoseconds. If calibration procedures outlined previously have been done correctly, the computer should print out an exact multiple of 50 nanoseconds.

An addition of delay cable to the X or Y output should produce a calculatable change in the delay. The length of cable A has no effect on the delay time interval, and therefore should have no effect on the computer output. Lengthening cable A has the effect of changing the length of the initial and final verniers. Any change in the initial vernier should be balanced

by a like change in the final vernier or one count change in the TIM and new readings for both verniers. In all cases the time interval calculated by the computer must not change.

If all measurements using the standard NIM pulses are satisfactorily met, then connect the 100 picosecond pulser and Light Emitting Photo Diode Circuits to the NAND X and Y outputs of the C102B using cables of identical length. The system may now be calibrated using two light pulses of known time separation so that the photomultiplier cables and input discriminators may be calibrated.

CONCLUSIONS AND SUGGESTIONS FOR FUTURE SYSTEMS

A time interval measurement system has been developed, using commercial equipment, to measure the time separation of two pulses about 2.5 seconds apart to an accuracy of 100 picoseconds. A calibration procedure using only a precision 20 MHz oscillator and a ruler as standards has been developed to test the system.

When used with laser equipment and photomultipliers in the Lunar Ranging System, an overall system accuracy of about 1 nanosecond should be achieved.

In normal operation, the Time to Pulse Height converters operate in a mode where 10 volts correspond to 200 nanoseconds. The Astroverter is connected such that 20 volts corresponds to 4096 channels. It would be desirable to change the Astroverter so that the unit responded to only +10 volts for 4096 channels insead of the + or - 10 volts as in the present model. This change could be achieved by changing resistors in the sample and hold amplifiers and adding a precise bias voltage. The system resolution would then be increased to 50 picoseconds. Further, if the sweep times in the Time to Pulse Height converters are changed so that 120 nanoseconds corresponds to 10 volts then the system resolution would increase to 30 picoseconds.

Work is presently continuing on the 100 picosecond pulser and light emitting diode system.

Future systems should use only one photo detecting

device such as a channeltron type photomultiplier with one time to pulse height converter going directly to a sample and hold amplifier and Digital Converter. The Time Interval Meter and Time Delay Generator would be completely binary units instead of binary coded decimals, and they would be built on cards fitting into the memory expansion chassis of the 620/i. All ephemeris calculations should be done in the computer to 100 nanosecond precision. The basic clock frequency should be 10 MHz.

A new system would require only one read-write tape deck and could be built in one 19 inch rack.

The ultimate precision, excluding error of the clock, could be 50 picoseconds.

APPENDIX A

CABLE LENGTH, MODULE AND SWITCH POSITIONS, AND TERMINATIONS

A) The NIM Module Arrangement (from left to right)

Photomultiplier Discriminator #1	Ortec 403A
Photomultiplier Discriminator #2	Ortec 403A
Photo Diode Discriminator	Ortec 417*
Delayed Clock Discriminator	Ortec 417
Initial Vernier TPHC	Ortec 437*
Final Vernier TPHC	Ortec 437*
Multiple Coincidence Gate	Ortec C104AN*
Final Vernier TPHC	Ortec 437*

Other Components

Time Interval Meter	Eldorado 783G*
Time Delay Generator	Eldorado 650*
Astroverter	Astrodata 3900*
Tape Deck #11	Digi-Data Corp. #1300 write only
Tape Deck #10	Digi-Data Corp. #1300 read-write
Computer	Varian Data Machines Model 620/i with 8k core memory
Computer Interface	Computer Operations Special Item

The TIM is located directly below the NIM bin and TDG is directly below the TIM. The Astroverter is below the TDG. In the second rack are found the tape decks, computer and computer interface.

* Modified

B) Cable Lengths (all RG 58c/u with BNC connectors)

Item	Signal Path	Length (Inches)
1	True Start of TPHC #2 to Stop of TIM	10.5
2	True Start of TPHC #1 to Stop of TIM (Cables are joined at a "Tee" on TIM)	10.5
3	True Start of TPHC #0 to "Start" of TIM (BNC Elbows at both ends)	10.5
4	Output #1 of 20 MHz Disc to AND Input #3 of Multiple Coincidence	7.0
5	TIM "First Count" to AND #4 of Multiple Coincidence	14.0
6	Multiple Coincidence AND Output to "Stop" of TPHC	8.5
7	Multiple Coincidence AND Output to "Stop" of TPHC	8.5
8	Multiple Coincidence AND Output to "Stop" of TPHC	8.5
9	TIM Units Disc to Multiple Coincidence "VETO	12.5
10	Photo Diode Disc Output #2 to "Start" of TPHC	6
11	Positive Output of P.D. Disc to Ext. Trig of TPHC	24
12	"Tee" on 20 MHz Input to TIM to Input of Delayed Clock Discriminator	48
13	Output of TDG to TPHC #2 Gate Input "Elbow" at TDG, "Tee" at TPHC	24
14	TPHC #2 to TPHC #1 Gates "Tee" at TPHC (loop coiled)	8.5
15	TPHC #1 Gate to Inhibit AND #4 of Multiple Coincidence. "Tee" at Multiple Coincidence with 50 ohm Termination	8
16	Timing Logic G_1 to TIM Reset	48

17	P. M. Disc to Start of TPHC #1	24
18	P. M. Disc to Start of TPHC #2	24
19	1 Ω Output of TPHC #0 to AA Astroverter	Not Critical Data Lines
20	1 Ω Output of TPHC #1 to EE Astroverter	
21	1 Ω Output of TPHC #2 to KK Astroverter	
22	Converter busy TPHC #0 to BB Astroverter	flag 0
23	Converter busy TPHC #1 to FF Astroverter	flag 1
24	Converter busy TPHC #2 to LL Astroverter	flag 2
25	20 MHz Clock to TIM	120--not critical
26	1 MHz Clock to TDG	120--not critical
27	I sec Clock to Timing Logic	120--not critical
28	Mirror Control Timing Logic to Mirror Motor	Long
29	Pockel Cell Timing Logic to Laser	Long
30	Flash Lamp Timing to Laser	Long

Interface cables are provided connecting computer interface to TIM, TDG, Timing Logic, Tape Deck #10, Tape Deck #11

Cable is also supplied from the computer I/O bus to the Astroverter

C) Switch Position (normal running mode)

Unit	Switch Name	Position
TDG	Ext. Trig	Ext. +
	Delayed Pulse	+6μ sec
	Rear panel Local/remote	Remote
Discriminators	Pulse Stretcher	Out
TPHCs	Range	.2μ sec
	Amplitude	10 volts
	Multiplier	X 1
Initial only	Coincidence	Anti-coincidence
Final only	Coincidence	Coincidence
Multiple Coincidence	AND Switches	#1 out
		#2 out
		#3 in
		#4 in

D) Terminations (50 ohm BNC)

1. Multiple Coincidence NAND output
2. Multiple Coincidence VETO output
3. Multiple Coincidence Inhibit VETO
4. Multiple Coincidence Inhibit 4th AND

APPENDIX B

TIME TO PULSE HEIGHT CONVERTERS

Reference should be made to the Operating Instruction Manual for the Model 437A Time to Pulse Height Converter of Ortec Corporation.

The basic changes are shown in diagram B-1 and are discussed below. They are:

1. The output pulse is changed from a 1μ second doublet to a single positive pulse of 5.5μ sec duration. This change provides a pulse of sufficient duration for the sample and hold amplifiers in the Astroverter. The change is accomplished by replacing the doublet producing circuit, Q-16, Q-17, Q-18 and Q-19 by one emitter follower circuit, T-1, whose input is tied to the gate lead of Q-11 and the output is connected to the base of Q-41. C-38 and C-13 are removed. The pulse is lengthened by adding a 10k ohm resistor in series with R-153.

2. The converter busy pulse is modified to produce a flag pulse of 4μ second duration. The flag pulse is started by a start pulse and stopped by the original circuit sample pulse inverted through a pulse transformer. The pulse transformer is connected between the collector of Q-40 and ground. The transformer secondary drives pin 5 of the IC via a 2.7k resistor and pin #2 of the IC is open.

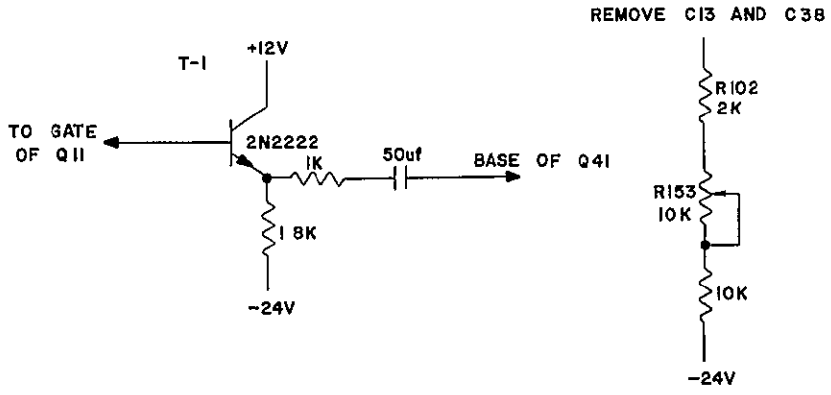
3. The reset system is modified so that the TPHC may accept one input pulse every 2 milliseconds to prevent the TPHC from operating on a noise pulse immediately after receiving a signal pulse. The 2 millisecond reset time assures that only one start pulse is received for each cycle of operation.

This change is affected by changing C-24 from .001μ to 2μf and adding a clamping transistor T-2 to the base of Q-22. The mode of operation of the circuit is as follows:

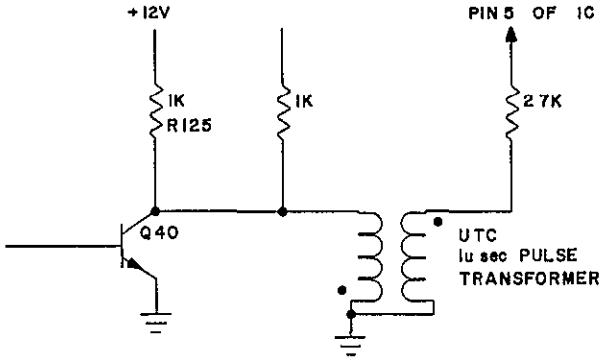
A stop pulse activates one shot Q-23 and Q-24 so that a 2 millisecond positive pulse is produced across R-174. This pulse is used to turn on T-2 and thus clamp the base of Q-22 to ground, which turns off Q-22 and allows tunnel diode D-2 to reset and remain so. The pulse across R-174 disappears at the end of 2 milliseconds allowing normal operation.

4. A True Start Pulse circuit consisting of emitter follower T-3 is added to provide a fast negative pulse with minimum delay after a start pulse.

1

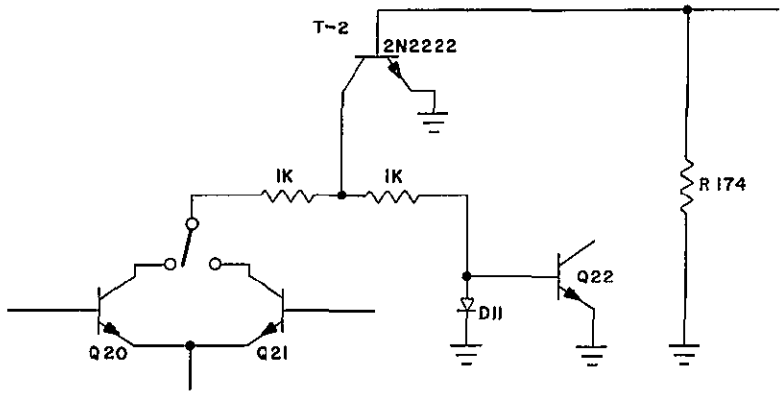


2



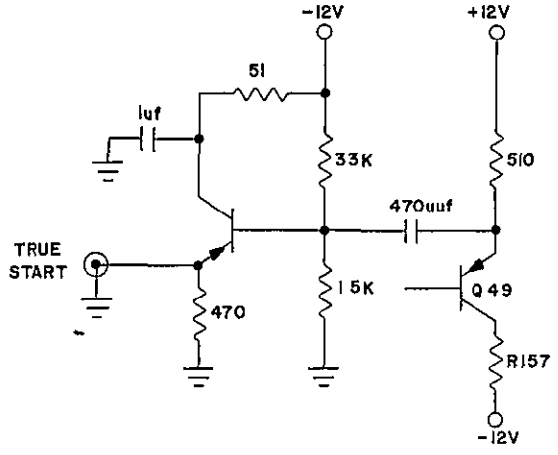
REMOVE WIRE ON PIN2 OF IC

3



CHANGE C24 TO 2uf

4



ENG	
DWN	
CKED	

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DIAGRAM B-1
CHANGES TO TPHC
MODEL 437A
ORTEC

ES 69/70 7790 | DATE 11-7-69

APPENDIX C

LOGIC CONTROL CIRCUITS

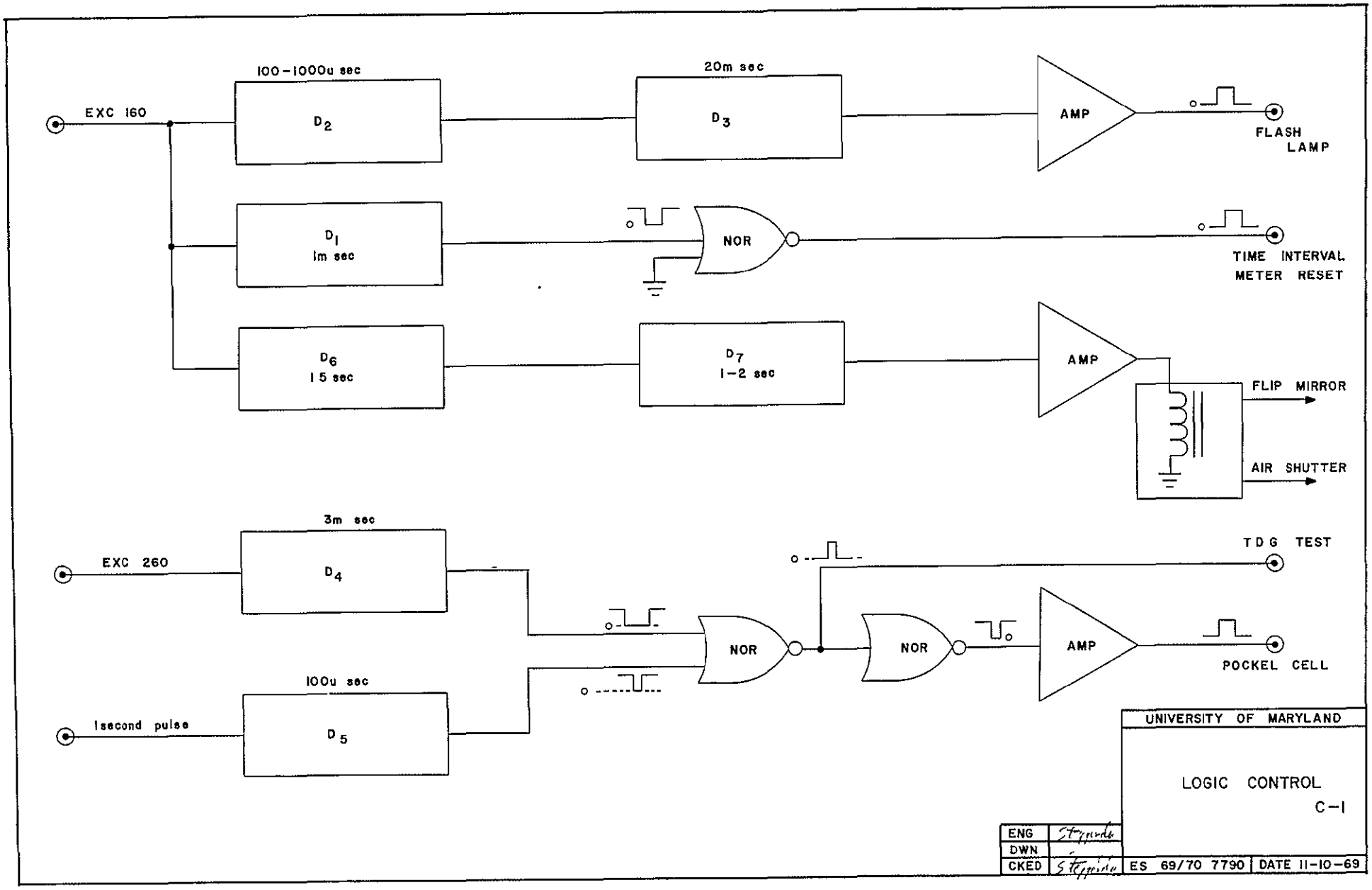
The logic control circuits act as interfaces between the computer, the laser power supply and the detector package system. A block diagram and a schematic diagram appear in Figures C-1 and C-2.

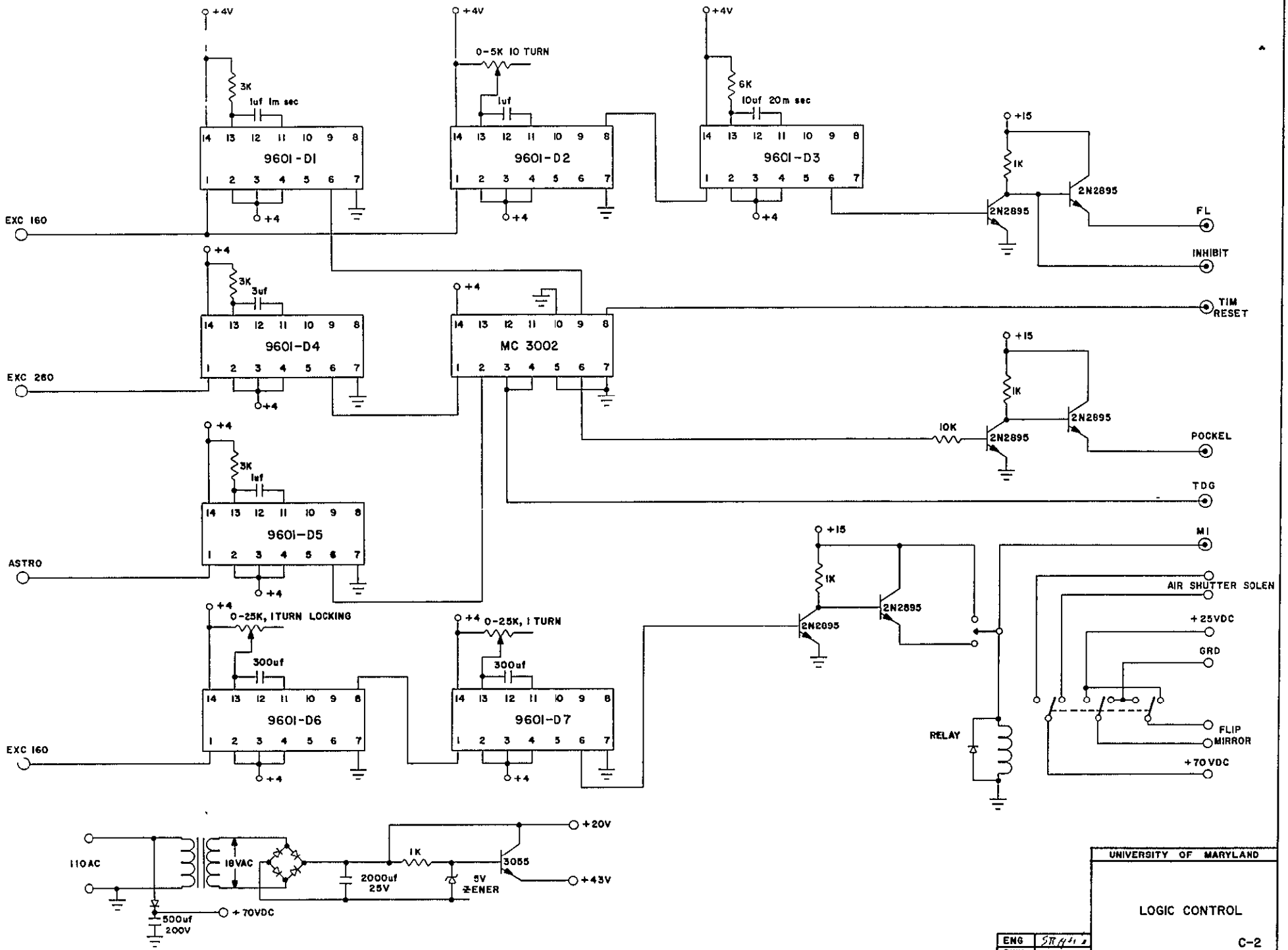
The laser control circuit receives a EXC 160 pulse from the computer 2 milliseconds before a one second clock pulse. The EXC 160 pulse, a 200 nanosecond pulse from the +3 volts to ground, is used to start three monostable multivibators (M.M.V.) D-1, D-2, and D-6. The pulse width from D-2 can be varied from 100 to 1000 microseconds. The trailing edge of D-2 is used to fire D-3, a 20 millisecond pulse shaping M.M.V. The output pulse from D-3 is amplified by a power transistor to give a positive 15 volt, 20 millisecond pulse to the flash lamp circuit. The delay of D-2 causes this output pulse to arrive 1900 to 1000 μ seconds before the one second clock pulse. The pulse width from D-1 is fixed at about 2 milliseconds. The pulse from D-1 is inverted by G_1, a NAND gate, and is used to reset the Time Interval Meter.

When the firing sequence has begun, the computer sends an EXC 260 pulse to fire MMV D-4, which has a pulse width of 3 milliseconds. The D-4 pulse asserts one half of a NAND gate G-2. The other half of G-2 is asserted when the one second pulse from the Astrodata Time of Day clock fires M.M.V. D-5.

The resultant output pulse is amplified and becomes the Pockel Cell firing pulse. A Time Delay Generator pulse pick off point is supplied for testing purposes.

The EXC 160 pulse is used to fire M.M.V. D-6 which has a pulse width of 1.5 seconds. The trailing edge of D-6 fires D-7, another M.M.V. whose pulse width can be adjusted from 1 to 2 seconds. In normal operation, this output pulse is amplified and is used to close a relay for a period of time from 1.5 seconds to 2.6 seconds after the flash lamp firing. The relay controls the flip mirror and a shutter located in the detector package.


EXC 160
100-1000u sec
D2
20m sec
D3
AMP
FLASH LAMP
D1
1m sec
NOR
TIME INTERVAL METER RESET
D6
1 5 sec
D7
1-2 sec
AMP
FLIP MIRROR
AIR SHUTTER
EXC 260
3m sec
D4
TDG TEST
NOR
NOR
AMP
POCKEL CELL
1second pulse
100u sec
D5
UNIVERSITY OF MARYLAND
LOGIC CONTROL
C-1
ENG
DWN
CKED
ES 69/70 7790
DATE 11-10-69



UNIVERSITY OF MARYLAND	
LOGIC CONTROL	
C-2	
ENG	
DWN	
CKED	
ES 69/70 7790	DATE 11-12-69

APPENDIX D

MULTIPLE COINCIDENCE WITH VETO CIRCUIT

Reference should be made to the instruction manual for the C104A/N Fourfold AND/NAND Module with VETO by E G& G. There are a number of versions of the C104; please refer to E G& G diagram #303372 revision A printed in December of 1968, or a later manual.

There are three changes in diagram #303372 as is shown in revised diagram D-1. One change incorporates a circuit which electronically inhibits the 4th AND circuit like the switch on the front panel. A second circuit, which is found to be unnecessary, inhibits the VETO circuitry. The third change removes one of the NAND outputs and replaces it with an AND output.

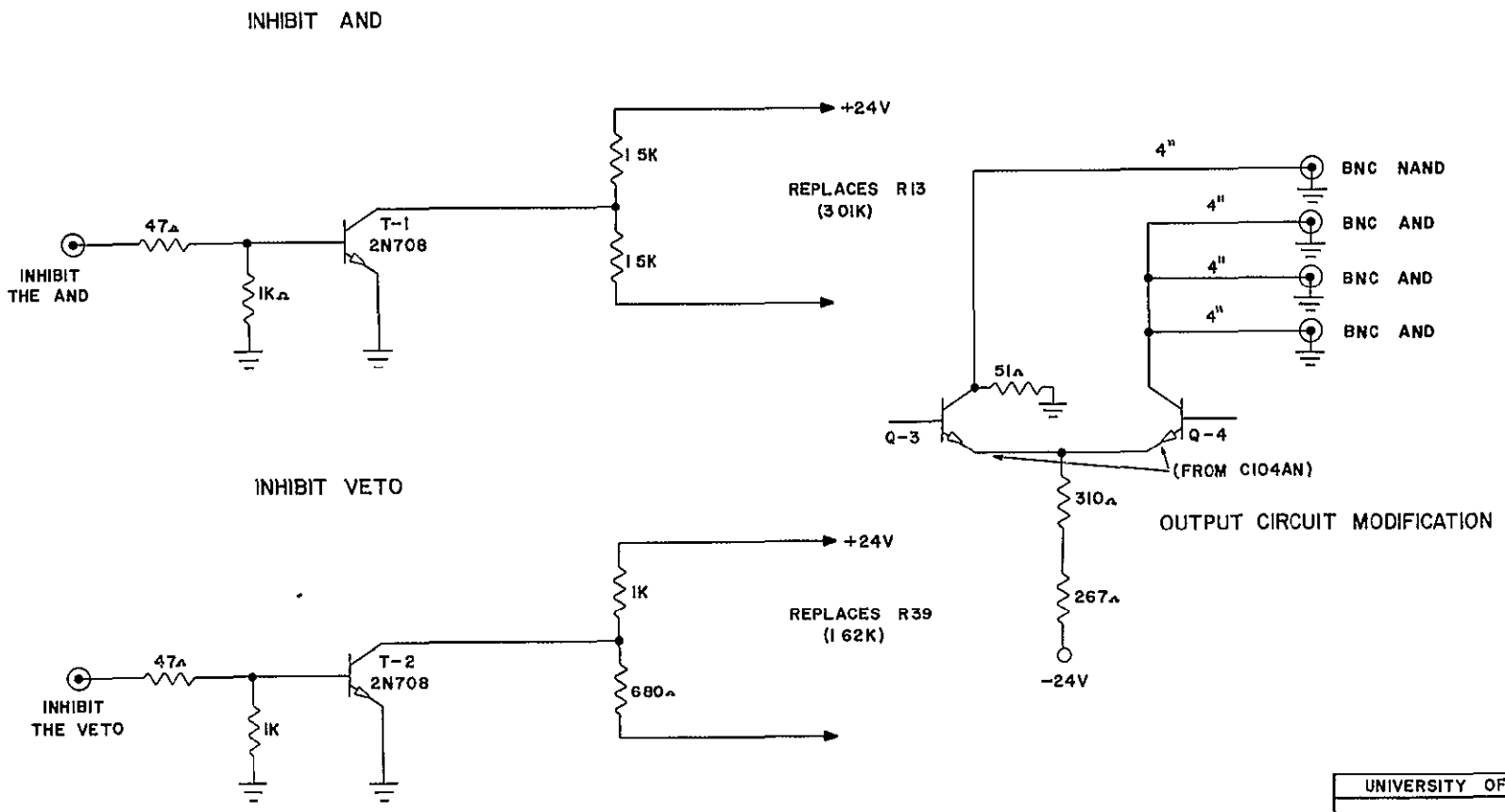
Transistor T-1, a 2N708, saturates "on" whenever a positive pulse of 1 volt or greater appears on the "Inhibit the AND" input jack. The collector of T-1 is connected to a pair of 1.5k ohm resistors which replace R-13. When T-1 is "on", the junction of D-8 and D-4 is essentially grounded causing D-8 to open causing the 4th AND input to be non-operative. When the inhibit pulse disappears, T-1 turns off and the 4th AND circuit reverts to normal operation.

Transistor T-2, another 2N708, performs identical functions in the Inhibit the VETO circuit. 1.0k ohm and .68k ohm resistors replace resistor R-39.

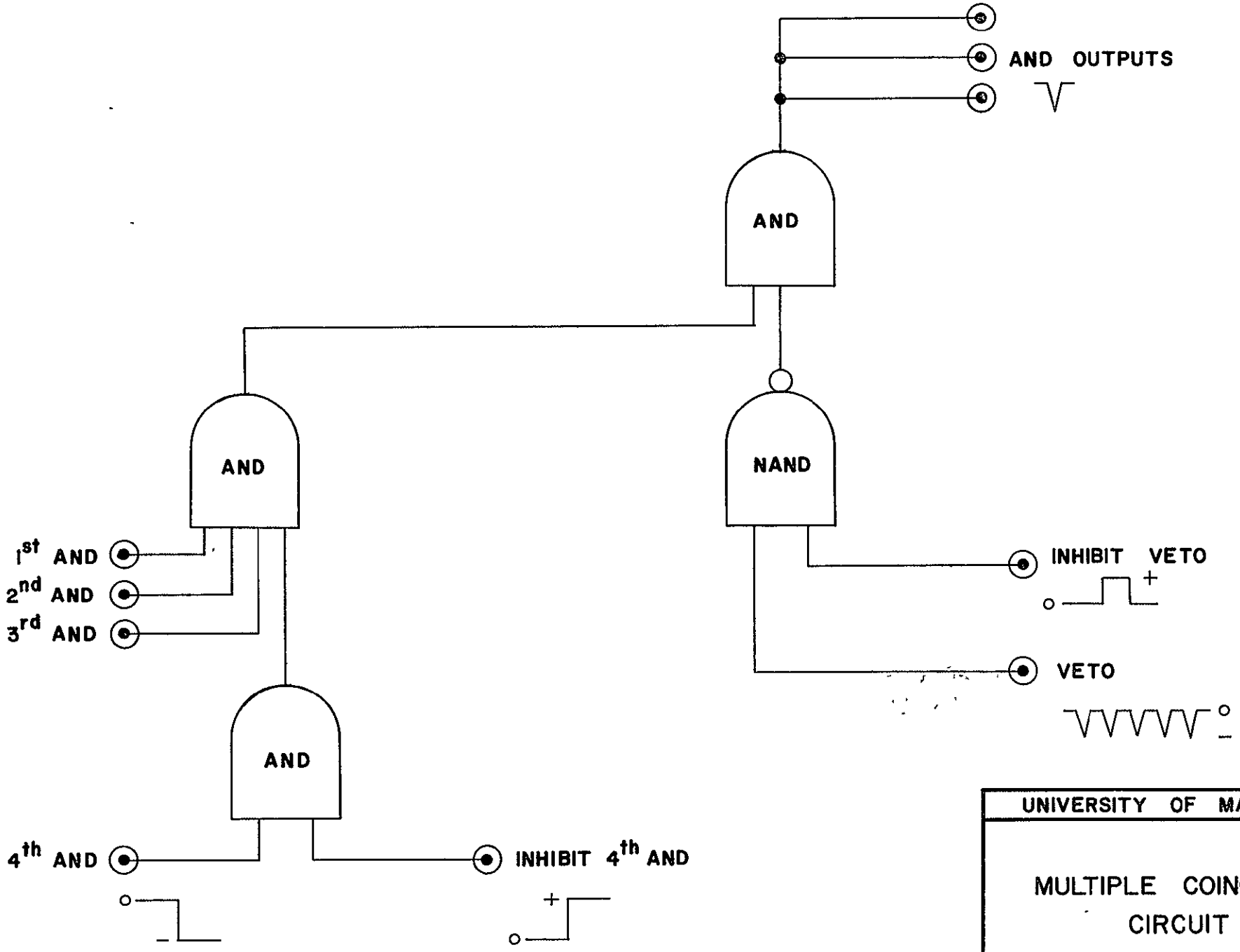
One of the NAND outputs with its cable is removed

from the collector of Q-3 and moved to the collector of Q-4. A 51 ohm resistor is connected from the collector of Q-3 to ground replacing the load removed.

Figure D-2 shows a block diagram of the logic operations of the multiple coincidence circuit. On any input or output the "true" state is the most negative. The circuit is somewhat of a hybrid in that some of the inputs shift from zero to negative voltages and others go from zero to positive voltages.



UNIVERSITY OF MARYLAND			
MODIFICATION TO C104AN 4 FOLD AND/VETO DIAGRAM 303372 REVA			D-1
ENG	S.T. Sgarlata		
DWN			
CKED	S.T. Sgarlata	ES 69/70 7790	DATE 11-4-69



UNIVERSITY OF MARYLAND

MULTIPLE COINCIDENCE CIRCUIT

D-2

ENG	Steggerda		
DWN	Lacy		
CKED	Steggerda	ES: 69/70 7790	DATE 11-3-69

APPENDIX E

TIME INTERVAL METER WITH MARYLAND UNITS DISCRIMINATOR AND FIRST COUNT CIRCUITS

Reference should be made to the Operating Instruction manual for the model 783G 10 Nanosecond Time Interval Counter of Eldorado Electronics.

The basic changes in the counter are:

1) The basic clock rate is changed from 100 MHz to 20 MHz and is supplied solely from an external source. All frequency multipliers and amplifiers are eliminated.

2) The switches and inverting transformers associated with the start and stop channels are eliminated. A BNC connector using 50 ohm cable feeds the start and stop signals directly to the input diode networks on the "G-14A Gate" Card drawing #C-3-1849.

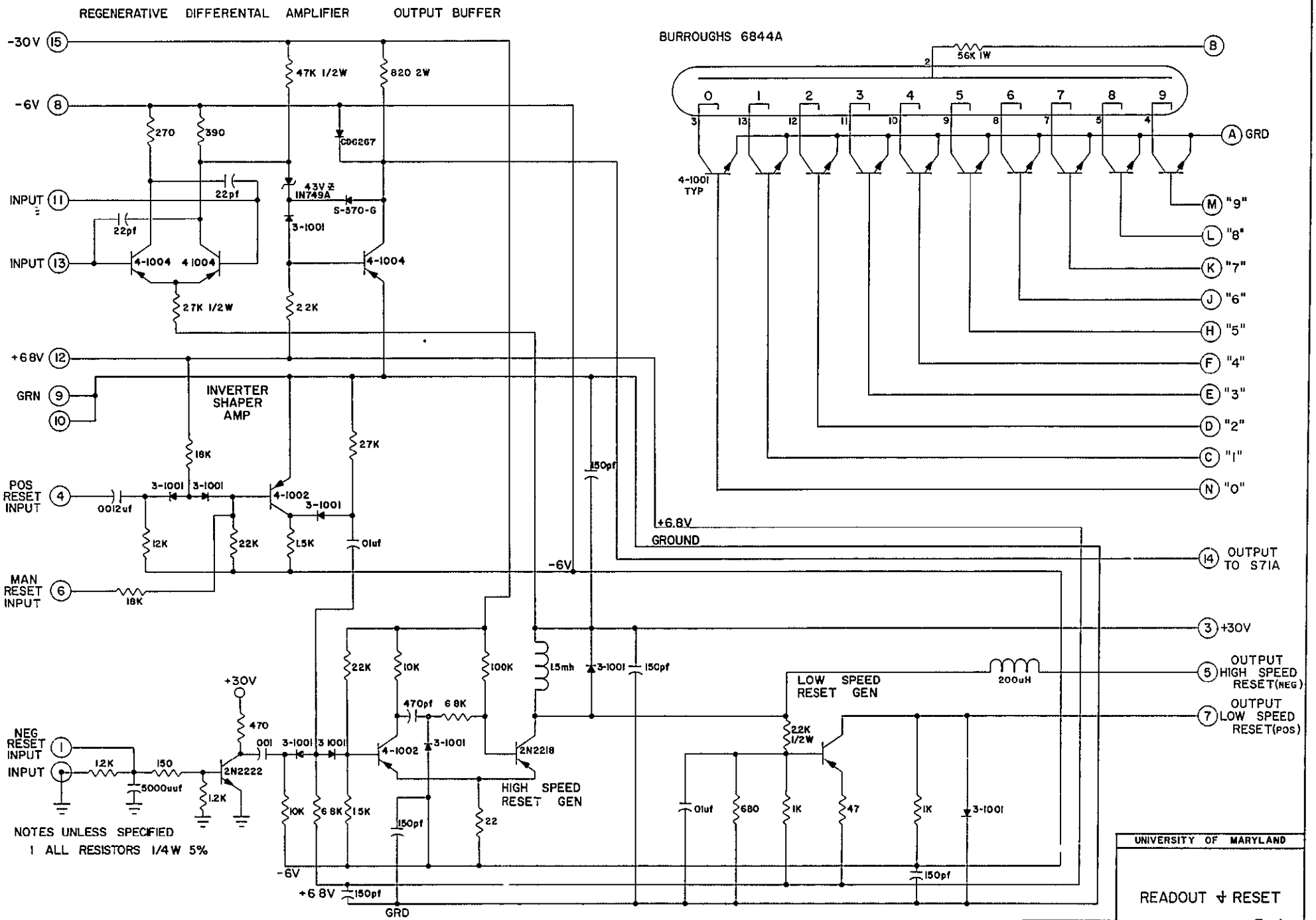
3) An external reset amplifier is added to the Readout and Reset card C-3-1822. This change is shown on schematic E-1. The reason for the change is to supply a system reset when a positive 5 volt 10μ sec or longer pulse is supplied to the input but be immune to large fields and stray pulses generated by firing the laser.

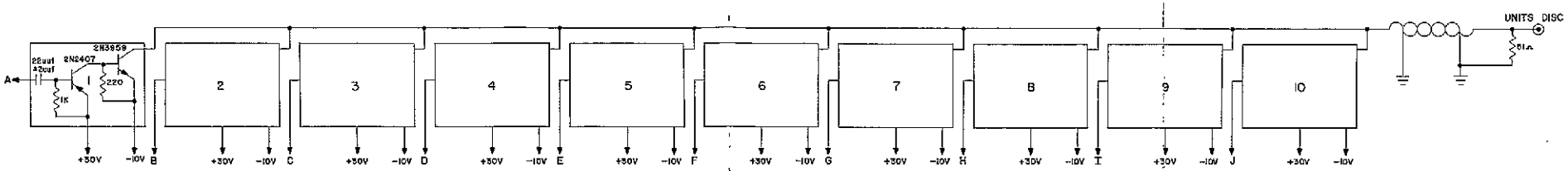
4) A Units Discriminator and a First Count Circuit are added to the "100 MC DCU board (schematic Diagram D-3-1856). The revised diagram is shown in Figure E-2. The mode of operation of the new circuits are as follows:

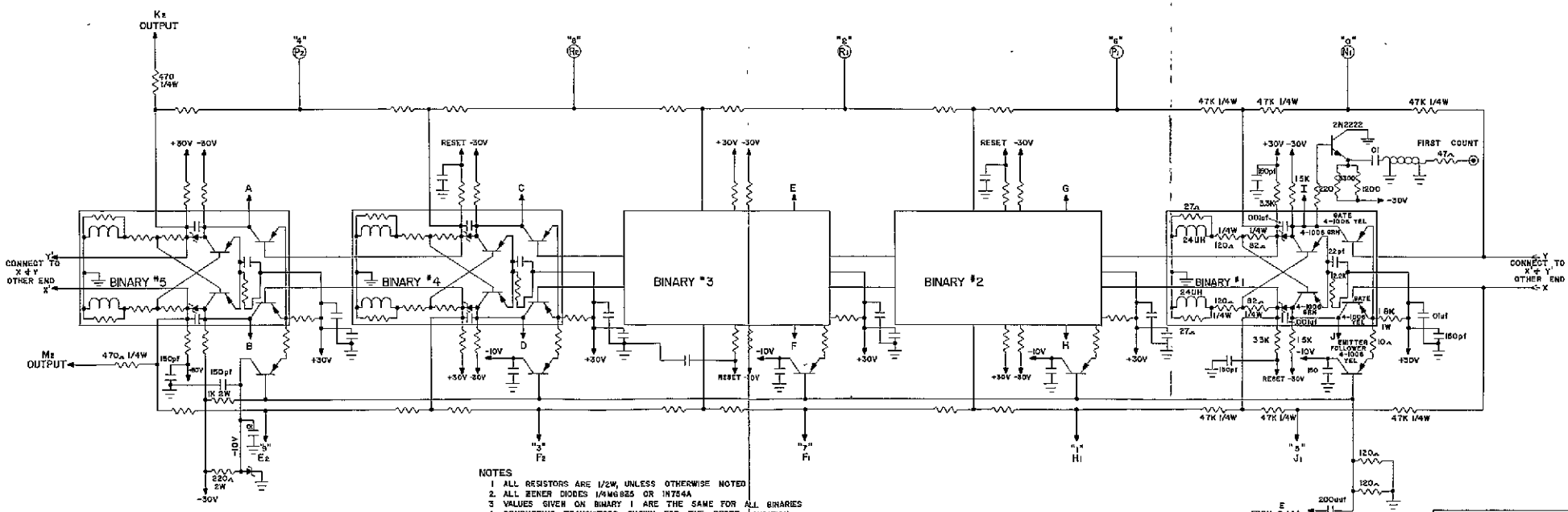
The First Count Circuit is an emitter follower connected

via a 220 ohm resistor to the collector of the "on" transistor of the flip flop which receives the first count. The First Count Output becomes about -2 volts when the first count is registered.

The Units Discriminator is a group of 10 amplifiers each connected to the collectors of the units counter flip flops. The collectors of the 2N3959 transistors in each amplifier are connected in parallel to form a 10 way OR gate. In each amplifier the 2N3907 transistor is in the "off" state until the collector to which it is connected becomes negative. The negative going transition causes the 2N2907 to conduct for about 15 nanoseconds causing the 2N3959 to conduct giving a negative output pulse of about 20 nanoseconds width and 2 volts amplitude. Each input capacitor determines the width and amplitude of the pulse associated with the negative level shift of one of the transistors. Each input capacitor is adjusted to provide equal output pulses, one for each units count.


REGENERATIVE DIFFERENTAL AMPLIFIER
OUTPUT BUFFER
BURROUGHS 6844A
-30V 15
-6V 8
INPUT 11
INPUT 13
+6.8V 12
GRN 9
10
POS RESET INPUT 4
MAN RESET INPUT 6
NEG RESET INPUT 1
INPUT
47K 1/2W
820 2W
270
390
CD6267
43V Z IN749A
S-570-G
22pf
3-1001
4-1004
4-1004
4-1004
27K 1/2W
22K
INVERTER SHAPER AMP
18K
27K
3-1001
3-1001
4-1002
0012uf
12K
22K
1.5K
01uf
18K
150pf
+6.8V
GROUND
-6V
56K 1W
2
0 1 2 3 4 5 6 7 8 9
3 13 12 11 10 9 8 7 5 4
4-1001 TYP
A GRD
M "9"
L "8"
K "7"
J "6"
H "5"
F "4"
E "3"
D "2"
C "1"
N "0"
14 OUTPUT TO S71A
3 +30V
5 OUTPUT HIGH SPEED RESET(NEG)
7 OUTPUT LOW SPEED RESET(POS)
+30V
470
001
3-1001
3-1001
1.2K
150
2N2222
5000uuf
1.2K
22K
10K
100K
1.5mh
3-1001
150pf
470pf
6.8K
4-1002
3-1001
2N2218
HIGH SPEED RESET GEN
LOW SPEED RESET GEN
200uH
22K 1/2W
10K
6.8K
15K
150pf
22
01uf
680
1K
47
1K
3-1001
150pf
-6V
+6.8V
150pf
GRD
NOTES UNLESS SPECIFIED
1 ALL RESISTORS 1/4W 5%
UNIVERSITY OF MARYLAND
READOUT & RESET
E-1
ENG
DWN
CKED
ES 69/70 7790
DATE 10-23-69





FOLDOUT FRAME 1

FOLDOUT FRAME 2

ENG	Straznicki	UNIVERSITY OF MARYLAND	
DWN	Leicht	20 Mhz COUNTING UNIT AND UNIT DISCRIMINATOR	
CKED	Straznicki	E-2	
ES 69/70 7790	DATE 10-15-69		

APPENDIX F

TIME DELAY GENERATOR (TDG) MODIFICATIONS

Reference is made to the operation manual for the Eldorado Model 650 1 Nanosecond Digital Delay Generator with 10 digit readout and provision for remote programming (Option J).

Diagram F-1 shows a pulse shaping network that is added to provide the proper strobe pulses so that information from the computer interface may be read into the TDG. The wire normally on pin A of switch S-1 is removed and connected to the output (b) of the pulse forming network while the input (a) of the pulse forming network is connected to pin A of S-1. Pulses from the computer interface have an amplitude of about plus 3 volts and width of 300 nanoseconds. The pulse shaper is a series of amplifiers connected so that an output pulse of +6 volts and 1 or 2 microsecond duration capable of driving the BCD to 9's compliment converters is produced.

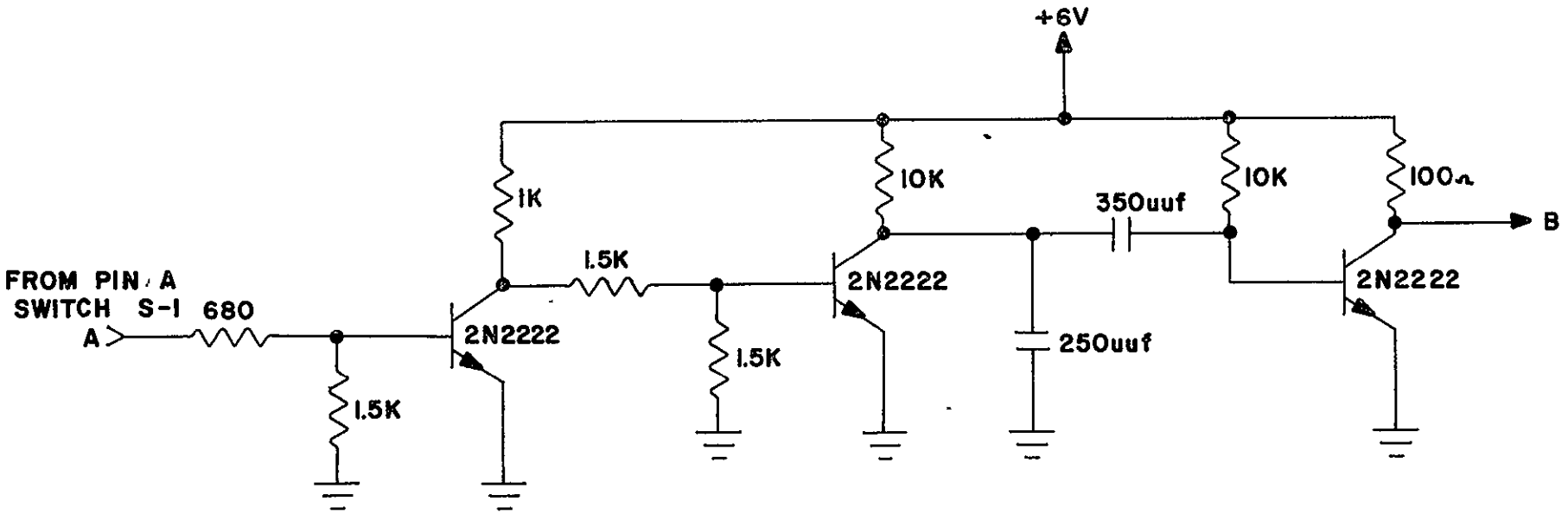
The Table on diagram F-1 shows the pin connections for the 10th digit and a listing of the spare pins on the computer interface jack which is located on the rear panel.

Refer to Eldorado diagram C-11-05636 concerning the schematic diagram of the BCD to 9's compliment circuits. Pins D and L corresponding to the "4" bit have a 1.5k ohm resistor connected to the +6 volt bus on all modules. Without this resistor, the voltage is +3.5 volts, causing an indeterminate state when a "true" signal is sent. The resistor supplies sufficient current to pro-

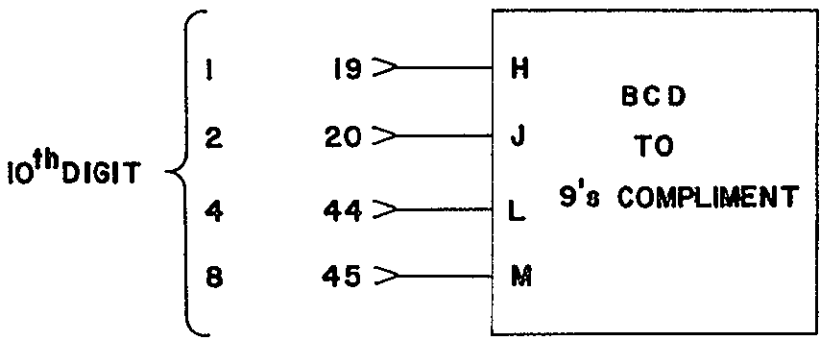
duce a "true" signal of +4.5 volts and a "false" signal of 0 volts. The "1", "2", and "8" lines do not have this problem.

Eldorado diagram D-11-05638 shows the schematic diagram for the BCD to Decimal circuits. Capacitors of .05μf capacity are added to the output terminals which lead to the 1 nanosecond and 10 nanosecond delay networks. The reason for this is that the capacitors are necessary to prevent any transient pulses that are picked up from firing the very sensitive tunnel diodes in the 10 and 1 nanosecond circuits. As an added precaution against noise, the input connections for the BCD "4" and "8" for the most significant digit are grounded. Thus it is impossible to derive a delay longer than 3.999999999 seconds.

Refer to diagram D-11-05327 the "Interconnect Diagram" for the final change. Between the terminals 12 and 14 on the delayed Output Amplifier and Shapers (32-05136) a .01μf capacitor is added to lengthen the output pulse to 6 microseconds. The 82μ capacitor found between terminals 14 and 16 on the output amplifiers is removed to produce a pulse of 50 nanoseconds.



10th DIGIT PIN CONNECTIONS



SPARE PINS 21, 23, 25, 46, 49

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PULSE FORMING NETWORK FOR TDG

F-1

ENG	STegarden		
DWN	danny		
CKED	STegarden	ES 69/70 7790	DATE: 11-3-69

APPENDIX G

ASTROVERTER SYSTEM

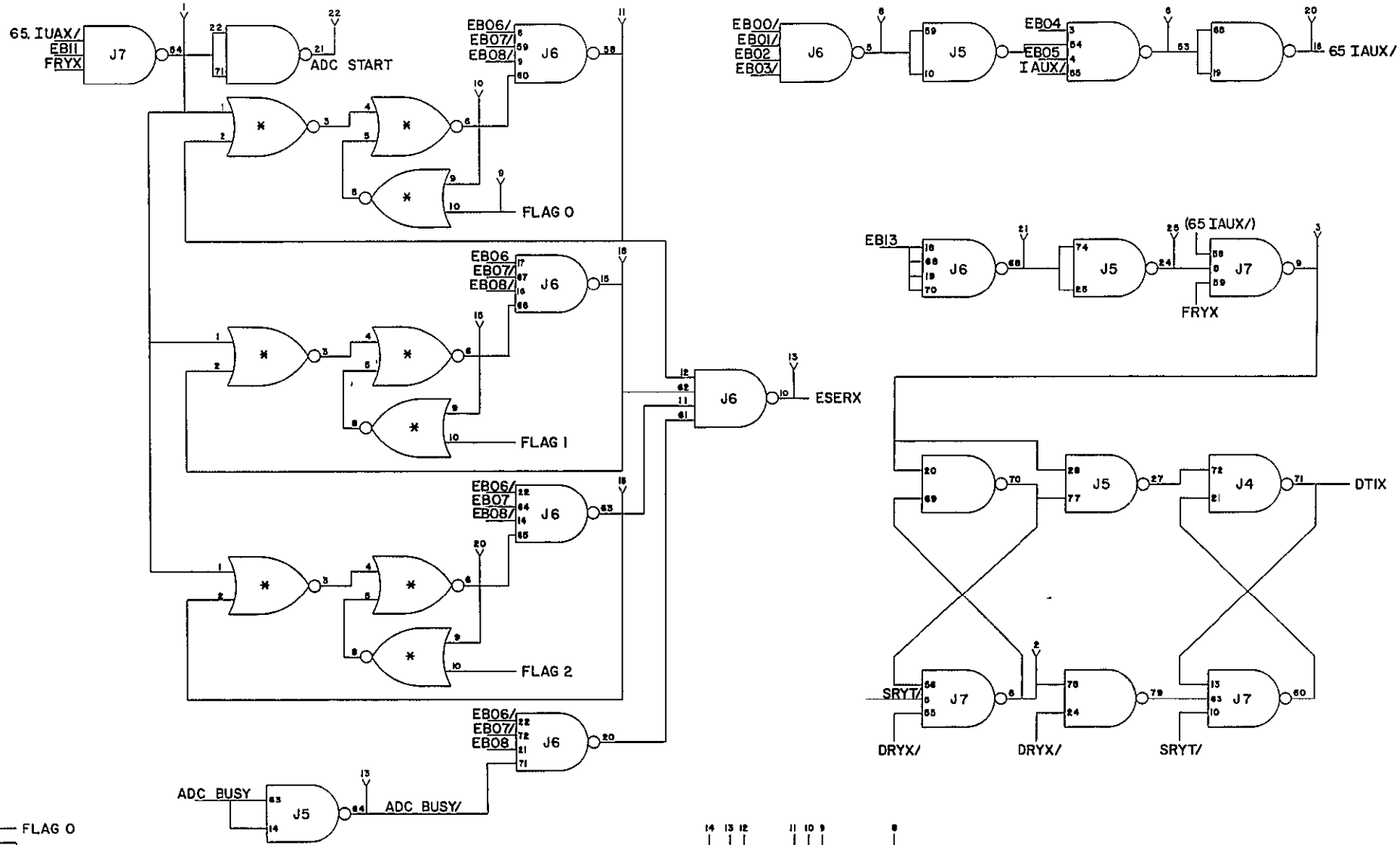
Reference should be made to the instruction manual supplied for this particular Astroverter system which describes in detain the individual circuits. Also please read J. Rayner's article concerning necessary programming for the 620/i computer to operate the Astroverter.

There are two changes in the logic of the computer-Astroverter interface. Reference is made to Astrodata drawings 3900-8000 sheet 2 of 2. This drawing is replaced by drawing G-1. The changes are described below:

1. Originally the computer data flag ESERX could only be found true while the flag pulses from the TPHCs were present, namely 4 microseconds. Unless the computer was in a tight programming loop watching for a particular flag it would miss the flag. A change was made to add flip flops so that a flag pulse from the TPHCs would set the flip flops, the outputs of which would be connected to the original AND gates. The computer could then read the flags at any time. The flip flops are reset with the multiplex address command (65.IUAX/, EB11 and FRYX).

The ICs chosen are NOR logic chips connected to form flip flops.

2. The connections to EB06, EB07/, EB08/ are removed from J6 pins 69, 19, 70, so that the computer has more flexibility in reading the output buffer. Without this change, only one computer command, namely "read into A register" could read data to the computer.



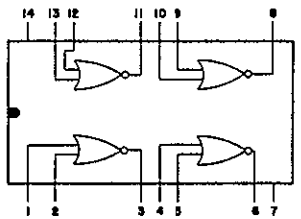
B D — FLAG 0

A C — DATA 0 | K M — DATA 2 | U — DATA 5 | M M — | B B — DATA 12

F J — FLAG 1 | N N — | W — DATA 6 | Y — DATA 9 | C C — DATA 13

E H — DATA 1 | P S — DATA 4 | V — DATA 7 | A A — DATA 10 | E E — DATA 14

L N — FLAG 2 | R T — FLAG 4 | X — DATA 8 | Z — DATA 11 | D D — DATA 15



PIN 14 = Vcc +5VOLTS

PIN 7 = GROUND

NOTE

* INDICATES NEW MODULES ADDED TO CARD J6

UNIVERSITY OF MARYLAND		
REVISED DRAWING OF COMPUTER INTERFACE LOGIC # 3900-702 # 2 OF 2 620 TO ASTROVERTER G-1		
ENG		
DWN		
CKED	ES 69/70 7790	DATE 10-31-69

APPENDIX H

DISCRIMINATORS

Type 1 Discriminator

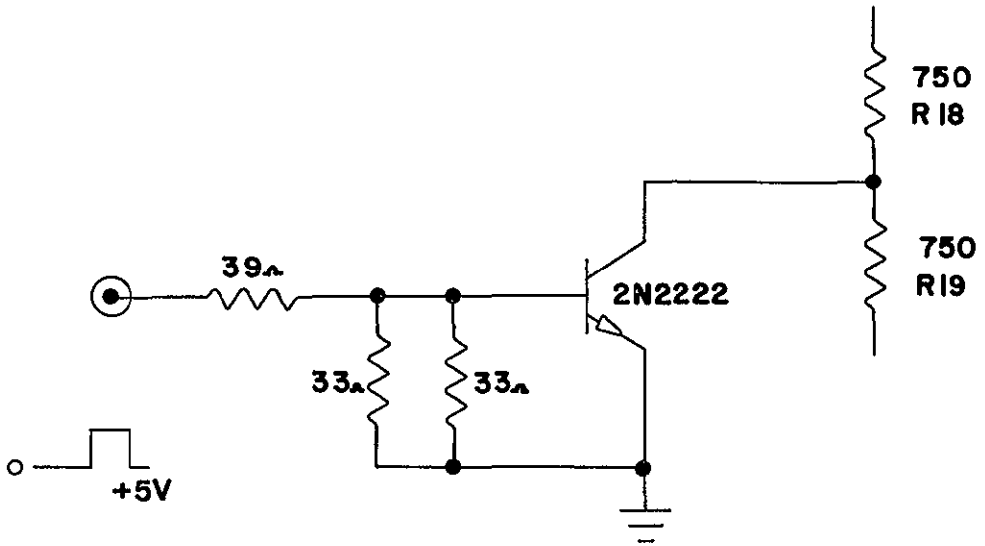
A Type 1 discriminator is an Ortec model 417 Fast Discriminator modified to accept positive 4 or 5 volt pulses from the Korad photo-diode light pulse detector. As is shown in Figure H-1 a single transistor is added whose collector is connected to the junction of R18 and R19 shown in Ortec drawing 417-0101-52 found in the Model 417 instruction manual. The input to the new transistor is connected to a new BNC input connector.

Type 2 Discriminator

Unmodified Ortec model 403 or equivalent.

Type 3 Discriminator

Unmodified Ortec model 417 or equivalent.



RESISTORS FOUND IN
ORTEC MODEL 417
FAST DISCRMINATOR

UNIVERSITY OF MARYLAND			
MODIFICATIONS FOR TYPE I DISCRMINATOR H-I			
ENG	Steggerda		
DWN	Lanny		
CKED	Steggerda	ES 69/70 7790	DATE: 11-3-69