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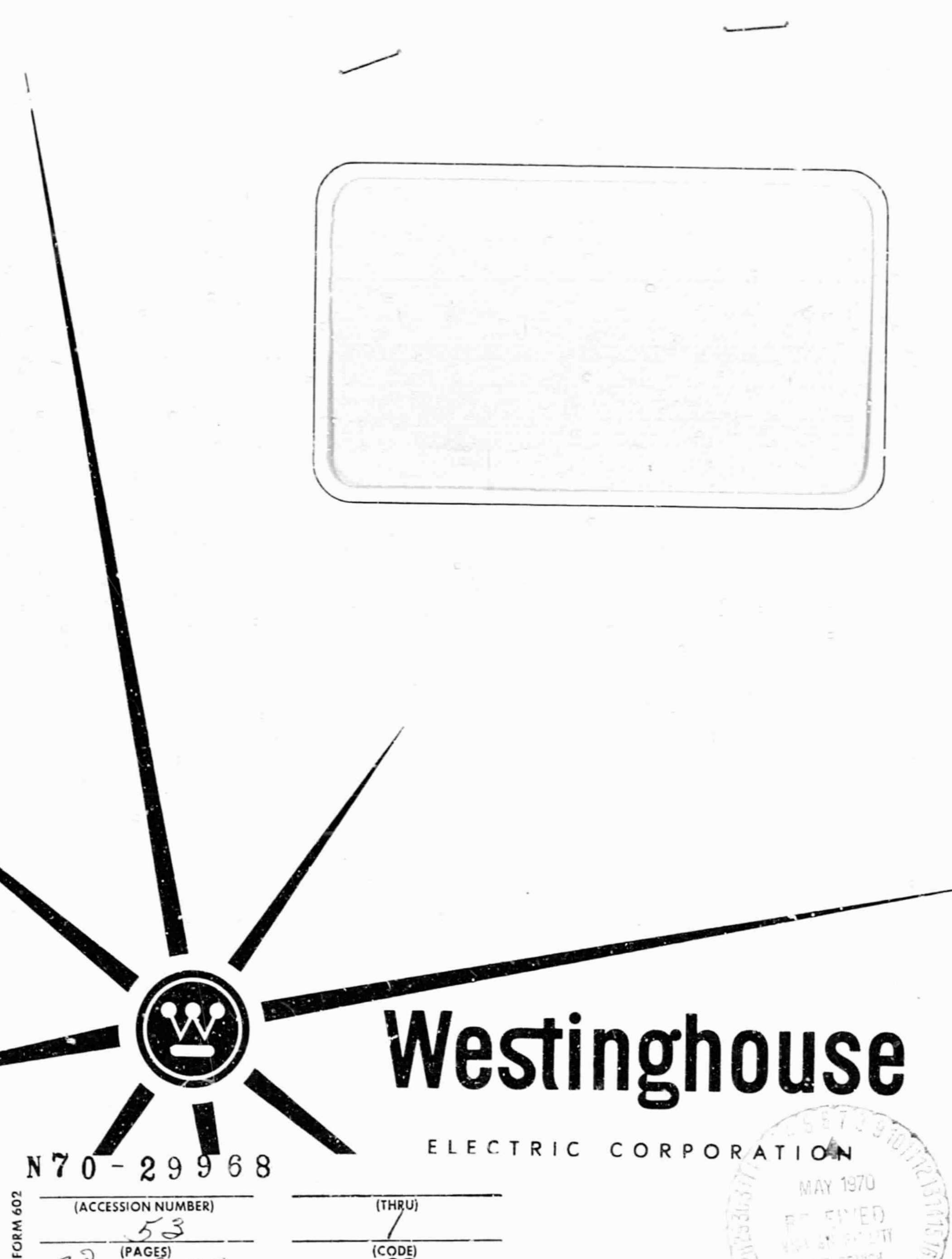

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Final Report
For

Apollo Communication Systems Support

Task 5 - Lateral PNP Design Optimization

NAS 9-6636

WEC GO HS - 51431

March, 1970

Prepared by

Westinghouse Electric Corporation
Defense and Space Center
Baltimore, Maryland

For

National Aeronautics and Space Administration
Manned Spacecraft Center
Houston, Texas 77058

1.0 INTRODUCTION AND SUMMARY

The purpose of this program was the design optimization of lateral PNP transistors. To this end an experimental set of lateral transistors were designed and fabricated. Parameters investigated included the various diffusion profiles as well as the geometric dimension of the transistor. Based on these results another set of transistors were designed and incorporated into a general purpose breadboard MSC-6 which included diffused resistors, pinch resistors, vertical NPN transistors and various designs of lateral PNP transistors. Packaged chips and wafers were delivered.

The lateral PNP transistor introduced to the integrated circuit field by H. C. Lin* of Westinghouse has found wide application despite somewhat poor performance as compared to vertical transistors. Some background concerning the lateral transistor and the composite PNP transistor are given in section 2.0. In section 3.0 the design consideration for lateral PNP transistors are discussed. Both the dc current gain and the high frequency performance are covered. In section 4.0 the experimental results are given as well as details on MSC-6. In the final section the processing problem areas and a specification are given.

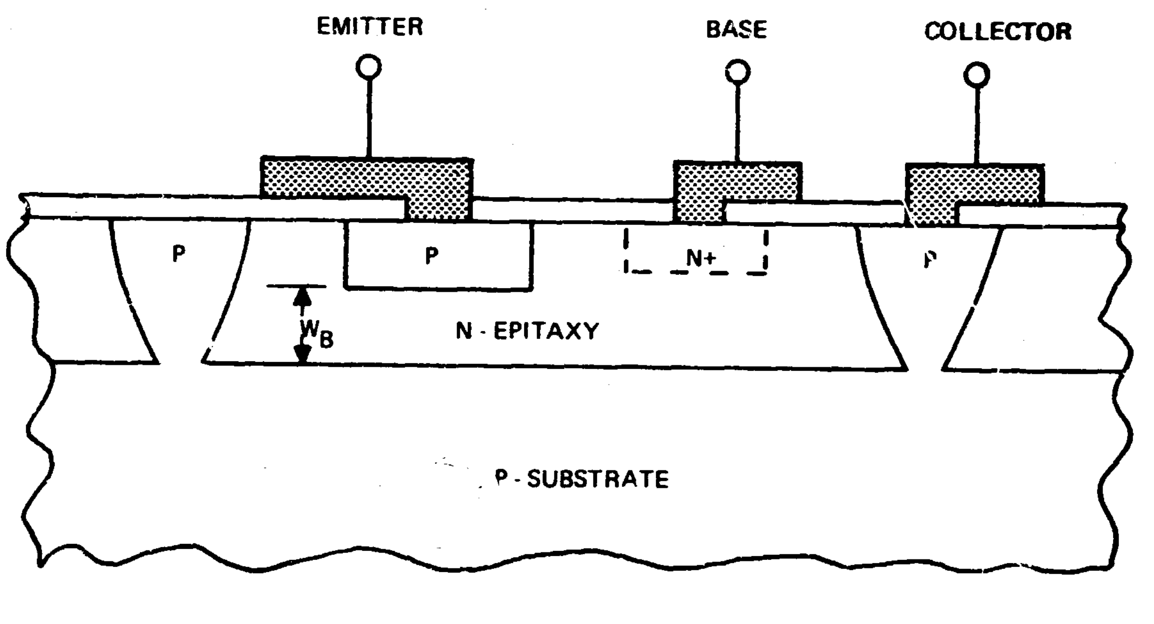
The conclusion of this program indicates that in order to obtain current gains greater than 100 @ Ic = 0.1 - 1.0 ma the emitter should be heavily doped, the collector should completely surround the emitter, the effective basewidth must be controlled by use of lateral diffusion and the surface state density must be minimized by proper sintering and passivation. To minimize losses to the substrate through parasitic transistor action, the emitter should be over an out diffused N+ region that creates a retarding

* US Patent No. 3197710

field for vertically injected hole current. This effect also improves frequency response by reducing the diode storage effect that would be present without the N+ region. Finally the transit time must be reduced by forming an aiding field in the base region either by passing a current through the base region from emitter to collector or by modifying the diffusion profiles by several techniques.

2.0 BACKGROUND

One severe limitation of the earliest available monolithic integrated circuits was that bipolar PNP transistors could not be used. Of course, for laboratory quantities of circuits rather elaborate processing sequencies could be used to allow the inclusion of PNP transistors, but this approach was not at all practical for large quantities of circuits. With the introduction of the burried collector process, as compared with the N/N+ double epitaxial process, it became possible to selectively utilize the parasitic vertical PNP transistor to the substrate as shown in figure 1. The applications of this structure, however, are limited to those where the PNP collector is connected to the most negative potential in the circuit. Even so, the parasitic vertical PNP transistor was used frequently and in particular it was used in many of the operational amplifiers available at the time.



More flexibility of design was achieved through the introduction of the lateral PNP bipolar transistor by the Westinghouse Electric Corporation.*

*H.C. Lin, et.al., Proc. IEEE, vol. 52, pp. 1491-1495, Dec. 1964..

This structure shown in figure 2 used the same diffusion that forms the NPN base region, to simultaneously form both the PNP emitter and the PNP collector.

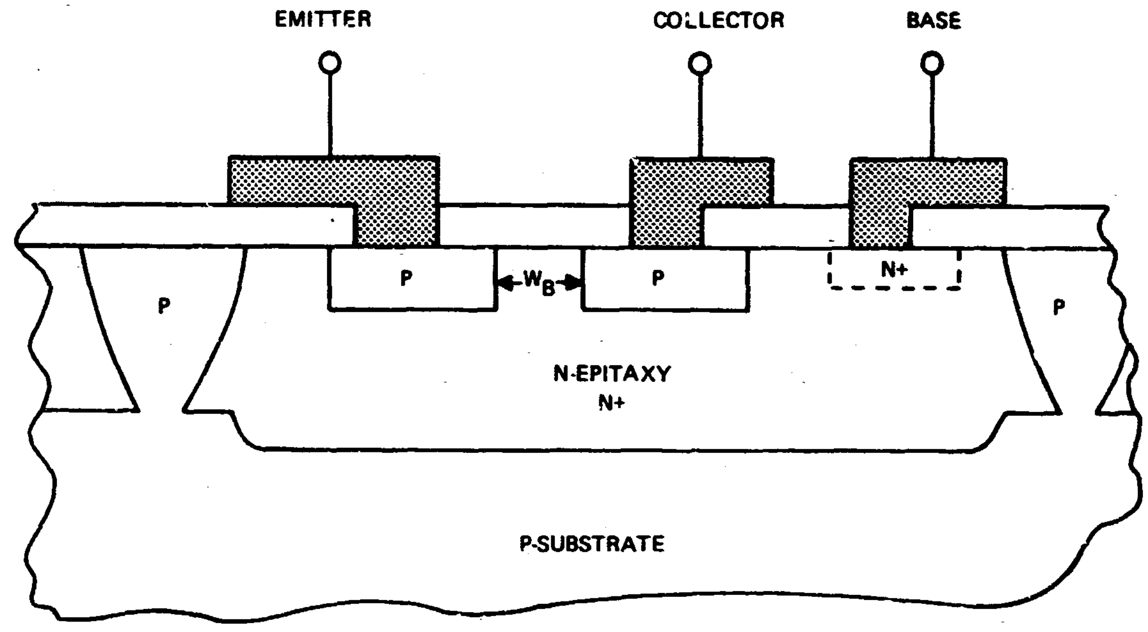


Figure 2. Lateral PNP Transistor S70-328-VA-9

Still, drawbacks existed, for the current gains were generally less than ten and the frequency response, f_T, was less than 10MHz. For many applications this type of structure was adequate. When circuit designs required higher Betas so that resistor ratios rather than absolute values could be used, the Lateral PNP transistor itself became inadequate.

Low current gains of the lateral PNP transistor were improved by the use of a vertical NPN bipolar transistor to amplify the collector current of the lateral PNP. This combination , also introduced by Westinghouse Electric Corporation, is referred to as the "Composite PNP" transistor. (See figure 3) Connected in the manner shown, the overall current gain is the product of the lateral PNP and the vertical NPN gains. Thus, even if the lateral PNP current gain is as low as unity the composite gain obtained is useable.

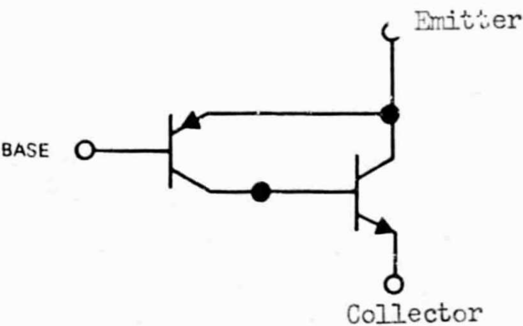
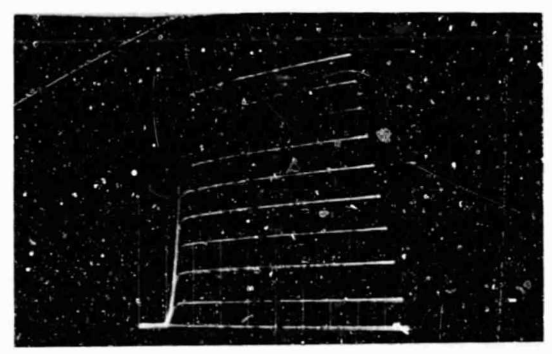


Figure 3. Composite PNP Transistor Schematic



HORZ 0.5V/DIV
VERT 0.1 MA/DIV
STEPS 0.001 MA/STEP

Figure 4. Composite PNP Characteristics

Four problems exist with the composite transistor:

a) Required area is doubled.

b) $V_{OFF-SET}$ is 0.6 volts. (See figure 4)

c) f_T is still poor.

d) For switching applications the storage time is large.

The area is doubled because the composite structure requires two isolated transistors to achieve useable current gains. The off-set voltage of a diode drop is introduced by the circuit configuration. If matching push pull stages are required, then the NPN must be degraded by placing a diode in series with the collector. The frequency figure of merit is not increased since the same lateral structure is used. The storage time is large because when the composite turns OFF the NPN base must discharge through the reverse biased base-collector junction of the lateral PNP transistor. One technique for reducing the storage time is to add a bleed-cff resistor to the base of the PNP transistor. This, however, reduces the overall composite current gain by diverting useable base drive and also increases the area of the composite structure to that of three components. This approach is quite useful in many applications.

With the advent of MOS-bipolar technology the bleed-off resistor can be replaced with a parasitic p-channel MOS transistor to the substrate. As shown in figure 5 this is a MOS transistor at the surface between the actual NPN base region and the p-type substrate. This approach requires no additional area, does not degrade current gain and does not require any stand-by power. In effect, the MOST is simply a switch that is open when the NPN is ON and is closed when the NPN of the composite is OFF. The signal required for the gate electrode is negative with respect to the NPN collector region. The

threshold voltage of the MOST is dependent on the oxide thickness under the gate, the orientation and resistivity of the epitaxial layer and the amount of mobile charge trapped within the oxide or at the interface. Typically this is of the order of 10-20 volts. A reduction of the oxide under the gate can selectively reduce the parasitic MOS threshold to less than 6 volts.

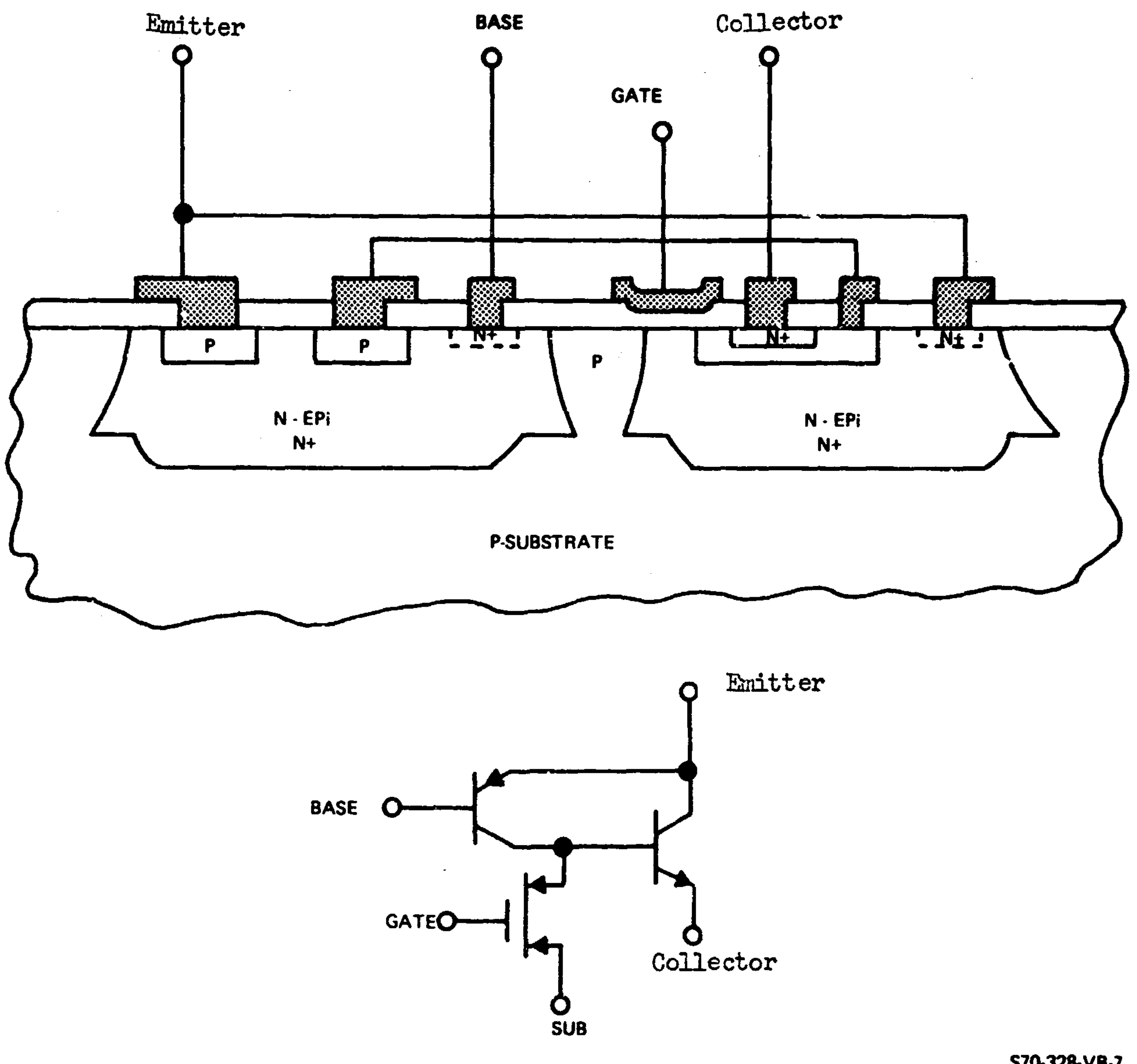


Figure 5. Composite PNP with MOS Switch

3.0 LATERAL PNP DESIGN CONSIDERATION

As previously mentioned, the purpose of this contract was the design optimization of lateral PNP transistors with a minimum addition of processing steps. The main areas that were concentrated on were:

a) Maintain a simple process.

b) Reduce losses through parasitic transistor action.

c) Increase peak current gain of lateral transistor.

d) Increase useful current range of lateral transistor.

e) Improve f_T of lateral transistor.

f) Reduce switching speeds of lateral transistor.

Each of the above areas were considered in the design and fabrication of lateral PNP transistors on this contract. Some areas showed slight improvement while other areas of interest were substantially improved.

3.1 Current Gain

If the lateral PNP transistor is fabricated with no additional process steps over the standard NPN circuits, then the same diffusion used for the NPN base will be used for the PNP emitter. A detailed cross-sectional view of this structure is shown in figure 6. There are two types of injected emitter current: hole current (I_p) injected into the base region and electron current (I_n) injected into the emitter. Each of these types has two components; the lateral (y) and the vertical (x) components. For the lateral PNP transistor the lateral injected hole current should be maximized and all other components minimized.

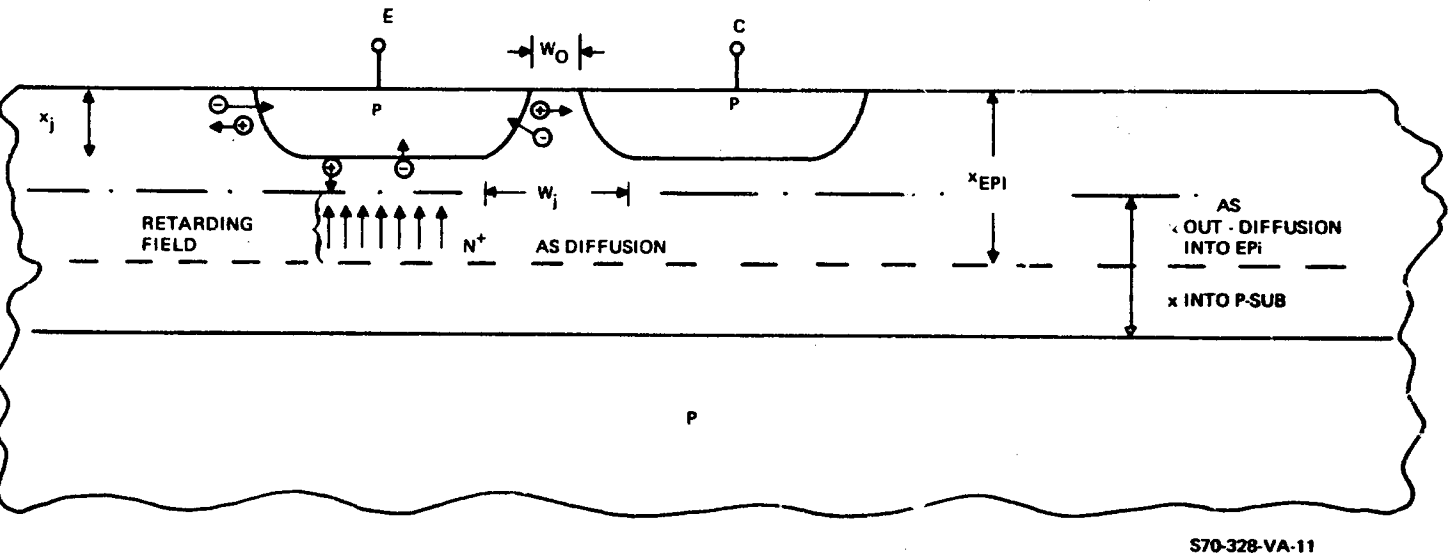


Figure 6. Lateral PNP Detailed Cross Sectional View

3.2 Concentration Gradient

For a double diffused PNP transistor with a P+ emitter, most of the emitter current is carried by the holes and the electron current can be neglected. In this case $I_p = I_E$. For the lateral PNP transistor described above the emitter is not P+ nor is it shallow diffused hence it can not be assumed that $I_p = I_E$. To minimize the electron current the concentration gradient within the emitter junction should be increased. If the PNP emitter diffusion is the same as the NPN base, and the diffused resistor diffusion, there are obvious limitations present. One technique for decreasing the electron current is to use a separate P+ diffusion with as high a surface concentration as possible. A shallow junction depth also increases the concentration gradient.

Since the p-type emitter is diffused into a homogenous base region, the n-type epitaxial layer, the vertical and lateral components of the hole current are the same. If a sub-diffusion of arsenic or phosphorous is performed beneath the emitter and allowed to out diffuse to the emitter then

$$\frac{I_{px}}{A_x} = J_{px} \neq J_{py} = \frac{I_{py}}{A_y}$$

where A_x and A_y are the planar and side areas of the emitter respectively and J_{nx} and J_{ny} are the vertical and lateral electron current densities. The out diffused n-type region can have two effects. It can alter the P-N step junction thereby effecting the electron current into the base and it can create a retarding field that effects the vertical component of the hole current injected. For both of these reasons it is desireable to include an N+ sub-diffusion beneath the emitter of the lateral PNP. If the diffusant used is phosphorous, it will out diffuse more rapidly and have a greater

effect*, however, this would require an additional two process steps and it would have an undesirable effect on the base emitter junction capacitance. A more straightforward solution would be to decrease the epitaxy thickness and to increase the arsenic pre-diffusion concentration.

Out diffusion of an n-type impurity beneath the emitter increases the capacitance per unit planar area by decreasing the base emitter space charge region. The decrease in electron current into the base is effected by the space charge region width since it can be subdivided into two components: the electrons that are injected into the p-type emitter, and those that are injected into the space charge region where they recombine with holes.

3.3 Geometric Effects

Geometric considerations are, of course, very important. If the ratio of hole currents I_{py}/I_{px} is to be a maximum, then the perimeter to area ratio of the emitter must also be a maximum. Thus interdigitated emitter and collector stripes of minimum width are best while circular emitters are poor. The problem with this solution is that the lateral PNP current gain generally peaks at low current levels ($I_c \leq 1$ ma) where surface effects are important. Maximizing the P/A ratio further enhances the effect the surface recombination velocity variations will have on current gain. This is discusses in more detail later in the next section.

3.4 Surface Recombination and the Diffusion Length

The lateral component of the hole current will now be considered.

* Hilbiber, D. F. IEEE-ED 14, July 67, p. 381.

The distribution of laterally injected holes in the uniformly doped base region depends on the minority carrier diffusion length L_p, the base width $W_{BO} \leq W_B \leq W_{Bj}$ and the effect of surface recombination velocity. If it is assumed that the hole concentration injected into the base falls off exponentially with distance from the emitter then if $W_B \gg L_p$ the distribution will be exponential. If $W_B \ll L_p$, then the exponential approximation is further reduced to a linear fall-off. The diffusion length of minority carrier holes in the base region is given as

$$L_p = \left[\frac{kT}{q}\right]^{\frac{1}{2}} \cdot \left[\tau_p \mu_p\right]^{\frac{1}{2}}$$

where τ_p and μ_p are respectively, the lifetime and mobility of holes in the n-type base region.

Lifetime is then subdivided into two components:

$$\frac{1}{\tau_p} = \frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_{surface}}$$

where

$$\tau_{surface} \sim C_1 \left[\frac{W_B}{S_o}\right] \cdot \left[\tau_{bulk}\right]$$

and S_o = surface recombination velocity and the constant C_1 determines what portion of the base width is effective in reducing τ_{eff}. The fact that surface recombination velocity is important can be seen by referring to figure 7 which indicates the change in peak current gain during sintering as a function of base resistivity.

Various sintering cycles with temperatures of 400-500°C, 0% H_2 - 100% N_2 to 100% H_2 - 0% N_2, times of 5-60 minutes and both rapid and slow cooling were investigated. The greatest effects were introduced with

hydrogen present. Small percentages of hydrogen are best since the effect passes through a peak as the concentrations of positive ions introduced in the oxide increases and the distribution changes. The only effect of temperature and time was to alter the rate of change of the peak current gain. No effect of rapid versus slow cooling was observable. It was assumed that the gas treatments were effecting the surface component of the lifetime by changing the surface recombination velocity. The image effect of changes in the oxide on holes present near the surface was discounted since devices operated with a gate electrode over the oxide between emitter and collector could not produce changes in peak current gain of 60 as was observed with sintering. The gate electrode effect on current gain was generally in the 2 to 5 multiplication range. The surface recombination velocity also effects the emitter injection efficiency by increasing the recombination rate in the space charge region of the emitter base junction. As S_o increases then the component of the electron current I_{nx} that results from electrons recombining in the space charge region will increase and emitter efficiency will decrease. The emitter efficiency can be derived* as a function of the surface recombination velocity and the surface areas (A_s) of the space charge region:

$$\gamma \sim \frac{1}{S_o A_s}$$

As epitaxy resistivity is increased the space charge region and A_s increase and S_o is more effective.

* A. S. Grove, Physic and Tech. of Semiconductor Devices (Wiley), p. 218.

It is pointed out by J. Lindmayer*, et.al., "that surface recombination velocity becomes a factor only at very high values of current gain, when the vertical current is small." The effect of surface recombination velocity on transistor current gain is also referred to by A. S. Grove**, "The recombination current in the surface space charge region around the PNP emitter is directly effected by the generation current in that region." One of the generation components thus effecting the recombination current is

$$I_{gen,s} = \frac{1}{2} q N_i SoAs$$

where N_i is the intrinsic carrier concentration and As the surface space charge region.

As previously pointed out the recombination current contributes to base current and thereby lowers the common-emitter current gain h_{FE}. This effect is important at low collector current levels. The effect is less at higher currents because** recombination currents increase with the factor $\exp q|V_F|/2kT$, but collector current increases as $\exp q|V_F|/kT$.

Since the experimental measurements discussed in the next section are generally made at low collector currents where the lateral PNP common emitter current gain can be as high as 100-200, surface recombination is considered to be important.

3.5 Current Gain Summarized

In summary, the current gain of the lateral PNP transistor is optimized

* Solid State Electronics, Vol. 10, No. 3, p. 225 (1967).

** A. S. Grove, ibid.

by increasing the concentration gradient within the emitter region to reduce I_n and creating a retarding field under the emitter by out diffusion to reduce I_{px}, by decreasing W_B so that $W_B << L_p$ and all laterally injected holes are collected and by minimizing surface recombination effects. Decreasing the basewidth was not covered in this section since it is primarily a process problem and as such is covered in Section 5.0

3.6 High Frequency Characteristics

The main effort in improving the high frequency characteristics of lateral PNP transistors concerned the switching speeds of the lateral transistor used as a load resistor. These considerations are covered in the section on experimental results.

For linear applications the f_T of the transistor should be considered. The main drawbacks of the lateral structure are:

a) charge storage of vertically injected carriers

b) poor transit time of laterally injected carriers

The charge storage effect in the base can be elinimated by reducing the vertical injection of holes into the base (I_{px}). As previously discussed, this is accomplished by performing an N+ diffusion beneath the emitter and forcing a retarding field. In this way I_{px} is reduced practically to zero and only a small electron current (I_{nx}) injected from the N+ sub-diffusion into the emitter remains. The magnitude of this current can be controlled by the doping levels. As a result, the N+ sub diffusion increases the low frequency current gain and extends the useful frequency. The method of detecting if the N+ diffusion is accomplishing the above effect is to observe the fall-off of current gain with frequency. If the N+ region is

effective, then the fall-off will be the usual -6 db/octave. If the fall-off is -3 db/octave, then the N+ region is not effective and the fall-off is resulting from base storage effects which predominate the high frequency performance.

The transit time for a uniformly doped base region, as exists in the lateral PNP transistor, is given as

$$t_b = \frac{W_B^2}{D_{pb}}$$

where W_B is the basewidth and D_{pb} is the minority carrier diffusion constant. The base cut-off frequency for the transistor is then given as

$$f_b = \frac{2.43\ D_{pb}}{2\ \pi\ W_B^2}$$

If the base region is graded, as in the case for the standard double diffused vertical PNP transistor, then the transit time is given as

$$t^1_b = \frac{t_b}{\ln\ (N_{BE}/N_{BC})}$$

where N_{BE} and N_{BC} are the donor impurity concentration at the edge of the base emitter and base collector junctions respectively. The built in electric field reduces the transit time significantly if N_{BE}/N_{BC} is large. Since there is no graded impurity distribution in the active lateral base region of the lateral PNP transistor, no drift field exists to accelerate the holes across to the collector. This effect reduces the usefulness of the lateral PNP transistor at high frequencies considerably.

There are two solutions to the problem: first alter the process to

form a graded impurity distribution in the base region and improve transit time, and second form an aiding electric field in the base region by applied voltages.

The techniquesfor performing the first are to numerous to detail. One technique previously mentioned is to use phosphorous as the sub diffusion beneath the emitter. Phorphorous out diffuses more rapidly then arsenic and it will form not only a retarding field for the vertically injected holes, but an aiding field for the laterally injected carriers. This requires that the phosphorous out diffuse vertically to the emitter and laterally toward the collector. Junction capacitances are increased.

A more straight forward approach is to pass a current through the base region from emitter to collector by the means of two base contacts. This effect was investigated using geometry No. 21 in the initial layout of devices. This structure has a circular N+ base contact surrounded by three P+ annular rings and then by an N+ annular ring. A dc current is passed from the center emitter to the annular base contact creating an aiding electric field in the base region. The first P+ annular ring is then used as the emitter and the next two rings are an a-c collector and a d-c collector. Using this technique the base transit time is reduced and given by the expression

$$t_b = \frac{W_B^2}{k(\epsilon)\, D_{pb}}$$

where $k(\epsilon)$ is given by * the expression

* A. N. Dow, et.a., Solid State Electronics, 10, 359 (1967)

$$k(\epsilon) = 2.43 (1 + \epsilon^{1.37})$$

$$\epsilon = \mu E W_B / 2D_{pb}$$

and

$$E \sim I\rho$$

where I is the lateral current flowing in the base region to form the aided field and ρ is the resistivity of the N+ region the current is flowing through.

The effect of the aided field is reduced if the N+ region carrying the current is not directly under the active base region, i.e., the N+ epitaxy or the pre-diffused region must out diffuse up to the emitter and collector regions. Alternately the N+ region can be eliminated from underneath the emitter as shown by E.L. Long.* The effect was observed on this program, but all transistors fabricated had the N+ region somewhat far removed from the emitter and collector regions so the improvements in current gain were not as great. Because the structure did not have the required profile, frequency measurements were not made.

* E. L. Long, IEEE Solid State Circuits Conference, 1970, Paper THPM Section 9.3

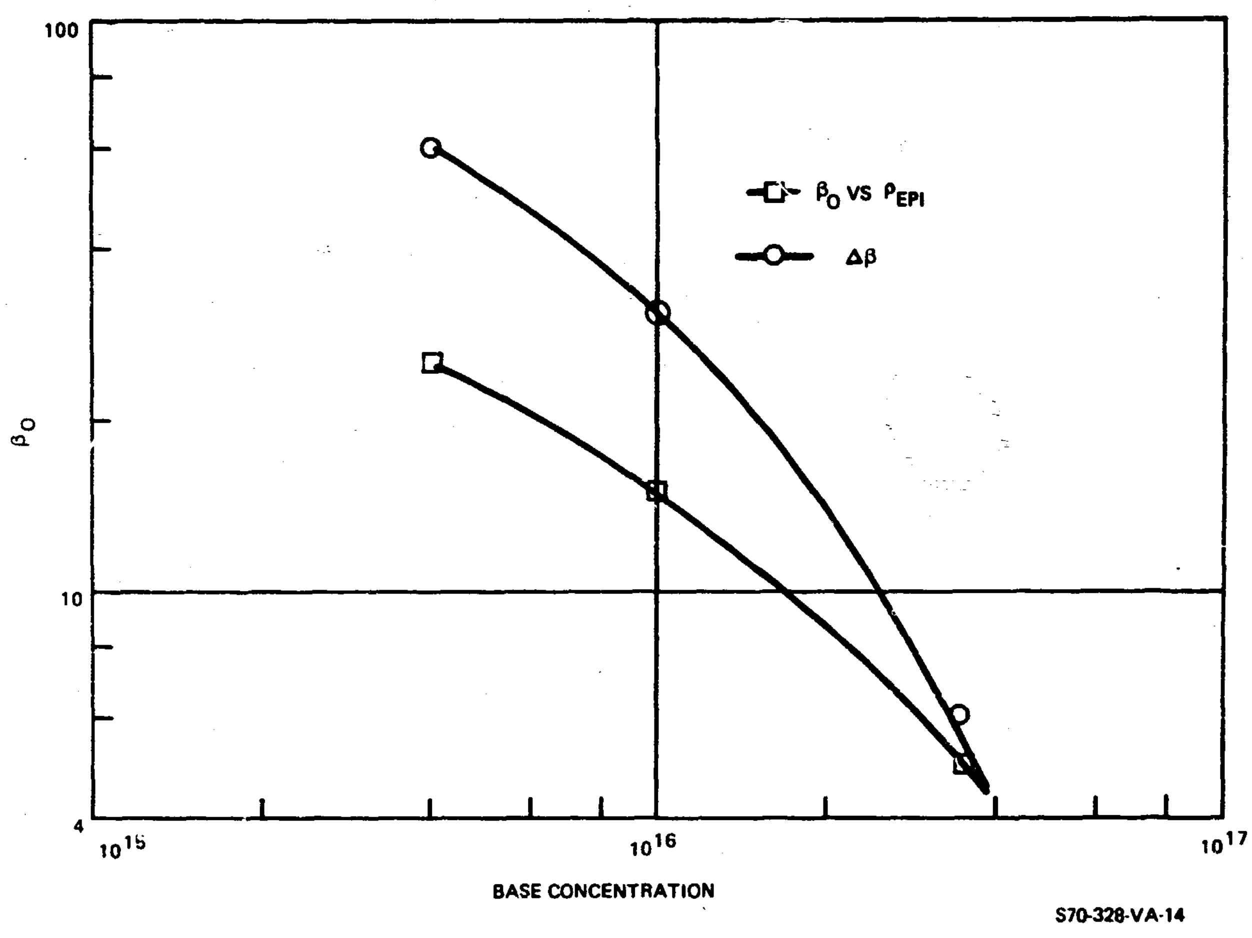


Figure 7. Variation of β_o with Sintering

4.0 EXPERIMENTAL RESULTS

4.1 MSC-6 General Purpose Breadboard Block

The MSC-6 breadboard block is a 109 x 109 mil die. (See Figure 8) The following table lists the major mask layout tolerances.

Minimum Resistor Width	0.4 mil
Resistor to Isolation Tub Edge	1.2
Minimum Spacing Between Adjacent Resistor Legs	1.2
Minimum Contact Window Dimensions	0.4
Smallest Contact Window	0.4 x 0.4
Minimum Spacing Between Contact Window & Junction	0.2
Nominal Spacing Between Contact Window & Junction	0.4
Minimum Isolation Lane Width	0.8
Collector to Emitter Spacing (Basewidth) of Interdigitated Lateral PNP's	0.4
Collector to Emitter Spacing (Basewidth) of Small Micropower Lateral PNP	0.2
Nominal Bonding Pad Size	4.0 x 4.0
Minimum Spacing Between Bonding Pads	0.4
Minimum Aluminum Stripe Width	0.8

The mask numbers and functions are listed below

Mask Number	Function
456-1	P+ Isolation diffusion
456-2	Base & resistor diffusion
456-3	P+ Diffusion
456-4	N+ Emitter diffusion
456-5	Contact window
456-6	Aluminum bonding pads

The chip consists of 52 components in 34 separate isolation tubs. There are 20 standard diffused resistors, 12 pinch resistors, 6 vertical NPN's, 11 lateral PNP's, 2 PN junction capacitors, and one thick oxide MOS-FET. All components except the resistors are in their own separate isolation tubs.

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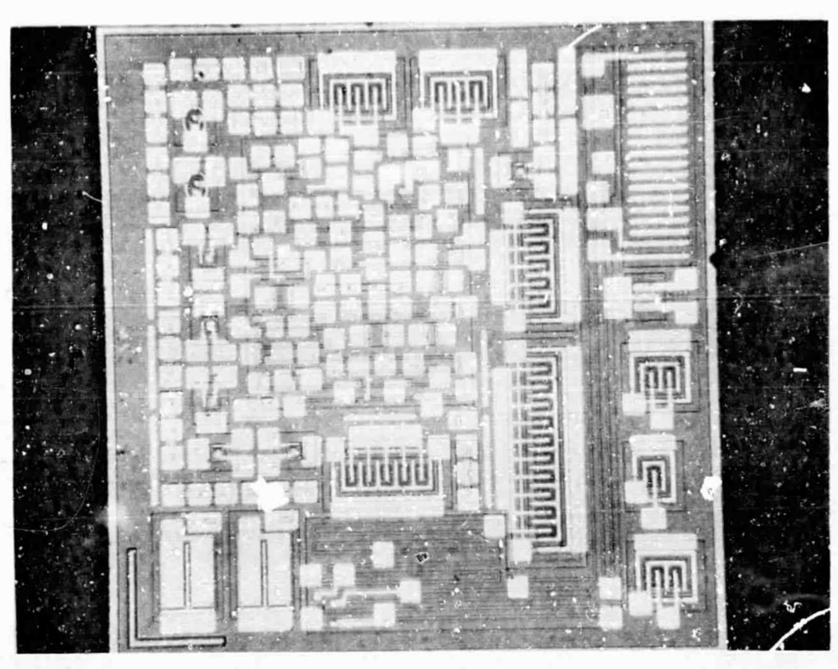

Figure 8. MSC-6

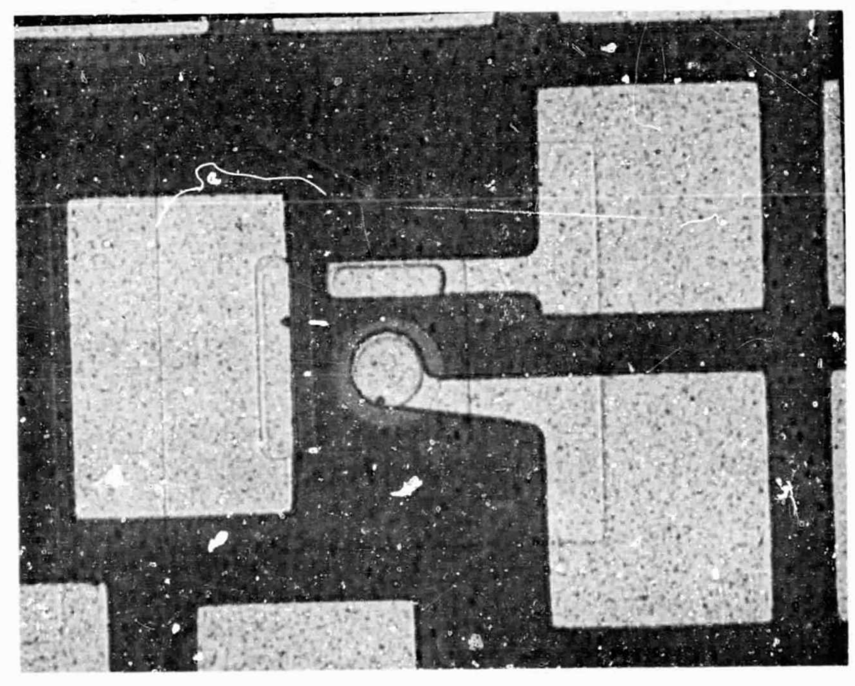

Figure 9. NPN Bipolar

The resistors are divided between two isolation tubs; the 4 large value resistors are in one tub and all remaining lower value resistors are in the other. The 12 pinch resistors are each located in a separate tub. Each is actually a pair with a common terminal.

The vertical NPN transistors are all identical in construction. Each has a rectangular base region 2.5 mils x 3.2 mils with a circular emitter of 0.9 mils diameter. Figure 9 is a photograph of one of the NPN's.

The two PN junction capacitors are identical and are actually a modified NPN structure. They are built like a large vertical NPN with the collector internally shorted to the emitter. This parallels the base-collector junction capacitance with the base emitter junction capacitance, thus the total capacitance is C_{bc} and C_{be}. Furthermore, the emitter is divided up into a striped configuration which increases the sidewall area of the emitter junction. The sidewall has a higher capacitance per unit area than the bottom of the junction due to the higher impurity concentration of the sidewall. The entire structure is metallized wherever possible to pick up additional MOS capacitance. The purpose of the design is to get the largest value capacitor possible in the smallest area possible. Since the base emitter junction and collector base junction are in parallel, the reverse breakdown voltage of the structure is determined by the base emitter breakdown.

Figure 10 shown the lower value resistor tub. This tub contains one 3K and three 4K resistors each tapped at 1K intervals, two 100 Ω and two 200 Ω resistors, four 50K resistors, two 18K resistors, one 20K resistor, and one 15K resistor. The 100 Ω and 200 Ω resistors are useful for monitoring the sheet resistivity of the base and resistor diffusion. The following

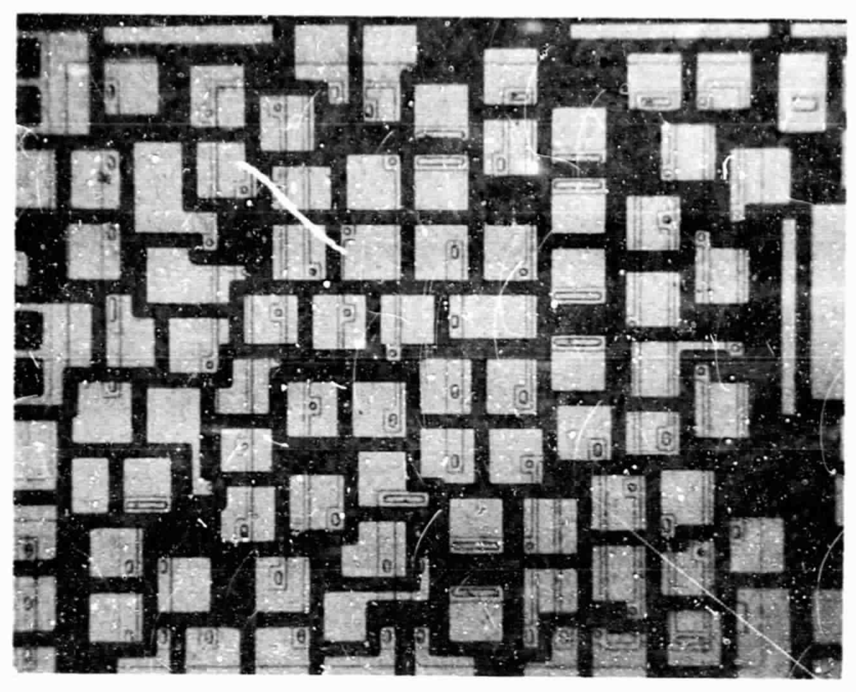

Figure 10. Low Value Diffused Resistors

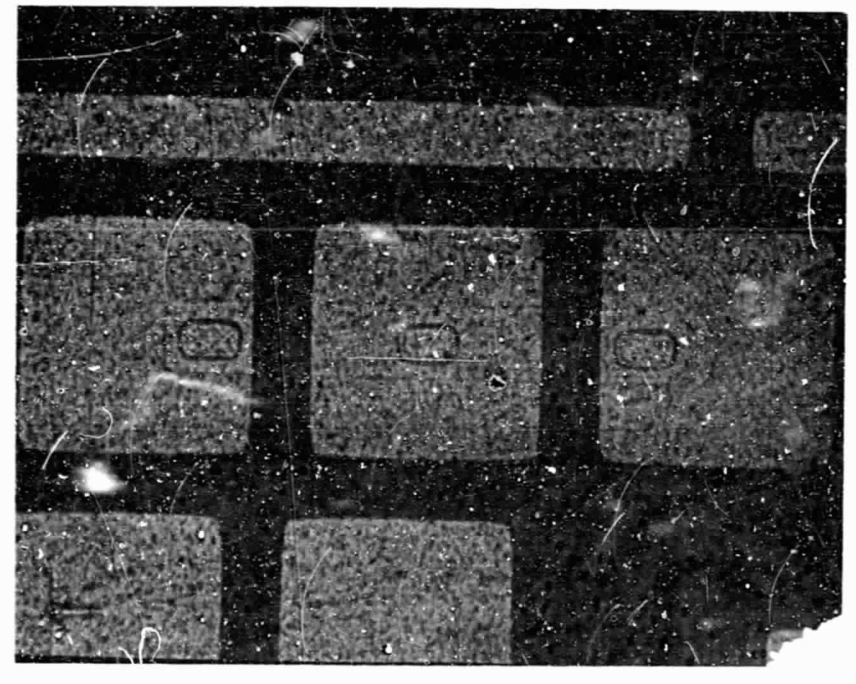

Figure 11. Pinch Resistors

table lists the resistor taps available on each resistor type.

R total (ohms)	R taps (ohms)
100	
200	
3K	1K, 2K
4K	1K, 2K, 3K
15K	9K, 12K
18K	6K, 15K
20K	10K, 14K
50K	3K, 11K, 14K, 22K, 28K, 34K, 40K, 46K
50K	10K, 16K, 26K, 29K, 34K, 36K
50K	10K, 12K, 15K, 26K, 34K, 40K, 43K
50K	8K, 14K, 21K, 27K, 33K, 41K, 45K

In addition to the above resistors, there are four higher value resistors: one 160K, two 80K, and one 200K. These are located in a separate common isolation tub and each is centertapped.

Figure 11 is a photograph of one of the pinch resistor pairs. The center bonding pad is common to each helf of the pair. In designing these components Irvins' curves* were used, hence the assumption was made that the presence of the N+ diffusion does not disturb the impurity distribution of the p-type impurities in the pinched-off region. The twelve pinch resistor

* John C. Irvin, "Resistivity of Bulk Silicon and of Diffused Layers in Silicon", Bell Syst. Tech. J., 41, p. 387.

pairs are of two designs: a 1.2 square 60KΩ pair (total resistance 120KΩ for the pair) and a 0.6 square 30KΩ pair (total of 60KΩ for the pair). There are six of each design on the MSC-6.

Figure 12 shows the thick oxide MOS-FET. This was included so that the threshold of the parasitic MOS-FET that exists between resistor legs and elsewhere could be measured and to allow C-V measurements for determining Q_{SS}.

The eleven lateral PNP transistors are divided into three types: interdigitated, micropower, and multiple gate. The interdigitated types are shown in figures 13 through 17 . These are subdivided into five types according to size and number of emitters although they all have the same basic geometry. There is one single emitter transistor, two double emitter, two triple emitter, two five-emitter, and one ten-emitter transistor. Each emitter is a 1.2 mil x 2.8 mil rectangle surrounded by the collector with a basewidth of 0.4 mil. Figure 18 shows one of the micropower PNP's. The circular emitters have a diameter of 1.2 mil with a 0.2 mil basewidth. Due to the narrow basewidth care must be taken in processing since these components may short due to lateral diffusion of the collector and emitter. On the other hand, the narrow basewidth offers the possibility of higher gain than is possible with wider basewidths. The multiple gate lateral PNP's is shown in figure 19 . This structure has a very wide basewidth (32 mils) with a series of intervening aluminum gates of 1.2 mil width spaced 0.8 mil apart. The intent of this design was to see which gate had the most effect on controlling the transistor beta when a voltage is applied to the gate.

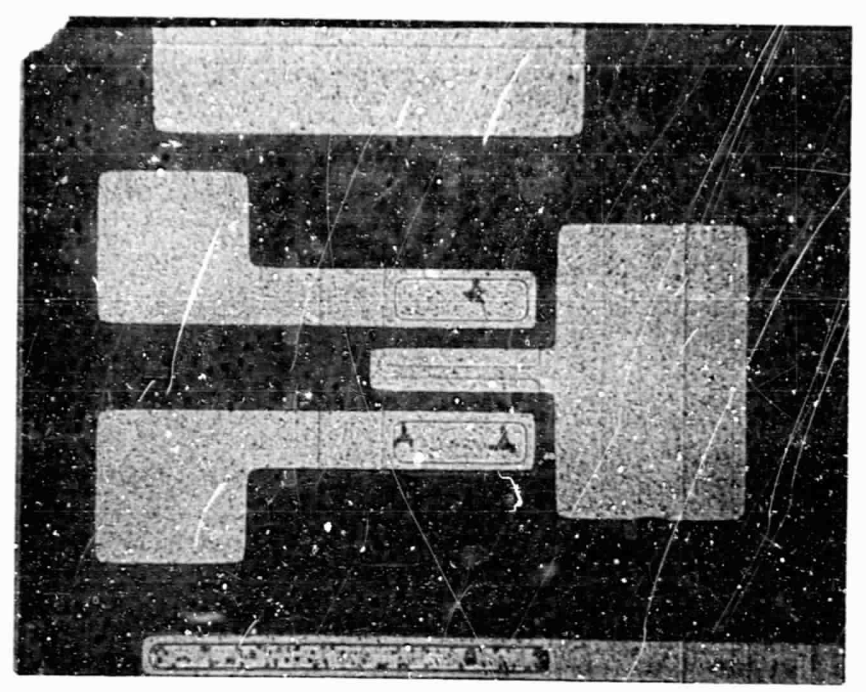

Figure 12. Thick Oxide P-Channel MOSFET

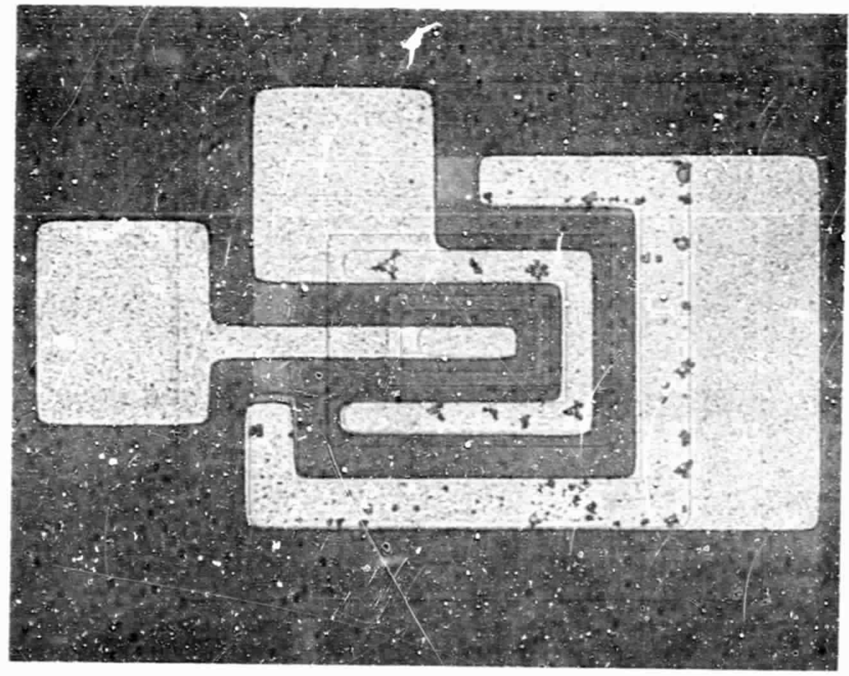

Figure 13. Lateral PNP Transistor - Single Emitter

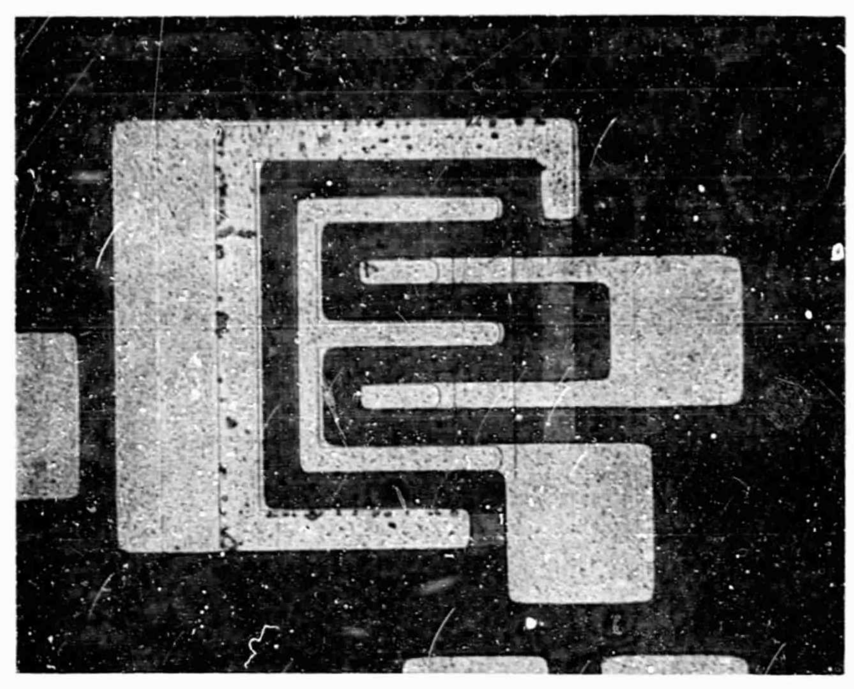

Figure 14. Lateral PNP Transistor - Two Emitters

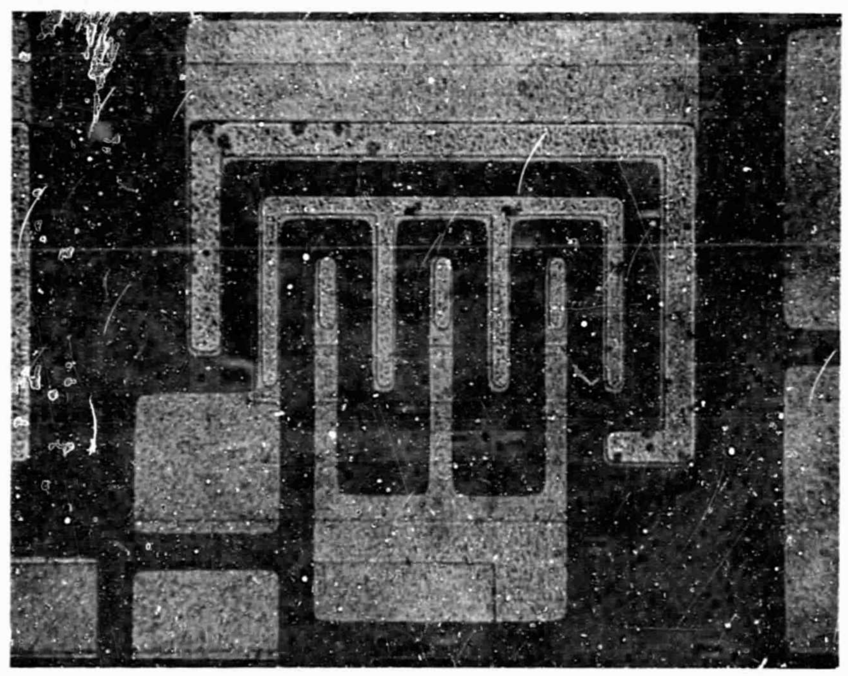

Figure 15. Lateral PNP Transistor - Three Emitters

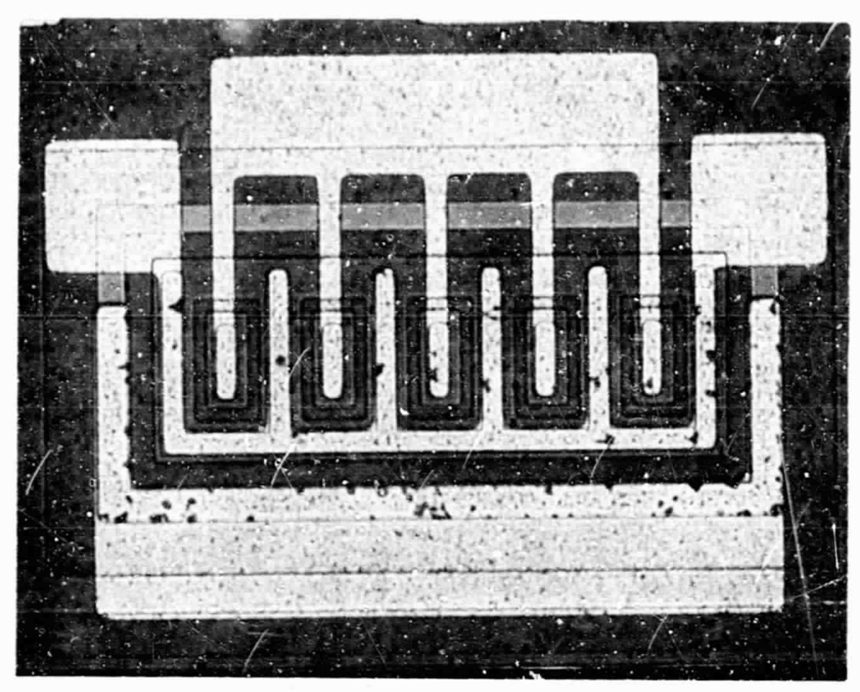

Figure 16. Lateral PNP Transistor - Five Emitters

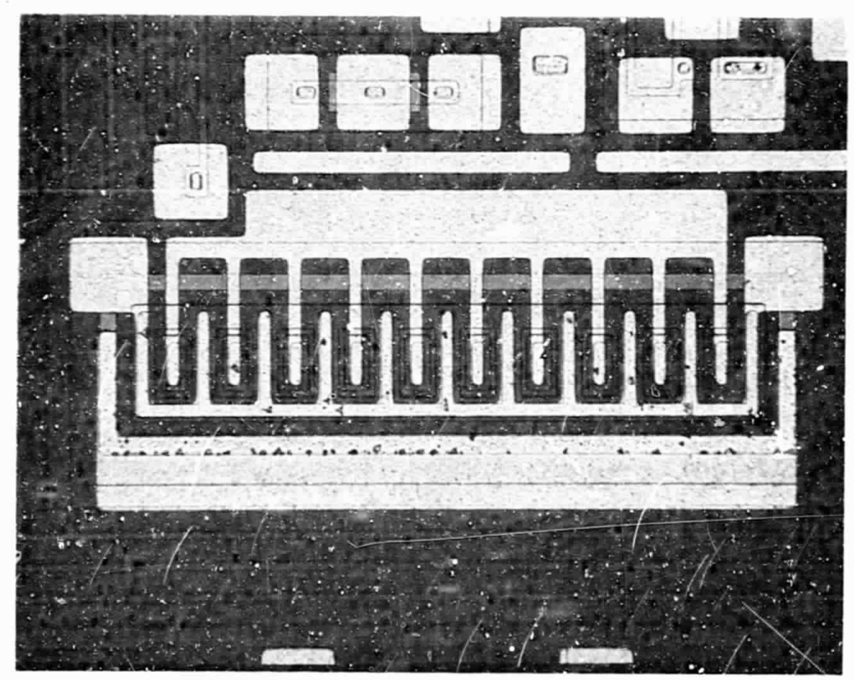

Figure 17. Lateral PNP Transistor - Ten Emitters

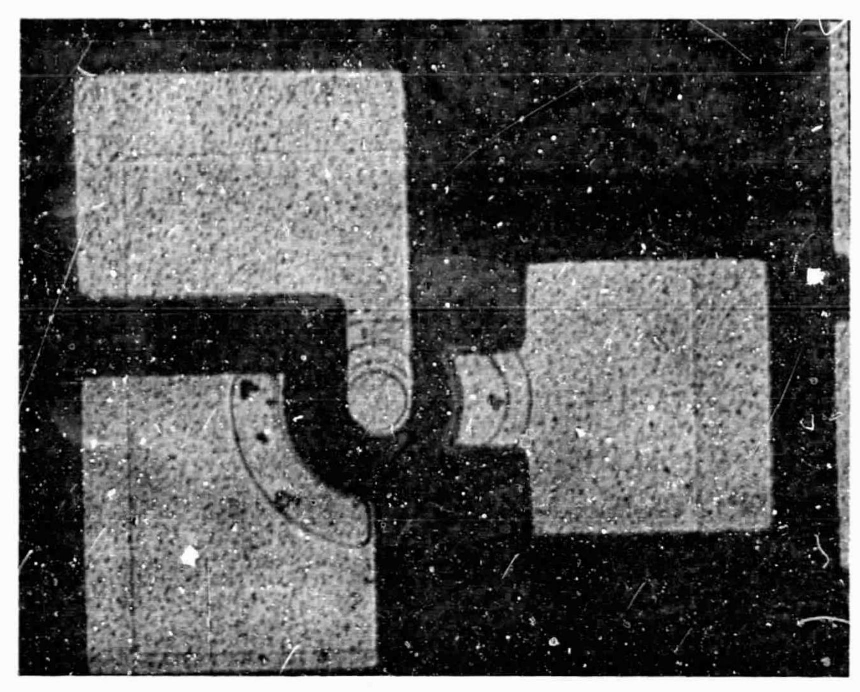

Figure 18. Micropower PNP

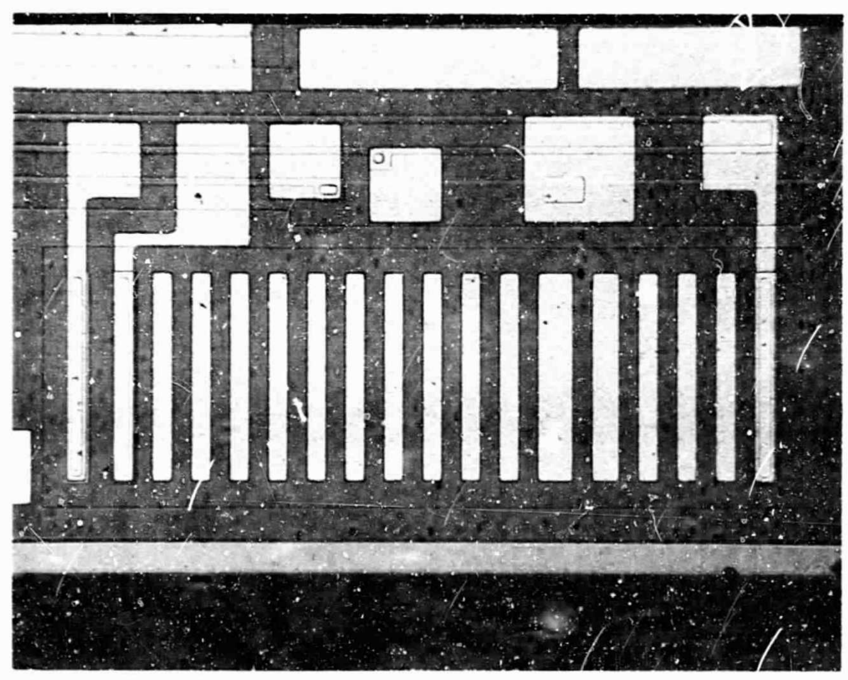

Figure 19. Multiple Gate Lateral PNP

4.2 Switching Characteristics of Lateral PNP Transistors

Lateral PNP transistors are frequently used to provide a complementary capability to reduce the standby power dissipation. In this application the PNP acts as a non-linear load resistor for the NPN transistor. The schematic circuit for testing the lateral PNP as a non-linear load resistor is shown in figure 20.

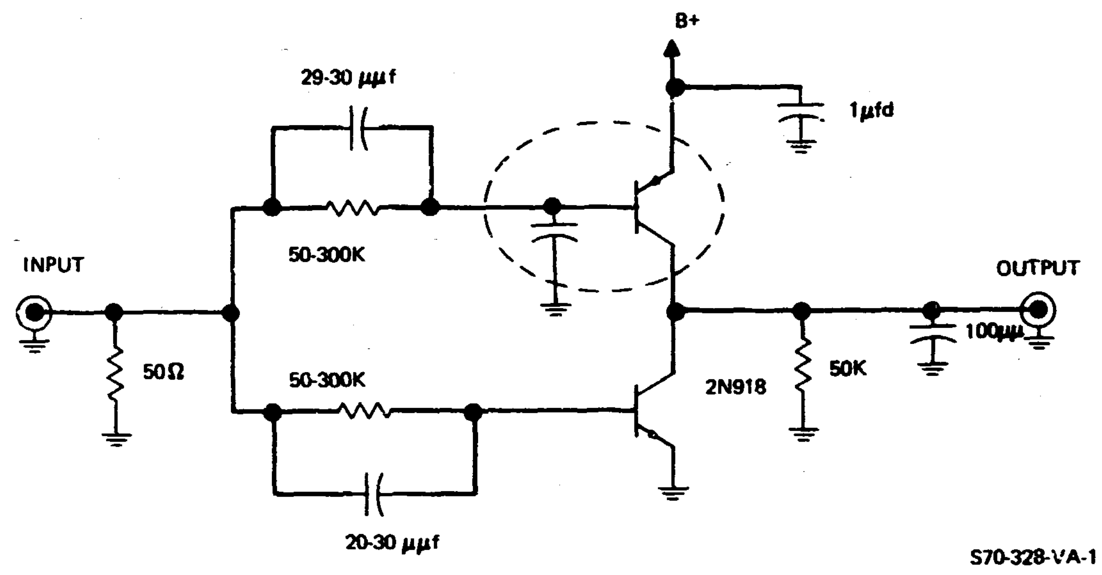

Figure 20. Test Circuit for Evaluating Switching Characteristics

The test circuit was evaluated with a commercial PNP vertical transistor to frequently greater than 10MHz before testing integrated lateral PNP transistors. To accurately simulate true I.C. operation, a four pin TO18 package was used with the substrate grounded so that the parasitic base to ground capacitance would be present. This also accounts for the parasitic PNP action to the substrate.

The test conditions for the device are listed below:

$B+ = 0.7, 1.0, 2.0, 3.0, 4.0, 5.0$ volts

$f = 10K, 30K, 100K, 300K, 1M, 3M, 10MHz$

The input and output waveforms are shown in figure 21 . The turn-on

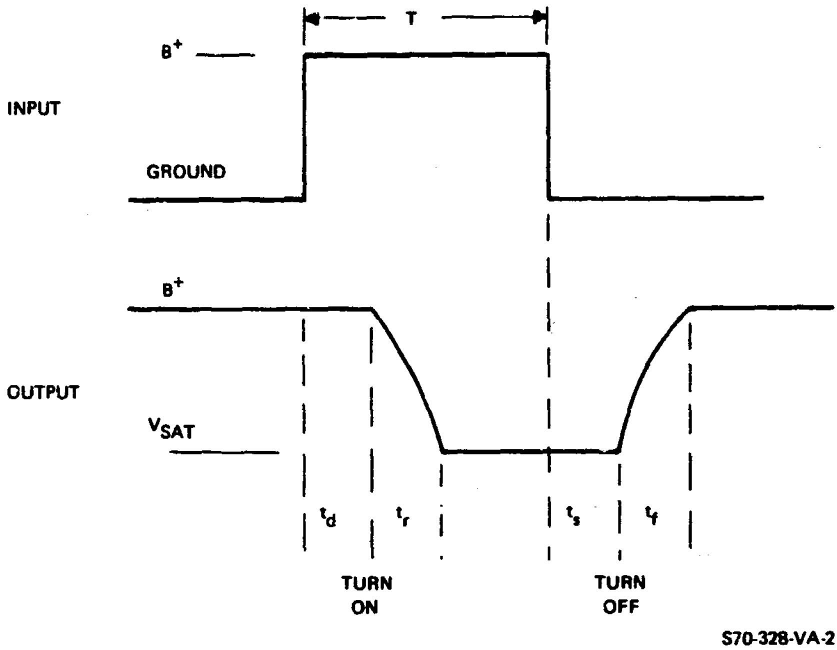

Figure 21. Switching Characteristic Waveforms

time, determined mainly by the 2N918, remained less than 100 nsec for all supply voltages and frequencies. The turn-off characteristics are used to evaluate the lateral PNP transistor. For no-lead conditions the turn-off time was less than 100 μsec for all supply voltages and frequencies. Then the transistors were evaluated driving an R-C load of 50KΩ and 100 μμfd. Results of these measurements are given in figures 22 and 23 . The measurements were made with a 1/10 duty cycle input square wave where T defines the pulse width. The 50% duty cycle is depicted in figure 22 as the diagonal line crossing the curves. With a 50% duty cycle 10MHz operation was achieved with B+ = 7.0 volts.

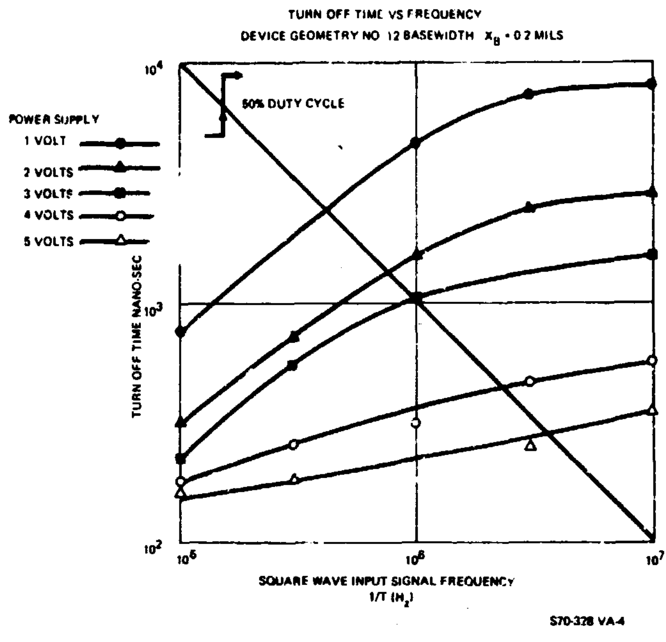

Figure 22. Turn Off Times vs Frequency

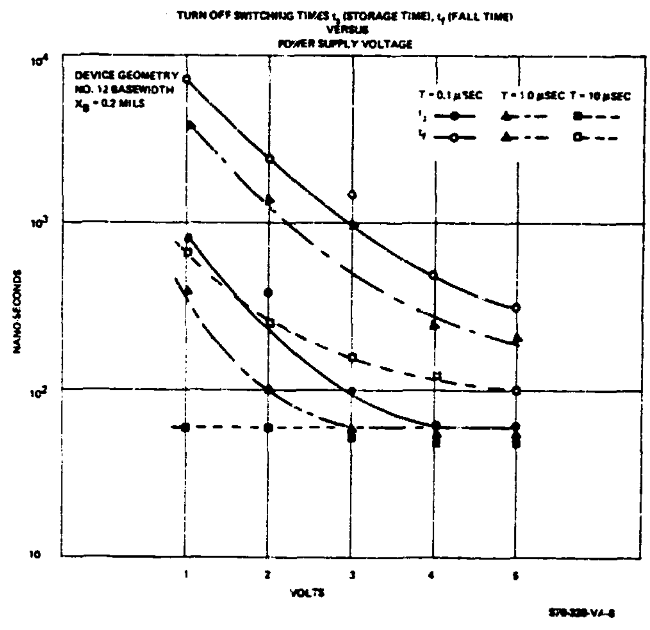

Figure 23. Turn Off Times vs Supply Voltage

The turn-off time is separated into the storage and fall times as a function of supply voltage in figure 23 . As seen, this device geometry was limited by fall-time rather than storage time. The fall-time is poor because the peak beta is achieved at lower currents than are required for optimum driving of the R-C load. As seen in figure 24 the peak current gain for this geometry device is achieved in the 0.1 - 1.0 ma range.

Since the switching speed is limited by the available current gain at current levels greater than 1 ma rather than due to capacitive effects the geometry of the lateral PNP transistor should be increased. As shown in Figure 25 the current gain vs. emitter current shifts to higher currents as more emitters are added. By adding up to tem emitters the useable lateral PNP current gain range can easily be extended into the 100-500 ma range (see figure 25). In this case the switching speed will become storage time limited. This in turn is effected by the effective lifetime in the base region. As the lifetime is decreased the current gain and the storage time are decreased.

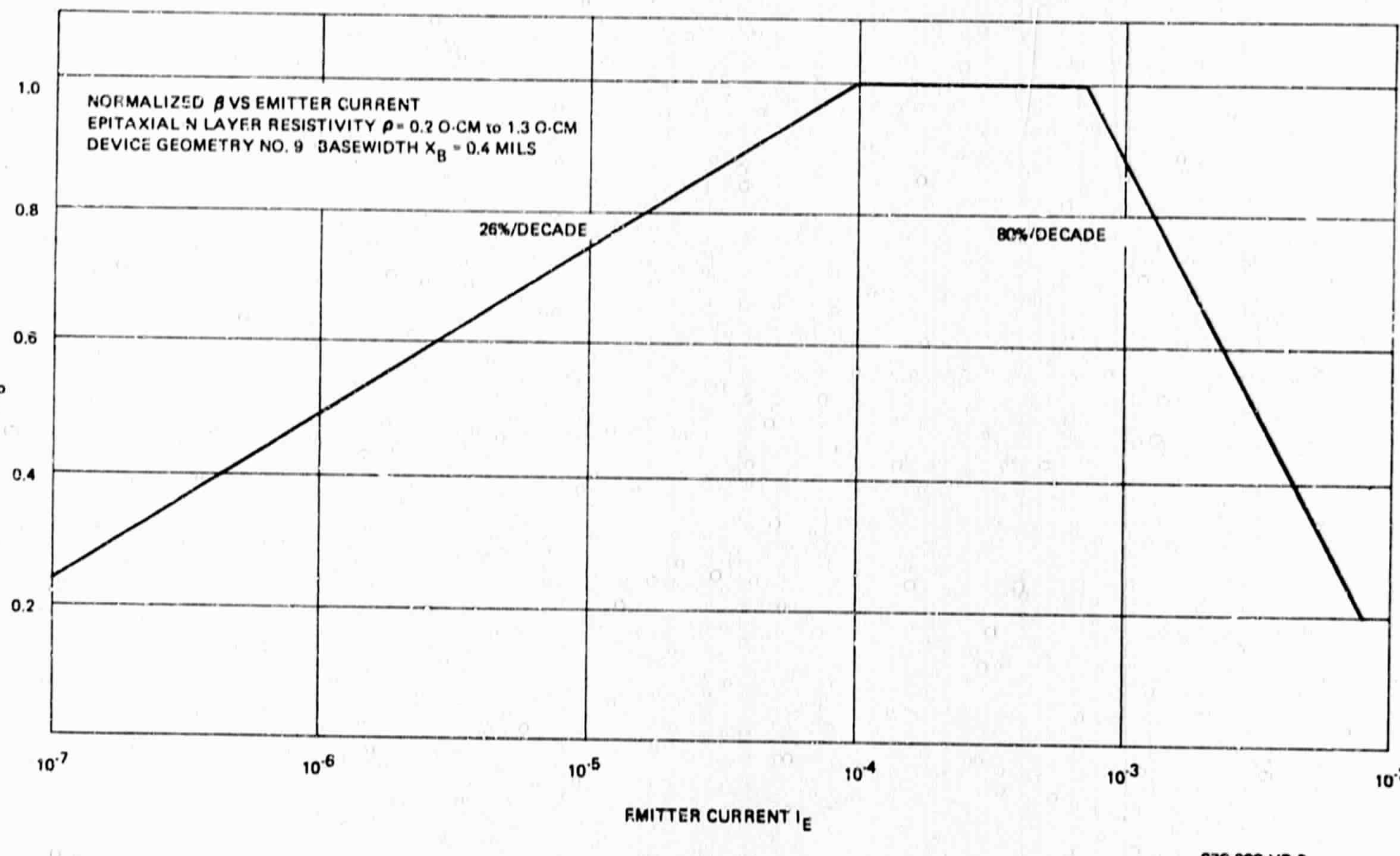

Figure 24. Typical β/β_o vs I_E

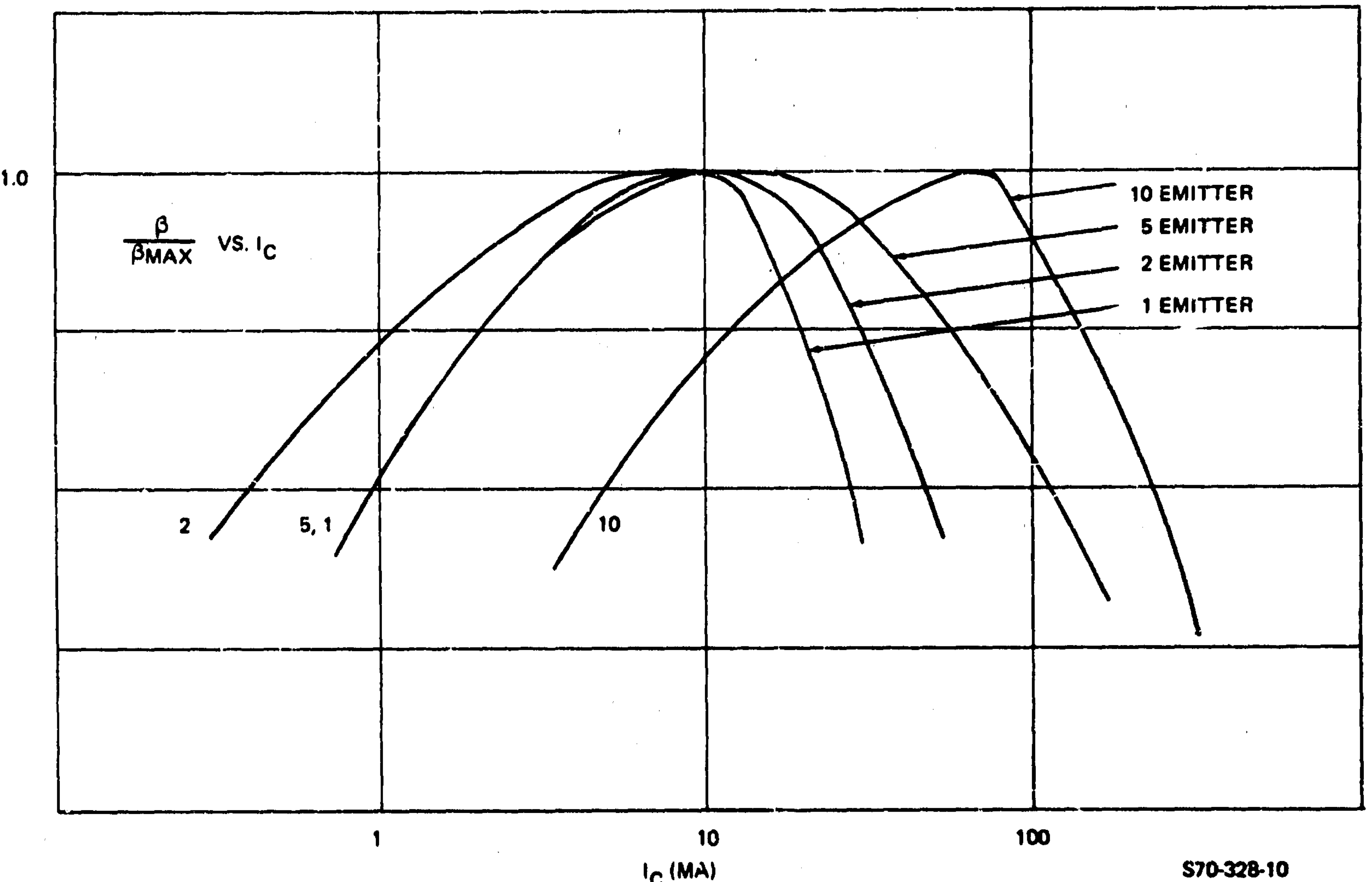

Figure 25. β/β_o for Multiple Emitter Structures

5.0 LATERAL PNP - VERTICAL NPN PROCESSING

In processing lateral PNP transistors the following areas are of particular interest:

a) Control of arsenic out-diffusion profile (N+ epitaxy or N+ pre-diffusion)

b) Control of epitaxy resistivity

c) Control of effective basewidth

d) Effect of passivation on surface

e) Effect of sintering on surface

5.1 Control of Parasitic Vertical Transistor Action

There are two ways to reduce the diffusion length of holes in the vertical direction so that they are not collected: reduce lifetime with gold doping or reduce lifetime with an N+ diffused region. Gold doping would also reduce the lateral transistor action and thus is undesirable. The N+ diffused or epitaxy region only effects the vertical action, and if the out diffusion of this region is controlled, a retarding field can also be established.

The N+ epitaxy approach is the most straight forward in that no additional process steps are required, and also no sneak paths for vertical transistor action are present. If an N+ pre-diffusion is performed, then a sneak path does exist to the substrate. Of course, the side walls of the isolation diffusion also act as collectors, but they can be located a distance greater than a diffusion length from the emitter thus minimizing their effect. If the sidewalls are a problem, then a separate N+ base diffusion guard ring completely surrounding the PNP collector and diffusing

down to the sub N+ region is required. This technique reduces the base series resistance as well.

The N+ out diffusion profile should be controlled so that the retarding field is present and so that the junction capacitance is not greatly increased. Arsenic is generally used for both the epitaxy and the diffused approach since it has a lower diffusion constant than phosphorous and the out diffusion is more controllable. The standard arsenic pre-diffusion of $\rho_s < 50$ ohms/square and $x_j = 8$ microns is well suited to lateral PNP fabrication. The epitaxial layer should then be $\rho = 1\text{-}3$ ohm-cm and the thickness depending on ρ should be 5-10 microns. The details for the N+ epitaxy are given in the attached process specification.

5.2 Control of Effective Lateral PNP Basewidth

For a vertical transistor the effective basewidth is controlled by diffusion profiles and by the relative diffusion rate of the emitter and base regions. For a lateral transistor the process is more complicated. The following factors enter into the effective basewidth of a lateral PNP transistor.

a) Basewidth on line drawing

b) Photographic & contact printing processes

c) Photoresist processing

d) Undercut in oxide etching process

e) Lateral diffusion of junction under oxide

f) Resistivity of epitaxial layer

g) Applied voltage

Of cource all of these parameters are important in NPN transistors

and diffused resistors and they must be carefully controlled; however, they do not effect so sensitive a parameter as basewidth. Fortunately the lateral transistor action is not as strongly dependent on basewidth variations as the NPN transistor and the spread of Betas obtainable is quite acceptable.

The first two processes are controlled by proper mask making techniques. In photoresist processing the thickness of the resist, the exposure time, the developing technique and the post bake time and temperature are all important. Oxide undercutting during etching will predictably reduce the basewidth as will the lateral diffusion under the oxide. The resistivity of the base region and the applied voltage determine the depletion layer spreading from the collector towards the emitter. Accounting for these various factors a 10 micron basewidth on the line drawing will result in a 1-3 micron effective basewidth. Of the above, the most difficult parameter to control is the oxide undercut, and as a result, close attention should be paid to the thoroughness of the developing, the adhesion of the resist, and the control of the oxide thickness to be etched. The etching process is very reproducible in itself.

5.2 Effects of Passivation and Sintering

As discussed in section 3.4 surface effects are important in optimizing lateral PNP transistors. For passivation, a phosphorous glass is required. This is generally covered with a neutral TEOS deposited glass to eliminate the problems of photoresist adherence and undercutting of a phosphorous doped glass. The passivations described in the attached process specification yield good NPN transistor characteristics prior to sintering, but generally the PNP current gain is poor. Sintering in Forming Gas (90% N_2 - 10% H_2) for 5-15 minutes at T = 400-500°C is required to obtain good PNP current gain.

The details of the sintering process attached are as a guide line only - experimentation is required to optimize both transistor current gains and get good ohmic contact. In many cases two sintering cycles were required before adequate gains were obtained. In general more than two sintering cycles is unwise since the NPN characteristics frequently degrade at that point.

5.4 Vertical NPN - Lateral PNP Bipolar Processing Specification

This specification describes a method for simultaneous fabrication of vertical NPN transistors, lateral PNP transistors, and resistors on a monolithic, integrated circuit. The process consists of four diffusions and six photoengraving steps.

The P+ diffusion simultaneously forms the emitter and collector regions of the lateral PNP transistor so that the basewidth is not a function of mask alignment. The P+ diffusion also forms the contact to the low value diffused resistors.

I. Material Specification

Supplier - Monsanto

Type and Resistivity - p type; 10 - 40 Ω-cm

Diameter - 1.3 inches

Thickness - 7-9 mils

Surface Preparation: mechanically - chemically polished

II. Vapor Etch and Epitaxial Deposition

Horizontal reactor tube dimensions are approximately 30 inches long and 60 mm i.d. Susceptor is a silicon-carbide-coated carbon graphite boat of dimensions 11" x 2" x ½, tilted from the horizontal by approximately 5.0°.

A. Vapor Phase Etch

Carrier Gas	H_2 @ 20 l/min
Etchant	HCl @ 105 ml/min
Temperature[1]	1225 $\pm$ 10°C
Time	3 minutes
Etch Rate	0.33 micron/min

B. Epitaxial Growth

Carrier Gas	H_2 @ 20 l/min
Silicon Source	$SiCl_4$ @ 0 $\pm$ 1°C
Source Gas	H_2 @ 1.6 l/min
Deposition Temperature	1150 $\pm$ 20°C
Growth Rate	1.0 micron/min

First Layer*

Dopent	AsH_3	Flow Rate[2]
Thickness	4.2	microns
Resistivity	0.8 $\pm$ 0.1	ohm-cm

Second Layer:

Dopant	PH_3	Flow Rate[2]
Thickness	11.8 $\pm$ 1.0	microns
Resistivity	0.9 $\pm$ 0.1	ohm-cm

Sheet Resistivity - Combined Layers 160 $\pm$ 30 ohms/square

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1 Temperatures given above are as measured on the center slice with an optical pyrometer.

2 Dopant Flow Rates must be adjusted by making individual calibration runs on each of the two layers. These numbers vary slightly from week to week.

* Alternately - arsenic diffusion step IIA with appropriate oxidation and photoengraving steps.

IIA Arsenic Prediffusion

A. Pre-diffusion cleaning (per section IIIA)

B. AsH_3 Deposition 1250°C

	Preheat	Dep	Flush	Units
Time	none	60	5	min.
Gas O_2		20	20	ml/min.
Gas N_2		2700	2700	ml/min.
Gas 1% AsH_3		750		ml/min.

C. Wafers are given a 2 min. etch in 10% HF to remove the doped glass.

D. Drive-in 1200°C

Time	16	hours
Gas O_2	1000	ml/min

Final $x_o > 5$ microns

$\rho_s < 40$ ohms/square

E. Remove all oxide prior to Epitaxial Silicon Deposition

III Oxidation

A. Pre-diffusion Cleaning:

1. 5 minutes in hot sulfuric acid @ 180 ± 10°C
2. Rinse in deionized (d.i.) water to 4.0 megohms (minimum)
3. 15 minutes in hot nitric acid @ 90 ± 10°C
4. Rinse in d.i. water to 4.0 megohms (minimum)
5. 5 minutes (minimmm) in hot d.i. water @ 90 ± 10°C
5. N_2 blow dry

Cleaning may be omitted if oxidation is done same day as epitaxial growth.

B. Oxide Growth:

Thickness	O_2	N_2	H_2	Time	Temp
6000 Å	2000ml/min (see note)	170 ml/min	4150ml/min	30 min	1200°C

The above is followed by a 5 minute flush at 1200°C in O_2 @ 1000 ml/min.

Note: The gas flows produce a steam atmosphere for oxidation.

Oxygen (O_2) bubbled through hot water is an equivalent method of producing steam for oxidation.

IV. Photoengraving

A. Isolation Diffusion Mask

B. Etch Time - 9 minutes in Buffered Etch*

Diffusion Furnace Operations: Wafers are loaded onto a room temperature boat. For drive-in and oxidation, wafers are stood up in slotted boats; for depositions, the wafers are laid flat on a solid boat inclined at approximately 5° to the horizontal. When steam is used, wafers are pushed directly into the steam flowing in the tube. Flow rates are given for a 50 to 55mm. i.d. diffusion tube.

V. Isolation Diffusion (Boron)

A. Pre-diffusion Cleaning (Section III-A)

B. B_2H_6 Deposition @ 1150°C:

---

* Formula for Buffered Etch is given at the end of this specification as Appendix A.

	Preheat	Deposition	Flush	Units
Time	5	60	1.0	min
Gas O_2	320	320	320	ml/min
Gas N_2	3340	3340	3340	ml/min
Impurity Mix		300		ml/min

Impurity Mix consists of 140 ml/min of 1% B_2H_6 plus 1000 ml/min of N_2. The excess impurity mix is exhausted.

C. Drive-In @ 1200°C

Wafers are given a 2 minute etch in 10% HF prior to drive-in to remove the doped glass, then cleaned according to Section III, Part A (3-6).

Time	10 min	24 hrs. (minimum)
Gas	steam	
Gas O_2		200 ml/min
Gas N_2		1000 ml/min

VI. Photoengraving

A. Base and Resistor Mask

B. Etch Time - 10 minutes in Buffered Etch

C. An electrical check of isolation is performed prior to the base and resistor diffusion.

VII Base and Resistor Diffusion (Boron) - Vertical NPN

A. Pre-diffusion Cleaning (Section III-A)

B. B_2H_6 Deposition @ 900°C:

	Preheat	Deposition	Flush	Units
Time	5	30	1.0	min
Gas O_2	115	115	115	ml/min
Gas N_2	4500	4500	4500	ml/min
Impurity Mix		300		ml/min

Impurity Mix consists of 158 ml/min of 1% B_2H_6 plus 1000 ml/min of N_2. The excess impurity mix is exhausted. The obtained resistivity (ρ_s) is 86 $\pm$ 2 ohms/square.

C. Wafers are given a 2 minute etch in 10% HF prior to drive-in to remove the doped glass, then cleaned according to Section III, Part A (3-6).

D. Drive-In @ 1150°C

	Oxidation	Drive-In	Units
Time	20	150	min
Gas	steam		
Gas O_2		200	ml/min
Gas N_2		1000	ml/min

Final Resistivity (ρ_s) = 390 $\pm$ 40 ohms/square

Final Oxide = 5K Å

Final Depth = 12 fringes

VIII. Photoengraving

A. P+ collector and emitter mask (for the Lateral PNP Transistor)

B. Etch Time - 9 minutes in Buffered Etch

IX. Collector and Emitter Diffusion (Boron) - Lateral PNP

A. Pre-diffusion Cleaning (Section III-A)

B. B_2H_6 Deposition @ 1150°C:

	Preheat	Deposition	Flush	Units
Time	0	10	1.0	min
Gas O_2		320	320	ml/min
Gas N_2		3340	3340	ml/min
Impurity Mix		300		ml/min

Impurity Mix consists of 158 ml/min of 1% B_2H_6 plus 1000 ml/min of N_2. The excess impurity mix is exhausted. The obtained resistivity is 6.5 ± 1 ohms/square

C. Drive-In @ 1000°C

Wafers are given a 2 minute etch in 10% HF prior to drive-in to remove the doped glass, then cleaned according to Section III, Part A (3-6).

Time	20	5	min
Gas	steam		
Gas O_2		200	ml/min
Gas N_2		1000	ml/min

Final Resistivity (ρ_s) = 10.5 ± 1.5 ohms/square

Final Oxide = 2-3K Å

Final Depth = 3 - 5 microons

X. Photoengraving

A. N+ emitter and collector contact mask (for NPN transistor)

B. Etch Time - 13 minutes in Buffered Etch

XI. Emitter Diffusion (Phorphorous) - Vertical NPN

A. Pre-diffusion Cleaning (Section III-A)

B. PH_3 Deposition @ 1000°C:

	Preheat	Deposition	Flush	Units
Time	5	10-20*	0.5	min
Gas O_2	200	200	200	ml/min
Gas N_2	2000	2000	2000	ml/min
Impurity Gas - 1%		720		ml/min

C. Wafers are given a 2 minute etch in 10% HF to remove a phosphorous-doped glass, then cleaned according to Section III, Part A (3-6). The obtained resistivity is 2.5 ± 1 ohms/square.

D. Drive-In @ 1000°C:

Time	30	10	2	20	min
Gas O_2	steam	1000			ml/min
Gas N_2			1000	360	ml/min
Gas H_2				880	ml/min

E. TEOS Passivation

Temperature	600	600	600	950	600	600	600	°C
Time	5	15	5	10	5	15	5	min
Gas O_2	4000	4000	4000	see note	4000	4000	4000	ml/min
Gas O_2 thru Saturator		1				1		ml/min

Note: For the 950°C operation, the standard deposition flows for the PH_3 furnace are used. The total thickness of the phorphorous-doped TEOS is approximately 3.2K Å, with the phosphorous being sandwiched between two neutral TEOS layers (Refer to XI-B).

XII. Photoengraving

A. Contact window mask

* Actual deposition time depends on x_j and ρ_s of base.

B. Etch Time - 6 minutes in Buffered Etch

XIII. Aluminum Deposition

A. Pre-diffusion Cleaning (Section III-A)

B. Electron beam evaporation with 8-10K Å of aluminum deposited.

XIV. Photoengraving

A. Aluminum bonding pad mask

B. Etch Time - 30 seconds in Aluminum Etch*

XV. Sintering

A. Sintered at 500°C for approximately 10-15 minutes. (See Figure 26)

B. Examine visually to confirm good Al-Si contact

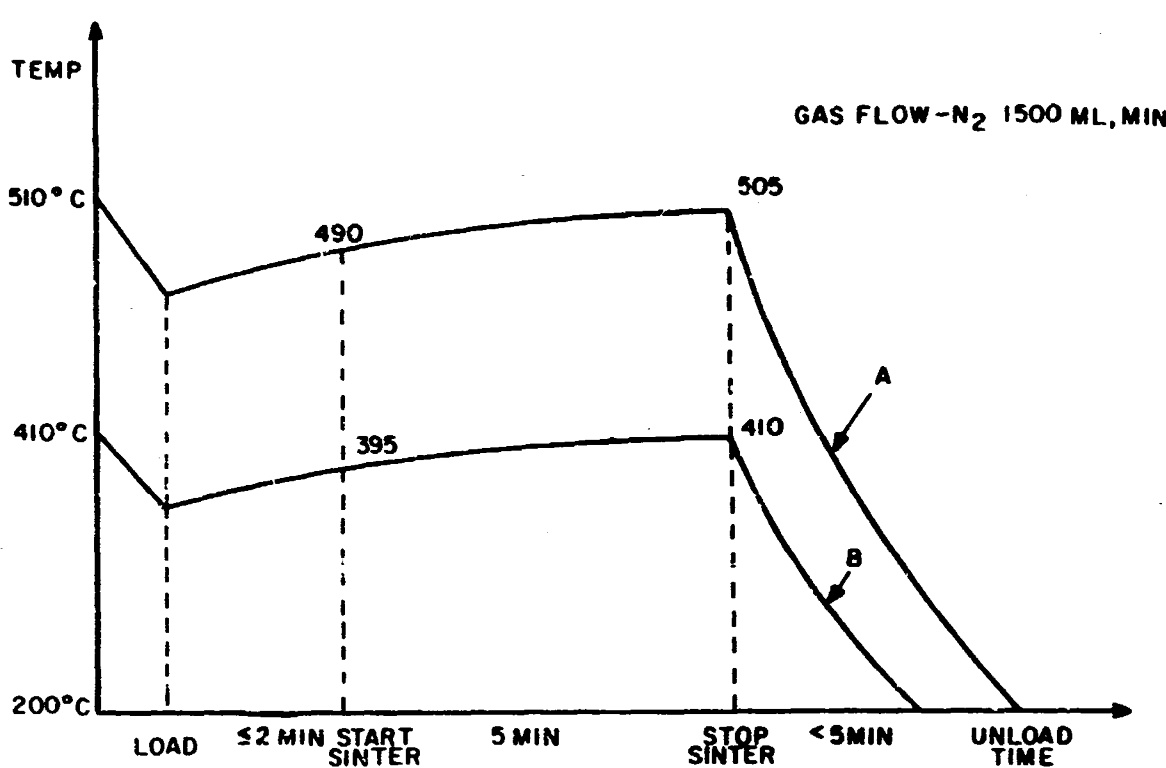
XVI. Electrical, Scribe, Dice and Visual Inspection

Standard measurements on each of the components are made on all wafers to insure the quality. Then the wafer is scribed and diced into the separate chips. Visual inspection can be performed at this point, although it is more effectively done prior to dicing if an automatic marking scheme is available.

* Aluminum Etch formula is included in Appendix B

Temperature versus Time

Hydrogen (H_2) Gas Flow - 150 ml/min



CURVE A: THIS CURVE DEPICTS THE SINTERING CYCLE FOR ALUMINUM THAT HAS NOT RECEIVED AN HF ACID DIP

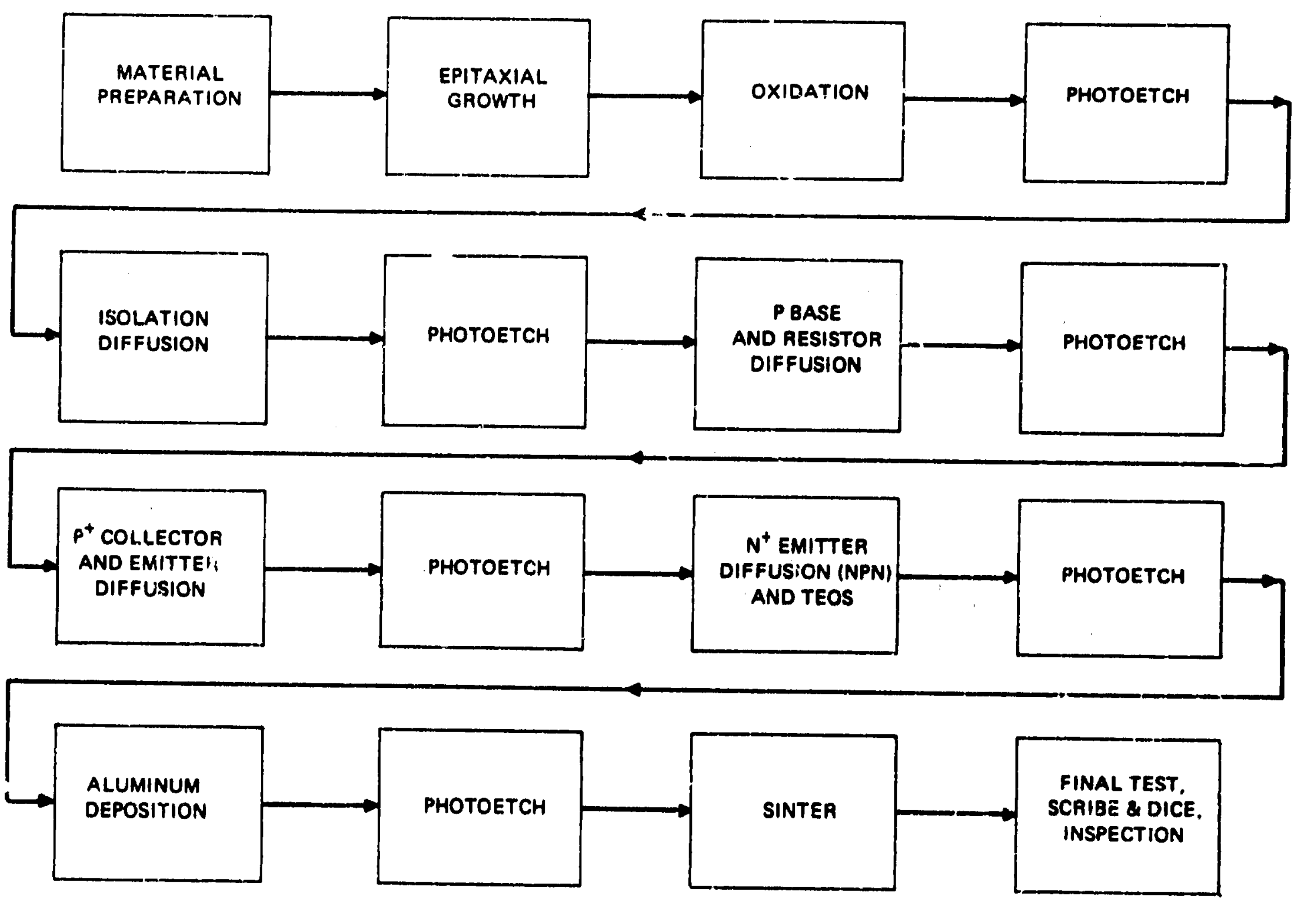
CURVE B: THIS CURVE DEPICTS THE SINTERING CYCLE FOR ALUMINUM THAT HAS RECEIVED AN HF ACID DIP

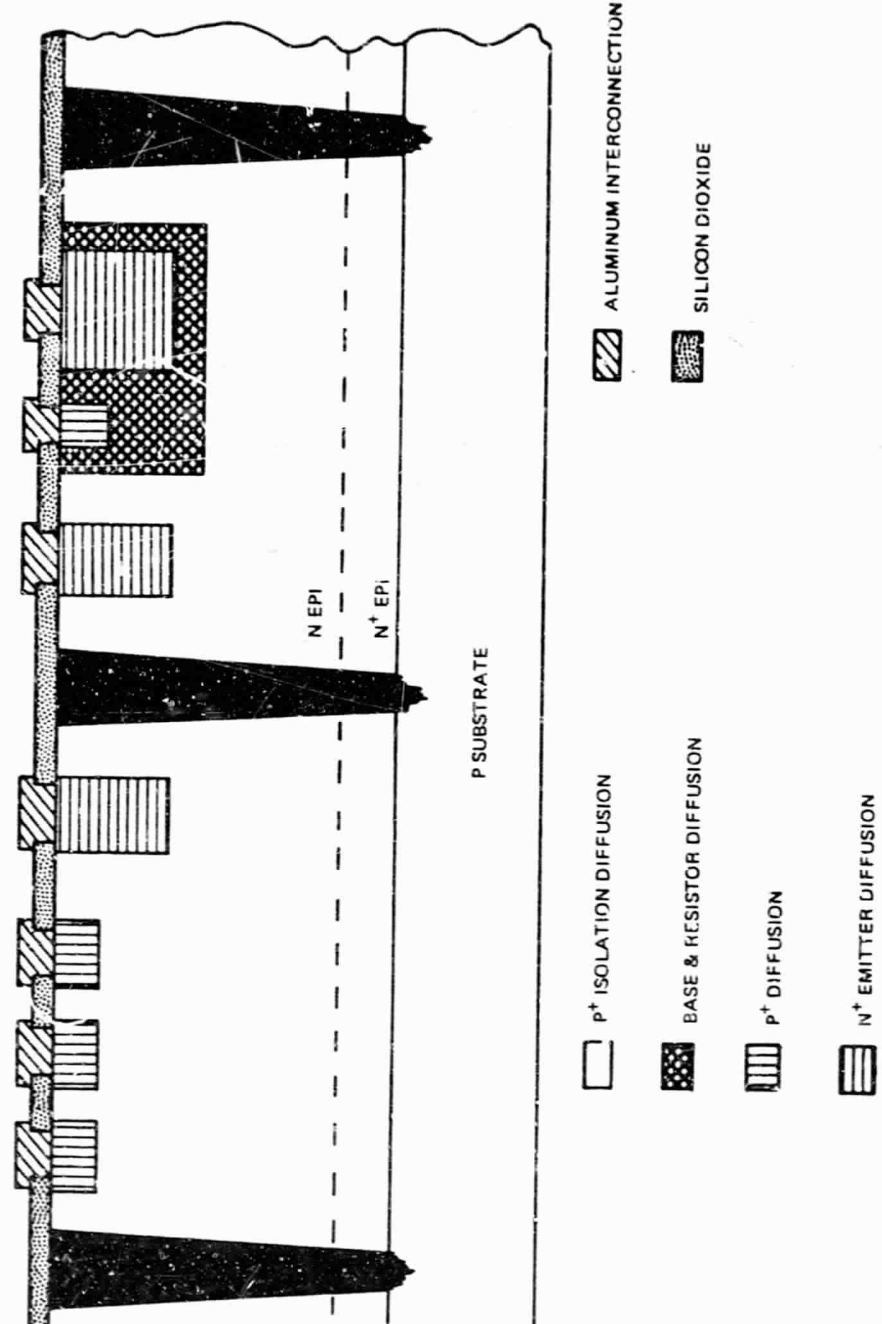
S70-164-V8-1

Figure 26 Sintering Process

Curve A: This curve depicts the sintering cycle for aluminum that has not received an HF acid dip.

Curve B: This curve depicts the sintering cycle for aluminum that has received an HF acid dip.


MATERIAL PREPARATION
EPITAXIAL GROWTH
OXIDATION
PHOTOETCH
ISOLATION DIFFUSION
PHOTOETCH
P BASE AND RESISTOR DIFFUSION
PHOTOETCH
P^+ COLLECTOR AND EMITTER DIFFUSION
PHOTOETCH
N^+ EMITTER DIFFUSION (NPN) AND TEOS
PHOTOETCH
ALUMINUM DEPOSITION
PHOTOETCH
SINTER
FINAL TEST, SCRIBE & DICE, INSPECTION
S70-328-VA-12


N EPI
N^+ EPI
P SUBSTRATE
P^+ ISOLATION DIFFUSION
BASE & RESISTOR DIFFUSION
P^+ DIFFUSION
N^+ EMITTER DIFFUSION
ALUMINUM INTERCONNECTION
SILICON DIOXIDE
370-328-VA-13

APPENDIX A

Buffered Etch

Stock solution = 1 lb. - NH_4F + 1000cc d.i. water

Etch is made fresh each day as follows: 10 parts stock solution to 1 part concentrated HF. (48%)

Etch rate = 750 Å/min (undoped SiO_2)

Etch temp = 25°C

APPENDIX B

Acid Etch for Aluminum

300cc H_3PO_4 (85%) + 12cc Concentrated HNO_3 + 60cc Glacial HAc

Etch temp = 60°C

Etch rate = 10,000 Å/min