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A STUDY OF MICROMINIATURIZED DEVICES FOR BIOASTRONAUTICAL MONITORING OR ANALYSIS

by

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I. Introduction

Since the last report progress has been made in the areas of active filter synthesis using RC distributed networks, d-c to d-c converters, digital filters and measurement techniques using pulsed solid-state light diodes.

Mr. Hooshang Mahdi has completed the theoretical aspects of his Ph. D. dissertation concerned with $\overline{URC}$ and $\overline{ERC}$ networks and their use in active filter circuit synthesis.

D-c to d-c converters have been developed that are capable of operating at voltages less than 1.35 volts and having dual polarity outputs using only a single polarity input.

A successful analogue digital synthesis of a third degree Butterworth filter has been realized. In order to make the circuit more suitable to monolithic integrated-circuit techniques a novel approach utilizing deficit charging and capacitance amplification is currently under development.

An analysis of the pulsed light diode method of measurement has made it possible to be more definitive in specifying the desired characteristics for the light emitting diodes.

II. Active Circuit Synthesis

Mr. Hooshang Mahdi has completed the theoretical aspects of his Ph.D. dissertation concerned with the synthesis of active distributed RC circuits using uniform distributed RC networks ($\overline{URC}$) and exponentially distributed RC networks ($\overline{ERC}$). This dissertation has considered the problem of approximating the magnitude response of various bi-quadratic functions using active $\overline{URC}$ or $\overline{ERC}$ synthesis. The synthesis procedures may be considered as p-plane synthesis with the distributed networks constituting the p elements as contrasted with lumped inductances and capacitances of s elements.

In general the p-plane, s-plane transformation is defined as

$$p \overset{\Delta}{=} [\cosh \sqrt{(\alpha d/2)^2 + sT_0} + \frac{\alpha d}{2\sqrt{(\alpha d/2)^2 + sT_0}} \sinh \sqrt{(\alpha d/2)^2 + sT_0}] \, e^{-\frac{\alpha d}{2}} \quad (1\text{-}1)$$

where p = the inverse voltage transfer function of an $\overline{ERC}$ network

αd = tapering factor = 0 for the uniform network

T_0 = untapered distributed network time constant.

Since infinitely many s-plane points will yield the same p-plane point through equation (1-1), p-plane synthesis is only useful for approximating the magnitude response for given s-plane specifications. Initial attention is given to these specifications followed by a study of the phase, transient response and Q sensitivity for various circuit configurations using combinations of distributed networks and voltage controlled voltage sources.

The p-plane synthesis is broken into two parts. The first part examines the s-plane characteristics of a p-plane polynomial given by

$$p + M = 0 \quad\quad\quad (1\text{-}2)$$

where M is a constant realized by the gain of a voltage controlled voltage source. This procedure amounts to synthesis on the real axis of the p-plane where p is defined by equation (1-1).

It has been found that this method of realization provides an excess phase resulting from the presence of the non-dominant s-plane roots of equation (1-2). The excess phase increases with increasing tapering factor and remains approximately a linear function of frequency well beyond the frequency range of interest

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determined by the dominant roots of equation (1-2). This characteristic tends to minimize the group delay fluctuations of all-pole transfer functions realized by this technique. It also allows an approximation of p+M by its dominant roots times a phase factor in the form

$$p + M = (s^2 + 2\cos\gamma \, s + 1) \, e^{\tau s} \tag{1-3}$$

where τ is the excess group delay. Specifications of the group delay fluctuations can be used as a design criterion for selection of the tapering factor αd. In synthesizing bi-quadratic factors the excess group delay may be eliminated by properly choosing the tapering factors of the distributed networks for the two sections in cascade.

In general, increasing the tapering factor for all-pole transfer functions results in improved phase linearity, lower required gain and lower Q sensitivity to changes in gain. The latter improvement tends to be negated by a rapidly increasing Q sensitivity to the tapering factor for increases in αd. The former improvements are obtained at the expense of higher time constant requirements and the loss of zero Q sensitivity to passive elements, a unique characteristic for $\overline{URC}$ networks.

The second part covers procedures for the realization of s-plane magnitude specifications through p-plane polynomials given by

$$p^2 + M_2 p + M_1 = 0 \tag{1-4}$$

where M_1 and M_2 are constants and $M_2^{\,2} < 4M_1$. These procedures are synthesis off the real axis of the p-plane.

For a given p, a specific tapering factor, the effect of the non-dominant s-plane roots of equation (1-4) on the magnitude response can be minimized by adjustment of M_1 and M_2. As for the case of equation (1-2) excess phase results from the presence of the non-dominant roots of equation (1-4). This excess phase is controllable by selecting different s-plane to p-plane mapping radii which in turn leads to different time constant requirements for the distributed networks used in the synthesis.

Similar to the realization by means of p+M the excess phase is a linear function of frequency within the pass band for all tapering factors and mapping radii. This characteristic tends to linearize the phase response and allow an

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approximation of equation (1-4) by its dominant roots times a phase factor
in the form

$$p^2 + M_2 p + M_1 = (s^2 + 2\cos\gamma\, s + 1)\, e^{\tau s} \tag{1-5}$$

where τ is the excess group delay.

In general the p-plane polynomials given in equations (1-2) and (1-4) have
s-plane roots which are given by

$$\prod_{n=0}^{\pi} [(s + \alpha_n)^2 + \beta_n^{\,2}] = 0 \tag{1-6}$$

where α_0 and β_0 are the real and imaginary parts respectively of the dominant
roots. For a given p, i.e. specifying αd in equation (1-1), the s-plane realiza-
tion is achieved by properly setting the dominant roots of equation (1-6) in the
desired location of the s-plane. This is done by properly selecting T_0 in
equation (1-1) and the coefficients M, M_1 and M_2 in equations (1-2) and (1-4).
The p-plane realizations are then achieved using circuit configurations which
are capable of producing p-plane polynomials.

The circuit configurations for low-pass voltage transfer functions based
upon equation (1-4) require twice as many voltage controlled voltage sources
and distributed networks as those configurations based upon equation (1-2).
The disadvantage of larger numbers of elements is more than compensated
by the greatly improved Q sensitivity to changed in gain and a drastic reduction
in the required time constant T_0.

The circuit configurations useful for the p-plane polynomials of equation
(1-4) are shown in Figure 1. The $\overline{\text{ERC}}$ networks are identical. Using this
nested configuration with identical $\overline{\text{URC}}$ networks for a second order Butterworth
function having an $\omega_{3dB} = 1$ rad/sec a reduction of an order of magnitude of T_0 can be
obtained over that necessary for the first order circuit of Figure 1. Further
reduction in the magnitude of the required value of T_0 can be obtained using
identical $\overline{\text{ERC}}$ networks with negative tapers. For example, the second order
Butterworth function mentioned above can be realized using two identical $\overline{\text{ERC}}$
networks with $\alpha d = -2$ and $T_0 = .005$ seconds. Using $\overline{\text{URC}}$ networks rather than
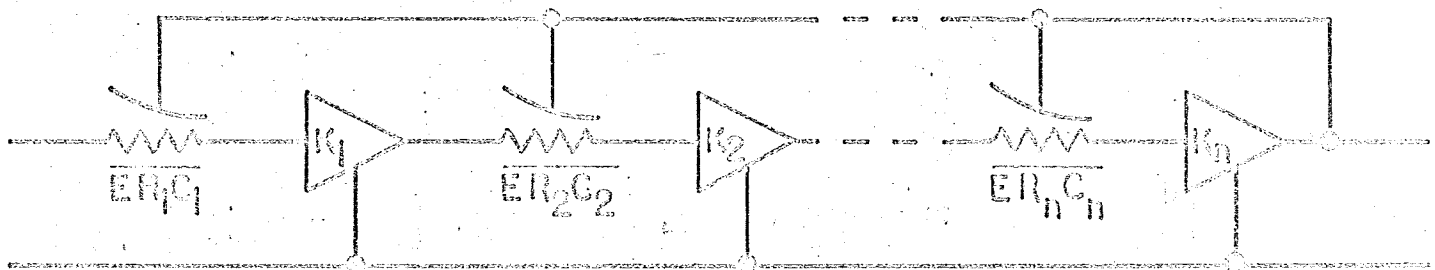the $\overline{\text{ERC}}$ networks, the required value of T_0 is 1 second.
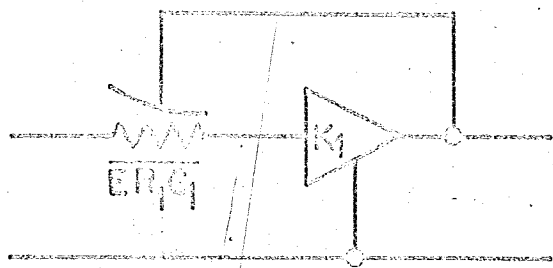
1ST ORDER

1(a)
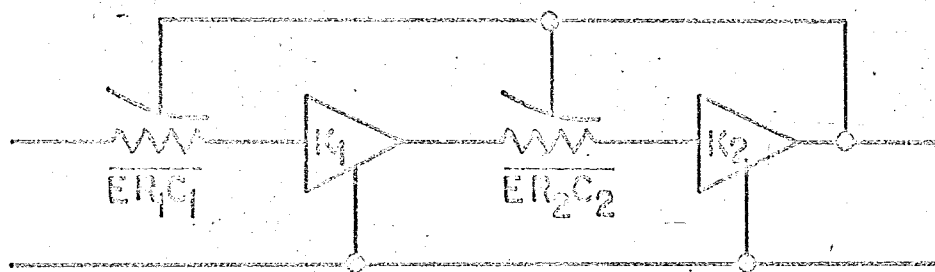
2ND ORDER

1(b)

nTH ORDER

1(c)

Figure 1. Circuit configurations useful for $p + M$ and $p^2 + M_2 p + M_1$ p-plane synthesis, (a) $p + M$ (b) and (c) $p^2 + M_2 p + M_1$ (b) 2nd order (c) nth order.

A significant advantage of the synthesis techniques developed from equation (1-4) is the use of identical networks in the nested configuration which allows the capacitive terminals of all the networks to be put at the same potential. This feature should be attractive from the viewpoint of fabrication of active $\overline{URC}$ and $\overline{ERC}$ circuits by monolithic and thin-film techniques.

The details of the theoretical work of this dissertation have been published in two papers and a presentation at the IEEE International Symposium on Circuit Theory, San Francisco, California in December of 1969. Two other papers have been submitted for publication. Titles and details are listed below.

Publications

H. Mahdi, "On the Synthesis of Active Distributed RC Circuits." It has been accepted for publication in the IEEE Transactions on Circuit Theory, Vol. CT-17, May 1970.

H. Mahdi, "Synthesis of Low-Pass Linear Phase Active Circuits Using Distributed RC Networks." It has been accepted for publication in the IEEE Transactions on Circuit Theory, Vol. CT-17, August 1970, and was presented at the IEEE International Symposium on Circuit Theory, San Francisco, Dec., 1969.

H. Mahdi, "Synthesis of Active Distributed RC Circuits Using Uniform and Exponentially Distributed RC Networks." This has been submitted for possible publication in the IEEE Transactions on Circuit Theory.

H. Mahdi, "Synthesis of Low-Pass Linear Phase Active Circuits Using Identical $\overline{ERC}$ or $\overline{URC}$ Networks." This has been submitted for possible publication in the IEEE Transactions on Circuit Theory, and for possible presentation at the 1970 IEEE International Symposium on Circuit Theory.

The final phase of this thesis will be experimental verification of the theoretical results. Attempts are being made by Dr. Nowak to fabricate $\overline{URC}$ and $\overline{ERC}$ networks with time constants useful for low-frequency low-pass filters. A second source outside the University is also being investigated. It is anticipated that the experimental work will be completed and the final form of the manuscript submitted by the first of June.

III. D-c to D-c Converters

Work on the d-c to d-c converters has continued with significant improvements. The clock circuit of Figure 2 has been re-designed so that it can now work on voltages smaller than that available from single mercury cells, or 1.35 volts. Prototype doublers and triplers have been developed which have dual polarity outputs.

In considering the future availability of nuclear sources having terminal voltages of 0.4 volts it became necessary to re-design the clock circuit utilizing germanium transistors with their lower junction voltages. The clock circuit is shown in Figure 3. There is no fundamental difference between this clock circuit and that of Figure 2. The polarities used are necessary if the clock is to be used for a negative output doubler. Operation is possible from supply voltages as low as 0.1 volts. With V_i = 0.3 volts and the rise and fall times of the output square wave are both 0.8 microseconds with an input current of 0.31 ma.

A complete four stage multiplier circuit using the clock circuit of Figure 3 and giving a negative output voltage is shown in Figure 4. The characteristics for this circuit are shown in Table I. With V_i = 0.4 volts and an input current of 1.1 ma, the output voltage is -1.29 volts. This circuit, when used with a 0.4 volt nuclear power source, would become an equivalent mercury cell with a rating of ma-years rather than ma-hours.

An extension of these ideas makes possible converters with dual polarity output voltages with only a single polarity input voltage. A dual polarity tripler circuit is shown in Figure 5. The block labeled clock is the clock circuit of Figure 2. Q_1, Q_2 and Q_3 make up the positive output tripler circuit giving an output voltage of 3.6 volts. Assuming negligible values for V_{CE}(sat), C_4 is charged to 3.6 volts through Q_4 and Q_6, since with E_s = 0, Q_7 will bias Q_6 into saturation. With E_s > 0 and positive Q_4, Q_6 and Q_7 are open and Q_5 is in saturation. Q_5 in saturation grounds the positively charged side of C_4 which effectively shunts the collector of Q_8 and the base of Q_9 with -3.6 volts. Q_8 is biased into saturation by Q_9 and C_5 charges to -3.6 volts.

Attentions is now being given to miniaturizing the circuits using hybrid techniques. Prototypes should be available in the near future.

Some of the details of this work has been published in Electronics Design Vol. 18, No. 4, 15 February 1970.
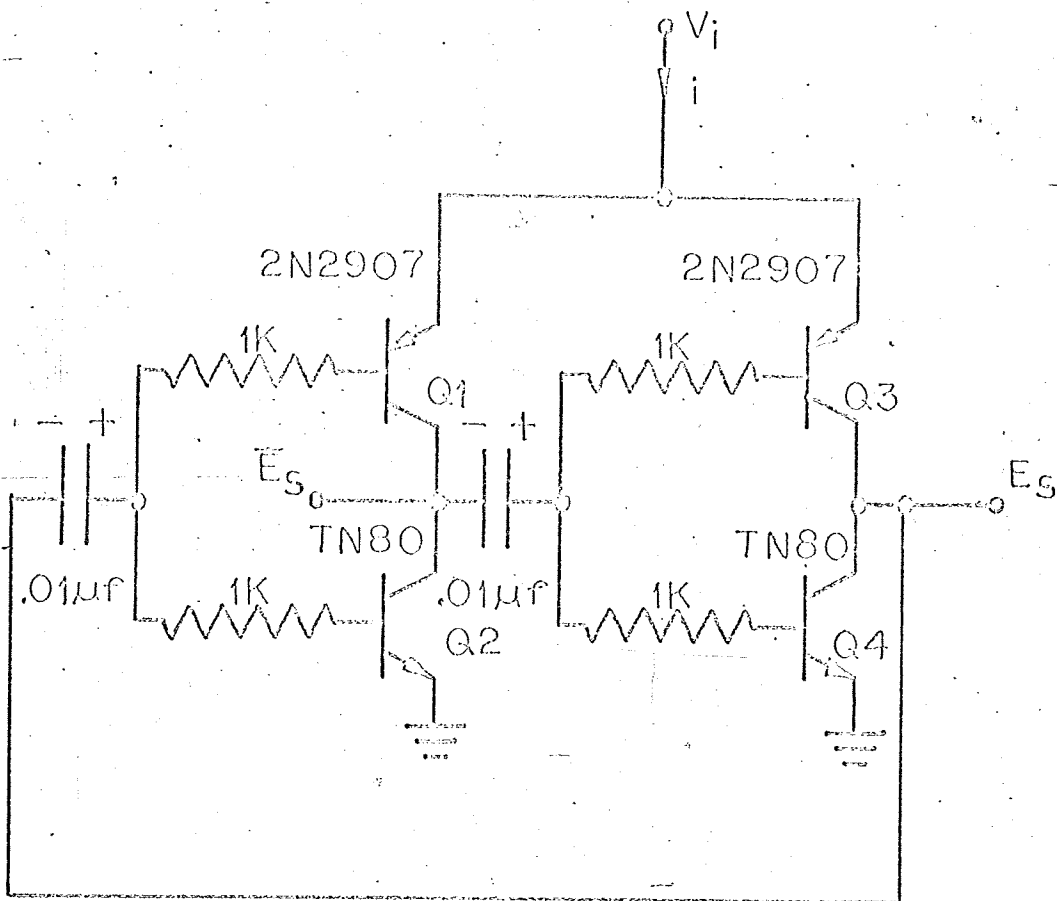
Figure 2a. Voltage doubler clock circuit.

Input Voltage (volts)	Input Current (ma)	Rise Time (ns)	Fall Time (ns)
1.25	.5	50	20
1.35	1.0	30	20
1.45	1.7	30	.20

Figure 2b. Characteristics of clock circuit of Figure 2a.

Figure 2. Voltage doubler clock circuit and its characteristics,
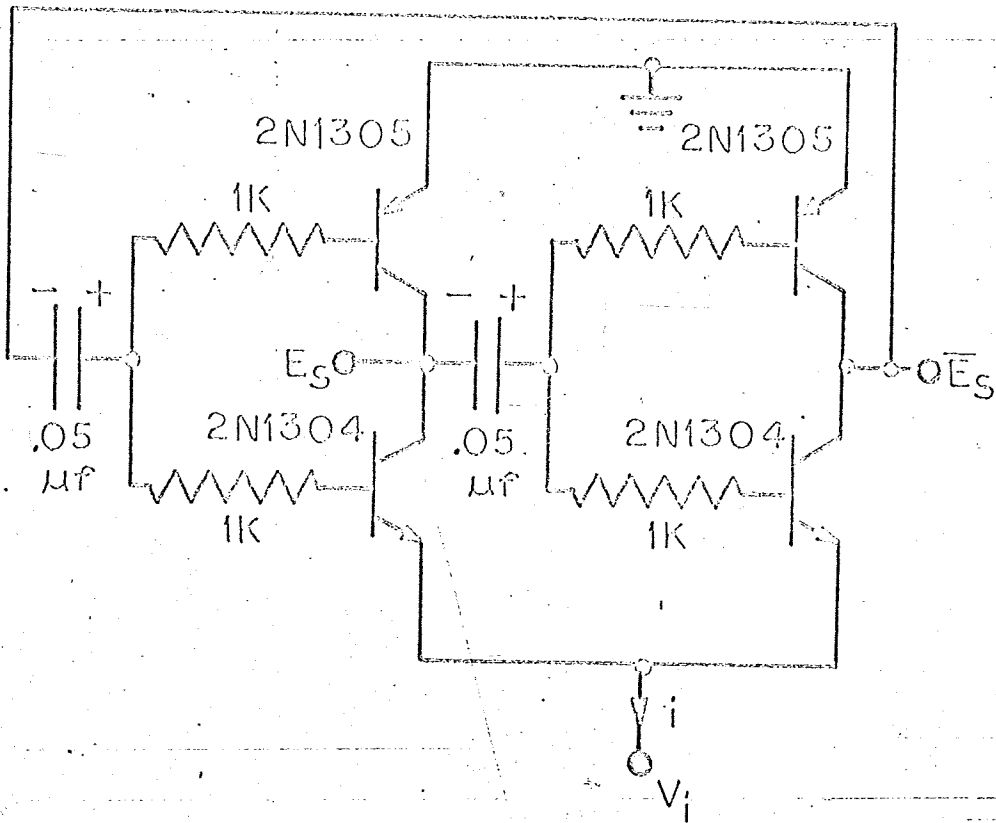(a) circuit (b) characteristics.

Figure 3. Clock circuit capable of operation with
supply voltage as low as 0.1 volts.

Table I. Four stage voltage multiplying
          circuit characteristics for the
          circuit of Figure 4.

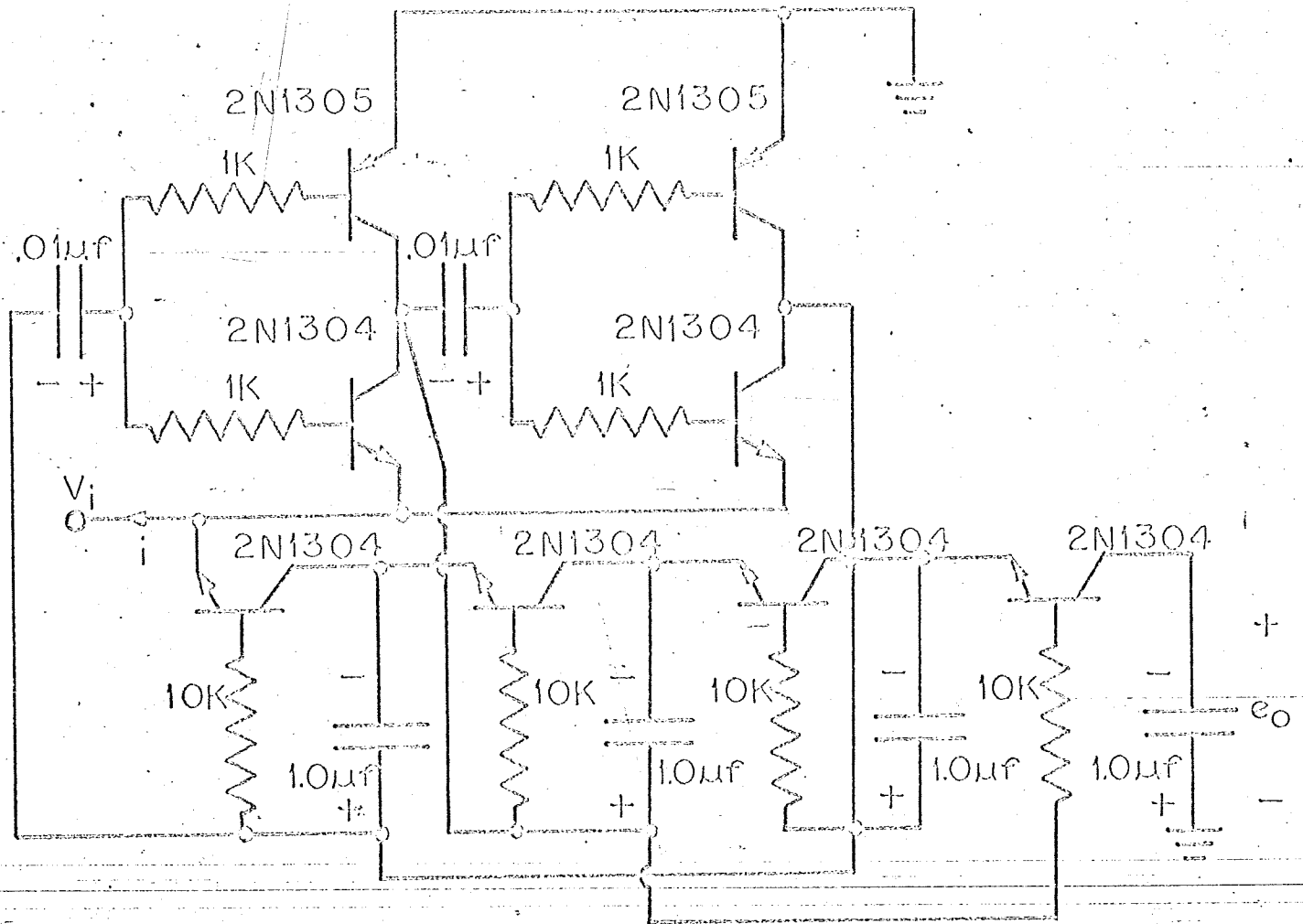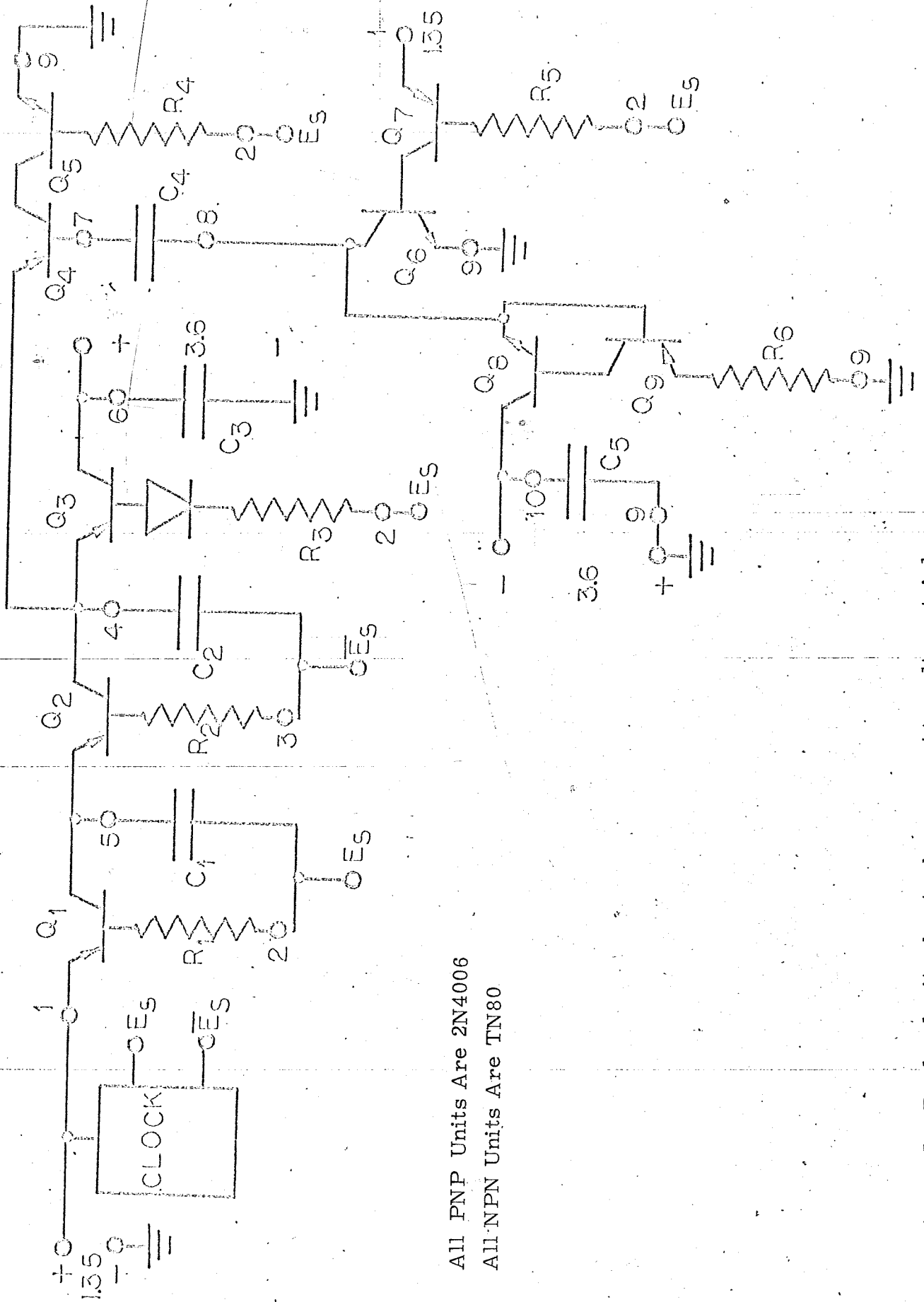| Input Voltage (volts)	Input Current (ma)	Output Voltage (volts)
-0.200	.23	-0.520
-0.300	.54	-0.910
-0.400	1.10	-1.290
-0.500	2.30	-1.665

Figure 4. Four stage voltage multiplying circuits capable
of operating from supply voltages of less than 0.4 volts.

All PNP Units Are 2N4006

All NPN Units Are TN80

Figure 5. Dual polarity d-c to d-c converter voltage tripler.

IV. Digital Filters

Report No. 3 carried the development of the first degree Butterworth filter utilizing analogue-digital techniques through to its completion. Since that time a similar development was carried out for second and third degree Butterworth types. The first degree Butterworth is a trivial case since it can be obtained more readily with a simple RC circuit. The second degree filter, on the other hand, requires a pair of complex poles and thus an active filter approach is required if inductors are not to be utilized. The third-degree filter was accordingly synthesized by following a simple first-degree RC circuit with a second degree filter of the analogue-digital design.

The resulting circuit is shown in Figure 6 and consists of an RC circuit followed by the second degree digital filter. The second degree filter itself follows directly from the synthesis techniques of Section VI of Report No. 2. The clock is also shown in the circuit schematic although it should not rightly be considered part of the filter proper. Figure 7 shows the response of this circuit when a cut-off frequency of 1 Hz and sampling-clock frequency of 100 Hz are employed. The entire circuit was constructed on a 3 1/4 by 2 1/4 inch printed circuit board.

When discrete components are employed, as indicated in Figure 6 , this type of approach doesn't readily show an advantage over a conventional active filter. Advantage will only be realized if an integrated circuit approach is followed. With this end in mind the storage-capacitor, isolation-amplifier portions of the second degree filter leave much to be desired. However, once it is recognized that this portion of the circuit is essentially a bucket-brigade type of delay line, the approach[*] utilized recently by the Philips Research Laboratories of Eindoven, The Netherlands, can be used to achieve a substantial size reduction with an integrated circuit approach. The approach in question utilizes the principle deficit charging and is illustrated in Figure 8 .

The circuit shown is included here to illustrate the concept involved. It consists of an isolation emitter follower, a sampling gate and two stages of bucket delay. The capacitance sizes illustrated are chosen to work with the discrete transistors employed. In any final integrated circuit instrumentation the values would be different and realized by the monolithic techniques discussed

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[*] F.L.J. Sangster, "Integrated MOS and Bipolar Analog Delay Lines using Bucket-Brigade Capacitor Storage," 1970 IEEE Solid-State Circuits Conference, University of Pennsylvania, February 18-20, 1970.
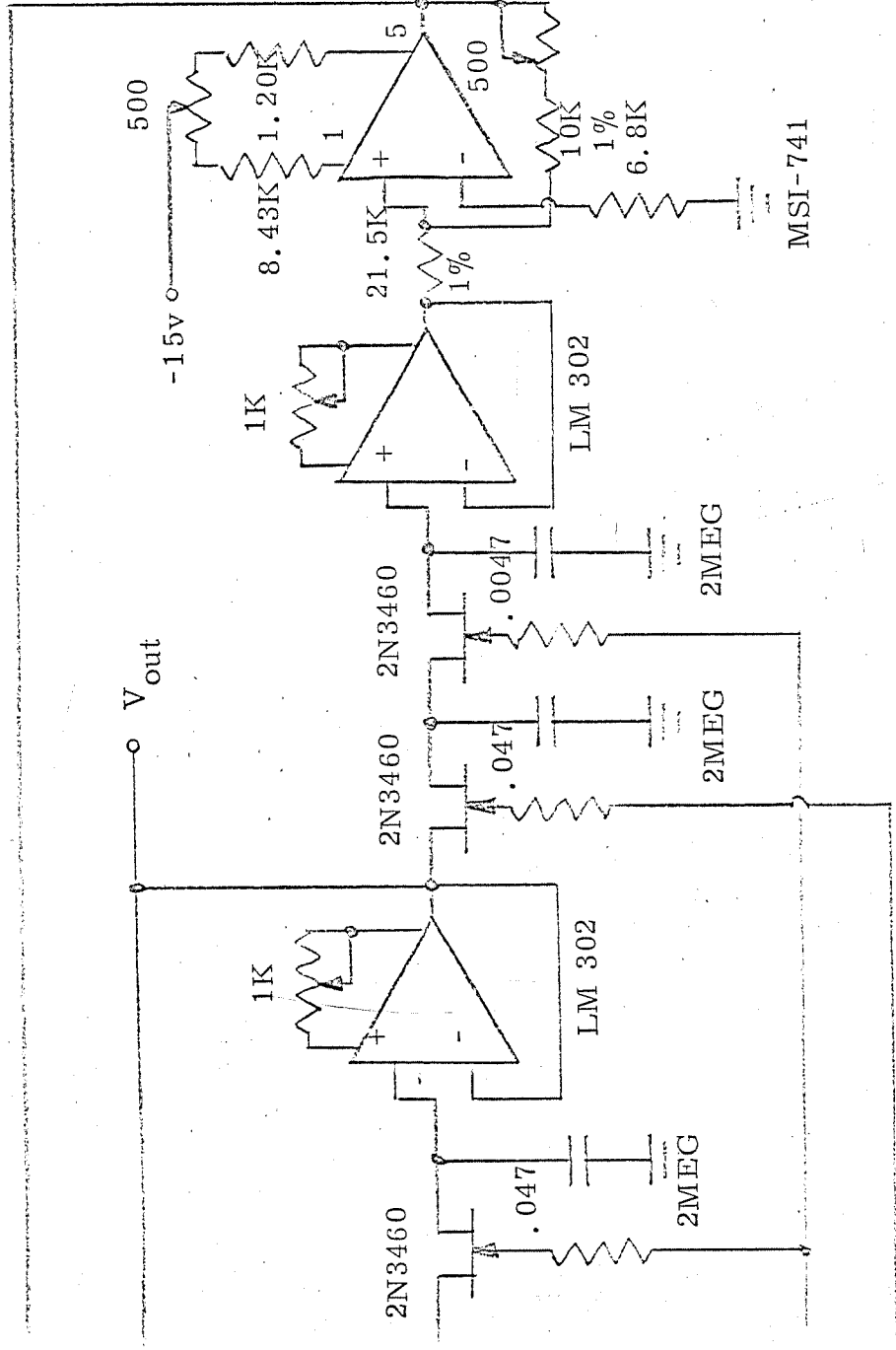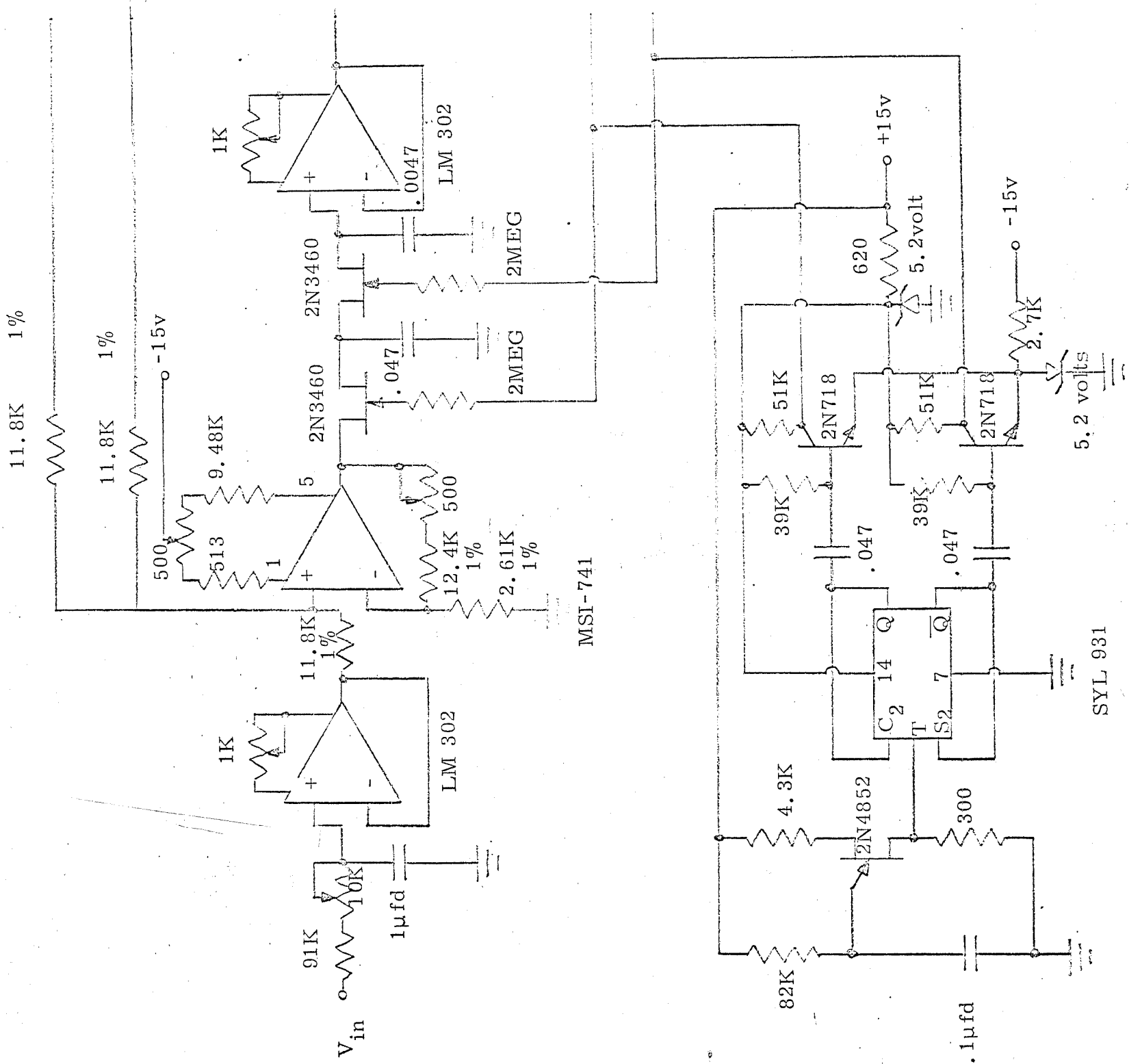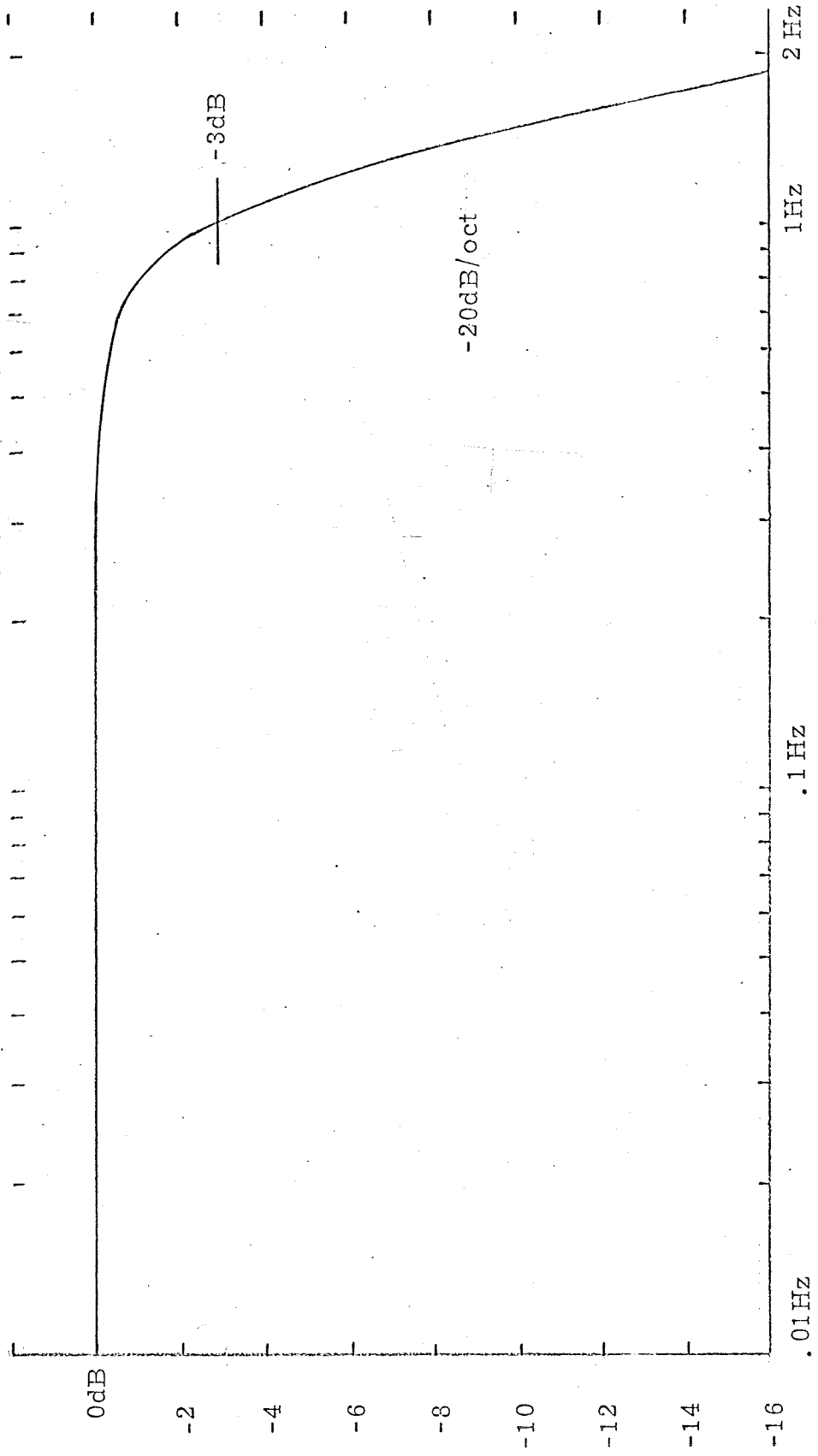
Figure 6. Third degree analogue-digital filter

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Figure 7. Voltage gain (in dB) vs. frequency for 3rd order filter system
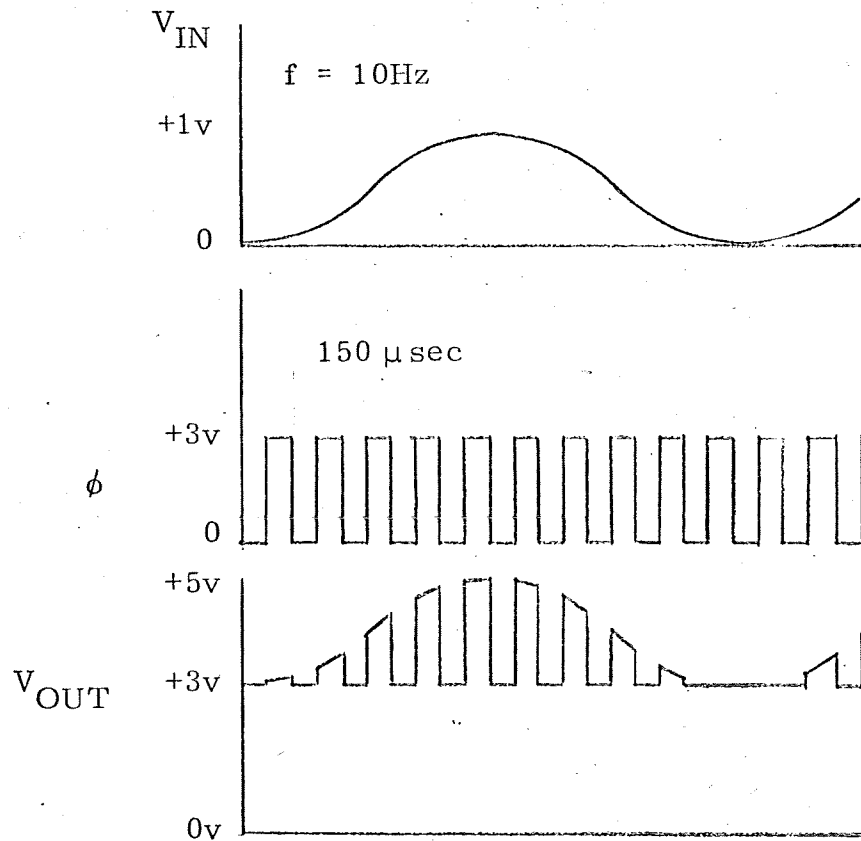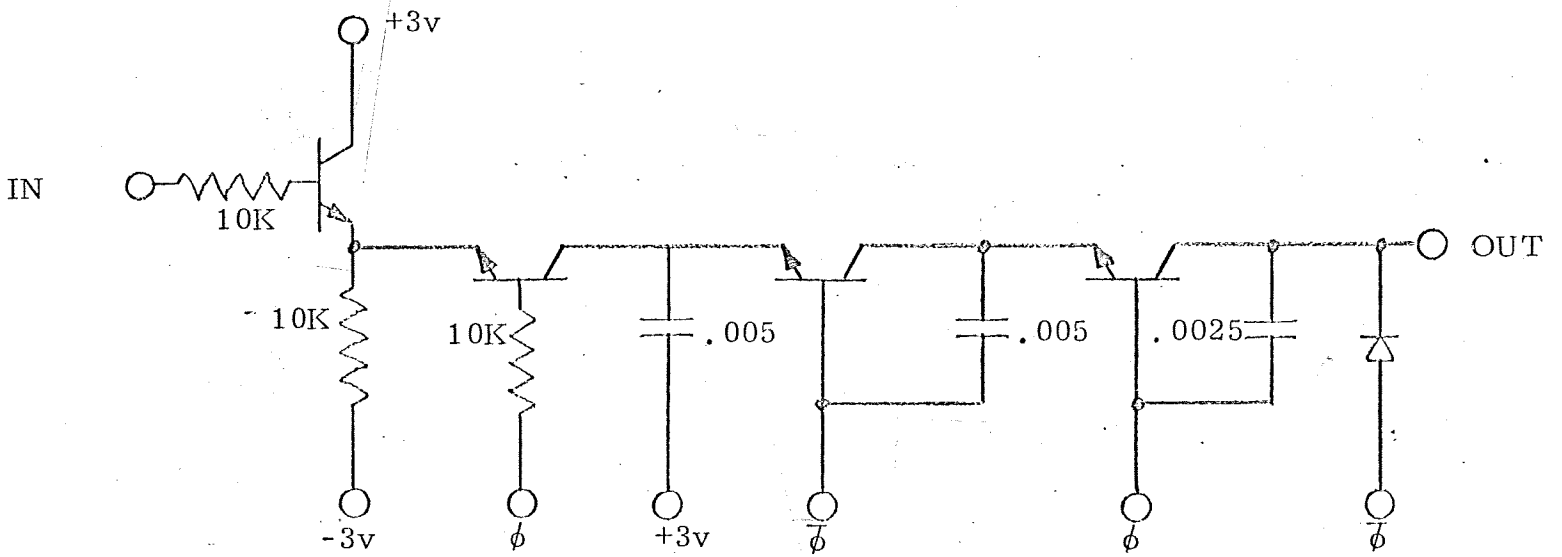
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Figure 8. Analog delay with gain

in the reference. To the extend that different capacitance sizes can be realized on the same substrate a capacitance amplifier can be realized thus eliminating the need for an operational amplifier. In the circuit illustrated the unequal sized capacitors allow an overall gain of two to be achieved. (This capacitance-amplifier concept goes beyond the scope of the reference sited and is an observation unique to this research).

As of this writing the deficit charge approach appears quite promising. A second degree filter is under development at present and gives every promise of more ready synthesis employing monolithic integrated circuits.

V. Analysis of Pulsed-Light Sources

A total of five duo-diode light sources were fabricated by K. Hergenrother[*] since the writing of Report No. 3. Each duo-diode consisted of two separate gallium-arsenide-phosphide junctions mounted on a TO-5 header. A spectro-photometer was used to measure the emission characteristics of each. One diode from each package was found to radiate at a wavelength of 665 ηm with a half-intensity bandwidth of about 18 ηm and a 5% intensity wavelength band-width of about 40 ηm. The other diode of each package had a center wavelength of 825 ηm with 50% and 5% intensity bandwidths of 30 and 80 ηm respectively. One of the 665 ηm diodes had a lot of energy at about 1 micron but this was prevented from influencing later measurements by utilizing a light filter which caused its attenuation.

The light diodes were employed in the pulsed mode in the light system described in Section V of the previous report. Transmission measurements were made through various solutions of dyes and blood samples. The amount of error encountered in measurements was discovered to be directly related to the spectral spread of the light sources and the variation in transmission characteristics of the solution in the spectral region in question. Reasonable accuracy was obtained when the transmission characteristics had certain shapes (such as flat, etc.) throughout the emission region of the diode under measurement.

Quantitative measurements and error levels were made by measuring the transmission characteristic with spectro-photometer, approximating the emission characteristics of the light sources with triangles, and utilizing a computer program to correlate experimental results with calculated results. The data and conclusions will be forthcoming in a M.S. Thesis by R. Lehman which will be submitted by September, 1970. Presently it appears that the Hergenrother diodes are not suitable for blood oximetery measurements because of their spectral widths. However, this does not preclude their use in connection with measurements made on different solutions.

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[*] Currently with NASA-ERC

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VI. Projections

The body of work associated with the theoretical aspects of the doctoral dissertation on active circuit synthesis will close in June, 1970. It is anticipated that the thesis itself will treat experimental synthesis only to the extent necessary to verify design concepts. Work will continue utilizing hybrid circuit techniques in order to produce working display units for various applications.

Prototype dc-to-dc converters should be available in the near future. Miniaturization will be carried out utilizing further refinement in hybrid techniques by a master's level graduate student who will join the group in June 1970.

The immediate future projection for work in the analogue-digital filter is also directly related with miniaturization and will proceed along with the converter development. In this case, however, emphasis will be directed more toward construction feasibility along monolithic lines.

The pulsed-light source analysis work will close with the submission of the M.S. Thesis in September, 1970. Future work may possibly be directed toward light sensors for specific applications.