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STUDY OF HIGH VOLTAGE SOLAR ARRAY CONFIGURATIONS WITH INTEGRATED POWER CONTROL ELECTRONICS

by

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GENERAL ELECTRIC COMPANY

prepared for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
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Contract No. NAS 3-8997
NASA Lewis Research Center

Bernard L. Sater, Project Manager

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Final Report

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ABSTRACT

This study defined solar array electrical configurations which regulate and reconfigure, by switching, a 16 KV, 15 KW array with electronics integrally mounted to the array substrate. A hypothetical mission included load requirements of: 1 KV to 16 KV, milliamperes to amperes, $\pm 0.1\%$ voltage regulation, and array switching to supply alternate load configurations. Voltage regulation is by a binary-coded digital switching system, which short-circuits series connected solar cell groups. Minimal total power dissipation and high power transfer efficiency are system characteristics. A general case solution and specific optimized systems were derived. Performance estimates show significant weight savings compared to conventional power conditioning. Problem areas include charged particle radiation and thermal transient effects, and high local power dissipation in semiconductor switches and electronics packaging. Future work requires high voltage switch and isolator development, resolution of environmental problems and breadboard regulator tests.

SECTION 1

SUMMARY

The purpose of the subject effort was to study electrical configurations for a high voltage solar array (HVSA) which would provide regulated D.C. power directly to spacecraft loads. Primary goals included definition of (1) conceptual designs of electrical configurations for HVSA systems with integral power conditioning, i.e., where all power control functions are array mounted, (2) problems (particularly with switches) associated with HVSA power system development, and (3) future effort to resolve problems identified.

A representative mission was hypothesized where the HVSA (1) supplies power to ion thrusters to raise a spacecraft from low orbit to synchronous altitude orbit in a 90 day period and (2) switches the power to high frequency high voltage electron tubes for broadcast purposes for a period of 5 years.

Definition of generalized load requirements was made in an attempt to define HVSA configurations having applicability to a wide range of loads. Requirements included: (1) voltage range from 1 Kv to 16 Kv, (2) regulated load power of 15 Kw at 16 Kv and alternately 15 Kw total at six or more voltage levels, (3) load current from milliamperes to amperes, (4) system regulation tolerance of $\pm 0.1\%$, and (5) provision for HVSA reconfiguration to supply alternate load systems.

The requirement to perform many and varied switching functions is fundamental to the HVSA. Switching is necessary to (1) arrange HVSA building blocks (power modules) in alternate series-parallel system configurations, (2) connect and disconnect loads from the power sources, (3) establish the voltage reference point, and (4) provide protection for loads and the array. Switches for functions (2) and (3) must block up to 16 Kv, which presently exceeds semiconductor device capability. System tradeoffs show building blocks should be designed for maximum output voltage; 1500 volt transistors are feasible and also satisfy the remaining switch functions.

Systems tradeoff studies have eliminated conventional series and shunt regulator systems and maximum power tracker systems in comparison to a system which achieves regulation by a binary-coded switching system. The selected discrete switching system (1) appropriately short circuits series connected solar cell groups to achieve voltage regulation and (2) reduces problems of rejecting excess array power and unneeded array power (when loads are off) by operating the solar cells in a shorted mode, which produces considerably less total heat dissipation than other techniques.

Reliability analyses resulted in selection of an optimum array configuration to minimize effects of cell failures and shadows. Tradeoff studies demonstrate that on the basis of efficiency considerations it is desirable to minimize the number of building blocks, and to design for highest building block voltage and current that satisfies the alternate loads when the HVSA is reconfigured.

Study goals for the HVSA configuration were the attainment of 108 watts/m^2 and 66 watts/Kg. System performance calculations demonstrate a typical 1.5 KV HVSA building block is capable of delivering 117 watts/m^2 and 70.5 watts/Kg when delivering regulated power. An optimized representative system of building blocks delivers 24.6 Kw of regulated power with a total system weight of 381 Kg.

Major conclusions are that the HVSA concept is feasible, but several major problems must be resolved. These include: severe radiation damage in the transfer orbit, minimization of synchronous altitude radiation damage in the transfer orbit, minimization of synchronous altitude radiation effects on array mounted electronics, developing and qualifying a solar cell module/electronics package capable of surviving thermal cycling, developing a 16 Kv load switch (semiconductor or lightweight/small volume relay), development of a high blocking voltage low level signal coupler, electronic device characterization at low HVSA temperatures, and high local heat dissipation in semiconductor switches.

Future work recommended includes high voltage device development, breadboard binary regulator fabrication and test, comprehensive power systems analyses, design and development of a typical HVSA building block, and resolution of aforementioned problems.

SECTION 2

INTRODUCTION

This is the Final Report of the "High Voltage Solar Array Electrical Configuration Study" performed by the Space Systems Organization of the General Electric Co. for the NASA - Lewis Research Center under Contract Number NAS 3-8997. Briefly, the purpose of this effort was to define solar array electrical configurations which condition high voltage, high power solar arrays with all power control electronics integral with the array. Parallel studies have been conducted for NASA Lewis Research Center under Contracts Number NAS 3-8995 and NAS 3-8996.

The anticipated advent of satellites incorporating ion thrustors and high frequency electron tubes (Klystrons, etc.) has created a need for D.C. power supplies with 2,000 to 16,000 volt outputs. The present thrustors require from 2,000 to 5,000 volts D.C. at the accelerator electrodes. The near future tubes may require up to 16,000 volts D.C.

The D.C. power required for the thrustors and tubes is expected to be derived from solar arrays. It is further expected that for many satellites where thrustors and tubes are involved, a major portion of the total solar array power will be used by these systems and used at relatively constant power levels during steady state operations.

Conventional solar arrays are wired to deliver their D.C. power at less than 100 volts. For the present low voltage solar arrays to meet the high voltage requirements noted above, it is necessary to transform the low voltage into a higher voltage through the use of heavy and complex power conditioning equipment. Typically, each one kilowatt of regulated power is delivered with 15-30 pounds (6.8-13.6 Kg) of conditioning equipment.

In light of the system needs described above, a departure from the conventional method of developing solar array power may be desirable. In this regard, it appears desirable and feasible to:

1. Develop solar array power at the voltage levels required by the major using loads.

2. Provide on the array itself, the power conditioning required by the major using D.C. loads.

Such a high voltage solar array (with integrated D.C. power conditioning equipment and capable of delivering discrete voltage levels from 2,000 to 16,000 volts to the using load) should reduce the complexity and weight and increase the overall reliability of the total power system.

The information necessary to design the high voltage solar array described above must be determined. To obtain the information to design such arrays, research and development effort is necessary in the areas of (1) operating high voltage solar arrays, (2) providing power conditioning and switching integral with the array (3) developing deployable large area array configurations. Studies of the first of these areas has been conducted under Contracts NAS 3-11534 and NAS 3-11535. The subject contract and this report are concerned with the second of these areas.

The subject effort is significant because it demonstrates that regulation on the array can be performed with high efficiency and minimum total power dissipation compared to conventional series and shunt regulated power systems. Regulated load power can be delivered with a penalty of only 0.33 pounds/Kw (0.15 Kg/Kw) including all electronic devices (with quad redundancy), heat sinks and radiation shielding.

Array reconfiguration, necessary to provide for supplying power to alternate load configurations, can be performed with transistors that are readily available or need minimal development.

Load switching on the array requires 16Kv silicon controlled rectifiers which are unavailable and may not be feasible. Relays may be a more successful approach. Voltage isolation (16 Kv) between signal circuits and high voltage sections is required and can be achieved using light emitting diodes - fiber optics - and photosensitive devices, which are feasible.

The HVSA concept is shown herein to be feasible, but the device problems described previously and radiation, thermal cycling, and packaging design problems must be resolved.

SECTION 3

REQUIREMENTS, DESIGN GOALS AND GUIDELINES

3.1 GENERAL

This section presents the contractual and technical bases for the subject study. Requirements and Design Goals established in the Statement of Work are discussed in Section 3.2. Section 3.3 establishes Guidelines derived from the Statement of Work and during the Mid-Term Oral Presentation.

3.2 REQUIREMENTS

3.2.1 SCOPE

The Statement of Work defines the scope of the subject effort to be a study of electrical configurations for a High Voltage Solar Array (HVSA) which would provide conditioned D. C. power directly to a using load and define:

1. Conceptual designs of electrical configurations for high voltage solar arrays with integral power conditioning.

2. The problems, and in particular the switch problems, associated with developing such electrical systems.

3. The efforts required to resolve the problems defined by the study.

3.2.2 TECHNICAL REQUIREMENTS

The possible applications of a switchable HVSA are many and varied. A single applications, hopefully representative of the general scope of problems, was defined to provide direction to the study.

The array application envisioned (1) supplied power to ion thrustors to raise a spacecraft from low orbit to a synchronous orbit and then (2) switched the power to high frequency electron tubes for broadcast purposes.

The array must be capable of providing power for the following periods:

1. Produce 15,000 watts of power divided between up to six (6) different voltage and power level combinations for a period of three months while traversing from a 100 N. M. (185 Km) to a synchronous altitude orbit.

2. Produce 15,000 watts of power at 16,000 volts at the end of a period of five (5) years at synchronous altitude.

General requirements for the HVSA study are:

1. Use switchable building blocks to comprise the array configuration. A building block (BB) is defined as a combination of solar cells, power conditioning, and switches capable of (1) delivering regulated load power at an output voltage, V_{BB}, and (2) being switched in series and parallel with other BB.

2. Load Power Requirements - 15 Kw @ 16 Kv and up to 15 Kw at several (> 6) voltages in the range from approximately 1 to 16 Kv.

3. Provide capability to reconfigure the solar array to any electrical series-parallel arrangement in the supply voltage range by command.

4. Provide floating output voltages or locate ground to obtain voltages up to $\pm$ 16 Kv to ground.

5. Provide capability to connect and disconnect any load.

6. Provide automatic protection against open circuit and short circuit failures.

7. Regulate load voltage to $\pm$ 0.1% zero to full load current.

8. Provide voltage isolation between signal (command) circuits and high voltage circuits on the HVSA.

9. The array must be capable of operating with either a negative or a positive bias relative to the space plasma potential.

10. The array must be capable of operating in the space environment from 100 N.M. (185 Km) to synchronous altitudes.

11. The array's ability to perform its mission function must not be negated (except for loss of power in the earth's shadow) by operation in eclipse orbits. The HVSA must servive the eclipse and provide protection to the power electronics and loads during the eclipse transients.

12. The array must have adequate safeguards for personnel protection during ground handling operations.

13. The array should be capable of producing 66 watts/kilogram (30 watts/lb) and 108 watts/sq. meter (10 watts/ft^2).

14. The reliability after array deployment is a 0.99 probability of design power at the end of 5 years with a 90% confidence level.

3.3 GUIDELINES AND GROUND RULES

1. The study was to concentrate on determining the feasibility of using microelectronic packaging techniques to implement power conditioning and switching functions integral with the array substrate. Because of the requirement to consider light weight solar arrays of relatively thin substrate cross section, conventional discrete electronic components are ruled out by virtue of their large size. The results of the investigations pursued shall be applicable to most array configurations or deployment techniques.

2. A major goal of this study was to identify the need for new devices, such as switches. On the basis of a survey of semiconductor device manufacturers, it was assumed that high voltage (16 Kv) silicon controlled rectifiers (SCR) and high voltage (1500 volt transistors) could be developed. This assumption permitted electrical configuration studies to proceed on the basis that device characteristics were not the limiting considerations.

3. The HVSA building block (BB) is to possess a maximum of flexibility - i.e., the capability of delivering power to the load over the widest practical range of voltage and current. The current range was from mA to amperes and the voltage range from hundreds of volts to non-integral multiples of 1 Kv, with an upper limit of 1500 volts established by semiconductor maximum voltage capability.

4. The technique of deployment and construction that shall be assumed for design estimates, as to weight and size, is that given in Feasibility Study 30 Watts Per Pound Roll-Up Solar Array Final Report No. 68SD4301, dated June 21, 1968, JPL Contract No. 951970 with General Electric Company, Missile and Space Division.

5. It was an early conclusion of this study that post-eclipse solar array substrate temperatures much below -55°C (+218° K) will occur at syncrhonous altitudes and that state-of-the-art voltage references cannot maintain ± 0.1% regulation over the anticipated temperature range. Therefore, a ground rule was established that the voltage reference and voltage sampling and error detection functions would be performed by a computer function on-board the spacecraft.

6. Additionally, a ground rule was established that power conditioning (voltage regulation) was not necessary at HVSA temperatures below -55°C (+218° K). This was important because little or no data exists for electronic device performance at temperatures below -55°C (+218° K). This ground rule did not preclude future requirements to raise or lower the "cold" array temperature at which the voltage regulation function would be initiated following spacecraft emergence from the earth's shadow.

   Solar cells, power conditioning, switch functions and spacecraft loads must all survive and be protected from the potentially deleterious affects associated with eclipse orbit low temperature excursions.

7. Electrical configuration studies will not be based upon specific load characteristics for the ion thruster and transmitter. Array and power conditioning configurations shall provide for maximum utilization of array power for all loads at all voltage levels. Ground rules were established concerning the spacecraft loads in order to maintain the study results general in nature:

   a. Loads require no power during the HVSA warmup interval following eclipse. Therefore, regulated voltage need not be made available under "cold" array conditions.

   b. Loads may not be used to hold down array voltage during post-eclipse warmup; certain loads may be damaged by exposure to increasing supply voltages.

   c. Loads do not require power during array reconfiguration. It is therefore possible to disconnect the load(s) when in the process of array reconfiguration.

   d. Loads may not be disconnected by slowly decreasing the array voltage - certain loads may be damaged when exposed to slowly decreasing supply voltages.

8. A major goal of this study was that requirements for new or modified devices be identified and justified. Recommendations for device development must be accompanied by justification that device development is feasible.

9. The preferred technique for voltage regulation uses switches to effect discrete or incremental voltage changes; however, other electrical systems concepts were to be considered.

10. Analyses conducted early in the study demonstrated significant (charged particle) radiation induced performance degradation of the HVSA occurred during the transfer period from parking orbit to synchronous altitude. Therefore, in order to avoid excessive array penalties which could not contribute to the study goals, this degradation mechanism was omitted. Recommendations were made for future analyses to consider various approaches to minimize the impact of radiation damage on the spacecraft and HVSA.

SECTION 4

ENVIRONMENT CONSIDERATIONS

4.1 GENERAL

The hypothetical mission described in Section 3 for the HVSA includes a range of earth orbits and an environment in which many spacecraft have successfully operated. However, the long duration ascent trajectory from parking out to synchronous altitude, low thermal mass and low radiation shielding properties of the rollup solar array, and requirements for high local heat dissipation capability combine to present unique environmental challenges to the HVSA. These environmental factors have been analyzed and the results are presented in this section. A separate program, the "High Voltage Solar Array Study," is being conducted for NASA (Contracts NAS3-11534 and NAS3-11535) to consider the problems of operating a high voltage (16 kv) solar array in the space environment.

4.2 HVSA ENVIRONMENT FACTORS

4.2.1 THERMAL CYCLING

The HVSA is to operate for five years in an equatorial 24-hour synchronous orbit which is achieved by a spiraling transfer orbit from the 100 NM (185 Km) circular parking orbit to the 19,300 (35,800 Km) synchronous orbit over a period of 90 days. Assuming the vehicle is constrained to fly a very nearly circular orbit while acted upon by a nearly tangential thrust, modulated so that the thrust to mass ratio remains a constant, an equation relating spacecraft altitude with time has been developed and is presented in Section 9.1, Radiation Environment and Effects Predictions, and is accompanied by a plot of the altitude vs time.

An approximation of the number of thermal cycles (day-night transitions) encountered during the 90-day transition is obtained by assuming a constant altitude during a 24-hour period, computing the resulting number of passes, up-dating the value of the altitude for the succeeding 24-hour period, computing the resulting number of passes, etc. summing thte total passes as this iteration is performed 90 times. The number of thermal cycles thus computed is 585. It can be shown that the maximum error is no greater than the number of passes during the first 24-hour period (16). This number (585) assumes that the transition orbiting occurs in the earth equatorial plane with each revolution yielding an eclipse period.

Eclipse periods in the synchronous equatorial orbit are encountered when the sun declination with respect to the equatorial plane is in the range of $\pm$ 8.3 degrees, which results in 90 eclipse periods per year, or about 450 thermal cycles during the 5-year mission at synchronous altitude.

The total number of thermal cycles incurred during the ascent and synchronous orbits is computed to be approximately 1035.

The occurrance of thermal cycling is significant for several reasons:

1. Experience with solar arrays has demonstrated that I-V curve degradation (softening of the knee of the I-V curve) and open circuits (associated with solar cell fractures and interconnection tab fatigue arising from repetitive working) are dependent upon (1) the number of thermal cycles, (2) rates of array temperature change, (3) maximum illuminated temperature, and (4) the "low" or "cold" eclipse temperature. For purposes of this study, it is sufficient to identify the thermal cycling environment as a potential cause of array mechanical and performance degradation - a discussion appears in Section 10, Problems Identified.

2. Another aspect of the array thermal cycling environment is the impact upon power conditioning and switching. Influence of temperature transients and array "cold" temperatures are discussed in Section 5, Technical Analyses, for the switching, regulation, and array functions of the HVSA.

3. Section 4.2.3 presents the array temperature profile predicted for the HVSA and the bases for the resulting calculations.

4.2.2 CHARGED PARTICLE ENVIRONMENT

An estimate of the electron and proton fluxes in the transition and synchronous orbits and the protons in a solar flare model is presented in Section 9.1, Radiation Environment and Effects Predictions. Radiation damage investigations reported in Section 5.3 show an intolerably large amount of solar cell power degradation caused by the ascent orbits passing through the dense regions of the Van Allen Belts. In order to proceed further in this study, it was assumed that this transition damage is protected against (perhaps by heavier solar cell shielding than that provided by the referenced rollup solar array, (see Section 3) by altering the flight path to synchronous altitude, or by deploying only that portion of the total array needed to power the ion thrustor.

The solar flare model produces about four times as much damage-equivalent, normally-incident 1-MeV electron flux as the synchronous trapped electrons and protons, such that about 28 percent solar cell power loss is predicted for five years if no flare is considered, and about 41 percent power loss if the solar flare flux is included in the damage assessment.

A possible enhancement to mission performance is the concept of retracting the rollup solar array in advance when a severe solar flare is expected. The referenced rollup array design readily accommodates this feature, requiring approximately 20 watts for less than 5 minutes per 250 ft^2 array section to perform the deployment or retraction operation. It is noted that intense flare activity can be present in the synchronous orbit for periods of time up to one or two days in duration, indicating the need for electrical energy storage to maintain spacecraft orientation and to allow access to ground commands as well as to re-deploy the rollup array sections.

The impact of the charged particle environment upon semiconductor device performance and array design is significant and is discussed at length in Section 9.1, Radiation Environment and Effects Prediction.

Sizing of the solar array for the HVSA systems considered in this study is based upon solar cell radiation damage due to the trapped particles at synchronous altitude and the predicted solar flare particles.

4.2.3 SOLAR ARRAY TEMPERATURE-TIME PROFILES

An estimate of the temperature versus time relationship for the HVSA was made for the 100 NM (185 Km) parking orbit and for the 19,300 NM (35,800 Km) synchronous orbit because these altitude extremes represent conditions which cause the highest and lowest array temperatures in the hypothetical mission established for this study.

It was assumed that the solar array is maintained perpendicular to the earth-sun line during the entire orbit. Array thermal mass is 0.2 lbs/ft^2* (0.98 Kg/m^2), with a specific heat of 380 W-sec/lb-^oK. Values of illuminated side absorptivity and emissivity of 0.67 and 0.8, respectively, were used with back side (Kapton) average values of 0.41 and 0.67 for absorptivity and emissivity. Heat transfer by radiation only was considered. A typical solar cell conversion efficiency of 8% was used for the temperature calculations of a normally loaded array and 0% for an unloaded array. The latter case defines the maximum array temperature used for heat sink area and semiconductor device temperature calculations (Section 4.2.4).

Figure 1 presents the temperature vs time profiles for the solar array for the two extreme orbits. The synchronous altitude profile is negligibly influenced by albedo and ranges from a low temperature of about -173^oC (100^oK) to a steady-state high temperature of about +43^oC (+316^oK). The significant albedo influence in the 100 NM (185 Km) orbit produces about a 20^oC (20^oK) increase in temperature when the array is above the subsolar point, which disappears as the array moves behind the earth terminator. Infrared radiation from the earth surface limits the cold temperature extreme in the low-altitude orbit to about -80^oC (193^oK) at the end of the eclipsed portion of the orbit. A high temperature of about +83^oC (356^oK) is predicted for the 100 NM (185 Km) orbit, unloaded (efficiency = 0) solar array.

*Value based upon characteristics of the referenced Rollup Array.

Based on available information, the expected cold temperature of -173°C (100°K) is beyond the range for which a rollup solar array has been qualified.

End-of-Eclipse temperatures have been calculated to demonstrate the impact of thermal mass and Kapton emissivity (ϵ) variations. Figure 2 relates end-of-eclipse temperature to thermal mass and shows a 10°C (10°K) increase in temperature for each 0.1 pound/foot^2 (0.49 KG/m^2) increase in mass. Since the mass of the referenced rollup array blanket assembly is 0.2 pounds/foot^2 (0.98 Kg/M^2) the penalty for increasing eclipse temperature by only 10°C (10°K) from -174°C (+99°K) to -164°C (+109°K) is 50% in blanket weight and 30% total array weight. Thermal mass changes do not affect steady-state high temperature (and array power output).

The wide variations reported for kapton ϵ* have prompted the need for the curves in Figure 3. Steady state (illuminated) and end-of-eclipse temperature are both affected by kapton ϵ variations but to differing degrees. Decreasing Kapton ϵ from a value of 0.67 to 0.5 increases "LOW TEMP" by only 3.5°C (3.5°K) and "HIGH TEMP" by 10°C (10°K) resulting in a 5% array power loss. This is a severe power penalty for a relatively small increase in eclipse temperature. The same increase in temperature can also be achieved by increasing thermal mass to ~ 0.235 pounds/ft^2 (1.15 Kg/M^2) which increases array blanket weight by 17%.

The conclusion is that increasing mass or reducing kapton ϵ to raise the eclipse temperature results in small temperature improvements with large penalties in weight and area. Therefore, future array thermal cycling qualification criteria will be insignificantly affected if temperature limits are based on minimum weight and area designs. Furthermore, measurements are required to provide considerably more statistical confidence in Kapton ϵ since ϵ variations affect array power sig ificantly.

Array sizing and performance estimates presented in Section 7, System Performance Estimates, are based upon a steady-state synchronous altitude orbit temperature of +43°C (+316°K). Further discussion appears in Section 5.3, Solar Cells and Array.

4.2.4 TEMPERATURE OF MICROELECTRONIC SWITCHES

It has been shown in Section 4.2.3 that the temperature of the rollup solar array can be as high as +83°C (356°K) with incident solar energy, albedo and earth "blackbody" radiation as the only heat inputs. Power dissipation in the regulation switches and the inter-building block switches will increase the array temperature locally to values greater than shown in the array temperature-time profiles. A worst-case thermal analysis was performed to estimate the maximum operating temperature of a semiconductor chip (switch) bonded to an alumina substrate, which in turn is bonded to the back side of the kapton array blanket with epoxy adhesive. It is assumed for this analysis that conduction between the actual semiconductor switch and its alumina substrate is ideal, i.e., they represent an isothermal mass. The choice of alumina as a microcircuit substrate has not been finalized, but it does appear as a representative candidate.

Appendix A presents the details of the thermal analysis. Starting with the rollup array and micro-circuit substrate, a much simpler but thermally equivalent model is developed. Iterative solution of conduction equation and a radiation equation yields the steady-state temperature for the microcircuit substrate, which is conservative (higher than actual) because of the worst-case assumptions made in the development of the thermal model.

This method has been mechanized, and a computer program used to determine temperatures for semiconductor substrates dissipating from 1 to 8 watts, with substrate areas of 4, 8, 12 and 16 cm^2. The results are plotted in Figure 4. The worst-case assumption of an array temperature of +83°C = +356°K (equator crossing at 100 NM (185 Km) altitude with maximum solar intensity) was employed to emphasize the possible high-temperature conditions. Values of power dissipated in the various semiconductor devices employed in the HVSA design are presented in Section 5.1.11.

*Emissivity values in the literature range from 0.65 to 0.89; an average value of 0.67 has been determined for this study.

The thermal model incorporated in the temperature calculation process is inadequate to analyze the effect of the very high SCR power dissipation (16 to 80 watts). A possible approach to reducing the dissipation in the SCR conducting mode (80 W for an 8A load) might be to employ several parallel devices for this purpose. However, the load sharing problem with parallel SCR's is apparently very complex. It is also noted that, even with parallel SCR's, the power dissipation due to leakage when blocking high voltage is not reduced for each SCR, and in fact may be even greater than the dissipation in the conducting state, since vendors have indicated that leakage currents as high as 20 mA may occur when blocking 16 Kv.

4.2.5 ULTRAVIOLET RADIATION ENVIRONMENT

UV radiation has been reported (Reference 1) to cause some degradation in solar array power output. While of significance to the array designer this factor is not significant to the subject study.

4.3 SUMMARY

The HVSA environment, in sufficient detail to quantitatively assess the most significant effects, has been defined. Reference is made to other sections of this report where the effect of the environment is considered. Temperature cycling, charged particle radiation, and the thermal environments are considered as significant environmental factors.

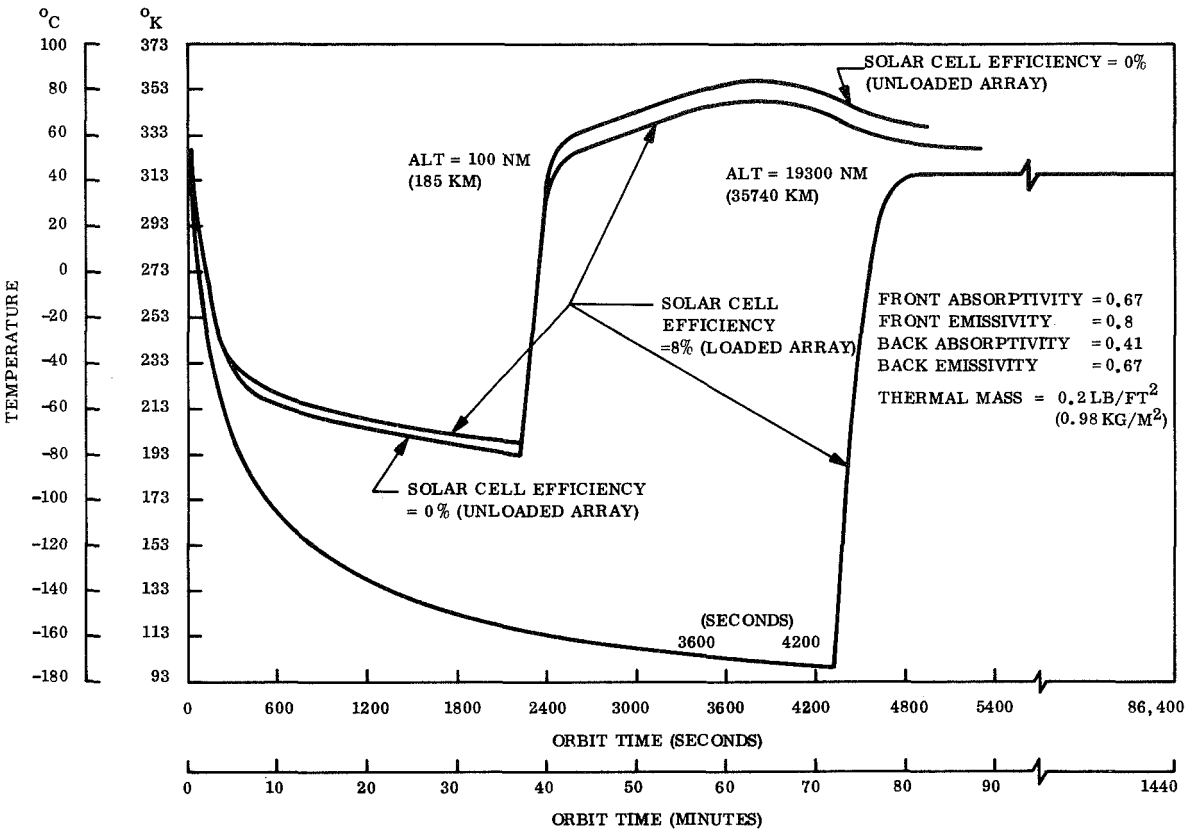


Figure 1. HVSA Temperature versus Time Profiles

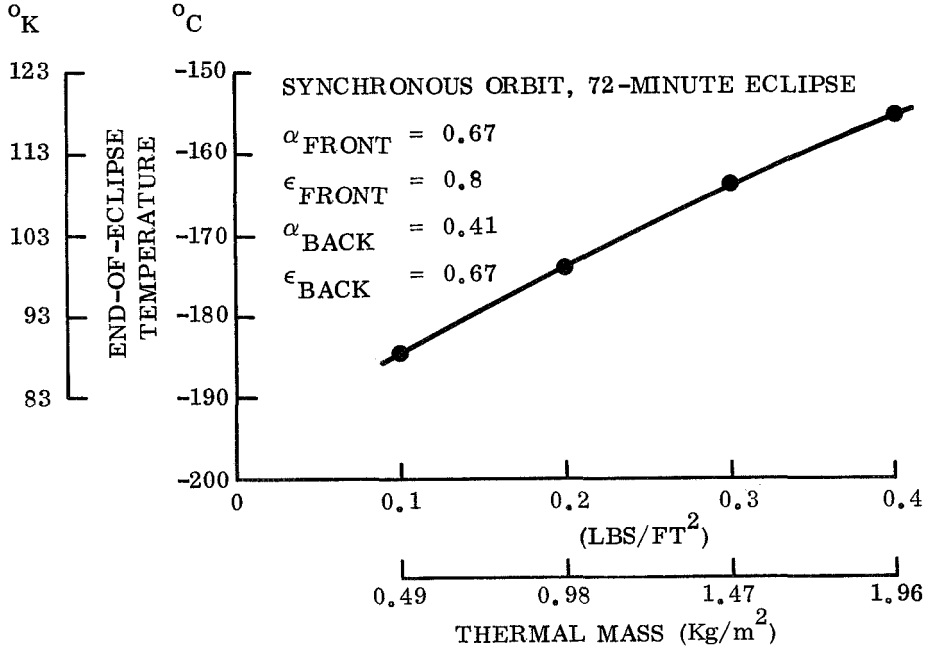


Figure 2. Effect of HVSA Thermal Mass on Temperature

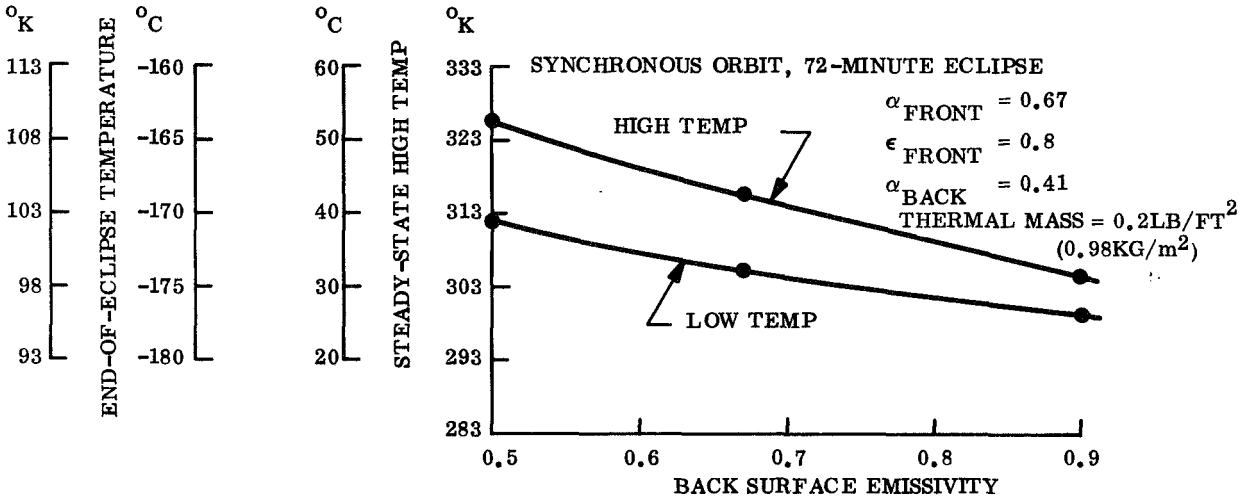


Figure 3. Effect of Back Surface Emissivity on HVSA Temperature

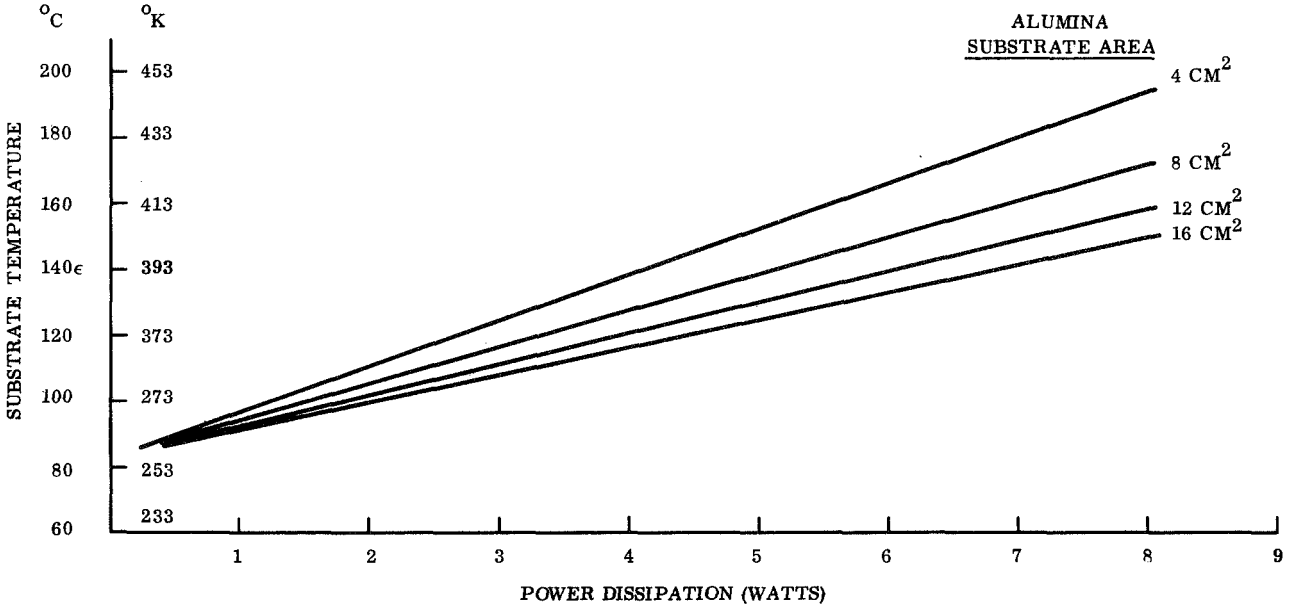


Figure 4. Microelectronic Substrate Temperature versus Power Dissipation and Substrate Area

SECTION 5

TECHNICAL ANALYSES

This section provides detailed discussion of switching, solar array, power conditioning and various system tradeoff considerations. Development of a recommended system switching configuration is presented, and alternate approaches to regulation by discrete switching are described. Circuit schematics for the various switching and regulation functions are introduced and the spacecraft/solar array signal interface is defined for a selected method of system regulation. Comparison of alternate power system block diagrams and solar cell connection arrangements is made. The impact of a wide range of building block voltage and current capability on total system sizing is discussed, resulting in definition of a general building block design criterion.

5.1 SWITCHING FUNCTIONS

5.1.1 GENERAL

The requirement to perform many and varied switching functions is fundamental to the concept of a HVSA. Switching is necessary to rearrange building blocks in alternate series-parallel system configurations, connect and disconnect loads from their power sources, establish the voltage reference point, provide protection for the loads and power source and to implement the discrete voltage change technique of load voltage regulation. Regulation switching is discussed in Section 5.2; this section presents considerations of the remaining switching functions.

A definition of each switching function is made here, and will apply to the use of these terms throughout this report.

1. Stacking Switch Connects a building block electrically in series with another building block when in the "ON" (closed) state.

2. Coupling Diodes Connect the positive and negative terminals of a building block electrically in parallel with the respective output terminals of another building block when the stacking switch between the two blocks is in the "OFF" (open) state.

3. Array Shorting Switch Short-circuits the entire output-power-generating solar cell complement of an individual building block when in the "ON" (closed) state.

4. Load Switch Connects the regulated solar array output to the "hot" terminal of an individual load, permitting load current, when in the "ON" (closed) state.

5. Load Return/Array Ground Switch Connects the spacecraft ground, or reference, point and/or the common load return to the solar array when in the "ON" (closed) state.

Each of the above switch functions can be maintained in either the "ON" or "OFF" mode for steady-state operation; blocking diodes are automatically reverse-biased (OFF) when the associated stacking switch is ON. Operation of any switch function is independent of other switches, although a particular switching sequence may be necessary or preferred. Signals governing operation of the switch functions are received from the spacecraft via high voltage signal couplers (see Section 5.2); signals may originate from ground commands or from on-board spacecraft logic functions.

Effort during this study has been directed toward the use of array substrate-mounted microelectronic components, which has precluded the investigation of more conventional, bulky components, such as packaged relays for switching functions. However, the question of the feasibility of a high-voltage semiconductor load switch remains, and a severe design problem exists in providing adequate heat sink capability on the array for such a device. Future effort to include feasibility determination of a high voltage semiconductor switch and development of a high voltage relay for the load switching function is recommended in Section 11.

5.1.2 GENERAL CASE SYSTEM SWITCHING CONFIGURATIONS

The goals to be attempted when selecting a general purpose switching configuration for a HVSA system are:

1. Compatiblity with the electrical requirements established in Section 3.

2. Flexibility in structuring the building block series-parallel arrangements.

A switchable block concept that would fulfill these requirements is shown in Figure 5. The system is arbitrarily powered by 16 1Kv building blocks and is supplying 6 different loads having various current and voltage requirements. There are 15 switches for connecting the 16 array building blocks in series, S_{S1}-S_{S15}, and 15 switches for paralleling the blocks, S_{PL1}-S_{PL15}. With this switch arrangement, a group of one to 16 blocks can be connected in series or parallel or a combination of both, independent and isolated from those blocks which were not switched. This scheme does not allow arbitrary placement of a block in parallel with or in series with any other block, but does permit all combinations of electrical series/parallel arrangements possible with 16 blocks. The scheme also provides 17 switches, S_{G1}-S_{G17}, for "grounding" the array at any point. The loads are connected at whatever electrical output tap represents the correct voltage for the loads.

The paralleling switches for this scheme require two poles, and therefore would be realized by two solid state switches. Thus a total of 62 switch functions are required to meet the most general electrical requirements established as a starting point for the switching concept developments, not including load switching.

A considerable simplification in the number of switches and in command requirements can be realized by eliminating the electrical isolation requirement on the array switching configuration. All electrical series/parallel combinations of 1-Kv building blocks are still available, but loads will be at some definite potential with respect to all other loads and the ground connection. The electrical position of the ground in the 16 Kv range is still arbitrary with this simpler switching arrangement. The switches in Figure 5 which were used to connect the building blocks electrically in parallel (S_{PL1}-S_{PL15}) are essentially replaced by diodes in the simplified configuration, which is presented in Figure 6.

In Figure 6, there are 15 switches controlling the series parallel arrangement, and 17 switches to select the arbitrary ground point, totaling 32 switches for this configuration (excluding load switches). The ground point could be determined merely by the loads being connected; that is, the return for the ground referenced load is connected to the array, and hence determines the array ground point if that return is grounded at the load. This would reduce the array configuration switching to 15 switches, each of which need only sustain the open circuit voltage of one building block.

The load switches SL1-SL6 in Figure 5 provide for a connect/disconnect function at each terminal of the individual load. Economy of load switching can be achieved by using a common switch in the return paths of several loads and also by allowing this switch to establish the array ground point. Examples of the significant reduction in the number of stacking, ground and load switches that can be achieved when optimizing the general switching provisions of Figure 5 for a specific system design are discussed in Section 6. In Section 6, two representative HVSA systems are optimized for the purpose of providing a base for performance estimates.

5.1.3 SWITCH VOLTAGE AND CURRENT REQUIREMENTS

The maximum voltage that a switch must block when in the open state, the polarity of the blocking voltage, and the maximum current that must be accommodated with the switch in the closed state are of course determined by the specific system design requirements. Representative requirements applied to this study are (1) load switch blocking voltages up to 16 Kv, either plus or minus, since the ground point can be located at any tap point on the string of building blocks comprising the system, and (2) maximum steady-state switch current of 7.5 amperes, since up to 15 Kw must be supplied at voltages in the range of 2Kv to 16 Kv. Determination of the maximum current and blocking voltage capability required of the various switch functions is discussed below.

1. Stacking Switch - This switch is employed between two building blocks which are either in series (when the stacking switch is closed) or in parallel (when the stacking switch is open and coupling diodes parallel the two blocks). As a result, the stacking switch need only block the output voltage of the building block. If the paralleled blocks are of unequal design voltages, the switch must accommodate the higher of the two voltages. The highest current in a stacking switch would occur in a minimum voltage, full power system configuration (7.5A at 2 Kv in this study). As seen in Figure 6, the top 8 building blocks would be paralleled with coupling diodes, the bottom 8 building blocks would also be paralleled with coupling diodes, and the series connection between the two 1 Kv, 7.5A building block arrangements would be made by stacking switch SS8, which must pass the maximum 7.5A.

2. Coupling Diodes - When a stacking switch between two building blocks is closed, the coupling diodes are reverse biased by the building block voltage, which is the maximum voltage that they must accommodate. With several or more building blocks paralleled by coupling diodes to provide sufficient load current, the maximum current through any one coupling diode will approach the value of load current, since the output current of the parallel block to which the load is connected does not pass through a coupling diode.

3. Array Shorting Switch - This switch must be capable of blocking the output voltage of the building block to which it is connected. The maximum current through this switch is the short-circuit current of the solar array associated with the single building block.

4. Load Switch - In the high voltage solar array configuration, the switches that must accommodate the greatest voltage difference across its terminals in the "open" condition are the load switches. The sum of the voltages which must be blocked in the forward plus the reverse directions never exceeds 16 Kv, as can be seen in Figure 7 and 8. Figure 7 shows a particular arrangement with the solar array grounded at the bottom of the lowest voltage building block, thereby supplying only positive voltages from the array to whatever loads may be connected. Switch S1 connects Load 1 to the +16 Kv potential, S2 connects Load 2 to the +8 Kv potential, and S3 provides the return path from the loads to the OV, or ground, potential. The table of load switch voltages in Figure 7 lists the range of possible voltages that can be obtained across the terminals of each switch for the given ground point of connection. It is seen that S1 must block +16 Kv at terminal A with respect to terminal B; S3 must block +16 Kv at terminal B with respect to terminal A; and switch S2 must block up to +8 Kv at terminal A with respect to B, or up to +8 Kv at terminal B with respect to terminal A.

   Figure 8 illustrates a situation where the ground connection is made at the opposite end of the array from that shown in Figure 7, thereby providing only negative voltages to the system. As can be seen from the table of load switch voltages in Figure 8, each switch (S1, S2 and S3) still must block the same voltages at one terminal with respect to the other terminal. Thus, any given load switch must be able to block either +16 Kv in one direction and OV in the other, or +15 Kv in one direction and only +1 Kv in the other, or +8 Kv in one direction and +8 Kv in the other, etc., but never more than a combined sum of forward and reverse blocking voltages of 16 Kv.

   Figure 7 shows a diode representation of forward-biased, "closed" SCR load switches; in the case shown, the loads are obviously powered by positive voltages only. Note that with the array grounded at either end, switches 1 and 3 must be able to block 16 Kv in the forward direction only; there is no requirement to block voltages in the reverse direction at these two switch locations. Switch 2, however, must be able to block 8 Kv in the reverse direction also. Table 1 shows the value of forward blocking voltage and the corresponding value of reverse blocking voltage the SCR load switch must be capable of blocking, depending on where in the array the load connection is made.

The conclusion to be drawn from the preceding discussion is that if a single, general-purpose load switch device were to be developed to accommodate all load point connections, it must be capable of blocking 16 Kv in the forward direction and 16 Kv in the reverse direction. If this development were not feasible, however, two devices could be used to accomplish all the desired load switching. One device must block 16 Kv in the forward direction and 8 Kv in the reverse direction, while the second device must block 8 Kv in the forward direction and 16 Kv in the reverse direction.

The maximum load current that a load switch must pass is 7.5A for the ground rules imposed on this study.

5. Load Return/Array Ground Switch - The maximum forward and reverse blocking voltages and maximum current that the load return and/or solar array ground switch must accommodate are identical to those for the "hot" side load switch: 16 Kv and 7.5A. Additionally, this switch must be able to function as a switch in the closed state with no current through it from the source or load, as described further in Section 5.1.9.

5.1.4 BUILDING BLOCK COUPLING DIODES

Connection of building blocks in a parallel electrical arrangement is required when reconfiguring the HVSA system to supply load currents which exceed the current capability of a single building block. Figure 5 presented a switching diagram showing that a double-pole, single throw switch function is needed to place a block in parallel with the block below it. A subsequent switch diagram (Figure 6) showed the replacement of each switch with two diodes to accomplish the paralleling function.

The electrical requirements on the coupling device to perform the parallel building block connection function are, basically, that it must be capable of blocking the maximum building block output voltage when the blocks are connected in series, and must be capable of passing the maximum load current required from the parallel building block connection (almost 8 amperes).

A transistor switch was considered as an alternate to the use of a diode for the coupling device. In the 8A coupling device application, a quad transistor switch would require about 1100 2 x 2 cm solar cells for operation, including drive power and cells necessary to overcome the series voltage drop. The use of a quad diode arrangement requires only 84 extra cells in a typical 1 Kw building block to overcome the series voltage drop. Additionally, drive circuitry and a command function would be required for the transistor switch. Figure 9 shows the application of both a diode and a transistor for the parallel block coupling function. The requirement for one emitter connection in the coupling device blocking mode and the opposite emitter connection in the paralleling mode show that the transistor cannot perform both functions. The simplicity and minimum power loss associated with use of the diode for this function, plus the conclusion that a transistor cannot function in the required two modes of operation, result in the specification of a diode (or quad diode arrangement) to perform the parallel building block connection function.

5.1.5 SERIES AND PARALLEL CONNECTION OF BUILDING BLOCKS

The semiconductor devices employed as switches and coupling devices introduce small voltage drops in the HVSA system configurations which must be accounted for a sizing the required solar array area.

Figure 10 presents a functional diagram of a portion of the switchable system showing parallel connection of 3 building blocks to supply a load. An arbitrary building block voltage and current of about 1 Kv and 1A have been selected for an example. The components contributing to significant voltage losses between the building blocks and the load are seen to be the load switches, a lumped "IR" loss, coupling diode losses, and blocking diode losses. Each building block will supply the same magnitude of voltage, but the voltage of each block is at a slightly different reference value. This effect is not detrimental, and is rather easily overcome by the system regulation logic scheme proposed in Section 5.2 of this report, which regulates by sensing voltage at the load.

Figure 11 shows a comparable diagram for a load supplied by a series connection of three building blocks. In this figure, the voltage drops are due to the load switches, stacking switches, lumped IR losses, and blocking diodes. As with the parallel connection of building blocks, each block operates at the same voltage magnitude but with each having a different reference point. The selected "up-down" regulation scheme readily accommodates this type of building block configuration, also. A more detailed description of the voltage and power losses associated with each switching function is included in Section 5.1.11.

5.1.6 STACKING SWITCH

Stacking switch current requirements for building block arrangements considered during this study range from less than 1 to almost 8 amperes. The difference in design of a 1 and 8 amp switch is in the number of driver stages and number of solar cells required for drive power. The reliability goal for the HVSA requires the use of a "quad H" arrangement of switch elements to ensure protection against failure.

Figure 12 presents a schematic diagram for one of the four elements of a quad 8-amp stacking switch. The base of the high voltage transistor is back biased by 1 x 2 cm cells and four switches are used in a quad arrangement. A conventional transistor arrangement is used here because it is most desirable for this switch to be normally "OFF", that is, requiring a positive signal to close the switch and thereby connect building blocks in series. An FET-type receiver may be required, however, depending upon the current capability of the LED/Photo transistor combination which is used as the high voltage signal coupler for the switch "ON" command from the spacecraft.

From investigation of typical power transistor parameters, a gain of 3 to 5 provides minimum power dissipation between the sum of $V_{ce\ sat}$ X pass current and base drive power. Accordingly, the stacking switch designs shown provide a base drive of greater than 1.6 amps for the 8 amp stacking switch.

Figure 13 presents a schematic diagram for one element of a 1-amp quad stacking switch arrangement.

A possible SCR switch for stacking is shown in Figure 14. The SCR stacking switch requires less auxiliary array for drive current, but will require more array in the power path due to its higher voltage drop. Another significant problem with the SCR stacking switch is turn-off. It seems quite unlikely that capacitive or inductive commutation circuits could be put on the array for stacking switch SCR turn-off, hence array shorting will have to be used to turn off the stacking SCR by reducing its forward voltage to zero.

The problem of possible SCR turn-on due to dv/dt from regulation or load transients exists, which might result in operational difficulty when building blocks are paralleled and the stacking switch is in the open state.

5.1.7 ARRAY SHORTING SWITCH

The array shorting switch reduces building block voltage to zero for load protection during reconfiguration, load switching, and emergence from eclipse when the possibility of high array voltages exists before regulation can be established. During normal operation of the building block, the array shorting switch is in the open state, and must withstand the maximum output voltage of the building block. The current that the switch must pass is the short-circuit current of the main array in the building block, which has a maximum value of 2.7 amps for the range of building block currents considered during this study. Consequently, the stacking switch described in the previous paragraph will accommodate the array shorting switch requirements and the same quad circuit arrangement is specified.

An estimate of the solar cell open-circuit voltage and short-circuit current as a function of time on emerging from earth shadow is presented in Section 5.3. It will be shown in a following section of this report that rated building block voltage is achieved at a per-cell operating voltage of 0.358 volt, with no regulation switches closed. This voltage may be present in as short a period of time as 2 to 3 microseconds, which requires that the array shorting switch be activated and effectively short the array within this time. Based on the solar cell voltage versus time estimates, the rate of voltage rise at the building block output terminals

may be well in excess of 10^6 volts per second. Therefore, the array shorting switch must not only protect the array components from a higher-than-building-block voltage condition, but must also prevent undesirable premature turn-on of the SCR load switches due to a possible excessive dv/dt condition. Since the drive power for the array shorting switch is supplied by a small auxiliary array having the same relative voltage and current buildup as the main array, a possibly severe design problem exists in that insufficient drive current may be available to activate the array shorting switch before high solar cell voltages are present. The ability of a transistor array shorting switch to safely accommodate this problem is uncertain, and must be established by test to verify the feasibility of a semiconductor switch for this function. The critical nature of this problem may result in the specification of a relay for the array shorting switch function.

5.1.8 LOAD SWITCH

Load switching is an extremely critical function in the HVSA system because of the need to isolate loads until regulated voltage from the source is achieved.

The extremely high voltages (up to 16 Kv) which must be switched is the most significant problem. Load voltages in excess of 2000 volts well exceed present transistor capability and even expected future development.

The semiconductor device which presently seems more capable of this function is the SCR. Application of transistor switching would be relatively simple and represent no serious problems from the turn on/turn off standpoint, but the SCR load switch presents several problems in this respect.

Turn on of the SCR does not appear difficult, although a continuous gating signal may be required if the value of load current is less than the minimum SCR holding current. The LED-fiber optics-photosensitive transistor receiver combination proposed as the HV signal coupler in Section 5.2 would provide the turn-on signal, but prevention of unwanted triggering must be carefully considered. The dv/dt on an output due to regulation switching and especially configuration switching must not exceed the SCR anode dv/dt capability. No large effect on triggering circuit noise problems is foreseen just due to the high voltage presence, although distributed capacitance on the array substrate and the space plasma effects presently represent an area of uncertain interaction with the semiconductor switching functions. Turn-off of the SCR load switch presents a problem. Several possibilities exist which depend upon the acceptability of voltage transients to the load to accomplish turn-off.

1. Capacitive - Figure 15 presents a capacitive SCR turn-off technique. SCR 1, supplying load current, is turned off by the turn-on of SCR 2, which provides a back bias for SCR 1 while the capacitor C1 charges. The load voltage at turn-off is also shown in Figure 15.

2. Load Capacitance - If there is capacitance at the load, and its value can be ascertained, the load switch SCR may be turned off by reconfiguring the array to a lower voltage so that the voltage on the SCR anode drops rapidly, thereby back biasing the SCR due to the load capacitance. This method of SCR turn off is shown in Figure 16. The load capacitance C_L required for a 100 usec time constant is only 0.025 mfd ← This may be true only at 16 Kv; i.e., sensitive to voltages.

3. Series Transistor - A transistor switch in series with the SCR interrupts the current for a sufficient time so the SCR will block when voltage is reapplied. This turn off must be done with the array configured to a low voltage to be within the transistor specifications. The transistor must be turned on again after the SCR is off so the SCR blocks the high voltage when the array is reconfigured. This technique is illustrated in Figure 17.

The technique of method (1) is subject to a serious drawback. A lightweight high-voltage capacitor suitable for mounting on the solar array is presently beyond the state-of-the-art. A consideration for method (2) is that the unknown magnitude of solar cell and substrate to ground capacitances on the array side of the SCR load switch may be comparable to the load capacitance, rendering this method ineffective.

Method (3) appears to be the most feasible approach to configuring the load switch. Use of the array shorting switches to reduce the source voltage to zero would result in a relatively short duration load turn-off time, with an excellent backup to ensure SCR turn-off being provided by the zero-voltage source. This method is proposed for the load switch, with appropriate redundancy to achieve reliability.

Figure 18 presents a block diagram of the redundant load switch arrangement. The switch redundancy features are:

1. Redundant to "close" by the parallel transistors and SCRs.

2. Redundant to "turn off", either by the turn off transistors in series with the SCRs, or by reduction of voltage by means of the array shorting switch located in the building block, both of which cause the SCRs to turn off by loss of holding current, and

3. Redundant to remain "open" by the series connection of the quad SCRs.

A schematic arrangement for an 8-ampere load switch is shown in Figure 19 and a 1-ampere load switch circuit is illustrated in Figure 20.

The transistor gate to the cathode in the "SCRs" provides maximum dv/dt capability of the SCR, to reduce the possibility of spurious turn-on due to regulation switching and reconfiguration voltage transients. The series transistors could be eliminated if knowledge of both the load and "SCR" can assure that the load current will be less than the "SCR" holding current, in which case SCR turn-off would be accomplished by merely removing the cathode gate. The series transistor circuit allows the transistor to be normally on, and the current interrupt function is initiated by the temporary presence of the LED-coupled "OFF" command. The SCR "ON" command is required to provide the gate current for the SCR to ensure conduction if the load current is less than the device holding current.

5.1.9 LOAD RETURN/ARRAY GROUND SWITCH

The block diagram in Figure 5 shows that 17 ground switches (SG1 - SG17) would be required in order to have the capability of placing the ground point at any 1 Kv voltage increment on a representative HVSA sytem having 16 Kv building blocks. Since the loads are returned to the system side of the grounding switch, a critical design problem would exist in that there may be no current through the switch when it is commanded closed, due to the absence of a return to the array from the ground side of the switch. The impact of this condition is that no collector current would exist for a transistor switch and no holding current would exist for a SCR type switch. It can be shown that transistor circuitry can be designed to overcome this problem, but of course the need for the ground switch to accommodate up to 16 Kv across it in the open configuration precludes the use of any present transistor.

While the array could be grounded at 17 different points with the arrangement shown in Figure 5, provided a suitable switching device were available, the final design would probably not require this many ground points, and only those ground switches necessary would be included. Therefore, another approach which could be used is to determine the ground point of the array by the loads connected to it. A switch would be required in the power return lines which are grounded at the load, and this switch may be in a common return line for several loads. An SCR or "gate turn-off switch" would probably be used, since this switch must block both polarities of voltage but pass current only in one direction.

The establishment of a ground reference point for the HVSA requires that a switch function connect spacecraft ground to a particular tap point on the array before the array shorting switches are opened and before the high voltage is applied to the loads.

It is proposed to accomplish the array grounding function and provide load return current with a single switch function, but since the loads are not powered at the time this switch function, a unique requirement on this switch is that it must operate when no load current exists.

Figure 21 presents a functional diagram of a "quad H" arrangement of the load return/array ground switch elements. The redundancy ensures that no single short or open failure will impair the switching function. The load return would be connected at the same terminals of the switch where the ground is shown. A schematic arrangement of one of the quad ground switch elements is shown in Figure 22. The SCR device Q2 and the group of solar cells between Q1 and Q2 provide a current path and sufficient voltage to ensure conduction for the main switch element, Q1, when the gate signal from the "ON" command is present, even with the absence of a current path external to the switch terminals. The transistor in series with Q1 and Q2 ensures cutoff of the main switch element, Q1, by reducing its current to zero with the presence of the OFF command signal. A light-emitting diode is employed as the signal isolator for both the ON and OFF commands from the spacecraft.

5.1.10 HIGH VOLTAGE STACKING SWITCH AND COUPLING DIODE FUNCTIONS

The stacking switches and coupling diode functions considered during the study have had the purpose of connecting a building block electrically in series or parallel, respectively, with another (adjacent) building block. In this application, each device must be capable of blocking the output voltage of one building block only.

In the design of a specific HVSA system, as evidenced by the optimized system configurations discussed in Section 6, it may be advantageous to retain several building blocks connected in series for more than one switchable system configuration. In this case it may be necessary to switch the string of building blocks, requiring stacking switches and coupling diodes which must block voltages higher than the output voltage from a single building block.

The stacking switch and coupling diode voltage requirements therefore exceed the operating ratings (1500 V) for the devices shown for these functions in the single building block applications. Section 5.4 presents the considerations in selecting switch voltage ratings. Consequently, such stacking switches will be a direct adaption of the SCR load switch design, which readily accommodates the higher blocking voltage requirements. The higher voltage coupling diode functions can be implemented by a series connection of several lower-voltage diodes, which is a common practice for obtaining high voltage blocking capability. Of course the SCR load switch design could also be used for this "coupling diode" function, but the complexity and auxiliary array penalty involved with the SCR switch makes the stacked diodes appear to be a better selection. The coupling diode function would be configured as the parallel connection of two stacked diode strings, each diode string having N diodes connected in series. The parallel redundancy protects against open-circuit failure. The number of series-connected diodes, N, will permit possible diode short-circuit failures without exceeding the breakdown rating of the remaining diodes. For the diode total failure rate employed in this study (0.005×10^{-6} failures per hour) and a 9 to 1 short versus open failure rate, the following tabulation presents the total number of series-connected diodes, N, needed to achieve .999999 reliability.

No. of Diodes Needed for Voltage Capability	No. of Additional Diodes for Rel.	Total No. of Series Diodes, N
2	1	3
4	1	5
6	2	8
8	2	10
10	2	12
12	2	14

5.1.11 SWITCHING FUNCTIONS SUMMARY

The following list defines the semiconductor device type and circuit redundancy arrangement recommended for each of the switching functions described in this section.

Function	Implementation
Parallel Connection of Building Blocks	Quad Configuration of HV Diodes
Stacking Switch	Quad Configuration of HV Transistors (normally OFF). Figure 12.
Array Shorting Switch	Quad Configuration of HV Transistors (normally OFF). Figure 12.
Load Switch	Quad Configuration of SCR devices (normally OFF) and Dual Configuration of Turn-off Transistors (normally ON). Figures 18, 19.
Load Return/Array Ground Switch	Quad Configuration of Elements, each having SCR device (normally OFF) and series Turn-off Transistor (normally ON). Figures 21, 22.

Table 2 presents the fundamental electrical operating requirements for each of the switching functions, as well as the maximum power dissipation in the devices. The maximum values apply to the application in the two representative optimized systems described in Section 6.

Table 1. Forward and Reverse Blocking Voltage Combination for Load Switch

Load No. 2 Connection at (KV)	Switch No. 2 Blocking Voltage Capability (KV)	
	Forward	Reverse
0	0	16
+ 1	1	15
+ 2	2	14
+ 3	3	13
+ 4	4	12
+ 5	5	11
+ 6	6	10
+ 7	7	9
+ 8	8	8
+ 9	9	7
+10	10	6
+11	11	5
+12	12	4
+13	13	3
+14	14	2
+15	15	1
+16	16	0

Table 2. Switching Function Voltages and Currents

FUNCTION	MAX. BLOCKING VOLTAGE	MAX. OPERATING VOLTAGE	MAX. STEADY-STATE CURRENT	MAX. POWER DISSIPATION*
Stacking Switch	1500 V	1 V	8 A	8 W
Array Shorting Switch	1500 V	1 V	2.7 A	2.7 W
Coupling Diode	1500 V	1 V	8 A	8 W
Load Switch SCR	16 KW	10 V	8 A	80 W**
Load Switch Turnoff Transistor	1500 V	1 V	8 A	8 W
Load Return/Array *Ground* Switch SCR	16 KV	10 V	8 A	80 W**

* Per device

** SCR power dissipation when blocking 16 KV may range from 16 to 320 W, based on estimated leakage current of 1 to 20 milliampere.

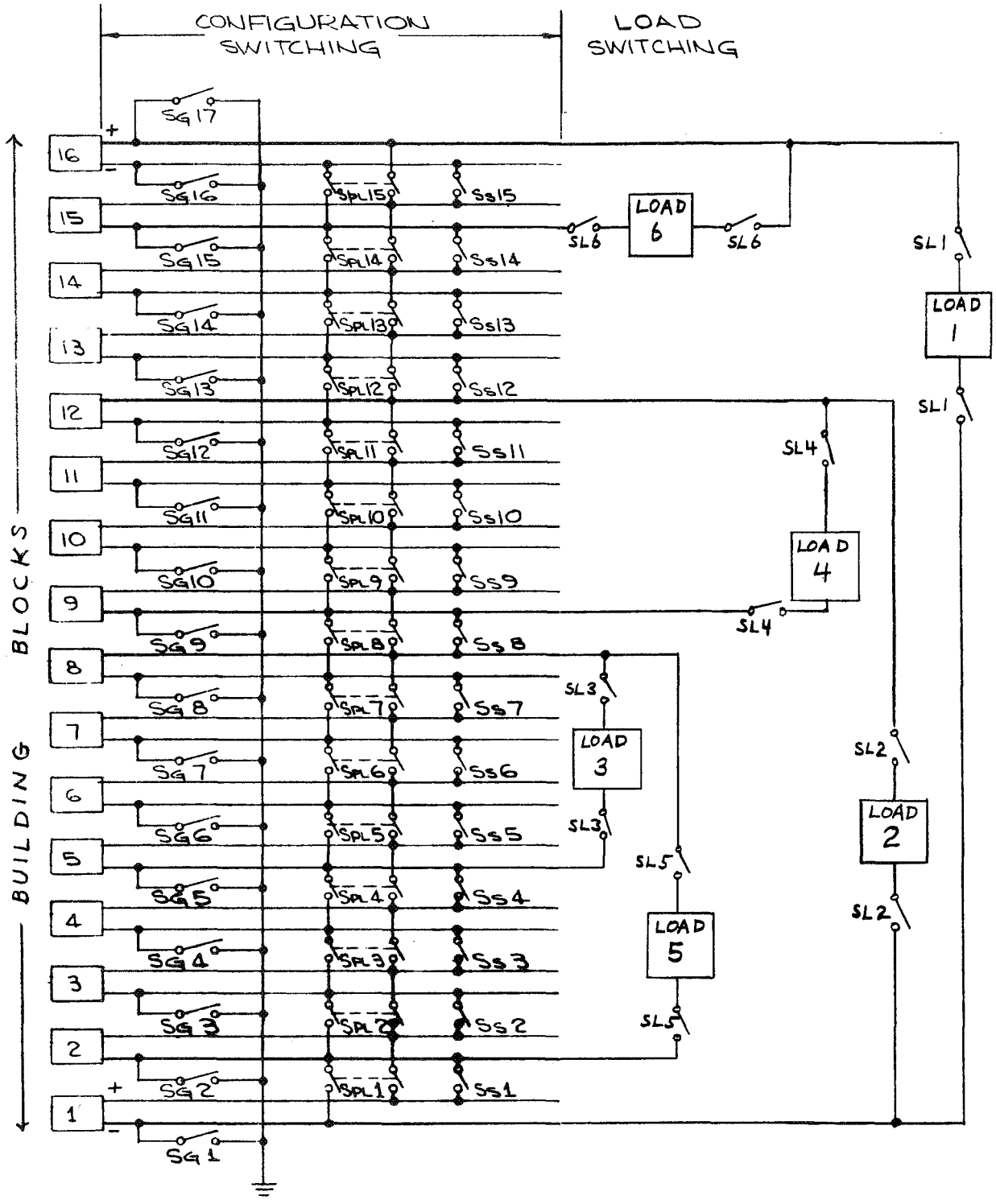


Figure 5. General Case System Switching Block Diagram

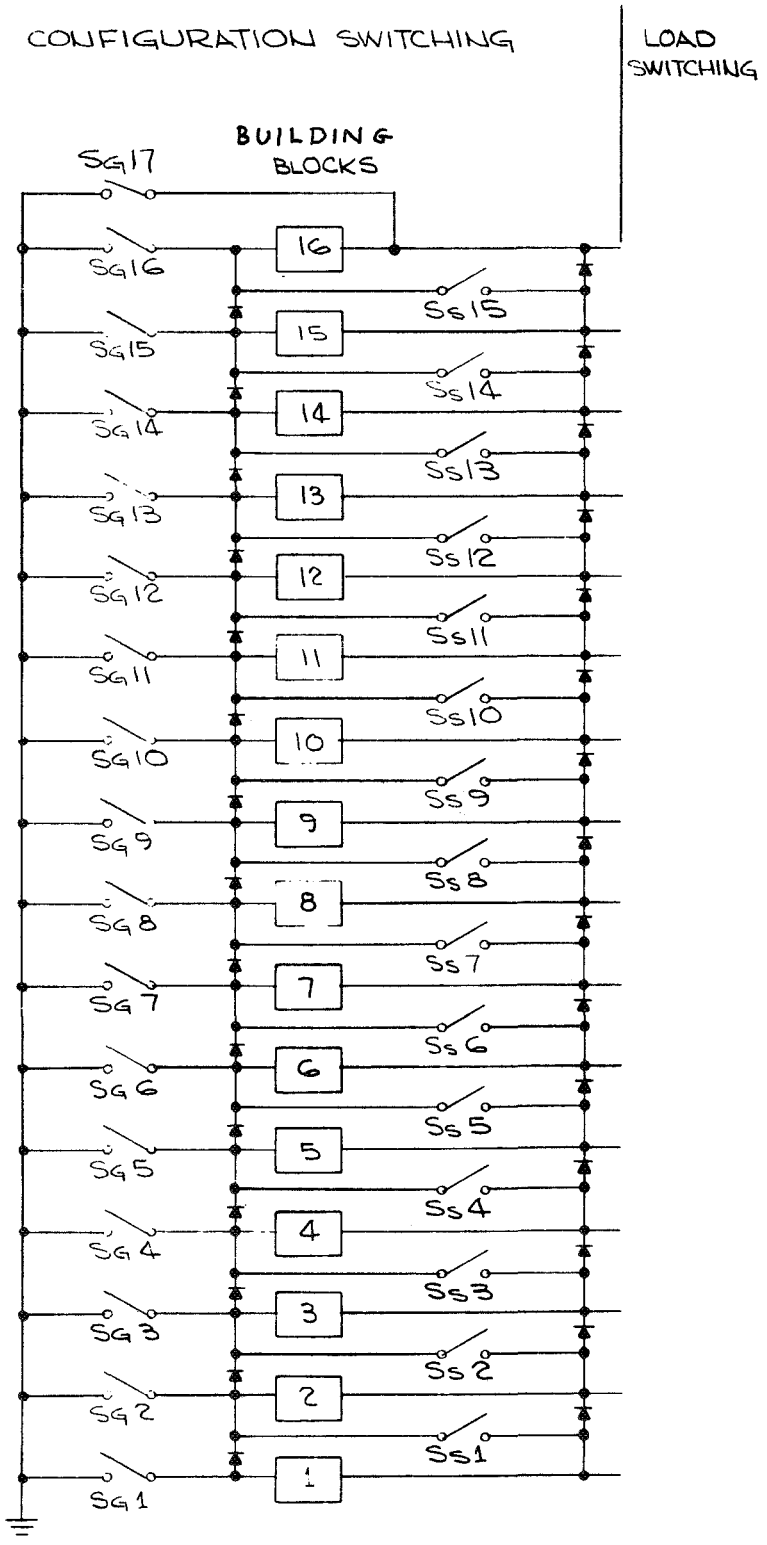
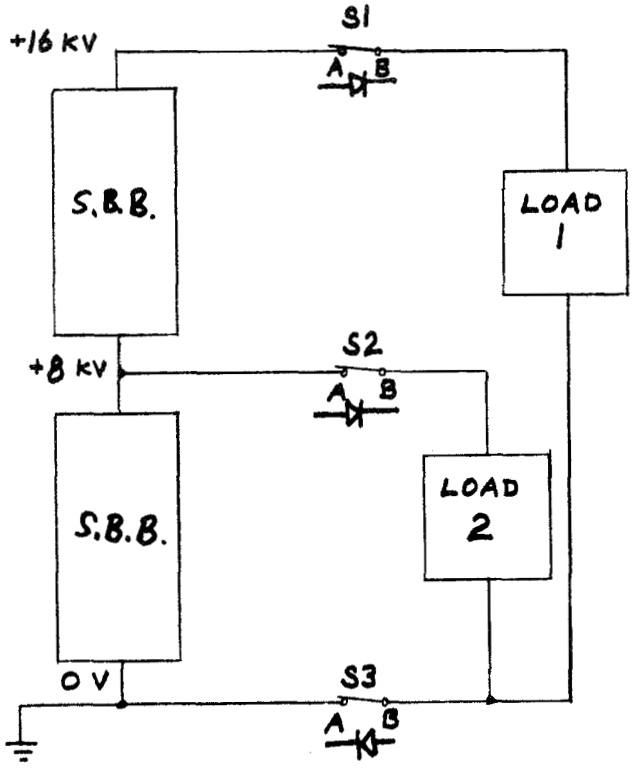
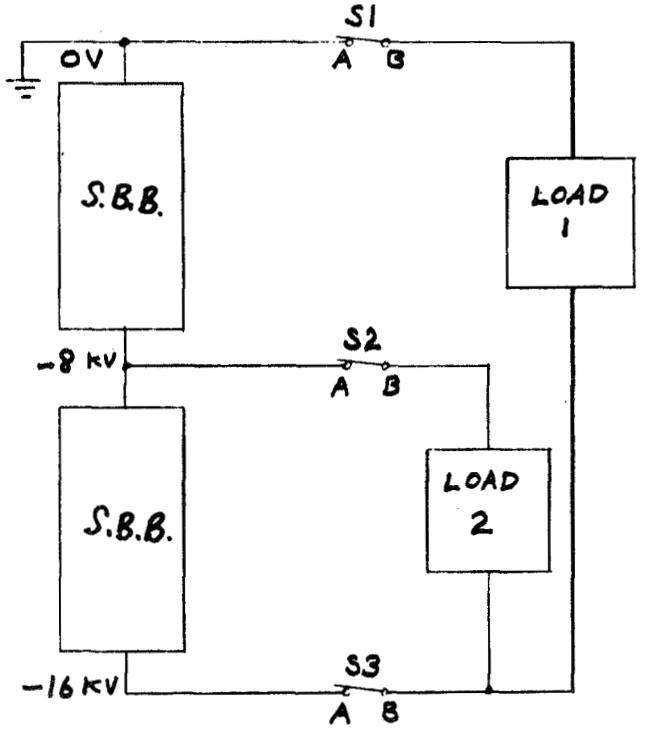


Figure 6. Switching Concept With No Output Isolation Provision



S1 :	closed	Open	Closed	Open
S2 :	closed	Open	Closed	Open
S3 :	Closed	Closed	Open	Open
V1A	+16	+16	+16	+16
V1B	+16	0	+16	0 MIN
V2A	+8	+8	+8	+8
V2B	+8	0	+8	[0 MIN, +16 MAX]
V3A	0	0	0	0
V3B	0	0	+16 MAX	+16 MAX

Figure 7. Load Switch Voltages With Solar Array Grounded At Bottom End



V1A	0	0	0	0
V1B	0	-16	0	-16 MIN
V2A	-8	-8	-8	-8
V2B	-8	-16	-8	[0 MAX, -16 MIN]
V3A	-16	-16	-16	-16
V3B	-16	-16	0 MAX	0 MAX

NOTE: All voltages listed are with respect to ground.

KEY: S.B.B. - BUILDING BLOCKS IN SERIES

Figure 8. Load Switch Voltages With Solar Array Grounded at Top End

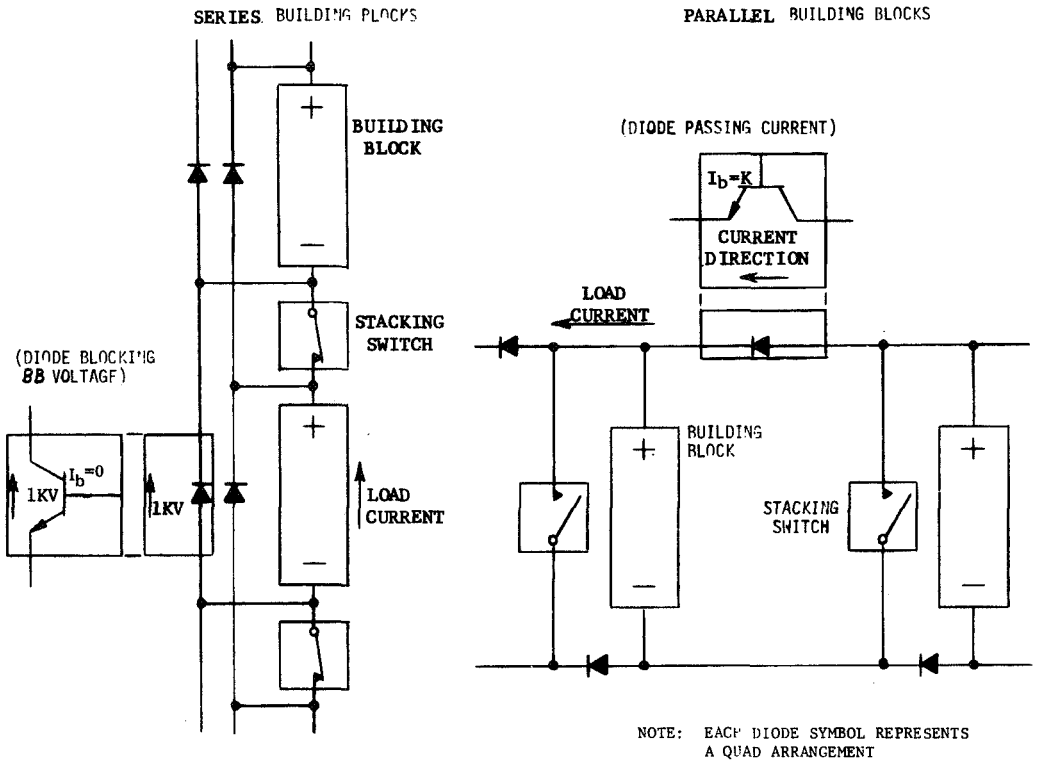


Figure 9. Building Block Coupling Diodes

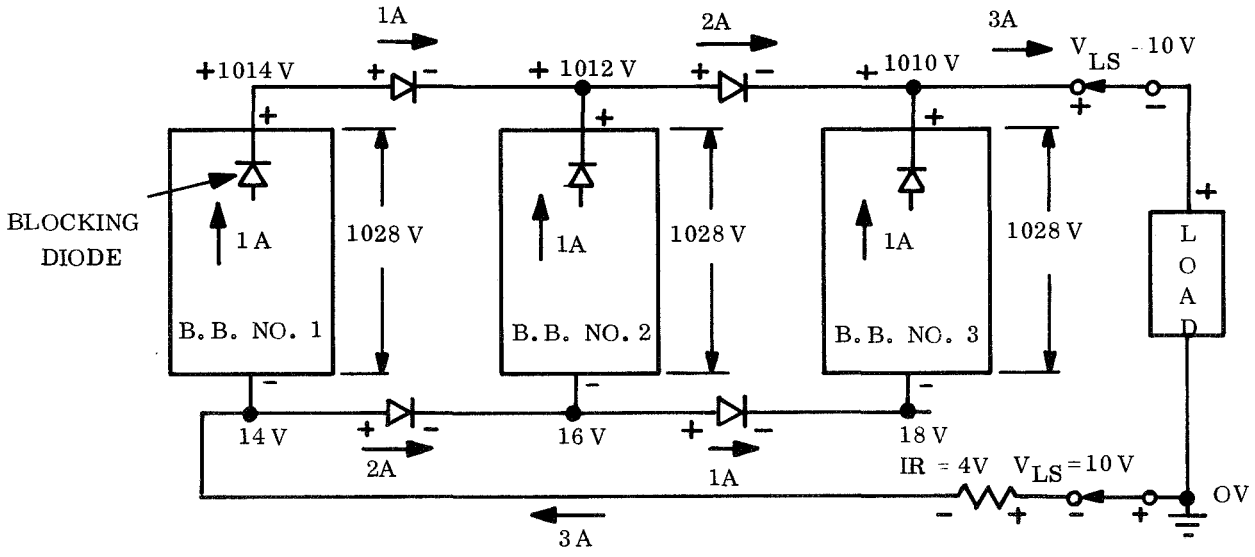


Figure 10. Parallel Connection of Building Blocks (B.B.)

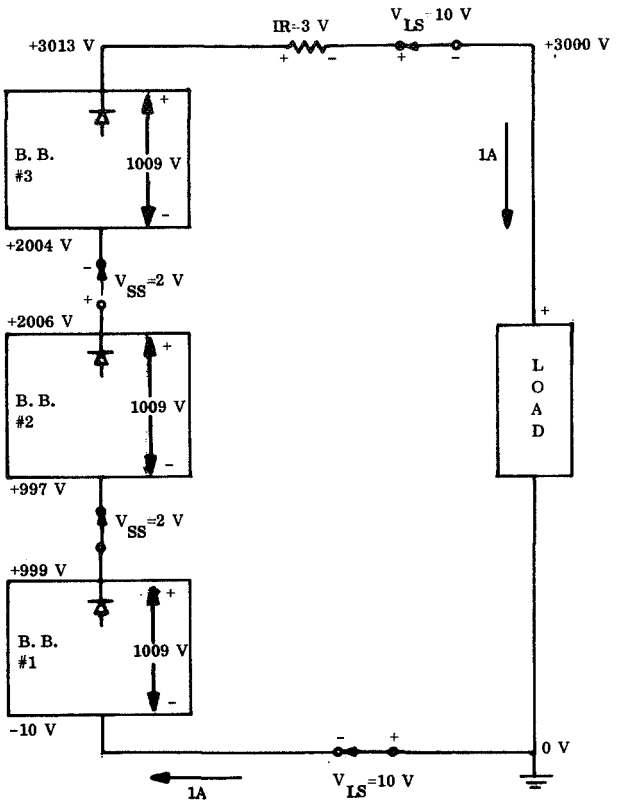


Figure 11. Series Connection of Building Blocks (B.B.)

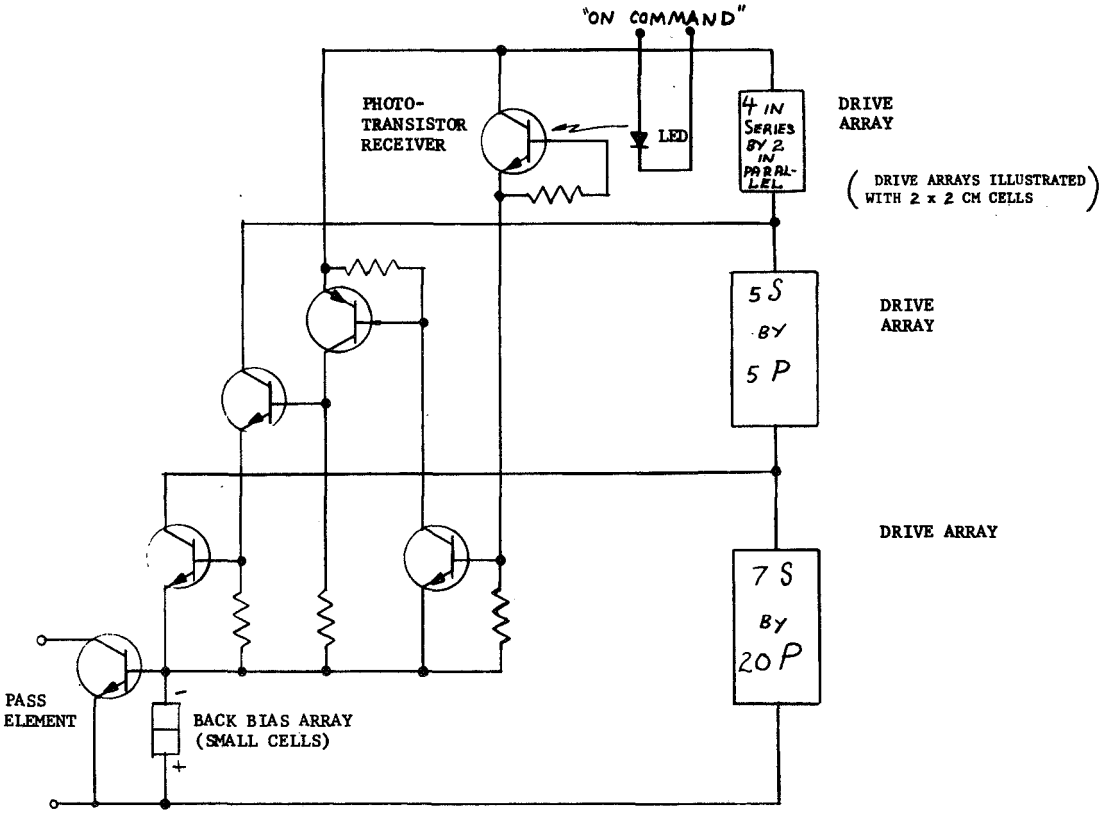


Figure 12. Stacking Switch Element (8 Amps), 1 of 4 in Quad.

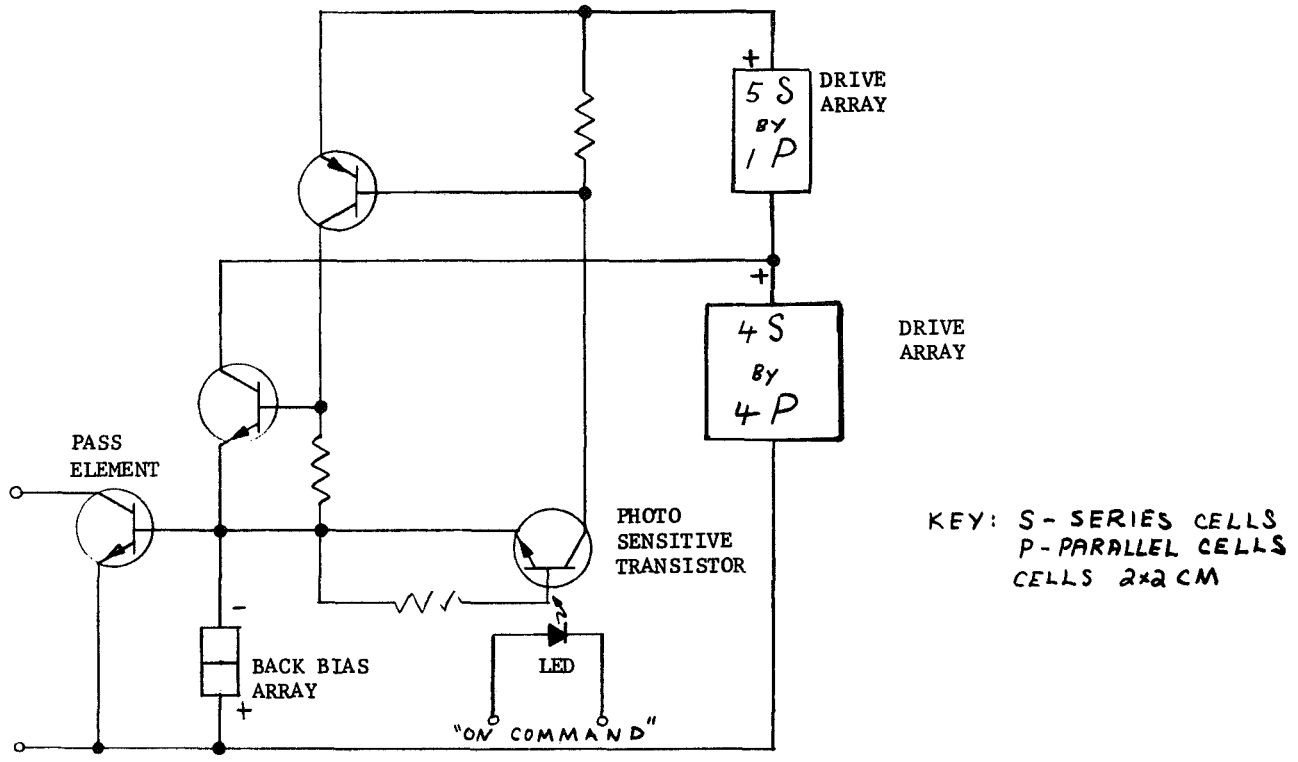


Figure 13. Stacking Switch Element (1 Amp)

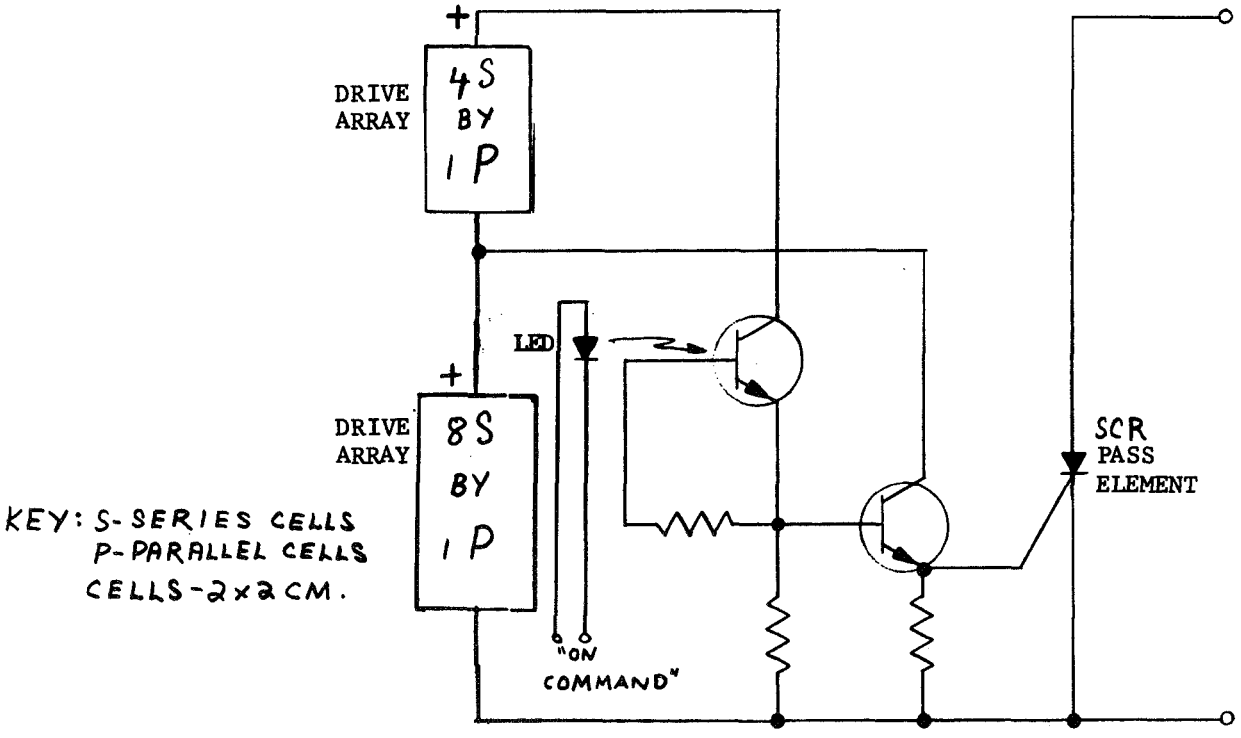


Figure 14. SCR Stacking Switch Element (8 Amps)

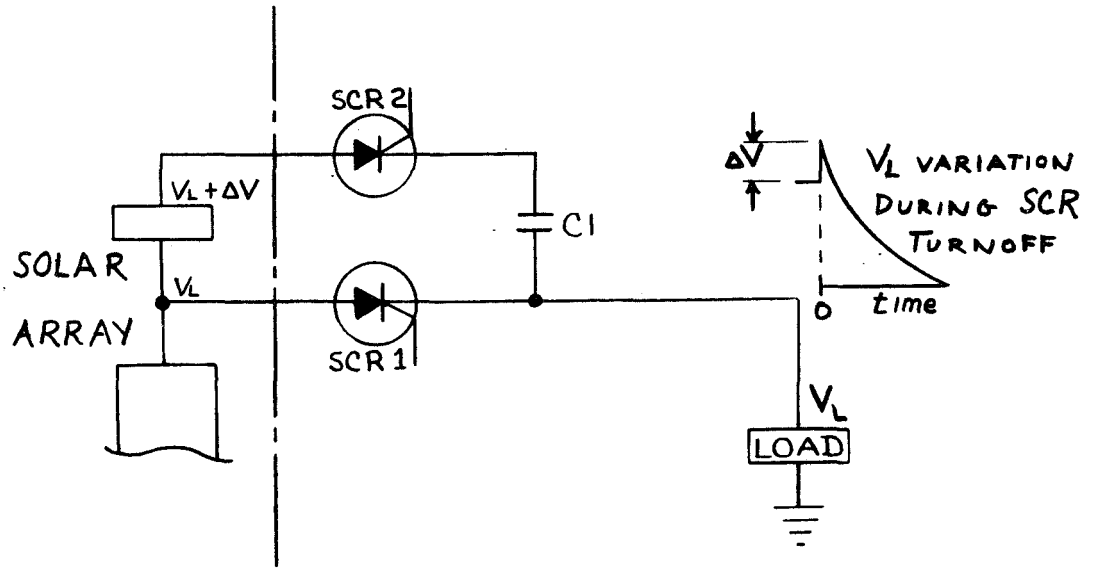


Figure 15. Capacitive SCR Turnoff

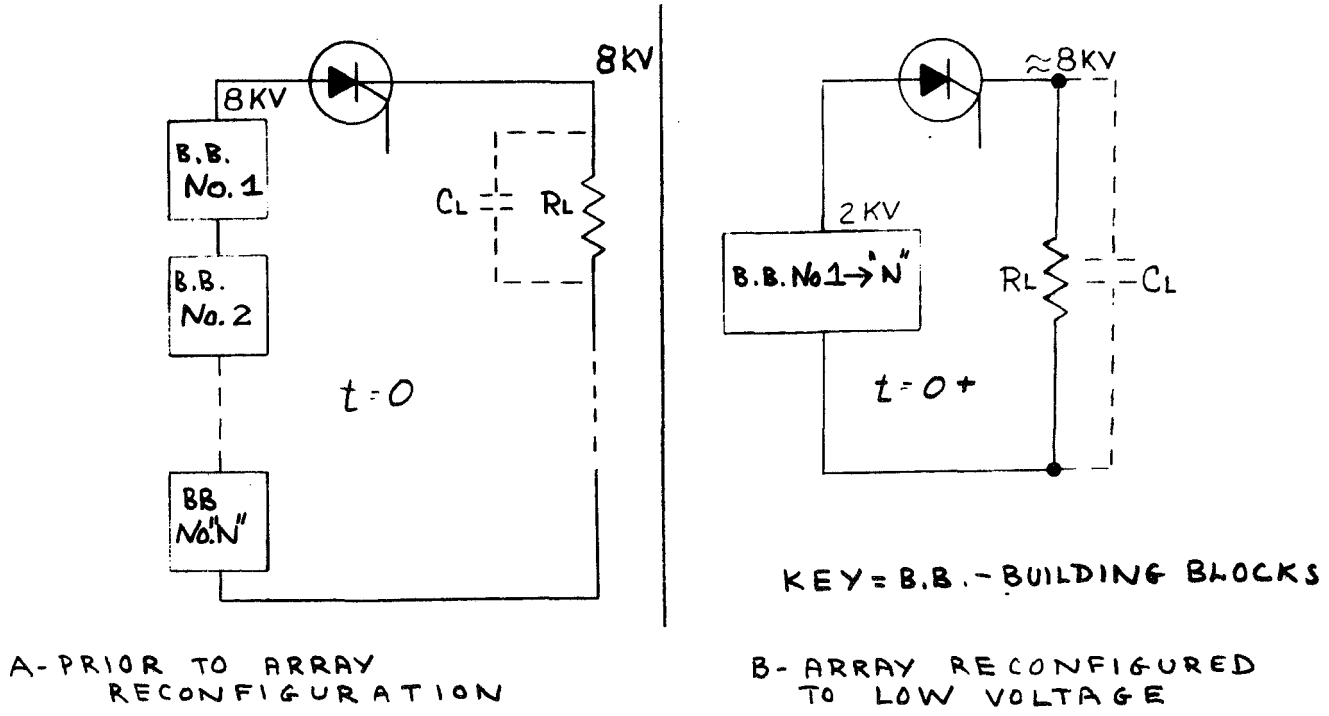


Figure 16. SCR Turnoff By Load Capacitance

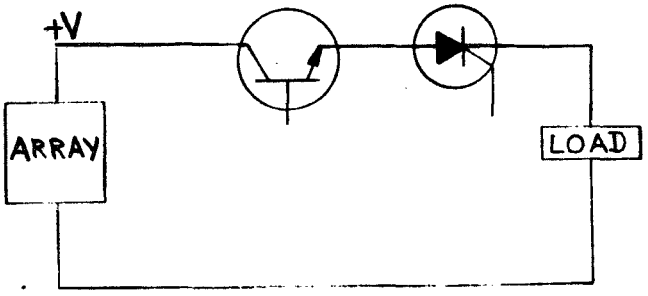


Figure 17. SCR Turnoff By Transistor

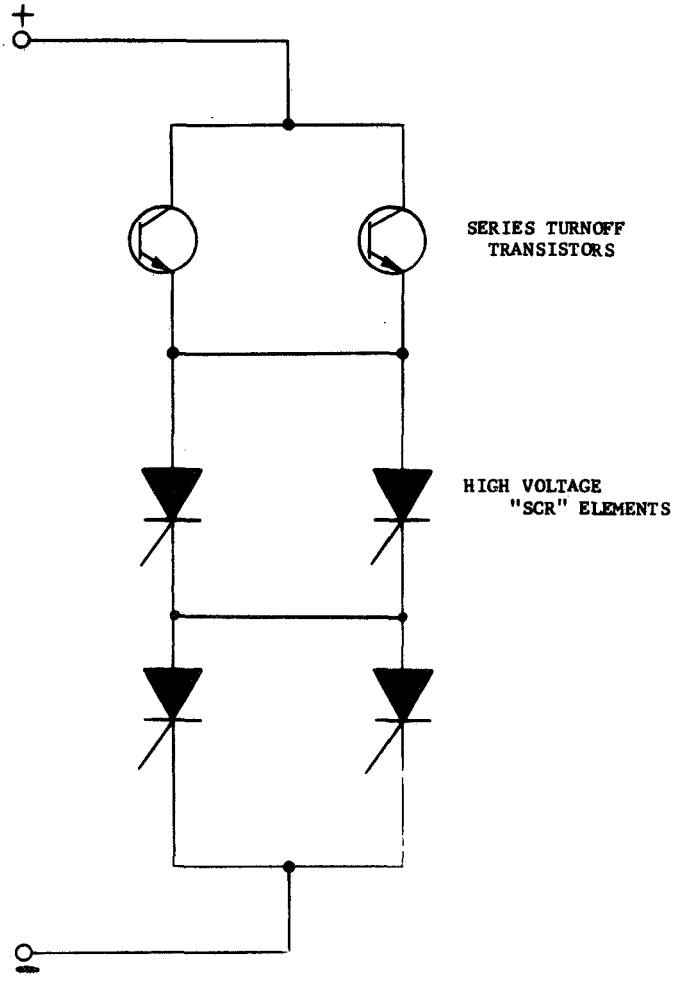


Figure 18. Quad Load Switch

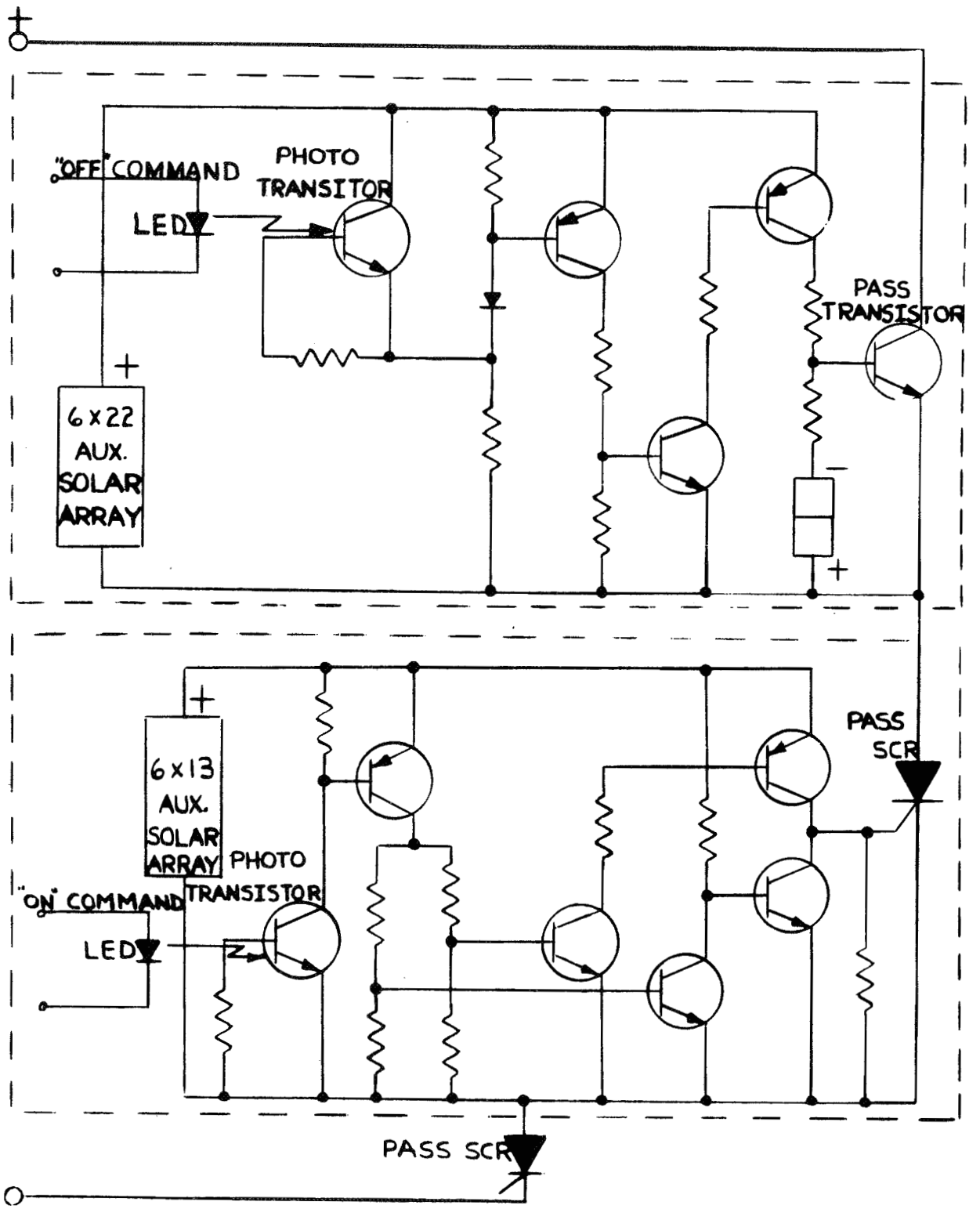


Figure 19. Load Switch Elements - 8 Amps

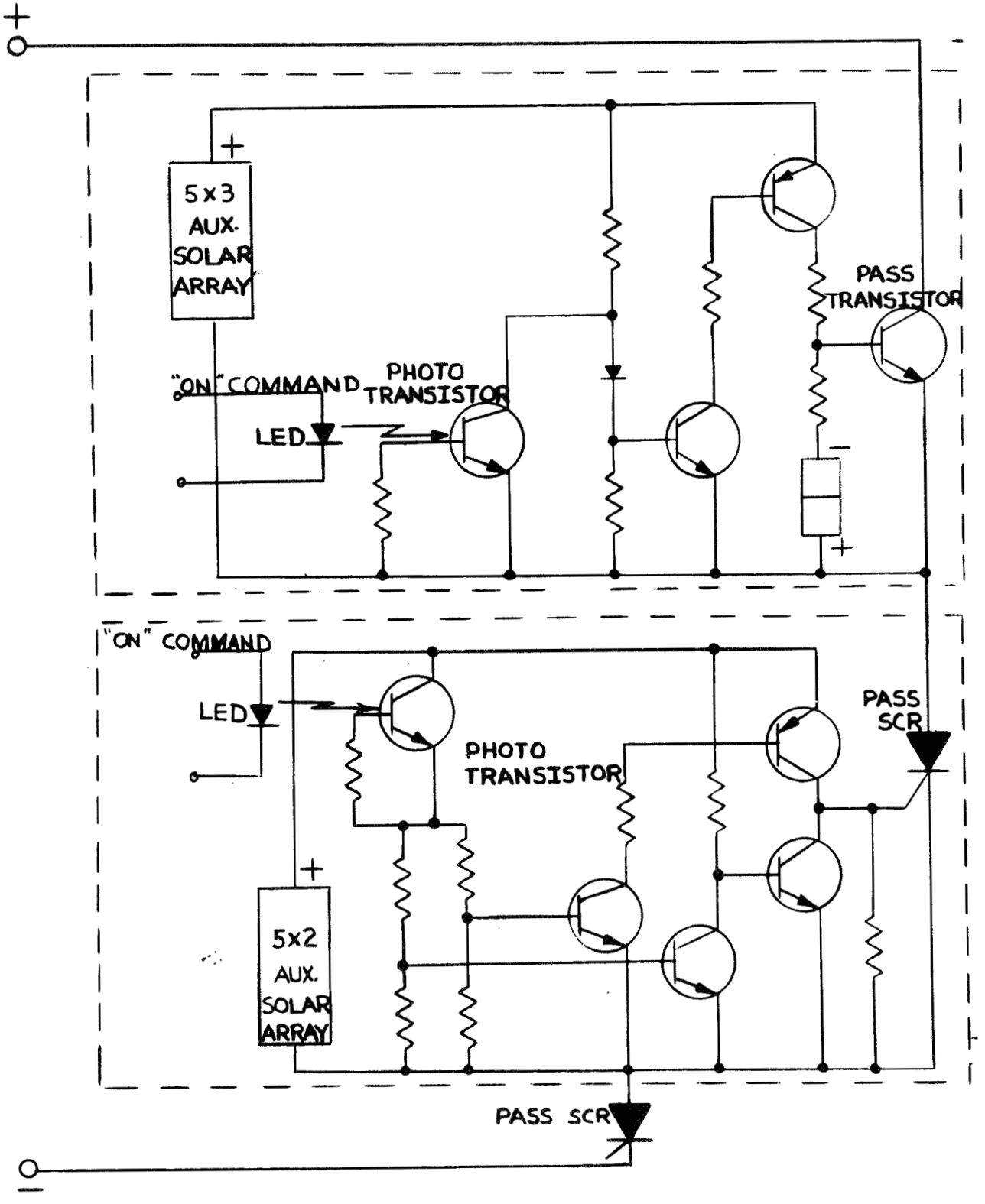


Figure 20. Load Switch Elements - 1 Amp

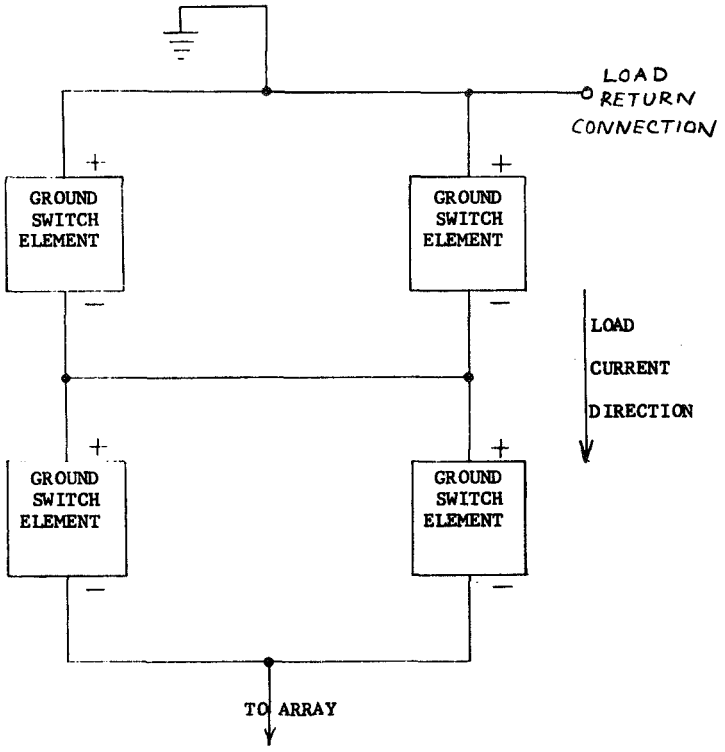


Figure 21. Quad Arrangement of Load Return/Array Ground Switch Elements

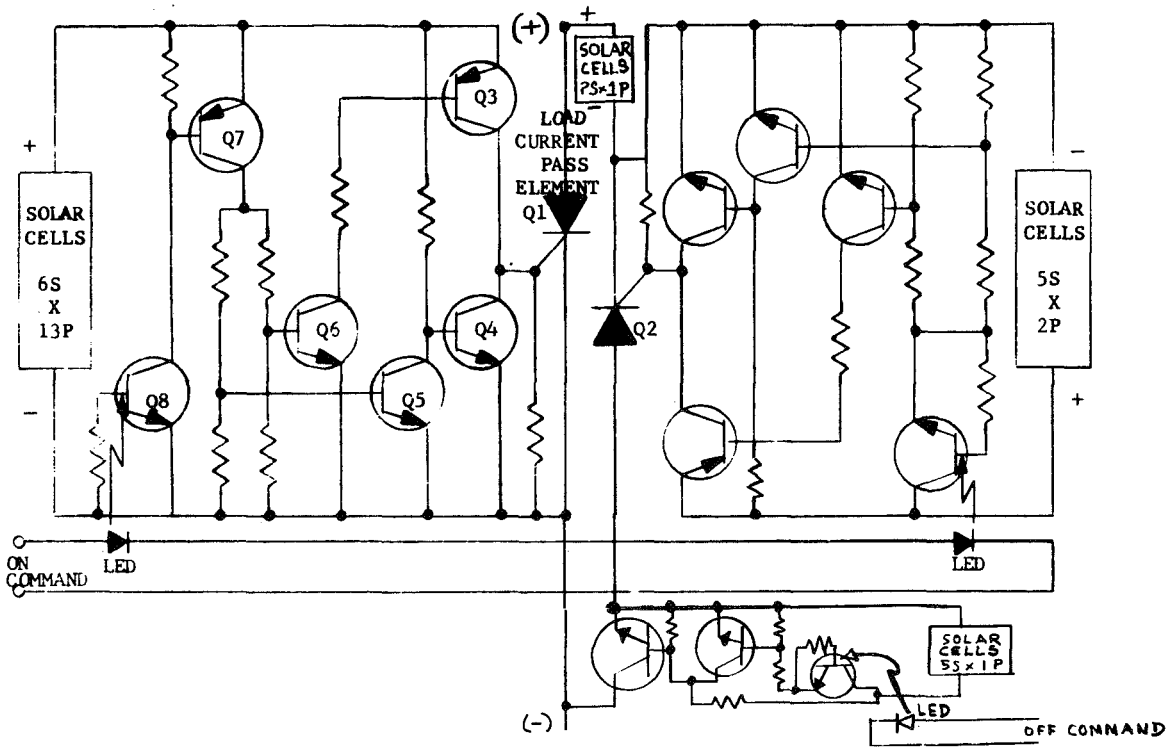


Figure 22. Load Return/Array Ground Switch Element

5.2 POWER CONDITIONING

5.2.1 GENERAL

The power conditioning effort during this study has included consideration of general methods of voltage regulation by discrete switching, circuit techniques to effect discrete switching, selection of a system regulation scheme for the HVSA, impact on circuit design of 0.1% regulation requirement, and methods of coupling signals from the spacecraft to the solar array functions across a 16 Kv interface. Significant impact of the selected design on the system requirements is introduced in the areas of switching voltage transients, switching speed characteristics and signals required from the spacecraft, which are discussed in this section.

5.2.2 VOLTAGE REGULATION BY DISCRETE SWITCHING

Voltage regulation of a current-limited, variable-voltage power source such as a solar array can be accomplished by dividing the source into discrete series-connected increments and short-circuiting the appropriate number of increments to maintain the output voltage at the desired level as the load and source characteristics change.

Figure 23 presents three approaches to maintaining regulation by discrete switching. In method A, voltage is sampled at the load on the spacecraft and this signal is sent to the solar array where the reference and logic circuits determine which of the regulating switches are open or closed, depending on whether the sampled load voltage is above or below or within the allowable deadband of the threshold detectors. Method B employs identical logic and functions as in Method A, except the spacecraft/array interface is now located at the "count up/count down" inputs to the array-mounted counter, with the reference and signal processing functions located within the protective environment of the spacecraft. This relocation of components minimizes the detrimental effects of extreme temperature variations and severe charged particle bombardment on load regulation. Method C differs from A and B in the respect that output voltage V_R can be changed in any predetermined amount rather than in steps equal to the operating voltage of a single solar cell. This is accomplished by loading a storage register/buffer stage on the array with a serial bit stream which defines which regulation switches will be open or closed upon execution of the "change switch state" signal. A somewhat sophisticated computation facility would be needed to predetermine what the new switch state should be to change V_R to a particular value. Knowledge of the existing switch state, not required by Methods A or B, would be employed in the data processing to determine the appropriate voltage change.

The functions required for Methods A and B are identical, and will be discussed in some detail because they represent a feasible approach to discrete switching regulation. A simplified block diagram of this scheme is presented in Figure 24, and consists of a sampling network and a constant voltage reference, an error amplifier that compares these two signals, and two threshold detectors to determine whether the sampled voltage is too low or too high. This circuitry is continuous analog. At most, only one of the threshold detectors will have an output at any instant of time; each detector is connected to its own gate, and in the presence of a detector signal and a clock signal, a counter changes state by one count. The activated detector determines whether the count should advance or decline, at a rate established by the clock. The counter output is coupled to the solar cell shorting switches through driver stages to reduce the power drain requirement from the counter and provide high voltage isolation. The gates, counter, drives and switches operate as digital logic at the clock stepping rate.

The sampling element senses the load voltage and provides a portion of that voltage as an input to an error amplifier. A constant voltage reference level is provided as the second input to the error amplifier. These two signals are compared, and the amplifier difference (error) is applied to the detectors. The detectors compare the error amplifier output with a portion of the voltage reference to determine whether the sampled array voltage is too high or too low, thereby controlling the direction of the counter.

If the error is below the threshold for the Low Detector, its output will allow the Counter to advance, at the clock rate, thereby increasing the array output voltage by removing the short-circuit switch across groups of cells. If the error is above the High Detector threshold, the counter will decline, reducing array output. The difference between the High and Low threshold constitutes the regulation deadband. Within this band, the counter does not change, thereby maintaining the output. By using the same reference for error sensing and thresholds, some reduction of drift errors due to temperature and radiation may be achieved.

The driver and switch block will contain the appropriate switches for shunting the solar cell elements and circuitry for interfacing with the counter. The power supply module provides operating voltages for the integrated circuits as well as the voltage reference.

This general regulator configuration can be used for any type of digital control by proper arrangement of the switches and solar cell circuits.

The following discussion delineates the functional requirements of each element and the major problems expected in meeting these requirements. For each element, a typical circuit is presented using present state-of-the-art devices. Since one common problem exists for all devices used, (the lack of any data at extremely low temperatures) the circuits are designed using the lowest temperature for which data is available. The design temperature range is $-55^{o}C$ ($+218^{o}K$) to $+60^{o}C$ ($+333^{o}K$). The predicted low temperature for the HVSA is about $-170^{o}C$ ($+103^{o}K$).

Another problem common to all devices is that of radiation damage. The effects of radiation will differ with each device and its application. To predict these effects with any accuracy will require precise data on duration, amount and type of exposure. No attempt will be made in the following discussion to include radiation effects in the element designs, although accounting for these effects is critical in a specific hardware design.

5.2.2.1 Sample Element

Figure 25 presents a circuit configuration for the sample element. The sampling element consists of a resistor divider which provides a sample of the array voltage and a voltage follower (unity gain amplifier to reduce the divider output resistance). The divider contains a trim resistor which is necessary to precisely match the nominal sample voltage to the reference voltage.

The large values of resistance in the divider are used to reduce the power dissipated. The 10 megohm will dissipate approximately 98 milliwatts (1 megohm would be 980 milliwatts, etc.). The resulting output resistance is much too high to drive a high gain error amplifier with minimum offset current drift error. Therefore, a unity gain amplifier is used to provide a source resistance for the sample voltage of less than 1 ohm. The drift of this amplifier is added to the sample level, but can be nulled to less than 0.0004% of the sample over the design temperature range. The error due to offset current drift and power supply rejection (assuming 1% supply regulation) will be negligible.

The total error contribution of this element would not exceed 0.0005% out of the 0.1% regulation requirement for the HVSA during this study. The power dissipated would be typically 300 mw.

5.2.2.2 Reference Element

The following minimum criteria should be considered in selecting the reference element: (1) temperature, (2) radiation effects and (3) dynamic response.

The best temperature compensated references presently available have temperature coefficients of $\pm 0.0005\%/^{o}C$. If regulation over the maximum expected temperature range of the HVSA is required, this reference would effectively "use up" more than 50% of the regulation range. This allows almost no effect of the remaining circuit parameters on regulation. Since the direction of this temperature error is not predictable, it is extremely difficult, if not impossible, to compensate.

The effect of radiation exposure on the reference element cannot be predicted with great accuracy; however, it is probable that there will be some effect, resulting in a reference voltage shift. When this is added to the temperature effects, it becomes obvious that available reference elements are not sufficiently stable to provide 0.1% regulation during array warm-up following the eclipse.

Another problem with achieving regulation upon coming out of an eclipse is that of reference dynamic impedance. Since the rate of array voltage increase is very high, a method of maintaining a dynamically stable reference is required. One approach to accomplishing this is with capacitive by-passing, provided

care is taken to prevent oscillation. A solution to the problem of maintaining a constant voltage over the temperature range is to use a temperature controlled reference. This may be accomplished within the HVSA packaging constraints with the same technique used in Fairchild μA726/7 amplifiers (Reference 2). This technique uses a temperature stabilized substrate, where circuit components are kept at constant temperature by an active regulator included on the chip. The regulator consists of temperature sensing circuitry which controls the collector current in a multiple emitter power transistor. As the ambient temperature decreases, collector current is increased thereby increasing power dissipation in the substrate. The use of multiple emitters allows even distribution of dissipated power in the chip. Due to the very small mass, the thermal time constant is very small. Fairchild data indicates a relative chip temperature delta of $-3^{o}C$ (^{o}K) to $+1^{o}C$ (^{o}K) over an ambient range of $-55^{o}C$ ($+218^{o}K$) to $+60^{o}C$ ($+33^{o}K$). Combination of this technique with a compensated reference (such as the FCT 1135) would result in an extremely stable reference element.

In the circuit shown in Figure 26, an amplifier identical to that used in the sample element is used for the reference element. It provides a similar output impedance and elevates the reference to a level matching sample element and error amplifier outputs (above +15 VDC).

5.2.2.3 Error Amplifier Element

This element actually performs two functions; comparison of the sample and reference voltages, and amplification of the difference or error signal. The stability requirement of this circuit is very critical since any drift on the input will be greatly amplified.

The circuit shown in Figure 27 utilizes a temperature controlled differential preamplifier (μA727) driving a low drift, extremely high gain operational amplifier (μA725). The pre-amplifier provides a gain of 100 with drive characteristics very nearly as good as a chopper stabilized amplifier (with much less complexity). Since the input to the operational amplifier stage has been amplified by 100, the affect of its drift on the pre-amplifier is approximately divided by 100. The effective offset voltage drift for this element would be less than 0.5 $V/^{o}C$ ($V/^{o}K$).

The error amplifier was designed to provide amplification of 500, which results in an error signal output of ± 3.35 V over the regulation range. The use of this minimizes the effect of detector offset drift and provides more positive switching of the detectors.

5.2.2.4 Detector Elements

The purpose of the detectors is to compare the amplified error signal to some upper and lower reference levels and provide a logic input to the proper counter gate if either limit is exceeded. The necessary criteria for circuit selection must include high gain, fast response time and low offset voltage.

The circuit in Figure 28 includes both upper and lower limit detectors and counter input gates. The same pre-amp/operational amplifier combination used as the error amplifier will provide very low offsets and temperature stability. In this application, the amplifiers are used in an open loop configuration, resulting in a minimum circuit gain of 100 million. Therefore, an input signal of 0.05 microvolts over the limit will present a logic input to the gate. The capacitive feedback serves to reduce AC gain and stabilize the stage. The size of this capacitor will be determined by the maximum response requirement. Since the open loop gain is so high, it could be reduced to lessen the effect of offset drift on the stage. The magnitude of drift is approximately the same as in the error amplifier, however, the effect on the output will be much greater due to the high gain.

5.2.2.5 Clock Element

The function of the clock is to provide a sampling rate. The actual rate required will be determined by the required transient response of the regulator and the switching speed of the transistors used as switches. If it is necessary to maintain regulation during emergence from an eclipse, the sample rate must be quite high; perhaps in the megahertz range. This would present no problem in the clock design, in fact, a higher rate would require smaller timing capacitors. However, the rate will be limited downstream by the power switches. Therefore, a tradeoff is necessary between required transient response, switching speeds (and efficiency) and, possibly, capacitor size.

A low frequency (5 KHz) clock circuit is shown in Figure 29. The frequency is determined by the values of C, R_1, R_2, and R_3 with temperature compensation of frequency accomplished by using a thermistor for R_2. Since variations in the 15 V zener voltage will affect only duty cycle and not frequency, stability in this device is not extremely critical. The output gate is required to insure the fast switching time necessary for operating Transistor-Transistor Logic devices.

If a clock frequency greater than about 5 KHz is required, it can easily be implemented using a high gain integrated RF/IF amplifier i.e., μA703 which can provide frequencies up to multi megahertz.

5.2.2.6 Counter Element

The counter must control the number of switch elements as a function of commands from the detectors. The rate at which the counter changes state is controlled by the clock and direction of counting by the detectors. This is accomplished by gating the clock pulses to either the UP or DOWN counter inputs through the High or Low gates. If the voltage sample is greater than the upper reference, clock pulses are fed to the down side of the counter which then increases the number of shunted cell elements. If the sample is greater than the upper reference, clock pulses are fed to the up counter which reduces the number of shunted cells. When the error is between limits, the counter does not change state.

An UP/DOWN counting circuit will 11 outputs is shown in Figure 30. The circuit receives clock inputs from one of the detector gates and provides signal outputs to the switch driving circuits. The additional gating shown inhibits the counter when the switch commands are either all open or all closed. This circuit is capable of operation at any counting frequency up to 30 MHz.

5.2.2.7 Power Supply Element

The function of this element is to provide all operating voltages for the digital regulator circuits. An auxiliary solar cell circuit is necessary for this purpose due to the inefficiency of dropping the main array voltage to the required level. The requirements of the auxiliary array would be 32 V at perhaps 0.5 amp. Output regulation is accomplished at two levels using integrated regulators, as shown in Figure 31.

5.2.2.8 Summary

One of the major problems common to all regulator elements is that of operation at temperature below $-55^{\circ}C$ ($218^{\circ}K$). Since no specifications for operation below this temperature have been published, a ground rule which is established for this study specifies that the solar array shorting switch will maintain zero output voltage upon emerging from orbital eclipse until the array components have warmed up to $-55^{\circ}C$. The time required for the array to warm up from its coldest eclipse temperature of $-173^{\circ}C$ ($100^{\circ}K$) to $-55^{\circ}C$ is approximately two to three minutes.

Radiation damage to semiconductors can be very severe for the 5-year HVSA mission. Considerations on providing adequate shielding to minimize the degradation of performance is presented in Section 9.1, Radiation Environment and Shielding.

5.2.3 TECHNIQUES FOR REGULATION BY DISCRETE SWITCHING

To devise a switching scheme to provide regulation, it is assumed that the solar cell voltage is essentially constant for a 1 volt change in the output of a 1000 volt building block (since there are always more than 1000 cells in series to develop 1 Kv, the voltage change per cell is less than 1 millivolt). Accordingly, the change in output obtained will consist of the voltage contribution of those cells added or removed. To regulate within a two volt band ($\pm 0.1\%$), the voltage change should be less than 2 volts but realistically must be less than 1 volt to allow for sampling and reference errors. This results in a requirement that the lowest increment switched is 1 or 2 cells, since the typical solar cell operating voltage is in the 0.4 to 0.5 volt range at steady state array temperatures. Special consideration must be made for the significantly higher output voltage from an unloaded solar cell at the cold post-eclipse temperatures, and will be discussed in this section. The regulation switch techniques that have been studied include non-binary incremental, binary with saturated transistor switches, binary with controlled-voltage switches, binary switching system with linear shunt regulator, binary switching with a digital shunt regulator, and a binary system with saturated transistor switching and a compensated digital shunt regulator.

5.2.3.1 Non-Binary Incremental Switching

In order to obtain a HVSA building block output voltage increment equivalent to 2 solar cells, for example, a switch could be placed across every two series-connected cells in the array. Two methods of accomplishing this switching are shown in Figure 32. A typical value of 1000 V is assumed for the building block, requiring approximately 3000 solar cells in series to provide maximum power from the array at the end of 5 years operation in the synchronous orbit. Of the 3000 cells, about 1300 may be unswitched, since the $-55^{o}C$ solar cell open-circuit voltage is 0.75 volt per cell, and the 1000 V building block limit would not be exceeded. The remaining 1700 cells would then require 850 switches to maintain voltage regulation.

The number of switches required for the technique of Figure 32 could be reduced by using 20-cell blocks after the first 10 switches as shown in Figure 33, and using appropriate logic. This reduces the required number of switches from 850 to 94. The same technique can then be applied to the 20-cell blocks; ten 20-cell blocks, then 200-cell blocks. If this reduction in switches is carried to the optimum arrangement, the switching arrangement is a binary one, that is, each succeeding block has twice the cells of the preceding block. With binary switching the logic is simplified to the least complex and minimum parts in that the controlling logic is the states of the memory flip flops in a binary counter.

Since each regulation switch must be provided drive current, the auxiliary power requirements for regulation increase as the number of switches increases. Since this power is provided by an auxiliary array, the area required for the array is also increased as the number of switches increases. Therefore, minimizing the number of switches reduces the auxiliary array requirements and improves the overall system efficiency and enhances reliability with a significantly lower parts count.

The use of an incremental switching scheme with many switches would minimize the voltage transients incurred when a switch changes state, since a switch would be across only a few solar cells. An arbitrary switching code, such as the Gray code, while changing only one bit at a time (unlike binary, which can change the state of all of its bits for a single count change), does change higher order bits, which would correspond to a change in output voltage of more than one solar cell at a time. Applicability of the Gray code to solar cell switching is rather uncertain, since the value of any given bit in a Gray code system changes as the count changes. This would correspond to a transistor switch being connected across different numbers of solar cells at various times, which does not appear to be a simply-implemented system.

A typical design of a regulation shorting switch in a quad redundant arrangement is shown in Figure 34. A Light Emitting Diode (LED) to photo transistor command interface provides voltage isolation between the command source and the switch. A junction Field Effect Transistor (FET) is used in the circuit because the FET has a low resistance, or is "ON," when no bias is applied to the gate. This element provides a normally ON condition which means all regulation shorting switches will be ON, or shorting, when no command is supplied from the regulator. Since regulation will not occur until sufficient power is available to operate the regulator, the array will always be in a low voltage state after an eclipse. The FET also provides a high impedance receiver to the photo transistor, which has a fairly high impedance output.

Each of the four elements of the quad shorting switch requires auxiliary driving arrays to the base of the shorting transistor. 1 x 2 cm or smaller solar cells can be used for the FET bias and base back bias cells to save area since the current demand is less than 30 milliamps for these cells. When the shorting switch is on, the back bias cells will be pushed into reverse voltage by the base drive current, and using small solar cells minimizes the current loss of reverse biasing these cells. The worst (or highest) current gain required of the output transistor is approximately 3 to 4 to ensure low saturation voltage.

5.2.3.2 Binary Switching with Saturated Transistor Switches

A minimum-parts switching arrangement to provide regulation is to apply binary techniques to remove or insert portions of the array, i.e., use switches which remove 1/2, 1/4, 1/8, 1/16 . . . . . of the array. This is accomplished by shorting series blocks of parallel cells, hence removing that block's contribution to the total voltage. A discrete change of one solar cell can be obtained, therefore, in shorting groups of 0 to 2047 solar cells with only 11 switches.

The smallest number of cells which must be switched is determined by the accuracy requirement, the output voltage being regulated, and worst case (highest) voltage of the solar cells. A 1000 volt building block has been selected as being representative for the HVSA study and the regulation requirement is 0.1%. The maximum worst case (open circuit, cold) solar cell voltage is approximately 0.9 volt. To regulate a 1000 volt block to 0.1% ($\pm$1 volt) the voltage band encompassing regulation is 2 volts wide. If the references, error detector and control were exact, the smallest increment switched could be ≤ 2 volts. But allowing about 1/2 the band for sensing, reference, and error detecting elements, the smallest element switched must be < 1.0 volt. Since the worst case voltage of one cell is approximately 0.9 volts (estimated for -170^{o}C (103^{o}K) array temperature), the smallest increment of which must be switched is one (parallel row) solar cell. The maximum number of series cells which do not need to have shorting switches is (1000 volts/0.9 volts/cell) or 1111 cells, if regulation were to be attempted immediately after leaving eclipse. However, if the array is permitted to reach -55^{o}C (218^{o}K) the maximum per-cell voltage will be 0.75 volt.

Figure 35 represents the switching arrangement for binary control of a 1000 volt array segment. Each block in the figure represents series-connected parallel rows of solar cells with a number in the block indicating the number of cells in series. Block 1 is comprised as shown in Figure 36,

where

V_o = voltage of one solar cell

$I_L = I_1 + I_2 + \ldots + I_n$ (as required to meet load current requirements)

Block 2 is comprised as shown in Figure 37,

where

$V_o = V_1 + V_2$ = voltage of two solar cells

$I_L = I_1 + I_2 + \ldots + I_n$ (as required to meet load current requirements).

Blocks 4, 8, 16 . . . 1024 and 747 are constructed similarly. Each block is either shorted by a switch placed in parallel with it, or allowed to contribute to the output voltage. The block above the 1024 block is the number of cells needed in addition to the binary blocks to provide 1000 volts at rated load at end of life plus margin for failures.

Each change in the binary number (output of counter) causes a change in the states of one or more of the switches in parallel with the binary blocks, but the net result is the addition or deletion of one solar cell row. This is true so long as the blocks are binary; that is, each block has twice the number of series cells of the preceding block. The number of unswitched cells in the main array, shown above the 1024-cell block in Figure 35, need not be a binary number. The electronics to perform most of the binary cell switching will be simple transistor switches. The highest transistor voltage requirement is 500 volts at S11. A quad arrangement, as shown in Figure 34, will provide full redundancy. A basic problem associated with the saturated switch is, of course, the voltage across the transistor when it is in the shorted (closed switch) mode. The voltage drops across the non-ideal switches may have a very significant effect on the system's ability to regulate within the narrow ($\pm$0.1%) tolerance band. This problem is treated further in the discussion of the controlled voltage switch.

An important failure effect which affects regulation capability is solar cell failure. The capability of the binary switching systems depends upon the voltage of each element being twice the voltage of the next lower one and so on. Solar cell failures will change the voltage contribution of a block, hence, altering the terminal voltage change expected when the element is added to removed. Where the block voltage is quite large (>100 volts), with bypass diodes around each small number of series - connected rows, the effect of losing a few series rows would be negligible. Obviously, in the 0.4, 0.8, and 1.6 volt segments, a failure among the cells in these rows will drastically affect the voltage change on closing or opening the

switch across these rows Bypass diodes prevent large voltage losses but will not prevent loss of regulation because the diodes can only provide a limit of approximately 0.7 volts forward drop which is -0.7 volts across the cell, which should be +0.4, or a net change of -1.1 volts. A more practical means of protection may be to put redundant solar cells in parallel in those rows which will be used for the 0.4, 0.8 and even the 1.6 volt regulation element.

5.2.3.3 Binary Switching with Controlled Voltage Switches

The need to obtain precise voltage changes in the switched binary cell sections of the building block is critical to meeting the regulation goal of this study. Precise voltage changes (corresponding to multiples of actual solar cell voltage) are required with each bit since even a seemingly small difference of 0.4 volt per bit (saturated voltage of a quad switch arrangement), when 10 bits change simultaneously, results in an error of 4 volts at the output bus, which is obviously loss of regulation for a 0.1% regulation requirement at 1 Kv. Adding cells above the binary increment number of cells in a regulation block to compensate for the switch drop will not solve the problem, since this compensating cell voltage will change significantly with cell temperature, while the switch saturation voltage is relatively constant. Figure 38 shows a block diagram of a regulation switch circuit which eliminates the effect of the possible series cumulative voltage drop of saturated transistor shorting switches, and ensures that an exact binary voltage change occurs upon a switch opening or closure. Voltage across reference solar cells in the main power stream is sensed and compared to the voltage across the regulation switch in the operational amplifier to maintain the regulation switch voltage at some multiple of one solar cell. This assures a precise binary voltage change at the building block output terminals.

The "Regulation Switch," when closed, "shorts" a series connection consisting of a pure binary complement of solar cells plus 4 additional solar cells. "Regulation Switch" voltage is forced to be equal to the "Reference Solar Cell" voltage via the "Operational Amplifier" feedback network. Thus, with the "Regulation Switch" closed "Regulation Block Solar Cells" (RBSC) output squals "Reference Solar Cells" output.

Prior to "Regulation Switch" closure, RBSC output equals the sum of the binary complement of solar cells plus the 4 additional solar cells which operate at the same voltage as the Reference Cells since all carry the same current. Closing the "Regulation Switch" reduces total RBSC output to a voltage equal to that of the "Referenced Solar Cells" by the feedback action described above. RBSC output changes effectively by the output voltage from the pure binary complement of solar cells.

With this technique, two solar cells are added in series within each binary segment of solar array for each transistor, or a total of four extra series cells per each quad switch, as shown in Figure 39 for a 11-binary-switch, 1 Kv building block. The voltage of each transistor in the shorting switch is regulated to be equal to the voltage of two solar cells in the power stream (reference cells). Figures 40 and 41 present a functional block diagram and a schematic showing circuit components, the reference solar cells, the regulation block, and auxiliary array for a quad redundant arrangement of the controlled voltage regulation switch. LED's are employed as the high voltage signal coupling device to open the normally-closed switches. An operational amplifier is used to drive the shorting switch. The switch voltage is compared to the drop across a block of reference cells at the summing junction to adjust the drive to keep the switch voltage equal to the voltage across the reference cells. Note that the reference cells are part of the output power array, and not part of the auxiliary array. The solar cells will always operate at greater than 0.358 V when delivering power, resulting in a switch voltage of at least 0.716 V, which minimizes the drive power needed from the auxiliary array (compared to saturated switch operation).

The schematic of Figure 41 applies to a regulation switch for a building block having a nominal load current capability of 0.9 ampere. As will be shown in Section 6, building blocks with maximum current requirements of 0.1A and 1.75 are also used to configure a representative HVSA system. The weight and area penalties associated with the regulation function can be minimized by a "custom design" of the regulation switches for the particular building block requirements.

Although the lower-order binary switches do not require the same high voltage blocking capability of the higher order switches (up to 1000 volts for the 12th binary switch in a 1.5 Kv building block), the same components and circuit design are recommended for all regulation switches in a building block to minimize the number of different devices which must be developed or qualified for the discrete-switching HVSA concept.

5.2.3.4 Binary Switching Enhanced with Linear Shunt Regulator

One technique which would compensate for the effects of saturated transistor switch voltage drops, provide more linear control of building block output voltage and higher frequency response, is to use an analog shunt regulator instead of shorting switches for the lower 3 bits in the binary switching system. Figure 42 shown the regulation elements and the interface from the error detector to the analog shunt regulator element. The analog regulator will control several more than twice the number of series cells representing 3 bits so that at zero output voltage error, the shunt regulating element will be a 50% of its voltage capability, providing a voltage transient capability equal to that of 3 bits (7 solar cells) of either polarity. The nominal design would permit the analog regulator to operate only plus or minus 40% from the nominal (zero output voltage error) 50% operating point, thus avoiding saturation and cutoff of the regulator, providing linear operation and somewhat faster response time. The 40% voltage range deviation from the regulator midpoint corresponds to a building block output voltage deviation which is at the limit of the up or down detector deadband threshold, so that a digital regulation switch correction to output voltage is initiated for any greater deviation of output bus voltage. Figure 43 illustrates this concept: if an output bus voltage deviation would tend to cause the analog regulator to operate below 20% or above 80% of its voltage range capability, the voltage correction would be made digitally, which would return the analog regulator voltage to near its nominal (50%) point of operation.

It is recognized that power dissipation associated with a shunt regulator may be a significant problem since the array-mounted microelectronic components are heat-sink limited in regards to handling power. Power dissipation on a per-regulating element basis could be minimized and reliability enhanced by using parallel solar cell strings in the reference loaded cell block and in the regulated cell block for the lower 3 bits. A shunt regulator element could be used with each of the parallel strings, isolating possible failures by the use of blocking diodes in each string, as shown in Figure 44.

5.2.3.5 Binary Switching with Digital Shunt Regulator

Another type of controller for the 3 least significant bits in a binary regulation scheme is shown in Figure 45. The three bit signals shown represent the three lowest outputs from an 11-bit counter which would normally activate the three lowest value digital regulation switches. Thus a digital interface is maintained: the voltage across the shunt regulator element corresponds to the voltage across the three least significant digital switches in a binary system, and regulation is still maintained by discrete voltage changes in the three lowest value solar cell blocks. However, an important advantage is obtained with this "incremental" shunt regulator, compared to a binary switch system. The signal obtained from the "reference" solar cell block, in conjunction with feedback from the regulator output, is used to ensure that the voltage change across the regulator in response to an input "bit" signal is an exact multiple of an actual solar cell operating voltage, as is required for proper operation of a binary regulation system. Without this feature, as in an uncompensated switching system such as described in paragraph 5.2.3(b), the voltage change upon a switch closure is not a multiple of actual cell voltage because the saturation voltage of the shorting switch prohibits a zero-volt short.

5.2.3.6 Binary System with Saturated Transistor Switching and Compensated Digital Shunt Regulator

Another approach to compensating for the voltage drop across shorted regulation switches is shown conceptually in Figure 46. Precise binary voltage regulation in response to signals from the 3 least significant bits from the counter is accomplished exactly as shown in Figure 45. In addition, the shunt regulator will provide a voltage correction for each of the remaining 8 higher order digital switch voltage drops. The switch compensation network shown in Figure 46 provides a signal to the shunt regulator operational amplifier which is proportional to the number of higher-order closed switches. Sensing of the reference solar cells allows the compensation network to provide a signal which accounts for the fact that switch saturation voltage is a function of load current. Since the voltage sensed across the reference solar cells is also affected by solar cell temperature and the switch voltage is not, the partial regulator shown in Figure 46

removes the effect of cell temperature from the compensation signal presented to the shunt regulator. Note that this technique requires that solar cell temperature be sensed, which is not required with any of the other regulation techniques considered during this study.

5.2.3.7 Regulation With Lower Values of Building Block Voltage

Allowing 0.1% of the 0.2% regulation band (±0.1%) for reference and sampling error, building block output voltage changes per switch change must be less than 0.1% of the output voltage. Assuming a regulation switching scheme which switches a single solar cell at a time, the minimum output voltage which can be regulated is therefore 1000 times the maximum solar cell voltage. Assuming an initial cell voltage of 0.75 V (open-circuit voltage at a cell temperature of (218°K) -55°C), the minimum block voltage that can be regulated to ±0.1% is 750 volts. This applies to the six discrete switching techniques described in the preceding paragraphs (a) through (f).

The lower building block voltage restriction of 750 V for 0.1% regulation is mandatory only when the lowest bit causes an output change which is equal to the operating voltage of one "whole" solar cell. With a linear, digital, 3-bit shunt regulator replacing the 3 lowest-order switches in a binary switching scheme, such as shown in Figure 45, the output voltage change corresponding to a single count change can be a fraction of the voltage of a single solar cell. However, the fourth bit would have to consist of an integer number of solar cells (since the fourth bit is a conventional shorting switch). If the fourth bit were only a single cell, the voltage change in the first, or lowest, bit would be one eighth of a cell, in a binary system. Again assuming a maximum solar cell voltage of 0.75 V, a one-bit change would result in a building block output change of about 0.094 volt, and a permissible building block voltage of as low as 94 volts with 0.1% regulation. However, such low voltage changes would be difficult to assure from a design viewpoint because the operational amplifier off-set drift and shunt regulator element gain changes due to the expected temperature range and radiation exposure would probably prevent a design for voltage changes in the millivolt range under worst-case conditions.

5.2.4 SELECTION OF HVSA SYSTEM VOLTAGE REGULATION METHOD

The various building block voltage regulation methods that have been described in the preceding paragraphs include:

1. Non-binary incremental switching
2. Binary system with saturated transistor switches
3. Binary system with controlled voltage switches
4. Binary switching with linear shunt regulator
5. Controlled voltage binary switching with digital linear shunt regulator
6. Binary saturated-transistor switching with compensated digital linear shunt regulator

For lower voltage applications (V_{BB} less than 750 V) the switching systems must be augmented with linear regulator sections in the building block if 0.1% regulation is to be achieved (item 4, 5 and 6 above). The linear regulators can provide analog output voltage control or can produce output voltage incremental changes which are a fractional part of a solar cell operating voltage. Since the highest solar cell voltage, when regulation is required, is 0.75 volt (beginning-of-life, 218°K(-55°C)), the lower building block voltage limit of 750 V is defined for systems where the smallest voltage change is that of a single cell and 0.1% regulation is required. Power dissipation in the shunt regulator elements can be kept acceptably low (less than 3 W per element) by the use of smaller area solar cells (2 x 2 cm) in the regulator array section, and employing one regulating element for each parallel string of series-connected solar cells. The efficiency of a shunt regulator-augmented system is slightly lower, and the additional circuitry required will probably somewhat reduce system reliability, but where 0.1% regulation is specified for a low output voltage these alternatives must be considered.

The non-binary incremental switching system (item 1 above) is the only system that can eliminate large switching voltage transients on the output bus while regulating (see Section 5.2.6 of this report for a discussion of switching voltage spikes). Placing a switch across each series-connected solar cell would of course eliminate the voltage spikes caused by switching a much larger binary segment of cells. The obvious drawback of the incremental switching system is the extremely large number of switches required (approximately 2200 for a 1 Kv building block). The reliability of such a high parts-count system would probably be significantly decreased, and the efficiency penalty involved with providing drive power for all the switches is very severe (approximately 0.3 ft^2 of auxiliary solar array area is required for a quad regulation shorting switch).

Methods to reduce the number of switches required to perform the regulation function have been described previously. As the reduction is carried to the optimum condition (fewest switches), the binary switching scheme results, and is represented by item 2, above, where the shorting switch (transistor) is either cut off (switch open mode) or saturated (switch closed mode). The disadvantage of this technique is that the saturated transistor is not an ideal, zero-voltage switch. Therefore, in a binary system when for example, the lower ten switches are opened and the eleventh switch is closed (representing a desired output voltage change from 1023 shorted cells to 1024 shorted cells) the actual output voltage change is that caused by one solar cell plus the saturated voltage of 9 transistors. Such a resultant voltage change would be about 4 volts (with quad transistor switches), which can be much greater than the required regulation tolerance.

The switch voltage drop problem discussed in the preceding paragraph is eliminated with the use of controlled voltage switches in the binary system. Figure 41 presented a circuit approach to achieve switch voltage control. Basically, the shorting switch (quad transistor arrangement) is connected across the required binary number of solar cells plus 4 solar cells. When the switch is shorted, its voltage is maintained precisely at the operating voltage of 4 solar cells, resulting in an exact binary cell voltage change.

Although a 10-bit binary switching scheme provides a count greater than 1000 ($2^{10} = 1024$) and therefore a single switch change is less than 0.1% of the total voltage, 11 binary switches are required to regulate a building block to 0.1% over the temperature range from $-55^{\circ}C$ ($218^{\circ}K$) to the high temperature steady-state value. This condition is determined as follows:

1. Example: Desired Building Block Output Voltage = 750 V
2. End-of-Life Solar Cell Maximum-Power Voltage ($+43^{\circ}C$) ($+316^{\circ}K$) = 0.358 V
3. Minimum Number of Solar Cells Required = $\frac{750}{0.358} = 2100$
4. Number of Unswitched Cells with 10-Bit System = 2100 - 1023 = 1077
5. Building Block Voltage at Beginning-of-Life at $-55^{\circ}C$ ($+218^{\circ}K$) with 10 binary switches shorted = 1077 x 0.75 V/cell = 808 V

Since the building block voltage can be higher than the desired value of 750 V, another switch, for a total of 11, is required to maintain regulation.

The minimum building block voltage capable of being regulated to 0.1% with a binary switching system is 1000 x V cell max or 750 volts for regulation starting at $-55^{\circ}C$ ($+218^{\circ}K$) (all allowing one half the $\pm 0.1\%$ regulation band for sensing and reference errors). This corresponds to a binary shorting regulator which adds one cell with the first bit and 1024 cells with the 11th bit and has approximately 50 non-switched cells. By adding in series the appropriate number of non-switched solar cells, the building block voltage can be raised to 1340 volts. Above 1340 volts, the 11-switch binary arrangement cannot be used because the block of unswitched cells which is needed in addition to the 2047 cells in the regulator to supply 1340 volts at end of life provides more than 1340 volts at $-55^{\circ}C$, beginning of life. Thus, a building block voltage of 750 to 1340 V can be obtained with the same 11-switch binary regulator design. Extra cells which are added to compensate for blocking diodes, coupling diodes, and reliability do not change the regulation design since they are added to overcome known (or allowed) losses and do not raise the theoretical output voltage.

To obtain building block voltages above 1340 volts with a binary switching concept, one of two alternatives may be selected. An 11-switch system with a base 2 can be used (the first switch shorts 2 cells instead of 1), but in order to maintain the 0.1% regulation requirement the minimum building block voltage for this system is 1500 V. The upper voltage limit for this system is 2680 volts. A 12-switch binary system can be used to accommodate the 1340 to 1500 volt range. This would permit 0.1% regulation, but at a slight loss in efficiency. The 12-switch binary system can also regulate up to a maximum limit of about 2700 V, with a single cell change per switch change. While the 12-switch binary system and the 11-switch binary system with a 2-cell base can functionally regulate the higher voltage building blocks, the higher voltages would require higher rated devices for the shorting and stacking functions. Both these switches must be capable of blocking the output voltage when in the "OFF" condition.

The stringent voltage regulation requirement of 0.1% is feasible with the discrete switching techniques, however, two fundamental operating conditions can significantly degrade the regulation performance of the proposed digital regulating scheme:

1. Instability of the voltage reference when exposed to the extreme temperature and charged particle radiation environment

2. Operation over a wide current range with variable in-line voltage losses between the source and the loads.

These two problems were recognized and discussed at the Mid-Term Presentation. It was concluded that the severe environmental effects on the voltage reference could be avoided by locating the required precision reference in the controlled environment aboard the spacecraft, and supplying any required reference signal to the array by means of the on-board computer or other type of spacecraft/array interface.

To compensate for the effect of line voltage drops on load regulation, the load voltage must be sensed at the load.

A sensing network (a precision resistive voltage divider) at each load would supply a continuous voltage signal to the voltage reference electronics for comparison to the controlled environment precision voltage reference.

Either "Method B" or "Method C," described in Section 5.2.2, can be utilized to overcome the two problems of line drop and reference voltage protection. The relative advantages of these two methods of regulation by discrete switching are not very well defined at the level of spacecraft interface studies considered during this effort. Method B will be tentatively selected as being representative of feasible regulation methods because it appears to present a somewhat less complex spacecraft/array interface, requiring only an up-count or down-count signal input to the counter, with no switch-state feedback to the spacecraft-mounted logic functions.

A functional block diagram for the recommended discrete switching regulation system is shown in Figure 47. The preferable signal arrangement between the spacecraft and the array would be two low-level logic lines (count up, count down) to accommodate voltage-isolating digital signal couplers. Basic operation of the system would be as follows. A pulse on the up-count line (initiated by sensing a low-voltage condition at the load) would cause an increase in array output voltage by commanding the binary regulation counter on the array to change the state of the digital regulation shorting switches, effectively placing more solar cells in series with the array. Two up-count pulses would provide twice the voltage increase at the array output. Likewise, pulses on the down-count line would cause a reduction of array output voltage. The pulse width would be determined by the logic selected for use on the array. The pulse repetition rate will be limited by the switching speed of the regulation switches. The counter will be (1) operated at the spacecraft ground potential, with high-voltage (up to 15 Kv) signal coupling between the 11 counter outputs and the regulation switch drivers, or (2) the counter can be operated at the building block potential, with up to 16 Kv coupling required at the up/down count input lines, and signal coupling between the counter and switch drivers across a potential no greater than the building block output voltage.

Other features possible with the coupling of up-down count or switch driver signal are:

1. In-flight trimming of load voltage by commands to the reference electronics or data processing electronics, such as may be required to alter the operating mode or output power of a load

2. Preset an array output voltage prior to connecting a load, either by sending a switch-state signal or temporary sensing at array output rather than at the load.

In addition to the above-described signals, spacecraft electronics should provide another low-level logic signal to the array-mounted regulator for failure management and to provide maximum control. An "All Open" signal could be sent to all switch drivers in a building block in the event that a counter malfunction is observed, provided that the regulation switches in the other series-connected building blocks can still maintain proper load voltage.

A feature of the binary switch system which provides flexibility of operation is its ability to limit building block output voltage considerably below the design value of output voltage. The building block voltage can range from its designed maximum value down to the voltage determined by the product of the number of unswitched cells and the maximum solar cell operating voltage. Since the voltage reference is contained in the spacecraft and the input "regulation" signal to the array is only an "up count" or "down count" signal, the switches will close and reduce output voltage as long as the "down-count" signal is present, down to a lower voltage limit determined by the number of non-shorted solar cells in the building block when all 11 binary switches are closed. Thus any arbitrary voltage above 2000 volts can be obtained by a series arrangement of 750 - 1340 volt blocks. Hence, it is possible to provide any tap voltage from 2000 to 16,000 volts. Such a series combination of blocks to provide taps will not readily reconfigure in parallel to provide higher current at lower voltages. By clever placement of the different voltage blocks and the stacking switch, it may be possible to obtain an arrangement that will have nearly equal voltages being paralleled when the array is reconfigured. The problem with inequality of building block output voltages when blocks are paralleled is that some power capability is lost because some cells may be operated at less than peak power or other groups of solar cells would have to be kept shorted to obtain the proper voltage. A building block rated for V_{BB} output voltage can be operated at a lower voltage. This is done by maintaining specific shorting switches closed continuously, reducing the maximum power capability of the block. If certain HVSA system power/voltage configurations do not require maximum power, this method could be used to obtain desired voltages, in the reduced power configuration, from blocks designed to provide maximum (higher voltage) power in another configuration.

Consideration of the advantages and limitations of each of the voltage regulation methods studied during this program has led to the decision to recommend the use of the 11-switch binary system with controlled voltage quad transistor switches for the HVSA building block output voltage regulation. The other regulating methods considered other advantages and present solutions to particular problems in several unique areas. However, on the basis of maximum system efficiency, least parts count, capability of providing maximum building block voltages from 750 to 1340 volts with identical regulator and switch design, and flexibility in allowing building blocks to operate over a range of voltage below the maximum value, the 11-switch binary system appears to be most advantageous for a general-purpose building block concept.

5.2.5 HIGH VOLTAGE SIGNAL COUPLING

A significant problem exists with providing an interface for the digital regulation switch signals and the solar cell switching transistors, as well as for actuation of the other switching and control functions (load and array grounding switches, stacking switch and solar array shorting switch). This interface requires the coupling of a very low voltage, common return driver to the high voltage, floating return switches. Two methods of accomplishing this function were investigated; transformer coupled using high frequency signals and light coupled devices.

The first method requires that the digital information be used to control a high frequency oscillator. The oscillator frequency is then transformer coupled to the high voltage array, rectified and filtered. The resulting DC is then used to control the high voltage switches. This concept is illustrated in Figure 48. The

use of sufficiently high frequency would reduce the transformer size; however, this reduction would be limited by the high voltage insulation requirement. The packaging constraints imposed in mounting components on the array will make the use of transformer coupling difficult due to their size.

The second and more promising approach is a light coupling technique using a light emitting diode (LED) transmitter and a photo sensitive receiver.

The coupling of a signal by light permits direct d. c. coupling without any electrical connection. The concept is simply a light emitting source illuminating a light sensitive receiver. The receiver signal is amplified to provide switched drive as required. The optical path provides physical separations and insulation for high voltage isolation.

Lamps, a common light source, could probably not be applied in this severe environment. However, semiconductor devices such as light emitting diodes (LED) or laser diodes are presently being used to illuminate photo diodes or light sensitive transistors for optically coupled isolation switches.

An investigation of existing light coupled devices in a single package showed present day ratings up to 5 Kv for an axial lead pencil shaped device. High gain devices rated at 100 volts were found. The high gain is desirable but not necessary when a high impedance element is used with the light detector, such as an FET. The high gain is due primarily to the closeness of the emitter and receiver and low transmission loss between the elements, hence the device inherently will have lower breakdown voltage.

Light-emitting diodes require 20 to 50 milliamps at a voltage of 1 to 1. 5 volts, or up to 75 milliwatts per LED. This current and voltage requires that drivers be used at the output of the logic circuits.

The load switch, stacking switch, and array shorting switch appear identical to the signal source: 4 LED's must be driven in a redundant manner. Four drivers and four lines could be used to signal a quad switch arrangement, as shown in Figure 49. The design of the drivers must have no single failures which leave it on.

The LED's for regulation switches are driven by the counter and the "all open" signal. Obtaining full building block output power is dependent upon opening all regulation switches, so the "all open" command must not be dependent upon circuitry or power associated with the counter, which could fail. Accordingly, it is assumed that sufficient drive will be available from the "all open" signal to drive all the LED's of the regulation switches. The circuitry to drive these LEDs from the counter and the "all open" signal is shown in Figure 50. The resistors limit and evenly distribute the current to the LED's. The diodes in the "all open" line prevent that line from loading the transistor output. The transistor is a current amplifier stage for the counter output.

The most readily adaptable micro-circuit device for the high voltage signal coupling application appears to be the Texas Instruments TIXL-103, which consists of an LED bonded to a photosensitive transistor with a thin layer of glass. This device, though rated at 100 volts, has a characteristic breakdown in excess of 800 volts and the manufacturer believes rated breakdown somewhat above 1000 volts can be obtained. This device is an encapsulated chip approximately 75 x 100 mils in area and about 50 mils thick. TI believes that significantly higher voltage isolation capability can be obtained by bonding the emitter and receiver to the opposite ends of a fiber optics bundle. Some gain will be lost due to a loss of light reaching the receiver compared to the TIXL-103, which has very little separation between the emitter and receiver. The most significant problem would probably be packaging the LED-fiber optics-photo transistor device and handling the high voltages into and out of the package containing the isolator. Applicable specifications for the LED high voltage signal coupler needed for the HVSA appear in Section 9. 4, Device Survey.

5. 2. 6 SWITCHING VOLTAGE TRANSIENTS

Step changes in output voltage are an inherent characteristic of any discrete switching voltage regulation system. In addition, transient voltages (or spikes) will occur in a sequence where more than one switch changes state.

The worst switching transient with a binary switching system will occur when the value of the count represented by the outputs of the binary counter is at its midpoint. At this point, the count change in an 11-bit arrangement causes 10 switches to close and one switch to open, or vice versa. The transient occurs because the switches do not change state simultaneously or in zero time. For instance, the "closing" switches may "close" faster than the "opening" switch "opens." This will probably be the case since the circuit design to accommodate worst case will result in excess gain existing under nominal conditions. The addition of some capacitance in the operational amplifier circuit could assure this "make before break" condition. This seems desirable since only negative voltage transients will occur and overvoltage spikes will be eliminated.

The magnitude of the negative transient in the binary switching scheme depends upon the building block output voltage. The conditions for maximum transient (switches 1-10 closed and switch 11 open) defines the number of cells supplying voltage at that time: 1024 cells of the 2047 cell in the 11-bit regulator, plus non-switched solar cells in the building block. Hence, the individual cell voltage at which the maximum transient occurs can be calculated:

$$V_{cell} = V_{BB}/\text{No. of non-shorted cells} \tag{1}$$

The total number of cells in the building block is determined by the minimum allowable cell operating voltage (Maximum-power voltage of a cell at steady-state temperature at end of 5 years):

$$\text{Total Cells} = V_{BB}/0.358\ \text{V} \tag{2}$$

For the condition of maximum negative transient, the cells in the first 10 bits are shorted, and the number of non-shorted cells remaining is equal to the number of total cells minus the cells in the first 10 bits or

$$\text{No. of non-shorted cells} = \frac{V_{BB}}{0.358} - 1023 \tag{3}$$

Substituting the relationship of equation (3) into the denominator of equation (1), the per-cell operating voltage at the time of maximum transient is

$$V_{cell} = V_{BB}/(V_{BB}/0.358\ \text{V} - 1023) \tag{4}$$

Now when the 11^{th} switch is closed, it will introduce a transient voltage at the building block terminals equal to the number of cells in the 11^{th} bit (1024) times the per-cell operating voltage, or

$$V_{TR_{max}} = 1024 \times V_{BB}/(V_{BB}/0.358\ \text{V} - 1023) \tag{5}$$

The maximum transient voltage defined in equation (5) was evaluated, and is plotted as a percentage of building block output voltage in Figure 51.

One conceivable method of reducing the switching transients is as follows: If the regulation shorting switches were ramped on and off, it may be possible to control the ramping so that the rate of voltage change is equal for both polarities (turning on and turning off). If the ramping were slow compared to the signal propagation time to all the switches, starting times of the different switch ramps would be virtually the same. The resulting output voltage transient would be zero if the "ramp-ons" were identical to the "ramps-offs." Without perfect synchronization, the transient would not be zero but a considerable reduction in the magnitude would be obtained. The ramping would, of course, cause a transient high power dissipation condition in the shorting switches, which will limit the ramp time obtainable. The ramping would also reduce the regulation response time since changes in count could not occur as rapidly.

It is noted that the voltage transient magnitude depicted in Figure 51 is a worst case, occurring only when the highest order (11^{th}) binary switch is actuated. This situation can occur only when the solar array temperature is warming up from $-55^{o}C$. If the array were to be maintained in a shorted condition for an additional short period of time (2 to 3 minutes) the available array voltage would be considerably less and the maximum transient may be only a fraction of the values indicated.

5.2.7 SWITCHING SPEED CHARACTERISTICS

An estimate of the switching speed (response time) for turn-on and turn-off of the various switching functions on the HVSA is presented below.

5.2.7.1 Regulation Switches

Switching Component	Regulation Switch Turn-ON	Turn-OFF
11 bit counter[1]	0.027 μS	0.027 μS
Light coupled switch[2]	3.0 μS	3.0 μS
Operational Amplifier slew rate[3]	8.2 μS	3.5 μS
Regulation switch and driver stages[4]	0.060 μS	0.490 μS
Total Delay =	11.3 μS	7.0 μS

Allowing some margin, 12 micro seconds are required for a one count change; the maximum (count) repetition rate is therefore $1 \div 12\ \mu$ sec = 83,000 Hertz. The total time required for a complete count for an 11 bit counter (maximum to minimum power) is 2047 counts x 12 μ sec/count = 24.5 milli seconds.

Notes: Switching times are based on:

1. Counter: NSC DM 7563.
2. Light coupled switch: T1 X L 103 rise and fall times.
3. Fairchild μ A741 operational amplifier slew rate is 0.425 V/μ sec.

   Output must fall from 1.5 V to 0 to turn off, and rise from -2 V to 1.5 V to turn on.
4. 3 transistors including regulation switch (2N5151).

5.2.7.2 Array Shorting Switch and Stacking Switch

The transition from array maximum to zero power (array shorted) occurs within 4 μ sec of the "array short command" for the array shorting switch. This includes the light coupled switch and transistor delay times. Since the stacking switch employs the same circuit and components, its response time will be the same.

5.2.7.3 Load Switch and Array Grounding Switch

No estimate can be made for the SCR switches since this device must be developed and tested, and the construction and switching characteristics are not known. Load switch switching characteristics are very important since up to kilowatts of power can be dissipated in this device during the transition from a cutoff condition (blocking) to a saturated condition (conducting load current).

5.2.8 SIGNALS REQUIRED FROM SPACECRAFT

A summary functional and electrical description of the various signals required by the HVSA from the spacecraft is presented in Table 3. Some of the signals are generated by logic functions in the spacecraft computer (such as up or down count signals for regulation), while others originate as transmitted ground commands (such as HVSA system reconfiguration signals).

5.2.9 POWER CONDITIONING SUMMARY

A method for maintaining voltage regulation by discrete switching has been selected which senses load voltage and provides a digital error signal to be sent across the spacecraft/array interface. The error signal is either an up-count or down-count signal which changes by one count the state of an array-mounted binary counter. Eleven quad redundant transistor switches respond to the output from the counter, shorting or opening a shunt path across binary numbers of series solar cells in the main array. A binary system with controlled-voltage transistor switches ensures meeting the goal of 0.1% output voltage regulation over a range of building block voltages from 750 to 1340 volts with a single 11-bit regulator design. Any building block can be operated at a lower-than-design voltage if required, at some loss in deliverable output power.

Light-emitting-diodes/fiber-optics/photo-transistor packages provide the high voltage isolation capability for transforming signals to the various HVSA functions.

Voltage transients approaching the building block voltage in magnitude can occur with binary switching, but can be significantly reduced if system regulation is not required until the array temperature approaches the steady-state value (about 5 minutes in synchronous orbit). Switching speed of the various switch functions is limited by the length of time a transistor requires to be pulled out of saturation, which is about 12 microseconds for most transistor switch functions on the HVSA.

Transistors having the capability of blocking up to 1000 volts are required for the binary switching arrangement in a 12-bit system.

Problem areas exist in trying to provide close-tolerance regulation before the load is connected, establishing a 16 Kv isolation capability for the LED signal couplers, eliminating switching voltage transients and providing fail-safe counter operation.

Table 3. HVSA Signals Required from Spacecraft

SIGNAL	FUNCTION	NUMBER	ELECTRICAL DESCRIPTION
Up Count	Raises regulation Counter count 1 unit to affect regulation	One signal per building block	1. Logic level pulse for more than 500 Nanoseconds with a maximum repetition rate of 83,000 per second.
Down Count	Lowers regulation counter count 1 unit to affect regulation	One signal per building block	2. Minimum rate depends upon required regulator transient response to satisfy loads.
Array Short Command	Shorts out entire building block; zero output voltage	One signal per building block	Steady state current drive for 4 LED's.*
All Regulator Switches "Open" Command	Opens all regulation switches, maximum building block output voltage	One signal per building block	Steady state current drive for 11 binary switches (44 LED's).
Stacking Switch Series Connect Command	Turns stacking switch on to configure array	1 signal per stacking switch	Steady state current drive for 4 LED's for "on" stacking switch.
Load Switch "on" Command	Turn on high voltage load switch	1 signal per load switch	Steady state drive for 4 LED's driving SCRs
Load Switch "off" command	Turn off high voltage load switch	1 signal per load switch	.5 to 1 second pulse drive for 2 LED's driving transistors
Load return/ Array Ground switch "ON" Command	Turn on high voltage load switch	1 signal per switch	Steadystate drive for 4 LED's driving SCRs
Load Return/ Array Ground Switch "OFF" Command	Turn off high voltage load switch	1 signal per switch	.5 to 1 second pulse drive for 2 LED's driving transistors

* NOTE: LED Drive Power: 50 mw per device (at 30 ma, 1.2 volts).

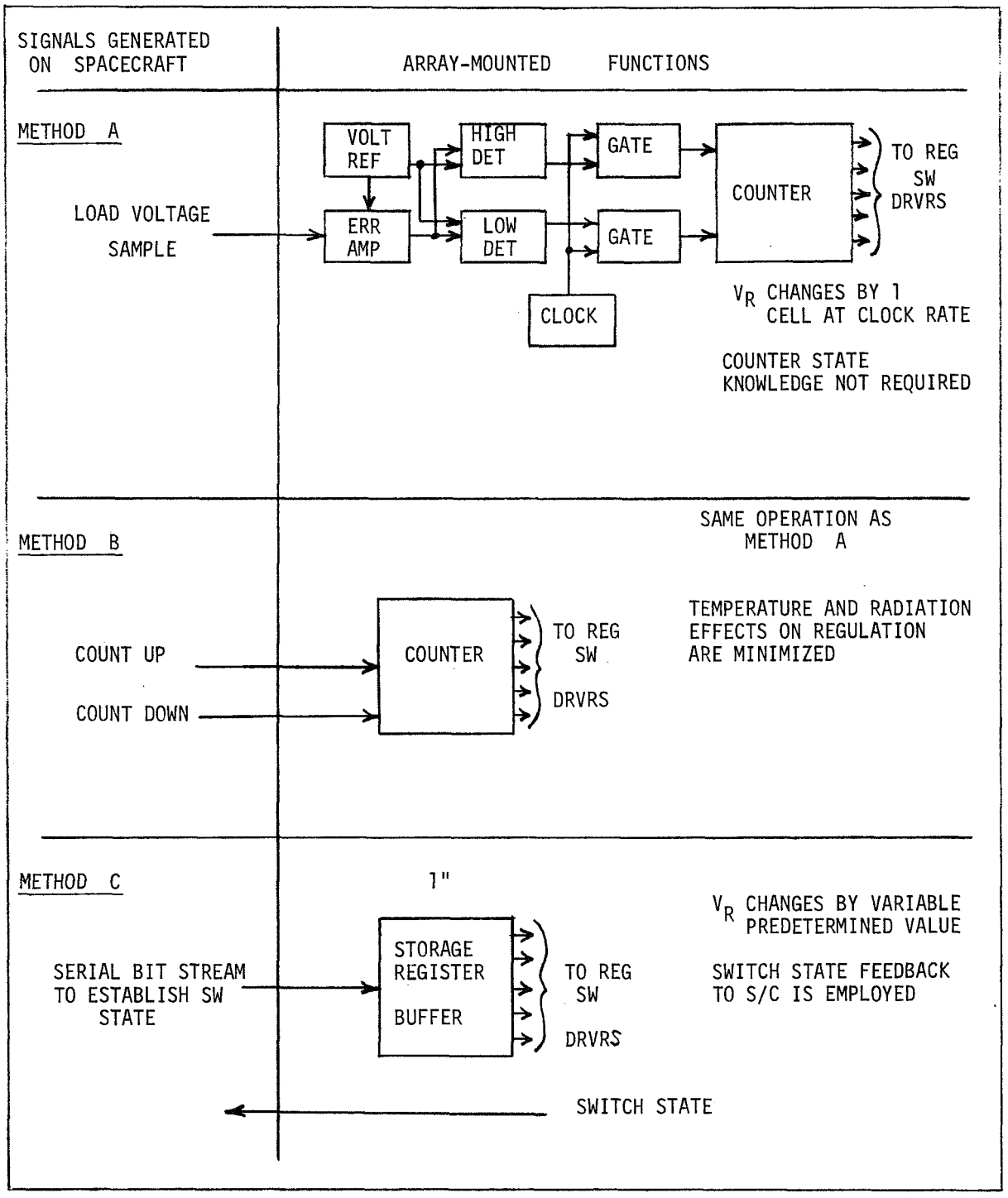


Figure 23. Methods of Regulation by Discrete Switching

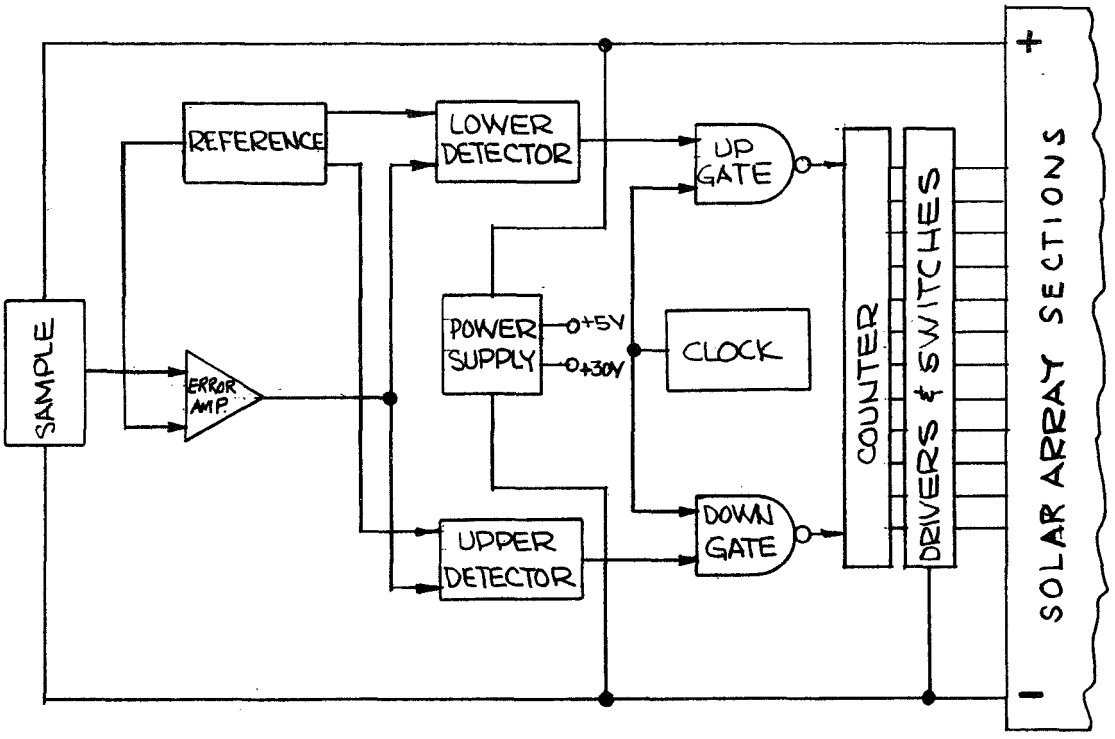


Figure 24. Block Diagram of Discrete Switching Voltage Regulation Scheme

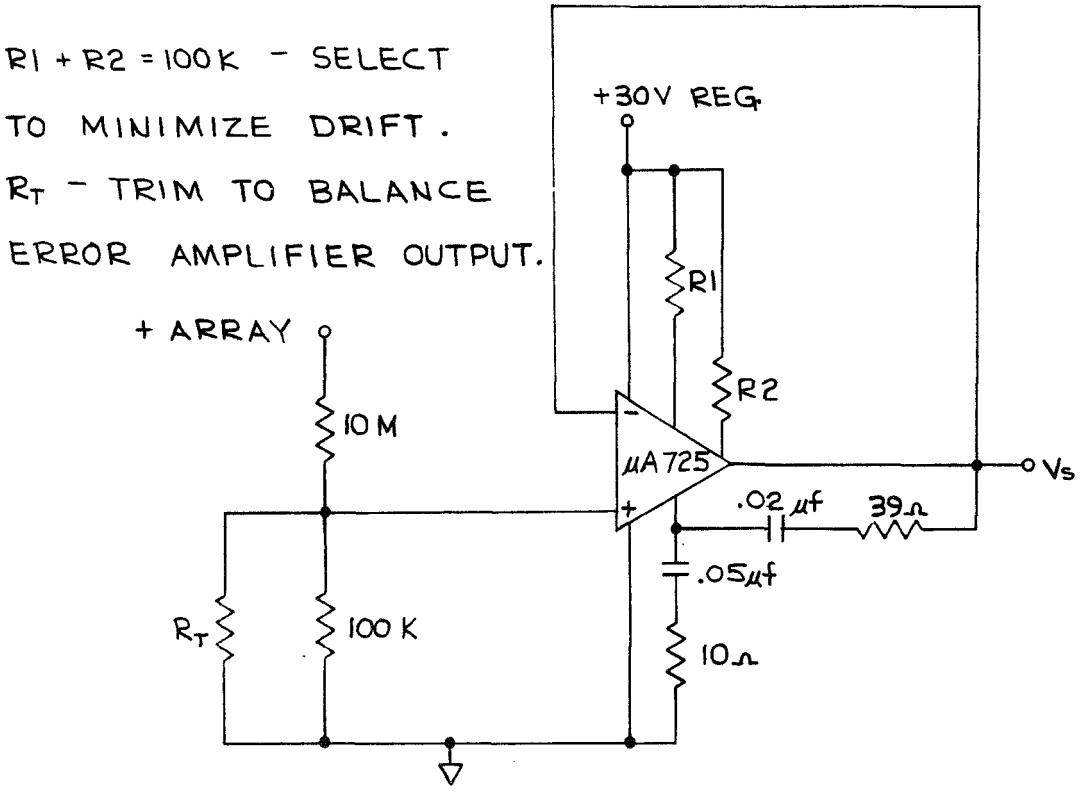


Figure 25. Sampling Element Circuit

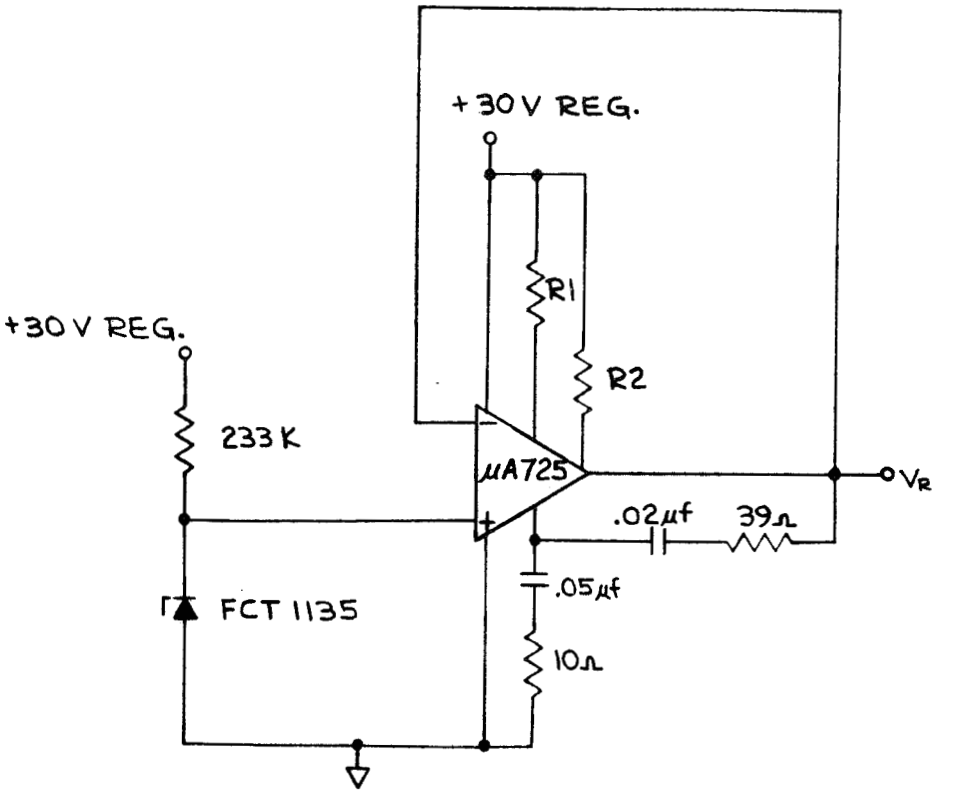


Figure 26. Reference Element Circuit

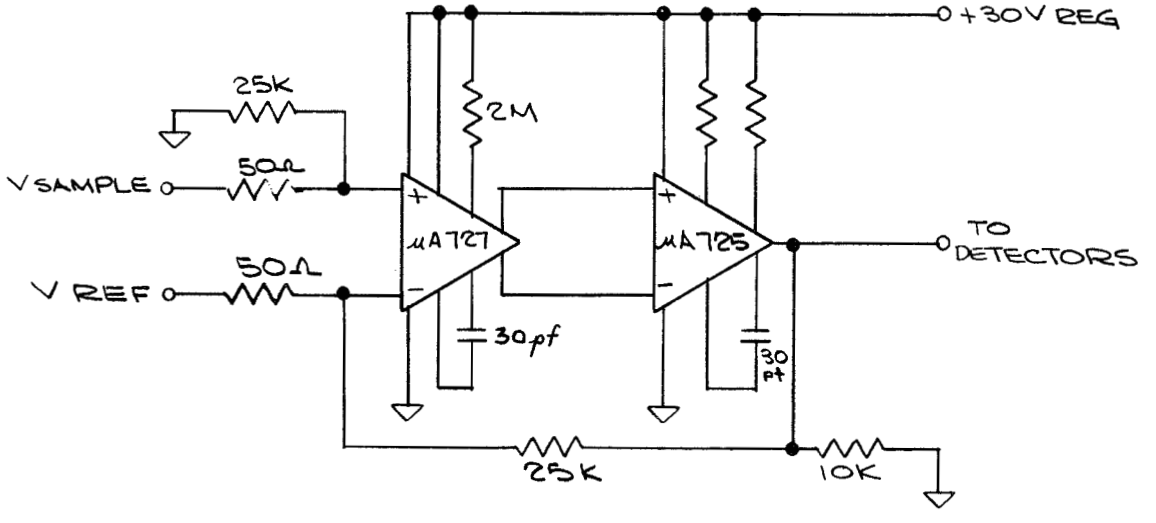


Figure 27. Error Amplifier Circuit

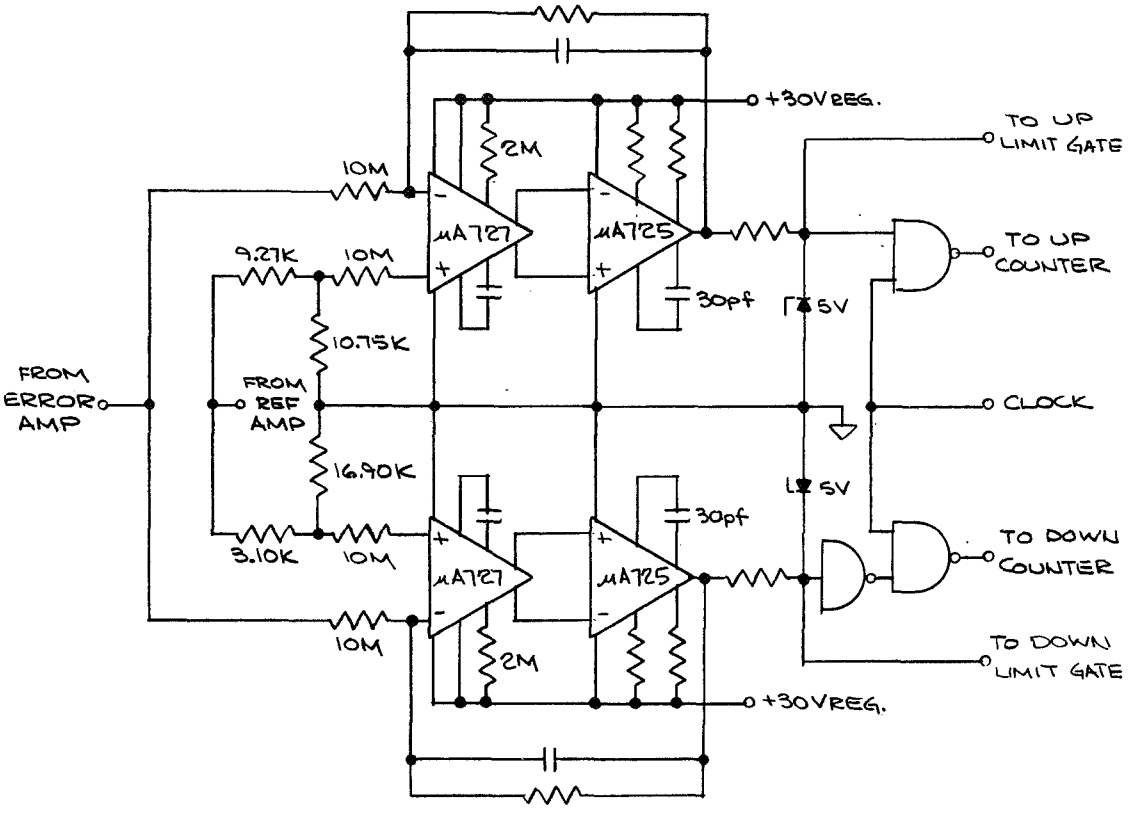


Figure 28. High and Low Detector Elements

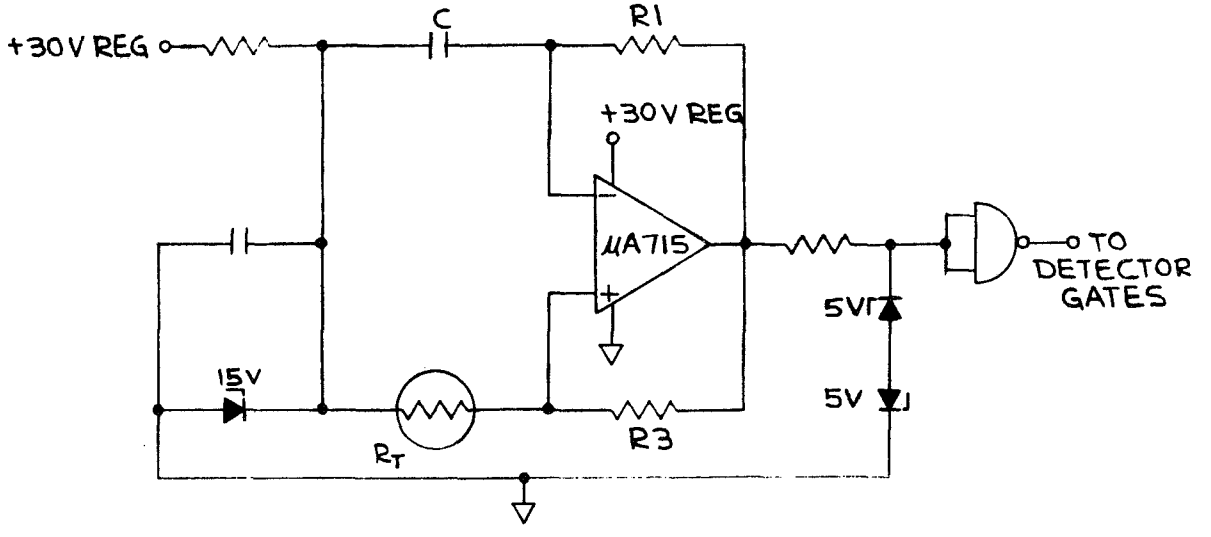


Figure 29. Clock Element Circuit

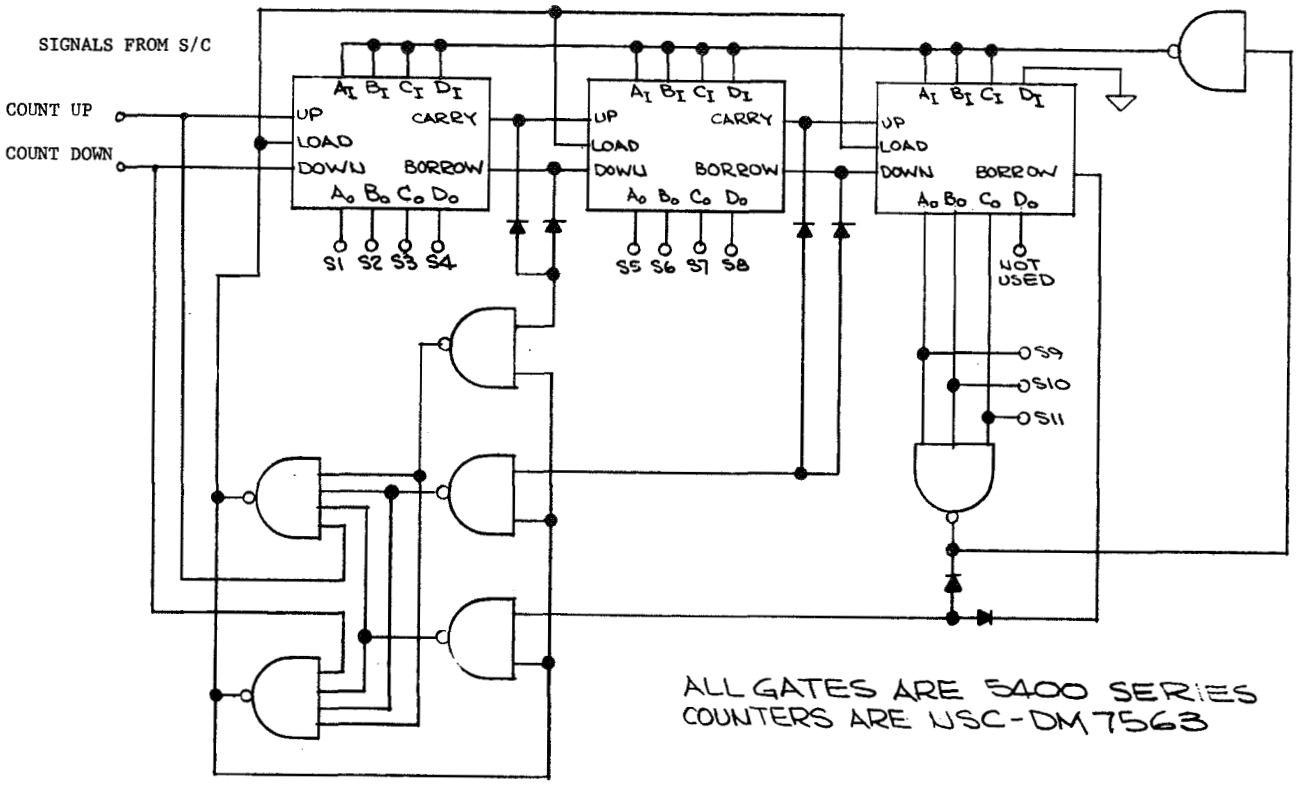


Figure 30. Counter Element Circuit

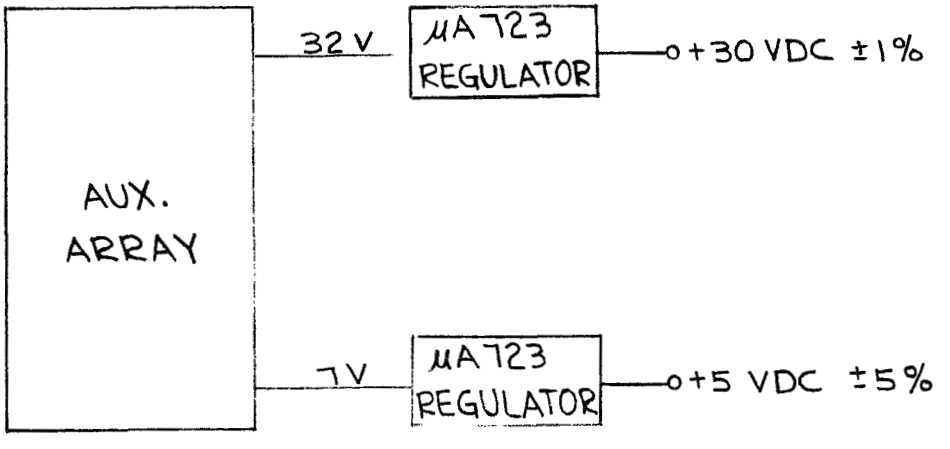


Figure 31. Power Supply Element

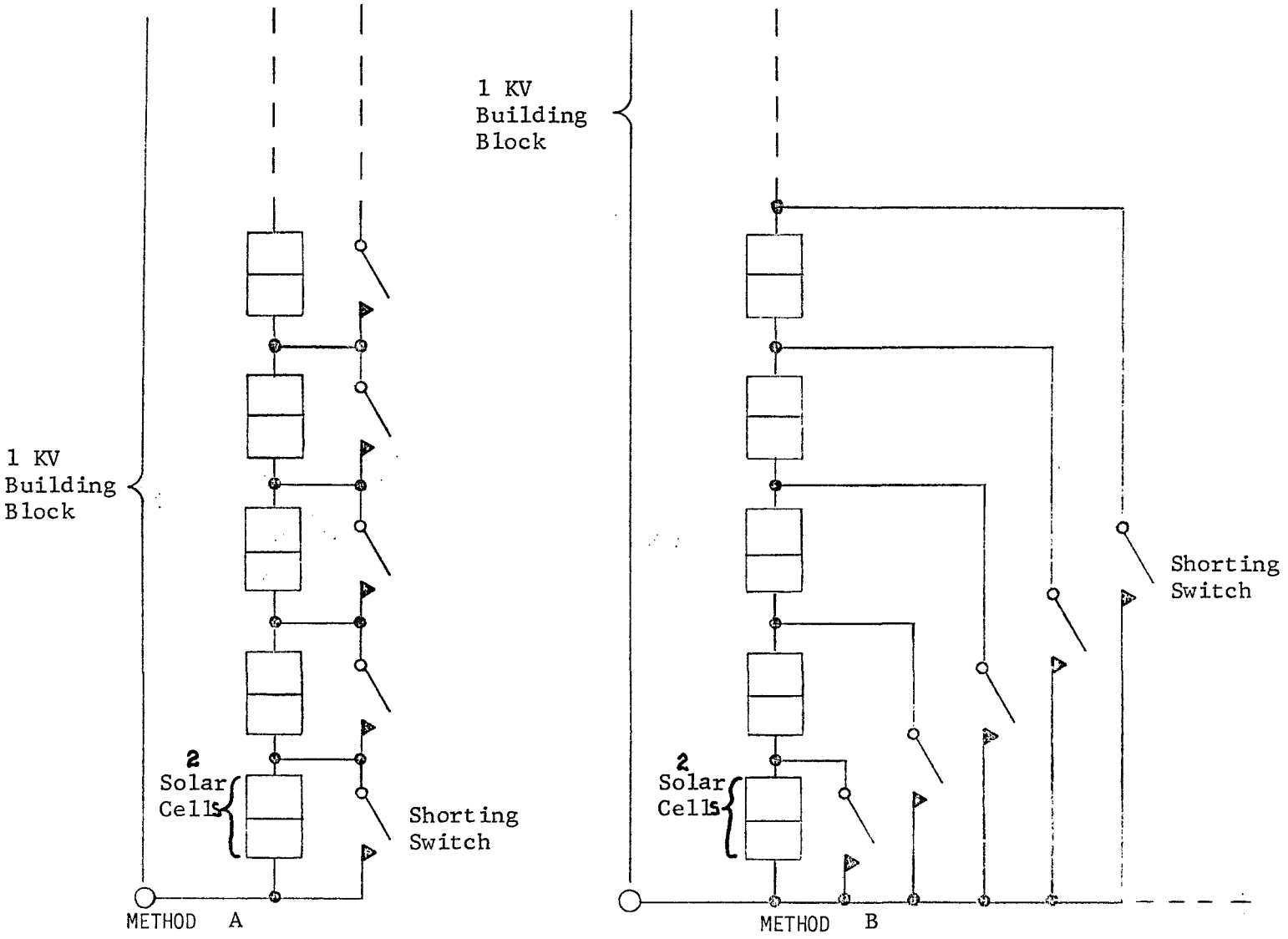


Figure 32. Incremental Switching Schemes

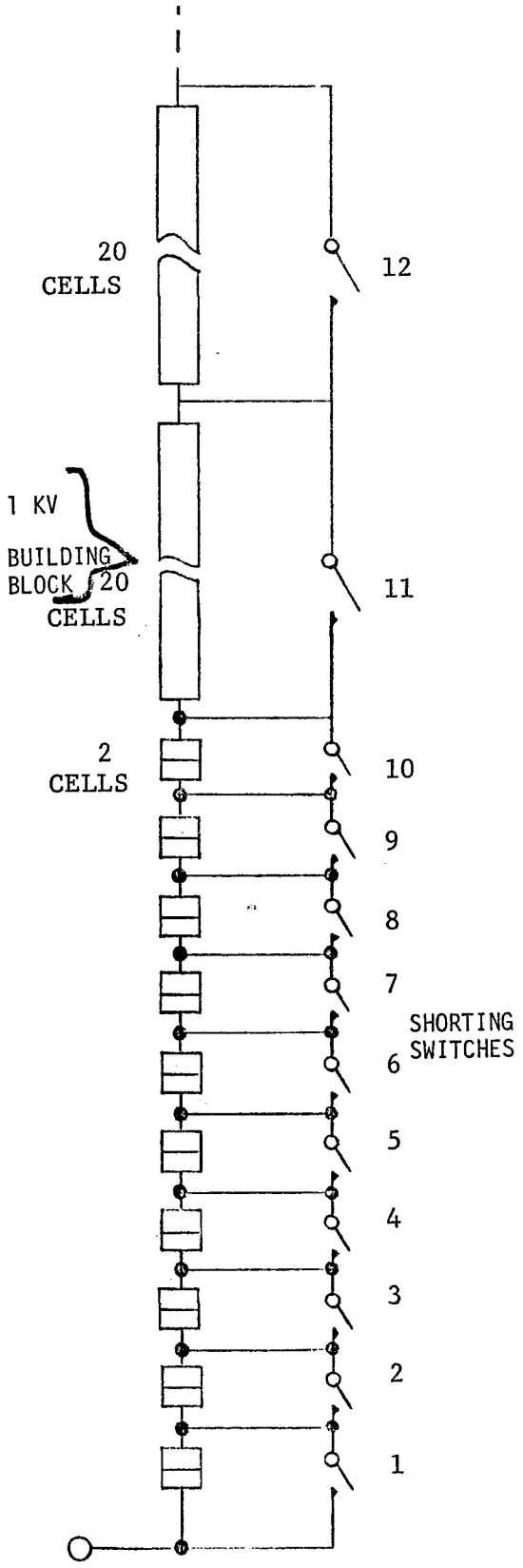


Figure 33. Reduced Incremental Switching Scheme

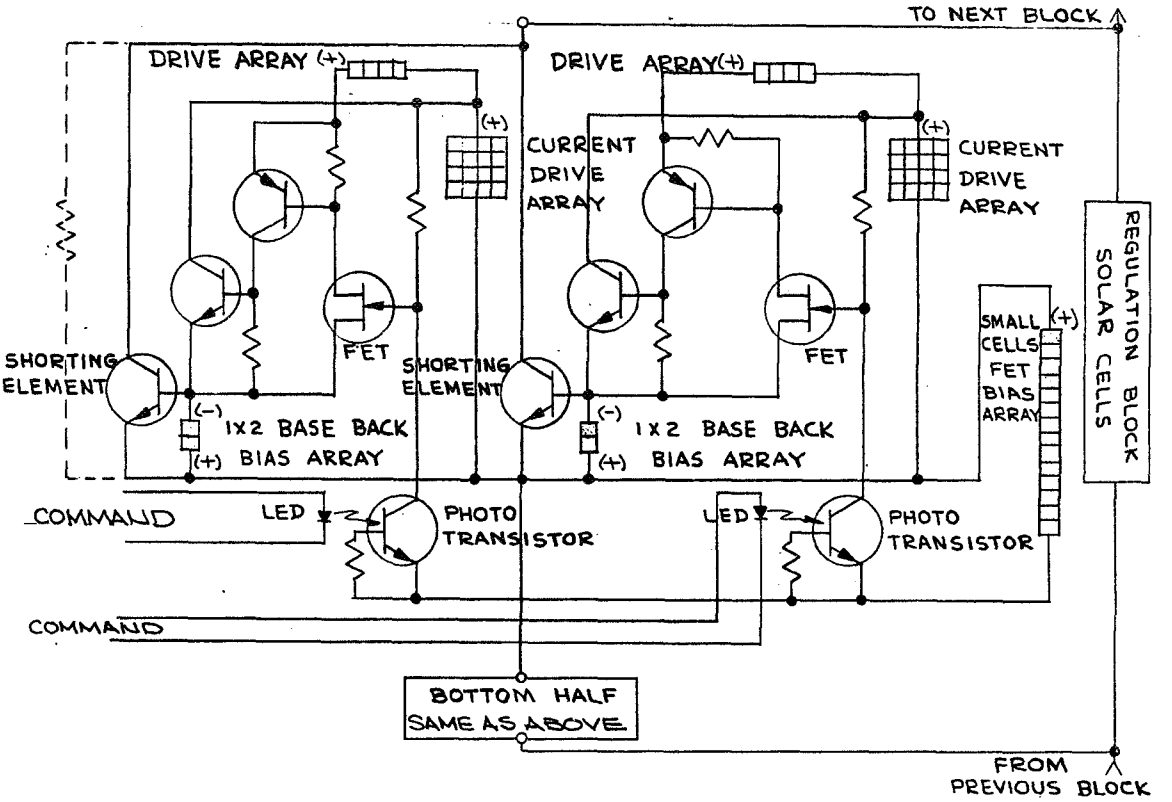


Figure 34. Quad Regulation Shorting Switch

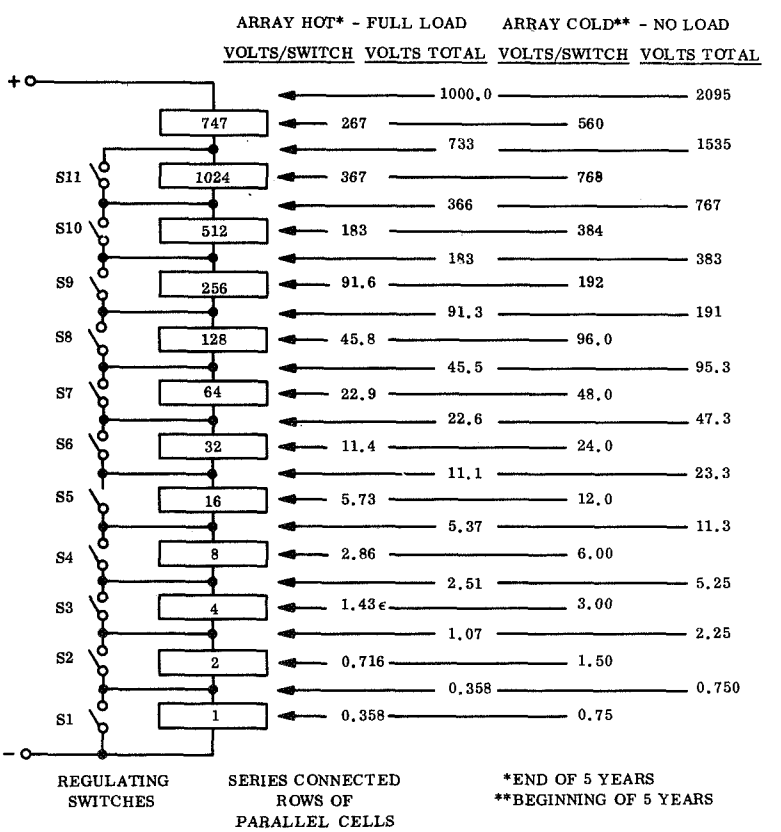


Figure 35. Binary Regulation Switching Configuration

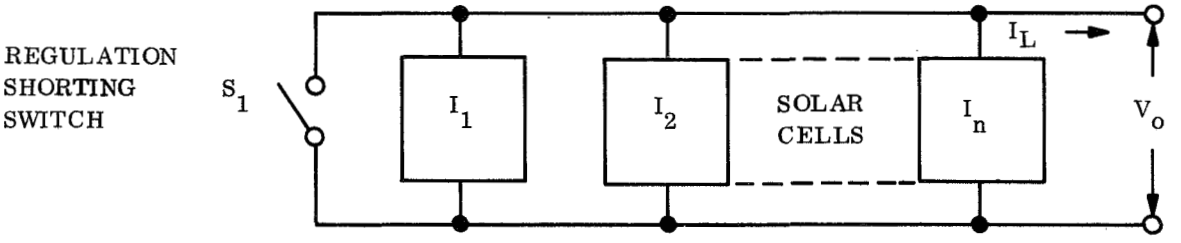


Figure 36. Regulating Block - One Series Cell

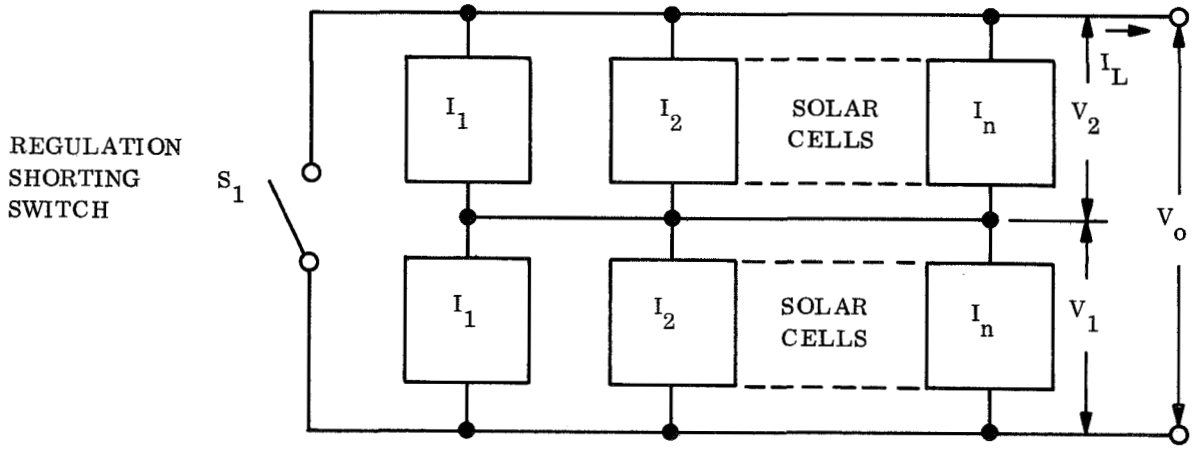


Figure 37. Regulating Block - Two Series Cells

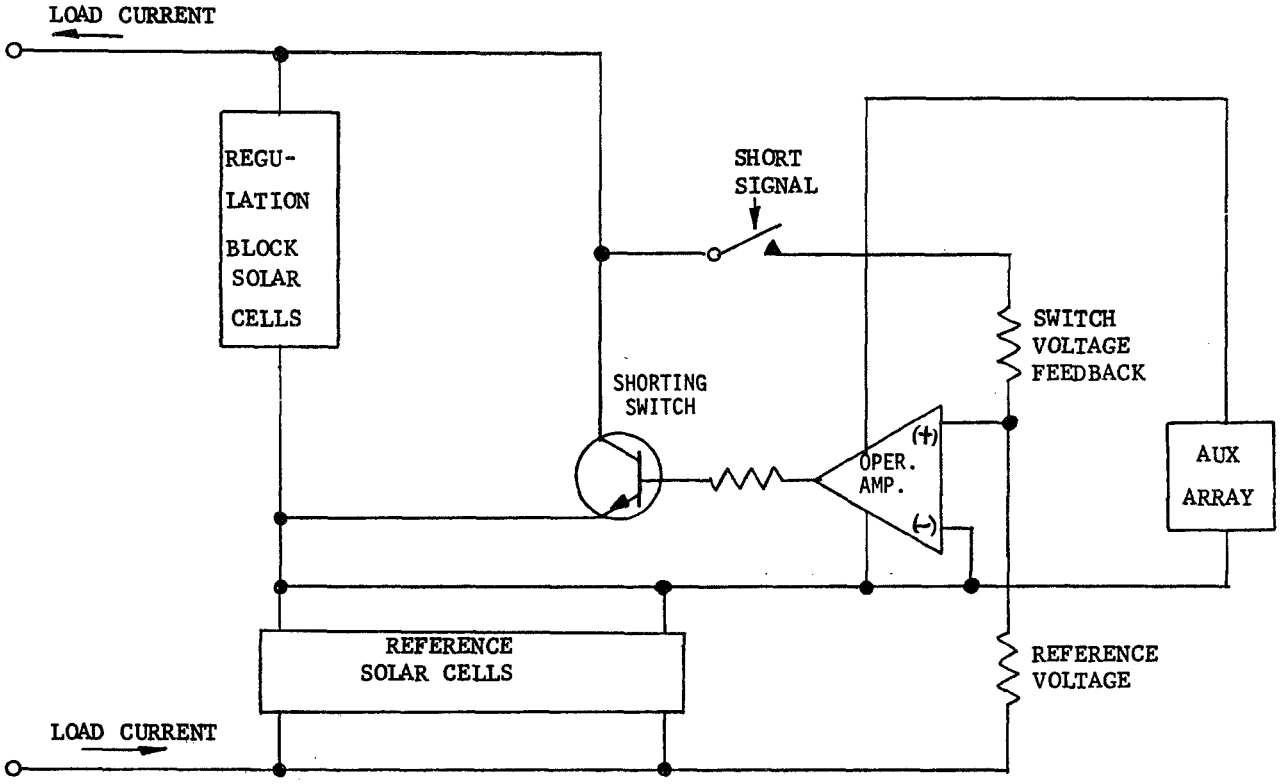


Figure 38. Controlled Voltage Regulation Switch Block Diagram

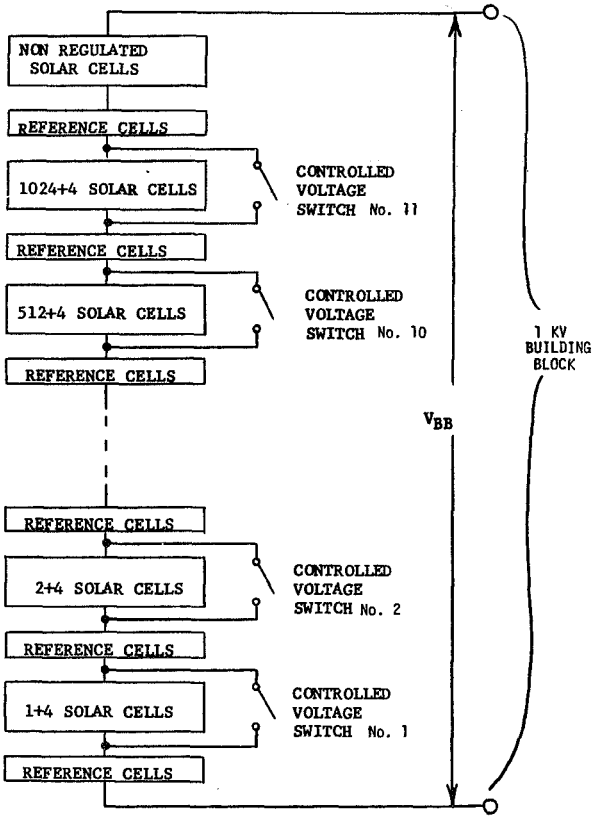


Figure 39. Building Block Regulation Scheme Using Controlled Voltage Switches

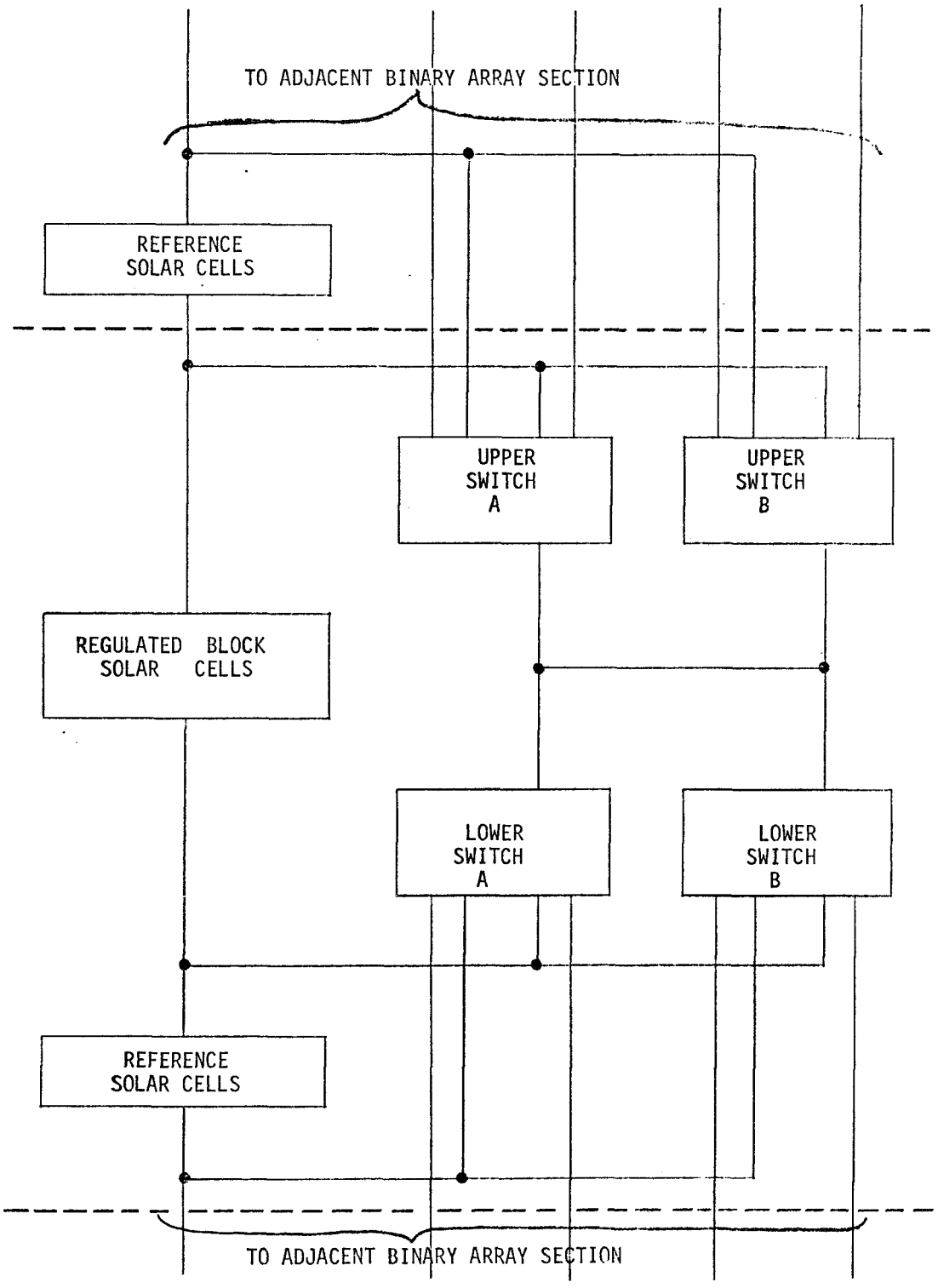


Figure 40. Functional Block Diagram of Quad Redundant Controlled Voltage Regulation Shorting Switch

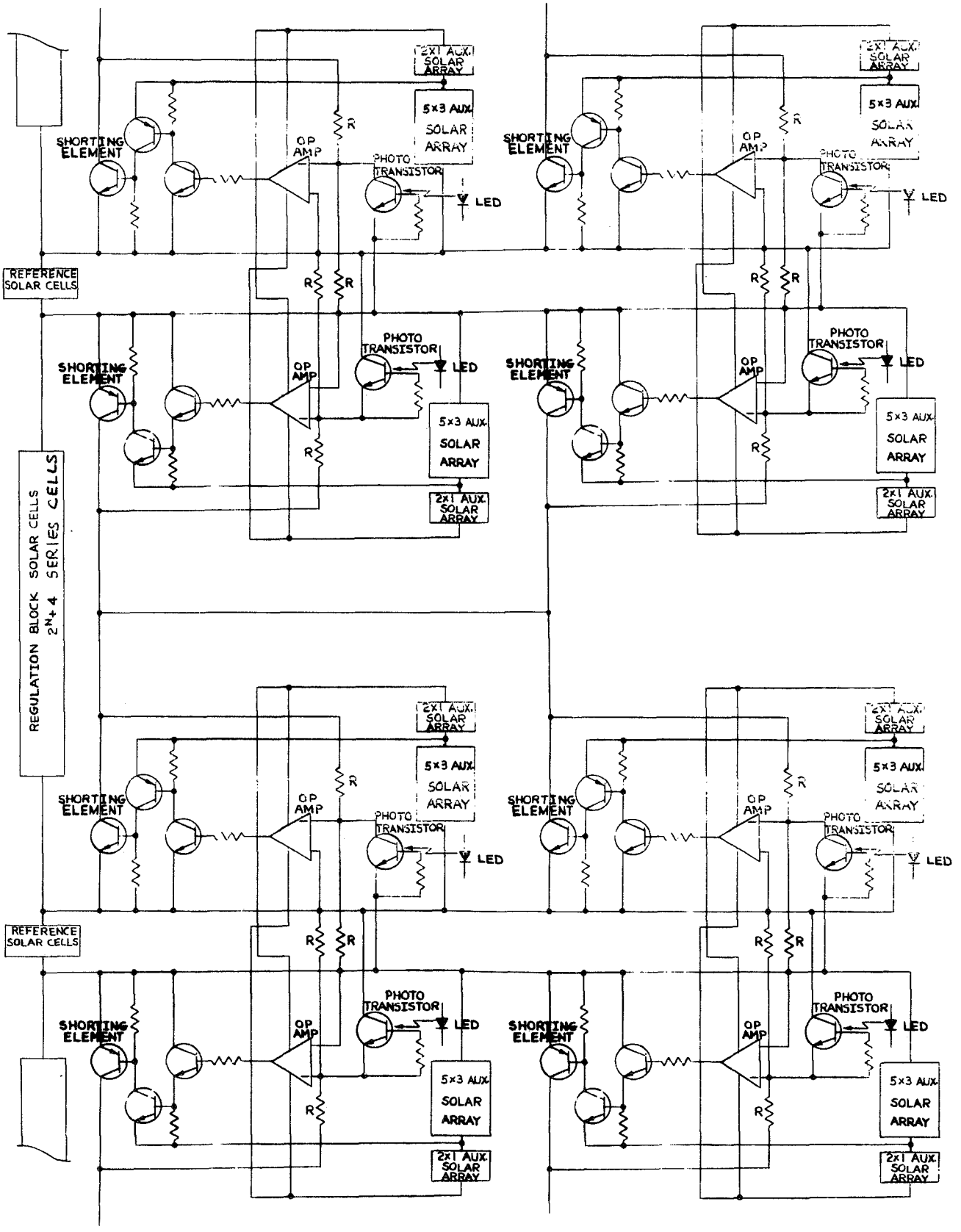


Figure 41. Controlled Voltage Regulation Shorting Switch Schematic

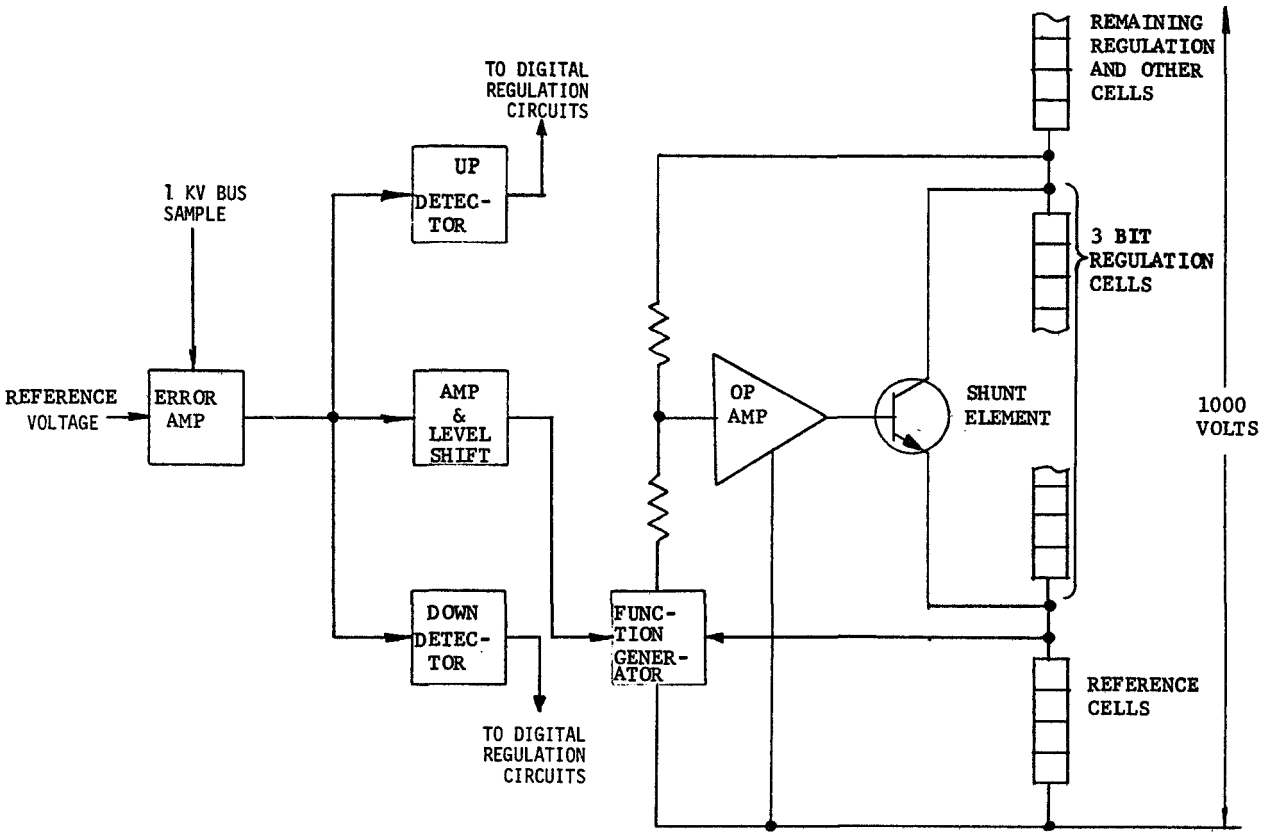


Figure 42. Three Bit Linear Regulator Block Diagram

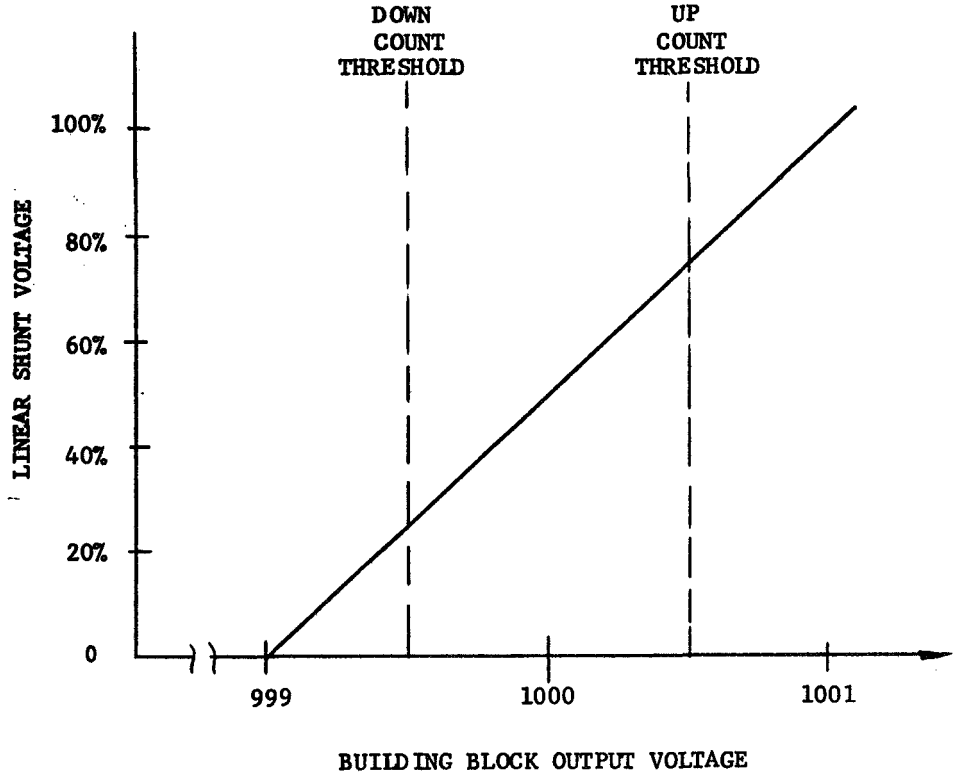


Figure 43. Linear Regulator/Counter Performance

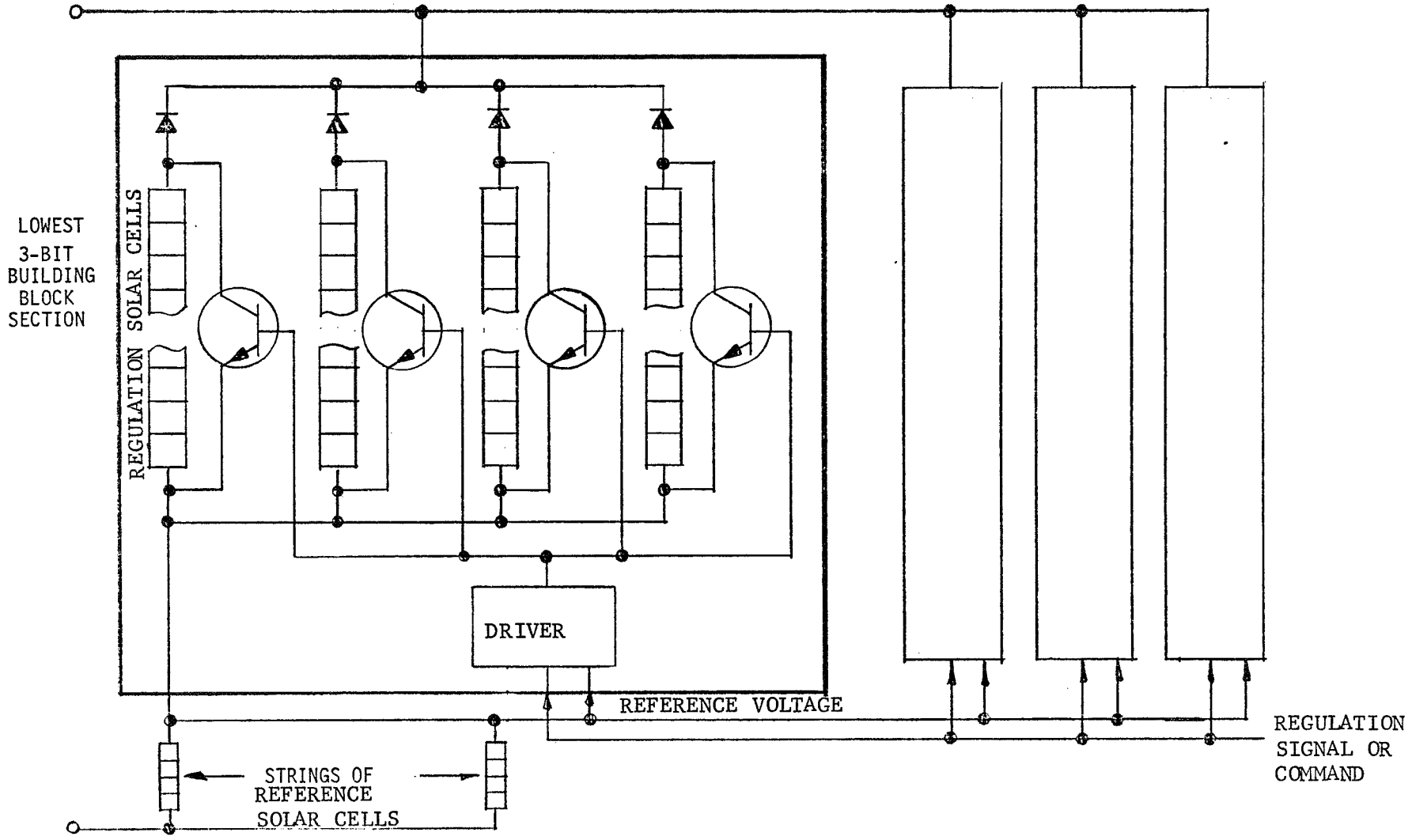


Figure 44. Linear Shunt Regulator with Parallel Regulating Elements

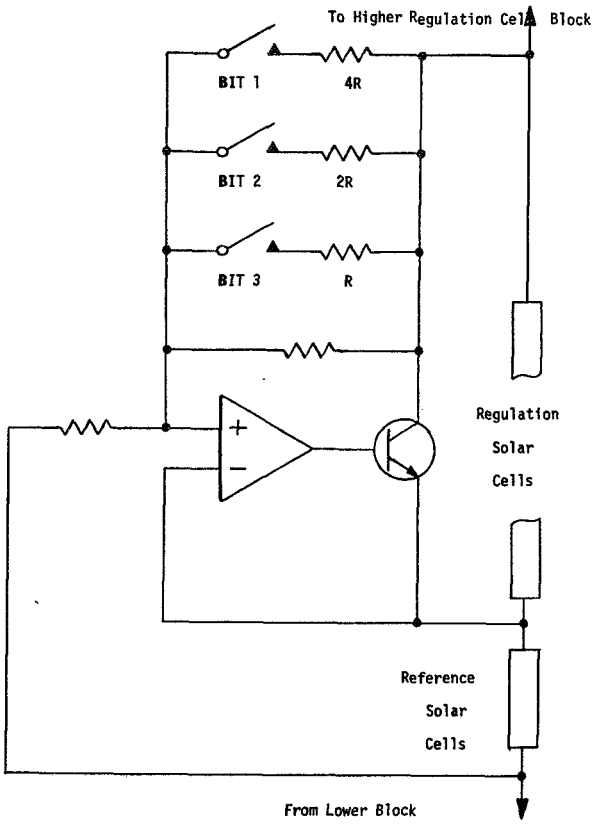


Figure 45. Digital Linear Three Bit Regulator Block Diagram

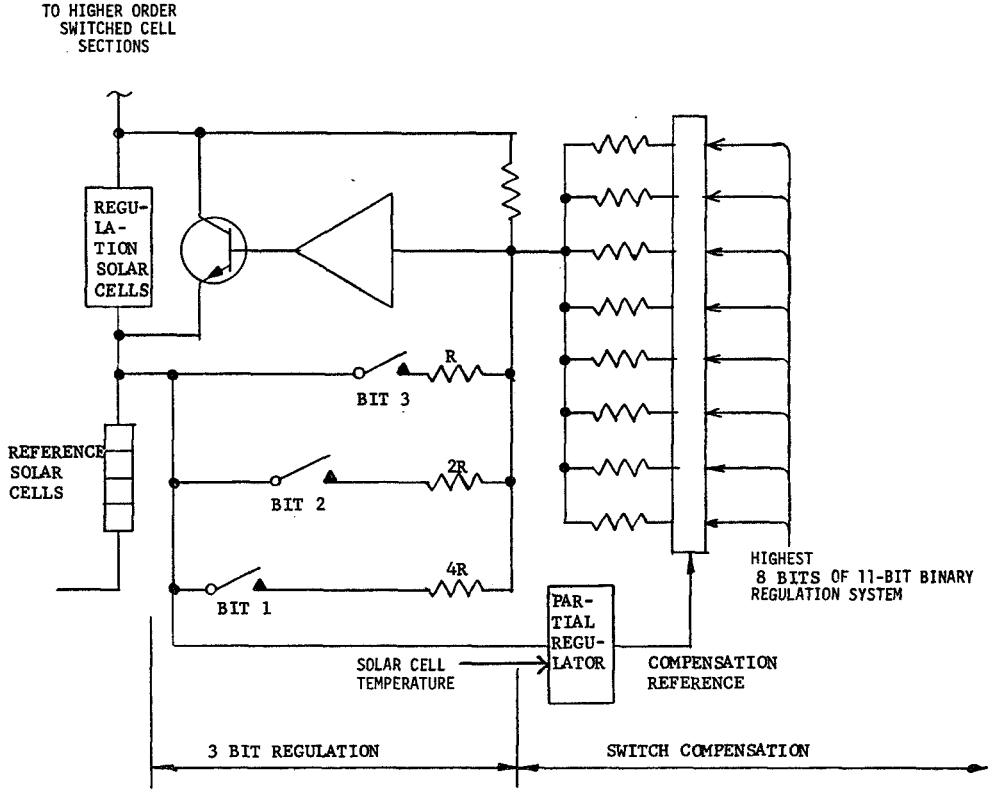


Figure 46. Compensated Digital Linear Regulator Block Diagram

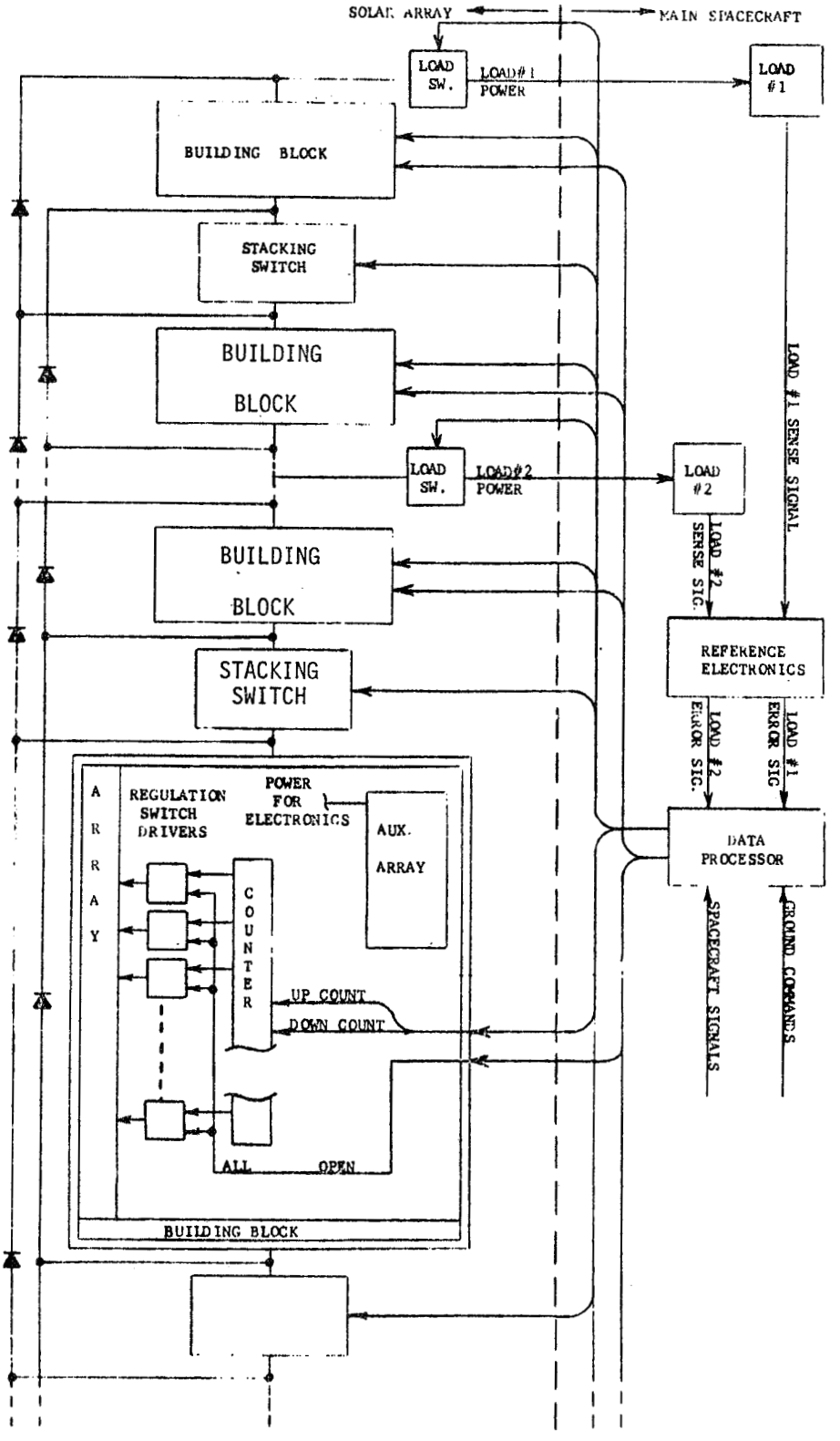


Figure 47. Conceptual Discrete Switching Regulation System

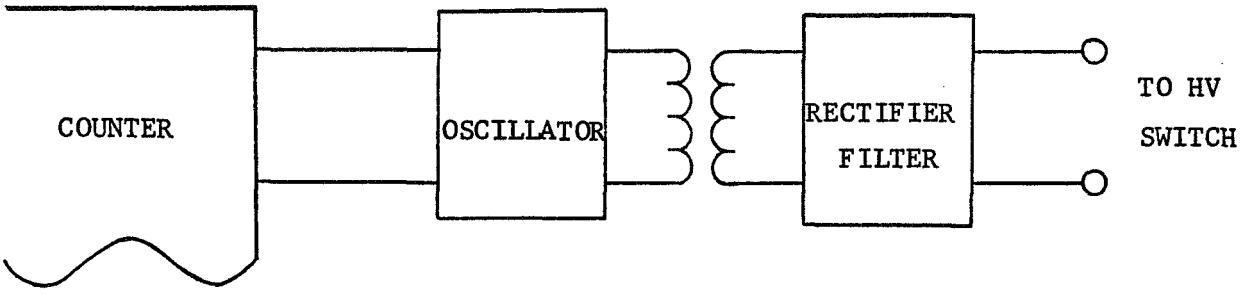


Figure 48. Counter/Shorting Switch Transformer Interface

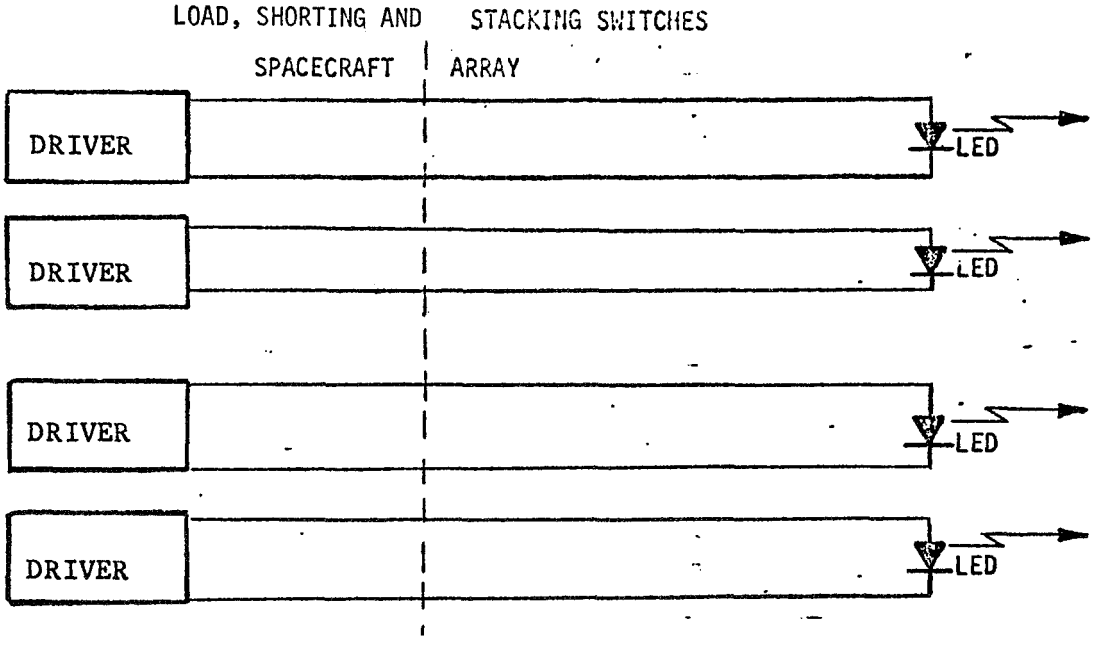


Figure 49. LED Signal Coupling for Quad

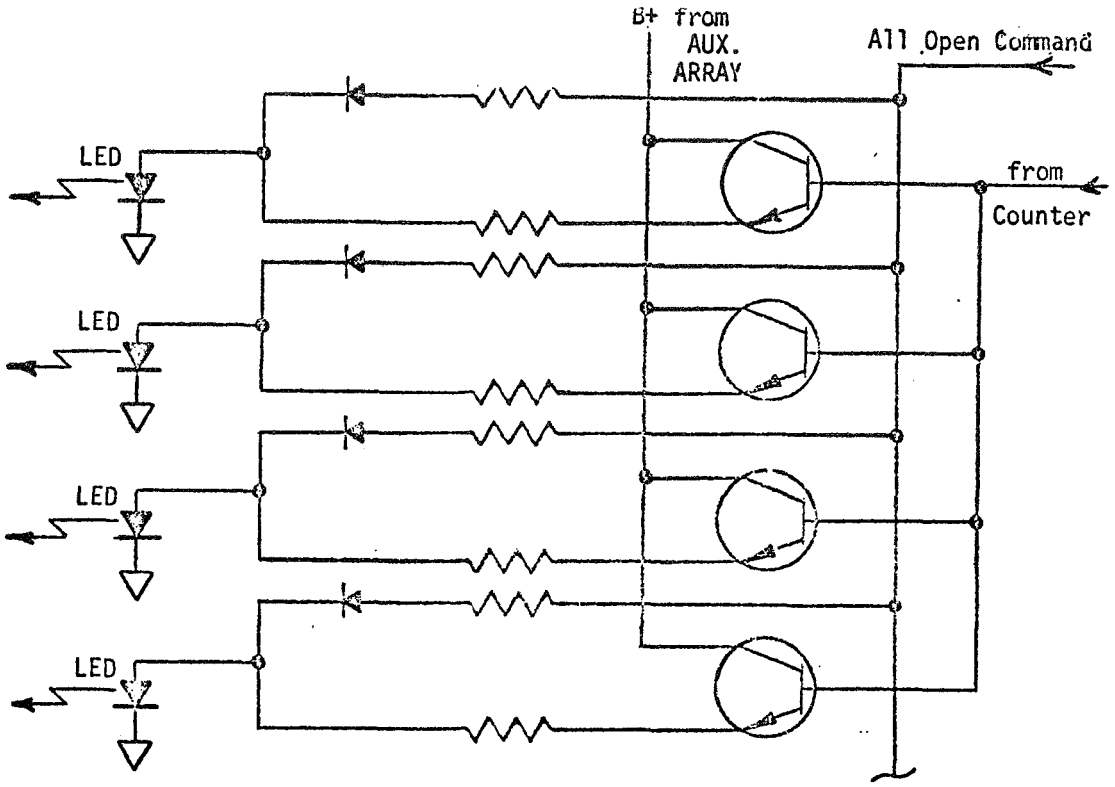


Figure 50. LED HV Signal Couplers and Logic for Regulation, Shorting Switch Quad Arrangement

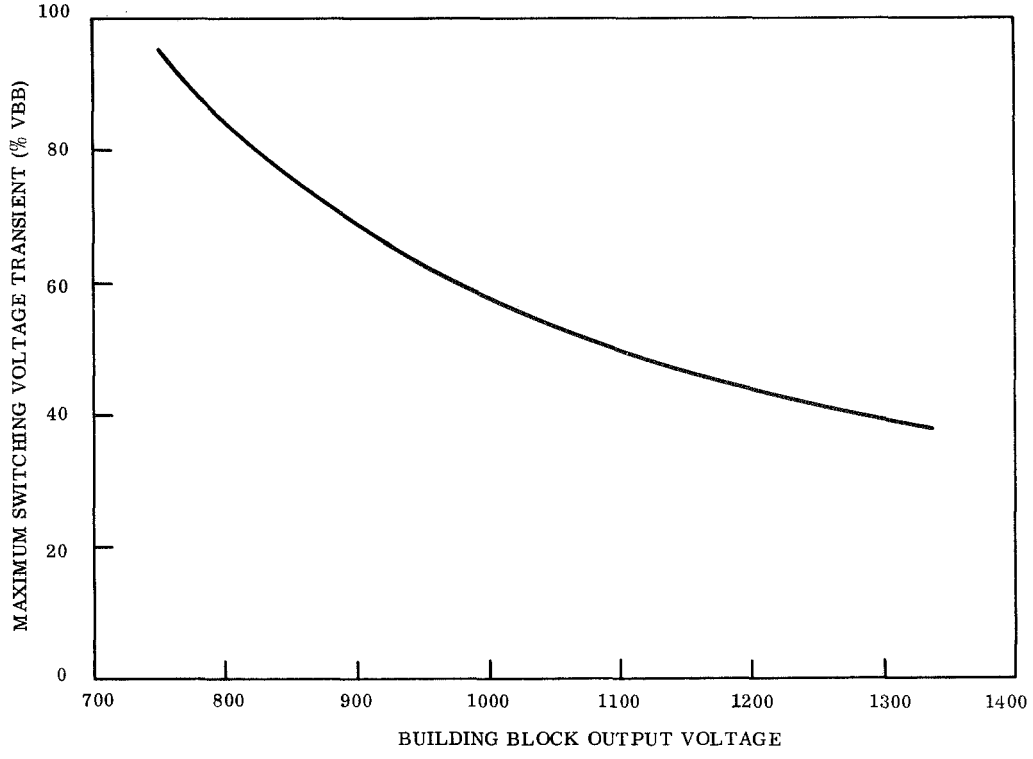


Figure 51. Maximum Regulation Switching Voltage Transients Versus Building Block Voltage

5.3 SOLAR CELLS AND ARRAY

5.3.1 GENERAL

Primary emphasis in the solar cell related effort was to define solar cell requirements for the selected systems and to describe the means for satisfying these requirements. This section describes the latter, i.e., essential solar cell and array characteristics and design performance factors which are the basis of meeting HVSA system requirements. Section 7, System Performance Estimates, describes the use of the information presented herein to calculate array performance and design characteristics (area, weight, etc.).

5.3.2 SOLAR CELL AND ARRAY CHARACTERISTICS AND DESIGN FACTORS

This section presents a description of the solar cell and array characteristics and design factors. The ground rule has been to utilize the components and design incorporated in the 30 watt/lb General Electric Rollup Solar Array, and to estimate the performance of these components in a typical 5-year HVSA mission at synchronous altitude.

5.3.2.1 Cell Type

1. N on P silicon with silicon-monoxide antireflective coating; Solderless, titanium-silver P contact and N contact bar and grid lines in conventional configuration.

2. 1 to 3 ohm-cm base resistivity range.

3. 11.4% bare cell efficiency at $+28^{o}$C, AMO illumination, which is equivalent to 129 mA at 0.47 V with 3.8 cm^2 active silicon area.

5.3.2.2 Cell Size

1. Nominal 8 mil (0.2 mm) thickness.

2. Cell area may be 2 x 2, 2 x 4, 2 x 6 or 2 x 8 cm, depending on circuit output current required and reliability specifications.

5.3.2.3 Coverglass

1. Nominal 3 mil (0.075 mm) thickness of Corning 0211 microsheet.

2. Ultraviolet rejection coating on top surface and antireflective coating on bottom surface.

3. Sylgard 182 adhesive (about 1 mil (0.025 mm) thickness) for bonding to cell surface.

5.3.2.4 Cell Interconnect Material

Expanded silver, "diamond mesh" pattern, about 1 mil (0.025 mm) thickness, solder plated to effect bond to solar cell contacts.

5.3.2.5 Radiation Environment

Estimated total 1-MeV electron damage-equivalent, normally incident particle flux is 5.3×10^{15} $e/cm^2/5$ yrs, accounting for synchronous trapped electrons and protons and solar flare protons, with shielding provided by Rollup Solar Array design.

5.3.2.5.1 Radiation Damage Analyses

An estimate of the electron and proton fluxes in the transfer and synchronous orbits and the protons in a solar flare model is presented in Section 9.1, Radiation Environment and Effects Predictions. These fluxes were converted to a damage-equivalent, normally incident 1-MeV electron flux by the use of an existing computer program, (Reference 3) which relates omnidirectional electron and proton fluxes to the

damage-equivalent, normally incident mono-energetic 1-MeV electron flux by the use of empirical shielding-dependent damage factors (Reference 4). Table 4 presents a summary of the 1-MeV flux calculations. The front and back solar-cell radiation shielding provided by the General Electric Rollout Solar Array is equivalent to 4 mils of fused silica (FS) and 2 mils of aluminum (Al), respectively. Other shieldings investigated were 4 mils FS and 4 mils Al, and 6 mils FS and 5 mils Al, respectively. The 1-MeV electron flux values in Table 4 show that the protons encountered in the 90-day transition to synchronous altitude produce the preponderant damaging flux. The synchronous protons are concentrated in the energy ranges which are easily stopped by only the rollup array shielding, and the damage produced by both the transition and synchronous electrons is relatively independent in the range of shielding thicknesses considered. The solar flare flux is significant, contributing about 5 times the 1-MeV electron flux produced by the trapped electrons.

The total 1-MeV electron flux computed from all the transition, synchronous and solar flare particle populations produces more than 50 percent degradation of solar array output power, even with the heavier shielding considered. In fact, very little experimental data on solar cell performance at these flux levels ($> 2.9 \times 10^{16}$ e/cm^2) has been reported. In order to provide the study effort with confident solar cell performance predictions, as well as to avoid a solar array configuration with at least a 2-to-1 overdesign margin, it is necessary to assume that the extremely damaging transition fluxes can be avoided. This may be achieved by one or a combination of techniques including:

1. Heavier solar cell shielding than that provided by the present rollup solar array,

2. Altering the flight path to synchronous altitude, or

3. Deploying only that portion of the total array needed to power the ion thrustor.

The loss in solar cell power, with the shielding provided by the General Electric Rollout Solar Array, is about 28 percent considering the synchronous electrons and protons only, and about 41 percent if the solar flare flux is also included. All array sizing and performance estimates for this study are based upon inclusion of synchronous altitude electrons and protons, and solar flare flux. A possible enhancement to mission performance is the concept of retracting the rollup solar array in advance of a predicted severe solar flare. The General Electric array design incorporates this feature, requiring approximately 20 watts for less than 5 minutes per 250 ft^2 (23.2 m^2) array section to perform the deployment or retraction operation. Intense flare activity can be present in the synchronous orbit for periods of up to one or two days in duration, indicating the need for electrical energy storage to maintain spacecraft orientation and to allow access to ground commands as well as to re-deploy the rollup array sections.

5.3.2.6 Solar Cell Temperatures

The following table presents solar cell temperatures based upon temperature profiles in Section 4, Environment Considerations. (1) The low temperature of -173^{o}C (+100^{o}K) establishes the minimum predicted eclipse temperature for array substrate mounted components. (2) High temperatures are presented for an unloaded array, Solar Cell Efficiency = 0, and a loaded array Solar Cell Efficiency = 8%. The 100 nautical mile (185 km) orbit case, for an unloaded array, establishes the maximum array ambient temperature (83^{o}C = 356^{o}K) for heat sink sizing and semiconductor device temperature calculations. Increasing orbit altitude to synchronous altitude substantially reduces the maximum temperature (by about 30^{o}C [^{o}K]). (3) Array area, series and parallel numbers of cells are temperature dependent but also depend on performance degradation considerations - which are discussed in Section 5.3.2.8.

Solar Cell Temperatures

	Low Temp	High Temp (Eff. = 0)	High Temp (Eff. = 8%)
100 NM (185 KM)	-80^{o}C (+193^{o}K)	+83^{o}C (+356^{o}K)	+73^{o}C (+346^{o}K)
19,300 NM (35,800 KM)	-173^{o}C (+100^{o}K)	+54^{o}C (+327^{o}K)	+43^{o}C (+316^{o}K)

5.3.2.7 Solar Module Assembly Losses

Solar cell module output includes the impact of (1) a 5% power reduction caused by the cover glass; it is a generally accepted value for the cover glass and optical coatings combination described in Section 5.3.2.3 and (2) a 1% voltage loss associated with solder and metal interconnect IR drops within the module. (3) The HVSA, for this study, is considered perpendicular to the sun vector, so that effective air mass zero solar intensity is 139.6 mw/cm^2 over the 3.8 cm^2 of active area of a 2 x 2 cm solar cell.

5.3.2.8 In-Orbit Cell Parameters

Solar cell I-V curves for a 2 x 2 cm cell, including module assembly losses, are presented in Figure 52 and the table below for Beginning of Mission and after 5 years. Minimum power availability occurs at 5 years, as shown in Figure 52 and determines array size. The array performance estimate, Section 7, System Performance Estimates, is based upon the Beginning of Mission synchronous altitude, +43°C (+316°K) array. The 100 nautical mile [185 km], +73°C (+246°K), case is illustrated in the following table to demonstrate that the "hot array" at the Beginning of Mission is not the power limiting situation.

In-Orbit Cell Parameters

		43°C (316°K)	73°C (346°K)
Beginning of Mission:	Isc	136 mA	138 mA
	Ipm	123 mA	124 mA
	Vpm	.432 V	.366 V
	Voc	.550 V	.484 V
	I@.358 Volts	134 mA	126 mA
5 Years in Orbit, Flux = 5.3×10^{15} 1-MeVe/cm^2	Isc	92.0 mA	
	Ipm	85.3 mA	
	Vpm	.358 V	
	Voc	.464V	
	I@.358 Volts	85.3 mA	
Key:	Isc = short circuit current		
	Ipm = maximum power current		
	Vpm = maximum power voltage		
	Voc = open circuit voltage		

5.3.2.9 Series-Parallel Arrangement

1. The number of series solar cells per building block will be determined by the maximum power voltage per cell at 5 years, at +43°C (+316°K), which is 0.358 volts.

2. The number of parallel 2 x 2 cm cells per building block is determined by the current per cell of 85.3 ma at 0.358 volts. Current output from other than 2 x 2 cm cells may be scaled directly from the area ratios.

3. Parallel cells are electrically connected together with common cell interconnect.

4. A bypass diode will be placed across each row of parallel cells, resulting in same number of bypass diodes as series cells. (Section 8, Reliability Analyses, provides the rationale for selection of this configuration.) Some selected electronic circuit designs may dictate use of redundant parallel cells in lieu of bypass diodes for small sections of the solar array.

5.3.2.10 Solar Cell Parameters Upon Leaving Earth Eclipse

The solar cell I-V curve will build-up rapidly immediately upon emergence of the solar array from the earth shadow (umbra). Section 5.2 included discussions of the potential problems associated with the presence of rapid voltage changes and excessive voltages. This section describes the calculations which develop solar cell characteristic data during the transient period following eclipse. The resulting data provided herein have been used to identify the voltage problems previously discussed.

Initially, an estimate was made of the increase of solar cell short-circuit current and open-circuit voltage with time after spacecraft emergence from the earth's shadow. A linear increase in solar intensity with time as the array passes through the penumbra was assumed. A full-intensity short-circuit current value of 140 milliamperes is specified for the selected solar cell type, and a penumbra (full geometric shadow to full sunlight) time of about 7.6 seconds and about 128 seconds was calculated for the 100 NM (185 km) and synchronous orbits, respectively. Since solar cell short-circuit current is proportional to illumination intensity, the current will increase linearly from 0 to 140 milliamperes in 7.6 and 128 seconds in the two orbits, as illustrated in Figure 53. It is known that "bending" of the sun's rays will introduce some illumination into the geometric shadow cone, but the magnitude is not known and is omitted from the intensity model.

The estimated solar cell open circuit voltage versus time in the 100 NM and synchronous orbits is shown in Figure 54. The starting point for the generation of each curve is at the time fully intensity is reached. The corresponding cell temperature is obtained from the temperature-time profile in Section 4, and the full intensity open-circuit voltage (Voc) is corrected by the Voc temperature coefficient, -2.2 $mV/^{o}C(mV/^{o}K)$. The nominal value of Voc at $+28^{o}C$ ($+301^{o}K$) is 0.580 volts, so that a $-160^{o}C$ $\left|+113^{o}K\right|$ the value of Voc would be 0.580 + .0022 (28-(-160)) = 0.994V. The change in open-circuit voltage due to intensity change is given by:

$$Voc = (A)\ (0.026)\ \left(\frac{T}{300}\right)\ \ln\frac{I_{sc2}}{I_{sc1}}\ , \text{ with}$$

T = temperature (^{o}K)

I_{sc1} = short-circuit current at intensity value 1

I_{sc2} = short-circuit current at intensity value 2

A = dimensionless number, usually between 1 and 3

The value of A is about 1 for intensities in the range of one-tenth to one sun, and about 3 for an intensity of about 0.01 sun. [Little is known about the dependence of A on very low intensities or very cold tempertures.]

As an example, the open circuit voltage at 12.8 seconds from the start of illumination in the synchronous orbit is determined as follows:

Voc ($28^{o}C = 301^{o}K$) = 0.580

Temperature at 12.8 seconds = $-160^{o}C$ ($113^{o}K$)

Intensity at 12.8 seconds = 0.1 sun

A = 1

Voc (12.8 sec) = $0.580 + 0.0022\ (28 + 160) + (1)\ (0.026)\ \left(\frac{113}{300}\right) \ln \left(\frac{0.1}{1.0}\right)$

= $0.580 + .0022\ (188) + (.026)\ (.377)\ (-2.3)$

= 0.971 V, which is plotted in Figure 54 at time = 12.8 seconds.

Solar cell I-V curves corresponding to time during the period of increasing intensity, and presented in Figure 55, were obtained by fitting an I-V curve shape to the corresponding Isc and Voc end points defined in Figure 53 and 54.

5.3.3 CONSIDERATION OF THIN-FILM SOLAR CELLS FOR HVSA

The use of 8-mil silicon cells, 3-mil coverglass and 1-mil coverglass-to-cell adhesive is responsible for 70% of the total solar array module weight (0.1682 lb/ft^2, or 0.716 Kg/m^2). A comparison of total array area and array blanket weight is presented in this section for the conventional silicon converter and the significantly lighter thin-film device.

Cadmium sulfide (CdS) thin-film cells are presently the most feasible alternative to silicon cells as a solar energy conversion device. A recent summary of the status of development of CdS cells (Reference 5) included the following data:

1. Standard Cell Size: 3 x 3 in, with 55 cm^2 active area
2. Conversion efficiency: 3.5% (Kapton-covered, AMO, +25°C)
3. Cell Weight: 1.75 gm per 3 x 3 inch cell

Allowing 2% area for inter-cell spacing, 15.68 3 x 3 inch CdS cells can be bonded to a square foot of rollout array Kapton substrate. The weight of a square foot of CdS array is then $\frac{15.68 \times 1.75 \text{ gm}}{454 \text{ gm/lb}}$ + 0.0500 (rollout SA less cells, glass and adhesive) = 0.1105 lb/ft^2 (0.54 Kg/m^2), compared to 0.1682 lb/ft^2 for Si (0.82 Kg/m^2)

An approximation to the relative total array area required for CdS cells compared to Si cells is determined by the inverse ratio of their conversion efficiencies:

$$\frac{\text{Area CdS}}{\text{Area Si}} \approx \frac{11.4}{3.5} = 3.26$$

Likewise, the relative weight of total solar array module area of CdS to Si is proportional to the area ratio and individual weights:

$$\frac{\text{SA Weight CdS}}{\text{SA Weight Si}} = 3.26 \times \frac{0.1105}{0.1682} = 2.14$$

The fact that charged particle irradiation causes a loss of about 40% of power in 5 years for the Si cells, and would not affect the CdS to any significant extent, would improve the area and weight ratios of CdS to Si. However, the susceptability of present-day CdS cells to degradation of output power due to humidity, thermal cycling and ultraviolet exposure should tend to offset the radiation induced power loss in Si.

The conclusion, based on data of recent CdS testing, is that at the present time severe area and weight penalties (up to a factor of 2 compared to silicon cells) would be associated with the use of the thin-film film cadmium sulfide cells. Anticipated improvement in energy conversion efficiency and ability of the CdS cells to withstand environmental effects may permit a more favorable comparison to silicon cells in the future.

Table 4. Results of Radiation Damage Investigation for Solar Cells

Equivalent Solar Cell Shielding Thickness				Damage-Equivalent, Normally-Incident 1-MeV Electron Flux ($e/cm^2/5$ yrs)						Solar Cell Power
Front (Fused Silica) MILS	Front (Fused Silica) MM	Back (Aluminum) MILS	Back (Aluminum) MM	Transition Electrons	Synchronous Electrons	Transition Protons	Synchronous Protons	Solar Flare Protons	Total 1-MeV Flux	Remaining at End of 5 Yrs (Percent)
* 4	0.1	* 2	0.05	1.0×10^{14}	6.5×10^{14}	1.5×10^{17}	4.2×10^{14}	4.2×10^{15}	1.5×10^{17}	< 50
4	0.1	4	0.1	0.9×10^{14}	5.9×10^{14}	8.4×10^{16}	1.9×10^{11}	2.2×10^{15}	8.6×10^{16}	< 50
6	0.15	5	0.13	0.8×10^{14}	5.1×10^{14}	2.8×10^{16}	0	8.5×10^{14}	2.9×10^{16}	≈ 50
4	0.1	2	0.05	--	6.5×10^{14}	--	4.2×10^{14}	--	1.1×10^{15}	72
4	0.1	2	0.05	--	6.5×10^{14}	--	4.2×10^{14}	4.2×10^{15}	5.3×10^{15}	59

* Front shielding of GE Rollup Solar Array is provided by 3 mils (0.075MM) of microsheet coverglass plus about 1 mil (0.025MM) of Sylgard 182 adhesive; backshielding is 2 mils (0.05MM) of Kapton plus about 1.5 (0.038MM) mils of GE SMRD epoxy adhesive

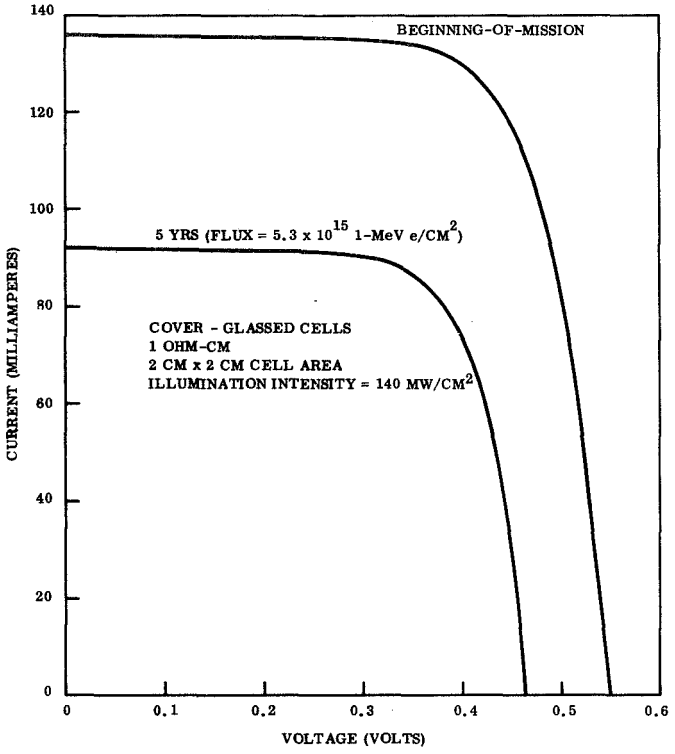


Figure 52. HVSA Solar Cell Current-Voltage Curves at +43°C (316°K)

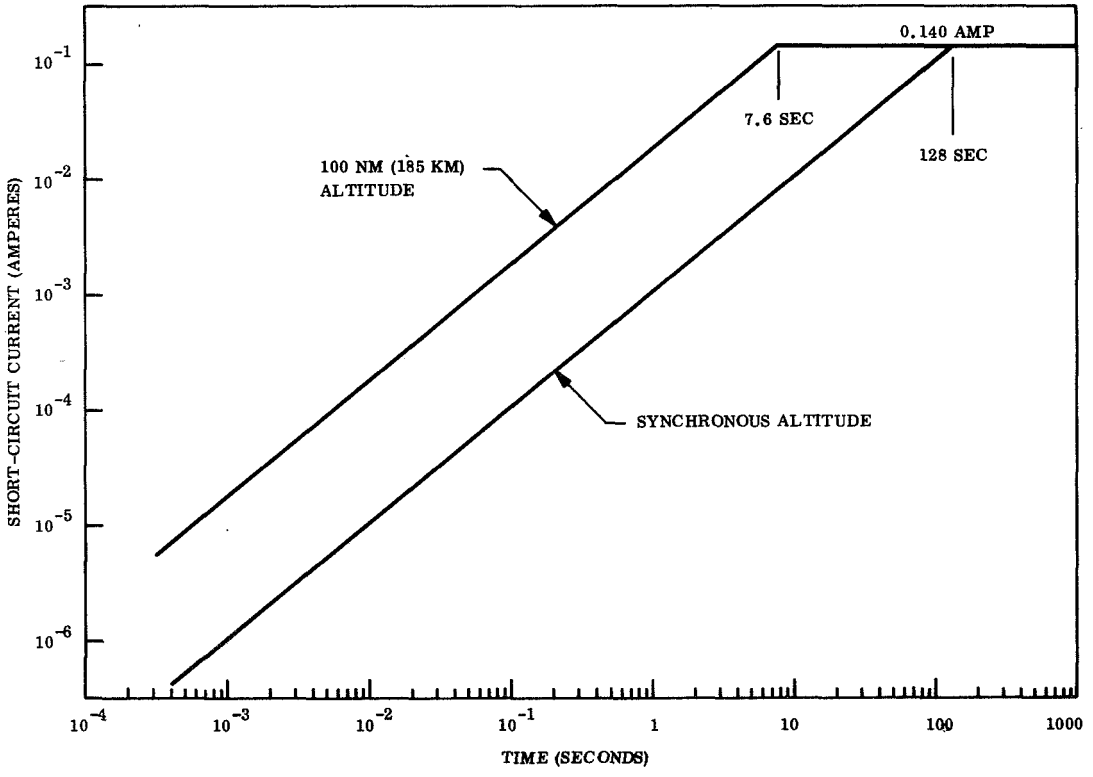


Figure 53. Estimated Solar Cell Current versus Time From Start of Illumination

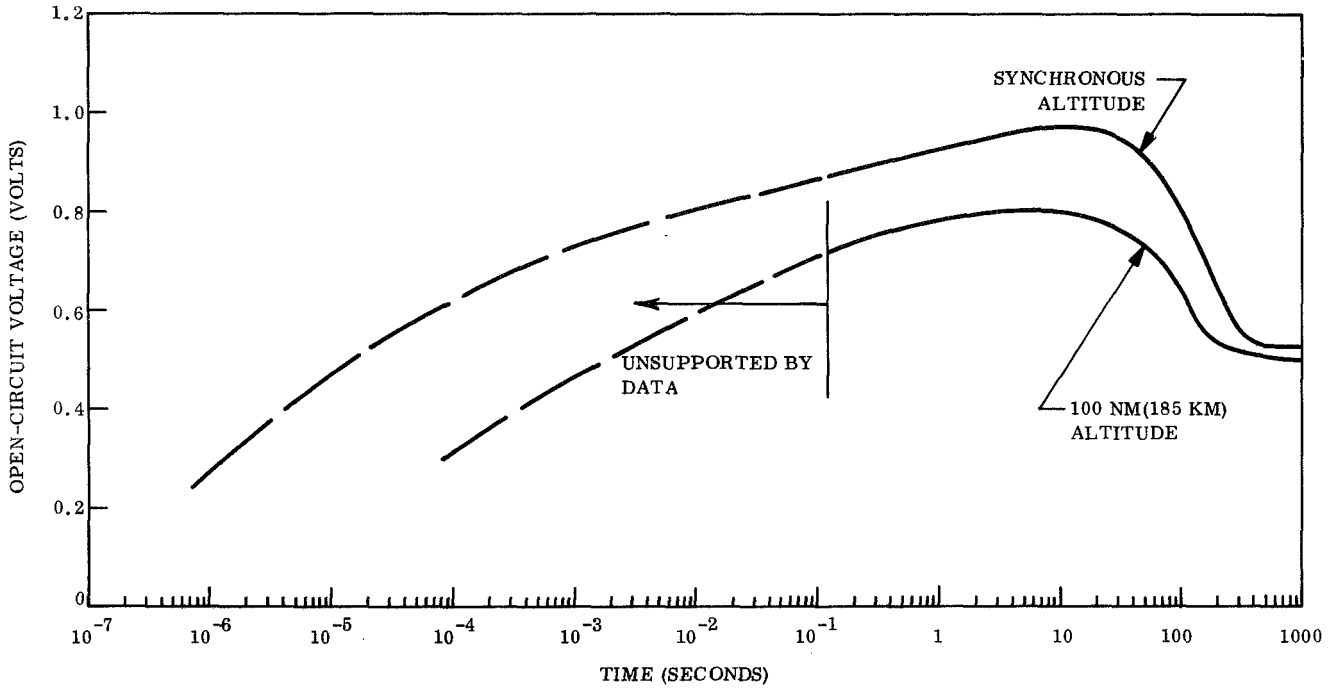


Figure 54. Estimated Solar Cell Voltage versus Time From Start of Illumination

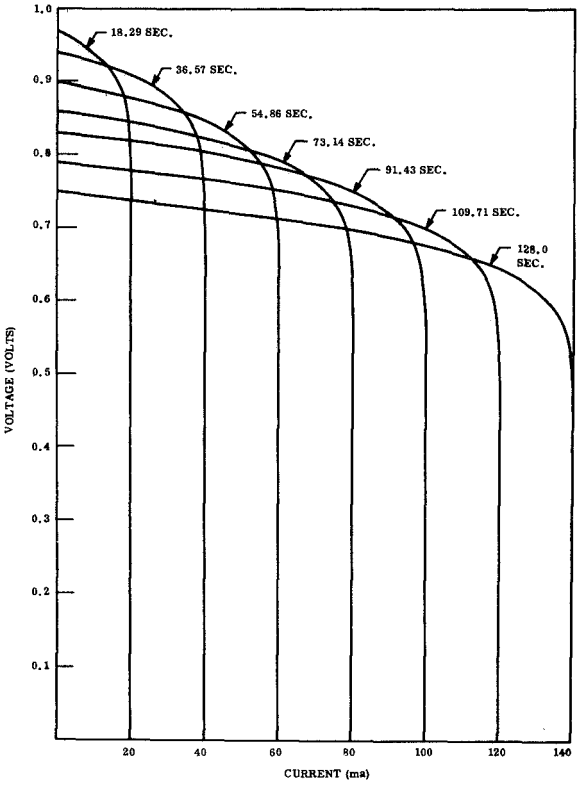


Figure 55. Solar Cell I-V Curves Emerging From Shadow in Synchronous Altitude

5.4 TRADEOFF ANALYSES

Several basic power system configurations have been investigated in an attempt to determine if an advantage could be realized by adapting an approach other than regulation by discrete switching. Alternate solar cell electrical connection and bypass diode configurations were considered from a reliability and failure effect standpoint. The impact on system efficiency of a wide range of building block output voltages and currents was investigated, resulting in the definition of a building block sizing criterion.

The results of the above tradeoff analyses are presented in the following paragraphs.

5.4.1 CONSIDERATION OF ALTERNATE POWER SYSTEM CONFIGURATIONS

In addition to the analysis of a system to maintain voltage regulation by the NASA Lewis Research Center preferred approach of discrete switching, several of the more conventional basic power system configurations which are usually compared during a system selection task were considered for applicability to the High Voltage Solar Array (HVSA) mission.

Figures 56, 57, 58, and 59 show fundamental representations of a series regulator system, shunt regulator system, maximum power tracker system and a discrete switching system. Usually an energy storage device (rechargeable battery) is included with each of the first three types of systems when considering an orbital mission, but they can be designed to operate without batteries, as shown.

The pass element shown in the series and shunt regulator systems can be either a series dissipative or switching (pulse-width-modulated) type. In the shunt regulator system, the dissipating element which is shown in series with the pass element can be resistive or may be replaced by the series dissipative pass element itself, if the total amount of power to be dissipated will permit this simplification. In general, a switching regulator is considerably more complicated than a series dissipative regulator but has higher power transfer efficiency and less pass element dissipation than the series dissipative type.

5.4.1.1 Series Regulator System

A series dissipative regulator (Figure 56) in the HVSA mission would have to accommodate a power dissipation in the regulator of up to two times the load power, since the solar array voltage can be as high as three times the desired regulated voltage and the current through the regulator is essentially the same as the load current. This would result in regulator dissipation values up to 2 Kw per 1 Kv, 1A building block, with a cold array and maximum load. The results of the thermal analysis reported in Section 4 show that under worst-case conditions the temperature of a semiconductor substrate 8 cm^2 in area is 94^oC ($+367^oK$) with a power dissipation of one watt in the semiconductor device. In order to maintain a safe operating temperature for the pass element, between one and two thousand regulator pass elements would be needed per 1 Kw building block to accommodate up to 2 Kw of dissipated power, with each element bonded to a radiating substrate 8 cm^2 in area.

5.4.1.2 Shunt Regulator System

A full shunt regulator system, as shown in Figure 57 would have to dissipate the total available array power at the building block voltage, under no-load conditions. Due to the necessary array overdesign to accommodate the expected 5-year degradation, this power would be approximately one and one-half times the 1 Kw required from the 1 Kv building block. The resulting 1.5 Kw of power to be dissipated in the shunt regulator elements would require in excess of one thousand semiconductor chip substrates, each 8 cm^2 in area, to assure safe temperatures. An improved shunt regulator system would be a "partial shunt" system, with the shunting elements connected across about 2/3 of the solar array. With this arrangement, the shunting elements would have to effectively short out 2/3 of the array at the extreme cold temperature to keep the building block voltage at the 1 Kv level. At the high steady-state array temperature at end-of-mission with a full load condition, the shunt would be effectively open and all available array power would be delivered to the load. However, high power dissipation will occur with this system also. At the high steady-state temperature under no-load conditions, the un-shunted 1/3 of the array would be at open-circuit voltage and the shunted 2/3 of the array would operate at a voltage slightly lower than the maximum-power voltage of the 2/3 portion of the array, in order to supply the required total building block voltage. At this voltage a current slightly greater than maximum-power current of the array would have to be shunted,

producing a power dissipation approximately equal to 2/3 of the total available array power, or about 700 watts per building block. For the same operating temperature and semiconductor chip substrate size criteria considered earlier, at least 500 pass elements would be required per 1 Kv building block with the partial shunt system.

5.4.1.3 Maximum Power Tracking System

The maximum power tracker systems (series or parallel tracker, Figure 58) can deliver the transient energy available from a cold solar array to the system. Maximum power tracking operation depends on a solar array power sensor controlling the duty cycle of the pulse-width modulated tracker unit such that the system operates at the solar array maximum-power voltage, and the presence of a suitable load to accept the transient energy (such as a battery requiring recharge). A pulse-width-modulated load voltage regulator is specified for tracker systems in order to optimize system efficiency. With a tracker system, an additional 20 to 25 percent of solar array energy can be delivered to the system in a low altitude orbit with a body-mounted or relatively heavy rigid solar array panel, compared to a non-tracking system. Another significant advantage of a tracker system is that it only takes from the array that power needed to satisfy the system loads, eliminating high power dissipation in series or shunt regulating elements.

It must be concluded that the tracker systems offer no advantage in the HVSA mission for two primary reasons: (1) the short-duration cold temperature transient of the lightweight rollup solar array in the synchronous orbit would yield less than one percent additional energy during an eclipse orbit with a tracker system, and (2) a suitable load to accent the time-varying transient energy is not present in the HVSA system.

5.4.1.4 Discrete Switching System

The discrete switching system (Figure 59) is described in detail in a binary version in Section 5.3 of this report. A total of 11 functional binary switches is required to maintain regulation within the required tolerance ($\pm 0.1\%$) at the 1 Kv building block level. Since the binary regulation switches operate in either the saturated or cutoff mode, minimum dissipation (one watt or less per switch) is incurred. Use of a quad switch arrangement for reliability purposes would result in even less power dissipation per semiconductor device, and still require less than fifty switching devices for each 1 Kv building block.

5.4.1.5 Conclusions

The extremely high number of transistors required to assure safe operating temperatures for the transistors in the series regulator and the shunt regulator systems presents a marked disadvantage to the use of either system in the HVSA application, compared to the relatively few devices needed in the discrete switching system. Additionally, it can be shown that the series regulator system introduces a significant efficiency penalty compared to the discrete switching system, and the requirement to supply drive current for analog control of the multicascaded pass elements in both the series and shunt regulator systems presents a critical design problem.

The capability of power tracking configurations present no advantage to the HVSA system, and implementation of the inductor and capacitor components required in microcircuit form would present a significant if not impossible, packaging challenge.

On the basis of the fundamental dissipation problem and the large number of regulating devices required with each system configuration considered, other than the discrete switching technique, it is concluded that the NASA-Lewis preferred approach to maintaining regulation by discrete switching is the most advantageous for the HVSA mission.

5.4.2 SELECTION OF SOLAR CELL ARRANGEMENT

Three basic methods of arranging solar cell interconnections, blocking diodes and bypass diodes were considered during this study. These three arrangements are designated Configurations A, B and C are shown in Figure 73 of Section 8, Reliability Analyses.

Configuration A would provide the greatest protection from short-to-ground types of failures, which however does not apply to an array with an insulating Kapton substrate. Redundancy is achieved by adding additional individual series strings of cells. In a typical 1 Kw, 1 Kv building block, this means providing 12 instead of 11 parallel 2 x 2 cm cells for the 5 year mission, resulting in redundancy increments equal to 9.1% of the basic array area. With one extra string of cells, protection is provided for the first cell failure, but should a second cell fail in one of the remaining strings, the mission design power cannot be provided. This has resulted in the lowest reliability number being predicted for Configuration A. With an open cell, or shadowed cell, in 2 or more strings, the array powering a lower order binary switching segment of the building block could be subjected to a reverse voltage condition. This would significantly impair building block regulation and may result in very high solar cell temperatures.

Configuration B achieves redundancy as in configuration A, with additional series strings of solar cells. Hence the reliability penalty is also significant for this configuration (9.1% for one redundant string in a 1 Kw building block). For the same number of redundant cells as Configuration A, however, the parallel interconnection between cells in every series row permits accommodation of many more cell failures, resulting in higher reliability predictions than for Configuration A. However, the occurrence of two or more cell failures, or two or more cells being shadowed, in a row of cells would produce the same severe impact on building block regulation as configuration A.

The highest solar array reliability estimate was achieved by Configuration C. Redundancy is provided by a small number (36 for a 1 Kv building block) of additional series rows of cells which are unswitched and always produce power. Failure of a cell results in forward biasing of the bypass diode connected across each row of cells. Selection of a bypass diode across each series row of cells was made to ensure a minimum disturbance of building block regulation in the event of a cell failure. It is recommended that in lieu of bypass diodes, additional parallel cells by employed in the cell rows associated with reference voltage for the controlled voltage regulation switches and with the lower order binary switched segments. This technique provides active redundancy and retains the ability to "fine tune" the building block output voltage with single cell voltage increments. Figure 60 summarizes the features of the solar cell and bypass diode connection arrangement recommended for the HVSA building blocks.

Table 5 presents the order of effectiveness of solar cell configurations A, B and C in the areas of providing high reliability, effect of a cell failure on regulation, shadow effects on regulation, and minimum total solar array area needed to achieve the apportioned solar cell reliability goal of 0.9998. The relative advantage of Configuration C in each area has resulted in its selection for the HVSA study.

Table 5. Comparative Ratings of Solar Cell Configurations

Area of Comparison	Solar Cell Configuration		
	A	B	C
Reliability Assessment	3	2	1
Failure Effect on Regulation	3	2	1
Shadow Effect on Regulation	3	2	1
Minimum Solar Array Area	2	2	1

5.4.3 CONSIDERATIONS OF BUILDING BLOCK OUTPUT VOLTAGES

An arbitrary building block voltage of 1 Kv has been used for general purpose design considerations during this study as being typically representative of a value which might be selected for a HVSA building block design. A certain conclusion to be made from the analytic investigations performed is that no single value of building block voltage (V_{BB}) is optimum for all system applications. Discussion is presented in this section of some of the more significant factors to be considered when selecting a building block voltage. The term "building block voltage", or V_{BB}, refers to the maximum value of output voltage a block can deliver, realizing that the block can be made to supply less voltage with proper signalling at the "down-count" input line.

Figure 61 presents plots of the percent regulation that can be achieved with a discrete switching system as a function of V_{BB}, for three solar cell temperatures. The solar cell open-circuit voltage temperature coefficient of -2.2 millivolts per degree centigrade is responsible for the degraded regulation effect at lower temperatures. A ground rule during this study has been that the HVSA will remain shorted after entering sunlight from an eclipse period until the array has reached a temperature of -55°C (218°K) or higher. This limitation is based on the unknown electrical performance of microcircuit components below this temperature. It is apparent from Figure 61 that significantly better regulation can be achieved over a wider temperature range with higher values of V_{BB}.

The range of V_{BB} that can be regulated with various numbers of binary switches is shown in Figure 62. The upper values of V_{BB} indicated are limiting; an 11-switch binary system can of course be used to regulate below 620 volts, although a 10-switch system would be slightly more efficient. In this example, the highest order (11th) switch in the 11-switch system would never be used (closed for V_{BB} values below 620 volts. An example of how to determine the minimum number of binary switches required for a given V_{BB} is presented in Section 5.2 of this report. It is noted from Figure 62 that the 11-switch binary system provides efficient operation over the widest range of V_{BB}, from 620 to 1340 volts, within the total voltage range considered.

Figure 63 illustrates the effect of using an 11-switch binary system for values of V_{BB} above 1340 V. The number of non-switched solar cells needed, in addition to the 2047 cells controlled by the 11 switches, in order to provide V_{BB} at end of life, increases with increasing values of V_{BB}. Above a V_{BB} of 1340 volts, the cold-temperature open-circuit voltage of the non-shorted cells produces a building block output voltage which is in excess of the desired V_{BB}. This over-voltage condition would exist until the array warmed up sufficiently to reduce the solar cell operating voltage. The curve in Figure 63 could be made to intersect the "regulation line" at a higher value of V_{BB} if regulation were not required until the array reached a temperature greater than -55°C. For example, if regulation were not required until the array temperature reached zero degrees centigrade (273°K) the 11-bit regulator could accommodate a 1600 volt building block, and the permissible V_{BB} is increased to 1900 volts if the array were kept in a shorted condition until the temperature reached +30°C (303°K). However, with the -55°C (218°K) ground rules for this study 1340 V represents an upper limit on V_{BB} for an 11-switch system.

As discussed earlier in this report, a building block can be operated at less than its maximum design voltage, with a corresponding proportional reduction of its power-delivering capability. If a block were operated at one-half of its V_{BB}, 50% of its power capability would be lost while operating at the reduced voltage. Figure 64 presents an illustrative example of the percentage of total HVSA power that could be lost if 3 building blocks were operated at a load voltage increment which is less than the design value of V_{BB}. In this example, the HVSA is composed of identical building blocks, i.e., either 8 2-Kv blocks, or 16 1-Kv blocks, or 32 500-V blocks, etc., each block having an output current capability of 0.94A. If three of the 8 2-Kv blocks were each operated at 1 Kv, then 3/16 (18.75%) of the total array capability is lost. If the array were composed of 16 1-Kv building blocks and 3 blocks were operated at 250 V, then $\frac{3 \times (1000 - 250)}{16 \times 1000}$, or about 14% of total power is lost. The conclusion to be drawn is that if many building blocks are to be operated at voltages less than their design V_{BB} values, less total array power is lost with lower values of V_{BB}.

Much of the auxiliary solar array area required for building block operation is fixed and independent of V_{BB}. For example, the drive power required for an 11-switch binary system is the same whether the design value of V_{BB} is 750 or 1300 volts, likewise, extra solar cells required to overcome stacking switch, blocking diode, or coupling diode voltage drops are the same for each building block, regardless of its output voltage. Consequently, these "fixed losses" result in a greater percentage of solar array area required as the value of V_{BB} is decreased, since more building blocks are required to total 16 Kv as V_{BB} is made smaller. The effect of building block voltage on solar array area "penalty" is presented in Figure 65. The solid line represents the percentage of total 15 Kw system solar array area that is required to provide all regulation, reconfiguration, and redundancy functions, as a function of V_{BB}. This figure assumes all building blocks in a given system to be identical in design, i.e., either 8 2-Kv blocks or 16 1-Kv blocks or 32 500 V blocks, etc. The dashed line is included in Figure 65 to indicate the relatively

small penalty that is associated with solar cell redundancy. As expected, a significant efficiency penalty is incurred with the selection of lower values of building block voltage. It must be noted, however, that in a specific system design, identical building blocks would probably not comprise the system, and a smaller array penalty than that shown would result from a more optimized design which eliminated unnecessary stacking switches, coupling diodes, etc. Figure 65 does not include the effects of load switches on required array area, since the use of load switches is not a "penalty" unique to a HVSA system.

Figure 66 presents the "solar array area penalty multiplier" as a function of the maximum value of building block output current. This multiplier must be applied to the array penalty values in Figure 65 if the building blocks are designed to provide less than the value of output current associated with a single-block-width system (0.94 ampere). The reason for the severe penalty involved with lower-current building blocks is the same as for the use of lower-voltage blocks --- many losses are fixed and independent of whether the block delivers 0.94A or a lower value of output current. Figure 66 also assumes that each building block in the system is identical in current output. If, for example, only several blocks in a system were designed to provide reduced current and the remaining blocks delivered 0.94A, the penalty would obviously be less than the worst-case situation shown.

The discussions presented in this section do not dictate an optimum value of V_{BB}, nor even a very narrow range of V_{BB}. However, the various considerations do indicate a trend of better regulation and higher efficiency associated with building block voltage in the range above 1 Kv, as opposed to values of V_{BB} much below this level. For purposes of illustratively selecting a typical general-purpose building block concept, the regulation considerations in Section 5.2, Power Conditioning, and the items presented in this section lead to the selection of an 11-switch binary system with controlled voltage quad transistor regulating switches, and operating at a maximum V_{BB} of between 750 and 1340 volts while providing 0.1% output voltage regulation.

From a system efficiency standpoint, it is desireable to minimize the total number of building blocks and to design the highest building block voltage and current that will accommodate the alternate loads when the HVSA system is reconfigured via ground command. Use of smaller building blocks results in fixed losses becoming a significant penalty in terms of total solar array area, weight and spacecraft interfaces.

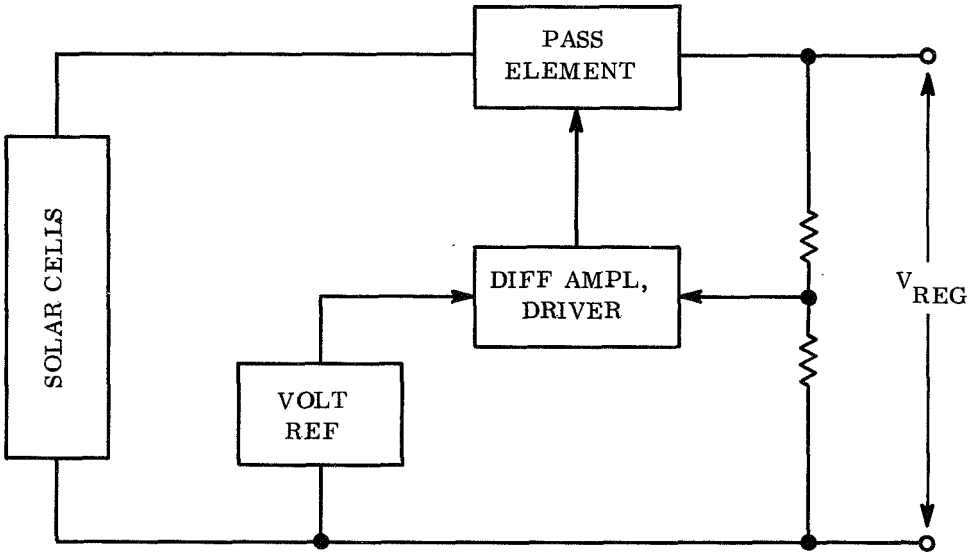


Figure 56. Series Regulator System

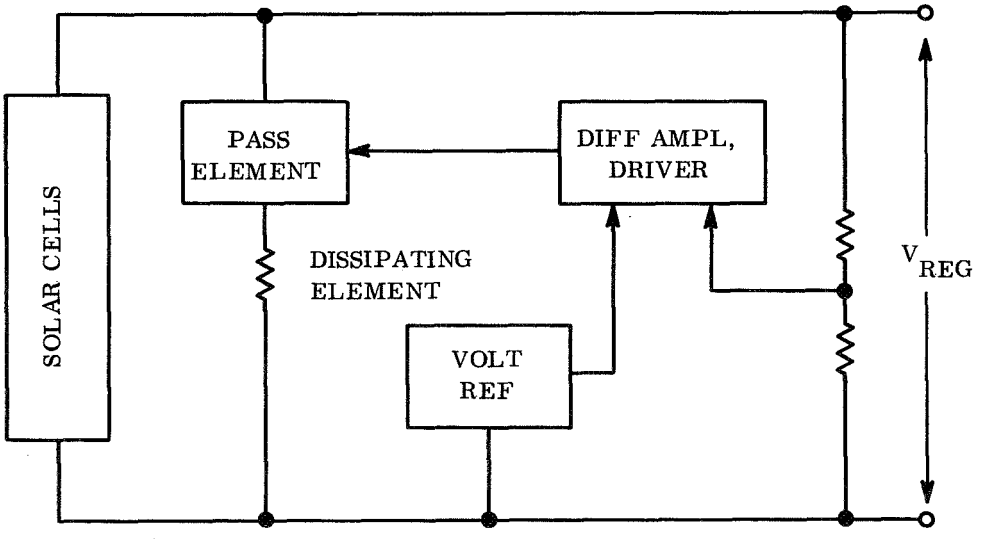


Figure 57. Shunt Regulator System

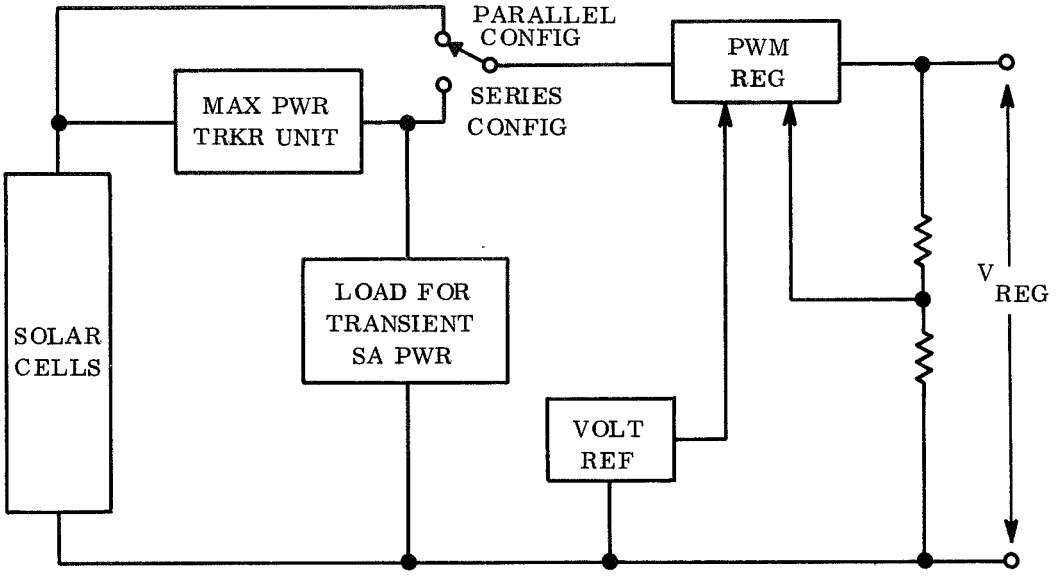


Figure 58. Maximum Power Tracker System

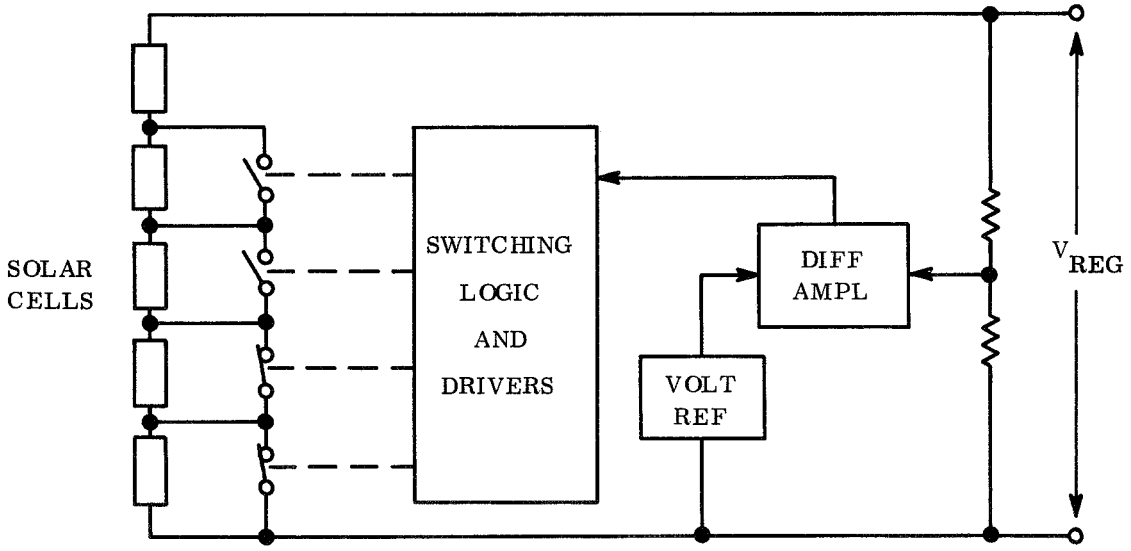


Figure 59. Discrete Switching System

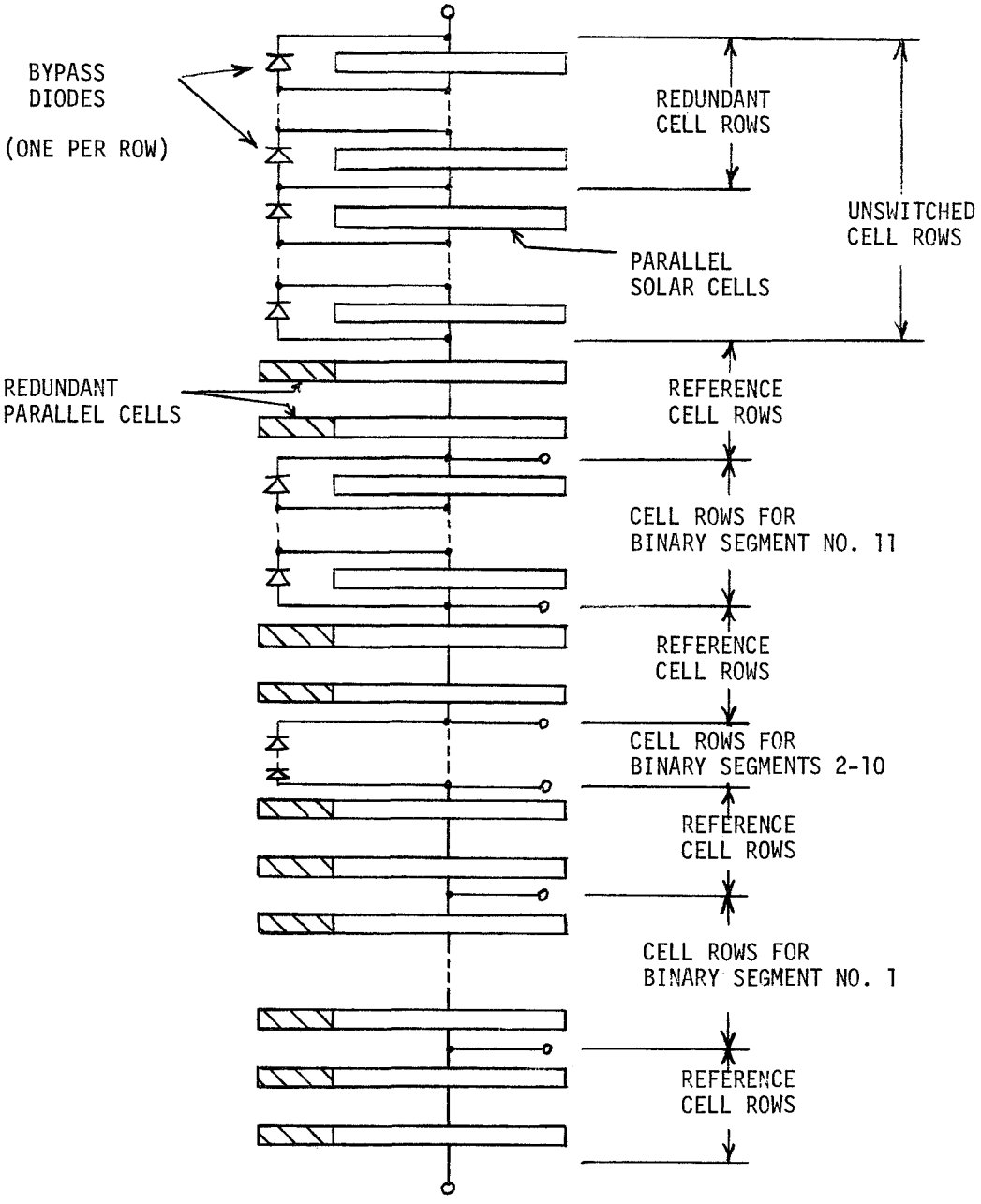


Figure 60. Selected Solar Cell and Bypass Diode Arrangement for HVSA Building Block

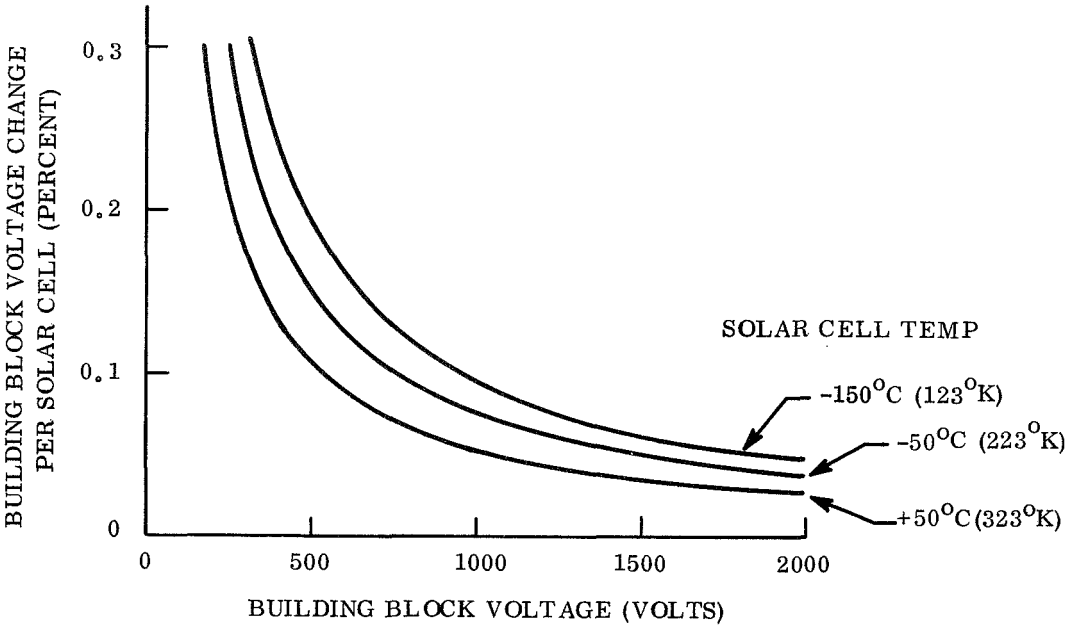


Figure 61. Percent Regulation versus Building Block Voltage at Three Solar Cell Temperatures

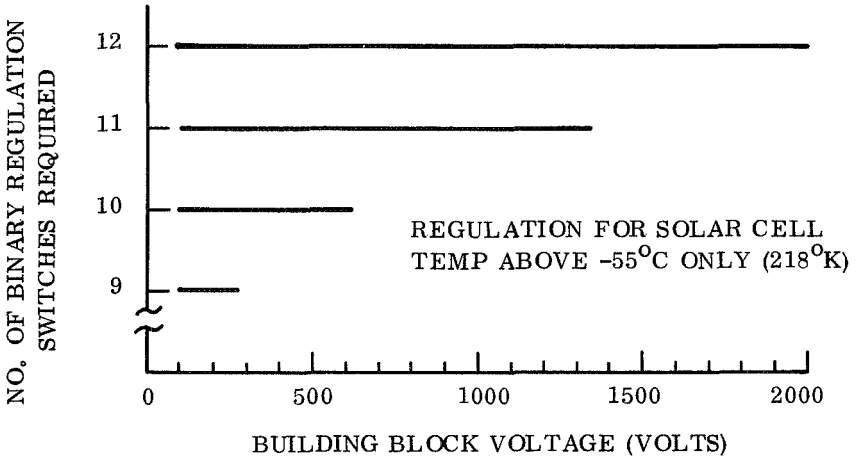


Figure 62. Number of Binary Switches Required versus Building Block Voltage

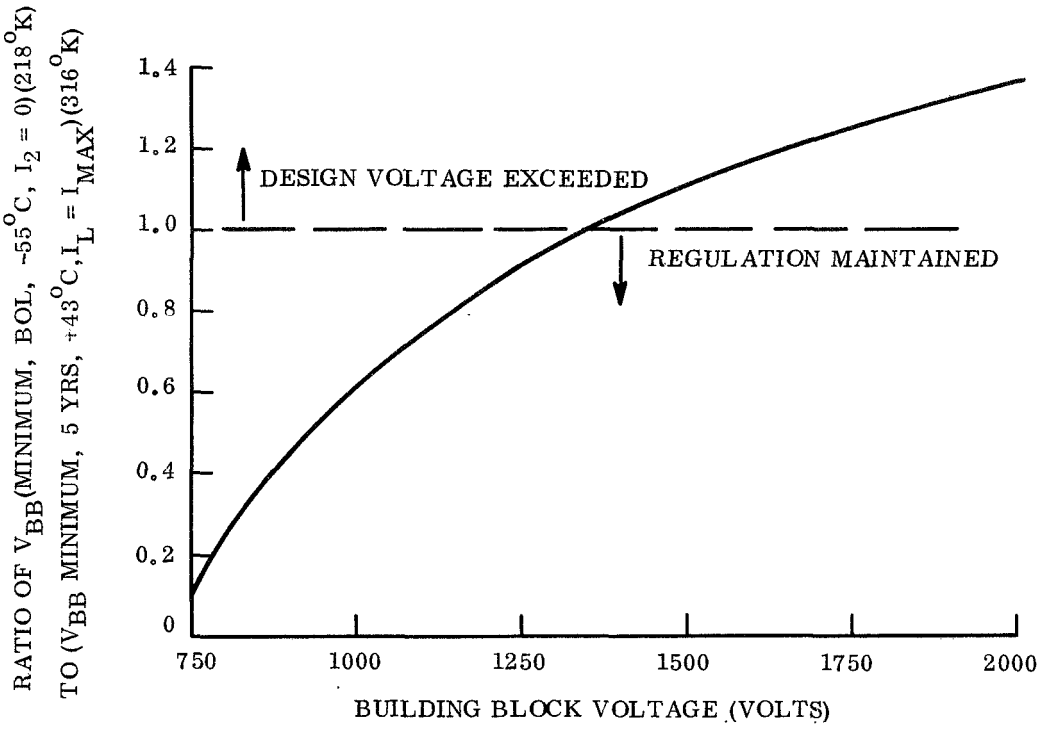


Figure 63. Voltage Regulation Range for 11-Switch Binary System

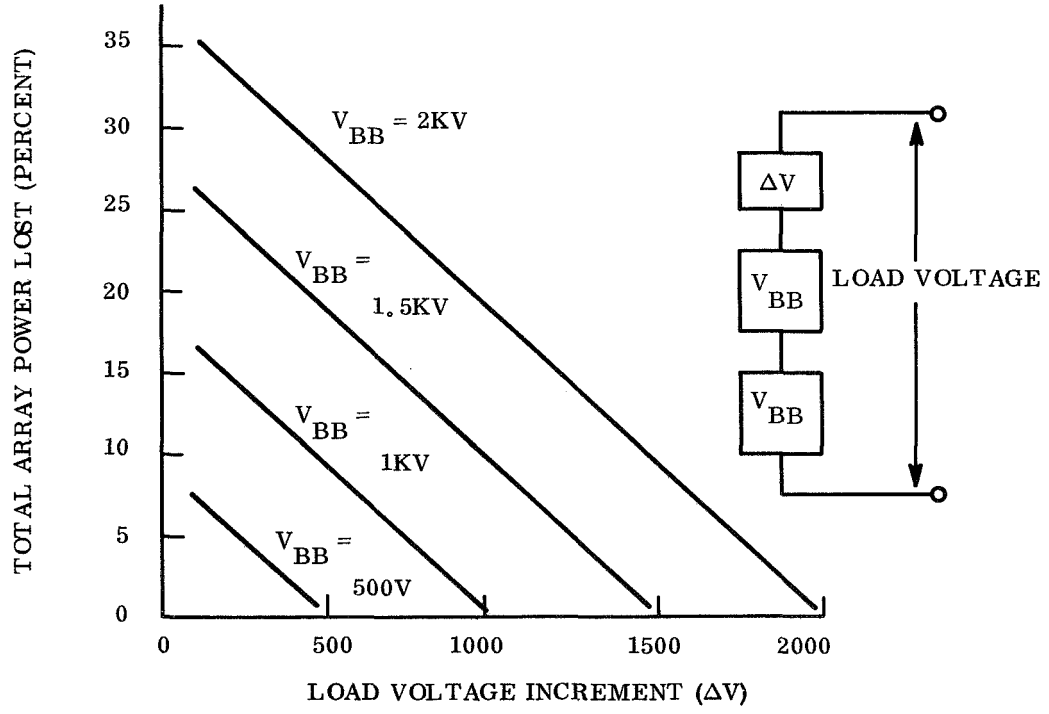


Figure 64. Effect of Incremental Load Voltage on Array Efficiency for Four Building Block Voltages

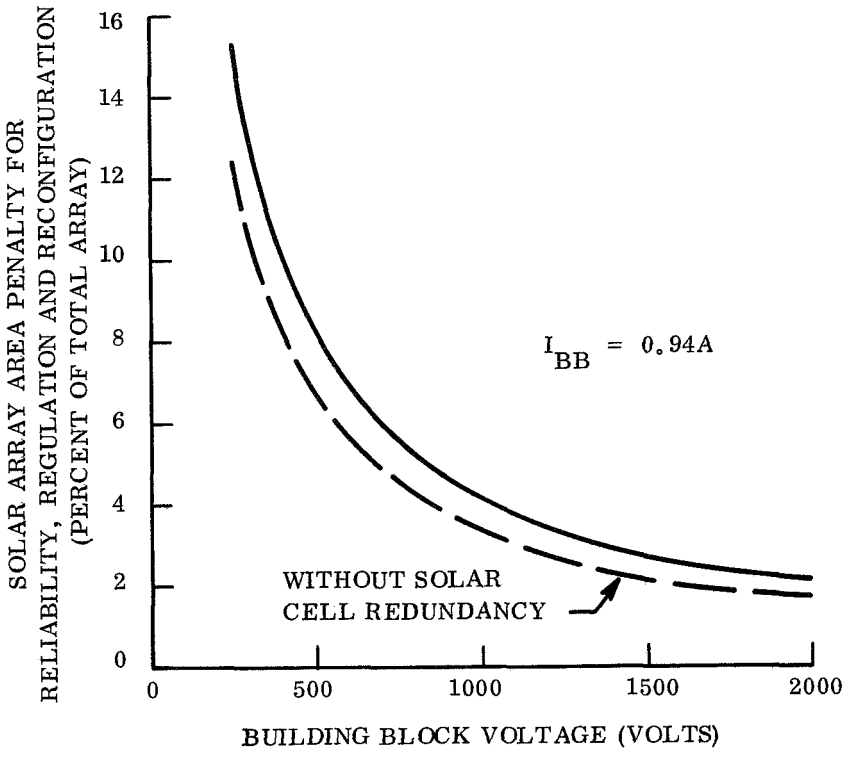


Figure 65. Solar Array Penalty versus Building Block Voltage

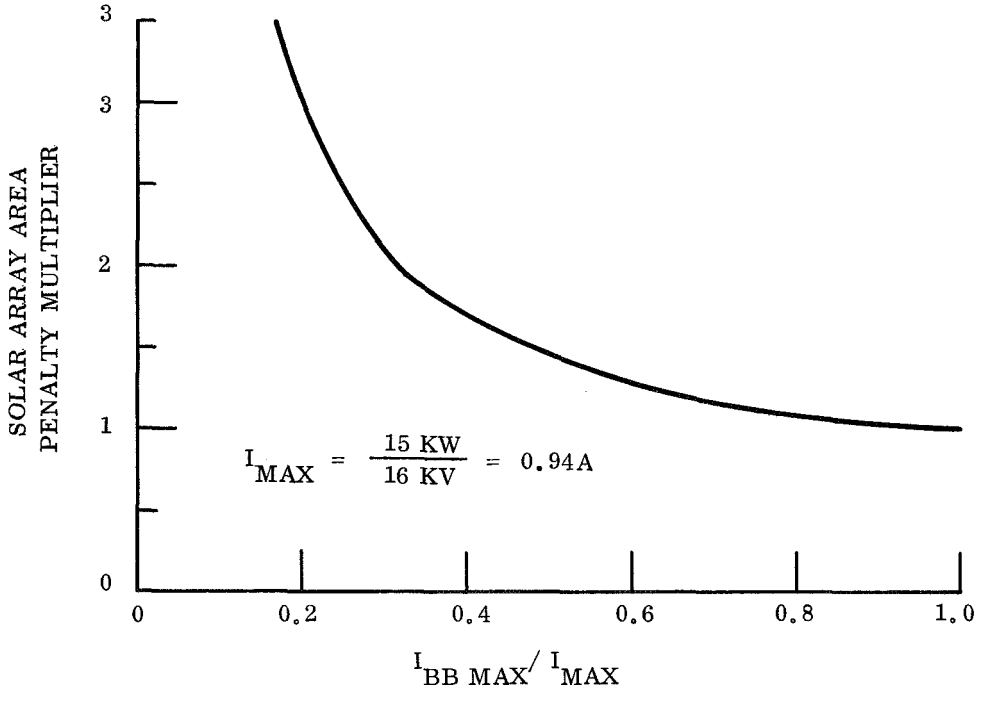


Figure 66. Influence of Reduced Building Block Current on Solar Array Penalty

SECTION 6

SELECTED SYSTEM CONFIGURATIONS

6.1 GENERAL

This section describes the general purpose building block configuration selected for the HVSA, presenting details of the sizing of the block for a specific application. Two HVSA system configurations are synthesized from load requirements, selected to be representative of switchable HVSA applications. The considerations of building block requirements to provide optimized systems are discussed, emphasizing system efficiency, high reliability and utilization of similar electrical functions wherever possible to minimize the extent of development effort required. Each of the two selected representative systems is capable of being reconfigured to accommodate two operational modes. These systems will serve as the basis for the performance estimates presented in Section 7.

6.2 BUILDING BLOCK DESCRIPTION

A functional block diagram of the general purpose HVSA building block is shown in Figure 67. The selected building block configuration is basically determined by the extremely high-reliability solar cell/bypass diode arrangement, "Configuration C", (Section 5.4), and the 11-switch binary regulation system with controlled voltage switches (section 5.4). All functional components in the selected building block configuration have been discussed in Section 5. The "Quad H" arrangement of blocking diodes is required to ensure that a low-voltage condition in one building block in a system will not allow that block to become a load to other building blocks connected in parallel with it. This technique is commonly used to isolate parallel strings of solar cells in a solar array configuration, preventing a shorted string of cells from becoming a current-demanding load on the remaining parallel cell circuits.

Figure 67 shows the building block having both a load switch and a load return/array ground switch. Both may not be employed at the same time; however, one switch could be used with the system in one configuration, and the other switch utilized in the reconfigured system mode. In the systems to be described, only those functions shown in Figure 67 that are required will be specified for each building block in the system. This will result in the elimination of coupling diodes, stacking switch, load switch and array ground switch in some of the building blocks.

An 11-switch regulator is shown in the general purpose block diagram. If greater than 1340V is required in a particular building block, a 12-switch regulator will be employed, for voltage requirements up to the specified building block design voltage limit of 1500 V.

A summary of the functional components and inputs and outputs associated with a typical general-case building block is shown in Figure 68. Note that the rollup solar array concept employs two identical Kapton blankets, and each blanket contains all the array-mounted components associated with a complete building block. With a concept utilizing 16 one-Kv building blocks, for example, eight rollup assemblies would be required if each blanket contained only one building block. Use of larger area rollup assemblies than the 250 ft^2 reference GE design would permit the accommodation of several building blocks on one rollup assembly.

Design of a HVSA system for a specific mission (particular voltage, current and switching demands) will result in some degree of nonsimilarity of building blocks and will reduce to a great extent the number of different components required on an array blanket section.

6.2.1 BUILDING BLOCK SIZING

The number of series-connected solar cells in a building block is determined by the required output voltage, voltage drops in the building blocks, extra cells required for reduncancy, and voltage drops outside the building blocks that must be provided for in part or entirely by the blocks being designed. The number of parallel solar cells is determined only by the required building blocks output current.

Section 5.3 of this report presents the 5-year solar cell I-V curve at the synchronous orbit steady-state array temperature of +43°C. Maximum-power voltage is 0.358V and maximum-power current is 85.3 mA for a 2 x 2 cm cell area with the described charged particle radiation damage. Minimum array area, a primary goal of HVSA design, is achieved by designing to operate the cells at this voltage at end of life, since this permits obtaining maximum energy from the array.

The calculation of the number of series and parallel solar cells for a specific building block is demonstrated below. The building block is typical of the blocks in the two HVSA systems defined in Section 6.3, being one of the five identical 1 Kv, 0.8A blocks required for System No. 2. This block required a stacking switch and coupling diodes so that it may be used to provide power in an alternate series-parallel arrangement of System No. 2 building blocks. It must also provide voltage to overcome the estimated voltage drops of 21 volts in a 7.5A load switch consisting of 2 series SCR devices with a 10 volt drop for each and the series turnoff transistor in the load switch, which has a 1-volt drop.

Number of Series Cells:

7.5A load switch $\frac{21 \text{ Volt Drop}}{0.358 \text{ volts/cell}}$	=	59
Coupling diodes (2 sets of quads)	=	12
Blocking diodes (1 quad)	=	6
Redundant series cell for reliability (12 + 24 for bypass diode drop)	=	36
Output voltage $\left(\frac{1000V}{0.358}\right)$	=	2795
Total series cells per BB:	=	2908 cells

Number of Parallel Cells: $\frac{0.8A}{0.0853A/\text{cell}} = 9.38 \rightarrow 10$ cells (2 x 2 cm)

Total Cells for Main Array within BB: 10 x 2908 = 29080

Main Array Area: $\frac{29080 \text{ cells}}{220 \text{ cells/ft}^2} = 132.1 \text{ ft}^2 = 12.3 \text{ m}^2$

Auxiliary Solar Array:

*	11 Quad Reg Switch	748
*	SA Short Switch	46
*	Stacking Switch	46
**	Counter, Power supply, LED Drivers	220
**	Load Switch Drivers 150/5 BB	30
		1090

Auxiliary Array Area: $\frac{1090 \text{ cells}}{220 \text{ cells/ft}^2} = 5.2 \text{ ft}^2 = 0.48 \text{ m}^2$

Total Array Area Per 1 Kv, 0.8A Bldg. Blk:

Main SA + Aux SA = 132.1 + 5.2 = 137.3 ft^2 = 12.6 m^2

This method of determining number of solar cells required and total solar cell module area was employed for each of the 25 building blocks in System No. 1, and the 16 building blocks comprising System No. 2.

* Obtained from circuit schematics in Section 5.0

** Estimated circuit power requirements

6.3 SYSTEM DESCRIPTION

Two HVSA system configurations have been selected for the purpose of making a performance estimate (determination of power to weight ratio and power to area ratio). These ratios will be compared to the comparable values for the low-voltage GE Rollout Solar Array, identifying the incremental area and weight penalties resulting from the use of high voltage and integral power conditioning, in Section 7. It is apparent that many system configurations can be conceived, each with different requirements. Consideration has been given to ensure that the two systems presented in this section include every significant functional capability investigation during this study.

Table 6 presents a list of representative basic load requirements and which of these requirements are demonstrated by each of the two system configurations. Each system supplies two sets of loads, identified as configurations "A" and "B" in Table 7. Reconfiguration of the building block series-parallel arrangement by spacecraft command is required to switch from one set of loads to the other. Table 7 also lists the load voltage, current and power requirements for each configuration of the two systems.

A functional block diagram of System No. 1 connected in configuration A is shown in Figure 69 with Figure 70 presenting the connection of System No. 1 in configuration B. Configurations A and B of System No. 2 are shown in Figures 71 and 72, respectively. The following nomenclature defines the elements of the systems in Figures 69 to 72.

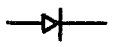
Building Block

Load

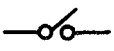
Connection to Spacecraft Ground

S1 to S9 — Load Switch for "Hot" side of Load

SG1, SG2 — Load Return/Array Ground Switch



Coupling Diode (Max. 1500 V)



Stacking switch (Max. 1500 V)

D1, D2, D3 — High Voltage Coupling Diode (Greater than 1500 V)

SS1, SS2 — High Voltage Stacking Switch (Greater than 1500 V)

A discussion of implementation of the stacking switches and coupling diode functions in System No. 1 which must block greater than 1500 V is included in Section 5.1.10.

In Figure 69 (Sys. No. 1, Configuration A), the coupling diodes D1, D2 and D3 are reverse biased, permitting no current to exist through them. The HVSA is grounded with switch SG1, which also provides the return path for load current from load L3. The -12 Kv required by L3 is supplied by the series connection of six 1.2 Kv blocks and four 1.5 Kv blocks, the latter also providing 0.6A at 6 Kv for load L2. Load L1 is provided with 0.1A at 4 Kv by the three 1.33 Kv blocks. Load L6 is supplied entirely by the single 1 Kv, 0.2A block, and load L5 obtains 3 Kv from the two 1.5 Kv, 0.5A blocks. The 10 Kv required by load L4 is obtained from the series connection of nine 1.2 Kv, 0.5A blocks, which operate at less than their maximum design voltage to provide 10 Kv. All stacking switches are closed and conducting in Configuration A, and all coupling diodes are reverse-biased and blocking current flow.

Figure 70 shows that loads L7, L8 and L9 only receive power in the configuration B connection of System No. 1. Unlike Configuration A, which supplied only negative voltages, Configuration B provides -2Kv to load L9, and +3.5 Kv to load 7 and +6 Kv to load L8, with the new ground reference point established with the array ground switch SG2. Load return current from all three loads is passed by switch SG2. This configuration shows the need for the nine 1.2 Kv, 0.5A blocks. They now operate at rated voltages, with three blocks paralleled by coupling diodes to provide a matrix of the nine blocks capable of supplying sufficient current and voltage for load L7. Note that the total current available at 3.5 Kv is 3 (0.5) + 2 (0.4) = 2.3A, and only 2A is required by the load. The entire current capability of each of the 1.2 Kv blocks is needed in Configuration A, which determines the current sizing, even though it is not required in the alternate configuration. In Figure 70 all stacking switches are open (not conducting) and all coupling diodes are passing current. It can be seen that the four 1.5 Kv, 1A blocks are retained in series for both configurations of System No. 1, thus there is no need for stacking switches or coupling diodes between them, and the;y are "hard-wired" in series. Only 21 of the 25 building blocks in System No. 1 are employed in Configuration B; the three 1.33 Kv blocks and the one 1 Kv block are "custom designed" for configuration A and serve no purpose in the alternate configuration.

Section 5.4.3 showed that significant system efficiency penalties accompanied the use of lower voltage and current building blocks to comprise a system, since more blocks resulted and the fixed losses per block added up to large auxiliary array area requirements. To avoid this penalty, the total number of building blocks must be kept to a minimum which is compatable with both configurations of a switchable system. Ideally, the building block would be "tailored" to one load, sized to provide the total load current with only one parallel block and designing the block voltage as high (up to 1500 V) as possible with the minimum number of identical series blocks resulting. However, in the use of the blocks in an alternate switched system arrangement of building blocks, the required block voltages and currents may not be the same.

The result is as discussed with System No. 1. In one configuration the blocks operate at a voltage lower than their maximum design value, but deliver their maximum current. In the alternate system configuration, the total block voltage capability is required but its total available current may not be needed. It is obvious then that maximum efficiency can be obtained if the building blocks are designed for one particular load only, but some power capability is not utilized when the block must accommodate several different load demands.

Inspection of the System No. 2 configurations shows that all stacking switches are closed and conducting in Configuration A, with all coupling diodes reverse biased. Switch SG 1 provides the return for loads L1, L2, L3 and L4, and also establishes the location of the ground connection to the HVSA so that -5 Kv and +11 Kv are simultaneously provided. In Configuration B, all power is delivered to a single, 7.5A load at 2 Kv, resulting in eight building blocks being coupled together with diodes to constitute a 1 Kv, 7.5A segment of the array, and a similar eight-block segment is series connected with it to meet the load demand at 2 Kv. All stacking switches are open in Configuration B, with all coupling diodes conducting. Note that the one 1.5 Kv block, designed to provide the necessary voltage source increment to power the 5 Kv load in Configuration A, is operated at only 1 Kv in parallel with the other blocks, in configuration B. Also, the 1.75A capability of the four blocks is needed to meet the current demand in Configuration B, and only need to deliver 1.70A in Configuration A. The use of slightly oversized blocks common to both configurations, however, results in a minimum total number of system building blocks and relatively high system efficiency.

Table 6. Requirements Demonstrated By Optimized System Configurations

LOAD REQUIREMENT TO BE DEMONSTRATED	SYSTEM NO.1	SYSTEM NO. 2
1. Reconfigure Building Block Series-Parallel Arrangement	X	X
2. Highest Load Current ($\frac{15\ KW}{2\ KV}$ = 7.5 A)		X
3. Low Value Building Block Output Current, Highest Voltage (16 KV)	X	
4. Multiple Voltage Taps, Unequal Load Currents	X	X
5. Voltage Tap at non-multiple of Building Block V_{BB}	X	X
6. Parallel Operation of Building Blocks with Different V_{BB}		X
7. Plus and Minus Output Voltages in Same Configuration	X	X
8. Non-ground Referenced Loads	X	

Table 7. Load Parameters for Optimized System Configurations

	LOAD NO.	VOLTAGE AND CURRENT	POWER
System No. 1	L1	-12 to -16 KV, 0.1A	0.4 KW
	L2	- 6 to -12 KV, 0.6A	3.6 KW
	L3	0 to -12 KV, 0.4A	4.8 KW
Config. "A"	L4	- 2 to -12 KV, 0.5A	5.0 KW
	L5	- 9 to -12 KV, 0.4A	1.2 KW
	L6	-11 to -12 KV, 0.2A	0.2 KW
			15.2 KW
	L7	0 to +3.5 KV, 2A	7.0 KW
Config. "B"	L8	0 to + 6 KV, 1A	6.0 KW
	L9	0 to - 2 KV, 0.5A	1.0 KW
			14.0 KW
System No. 2	L1	0 to +11 KV, 0.5A	5.5 KW
	L2	0 to + 5 KV, 0.5A	2.5 KW
Config. "A"	L3	0 to +3.5 KV,0.7A	2.5 KW
	L4	0 to -5 KV, 0.8A	4.0 KW
			14.5 KW
Config. "B"	L5	0 to +2 KV, 7.5A	15.0 KW

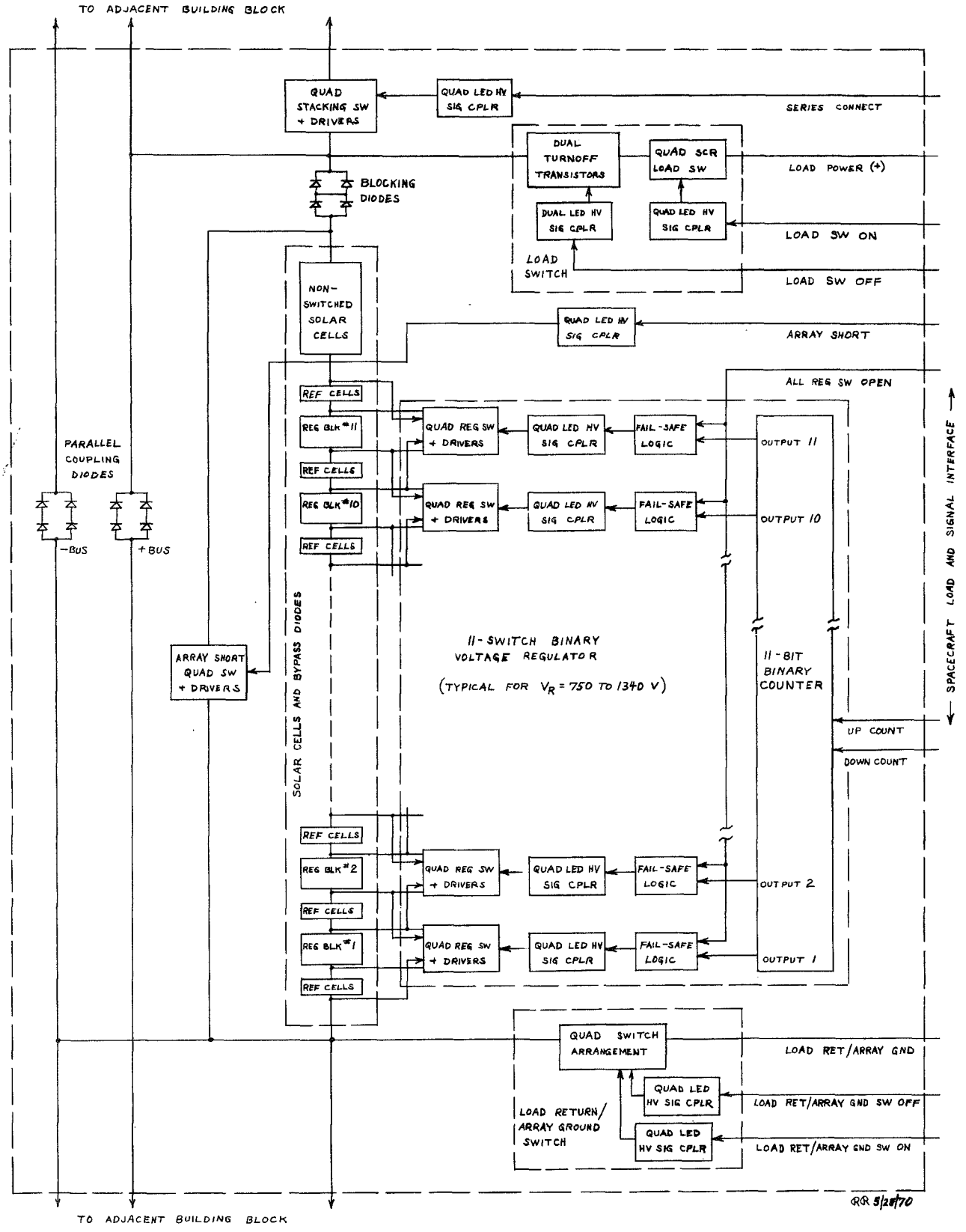


Figure 67. Functional Block Diagram Typical HVSA Building Block

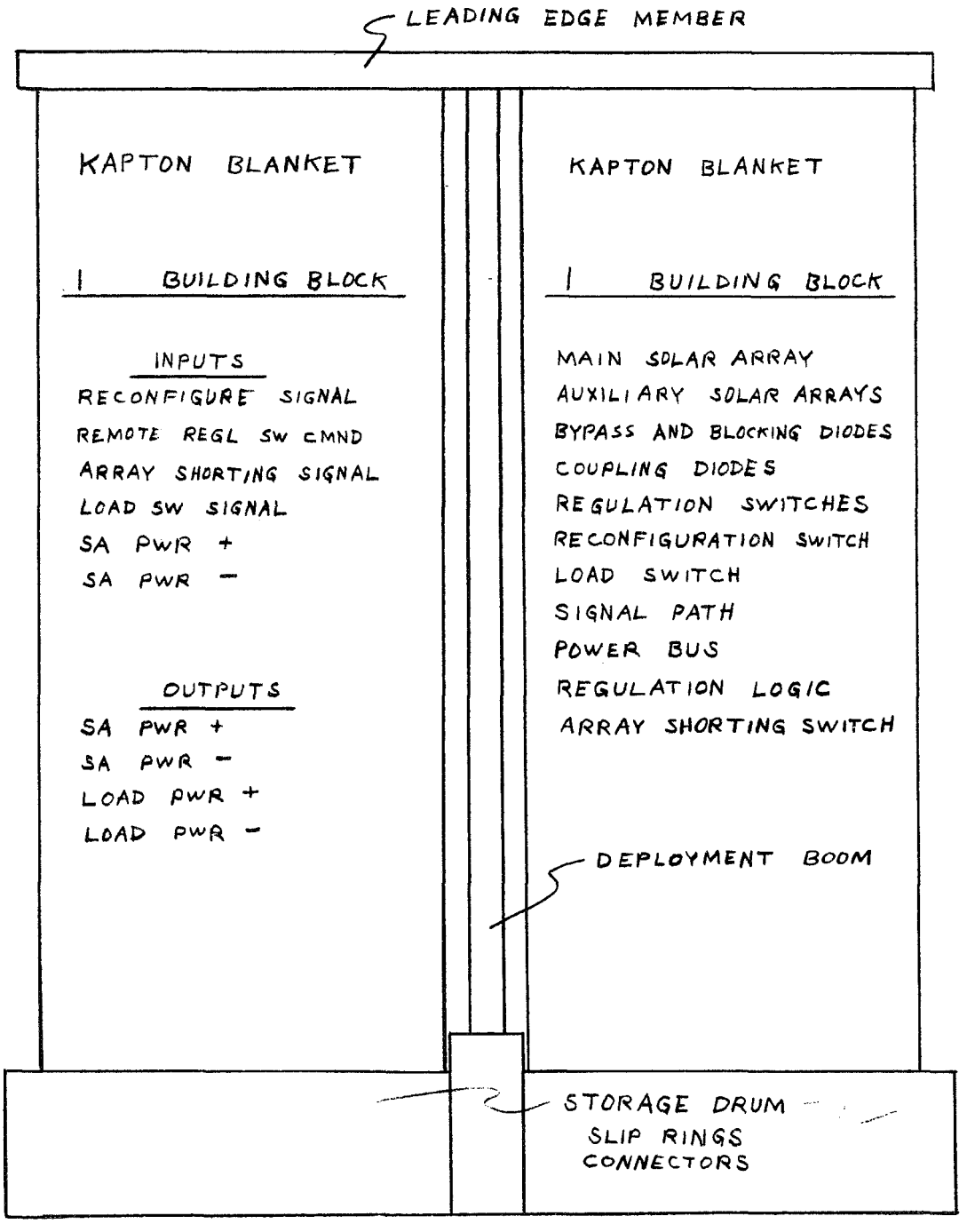


Figure 68. Rollup Solar Array with Two Building Blocks

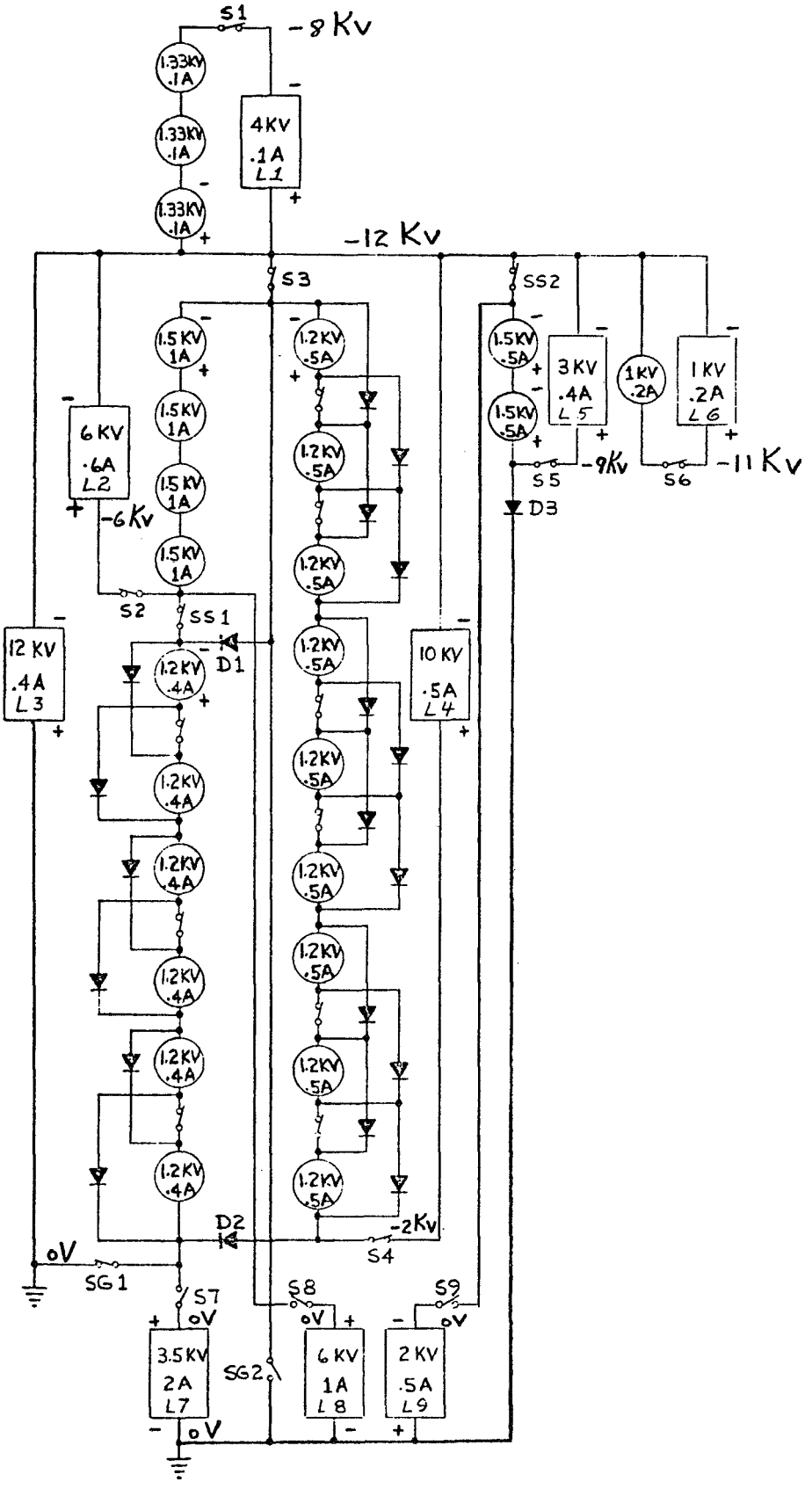


Figure 69. Functional Block Diagram of System No. 1 in Configuration A

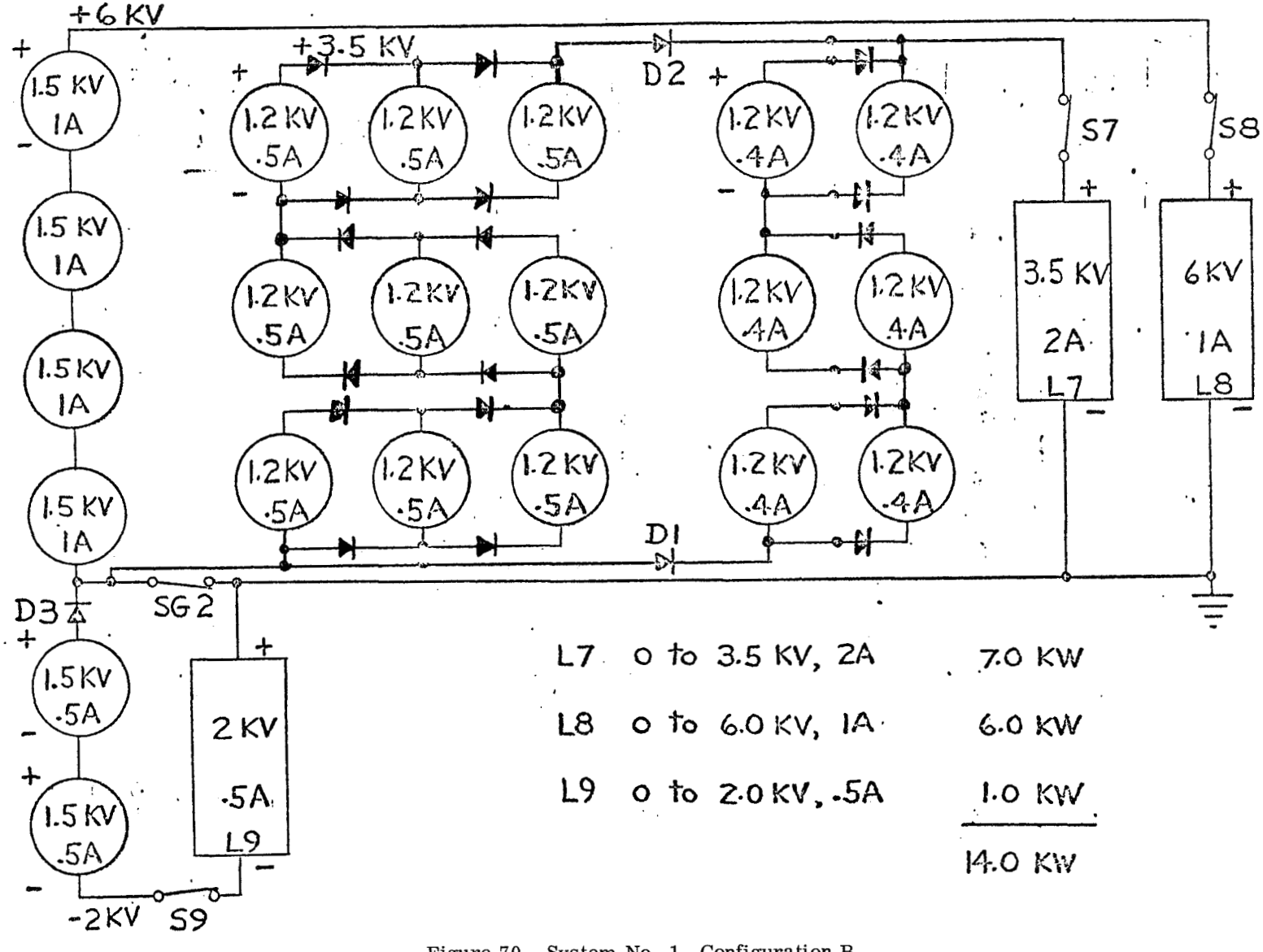


Figure 70. System No. 1, Configuration B

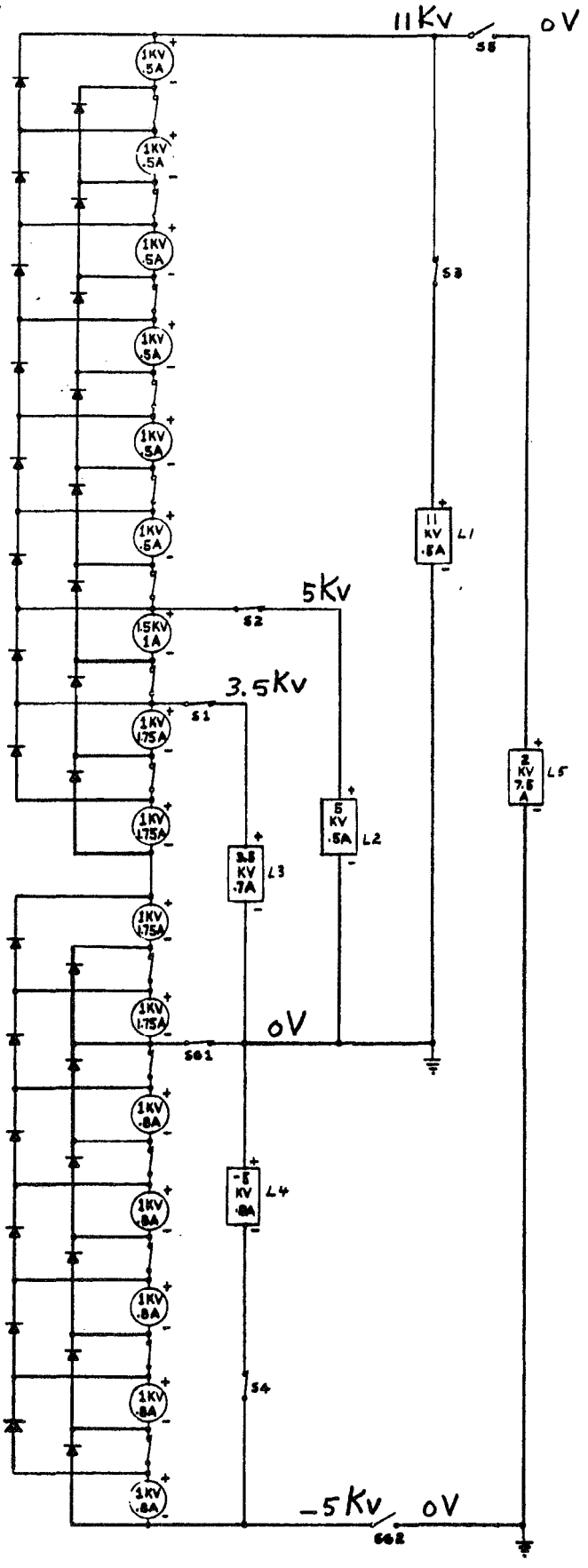


Figure 71. Functional Block Diagram of System No. 2 in Configuration A

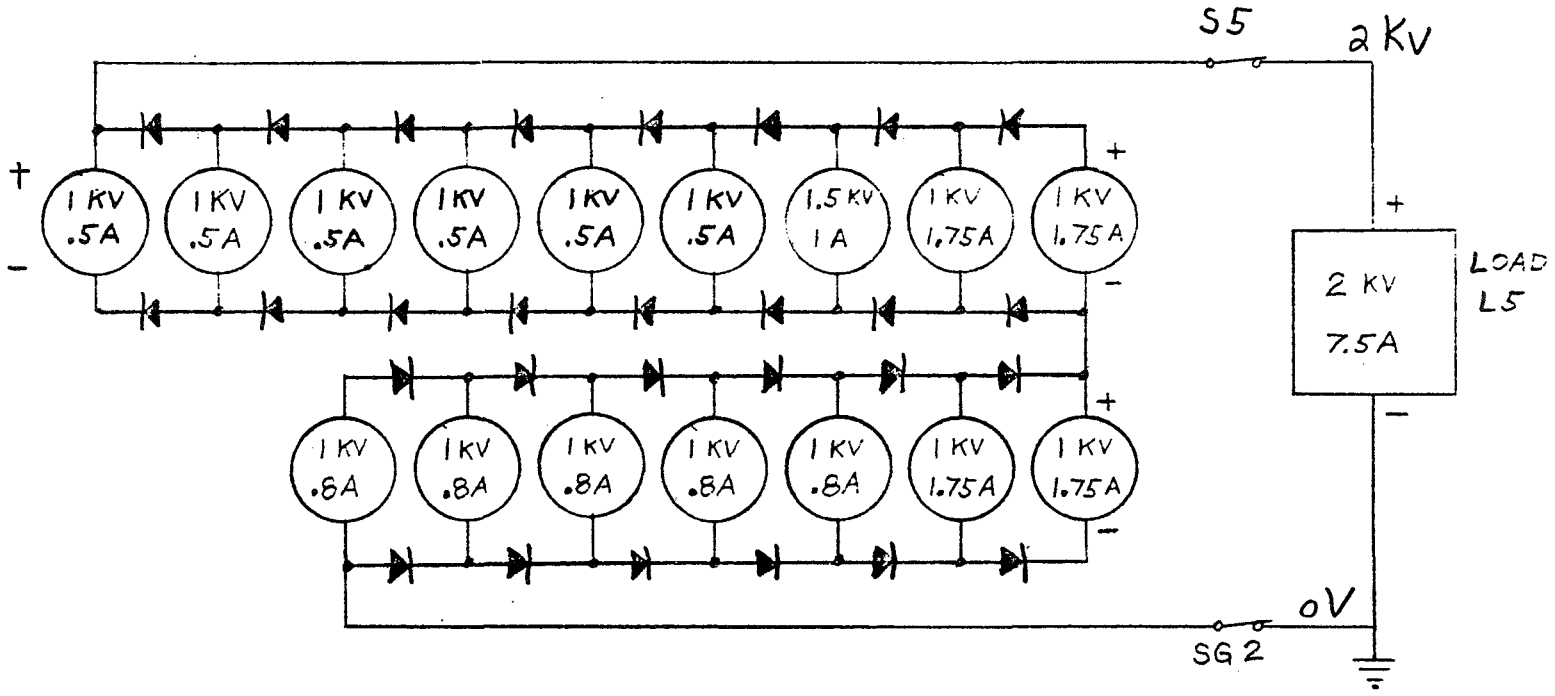


Figure 72. System No. 2, Configuration B

SECTION 7

SYSTEM PERFORMANCE ESTIMATES

7.1 GENERAL

The two HVSA system configurations described in Section 6, Selected System, and designated as System No. 1 and System No. 2, have been analyzed to determine output power, weight and area parameters. Additionally, a 1.5 kv 1.0A building block with an array area of 250 ft^2 (23.2 m^2) has been compared to the 250 ft^2 (23.2 m^2) baseline GE Rollout Solar Array, showing the incremental area and weight penalties associated with the array-mounted power conditioning and reliability required by the HVSA application.

7.2 NUMBER OF SOLAR CELLS AND ARRAY AREA

Table 8 presents the number of 2 x 2 cm solar cells needed for the various functions of System Nos. 1 and 2 and the 1.5 kw building block. The column headed "solar cells for load power" includes approximately one percent of cells which are required to achieve the apportioned solar array reliability goal of 0.9998 for the 5-year mission. The three columns under the "baseline" heading show the additional solar cells required to accommodate the basic regulation, load switch, and reconfiguration functions. The percentages in the "redundant cells" column reflect additional cells specified for redundancy of the regulation, load switch and reconfiguration circuits. It is seen from Table 8 that the basic power conditioning, load switch and reconfiguration functions result in less than a two percent array area penalty, and the additional cells needed to provide quad redundance of these circuit functions requires almost twice the baseline number

Summing the solar cells for Table 8 for each system and dividing by 220 solar cells per ft^2 (the solar cell packing factor achieved on the GE Rollout Solar Array) yields the total solar cells module areas shown in Table 9. An estimate of the additional Kapton substrate leader area* was made by scaling the 11.6 ft^2 (1.08 m^2) required for the 250 ft^2 (23.2 m^2) GE Rollout SA. The actual solar array area contributing to array output power at beginning of life (BOL) is shown in Table 9; determined by subtracting the array area required for regulation, circuit redundancy, blocking diode voltage drops and reconfiguration switch voltage drops.

7.3 ARRAY WEIGHT ESTIMATES

A summary of the packaged microelectronics weight for the HVSA building blocks used in the two system configurations is presented in Table 10. The weights range from 0.74 lb (0.33 Kg) for an 11-bit building block with no reconfiguration requirement to 0.91 lb (0.41 Kg) for a 12-bit building block with stacking switch and coupling diodes. Details of the redundant circuit weight calculation, including radiation shielding, are presented in Section 9.3, Microelectronics Package Weight Calculations.

Table 11 presents the total estimated weights for System No. 1 and System No. 2, with a breakdown of the major weight-contributing components. Note that the estimated weight of the array storage, deployment and power transfer components is scaled up from the 250 ft^2 (23.2 m^2) GE Rollout Solar Array, and has not been optimized for actual solar array required by the two HVSA systems.

The copper path requirements for low-level signals on the HVSA will be greater than those of the 100 V GE Rollout SA, but the output current is significantly less on the HVSA building block (maximum of 1.75 A as compared to about 25 A on the low-voltage array). Therefore, the weight contributed by electrical buses on the GE Rollout SA was retained with no reduction in estimating the HVSA weights.

7.4 ARRAY OUTPUT POWER

The maximum power available from the 2 x 2 cm cell used in the HVSA study (Section 5.3) is the product of 123 mA and 0.432 V per cell, at BOL at a steady-stage synchronous altitude array temperature of +43°C, (316°K). The packing factor of 220 cells per ft^2 (2370/m^2) results in an array output of 11.7 watts per ft^2 (126 watts/m^2) of area contributing to output power, as discussed in Section 7.2, when the array building blocks are operated at their maximum-power voltage.

*Leader Area: deployed Kapton substrate area which does not contain solar cell modules; it includes the initial wrap around the storage drum and the exposed substrate when the array is in the stowed position.

7.5 SYSTEM PERFORMANCE PARAMETERS

Table 12 presents the results of the performance estimates for the two HVSA system configurations and for the 250 ft^2 (23.2 m^2), 1.5 kw building block. The array output power, power-to-weight ratio and power-to-area ratio are presented for operation at both the maximum-power point and at regulated voltage. The performance estimates apply to an array surface perpendicular to the mean-intensity solar vector, at a temperature of +43°C (316°K) and with no orbital power degradation.

It is seen in Table 12 that the power available at regulated voltages at BOL is about 1.62 times the design value for the 5-year mission, due primarily to the effect of the charged particle environment (including solar flares) accommodated in the design.

7.6 COMPARISON OF HVSA TO GE ROLLOUT SA

A performance comparison of the low-voltage (100 V) GE Rollout Solar Array and the 1.5 kv, 1.0 A HVSA building block was selected because it is similar in area to the 250 ft^2 (23.2 m^2) baseline GE Rollout SA and therefore the weight of the array deployment and storage components are applicable to both arrays. To validate the performance comparison, the low-voltage GE array was assigned the same solar cell characteristics as the HVSA, and a 1-volt blocking diode loss was relegated to the low-voltage array (the original GE Rollout SA did not specify blocking diodes and the HVSA includes a 2-volt drop across a quad arrangement of blocking diodes).

The somewhat smaller area of the HVSA building block results in a 1 lb (0.454 Kg) lighter weight than the GE Rollout SA. However, the power-to-weight ratios show that about a 4.5% weight penalty is incurred by the quad-redundant regulation and switching circuits and their auxiliary solar array requirements.

Table 13 also shows the HVSA performance parameters with the building block supplying output current at regulated (1.5 kv) voltage. Delivering regulated power, the HVSA building block is capable of 9.6 W/ft^2 (104 w/m^2) and 32.0 W/lb (70.5 w/Kg), at beginning of life with a solar cell temperature of +43°C (316°K).

Table 8. Solar Cells Required for HVSA Functions

	SOLAR CELLS FOR LOAD POWER	REDUNDANT CELLS FOR CIRCUIT FUNCTION RELIABILITY	BASELINE (NO REDUNDANCY)		
			AUX ARRAY FOR REGULATION	LOAD SW DRVRS & VOLTAGE DROP	RECONFIGURATION STACKING SW BLOCKING DIODES COUPLING DIODES
SYSTEM NO. 1	558556 *	20614	7700	1732	982
(25 BLDG BLKS)	100%	3.7%	1.4%	0.3%	0.2%
SYSTEM NO. 2	531672	16264	5350	1876	1888
(16 BLDG BLKS)	100%	3.1%	1.0%	0.4%	0.4%
1.5 KV, 1.0 A	50782	1177	347	212	154
BLDG BLK	100%	2.3%	0.7%	0.4%	0.3%

* All numbers based on 2 x 2 cm cell area

Table 9. Solar Array Areas

	SYSTEM NO. 1	SYSTEM NO. 2
Total Solar Cell Module Area	2680 ft^2 (249m^2)	2532 ft^2 (235m^2)
Kapton Substrate Leader Area*	124 ft^2 (11.5m^2)	117 ft^2 (10.9m^2)
Total Solar Array Area	2804 ft^2 (260.5m^2)	2649 ft^2 (246m^2)
Solar Array Area Contributing to Output Power at BOL	2555 ft^2 (237m^2)	2430 ft^2 (226m^2)

* Scaled from 11.6 ft^2 (10.8 m^2) Leader Area for 250 ft^2 (23.2 m^2) GE Rollout SA

Table 10. Microelectronics Weight Estimate for HVSA Building Blocks

11 Quad Reg Sw 11 x .0253	0.278
11 Failsafe Logic for Reg Sw 11 x .00628	0.069
11 LED/Photo TX Quad 11 x .0056	0.060
1 Counter (11-Bit)	0.008
1 Blocking Diode Quad	0.017
1 SA Shorting Sw Quad	0.059
1 LED/Photo TX Quad	.006
	0.497 lbs (0.225 Kg)
2 Coupling Diode Quads 2 x .0298	0.060
1 Stacking Sw Quad	0.059
1 LED/Photo TX Quad	0.006
	0.125 lbs (0.057 Kg)
Bypass Diodes .0748 lbs per 1000 x 3.2	0.240 lbs (0.109 Kg)
12 Quad Reg Sw 12 x .0253	0.304
12 Failsafe Logic for Reg Sw 12 x .00628	.075
12 LED/Photo TX Quad 12 x .0056	.067
1 Counter (12-Bit)	.012
1 Blocking Diode Quad	.017
1 SA Shorting Sw Quad	.059
1 LED/Photo TX Quad	.006
	0.540 lbs (0.245 Kg)

*

SUMMARY - All E + Bypass Diodes (No Load Sw)	Weight Per Bldg Block
11-Bit with Stacking Switch and Coupling Diodes	0.862 lbs (0.391 Kg)
11-Bit No " " "	0.737 " (0.334 Kg)
12-Bit with " " "	0.905 " (0.410 Kg)
12-Bit No " " "	0.780 " (0.354 Kg)

*Microelectronics

Table 11. Estimated HVSA System Weights

SYSTEM COMPONENTS	WEIGHT	
	SYSTEM NO. 1	SYSTEM NO. 2
Total 4 E + SA Bypass Diodes*	19.8 lbs (9.0 Kg)	13.7 (6.2 Kg)
Redundant Solar Cells**	4.2 (1.9)	5.0 (2.3)
Auxiliary Solar Array*	19.9 (9.0)	14.2 (6.4)
Array for Load Sw Drvrs + Volt. Drop*	2.6 (1.2)	3.0 (1.4)
Array for Reconfig. (Blk + Cpl Diodes, Stk Sw)*	1.2 (0.6)	2.5 (1.1)
Main Solar Array for Load Power	422.3 (191)	401.0 (182)
Kapton Substrate Leader	2.1 (1.0)	1.9 (0.9)
Total Solar Array Blanket	452.3 lbs (205 Kg)	427.9 lbs (194 Kg)
Storage, Deployment, Pwr Transfer (Scaled up from 250 ft^2 (23.2 m^2) GE Rollout SA)	369 lbs (167 Kg)	348 lbs (158 Kg)
Total HVSA System Weight	841 lbs (381 Kg)	790 lbs (358 Kg)

* Weight includes accommodation of quad redundant circuit functions.
** Redundant cells to achieve apportioned solar array reliability goal.

Table 12. Results of System Performance Estimate

	SYSTEM NO. 1		SYSTEM NO. 2		1.5 KV, 1.0A BLDG BLOCK	
5 Year Mission Power Requirement	15.2 KW		15.0 KW		1.5 KW	
Total Solar Array Area	2804 ft^2	260.5 m^2	2649 ft^2	246 m^2	250.3 ft^2	23.24 m^2
Total System Weight	841 lbs	381 Kg	790 lbs	358 Kg	75.4 lbs	34.15 Kg
Power Output: Max Pwr Point, BOL,+43°C	29.8 KW		28.4 KW		2725 W	
Regulated, BOL, +43°C (316°K)	24.6 KW		24.4 KW		2410 W	
Power to Weight Ratio: Max Pwr Point	35.4 w/lb	78.2 w/Kg	36.0 w/lb	79.4 w/Kg	36.2 w/lb	79.9 w/Kg
Regulated	29.2 w/lb	64.5 w/Kg	30.9 w/lb	68.2 w/Kg	32.0 w/lb	70.5 w/Kg
Power to Area Ratio: Max Pwr Point	10.6 w/ft^2	114 w/m^2	10.7 w/ft^2	115.4 w/m^2	10.8 w/ft^2	117.2 w/m^2
Regulated	8.8 w/ft^2	94.5 w/m^2	9.2 w/ft^2	99.2 w/m^2	9.6 w/ft^2	103.7 w/m^2

Table 13. Performance Comparison, GE Rollout SA and HVSA

	GE ROLLOUT SA		HVSA BLDG BLOCK 1.5 KV, 1.0 A	
Main SA Module Area	250.1 ft^2	(23.2 m^2)	233.5 ft^2	(21.7 m^2)
Aux SA Module Area	-		5.2 ft^2	(0.48 m^2)
Total SA Module Area	250.1 ft^2	(23.2 m^2)	238.7 ft^2	(22.2 m^2)
Kapton Substrate Leader Area	11.6 ft^2	(1.08 m^2)	11.6 ft^2	(1.08 m^2)
Gross SA Area	261.7 ft^2	(24.3 m^2)	250.3 ft^2	(23.2 m^2)
Storage, Deployment, Power Transfer Weight	34.4 lbs.	(15.6 Kg)	34.4 lbs.	(15.6 Kg)
Auxiliary SA Blanket Weight	-	-	0.87 lbs.	(0.39 Kg)
Main SA Blanket Weight	42.0 lbs.	(19.0 Kg)	39.3 lbs.	(17.8 Kg)
Total SA Blanket Weight	42.0 lbs.	(19.0 Kg)	40.2 lbs.	(18.2 Kg)
Regulation and Reconfiguration E Weight	-	-	0.8 lbs.	(0.36 Kg)
Total SA Weight	76.4 lbs.	(34.6 Kg)	75.4 lbs.	(34.15 Kg)
SA Maximum Output Power (Pout Max.) (Main SA Cells at P_{max}, BOL, +43°C (316°K) Blk Diode = 1V GE, 2V HVSA	2895 w		2725 w	
$P_{Out\ Max}$/ Gross SA Area	11.1 w/ft^2	(119 w/m^2)	10.8 w/ft^2	(117 w/m^2)
$P_{Out\ Max}$/Total SA Weight	37.9 w/lb	(83.5 w/Kg)	36.2 w/lb	(79.9 w/Kg)
SA Output Power Regulated at 150OV BOL	-		2410 w	
P reg max/Gross SA Area	-		9.6 w/ft^2	(104 w/m^2)
P reg/Total SA Weight	-		32.0 w/lb.	(70.5 w/Kg)

SECTION 8

RELIABILITY ANALYSES

8.1 GENERAL

Reliability effort in this study was directed to (1) the analytical development of mathematical models for the array, switching, and power conditioning functions, (2) preparation of failure rate estimates for solar cells and electronic components, and (3) numerical evaluation of building block and systems reliability. Model development and evaluation, which were co-ordinated with the switching, power conditioning, and array analyses described in Section 5, established the redundancy requirements described. Reliability of the two optimized systems described in Section 7, was evaluated to ascertain how closely the study goal of 0.99 reliability (for 5 years in orbit) can be approached.

8.2 SOLAR CELL CONFIGURATION

8.2.1 INTRODUCTION

This analysis has been performed to evaluate the relative reliability of three specific solar cell configuations for a single switchable section (building block) of the high voltage solar array. For each of the three configurations the basic array section consists of "n" rows of cells, with "m" cells in each row. For this analysis, the "n" cells in each column of the array section are considered to be connected in series, and will be called a "string". Other cell connections within the array section will vary among the three configurations. Figure 73 presents the series-parallel solar cell and protection diode arrangement for the three configurations being considered in the reliability analysis.

Configuration A consists of (m + 1) strings of cells, with n cells and a blocking diode in each string. There are no parallel interconnections except at both ends of the array section. For this configuration, the basic array configuration was modified by the addition of one extra string to provide redundancy and by the addition of a blocking diode to each string to protect against individual string short-circuit failures.

Configuration B consists of (m + 1) strings of cells, with n cells in each string and parallel interconnections across each row of cells.

Configuration C consists of m strings of solar cells with (n + y) cells in each string. In this case $y = \frac{n}{m}$, so that the total number of cells is the same as for configurations A and B. The cells are series/parallel interconnected and have a bypass diode across each "x" rows. The purpose of the bypass diode is to provide a low voltage loss across a group of "X" rows in the event of an open-circuit failure within the group. The additional "y" rows of solar cells provide the voltage required for system operation when a group of "X" rows no longer supplies voltage.

8.2.2 RELIABILITY MODELS

The following definitions are used in the reliability models for the three configurations:

Pc = Probability of a single cell failure.

Rc = (1 - Pc) = Probability of a single cell not failing.

Pdo = Probability of a diode failing open.

Pds = Probability of a diode failing short.

Rd = (1 - Pdo - Pds) = Probability of a diode not failing.

8.2.2.1 Configuration A

Configuration A contains (m+1) strings of cells, and m of these strings are required for successful operation. Therefore, the array fails if more than one string fails, and is good if zero or one string fails. A string fails if either the diode or any one or more of the cells become open-circuited.

Let P1 = probability of a single string not failing.

$P1 = (1-Pc)^n (1-Pdo) = Rc^n (1-Pdo)$

$(P1)^{(m+1)}$ = probability of none of the (m+1) strings failing.

$(m+1)\ P1^m (1-P1)$ = probability of exactly one of the (m+1) strings failing.

RA = Probability of success for configurationA.

RA = Probability of none or one of the (m+1) strings failing.

$RA = P1^{(m+1)} + (m+1)\ P1^m (1-P1)$

$RA = (m+1)\ P1^m - m\ P1^{(m+1)}$

$RA = (m+1) \left[Rc^n (1 - Pdo)\right]^m - m \left[Rc^n (1 - Pdo)\right]^{(m+1)}$

8.2.2.2 Configuration B

For configuration B, the array section operates successfully if no more than one cell opens in each row. Since this array section has parallel interconnections across each row, the effect of a loss of one cell in each row is the same as the loss of one string in Configuration A.

Let P2 = Probability of no cells failing in a single row of (n + 1) cells.

$P2 = Rc^{(m+1)}$

Let P3 = Probability of exactly one cell failing in a single row of (m + 1) cells.

$P3 = (m+1)\ Rc^m\ Pc$

RB = Probability of success for configuration B.

$$RB = \sum_{i=0}^{n} \binom{n}{i} P_2^{\,i} P_3^{\,(n-i)}$$

$$RB = \sum_{i=0}^{n} \binom{n}{i} \left[R_c^{\,(m+1)}\right]^i \left[(m+1)\ Rc^m Pc\right]^{(n-i)} = \left[R_c^{\,m+1} + (m+1)\ R_c^{\,m} P_c\right]^n$$

where

i = number of rows with all cells good.

(n - i) = number of rows with m cells good and 1 cell failed.

8.2.2.3 Configuration C

Configuration C contains n + y rows of cells with m cells in each row. There are parallel interconnections between each row and a bypass diode across each x rows. The array section can therefore be considered as consisting of $\frac{n+y}{x}$ subsections with each subsection containing x rows of m cells. For the size of the array being considered, the diode bypass is required to pass array current, if one or more cells fail in any one or more rows of any subsection. Therefore a subsection is considered "good" only if all cells are good and the diode is not shorted.

In this configuration, y additional rows have been added for redundancy and up to $\frac{y}{x}$ subsection failures can therefore be tolerated where the value of x is constrained only by the condition that it be a submultiple of y, i.e. . $x = \frac{y}{i}$ where i = 1, 2, 3, ..y. It is intended to evaluate the array section reliability model for an optimum value of x, if it exists.

Failure for configuration C is therefore defined as failure of more than $\frac{y}{x}$ subsections.

The various states of cell rows and diodes to be considered for the model are as follows:

Condition	Cell Rows	Diodes
1	good	good
2	good	open
3	good	shorted
4	failed	shorted
5	failed	good
6	failed	open

The reliability model is developed by identifying and summing up all the good states, i.e. those states for which $\frac{y}{x}$ or fewer subsection have failed for each of the above conditions.

Condition 1 - Cells good and diodes good

P4 = Probability of all cells and diodes good

$$P4 = Rc^{m(n+y)}\, Rd\, \left(\frac{n+y}{x}\right)$$

Condition 2 - Cells good and diodes open

If all cells are good, one or more open diodes have no effect on array performance.

P5 = Probability of all cells good and one or more of the $\frac{n+y}{x}$ diodes open.

$$P5 = Rc^{m(n+y)} \sum_{i=1}^{\frac{n+y}{x}} \left[\binom{\frac{n+y}{x}}{i} Pdo^{i}\, Rd\, \left(\frac{n+y}{x} - i\right)\right]$$

$$= Rc^{m(n+y)} \left[(1-Pds)\left(\frac{m+y}{x}\right) - Rd\left(\frac{m+y}{x}\right)\right]$$

Condition 3 - Cells good and diodes shorted

Each diode short effectively fails one of the $\frac{n+y}{x}$ subsections, and, as indicated previously, up to $\frac{y}{x}$ subsection failures can be tolerated.

P6 = Probability of all cells good and diodes shorted for $\frac{y}{x}$ or fewer subsections.

$$P6 = \sum_{i=1}^{\frac{y}{x}} \binom{\frac{n+y}{x}}{i} (Rc^{mx}\, Pds)^{i} \left[Rc^{mx}\, (1-Pds)\right] \left(\frac{n+y}{x} - i\right)$$

Condition 4 - Cells failed and diodes shorted.

Cell failures can be tolerated in up to $\frac{y}{x}$ subsections with shorted diodes since array current will be bypassed through the diode regardless of whether the cells are good or bad.

P7 = Probability of one or more failed cells and shorted diodes in up to $\frac{y}{x}$ subsections.

$$P7 = \sum_{i=1}^{\frac{y}{x}} \binom{\frac{m+y}{x}}{i} \left[(1 - Rc^{mx})\ (Pds)\right]^{i} \left[\ Rc^{mx}(1-Pdo)\right]^{(\frac{n+y}{x} - i)}$$

Condition 5 - Cells failed and diodes good.

Up to $\frac{y}{x}$ subsections of mx cells each can fail if the corresponding diode for each failed subsection is good.

P8 = Probability of one or more failed cells and good diode for up to $\frac{y}{x}$ subsections.

$$P8 = \sum_{i=1}^{\frac{y}{x}} \binom{\frac{n+y}{x}}{i} \left[(1 - Rc^{mx})\ Rd\right]^{i} \left[Rc^{mx}(1-Pds)\right]^{(\frac{n+y}{x} - i)}$$

Condition 6 - Cells failed and diodes open.

There are no good states under condition 6.

$$R\bar{c} = P4 + P5 + P6 + P7 + P8$$

where

$$P4 = Rc^{m(n+y)}\ Rd^{(\frac{n+y}{x})}$$

$$P5 = Rc^{m(n+y)} \left[(1-Pds)^{(\frac{n+y}{x})} - Rd^{(\frac{n+y}{x})}\right]$$

$$P6 = \sum_{i=1}^{\frac{y}{x}} \binom{\frac{n+y}{x}}{i} (Rc^{mx}\ Pds)^{i} \left[Rc^{mx}(1-Pds)\right]^{(\frac{n+y}{x} - i)}$$

$$P7 = \sum_{i=1}^{\frac{y}{x}} \binom{\frac{n+y}{x}}{i} \left[(1-Rc^{mx})\ (Pds)\right]^{i} \left[Rc^{mx}(1-Pds)\right]^{(\frac{n+y}{x} - i)}$$

$$P8 = \sum_{i=1}^{\frac{y}{x}} \binom{\frac{n+y}{x}}{i} (1-Rc^{mx})\ (Rd)^{i} \left[Rc^{mx}(1-Pds)\right]^{(\frac{n+y}{x} - i)}$$

$$P4+P5 = Rc^{m(n+y)}\ (1-Pds)^{\frac{n+y}{x}}$$

$$P6+P7 = \sum_{i=1}^{\frac{y}{x}} \binom{\frac{n+y}{x}}{i} Pds^{i}\ (1-Pds)^{(\frac{n+y}{x} - i)} \left[Rc^{mxi} Rc^{mx(\frac{n+y}{x} - i)} + (1-Rc^{mx})^{i}\ Rc^{mx(\frac{n+y}{x} - i)}\right]$$

since Rc^{mx} and $(1-Rc^{mx})$ are mutually exclusive,

$$Rc^{mxi} + (1-Rc^{mx})^{i} = \left[Rc^{mx} + (1-Rc^{mx})\right]^{i} = 1$$

Therefore:

$$P6 + P7 = \sum_{i=1}^{\frac{y}{x}} \binom{\frac{n+y}{x}}{i} Pds^{i} \left[Rc^{mx}\,(1-Pds)\right]^{(\frac{n+y}{x} - i)}$$

and

$$P4 + P5 + P6 + P7 = \sum_{i=0}^{\frac{y}{x}} \binom{\frac{n+y}{x}}{i} Pds^{i} \left[Rc^{mx}\,(1-Pds)\right]^{(\frac{n+y}{x} - i)}$$

Rc = Probability of success for configuration C.

$$Rc = \sum_{i=1}^{\frac{y}{x}} \binom{\frac{n+y}{x}}{i} \left[(1-Rc^{mx})\,Rd\right]^{i} \left[Rc^{mx}\,(1-Pds)\right]^{(\frac{n+y}{x} - i)}$$

$$* \sum_{i=0}^{\frac{y}{x}} \binom{\frac{n+y}{x}}{i} Pds^{i} \left[Rc^{mx}\,(1-Pds)\right]^{(\frac{n+y}{x} - i)}$$

where the asterisk (*) indicated the convolution of the two expressions.

The model for configuration C can be stated in explicit from by considering the appropriate terms of the convolution, as follows:

$$R\bar{c} = \sum_{j=0}^{\frac{y}{x}} \sum_{l=0}^{\frac{y}{x} - j} \frac{(\frac{n+y}{x})!}{j!\,l!\left[\frac{n+y}{x} - (j+l)\right]!} \left[Pds\right]^{j} \left[Rd\,(1-Rc^{mx})\right]^{l} \left[Rc^{mx}\,(1-Pds)\right]^{A}$$

$$\text{where } A = \left[(\frac{n+y}{x}) - (j+l)\right]$$

8.2.3 APPORTIONMENT

Prior to the computation of predicted reliability for the three solar cell configurations, the system reliability goal of 0.99 for a 5 year mission was apportioned to lower level assemblies. The objective of this apportionment is to allocate reliability goals to lower level assemblies.

The apportionment is summarized in Table 14.

Historically, the reliability of solar cell configurations has been extremely high in comparison with the power conditioning equipment. The apportionment was therefore based on the amount of electronics used in each element. The complete high voltage solar array was considered to consists of three elements:

1. Solar cell building blocks with regulation switching
2. Configuration switching
3. Load switching.

The criteria used to allocate the allowable probability of failure is the estimated number of switches in each element as follows:

Element	Number of # Switches	Allocation
a) Building Blocks (16)	176	176/204 x 0.01 = 0.0086
b) Configuration Switching	16	16/204 x 0.01 = 0.0008
c) Load Switching	12	12/204 x 0.01 = 0.0006
	204	

A HVSA consisting of 16 building blocks was assumed to be a representative system configuration, and therefore the allocation for each building block is 0.0086/16 = 0.00054, and the reliability goal for each building block is R_{BB} = (1-.00054) = 0.99946.

The apportioned values given in Table 14 should be considered as initial goals and subject to modification if future work indicates that they are unrealistic. The apportionment, in general, should always be considered in the proper perspective, i.e. a means of allocating a higher level goal to lower level elements such that if the lower level goals are met, the higher level goal is also achieved.

8.2.4 SOLAR CELL RELIABILITY MODEL EVALUATION

8.2.4.1 Parameter Values

The selected values for the parameter used for numerical evaluation of the solar cell reliability models are as follows:

8.2.4.1.1 Solar Cell Reliability

The prevalent failure mode of solar cells is "open" connections. These open connections are assumed to be a function of the number of thermal cycles experienced. A typical failure rate is 3 failures per 10^8 thermal cycles per connection. The total number of thermal cycles is:

5 year mission x 90 eclipse periods per year = 450

Number of thermal cycles during orbit acquisition = 583

1033

The expected number of cell failures dueing the mission (Xct) is therefore: Xct = 1033 thermal cycles x 2 connection per cell x 3 x 10^{-8} Xct = 61.98 x 10^{-6} failures/mission $\approx$ 0.000062.

The reliability of a single solar cell (Rc) is therefore estimated as Rc = 1-Xct = 0.000038.

8.2.4.1.2 Diode Reliability

A typical diode short-circuit failure rate is 5 x 10^{-9} failures per hour. For the 5.25 year mission (includes synchronous orbit and ascent time), the expected number of failures (probability of a diode failing in the shorted mode) is: Pds = 5.25 yrs. x 8760 hrs/yr x 5 x 10^{-9} = 229.95 x 10^{-6} $\approx$ 0.0002

The ratio of short to open failures is in the range of 5:1 to 10:1, therefore:

Pdo = 0.00003

8.2.4.1.3 Failure Probabilities

Reliability estimates for the three solar cell configurations were computed by applying the solar cell and diode reliability values to the reliability models in Section 8.2.2. The baseline array size used for a single 1 Kv, 1 Kw building block is 12 strings of 3024 cells each, based on a 2 x 2 cm cell size.

In order to evaluate the effect of possible failure rate inaccuracies, the models were also evaluated with the diode and cell failure probabilities increased and decreased by a factor of 10.

The resulting failure probabilities used are as follows:

Probability Of Failure	Diodes Open	Diodes Short	Solar Cells
Low	0.000003	0.00002	0.0000062
Nominal	0.00003	0.0002	0.000062
High	0.0003	0.002	0.00062

8.2.4.2 Reliability Estimate for Configurations A&B

The resulting estimated reliability for configurations A&B are as follows:

			Cell Reliability		
			High	Nominal	Low
Diode Reliability	High	R_A	0.9765041	0.3216505	0.1877763
		R_B	0.9999909	0.9990941	0.9136942
	Nominal	R_A	0.9764416	0.3215746	0.1877163
		R_B	0.9999909	0.9990941	0.9136942
	Low	R_A	0.9758126	0.3208163	0.1871174
		R_B	0.9999909	0.9990941	0.9136942

It is noted that in every case, configuration B produces a higher reliabiliry value than configuration A, thus establishing the superiority of parallel interconnected strings of cells over series strings of cells without parallel connections.

8.2.4.3 Reliability Estimate for Configuration C

In order to provide a direct reliability comparison with configurations A and B for an equal number of extra solar cells, configuration C contains an equivalent number of extra cells. However, these cells are added as an additional "y" rows of "m" cells each, (y = 252, m = 12). Protection against open cells is provided by adding bypass diodes across each "x" rows. Further evaluation of configuration C with fewer extra cells will be discussed in Section 8.2.5.

The reliability number predictions for configuration C were computed for values of "x" from 1 to 252, for each combination of cell & diode failure rates. The resulting curves are shown in Figure 74. The curves indicate that for each combination of cell and diode failure rates, the reliability increases as the number of diodes increases up to an "optimum" value at the knee of the curve. The increase in reliability for a further increase in the number of diodes, beyond the knee of the curve, is insignificant. It is also noted, that at the knee of each curve, the reliability is higher than the reliability for configuration B, using the same combination of diode and cell failure rates. A summary of the predicted reliability for configurations A, B, and C, (using the knee point of each curve in Figure 74 for configuration C), is given in Table 15.

It is therefore concluded that:

1. Configuration C can be made more reliable than configurations A and B by adding a sufficient number of bypass diodes.

2. Adding more diodes than required to reach the knee of the curve in configuration C does not significantly improve reliability.

8.2.5 RELIABILITY OF CONFIGURATION C WITH FEWER THAN 252 ROWS OF CELLS ADDED FOR REDUNDANCY

The analysis contained in Section 8.2.4 provided for the addition of 252 rows of cells to the basic 1000 V building block for Configuration C. This number of rows was selected to provide an array area equivalent to that obtained when one cell per row is added to configurations A and B for redundancy.

The analysis was extended determine the effect on reliability of Configuration C, of adding fewer than 252 rows of cells. "Nominal" failure rates were used for both solar cells and diodes. Computations were made for the case of 1, 2, 3, 8, and 21 rows of cells per diode. For each case, the reliability values increase rapidly with an increase in the number of redundant cell rows (varied from 1 to 252) and then rapidly levels off. The reliability objective of 0.9998 is achieved in each case with the following number of redundant rows:

No. Rows per Diode	Number of Redundant Rows for 0.9999
1	12
2	24
3	36
8	96
21	252

In each of the above cases, 12 redundant groups (group = x rows of cells bridged by a bypass diode) are required to provide a reliability of 0.9998.

The preceding analysis was repeated using a very high diode reliability to reflect the use of a quad redundant configuration. Although resultant configuration reliability values were higher, the same number of redundant rows are required to provide a reliability value of 0.9998.

It is therefore concluded that the number of redundant rows of cells required to provide a reliability of 0.9998 for the 1000 V building block solar cell configuration C is 12 x the number of rows per diode.

Therefore, as few as 12 redundant series rows of 2 x 2 cm cells (out of a 3000 baseline requirement for a typical 1 Kv building block) can yield the apportioned solar cell reliability goal of 0.9998, based on the use of nominal cell and diode failure rates. This number of redundant rows (12) requires the use of a bypass diode function at each series solar cell row. The array area penalty required to achieve the reliability goal is only 0.4%. The use of fewer diodes will require extra cell rows to achieve the same reliability. For example, if a bypass diode were connected across 8 series cell rows, 96 redundant cell rows are required, resulting in a reliability penalty of about 3% of the total array area. Other considerations, such as the effect on regulation of cell failures, will influence the selection of the number of cell rows per bypass diode.

The apportioned reliability number of 0.9998 expresses the probability that no more than the 12 rows out of the (3024 + 12) total rows will fail. However, as some rows fail, it becomes necessary for other rows to overcome the voltage drop introduced by the bypass diode across the failed row. Thus, to ensure the 0.9998 probability of having 3024 solar cells output voltage, sufficient extra cells to overcome the drop across 12 bypass diodes are needed. This criterion results in an additional 24 series cells (2 solar cells = 1 diode drop), or a total of 36 additional series rows beyond the baseline 3024.

8.2.6 EFFECT OF VARIATION IN CELL SIZE ON RELIABILITY

This analysis was performed to determine the effect of varying the cell size on reliability of the 1000 V building block solar cell configuration C. Reliability estimates were computed for cell sizes of 2 x 4 cm, 2 x 6 cm, and 2 x 8 cm, to determine the minimum number of extra rows required to provide a reliability of at least 0.9998 for each cell size.

For these computations, "nominal" cell and diode failure rates were used. Because cell failure rate is dependent only on the number of connections, the larger cells were assigned the same failure rate as the 2 x 2 cm cells.

The results are shown in Table 16 from which it can be concluded that the 0.9998 reliability objective can be met with fewer redundant rows of cells as the cell size increases.

It is also expected that the appreciable cell cost savings and fewer solar array fabrication operations associated with the larger area cells will dictate their use on the HVSA. Considerations such as low power dissipation in the shunt regulators may show the use of 2 x 2 cm cells to be advantageous in a small portion of the array. Requirements for low-current auxiliary array functions may also minimize array area penalties with the use of smaller cells.

8.2.7 EFFECT OF BUILDING BLOCK VOLTAGE ON SOLAR CELL RELIABILITY

The 1-Kv building block size has been used throughout the reliability analysis as being a typical design voltage. Since actual design may encompass a wide range of voltages, the effect on solar cell reliability was determined.

The 1-Kv building block reliability model assumed a baseline series cell requirement of 3024 cells. With this number changed to 6048 series cells (approximating a 2 Kv building block) and 1512 series cells (approximating a 500 V building block) the following configuration C reliability numbers were obtained with nominal failure rates:

Series Cells	Redundant Cells	Reliability No.
3024	12	0.999922
1512	8	0.999947
1512	12	0.999966
6048	12	0.993819
6048	20	0.999864

As expected, the reliability number increased for fewer cells in series, and decreased with more cells in series. It is seen that some small savings in redundant cells can be realized at lower building block voltages, and some additional redundant cells are required at the very high building block voltage to approach the reliability goal.

8.3 BUILDING BLOCK RELIABILITY MODEL

8.3.1 GENERAL

The functional arrangement of the typical 11-bit voltage-regulated building block presented in Section 6 is the basis of the building block reliability model. Figure 75 presents the reliability model for a typical HVSA building block. The two criteria employed in the development of this model are:

1. Each functional circuit within the building block becomes a series-connected reliability component (affecting a worst-case model), and

2. Each functional circuit is characterized by the failure rates of its identifiable parts, obtained from the electrical schematics, Section 5.

Because of the quad redundancy technique employed with the regulation shorting switches, drivers, high-voltage signal couplers and fail-safe logic, these parts are combined into the reliability component labeled "Regulation Switching". The relation of the remaining reliability components in Figure 75 to the equivalent electrical function described in Section 5 is readily apparent.

8.3.2 RELIABILITY COMPONENT EXPRESSIONS

8.3.2.1 Regulation Switching (with Drivers, Signal Coupling and Fail-Safe Logic)

Quad Regulation Switch Reliability = RRS

$$RRS = 1 - (2\,Po^2 - Po^4 + 4Ps^2 - 4Ps^3 + Ps^4)$$

where

$$Po = \left\{1 - \exp\left[(-\lambda o - \lambda s)\,t\right]\right\} \frac{\lambda o}{\lambda o + \lambda s}$$

$$Ps = \left\{1 - \exp\left[(-\lambda o - \lambda s)\,t\right]\right\} \frac{\lambda s}{\lambda o + \lambda s}$$

λo = failure rate for open failure mode.

λs = failure rate for short failure mode.

t = mission time

8.3.2.2 Counter

Counter Reliability = RCN

$$RCN = \exp\left[(-\lambda\,CN)\,t\right]$$

where

λCN = counter failure rate

t = mission time.

8.3.2.3 Stacking Switch (with Drivers and Signal Couplers)

Quad Stacking Switch Reliability = RSS

$$RSS = 1 - (2Pos^2 - Pos^4 + 4Pss^2 - 4Pss^3 + Pss^4)$$

where:

Pos = Probability of single switch section failing open.

Pss = Probability of single switch section failing short.

$$Pos = \left\{1 - \exp\left[(-\lambda os - \lambda ss)\,t\right]\right\} \frac{\lambda os}{\lambda os + \lambda ss}$$

$$Pss = \left\{1 - \exp\left[(-\lambda os - \lambda ss)\,t\right]\right\} \frac{\lambda ss}{\lambda os + \lambda ss}$$

λos = failure rate for open failure mode

λss = failure rate for short failure mode

t = mission time.

8.3.2.4 Array Shorting Switch (With Drivers and Signal Coupler)

Quad Array Short Switch Reliability = RAS

This switch is identical in parts and function to the stacking switch, and hence is modelled the same way:

RAS = RSS

8.3.2.5 Blocking Diodes

Quad Blocking Diode Reliability = RBD

$$RBD = 1 - (2 P_{OBD}^{2} - P_{OBD}^{4} + 4 P_{SBD}^{2} - 4 P_{SBD}^{3} + P_{SBD}^{4})$$

where

P_{OBD} = probability of single diode failing open

P_{SBD} = probability of single diode failing short

$$P_{OBD} = \left\{1-\exp\left[(-\lambda_{OBD} - \lambda_{SBD})\, t\right]\right\} \frac{\lambda_{OBD}}{\lambda_{OBD} + \lambda_{SBD}}$$

$$P_{SBD} = \left\{1-\exp\left[(-\lambda_{SBD} - \lambda_{OBD})\, t\right]\right\} \frac{\lambda_{SBD}}{\lambda_{OBD} + \lambda_{SBD}}$$

λ_{OBD} = failure rate for diode open

λ_{SBD} = failure rate for diode short

t = mission time

8.3.2.6 Coupling Diodes

Quad Coupling Diode Reliability = RCD

$$RCD = 1 - (2 P_{SCD}^{2} - P_{SCD}^{4} + 4 P_{OCD}^{2} - 4 P_{OCD}^{3} + P_{OCD}^{4})$$

The definition of terms is analogous to that for blocking diodes in Paragraph 8.3.2.5.

8.3.2.7 Solar Cells and Bypass Diodes

Solar Cell Reliability = RCS

Section 8.2 detailed the reliability analysis for the solar cell/bypass diode Configuration "C". The value of solar cell/bypass diode reliability to be used in the evaluation of building block reliability is

RCS = 0.9998

8.3.3 MATHEMATICAL BUILDING BLOCK RELIABILITY MODEL

The components comprising the HVSA building block reliability model on Figure 75 are:

11	Regulation Switches	(Quad)
1	Counter	
1	Stacking Switch	(Quad)
1	Array Shorting Switch	(Quad)
1	Blocking Diode	(Quad)
2	Coupling Diode	(Quad)
1	Solar Cell/B ypass Diode Configuration	

The building block reliability, RBB, is defined as:

$$RBB = RRS^{11} \times RCN \times RSS \times RAS \times RBD \times RCD^{2} \times RSC.$$

8.3.4 FAILURE RATE ESTIMATES

8.3.4.1 Discussion

Failure rate estimates for the various reliability components, described in Section 8.2.2, to be used in determining the building block reliability, are presented herein. Small auxiliary solar arrays are required to power much of the circuitry, but these have a very low failure rate relative to other circuit components, and can easily be made redundant so that their failure rate has been specified as insignificant. The failure rate for integrated circuits is the weighted (by test hours) average of the values presented in Table 17. It is expected that most of the electronic functions on the HVSA will be fabricated using combinations of integrated circuits and discrete components.

The reliability analysis considers each electronic piece part, its function in the circuit, the usual piece part failure modes that could prevent the part from performing its function in the circuit, and the probability that the total circuit will fail based on this detailed analysis of each part. The failure rates for the resistors, transistors, and diodes have been reduced by a factor of ten from those usually considered for conventional piece parts. The rationale for this is that the final configuration will, in all probability, utilize many integrated circuits to accomplish the electronic functions. These integrated circuits are assigned a higher inherent reliability than what would be indicated by the number of parts required to reproduce the circuit function with individual discrete parts.

The higher reliability of the integrated circuit is due to the following:

1. There is a higher degree of uniformity and standardization associated with circuit elements in an integrated circuit, since only the elemental function in its simplest form is utilized in the circuit.

2. These part functions are deposited directly on the interconnecting substrate or metalurgically bonded to it directly, without the multiple interconnections associated with the mechanical package of the discrete piece part.

3. The dissimilar metal possibility with a variety of termination methods and the hazards of oxidation, contamination, and electrolysis are removed with the elimination of these superfluous interconnections.

4. The fabrication process is usually automated and contnuous, and not subject to human operator error to the same extent as discrete circuitry fabrication by either welding or soldering.

5. The process is more tightly controlled, and inspection is one hundred percent under magnification by comparator techniques to assure the uniformity inherent in the process.

6. The process is typically high volume, or high volume usage of individual circuit functions created under the same conditions, and this larger sample gives a higher assurance of detecting a flaw or malfunction.

7. The number of circuit connections that pass through the integrated circuit interface is minimized, reducing the possibility of electrical interaction with other circuit elements.

8. The integrated circuit performs a complete electrical function, and is fully tested with all its piece parts in place, sealed in a controlled environment, with established physical interrelationships.

9. The single substrate and the high thermal conductivity assure a common operating temperature, and reduce the possibility of differential thermal expansion, or parameter drift due to the temperature differences between piece parts.

10. The piece parts within the integrated circuit are protected from oxidation, contamination, and mechanical abuse by the substrate enclosure.

The failure rates used for the reliability analysis are summarized below:

Circuit or Device	Failure Rate (λ)
Resistor	0.001×10^{-6} failures/hr
Transistor	0.008×10^{-6} failures/hr
Diode	0.005×10^{-6} failures/hr
Integrated Ckt	0.025×10^{-6} failures/hr

8.3.4.2 Reliability Component Failure Rate

The failure rate determination for each reliability component defined in Figure 75 is presented in the following paragraphs.

8.3.4.2.1 Regulation Switching (with Drivers, Signal Couplers and Fail-Safe Logic)

The failure rate for each section of the quad regulation switching component is determined by summing the weighted part failure rates:

13 Resistors	x	0.001×10^{-6}	=	0.013×10^{-6}
1 Integrated Ckt	x	0.025×10^{-6}	=	0.025×10^{-6}
7 Transistors	x	0.008×10^{-6}	=	0.056×10^{-6}
5 Diodes	x	0.005×10^{-6}	=	0.025×10^{-6}
		λRS	=	0.119×10^{-6} failures/hr

Assuming the regulation switching is equally likely to fail short or open, then

$\lambda o = \lambda s = 0.0595 \times 10^{-6}$ failures/hr.

8.3.4.2.2 Counter

7 Intergrated Ckts x $0.025 \times 10^{-6} = 0.175 \times 10^{-6}$

$\lambda CN = 0.175 \times 10^{-6}$ failures/hr.

8.3.4.2.3 Stacking Switch (With Drivers and Signal Couplers)

6 Transistors	x	0.008×10^{-6}	=	0.048×10^{-6}
6 Resistors	x	0.001×10^{-6}	=	0.006×10^{-6}
2 Diodes	x	0.005×10^{-6}	=	0.010×10^{-6}
		$\lambda stsw$		0.064×10^{-6}

Assuming short or open failure equally likely,

$$\lambda ss = \lambda so = 0.032 \times 10^{-6} \text{ failures/hr.}$$

8.3.4.2.4 Array Shorting Switch (With Drivers and Signal Couplers)
This switch is identical to the stacking switch, so the failure rates are the same as in 8.3.4.2.3.

8.3.4.2.5 Blocking Diodes
The diode failure rate when used in a hybrid circuit is estimated to be 0.005×10^{-6} failures per hour. It is also estimated that diodes short about none times out of ten failures.

Therefore:

$$\lambda_{SBD} = 0.0045 \times 10^{-6} \text{ failures/hr.}$$

$$\lambda_{OBD} = 0.0005 \times 10^{-6} \text{ failures/hr.}$$

8.3.4.2.6 Coupling Diodes
The failure rates for the coupling diodes are the same as for the blocking diodes:

$$\lambda_{SCD} = 0.0045 \times 10^{-6} \text{ failures/hr}$$

$$\lambda_{OCD} = 0.0005 \times 10^{-6} \text{ failures/hr}$$

8.3.4.2.7 Solar Cells and Bypass Diodes
The failure rates for the solar cells and blocking diodes have been discussed in Section 8.1. The resulting value of calculated reliability for nominal failure rates will used in the evaluation of building block reliability:

$$R_{SC} = 0.9998$$

8.3.5 EVALUATION OF BUILDING BLOCK RELIABILITY
A numerical determination of building block reliability has been made, using the failure rates estimates presented in Section 8.3.4.2 and the reliability expression for an 11-switch building block:

$$RBB = RRS^{11} \times RCN \times RSS \times RAS \times RBD \times RCD^{2} \times RSC.$$

The following tabulates the total building block (RBB) and functional circuit reliability numbers.

RBB	(total building block)	0.991924
RRS^{11}	(11 regulation switches)	0.999679
RCN	(Binary counter)	0.992364
RSS	(Stacking switch)	0.999989
RAS	(array shorting switch)	0.999989
RBD	(blocking diode quad)	0.999999
RCD^2	(2 coupling diode quads)	0.999999
RSC	(solar cell/bypass diodes)	0.999800

8.4 LOAD SWITCH RELIABILITY MODEL

The circuit diagram for the load switch (8A and 1A) appears in Section 5.1. The reliability expression for the load switch which consists of a dual transistor turnoff switch plus a quad SCR high voltage switch is

Load Switch Reliability = RLS

$$RLS = (1-P_{to}^{2})\left(1-\left[2P_{so}^{2}-P_{so}^{4}+4P_{ss}^{2}-4P_{ss}^{3}+P_{ss}^{4}\right]\right)$$

P_{to} = probability of a single transistor turnoff switch failing open.

P_{so} = probability of a single SCR switch section failing open.

P_{ss} = probability of a single SCR switch section failing short.

$$P_{to} = \left[1-e^{-(\lambda_{to}+\lambda_{ts})\,t}\right] \quad \frac{\lambda_{to}}{\lambda_{to}+\lambda_{ts}}$$

where

t = mission time

λ_{to} = failure rate for transistor circuit open

λ_{ts} = failure rate for transistor circuit short

$$P_{so} = \left[1-e^{-(\lambda so+\lambda ss)\,t}\right] \quad \frac{\lambda so}{\lambda so+\lambda ss}$$

$$P_{ss} = \left[1-e^{-(\lambda so+\lambda ss)\,t}\right] \quad \frac{\lambda ss}{\lambda so+\lambda ss}$$

λso = failure rate for high voltage switch open

λss = failure rate for high voltage switch short

Since a backup method of turning the high voltage switches off exists by total shorting of the solar array, only failures of the transistor switches which open the power path irrevocably cause a power switch failure.

Failure rate estimates for the transistor turnoff switch elements and the quad SCR load switch elements are presented in Tables 18 and 19. Component failure rates are those presented in Section 8.2.4.2. Since no data exists for the high voltage SCR failure rate, a value was assigned which is worse than a transistor failure rate by a factor of 10.

A numerical determination of load switch reliability (RLS) has been made, using the mathematical model and the failure rates presented in this section. The results are:

RLS = 0.999936 (1 Amp Switch)

RLS = 0.999738 (8 Amp Switch)

8.5 SYSTEM RELIABILITY MODEL AND ESTIMATE

The reliability model for a HVSA system configuration consisting of building blocks, load switches and array grounding switch is presented in the following equation.

$$RSYS = \left[\prod_{i=1}^{NBB} RBB_i\right] \left[\prod_{j=1}^{NLS} RLS_j\right] \left[\prod_{k=1}^{NGS} RGS_k\right]$$

where

RSYS = system reliability

RBB = building block reliability

RLS = load switch reliability

RGS = load return/array ground switch reliability

NBB = number of building blocks in system

NLS = number of load switches in system

NGS = number of array ground switches in system

The system reliability model accommodates the effect of some building blocks having stacking switches and coupling diodes while others do not, and the effect of a high and/or low current load switches, which have somewhat different reliability numbers. The array grounding switch, discussed in Section 5.1, has the same reliability expression as the load switch, with the effect of a slightly different circuit arrangement being accounted for in the determination of a quad element failure rate.

Evaluation of the system reliability model for the two optimized systems, presented in Section 7, produces the following numbers:

System No. 1: RSYS = 0.81574

System No. 2: RSYS = 0.87696

The higher reliability for System No. 2 is due to its requiring only 16 building blocks compared to System No. 1 which is comprised of 25 building blocks.

8.6 SUMMARY

Reliability analyses of candidate solar cell arrangements shows that the configuration which yields the apportioned reliability goal over the greatest range of solar cell and protective diode failure rates employes bypass diodes in parallel with small numbers of series-connected cell rows, where each cell row is the total number of parallel solar cells needed in the array and electrically connected in parallel. Redundancy with this scheme is provided by 36 additional series-connected cell rows in the array for each building block. In addition to providing the highest reliability, the bypass diode arrangement also minimizes the power loss effect of transient shadowing of the solar array, if such were encountered during the mission. The bypass diodes could be fabricated as microelectronic elements on substrates similar to those being considered for other electronic functions to be mounted on the solar array.

Reliability of a 1 Kv, 11-bit building block is estimated to be 0.9919, compared to an apportioned goal of 0.9994. The limiting reliability component is the binary counter which has 0.992 reliability compared to the remaining functions which are each above 0.9996. Obviously, the reason for this situation is that binary counter redundancy has not been implemented. Further study is needed to identify the best approach to providing counter redundancy.

System reliability has been calculated for the two optimized systems described for this study. Although the study goal of 0.99 was not attained (System No. 1 reliability is 0.81 and System No. 2 is 0.87) these preliminary values do provide confidence that the recommended HVSA systems concept can be implemented with high reliability.

Table 14. Reliability Apportionment

Reliability Goal = 0.99 for 5 Yr. Mission

Allowable Probability of Failure = 0.01

		Probability Of Failure	Apportioned Reliability
1.	Load Switching	0.0006	0.9994
2.	Configuration Switching:	0.0008	0.9992
3.	Building Blocks (16):	0.0086	0.9914
	Single Building Block:	0.00054	0.99946
	a. Regulation Switching:	0.00036	0.99964
	b. Cell and Diode Array:	0.00018	0.99982

Table 15. Effect of Variation in Solar Cell and Diode Reliability

			CELL RELIABILITY		
			HIGH	NOMINAL	LOW
DIODE RELIABILITY	HIGH	R_A	.9765041	.3216505	.1877763
		R_B	.9999909	.9990941	.9136942
		R_C	.9999992	.9999915	.9999276
	NOMINAL	R_A	.9764416	.3215746	.1877163
		R_B	.9999909	.9990941	.9136942
		R_C	.9999926	.9999260	.9990837
	LOW	R_A	.9758126	.3208163	.1871174
		R_B	.9999909	.9990941	.9136942
		R_C	.9999268	.9992704	.9924335

Table 16. Cell Size Effect on Reliability

CELL SIZE	NO. ROWS PER DIODE	MINIMUM NO. OF REDUNDANT ROWS FOR .9999 RELIABILITY
2 x 2 cm	1	12
	12	144
	21	252
2 x 4 cm	1	9
	12	96
	21	168
2 x 6 cm	1	8
	12	72
	21	126
2 x 8 cm	1	8
	12	72
	21	126

Table 17. Microelectronics Failure Rate Data

SOURCE NAME	DATA SOURCE	MICROCIRCUIT TYPE	OPERATION TIME (UNIT-HOURS)	FAILURE RATE x 10^6
1. Motorola	Ring Counter Life Tests	Epitaxial	18 x 10^6	0.0385*
2. Signetics	"	"	59 x 10^6	.0117*
3. NASA Data	225 Space-craft	Misc.	6.3 x 10^6	.1150*
4. Hughes	Estimate	Misc.	-	.0250
5. Autonetics	Minuteman 2 History	Unknown	-	.0080
				*50% confidence

Table 18. Failure Rates for Transistor Turnoff Section of Load Switch

Component Name	Failure Rate	Number and λ of Components: 1 Amp	λ_o	λ_s	8 Amp	λ_o	λ_s
High Voltage Transistor	.016	1	.008	.008	1	.008	.003
Transistor	.008	2	.008	.008	4	.016	.016
Resistor	.001	6	.003	.003	8	.004	.004
Photo Transistor	.008	1	.004	.004	1	.004	.004
Diode	.005	1	.0025	.0025	1	.0025	.0025
LED	.005	1		.005	1		.005
Solar Cells	.00142	17	.024		134	.190	

Note: all numbers have units of 10^{-6} failures/hr

Totals $\lambda_{to} = .0495$, $\lambda_{ts} = .0305$ $\lambda_{to} = .2245$, $\lambda_{ts} = .0395$

Table 19. Failure Rates for Quad SCR Elements of Load Switch

Component Name	Failure Rate	Number and λ of components: 1 Amp	λ_o	λ_s	8 Amp	λ_o	λ_s
High Voltage SCR	.08	1	.04	.04	1	.04	.04
Transistor	.008	4	.016	.016	5	.02	.02
Resistor	.001	8	.004	.004	9	.0045	.0045
Photo Transistor	.008	1	.004	.004	1	.004	.004
Diode	.005						
LED	.005	1	.005		1	.005	
Solar Cells	.00142	10	.0142	0	78	.111	0

Note: all numbers have units of 10^{-6} failures/hr

Totals $\lambda_{SO} = .0832$, $\lambda_{SS} = .064$ $\lambda_{SO} = .1845$, $\lambda_{SS} = .0685$

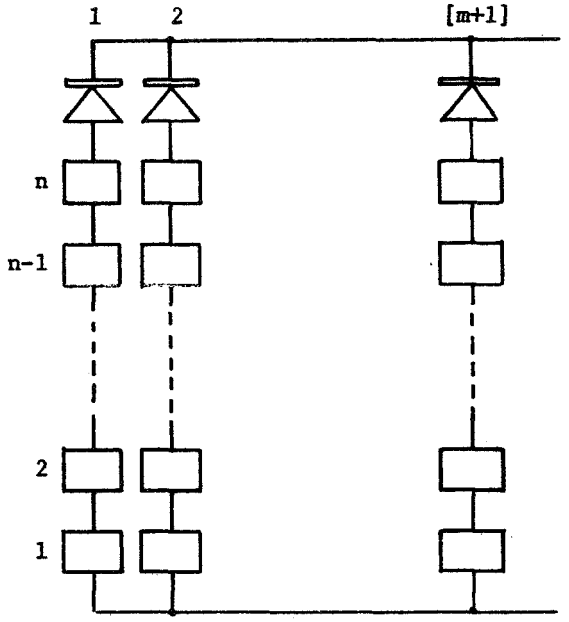


Figure 73A. Configuration A - Reliability Model

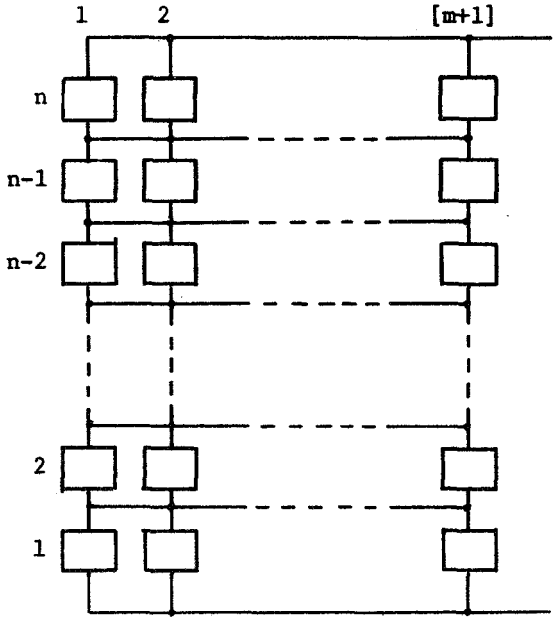


Figure 73B. Configuration B - Reliability Model

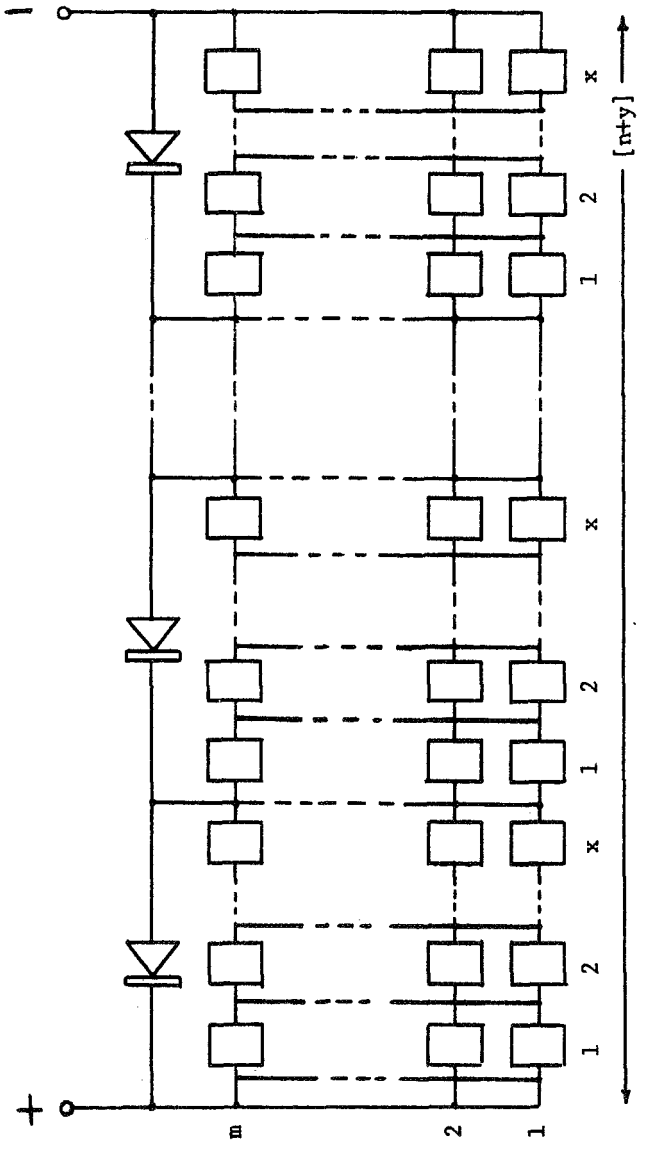


Figure 73C. Configuration C - Reliability Model

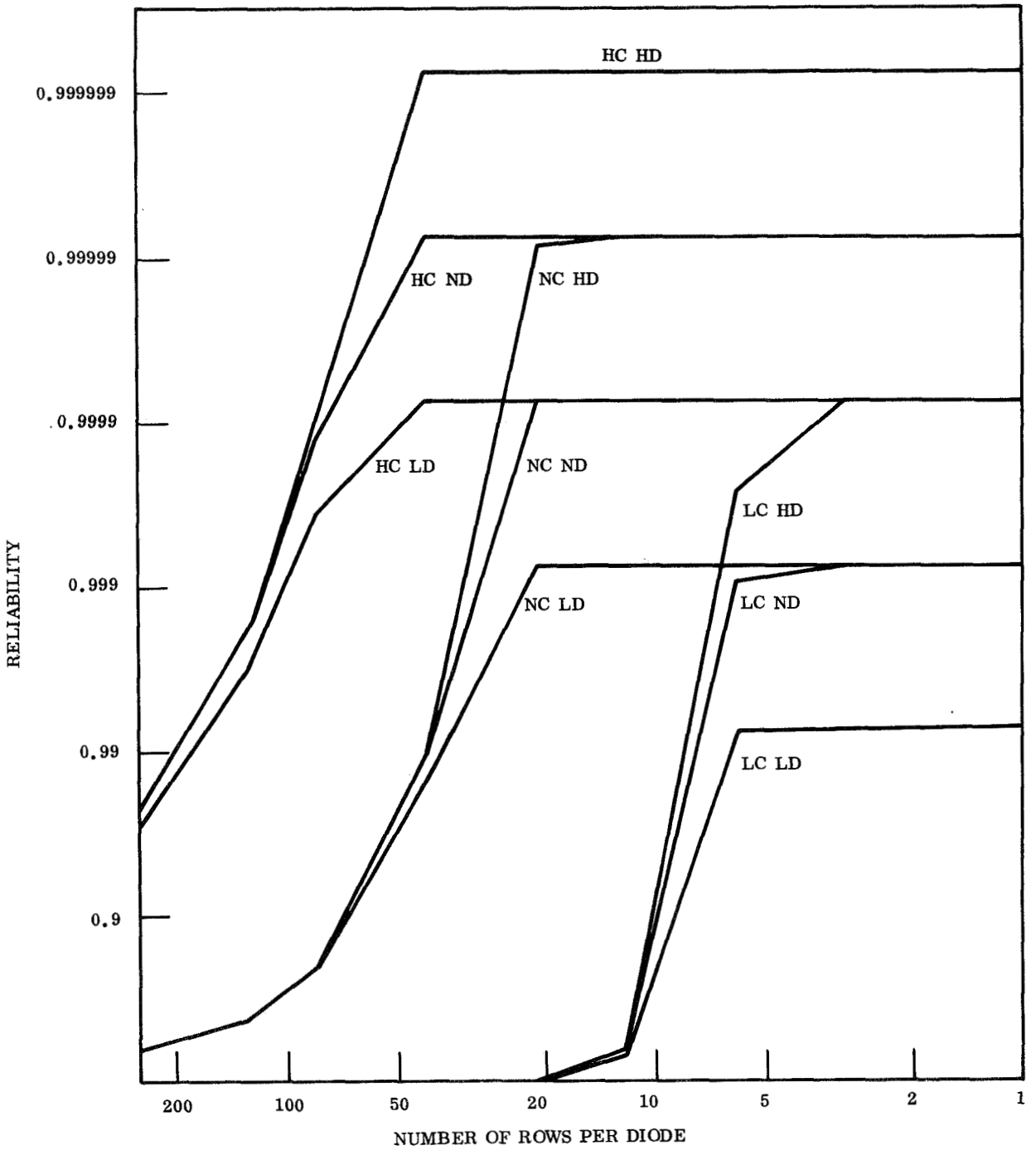


Figure 74. Reliability of Solar Cell Arrangement with Bypass Diodes

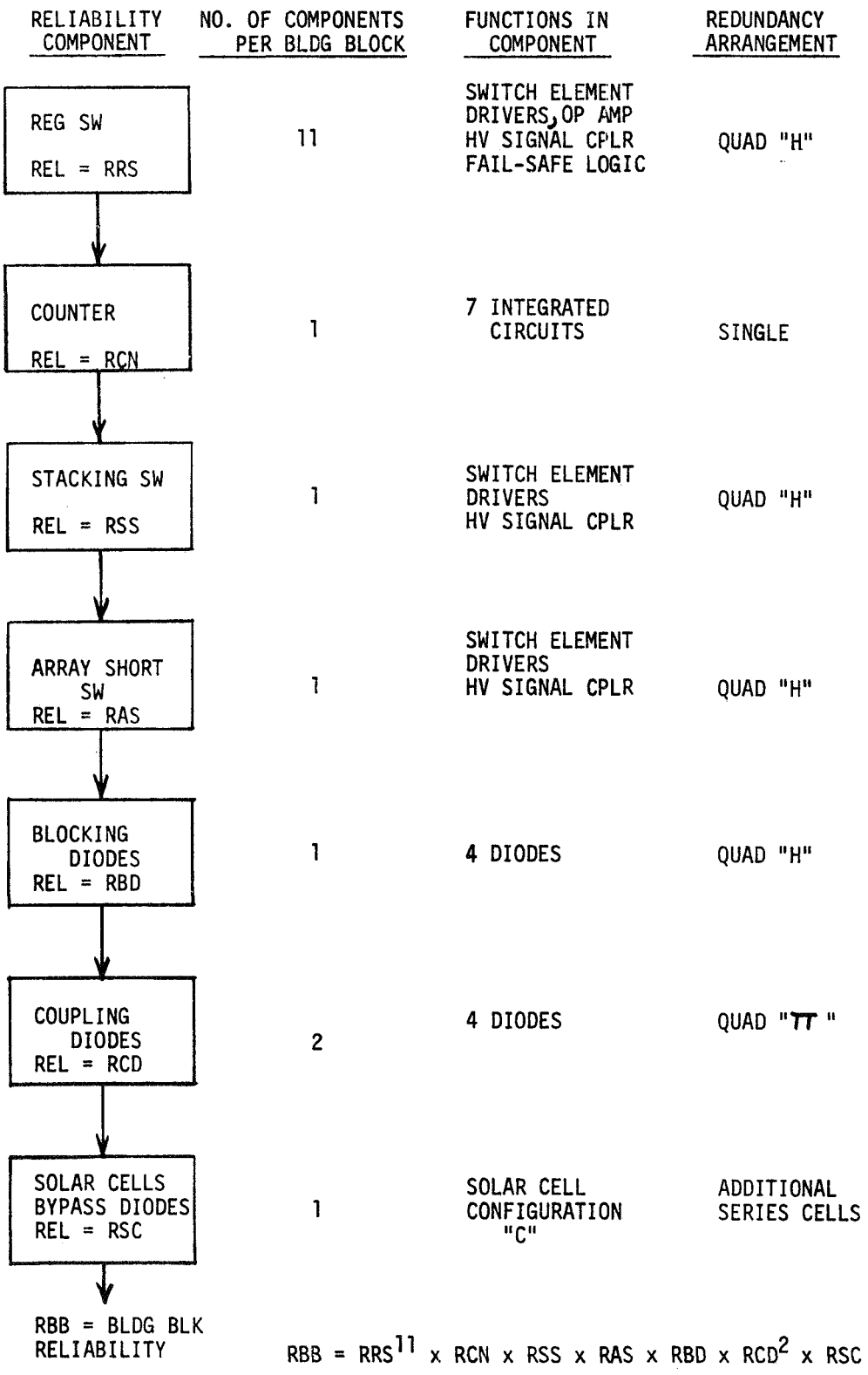


Figure 75. Reliability Model for HVSA Building Block

SECTION 9

RELATED ANALYSES AND CONSIDERATIONS

This section presents the various efforts performed to (1) support the technical analyses described in preceding sections and (2) provide additional insight into aspects of the HVSA not previously discussed.

9.1 RADIATION ENVIRONMENT AND EFFECTS PREDICTIONS

9.1.1 GENERAL

This section defines the charged particle radiation environment between 100 nautical miles (185 Km) and synchronous altitude, describes the radiation effects upon semiconductors, provides estimates of shielding thickness to limit performance degradation, and discusses several techniques to minimize radiation effects. Shielding estimates made herein have been used to calculate circuit package weight reported in Section 9.3.

9.1.2 HIGH VOLTAGE SOLAR ARRAY MISSION

The high voltage solar array is to operate for 5 years in an equatorial 24 hour synchronous orbit which is achieved by a spiraling transfer orbit from a 100 nm (185 Km) parking orbit to the 19,300 nm (35,800 Km) synchronous orbit over a period of 90 days. The equation for the orbit transfer period is

$$A = \frac{185 + Re}{(1-0.00674t)^2} - Re$$

A - Vehicle Altitude (Km)

Re - Earth Radius (6360 Km)

t - Elapsed time during transfer phase (days)

and is plotted in Figure 76. The orbit is assumed to be in the earth equatorial plane during the entire transfer phase.

9.1.2.1 Implication of the Mission on the Radiation Environment

The radiation particles of principal interest to this study are the geomagnetically trapped electrons and protons which surround the earth to synchronous altitude and beyond, and the protons which are associated with solar flares.

The radiation environment to be experienced by the solar array is composed of the relatively constant proton and electron flux of the 5 year orbit phase at synchronous altitude, the altitude dependent proton and electron flux of the 90 day period during the transfer from the parking orbit to the synchronous orbit, and the probalistic proton flux exposure of the entire mission due to solar flares.

9.1.3 RESULTS OF THE RADIATION ENVIRONMENT DETERMINATION

The integral energy spectra for protons and electrons for the orbit phase are presented in Figure 77. The proton data is derived from "ATS Power Subsystem Radiation Effects from Study Phase 1/Final Report" by Hughes Aircraft Company (Contract NAS 5-3823) which is extrapolated from the 18,000 nm (33,300 Km) data of the orbital integration map AP5 of Volume IV (Low Energy Protons) of NASA SP-3024 (Models of the Trapped Radiation Environment). The orbit phase electron environment is derived from Table 4 of Volume III (Electrons at Synchronous Altitudes) of NASA SP-3024. The proton data is for a zero degree magnetically inclined orbit while the electron data is for a theoretical dipole representation of the earth's magnetic field (B/Bo = 1).

The integral energy spectra for the solar flare protons for the mission is presented in Figure 78. This data is based on information obtained from a draft copy of "Voyager Environmental Predictions Document" issued by the Jet Propulsion Laboratory as Document SE 003 BB 001-1B28 (1966) and on the environment created by solar cycle 19 and includes the total of the peak 5 years corresponding to 1957 through 1961. This data was compared with the data of the "Solar Proton Manual" issued by NASA as NASA TR-R-169 (1963) and found to be in reasonable agreement.

Determination of the proton and electron environment for the transfer phase involved plotting the integral orbital flux per day as a function of particule energy and altitude and then using the orbit altitude information of Figure 76 to determine the daily integral flux for several particle energies over each day of the transfer phase. Summation of the daily integral fluxes gave the total flux for the various particle energies. The data so derived for the proton and electron environments is illustrated in Figure 79. The data base for the proton environment is taken from AP1 and AP3 as discussed in Vol. 1 (Inner Zone Protons and Electrons), AP5 of Vol. IV (Low Energy Protons), and AP6 of Vol. V (Inner Belt Protons) of NASA SP-3024. Both the proton and electron data corresponds to zero degree magnetically inclined orbits although the magnetic equator is inclined approximately 11 degrees to the earth's equatorial plane.

Two principal interactions are of concern when these high energy radiations interact with materials: ionization and atomic displacement effects. Both effects are critical to semiconductor operation. It is necessary to use the environments defined to determine the resulting ionization and atomic displacement doses which accumulate over the 5-year mission. It is also of interest to determine these doses as a function of shielding.

Since the principal concern for this mission are the effects on semiconductor devices, atomic displacement effects are referenced to effects occurring in silicon semiconductors such as transistors. A great amount of experimental data exists for atomic displacement effects in semiconductors utilizing neutrons rather than charged particles such as protons and electrons. It has become somewhat standard to express the total atomic displacement dose in terms of an equivalent dose of 1 MeV neutrons defined such that it creates an amount of atomic displacement damage equivalent to the actual environment specified.

Since evaluation of the effects of the transfer orbit phase on the array indicates that this trajectory results in very high radiation doses, only the 5-year orbit phase at synchronous altitude will be considered for further shielding analysis.

Figure 80 shows the total accumulated equivalent 1 MeV neutron dose for the trapped electron dose for the 5-year synchronous orbit as a function of shield thickness. The shielding analysis is carried out utilizing standard electron range-energy relationships. Two shielding materials are considered, BeO, since it represents a typical material for semiconductor substrates and tantalum since it is a typical high density shielding material. Use of high density shield material is desired since more shielding can be placed in a given volume compared to using a low density material. This will be important in shielding tradeoff studies. Figure 80 shows the accumulated equivalent 1 MeV neutron dose for the 5-year solar flare environment. Figure 80 presents the total 5-year accumulated equivalent 1 MeV neutron dose for the total synchronous environment. Trapped protons have very low energy at this altitude, and do not contribute significantly to the atomic displacement damage if a few mils of shielding are provided.

Figure 81 shows the corresponding 5-year ionization dose for the electron environment, in terms of RADS (silicon), as a function of shielding. Similarly, Figure 81 shows the ionization dose of the 5-year solar flare environment. The trapped electron environment represents essentially the total ionization dose for the five year mission, at least for reasonable shield thicknesses. Trapped protons do not contribute significantly to this dose since they are readily shielded.

The magnitude of the environment described is such that the principal effects occur in semiconductor devices. These discussions will concentrate on semiconductor devices and design approaches to overcome these effects.

9.1.4 RADIATION EFFECTS ON SEMICONDUCTOR ELECTRONICS

The main radiation effects on semiconductor electronics, particularly transistors, are the displacement damage effects or bulk damage, and the so-called radiation-induced surface effects. The bulk damage effect is the disruption of the crystal lattice of the semiconductor material. In transistors, this causes a decrease in carrier lifetime in the base region of the device. This effect takes place whether or not the device is electrically active. The surface-effects phenomenon, however, is more predominant when a device is under simultaneous electrical stress and exposed to ionizing radiation. This is due mainly to the interaction of the ionized gas (in the hermetically sealed transistor) and ionized surface impurities with the semiconductor surface.

Both effects (bulk and surface) can affect the transistor gain significantly. In addition, the surface effects can also alter junction leakage currents considerably. The extent to which device parameters are altered for a given radiation dose can depend to a large degree on device construction and initial electrical characteristics.

Each of these effects and how they relate to the present system are briefly described below.

9.1.4.1 Ionization Effects

The absorbed ionizing dose is of concern because of the surface effects damage mechanism in semiconductor devices. Ionizing radiation creates electron-ion pairs in the encapsulant gas and passivated surface of semiconductor devices. The mobile charge carriers - electrons and ions in the gas and electrons in the passivation layer - are redistributed by local electric fields. Redistribution of charge states results in the formation of fast intersurface states (recombination centers) and a positive charge build-up in the passivation layer. These phenomena significantly affect junction leakage current, minority carrier transistor gain and majority carrier transistor threshold voltages. Because of the surface nature of the damage mechanisms, the magnitude of change in device characteristics is strongly influenced by surface and/or passivation layer contaminants. Since local electric fields play an important role, surface effects damage is most significant for powered devices.

Figure 82 shows surface effects induced gain degradation for a typical minority carrier device. Gain degradation becomes progressively more severe as the collector current is reduced. This characteristic is typical of surface effects induced transistor gain degradation. The 2N708 device is a passivated surface structure. Gain degradation much more severe than that indicated by Figure 82 has been observed for unpassivated surface devices. Evacuation of the packaging gas will reduce the effect, although it will not eliminate it entirely. Figure 83 shows the effect of evacuation on a 2N708 passivated device.

Figure 84 shows surface effects leakage current which is typical of an integrated circuit isolation junction. Passivated surface discrete devices generally exhibit similar characteristics. The change in slope at about 10^5 rads is attributed to saturation of the radiation induced fast intersurface states.

Figure 85 shows a range of MOS FET threshold voltages as a function of radiation dose under worst case bias conditions. The wide variation in surface effects sensitivity is due to the effects of isolation layer material type and thickness, and contaminants.

9.1.4.2 Displacement Effects

The permanent damage effect of the electron and proton environments is normally expressed in terms of an equivalent 1 MeV neutron fluence. This damage unit provides a measure of the number of crystal lattice defects produced in semiconductor structures. These defects act as carrier recombination centers which cause a decrease in minority carrier lifetime.

One of the primary manifestations of decreased minority carrier lifetime is transistor gain degradation which has been estimated from the empirically derived equation:

$$B(\phi) = \frac{Bo}{1 + K\phi \frac{B_o}{2\pi f_t}}$$

where $B(\phi)$ is the degraded current gain

Bo is the initial current gain

ϕ is the equivalent 1 MeV neutron fluence

K is a material dependent damage constant

f_t is the transistor intrinsic gain-bandwidth product

Figure 86 is a plot of the gain degradation for typical values of gain-bandwidth and initial gain. The empirically based data does not give worst-case results and either an appreciable design margin must be provided or radiation test data must be acquired.

9.1.5 DESIGN CONSIDERATIONS

9.1.5.1 Ionization Effects

Based upon the anticipated 5-year synchronous altitude environment and consideration of the typical types of candidate semiconductor piece parts, it appears that shielding is necessary to minimize possibly severe radiation induced surface effects. Low power linear and digital integrated circuits are relatively sensitive since they will be utilized in a very low current circuit configuration. The magnitude of radiation induced surface effects in very high voltage transistors and SCRs must be determined for the specific devices developed. In general, the higher the junction voltage, the more severe the effects, particularly on gain and junction leakage current, although this will be very dependent upon semiconductor surface contaminants and control of the surface fields.

Based upon available data, it appears that a reasonable threshold ionizing radiation dose for surface effects is about 10^4 RADS and requires radiation shielding equivalent to about 40 mils (1.0 mm) of tantalum, according to Figure 81. This threshold could probably be increased with a corresponding decrease in the shielding requirement, if very careful device selection procedures are utilized along with design techniques that could make the resultant circuit configuration less sensitive. The low current, low offset and low noise requirements for the linear and digital integrated circuits are particularly sensitive. Tradeoffs between these circuit requirements and the required shielding should be carefully analyzed in the design phase. Also additional test data for the particular circuit configurations of interest must be obtained to better define the magnitude of the problem. A radiation dose threshold of 10^6 RADS is probably an upper limit for circuit hardness. According to the environment data presented, this would require a shield thickness equivalent to about 20 mils (0.5 mm) of tantalum. Thus shielding requirements will probably be between 20 and 40 mils (0.5 and 1.0 mm) of equivalent tantalum shielding on each side of the semiconductor chips to overcome the potential surface effects problem. This shielding range will also overcome any expected atomic displacement damage effects as well.

9.1.5.2 Displacement Effects

Low-frequency transistors such as high-voltage and high power transistors are relatively susceptible to displacement damage effects. Since SCR's are essentially two transistors connected in a regenerative circuit configuration, they are subject to the same type of damage. Light-emitting diodes and photo transistors may also be susceptible to this type of damage.

From a design viewpoint, it is obviously helpful to select devices for maximum gain-bandwidth. This is not a complete solution at an environmental level on the order of 10^{12} c/cm^2, however, since the required frequency characteristics may be incompatible with the power or breakdown voltage requirements. Design derating, that is a circuit design which will accommodate a very low transistor gain, is an additional consideration. Shielding is a third design consideration and may in fact be the most practical approach -- particularly for those applications wherein device selection and design derating are of marginal value. An example of this would be an application which required a 1200 to 1500 volt transistor or SCR.

A design dose of 10^{12} equivalent neutrons/cm^2 may induce a considerable degradation in gain in these types of devices. Thus, local shielding must be provided to limit accumulated dose to less than 10^{12} equivalent neutrons/cm^2. Based upon the shielding data provided, a shield thickness greater than that equivalent to about 20 mils (0.5 mm) of tantalum would be required. A shield thickness on the order of 40 mils of tantalum would reduce the accumulated dose to about 5×10^{10} equivalent neutrons/cm^2 which represents a reasonable threshold for displacement damage in the most sensitive devices considered. Thus the shielding range of interest is between 20 and 40 mils (0.5 and 1.0 mm) of equivalent tantalum shielding on each side of the semiconductor chips. Further design tradeoff studies should be performed to further optimize the design from a parts selection, circuit design and shield design point-of-view. Additional radiation test data will also be required for the more sensitive devices for which little data now exists. This includes the high voltage transistors, SCR's and the light emitting diodes and photo transistors in particular.

9.1.6 SUMMARY

In summary, surface effects in the integrated circuits and high voltage devices and atomic displacement effects in low frequency transistors, high voltage SCR's, photo transistors and LED's appear to be the major radiation effects problem areas. Table 20 summarizes these effects. Although circuit design techniques may be used to reduce the influence of the effects on circuit operation, it appears that radiation shielding equivalent to about 20 to 40 mils (0.5 to 1.0 mm) of tantalum will be required. More detailed circuit design and shielding tradeoff studies should be performed in order to better optimize the design. Additional experimental data will also be required on most of the semiconductor devices for the particular circuit configuration being considered.

9.2 PACKAGING CONSIDERATIONS

9.2.1 GENERAL

It was the intent of this study to define solar array/electrical configurations capable of performing high voltage - high power conditioning integral with the rollout solar array, i.e., electronic components would be mounted upon the array Kapton substrate. This goal precluded use of conventional components such as relays, transformers, high voltage capacitors, standard transistor and diode packages which are too bulky to be mounted on the thin Kapton substrate which is wrapped around the support drum for stowage during launch. However, an assessment of packaging requirements and problems relative to implementing the circuit functions with microelectronic components was made. The results of this investigation are presented in this section.

9.2.2 PACKAGING FUNCTIONS AND INTERFACES WITH THE ROLLOUT ARRAY

The electronic circuit package must perform several functions: (1) provision of a mounting surface for components and interconnections, (2) provision of an adequate heat sink to conduct away and radiate dissipated power, and (3) provision for protection against the potentially damaging charged particle radiation environment. Application and extension of existing microelectronic techniques apparently would readily achieve the mounting function. However, as shown in Section 9.3 large heat sink areas (64 cm^2 and greater) are required to limit semiconductor chip temperatures. The largest single rigid package on the referenced GE Rollout Solar Array is the solar cell which is 2×2 cm $= 4$ cm^2 in area. Whereas many individual devices (semiconductors and resistors) may be mounted within the equivalent solar cell area, the required heat sink area is much greater. Thus, techniques must be investigated for providing an effective heat sink area much larger than solar cell area. The drum radius of curvature limits the dimension

of rigid substrates in the direction normal to the drum radius, i.e., the direction of substrates in the direction normal to the drum radius, i.e., the direction of substrate wrap. Thus, it appears that a suitably flexible heat sink must be designed to provide the needed area. Radiation effects analyses indicate that shielding thickness equivalent to 0.040 inches (1.0 mm) of tantalum is required in all directions around semiconductor devices. Total package thickness is therefore a minimum of about 0.090 inches (25 mm) including a 0.010 inch semiconductor chip, and 0.080 inches of tantalum. The maximum envelope thickness of the GE rollout array is 0.055 inches (1.4 mm) which includes cover glass, glass-to-solar-cell adhesive, solar cell, cell-to-kapton adhesive, silver interconnector, kapton, and RTV adhesive button cushions. Therefore, HVSA electronics packages exceed the envelope thickness of the rollout array. Package thickness will be even greater than stated herein because of the semiconductor chip mounting substrate (which may include molybdenum or tungsten base upon an alumina substrate), insulation material, and the kapton substrate.

Several possible alternatives have been identified for mounting the electronics. These include: (1) Increasing the height of the RTV protective buttons from the present 0.040 inches (1.0 mm) to provide greater clearance volume on the backside of the solar cell covered kapton substrate; (2) Providing keyed cut-outs in adjacent substrate wraps about drum into which the packages may protrude from their mounting location; (3) Locating all electronic packages within the available unused volume of the drum; (4) Locating the electronics in the unused "leader area" of the array blanket at the tip (or leading edge member end of the blanket) which is not wrapped around the drum during stowage.

9.2.3 MICROELECTRONIC PACKAGING TECHNIQUES

Two microelectronic packaging techniques can be combined for this application; monolithic and hybrid circuit technology. Monolithic circuitry is restricted to low power applications such as the binary counter with integrated circuit gates and counters and the operational amplifier in the regulation switch.

Many of the remaining circuit functions identified in Section 6, represent HVSA custom designs which can use a combination of integrated circuits for low power dissipation functions and discrete semiconductor chips (transistors, diodes) and possibly resistors (thick or thin film) mounted on one or more substrates for high power dissipation circuit functions; the number of substrates to be determined by considerations of parts type and count, power dissipation level, available package volume, interconnection factors, and circuit fabrication techniques.

Several techniques have been used for making electrical connection to semi-conductors including thermo-compression bonding, ultrasonic bonding, "flip-chip", and "beam-lead" techniques. Regardless of the approach used, the HVSA requires a package capable of dissipating the heat generated within the mounted components.

Flip-chip and beam-lead devices have limited thermal capacity. Conduction of heat through three leads of a beam leaded transistor (measuring two or three mils wide by 1/2 mil thick each) does not compare favorably with the conduction path through the entire twenty or thirty mil square mounting surface of the back of the transistor chip.

A possible packaging approach is to use semi-conductor chips in a planar interconnection system. Several possible approaches to this problem are outlined. The overall processes to fabricate the complete assemblies must be developed, although many of the individual steps such as chip bonding, dielectric encapsulation, interconnective plating, flexible printed interconnection tapes and thick and thin film circuit fabrication are common practice.

9.2.3.1 Thick Film Circuit on Ceramic with Chip Semiconductors and Plated Interconnections

This consists of a ceramic substrate of alumina or beryllia to which conductor runs and passive components are applied by screen printing technology. Semiconductors and other silicon chip devices are next installed in precise locations, using beam splitting microscopes or other forms of optical tooling. This is required

because of the small tolerance available over the entire assembly for mismatch of device terminal pads and interconnection circuitry. A dielectric film can then be added over the entire assembly and etched away in required interconnect pad locations. Interconnection conductor runs can then be selectively plated between the appropriate exposed pads to complete the electrical circuit. A dielectric film coating is added to protect the circuit from adverse environment and handling damage. This interconnection scheme is illustrated in Figure 87.

9.2.3.2 Thick Film Circuit on Ceramic Substrate with a Flexible Circuit or Tape Interconnection System
This system, shown in Figure 88, is similar to the previous configuration except that the interconnection circuit could be prepared before final assembly. Final assembly requires only the mechanical registration and assembly of the interconnecting tape and electrical connection of the appropriate conductor terminals to device pads. This approach has the advantage of minimizing the amount of processing and handling involved by the semiconductors, which usually are the most sensitive components within the assembly. A disadvantage is the tendency of the flexible printed circuit to wrinkle, shifting the position of the interconnection pads with respect to each other, thus complicating the problem of device location and orientation.

9.2.3.3 Thin Film Interconnection System Utilizing a 1 Mil Kapton as a Base Material
Passive components and conductor runs can be deposited on a kapton film using thin film technologies as shown in Figure 89. Semiconductor chips and other devices can then be installed and a dielectric film bonded over the entire surface. Pad areas where electrical connections must be made can then be etched away, and an interconnecting conductor pattern can be added by plating. A final protective insulation layer completes the assembly. A modification of the configuration in Figure 89 above would be necessary to provide a thermal path for high heat dissipating semiconductors. This can be done by mounting these devices on individual ceramic substrates to provide a thermal conducting path radially outward from the device.

9.3 MICROELECTRONICS PACKAGE WEIGHT CALCULATIONS

9.3.1 GENERAL
Microelectronics package weight was calculated for each array mounted circuit function identified in the Functional Block Diagram Typical HVSA Building Block, Section 6, Selected System. Figure 90 identifies the package model employed in the weight calculations. This section describes the assumptions made in the weight analyses and presents for each circuit function all component types, parts counts, total weight and heat sink area.

9.3.2 ASSUMPTIONS
All circuit components, including semiconductor chips and resistors, are bonded to a thermally conductive alumina substrate (0.010 inches = 0.0254 cm thick) which functions as a local heat sink. Radiation shielding is provided by tantalum shielding of 0.040 inches (0.102 cm) minimum thickness surrounding each resistor. Additional shielding provided by the molybdenum or tungsten mounting substrate for semiconductor chips, insulation, kapton blanket, solar cells, adhesives, cover glass, and heat sink has not been considered, but will permit a reduction in tantalum thickness and retain the required total effective shielding. Total package dimensions will increase, however, with the accounting for lower density materials than tantalum.

The required tantalum shielding dimensions were defined in Section 9.1. Required alumina substrate area must simultaneously satisfy two criteria:

1. Semiconductor junction temperature shall be limited to a specified maximum value under worst case power dissipation conditions. The curves in Section 4, Environment Considerations, presents a worst case estimate of microelectronics substrate temperature as a function of power dissipation in the chip and substrate area. Power dissipation within each circuit function is used to determine substrate heat sink area for a specified limit temperature. A limit temperature of $120^{o}C$ ($393^{o}K$) was used except for 2 cases described in the following section.

2. The substrate area must support all mounted components and interconnections. For circuit functions with many components and low heat sinking area requirements the high parts count determines mounting area.

The following material densities were employed in the weight calculations:

Material	Density Pounds/In^3	Grams/cm^3
Tantalum	0.60	16.6
Silicon	0.087	2.7
Resistor (cermet)	0.60	16.6
Alumina	0.134	3.7

Semiconductor chip dimensions used were for the specific transistor type identified. Where the specific device remains to be developed, dimensions were estimated based on existing similar devices. Resistor dimensions were estimated to be 0.150 inches (0.380 cm) by 0.150 inches (0.380 cm) and 0.005 inches (0.0127 cm) thick.

9.3.3 RESULTS

Results of the calculations are shown in Table 21. Because the semiconductor load switch has not been developed and represents a major departure from existing device technology, it is difficult to estimate dimensions and dissipation (forward and leakage). Based upon the device survey conducted in this study, chip dimensions have been assumed and total weight including shielding determined. Load switch weight (8 amp switch) is 0.086 pounds = 39.1 grams. The Load Return/Array ground switch weight is 0.11 pounds = 50.0 grams. Both switches include many parts but heat sink substrate area is determined by leakage dissipation which is estimated between 16 and 300 watts per SCR chip.

Bypass diode weight includes the weight of a 0.0105 inch (0.27 mm) thick by 0.090 inch (2.3 mm) diameter device manufactured by Solitrode Devices and silver interconnection tabs to the solar cells. Shielding is provided by the tabs (top and bottom), insulation, solder, metallization on the diode chip, adjacent solar cells and the kapton blanket. A minimal amount of shielding is anticipated to limit leakage current increases due to radiation.

9.4 DEVICE SURVEY

9.4.1 DEVICE REQUIREMENTS

Analyses of load switching and grounding requirements have identified requirements for a 16 Kv, 8 ampere (maximum) semiconductor switch. Array reconfiguration via stacking switches and regulation switches assumes availability of 1500 volt transistors; devices up to 1400 volts are marketed. Isolation between the high voltage array and spacecraft (or array) signal circuits shall be accomplished with an "assembly" consisting of a "light emitting diode - fiber optics - and a photosensitive transistor" referred to herein as a "high voltage signal coupler". A survey of leading device manufacturers was conducted to ascertain feasibility, development risk, technical response, and cost of development. Proposals were requested in response to the specifications or "design goals" presented in Tables 22, 23, and 24.

9.4.2 SURVEY RESULTS

Manufacturer responses are presented in Tables 25, 26, and 27. Although 16 Kv SCR feasibility is considered unlikely by one vendor, affirmative responses from two sources suggest a phased development effort which initially explores feasibility. Other device problems include: (1) minimum chip thickness possible is 0.1 inch (2.5 mm) which exceeds available void volume on the array substrate; (2) resistivity

required to achieve high voltage capability is 1500 ohm-centimeters; this material has been made but is not readily available; (3) leakage current increases with temperature and above $100^{o}C$ ($373^{o}K$) thermal runaway is a problem; large heat sinks are required to limit device temperature.

Present industrial SCR applications are limited to 2 Kv devices; power generation systems employ stacked 2 Kv devices to obtain hundreds of kilovolts. The highest rated SCR is 10 Kv reported by a Japanese company, but no samples or supporting data is available to substantiate the claim.

Attainment of a 1500 volt transistor requires little or no development since 1400 volt rated units are now available. Requirements for a 1 volt saturation drop and an h_{fe} of 10 may require the major share of the development effort.

Two bids were received to develop a high voltage signal coupler. Company H quoted $50,000 to develop a high voltage isolation switch with an additional $50 per device delivered from the development effort. No supporting discussion was supplied. Company I responded with a 6 month $25,000 effort to develop 12 units and states that because of the thickness restrictions, and high voltage isolation requirements, new wafer and package concepts are needed. The major problem is the method of making permanent electrical contact to the emitter and sensor semiconductor wafers. Device dimensions may be up to 0.060 inch depending upon the contact technique. Company I believes there should be no problem meeting a requirement of 1 nanoampere maximum leakage current at a 16 Kv potential difference but measurements are difficult to perform because of extraneous sources of leakage current.

Catalog, low voltage, light coupled emitter-receivers are available but do not meet essential HVSA requirements. Catalog devices from Monsanto have a 2500 volt isolation rating and exceed dimensional limitations. Texas Instruments had manufactured light coupled devices for ayear and markets the TIXL102 and 103, but these are limited in voltage rating and exceed dimensional requirements. Hewlett Packard catalog data includes two devices, the HP 5082-4309 and HP 5082-4303, rated at 50 Kv and 20 Kv respectively. Development would be required to increase signal level capability and reduce dimensions to meet HVSA requirements. Other applications of high-voltage light-coupled isolators have been described in the literature for voltages of 100 Kv or more (Electronic Products, June 1968 and EDN, February 1970).

9.4.3 DISCUSSION

Development of the SCR appears to be the major device problem. Minimal transistor development is necessary. The high voltage signal coupler requires development centered about techniques of packaging and electrical connections. Array packaging constraints will dictate and closely control signal coupler design.

9.5 OPERATIONAL DESCRIPTION OF HVSA

9.5.1 GENERAL

This section describes a representative sequence of commands required to accommodate each of the various operational modes of the HVSA. The commands are those described in Section 5.2; execution of the commands is performed by the circuit functions described in Section 6. In some cases, alternate command sequences are possible with the selected building block electrical configuration. Specific load characteristics and restraints will of course govern the command sequences and may require design features other than what has been considered in this feasibility study.

9.5.2 COMMAND SEQUENCES

9.5.2.1 Emergence from Earth Shadow

This sequence assumes that all loads have been previously disconnected and that the regulation counters are in any arbitrary state. The sequence is:

ECLIPSE
SUNLIGHT

1. Provide "Array Short" command to all building blocks.

2. Provide "Series Connect" commands to appropriate stacking switches to achieve desired building block series-parallel configuration.

3. Provide 2047 "down-count" signals to each 11-switch building block to ensure that all regulation switches are in shorted position.

4. Provide a pre-determined number of "up-count" signals to each building block to establish a regulation switch configuration corresponding to desired building block output voltage. *

5. Provide "Load Return/Array Ground Switch ON" command to establish HVSA reference point.

6. Remove "Array Short" commands to allow all building blocks to supply a no-load voltage when the solar array temperature has reached at least - 55^{o}C (218^{o}K).

7. Provide appropriate "Load Switch ON" commands to SCR circuits in load switches.

8. Provide normal "up-count" or "down-count" regulation signals to each building block based on remote load voltage sensing.

9.5.2.2 Load Connect

After regulated voltage has been obtained from the appropriately-configured solar array, as described in the previous paragraph, individual loads are connected by providing the "Load Switch ON" command for each load.

9.5.2.3 Load Disconnect

This sequence assumes that loads are connected and voltage regulation has been maintained:

1. Provide "Array Short" commands simultaneously to all building blocks supplying power to the load which is to be disconnected. **

2. Remove "Load Switch ON" command, which removes drive power from load switch SCR's.

3. Provide "Load Switch OFF" command, which turns off series transistors in load switch, ensuring SCR cutoff.

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*The number of up-count signals can be (1) determined by prior experience or calculation, (2) zero if it is desired to connect the load to nominally low voltage, or (3) provided after steps 5 and 6 above, and based on temporarily sensing voltage at the array side of the load switch until the load is connected. The last possibility would require a switchable voltage sensing function.

**If building blocks are common to more than one load, it is necessary to also short the non-common building blocks in the other load(s) while the one load is being disconnected. For example, in the optimized System No. 2, the four 1 Kv, 1.75 A blocks supply current to the 3.5 Kv, 5 Kv and the 11 Kv loads. If it is desired to disconnect only the 5 Kv load (with load switch S2), the six 1 Kv, 0.5 A blocks and the 1.5 Kv, 1A block must also be shorted to protect against a possibly damaging low voltage condition on the 11 Kv load. After the 5 Kv load has been disconnected, both the 3.5 Kv and the 11 Kv loads must also be disconnected, then the array short commands removed, blocks again brough up to regulated voltage, at which time the 3.5 Kv and 11 Kv loads may be connected again.

9.5.2.4 Entering Earth Shadow

To ensure that a possibly damaging, slowly decreasing load voltage condition does not occur as the spacecraft enters the penumbra, the loads must be disconnected while full solar array power is still available near the end of the illuminated portion of the orbit period. The following sequence applies:

1. Provide "Array Short" commands simultaneously to all building blocks.

2. Removal all "Load Switch ON" commands.

3. Provide "Load Switch OFF" commands.

SUNLIGHT
ECLIPSE

4. "Series Connect", "Load Return/Array Ground ON", and "Array Short" commands (in sequence) may be removed at this time if desired.

9.5.2.5 HVSA Reconfiguration

Reconfiguration of the HVSA building blocks into a different series-parallel arrangement can be done upon emerging from eclipse, in which case the command sequence of paragraph 9.5.2.1) applies, or at any other time in the illuminated portion of the orbit. The following sequence for reconfiguration assumes that loads are being supplied in one configuration and it is desired to reconfigure:

1. Provide "Array Short" commands simultaneously to all building blocks.

2. Remove all "Load Switch ON" commands.

3. Provide "Load Switch OFF' commands to all loads.

4. Remove all "Series Connect" commands.

5. Remove "Load Return/Array Ground ON" command.

6. Provide "Load Return/Array Ground OFF" command.

7. Follow command sequence 2 through 8 in paragraph 9.5.2.1.

Table 20. Radiation Effects for HVSA Devices

Damage Mechanism	Primary Radiation Effects	Sensitive Devices	Damage Threshold	Comments
Ionization due to electrons and protons - measured in rads (Si).	In minority carrier devices, the most important effects are an increase in pn junction leakage current and a decrease in transistor current gain.	Low-power linear and digital integrated circuits. High-voltage transistors and SCR's.	10^4 rads (10^2 joules/kilogram)	Low-current circuit configurations are particularly susceptible. Circuit design must provide a large hold-off-current to accommodate the radiation induced increase in leakage current.
Lattice defects due to energetic electrons and protons - measured in equivalent MeV neutrons/cm^2	The lattice defects result in a decrease in minority carrier lifetime which causes a degradation in transistor current gain. Lattice defects also result in an increase in the resistivity of semiconductor material which causes a shift in reference diode characteristics.	Low frequency, transistors, high-voltage SCR's, photo-transistors and LED's. Reference diodes and semiconductor varistors.	10^{11} n/cm^2 10^{12} n/cm^2	Thin-base (i.e., high-frequency) devices should be selected. The operating point for reference diodes is important. Additional test data needed, particularly for high voltage devices.

Table 21. Microelectronic Package Characteristics

CIRCUIT FUNCTION	POWER [a] DISSIPATED WATTS	COMPONENT COUNTS[b] SEMICONDUCTORS	RESISTORS	WEIGHT[c] POUNDS	GRAMS	SUBSTRATE [d] AREA-cm^2
1. Binary Counter	1.2	NSC-DM 7563, (3) T.I. 5400(3)	-	0.0078	3.5	1.0 [e]
2. Fail-Safe Logic (Quad)	0.76	2N930(4) 1N649 (4)	8	0.015	6.8	6.0 [e]
3. Quad LED High Voltage Signal Coupler	0.4	LED (4) [b] Phototransistor(4) Fiber Optics (4)	0	0.0057	2.6	4.0 [e]
4. Quad Regulation Shorting Switch	5.0	2N5151(4) 2N1711 (8) 1C-741 (4)	20	0.043	19.5	16 [e]
5. Blocking Diodes (Quad)	3.5	High Voltage Diodes (4)	0	0.017	7.7	8.0 [f]
6. Parallel Coupling Diodes (1 Quad)	16.0	High Voltage Diodes(4)	0	0.030	13.6	64 [g]
7. Array Shorting Quad Switch & Drivers	5.4	8 Amp Transistor(4) 2N2880(4) 2N1711 (8) 2N2907 (4)	20	0.059	26.7	64 [e]
8. Quad Stacking Switch And Drivers	16.0	8 Amp Transistor(4) 2N2880 (4) 2N1711 (8) 2N2907 (4)	20	0.059	26.7	64 [g]

a. Values represent maximum power dissipated within the "Circuit Function."

b. Total parts count for the associated circuit function. Semiconductor parts count in ( ).

c. Total weight for the associated circuit function.

d. Total substrate area for the associated circuit function.

e. Area determined by parts count.

f. Area determined by dissipation requirements.

g. Heat sink area limits temperature to +150°C (423°K). A larger heat sink is required for a +120°C (393°K) limit but a more sophisticated thermal model is required.

Table 22. SCR High Voltage Switching Devices (Chips) Design Goals

Parameters	Type A	Type B
Forward Blocking Voltage - Volts	16,000, Min.	8,000, Min.
Forward Current - Amperes	1) 0 to 0.250 2) 0 to 2.0 3) 0 to 8.0	Same Same Same
Forward Voltage - Volts	Preferred: 5, Max. Acceptable: 10, Max.	Same Same
Reverse Blocking Voltage - Volts	8,000, Min.	16,000, Min.
Reverse Leakage Current - u A (at Min. V_{RB})	100, Max.	Same
Forward Blocking Leakage Current - u A (at Min. V_{FB})	100, Max.	Same
Holding Current	No Specification	Same
dI/dT Amperes/Second	10^6	Same
dV/dT Volts/Second	10^6	Same
Chip Thickness - inches	0.040, Max.	Same
Chip Diameter - inches	0.75, Max.	Same
Non-operating Ambient Temperature	-170°C to +83°C	Same
Operating Ambient Temperature	-55°C to +83°C	Same
Thermal Cycles - (1,100)	-170°C to +83°C to -170°C	Same

NOTES: 1) Values shown are actual circuit design values without benefit of derating.

2) Devices must be a single chip design.

Table 23. High Voltage Transistor (Chip) Design Goals

Parameters	Value
V_{CEX}	1,500 V, Minimum
I_{CEX}	100 u A, Maximum
H_{FE}, (I_C = 8 A)	10, Minimum
V_{CE} (sat), ($I_C = 5I_B$)	1, V, Maximum
Chip Thickness	0.040 inch, Maximum
Chip Diameter/Length/Width	0.500 inch, Maximum
Non-operating Ambient Temperature	-170 to +83°C
Operating Ambient Temperature	-55 to +83°C
Thermal Cycles - (1,100)	-170°C to +83°C to -170°C

NOTES: 1) Values shown are actual circuit design values without benefit of derating.

2) Transistor must be a single chip design.

Table 24. High Voltage Signal Coupler Design Goals

OUTPUT CHARACTERISTICS

"0" State: Breakdown voltage - 30 V minimum
Leakage current (at 100°C), I_{OFF} - 1/1000 I_{ON}, maximum

"1" State: V_{ON} - 5 V, maximum
I_{ON} - 10 ma, maximum

Output Rise/Fall Times - 5 μsec. maximum

Output/Input Current Gain 0 0.5, minimum

Input Power - 100 mW, maximum

Input to Output Voltage Difference(*) - ± 16,000 V, minimum

Input to Output Leakage Current at ± 16,000 volts difference(*) - 1 nanoamp, maximum

Mechanical:

height:	0.040 inch, maximum
width:	0.75 inch, maximum
length:	12 inches, maximum

Temperature:

storage	-170 to + 100°C
operate	-55 to + 85°C

Thermal Cycles - (1,100) -170°C to +85°C to -170°C

Life - 5 years, deep space

(*) These are application stresses and proper derating will require higher device capabilities.

Table 25. SCR Survey Results

	VENDOR			
ITEM	A	B	C	D
DEVICE FEASIBILITY	NO	YES	YES	?
STATE OF THE ART	NO	NO	NO	NO
VOLTAGE AVAILABLE	-	1300	2000	5000
THICKNESS		0.100 in. (2.5 mm)	0.040 in. (1.0 mm)	0.100 in. (2.5 mm)
SUBSTRATE			MOLY, TUNGSTEN	MOLY, TUNGSTEN
COST $		135 K	20 K	NO BID

Table 26. Transistor Survey Results

ITEM	VENDOR E	F	G
DEVICE FEASIBILITY	YES	YES	YES
STATE OF THE ART	YES	YES	YES
VOLTAGE AVAILABLE	1000	1000	1400
SUBSTRATE	MOLY		
COST $	6.5 K	74 K	NO BID

Table 27. High Voltage Signal Coupler

ITEM	H	I	HEWLETT PACKARD *
DEVICE FEASIBILITY	YES	YES	YES
STATE OF THE ART	YES	YES	YES
VOLTAGE AVAILABLE	2500	5000	50,000
THICKNESS		0.060 inches (1.5 mm)	0.450 inches (11.4 mm)
COST $	50 K	25 K	0.130 K

* - Catalog Data

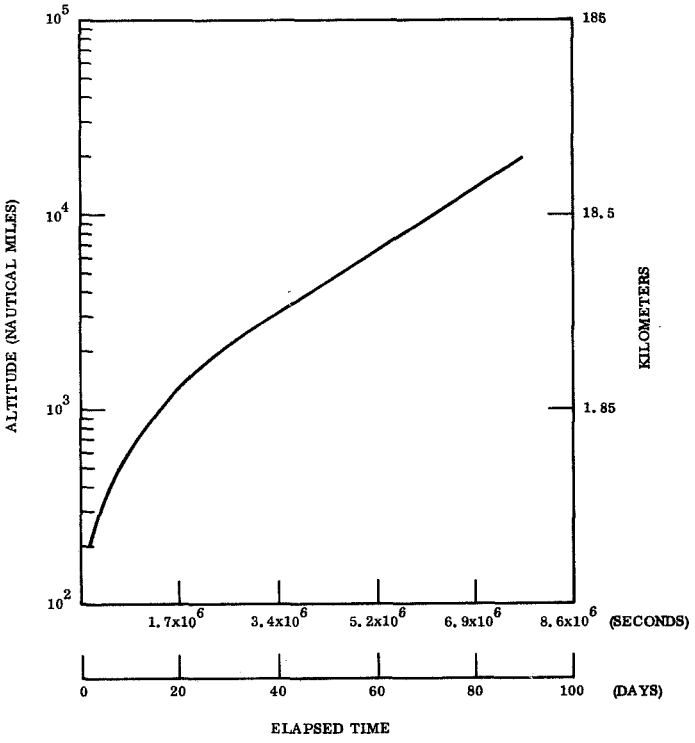


Figure 76. Transfer Phase Orbit Attitude versus Time After Parking Orbit Departure

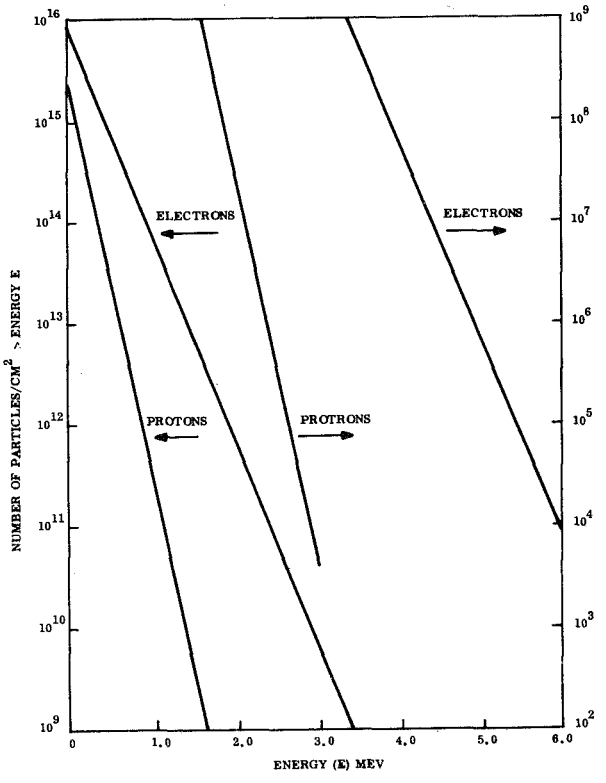


Figure 77. Orbit Phase Omnidirectional Electron and Proton Integral Energy Spectra

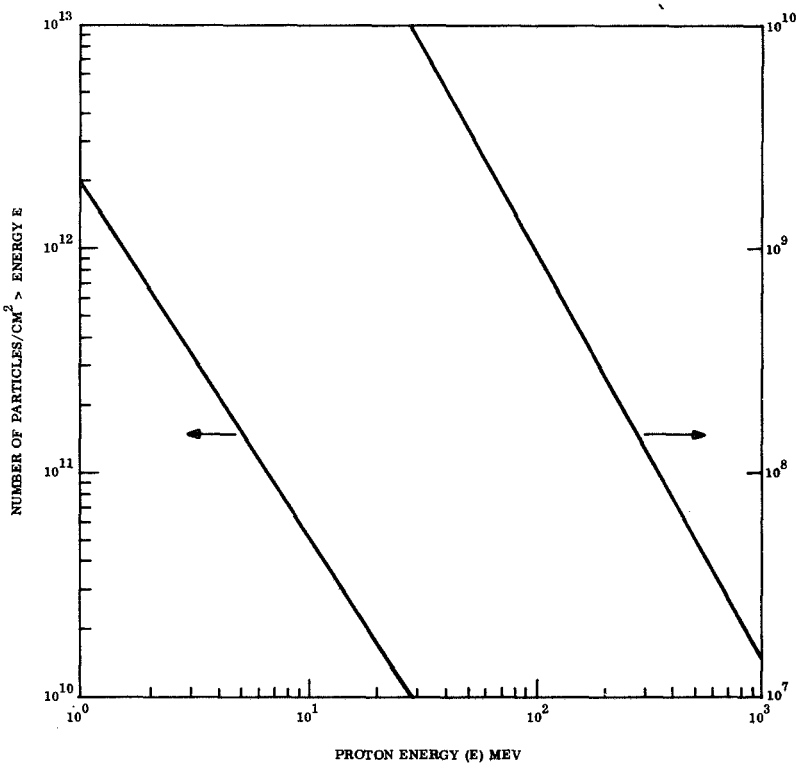


Figure 78. Solar Flare Omnidirectional Proton Integral Energy Spectra

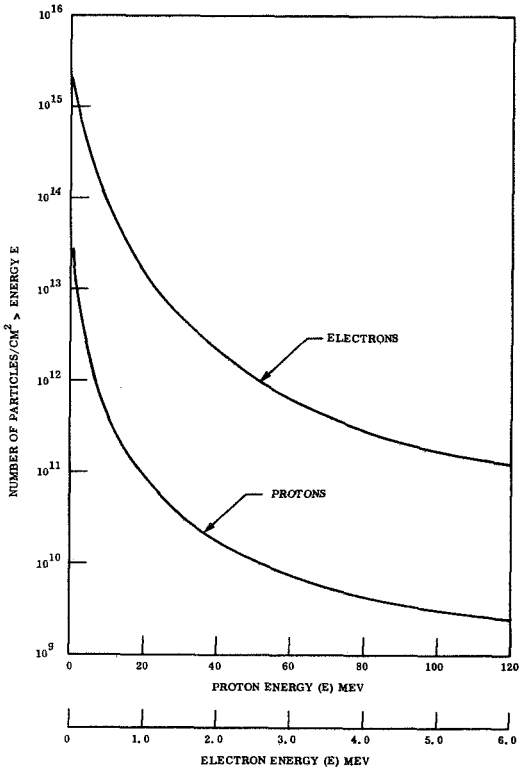


Figure 79. Transfer Phase Omnidirection Particle Integral Energy Spectra

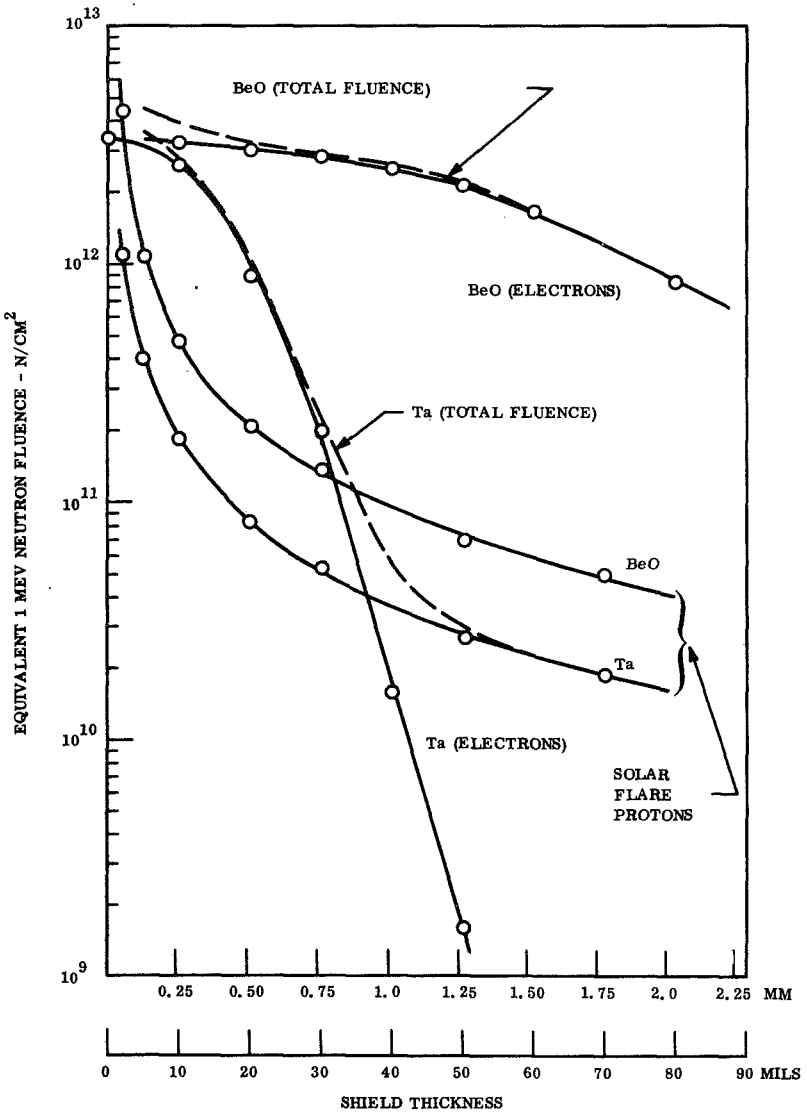


Figure 80. Damage Equivalence versus Shield Thickness for a Five-Year Synchronous Environment

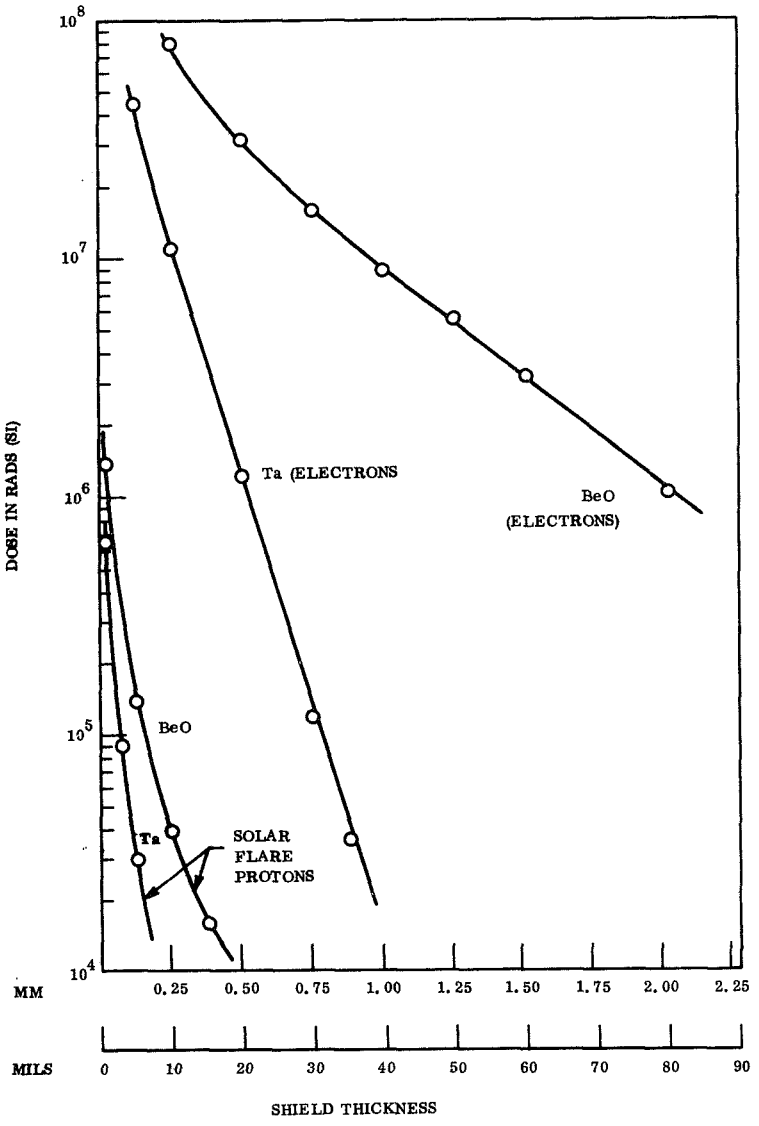


Figure 81. Ionizing Dose versus Shield Thickness for a Five-Year Synchronous Environment

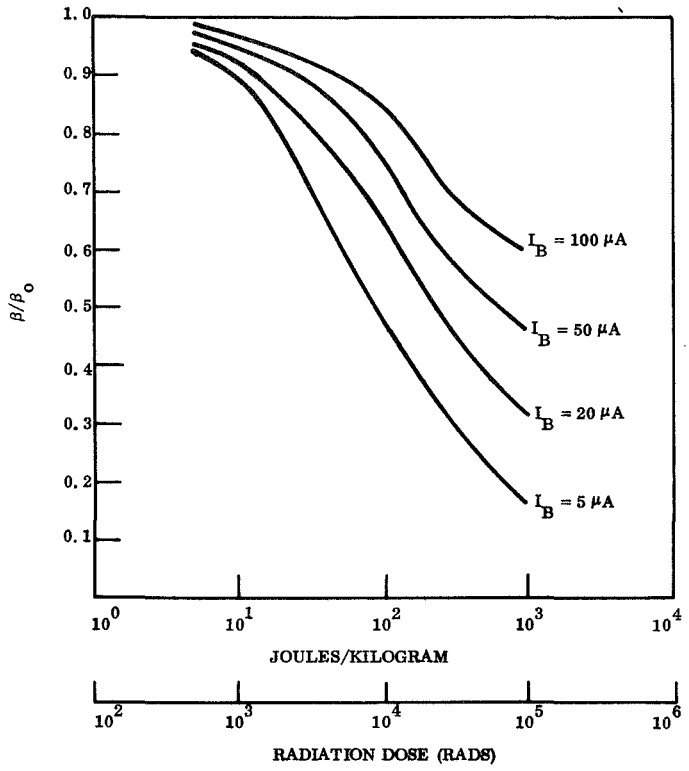


Figure 82. Gain Degradation of 2N708 Transistor

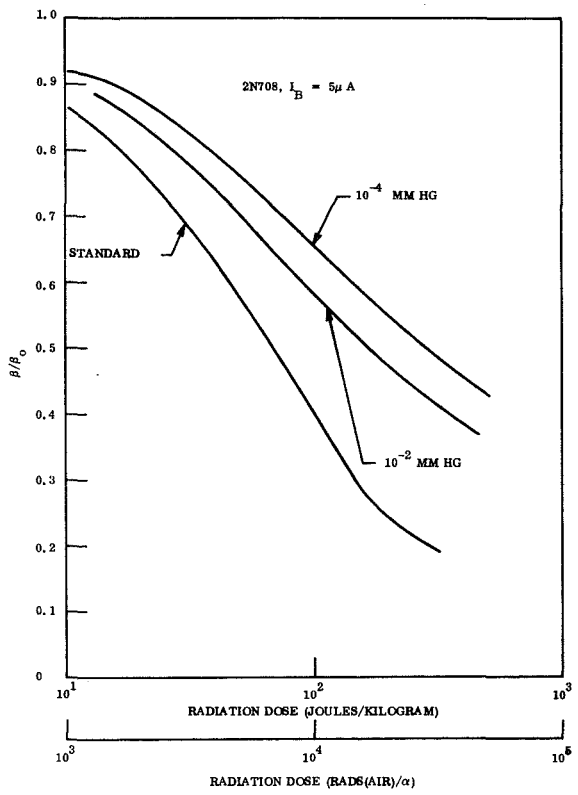


Figure 83. Gain Variation with Radiation and Vacuum, 2N708

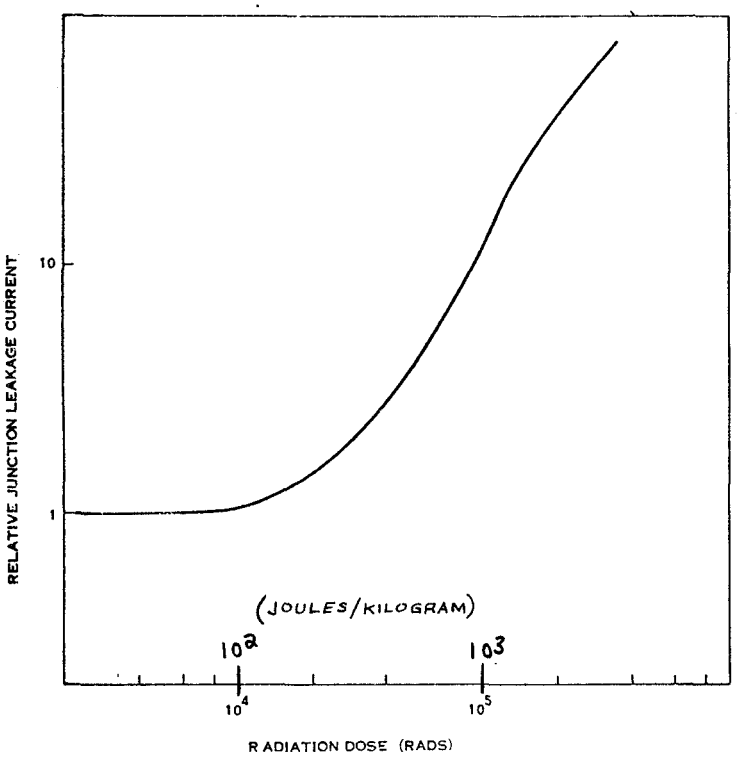


Figure 84. Junction Leakage Current

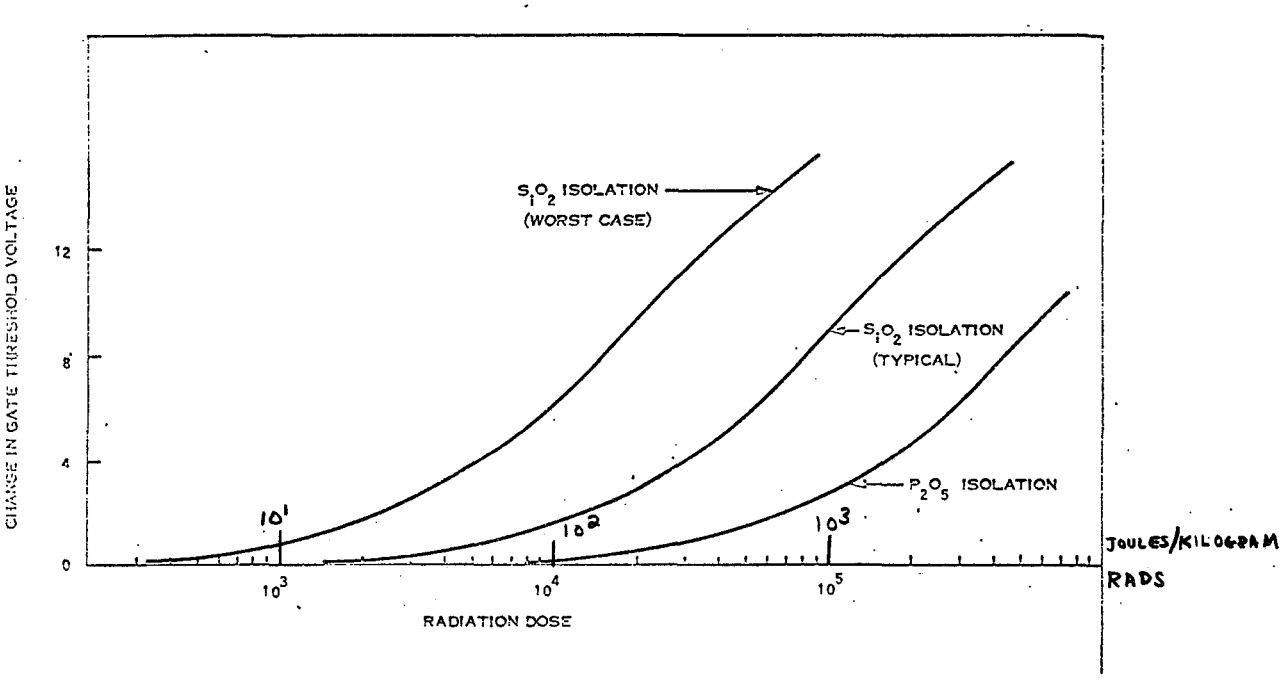


Figure 85. MOS FET Gas Threshold Voltage Change

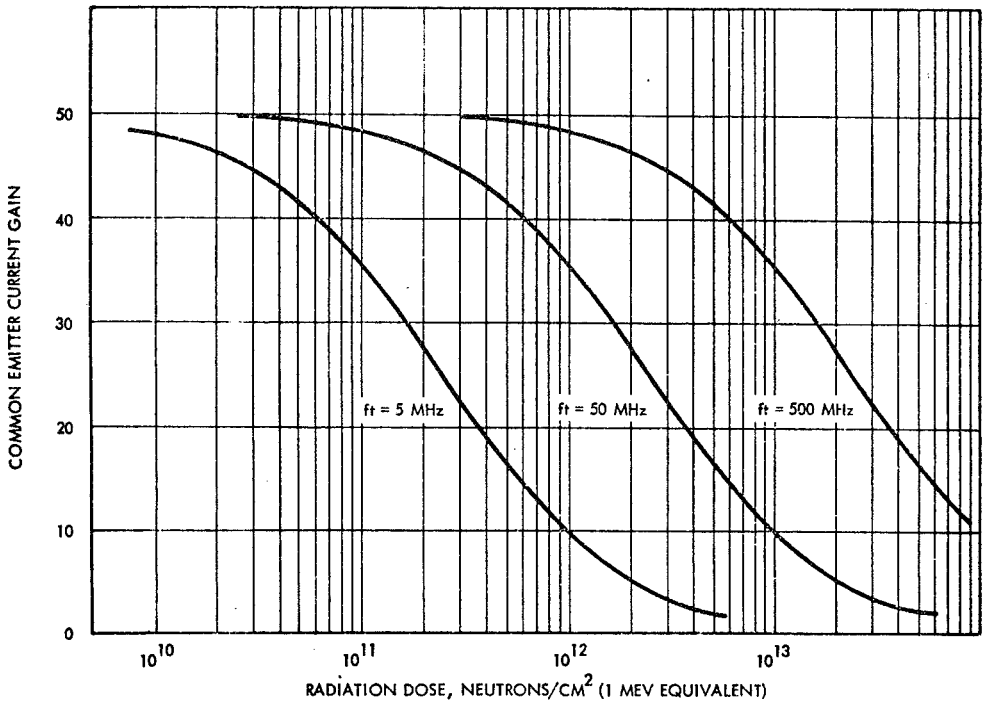


Figure 86. Common Emitter Current Gain versus Newtron Dose for Typical Values of Transistor Gain - Bandwidth Product (f_t)

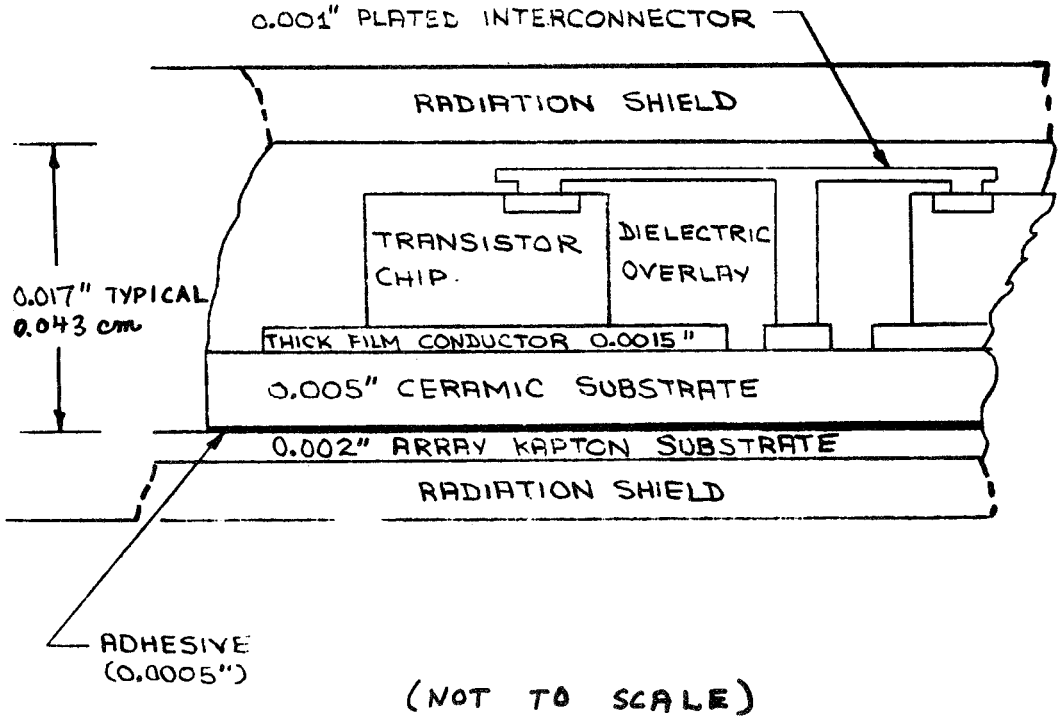


Figure 87. Thick Film Hybrid and Plated Interconnections

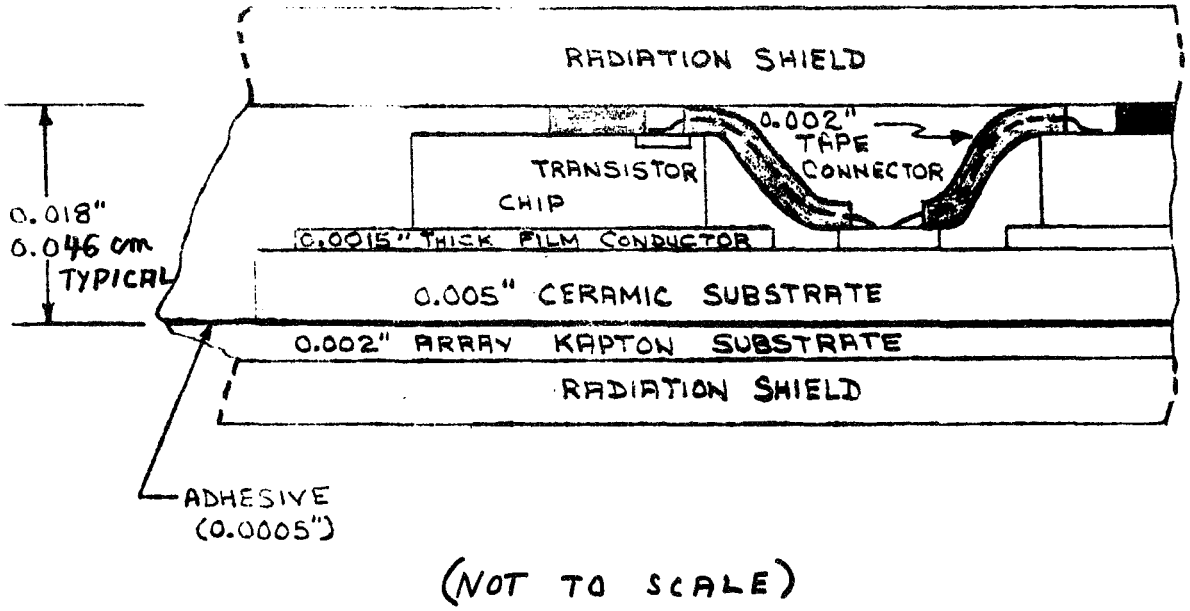


Figure 88. Thick Film Hybrid and Tape Interconnections

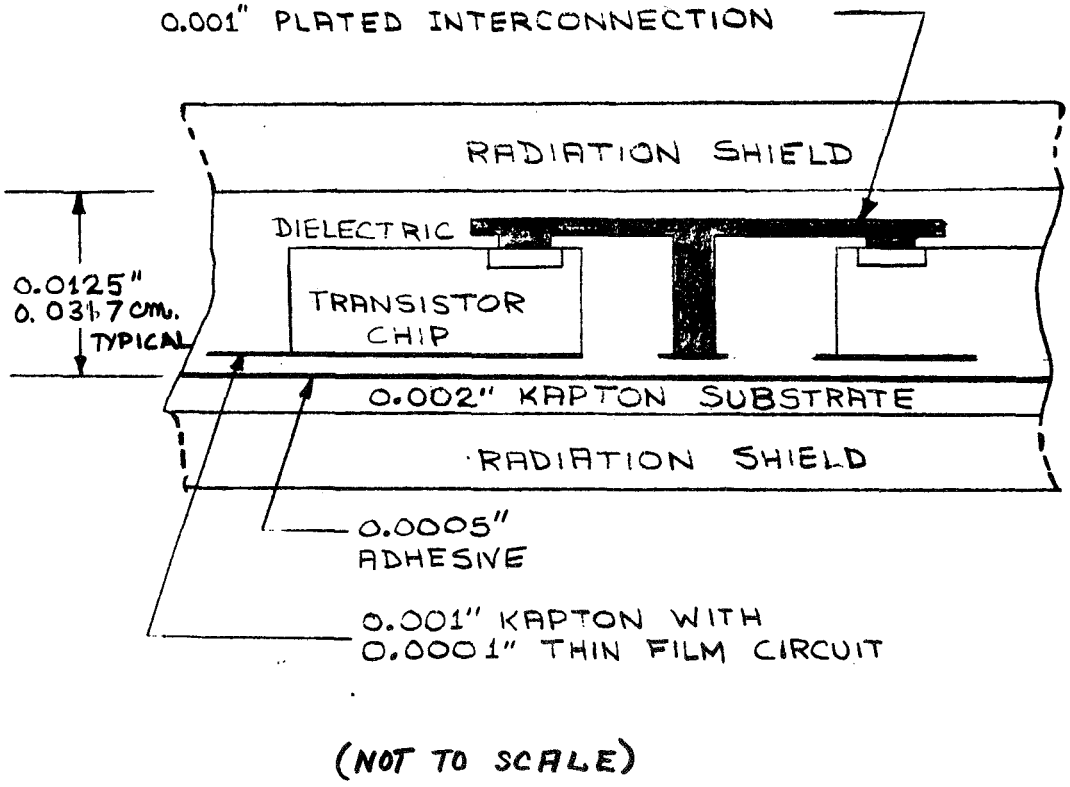
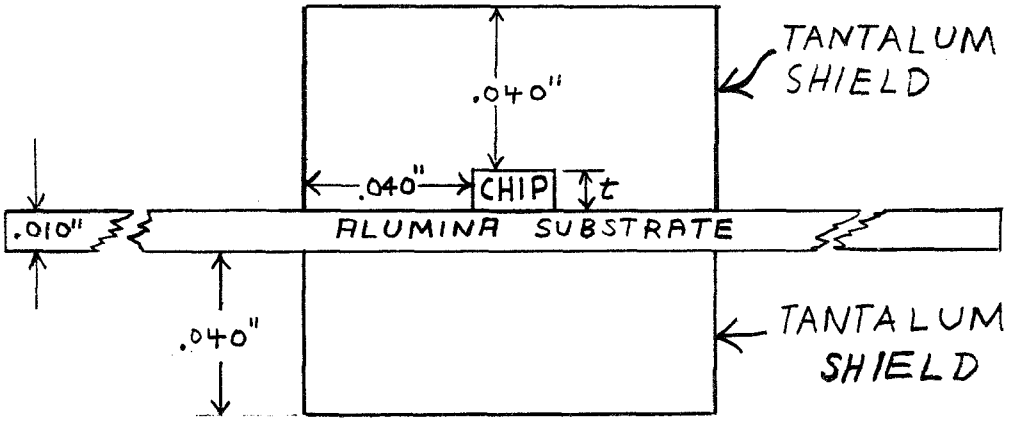


Figure 89. Thin Film Hybrid-Plated Interconnections

MICROCIRCUIT MODEL FOR WEIGHT CALCULATIONS



Tantalum Shielding - .040" reduces ionizing dose to $\sim 10^4$ rads and bulk damage dose to 5×10^{10} equivalent neutrons.

Alumina Substrate - Sized: to limit junction temperature to 120°C, and to Mount chips, resistors, interconnects

Figure 90. Microcircuit Model for Weight Calculations

SECTION 10

PROBLEMS

10.1 GENERAL

A requirement of this study was to identify and define problems associated with the design, fabrication, and test of HVSA electrical configurations and to define future effort required to provide problem solution. This section provides discussions in response to these requirements. Section 11, which follows, will provide a comprehensive description of recommended future effort.

10.2 PROBLEMS

10.2.1 RADIATION DAMAGE IN THE TRANSFER ORBIT:

Section 4, Environment Considerations, presents calculations which show the severe radiation induced performance degradation of the HVSA in a defined transfer orbit from 100 nautical miles to synchronous altitude. An additional 70% array area is required to compensate for this degradation, but array sizing and weight calculations have omitted this cause of array degradation. It was assumed, for this program, that additional systems - oriented analyses were needed to assess the impact of radiation damage. Similarly, the degradation of semiconductor components would also be severe and these effects too were omitted from consideration. Impact of radiation effects can be lessened by 1) using increased shielding for solar cells and electronics, 2) partial array deployment to satisfy transfer orbit power needs while providing shielding for the remainder of the stowed array, and 3) modification of the transfer orbit to raise the parking orbit, reduce transfer time, etc., or a combination of these approaches. The optimum approach can only be ascertained via the aforementioned systems level tradeoffs. Since these tradeoffs were obviously beyond the scope of this study, and the subject performance penalties severe and of little consequence to the basic study objectives, the impact of the transfer orbit environment upon the HVSA has been identified as a major problem requiring further analyses.

10.2.2 RADIATION DAMAGE TO SEMICONDUCTORS

There exists a lack of radiation effects (surface and bulk damage) data for the selected HVSA semiconductor components, as discussed in Section 9.1, Radiation Environment and Effects Predictions. Data is required for each semiconductor type as an unpackaged chip, i.e., removed from its conventional protective container. Furthermore, new devices to be developed for the HVSA must also be characterized in the anticipated radiation environment at synchronous altitudes. Data is required to perform circuit analyses and design, to conduct accurate circuit package designs and prepare weight estimates. Also, auxiliary array power requirements and area are influenced by the amount of beta (gain) degradation permitted at the end of 5 years.

10.2.3 MINIMIZATION OF RADIATION DAMAGE EFFECTS

The analyses of Section 9.1 have indicated the need for approximately 0.040 inches (1.0 mm) of tantalum shielding in all directions surrounding each semiconductor device. Shielding accounts for about two-thirds of electronic package weight and package dimensions. Reduction in the amount of shielding required can produce significant percentage savings in weight and thickness. The discussions in Section 9.2, Packaging Considerations, indicate that package thickness is a major obstacle to achieving a solar array substrate with integral power conditioning. Therefore, alternate techniques of minimizing radiation damage impact on HVSA design should be considered. These include circuit designs which permit parameter degradation at the expense of additional circuitry and drive power (array penalty), and new semiconductor devices with radiation resistant properties. However, emphasizing device radiation resistance may compromise basic device design parameters. The optimum approach to design for minimum radiation effects must be determined for the HVSA application.

10.2.4 THERMAL CYCLING ENVIRONMENT

The HVSA will experience 450 thermal cycles in 5 years at synchronous altitudes and an additional 585 cycles during the assumed transfer orbit trajectory. Thermal cycling is a major potential cause of solar cell array failure. However, conventional solar arrays, i.e., of relatively heavy weight

1.0 pound/ft^2 (4.9 kilograms/m^2) design, have been designed to withstand extended thermal cycling as proved by successful in-orbit performance of many spacecraft. These successes were achieved after extensive solar cell assembly development and test programs whcih determined the proper combination of solar cell interconnect material and geometry, adhesive systems for module and glass bonding, and processes and techniques of soldering and bonding solar cell modules to the array substrate. Similar design and assembly techniques have been applied to the various rollout and other lightweight arrays developed in recent years, but these have not generally received extended cycling tests. The combination of rollout array properties and the typical HVSA mission specified, produce a severe set of thermal cycling conditions.

For example, the low thermal mass of theHVSA, of 0.2 pounds/foot^2 (0.98 kilograms/m^2), results in a high rate of temperature change: about 0.55^{o}K/second upon array emergence from the earth's shadow. The low thermal mass and long eclipse period at synchronous altitude result in a very low end-of-eclipse temperature of -173^{o}C (+100^{o}K). Corresponding characteristics for Nimbus arrays were 5^{o}C/minute (0.06^{o}K/sec) and -52^{o}C (+221^{o}K) for a lower altitude orbit having a shorter eclipse period. The maximum HVSA temperature predicted is +54^{o}C (+327^{o}K) for the solar cells and approximately +120^{o}C (+393^{o}K) for high power dissipating semiconductors. These high temperature limits are equivalent to those experienced on previous spacecraft.

In summary, the rates of temperature change, low temperatures, and temperature range represent a severe challenge to the mechanical integrity of the HVSA solar modules and electronics packages over the anticipated 1035 thermal cycles. A development program is necessary to demonstrate the ability of the solar cells, electronic components, and hybrid metal/substrate and adhesive systems to successfully withstand the thermal cycling environment.

Facilities required for this program include conventional illuminators for solar cell testing, and thermal vacuum chambers equipped with heaters and liquid nitrogen cooling systems to thermally cycle the solar array test specimens.

10.2.5 NEW OR MODIFIED DEVICES REQUIRED

It was the goal of this study to identify and justify the need for new devices and to provide justification that development is feasible.

Requirements for 4 new or modified electronic devices have been identified in this study and discussed in Section 5, Detailed Technical Analysis and Section 9.4, Device Survey. The survey results indicate that high voltage SCR feasibility is questioned, but two vendors believe development is possible. The high voltage (1500 volt) transistor requires some development effort, but may become available in any event if spurred by TV industry needs. Responsive quotes for the "high voltage signal" coupler from two sources and availability of high-voltage (but, low output signal strength) catalog devices from another, provides confidence that packaging and electrical connection problems can be solved with a modest development effort.

In Section 11, Future Effort, a phased SCR development program is recommended, with the initial effort limited to determine device feasibility. However, many other problems exist with a high voltage SCR. These are discussed in Section 10.2.6.

10.2.6 LOAD SWITCH PROBLEMS

High voltage switches are required to apply and remove power from spacecraft loads and to make/break ground connections. Implementation with a 16 Kv semiconductor device located on the HVSA substrate introduces significant device and design problems.

10.2.6.1 Packaging

A 16 Kv SCR has a minimum thickness of 0.100 inches (2.5 mm), which does not include heat sinking and shielding, and therefore exceeds available package volume on the substrate by a significant margin.

10.2.6.2 Thermal

Leakage current increases with area and temperature. Above +100°C (+373°K) leakage is particularly severe and thermal runaway is a problem. Device manufacturers indicate leakage currents may be 0.020 amperes when blocking 16 Kv. Leakage dissipation of up to 320 watts requires very large heat sink areas. Resulting heat sink package requirements may be incompatible with HVSA mounting. Forward dissipation may also be high: a 10 volt drop, presently estimated, produces 80 watts under an 8 ampere load.

10.2.6.3 Material

High voltage capability requires use of high base resistivity (1500 ohm-cm) material, which has been made, but is not readily available and for which there is little experience. Long lead procurement cycles are expected and special processing will be required to maintain resistivity and lifetime.

10.2.6.4 Device Physics

Device feasibility was discounted by one vendor. The major problem is to achieve a high-voltage capability. Present devices are limited to 5 Kv.

10.2.7 VOLTAGE SPIKES PRODUCED BY REGULATION SWITCH ACTION

Binary counter/regulation switch operation produces a net one solar cell equivalent voltage change for each up or down count signal to the counter. However, as discussed in Section 5.2, Power Conditioning, large positive or negative voltage transients can occur during switch operation intervals, because the swtiches do not open and close simultaneously. The concept presented provides for negative-going (reduced voltage) spikes, but this may be unacceptable for many load types.

A practical solution uses filtering at the input to susceptible loads. In addition, the impact upon transient magnitude of solar cell-to-array shielding capacitance and individual solar cell capacitance must be ascertained.

10.2.8 POWER DISSIPATION IN ELECTRONIC CIRCUITS

Heat sink area requirements are established in Section 4, Environment Considerations, based upon the Thermal Model developed in Appendix A. In general, two analytical/design problems exist: (1) An accurate heat sink analytical model including all electronic package elements must be developed to calculate device temperatures because the model presented is accurate only for small, circular, heat sink areas. The model should also include the specific geometry and materials used in the electronics package with laboratory derived data for temperature gradients (°K/watt)across interfaces (chip-to-substrate metallic bonds, cell-to-adhesive bonds etc.). (2) Large heat sink areas, many times the area of the largest cells (2 x 10 cm) will be required; (some heat sinks may exceed 64 cm^2 in area). Heat sink designs compatible with roll-up array packaging restrictions and capable of limiting device temperatures to safe values must be designed, fabricated, and tested.

10.2.9 DEVICE CHARACTERIZATION VERSUS TEMPERATURE

Little data is available describing solar cell performance at temperatures between 0°C (+273°K) and -173°C (+100°K). At temperatures below -55°C (+218°K)*, where regulated power is not required, solar cell parameters are needed to determine the maximum rate of voltage change with time after emergence from the earth's shadow, because of SCR susceptibility to turn on by rapid dv/dt; and to calculate power available for the array shorting switch which must operate to limit maximum available array open circuit voltage during the warmup transient. Data is required to determine auxiliary array power available for power conditioning and array switching functions and main array power to supply spacecraft loads.

* A study ground rule was that load voltage regulation is not required when HVSA temperature is below -55°C (+218°K).

Virtually no data is available for electronic devices at temperatures below -55°C (+218°K). Although regulation is not required below this lower limit the array shorting switches must operate (remain closed), and high voltage signal couplers must provide drive signals to the shorting switches, and all components must survive the temperature excursion. Characterization of essential device parameters below -55°C is a requirement, unless the affected functions are located in a warmer thermal environment.

10.2.10 INTEGRATION OF ELECTRONICS PACKAGES WITH THE ROLLUP-ARRAY

As discussed in Section 9.4, Packaging Considerations, electronics package thickness and area requirements introduce potential mechanical interface problems with the HVSA. The optimum packaging approach must be determined - it will, of course, depend upon results of the "High Voltage Solar Array Study" (Reference 6), required component radiation shielding, dimensions of the new device(s) developed for the HVSA, heat sink area requirements, and mechanical constraints imposed by the rollup solar array.

10.2.11 FAILURE-RATE DATA REQUIREMENTS

Reliability estimates have been performed using available failure rate data for solar cells and electronic components. However, these data are not based upon the complete HVSA environment which includes: (1) operating temperature range from about +120°C (+393°K) to -173°C (+100°K), (2) thermal cycling: 450 cycles between +120°C (+393°K) and -173°K (+100°K) in 5 years at synchronous altitude plus 580 thermal cycles accumulated in the transfer orbit, and (3) device and materials operation under high voltage stress conditions for extended periods. Accurate reliability predictions with high confidence levels require generation of component performance data under the aforementioned conditions.

10.2.12 SOLAR ARRAY TEMPERATURE PREDICTIONS

Many factors influence HVSA temperature, but two have had significant effects upon the study results and require further consideration.

Microelectronic substrate temperatures and heat sink areas presented in Section 4, Environment Considerations, are based upon a HVSA ambient (steady state) temperature of +83°C (+356°K), which is the maximum array temperature in the 100 nautical mile (185 Km) orbit and the defined hypothetical mission. Increasing the parking orbit altitude lowers maximum HVSA and microelectronics temperatures, and permits reductions in heat sink area requirements. This impact of packing orbit altitude must be considered in subsequent studies.

HVSA temperature depends, in part, upon kapton emissivity (E) and solar abosrptivity (α). The range of the reported values of E is 0.65 to 0.89, corresponding to a 12°C (+12°K) span in steady state array temperature and a 6%span in power output.

Furthermore. a literature survey indicates a paucity of α and E data for kapton. Measurement techniques, types of samples measured, and calculation methods vary considerably among the experimenters and may obscure the real dependency of E on thickness, temperature, and backing material. Future programs should include measurements of carefully selected kapton/adhesive/solar cell assemblies to provide statistical confidence for α and E.

10.2.13 OPERATION IN SPACE PLASMA ENVIRONMENT

Operation of the HVSA in the space plasma environment was the subject of a parallel study conducted by NASA-Lewis Research Center (Reference 6). No problems were identified in this study due to the presence of the space plasma.

10.2.14 EFFECT OF SOLAR CELL MISMATCH ON BINARY REGULATION

Differences in current-voltage (I-V) characteristics of solar cells within building block binary sections results in deviations from pure binary boltage increments upon controlled regulation switch operation. Differences in I-V curves can be minimized by cell matching and paralleling many solar cells (to obtain desired building block current) to achieve "averaging" benefits. However, some initial differences

will exist and may be accentuated if radiation damage produces additional variations in I-V curve shapes. Should analyses indicate that differences in I-V curves are significant, measurements of solar cell characteristics versus radiation close will be required to provide statistical information describing curve shape variations.

Open circuited solar cells, caused by interconnection tab failures cause similar, but more pronounced voltage deviations from pure binary operation. Loss of an individual cell results in a lower operating voltage for the remaining parallel cells which are each forced to carry a larger percentage of load current. The impact is greatest for a reference cell failure and in the lower binary sections where each failure is a larger percentage of the total number of cells. The solution which minimizes open circuit impact on binary regulation is the use of additional parallel solar cells for all reference cells and in lower binary sections. The penalty is small because relatively few cells are involved. Analysis is needed to determine percent reduction deviation from pure binary voltage changes versus additional protection provided.

10.2.15 CAPACITIVE EFFECTS

There are several sources of capacitance on the HVSA which may affect circuit and device performance. Sources include solar cell capacitance, capacitance between the metallic radiation shields and electrical conductors, and stray capacitance of circuit elements. The stored energy of these capacitors may produce high rate discharges when regulation, stacking, shorting, and load switches are closed. Stored energy is proportional to the voltage squared (V^2) and relatively small capacitors may deliver large quantities of energy because of the available high voltage levels. Additionally, the contribution, if any, of space plasma to capacitor charging must be considered.

10.2.16 OPERATIONAL PROBLEMS

A potential operational problem exists with the procedure for establishing regulated building block output voltage after spacecraft emergence from eclipse when array voltage is changing and all loads are disconnected: A basic requirement exists to provide regulated voltage, but with the condition of all loads removed the closed loop feedback network which normally provides voltage sensing and adjustment is open and there is uncertainty concerning the instantaneous supply voltage immediately after load switch closure. Several techniques of pre-setting load voltage have been discussed in Section 9.5, Operational Sequences. New techniques may be needed for eliminating or reducing initial voltage deviations depending on the sensitivity characteristics of specific loads.

10.2.17 REDUNDANCY IMPLEMENTATION OF THE BINARY COUNTER

Reliability calculations, Section 8, demonstrate system reliability is limited by the binary counter. The selected system does not provide redundant counters because in general normal regulation in a series string of building blocks can still be achieved with one failed counter. However, the most desirable technique may be to provide redundancy via a majority voting scheme employing 3 or more counters. Diode-or-gating counters are not acceptable when failure results in spurious output(s). Further analyses are required to analyze tradeoffs between using added counters or relying upon the inherent functional redundancy.

10.2.18 TESTS OF HVSA EQUIPMENT

Testing of HVSA functions introduces new test requirements arising primarily because of the array size and presence of high voltages. Problems associated with array size are, however, not unique to the HVSA; for example, large arrays are currently planned for manned space programs. Unusual aspects of a HVSA test program are discussed in the following paragraphs.

- Non-uniform, binary, array sections provide a variety of array sizes to be tested compared to low voltage arrays, without integrated power conditioning, which are usually subdivided into many equal areas.

- A complete test of a building block regulation system requires a building block size illuminator. It is not necessary, however, to provide air mass zero illumination intensity since the main array solar cells can operate at much lower intensity. Auxiliary arrays must be driven to provide only that power expected at the end of design life -- or only about 70% of air mass zero intensity.

- Tests of the stacking switches require more than one array building block. Component tests may be conducted using electronic power supplies to simulate array building block voltages. Functional system tests will require low level illumination of at least 2 building blocks.

- Low level illumination tests on a system of building blocks will satisfactorily check out basic functions. Full scale illumination is necessary to verify performance under worst case thermal conditions, i.e., power dissipation, but this may be possible on a small area basis. Verification of array first-day-in-orbit power capability may be performed under less than full illumination -- this has been done for conventional arrays. However, the minimum required intensity may be greater than that acceptable for functional tests.

- Complete tests of the HVSA will require the availability of load simulators and possibly the real loads if specific load characteristics cannot be confidently simulated.

- Safety - The presence of high voltage will require exercising of normal safety high voltage safety precautions. Safeguards must be provided for personnel, test equipment, loads, and the HVSA. The recommended system includes provisions for shorting complete building blocks when full voltage is not required and personnel protection is needed. However, an unshorted array section of 3000 cells can produce many hundreds of volts under very low (1/10 air mass zero or less) intensity conditions. The possible presence of high voltages will make it necessary to provide external array shorting bars during assembly and repair operations.

- Logistics

  a. Large area facilities are required for array fabrication and inspection.

  b. Large area low level intensity illuminators will be required for testing.

  c. Special test facilities are needed to provide for isolation from high array voltages during all test phases.

  d. Complete thermal-vacuum testing of an illuminated HVSA is prohibited by size limitations of available facilities, but outdoor sunlight or indoor tests under low level illumination is practical and should be meaningful if sufficient lower functional level tests are conducted in vacuum.

SECTION 11

FUTURE WORK

11.1 GENERAL

Recommendations for future work, presented herein, are based upon study conclusions that the HVSA is feasible and capable of delivering conditioned high voltage - high power at a significant saving in weight compared to conventional conditioning techniques. Future work is needed to resolve the problems defined in Section 10 and perform those tasks which culminate in hardware development, fabrication and test.

Future work shall be divided into categories convenient for discussion. Timing and phasing of these efforts shall, of course, depend upon program level considerations.

11.2 DEVICE DEVELOPMENT

1. Phased development of a high voltage SCR should be started, with the initial goal to resolve the question of device feasibility. A positive finding should be followed by determination of performance - particularly reverse current leakage and forward voltage drop since these are significant to successful thermal designs. Should subsequent effort be desirable, it will be necessary to develop firm performance requirements and proceed to define processes, purchase raw materials, design and build specialized processing equipment, and fabricate, test and evaluate small quantities of devices.

2. Availability of a 1500 volt transistor appears possible within the next year. Some development is likely to be required to meet gain, current, and saturation voltage requirements peculiar to the HVSA.

3. Development of a high voltage signal coupler is required. Major items requiring attention are output signal strength, minimization of package thickness, and making electrical connections to the input and output devices.

4. High voltage coupling diodes rated at 1500 volts, can replace transistor switches for parallel connection of building blocks, and should be developed.

5. Because high voltage SCR feasibility is in doubt and SCR thermal dissipation on the HVSA kapton substrate may be a design limitation, a high voltage electromagnetic vacuum relay should be developed. Although 17 Kv-8 ampere vacuum relays are available, device dimensions range upward from approximately 2 inches (5 cm) and are incompatible with substrate mounting. It may be practical to mount relays external to the spacecraft structure, for example, within the rollout array drum void volume. Modification of existing relay designs to reduce weight and volume should be considered early in the development cycle.

11.3 PROOF OF PRINCIPLE DEMONSTRATION

The selected method of array voltage regulation employs a binary-weighted digital switching system. Feasibility and operating principles have been analytically demonstrated. The next step includes fabrication and test of a small-scale solar array with breadboard electronics using conventional components to serve as a live demonstration of proof-of-principle.

The solar array need only be sized for minimum current output, using a single series connection of conventional 2 x 2 cm solar cells. Table 28 presents the total solar array area required to configure an 11 binary switch 750 volt output building block capable of being regulated to within $\pm$ 0.1%. Low level intensity illumination of the solar array would suffice to demonstrate regulation capability. Anticipated variations in solar array I-V curves can be produced by adjusting illumination level and temperature, the latter using

a combination of refrigerated air and heaters. The basic configuration is similar to the selected building block except for the addition of those functions performed by the spacecraft computer and data processing equipment.

A block diagram of the breadboard regulation scheme is shown in Figure 91. It includes a load voltage sampling network, a constant voltage reference, an error amplifier that compares the two signals, and two threshold detectors to determine if sampled voltage is too low or too high. Only one threshold detector will have an output at any time; each detector is connected to one gate, and in the presence of a detector and clock signals, a counter changes state by one count. The activated detector determines whether the count should advance or decline, at the clock rate. Counter output is coupled to the shorting switches through driver stages.

Other building block functions are readily incorporated. Off-the-shelf transistors can be used to perform the array shorting switch function; and conventional relays can be used as high voltage load switches and signal couplers.

Loads may be simulated with provisions for varying the load current and transient loading.

The solar array may easily be fabricated on a kapton substrate to provide realistic simulation and to allow for subsequent upgrading or thermal vacuum cycling tests.

Tests shall demonstrate regulation capability as a function of load and array changes, impact of solar cell failures upon regulation, shorting switch operation, and techniques of establishing building block voltage prior to load switch closure.

11.4 POWER SYSTEMS ANALYSES

Detailed design of a solar array is preceded by spacecraft level and power systems studies and tradeoffs. These latter analyses consider mission goals and spacecraft requirements; alternate power systems are compared on the basis of performance, spacecraft compatibility, cost, development risk, growth capability etc. Ultimately a single configuration is selected for detailed performance analyses and design. Hardware design is based upon performance and interface specifications prepared during the power system design effort. Table 29 identifies some of the many factors that are included within the power systems and array analyses. When these analyses are completed hardware design can logically follow.

11.5 HVSA DESIGN AND DEVELOPMENT PROGRAM

11.5.1 GENERAL

Progress and results of new device development, device improvement, proof-of-principle breadboard regulator tests, power systems and array analyses, and solution of the outstanding problems (Section 10) will have a major effect on the timing and scope of a program to design and develop a full scale building block (array with integrated power conditioning) mounted upon a roll-up solar array. This section identifies the effort to design, develop and test a prototype HVSA employing all the functions, but not the total solar cells, of two building blocks. The components, materials, manufacturing processes, designs, inspections and controls, and performance criteria are intended to be identical to that of a flight HVSA. The quantity of solar cells would be limited as a cost effective measure.

11.5.2 TASKS IDENTIFIES

1. Definition of interfaces (mechanical, thermal, electrical, dynamic) and performance requirements

2. Mechanical design of selected configuration - layouts, stress analyses, design of all hardware elements including drum, boom, substrate, leading edge member, attachment hardware to spacecraft structure. Solar cell module design.

3. Electrical design of solar cell array, power conditioning, and switching functions. Detailed electrical design of all electronics functions. Determination of number of series/parallel solar cells to meet building block required output. Exact sizing of solar array to meet 5 year design goal.

4. Thermal analyses of solar array substrate, solar array structure, and all circuit functions to define packaging requirements and temperature limits.

5. Packaging design and fabrication of all circuit functions using microelectronic components and processes.

6. Assembly and wiring on the kapton substrate of a single building block with a partial main (power) solar array, all (packaged) electronics functions, and all auxiliary arrays. Total building block voltage, about 1 Kv, shall be supplied by series connected solar cells. Limited quantities of parallel connected cells shall be provided. Glass chips provide mechanical simulation where solar cells are omitted.

7. Assembly and wiring of an additional building block with a main solar array, all electronics functions, and all auxiliary arrays. The main array will provide full output voltage but with only a single row of solar cells. Use of this building block described in item (10).

8. Design and fabrication of electronic load simulators, electronic building block simulators to attain 16 Kv capability, and low level illuminators for solar cell power generation.

9. Environmental Test Program

   a. Thermal cycling representative of mission

   b. Operational tests to reproduce thermal dissipation extremes, demonstrate regulation capability under "cold" array conditions, and operate array shorting switches under "cold" array conditions.

   c. Assembly of two building blocks to a rollout structure including drum, boom, leading edge member, attachment hardware. Conduct stowed dynamic tests, deployment-retraction cycles, and resonance survey in deployed mode.

10. Operational Tests to demonstrate operation of all electronic functions within the building block. Use of two building blocks to demonstrate parallel operation of regulation systems in response to dynamic loading. Use of live and electronically simulated building blocks to demonstrate high voltage switch operation.

11.6 PROBLEM SOLUTION

The effort to resolve those problems identified in Section 10 are assigned, in Table 30, to the specific category of future work that produces the most effective results.

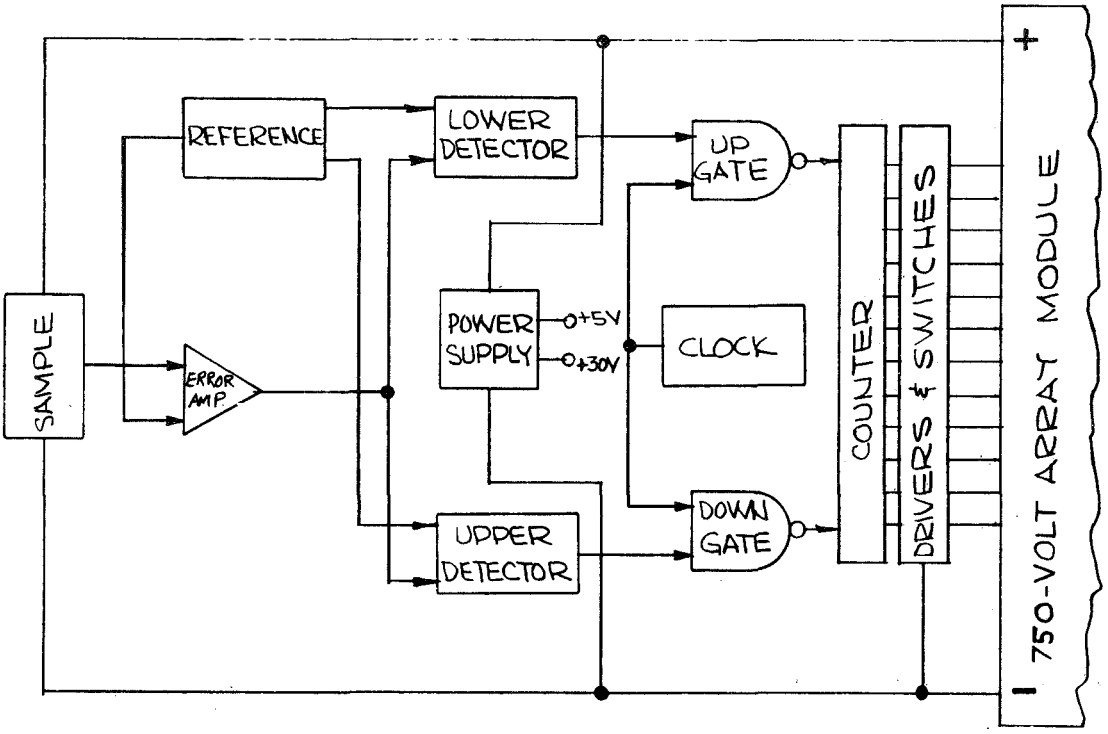


Figure 91. Breadboard Voltage Regulation Block Diagram

Table 28. Solar Array Area for Breadboard Regulator

NUMBER OF BINARY SWITCHES	INCLUDES BINARY LEVELS	TOTAL ARRAY AREA	
6	1, 2, 4, 8, 16, 32	0.5 ft.^{2}	(0.047M^2)
7	above plus 64	0.8	(0.074)
8	above plus 128	1.4	(0.13)
9	" " 256	2.6	(0.24)
10	" " 512	5.0	(4.6)
11	" " 1024	10	(9.3)

Table 29. Power Systems and Array Design Analysis Factors

I. POWER SYSTEMS

- o Mission goals
- o Design life, orbit characteristics
- o Launch vehicle constraints
- o Operational date, development and test cycle
- o Reliability goals, redundancy
- o Load descriptions: voltages, AC/DC split, regulation required, essential & non-essential load profiles, transient requirements; energy storage requirements.
- o Spacecraft: configuration, orientation in-orbit, dynamic inputs, thermal control and limits, shadowing.
- o Environment: radiation (particle, UV), vibration, shock, acceleration, atmosphere, rocket exhaust
- o Performance verification: ground test, telemetry
- o Power transfer and orientation systems

II. ARRAY

- o Configuration: launch stowage; number and size of sub-arrays; attachment location to spacecraft; orientation axes and deployed configuration
- o Electrical: required power; voltage levels; sizing for area; numbers of series/parallel cells; interface with power conditioning; shadowing effects
- o Dynamics: launch environment; deployed (natural forces, perturbations).
- o Mechanical: stress analyses; thermal bending; weight versus aspect ratio tradeoffs
- o Power Transfer and Orientation: interfaces; power required; life;

Table 30. Problem Resolution Keyed to Future Effort

Problem Area	Program Phase
Radiation Damage in Transfer Orbit	MS
Radiation Damage to Semiconductors	H
Minimization of Radiation Damage Effects	H
Thermal Cycling Effects	H
New or Modified Devices	D
Load Switch Problems	D, H
Voltage Spikes	H
Power Dissipation in Electronic Circuits	H
Device Characterization Vs. Temperature	H
Integration of Packaging with the Array	H
Failure Rate Data Requirements	H
Solar Array Temperature Predictions	PSA, H
Operation in Space Plasma Environment	--
Mismatch Effects on Binary Regulation	P, H
Capacitive Effects	P, H
Operational Problems	PSA, P, H
Redundancy Implementation of Binary Counter	PSA, H
Tests of HVSA Equipment	H

D - Device Development

P - Proof of Principle Demonstration

MS - Mission Studies

PSA - Power Systems Analyses

H - Hardware Design and Development

SECTION 12

CONCLUSIONS

The purpose of the subject effort was to study electrical configurations for a high voltage solar array (HVSA) that would provide regulated D. C. power directly to spacecraft loads. Primary goals included definition of (1) conceptual designs of electrical configurations for HVSA systems with integral power conditioning, i.e., where all power control functions are array mounted, (2) problems (particularly with switches) associated with HVSA power system development, and (3) future effort to resolve problems identified.

The following results and conclusions have been derived on the basis of the subject study effort.

1. The high voltage solar array (HVSA) concept with regulation by a binary coded switching system is feasible.

2. The significant environmental factors affecting operation and survival of the HVSA are charged particle radiation damage and thermal cycling.

3. All switching functions, except for load and grounding switches, can be performed using transistors. Transistors with up to 1500 volt ratings are expected to be made available with some development effort.

4. A quad redundant arrangement of all switch functions is required to approach system reliability goals.

5. Load and ground switches require a 16 Kv blocking capability which is not available with existing semiconductors. Maximum reported capability is 5 Kv for a device developed in the United States; the Japanese claim 10 Kv capability.

   Because the feasibility of a 16 Kv SCR (silicon controlled rectifier) is questionable, and very high power dissipation is predicted for such a device, it is recommended that load and ground switching be performed withinthe spacecraft using electromagnetic vacuum relays.

6. The binary coded switching regulation system with controlled voltage switches is superior to conventional series and shunt regulated power systems and other digital regulation systems. This system features maximum efficiency, minimum parts count, and low power dissipation.

7. The HVSA should be synthesized from switchable building blocks. Maximum system efficiency is achieved by designing building blocks for highest voltage (1500 volts, limited by transistor capability) and maximum current, which minimizes the number of building blocks. Highest reliability is achieved with many parallel connected solar cells and bypass diodes across small numbers of series connected rows of solar cells.

8. Isolation between signal circuits and high voltage circuitry can be achieved with a high blocking voltage, (16 Kv) low level, signal coupler. This device consists of a light emitting diode-fiber optics-photo sensitive transistor assembly. The device is feasible and requires development for electrical interconnections and packaging compatable with array substrate mounting.

9. Large voltage spikes can occur as a result of binary regulation switch operation, but their effects can be minimized by design or changes in operational procedures.

10. Wide temperature extremes preclude $\pm$ 0.1% regulation tolerance if voltage references are mounted on the array substrate.

11. The present solar cell module design is not qualified over the predicted HVSA temperature extremes.

12. Transfer orbit charged particle radiation damage results in very high HVSA area and weight penalties.

13. Spacecraft loads must be protected by an array shorting switch during (a) HVSA reconfiguration, (b) the post-eclipse array thermal transient and (c) load connect and disconnect operations.

14. Regulated load power is delivered by a HVSA building block, employing a binary-coded switching arrangement, at 117 watts/m^2 and 80 watts/Kg.

15. Phased development of a 16 Kv SCR should be initiated to ascertain feasibility. Parallel development of a high voltage electromagnetic vacuum relay should be conducted.

16. HVSA testing appears practical; it will require large scale illuminators operating at reduced intensity to check most functions. Safety of equipment and personnel will require usual high voltage practices and procedures.

17. Power dissipation in the binary regulation switches is not a problem, however, HVSA reconfiguration switches will require special design consideration to limit temperatures. SCR load switches, if used, have potentially high dissipation and may present difficult design problems.

18. Future work recommended includes device development, test of a breadboard "binary" regulator to demonstrate proof-of-principle, resolution of defined problem areas, and subsequently, design and development of a high voltage building block.

REFERENCES

1. "Handbook of Space Environmental Effects of Solar Cell Power Systems," Exotech Inc., prepared under NASA Contract No. NASW - 1345.

2. J. D. Lieux, "A New Approach to Low Drift Amplifiers", Fairchild Technical Note, March 1968.

3. A. F. Obenschain and R. Rasmussen, "The Solar Array Synthesis Computer Program", NASA-GSFC Document No. X-716-69-390, dated September 1969.

4. Brown, W. L., J. D. Gabbe and W. Rosenzweig, "Results of the Telstar Radiation Experiments," Bell System Tech. Journal 42:1505-1561, July 1963.

5. F. A. Shirland, A. F. Forestieri and A. E. Spakowski, "Status of the Cadimium Sulfide Thin-Film Solar Cell", Intersociety Energy Conversion Engineering Conference 1968 Record, Vol. 1, pp 112-115.

6. "High Voltage Solar Array Study," parallel study conducted for NASA - Lewis Research Center under Contracts NAS 3-11534 and NAS 3-11535.

APPENDIX A

DETERMINATION OF MICROELECTRONICS SUBSTRATE TEMPERATURE

The purpose of this study was to determine if sufficient heat transfer exists between the microelectronic semiconductor switching device, the space environment and the roll-up solar array during worst case conditions, i.e., (a) maximum solar intensity on the front side of the array, (b) an on-state condition of the switch, and (c) a low orbital altitude of the spacecraft, to maintain a safe operating temperature. Heat input from both earth emitted radiation and reflected sunshine (albedo) are greatest at the lower altitudes.

The steady state high temperature of the array is calculated from established values of emissivity and absorptivity, solar input at an average 1.0 A.U. orbit, albedo, earth radiation and the amount of electrical power extracted from the array circuitry. The treatment of all energy inputs and outputs yields the following relation.

$$\frac{mcdT}{dt} = (\alpha_1 - n) A_f S + \bar{\alpha} A_t \bar{\rho} + \bar{\epsilon} A_t \bar{\mu} + Q_i - \epsilon_1 A_f \delta T^4 - \epsilon_2 A_b \delta T^4$$

Q_i = Internally generated heat (power dissipating device)

α_1 = Front side absorptivity

ϵ_1 = Front side emissivity

n = Solar cell conversion efficiency

α_2 = Back side absorptivity

ϵ_2 = Back side emissivity

S = Solar power input

$\bar{\rho}$ = Reflected sunshine at altitude

$\alpha = \frac{\alpha_1 + \alpha_2}{2}$ = Average Absorptivity

$\epsilon = \frac{\epsilon_1 + \epsilon_2}{2}$ = Average Emissivity

$\bar{\mu}$ = Emitted earth radiation at altitude

δ = Stefan-Boltzmann Constant

A_f, A_B, A_T = Area of front, back, and total array, respectively

T = Temperature

m = Thermal mass

c = Specific heat

t = Time

Because steady-state temperature T_{ss} is desired, $\frac{dT}{dt} = 0$ and T_{ss} is evaluated:

$$T_{ss} = \left[\frac{(\alpha_1 - n) A_f S + \alpha A_T \rho + \epsilon A_T \mu + Q_i}{\epsilon_1 A_f \delta + \epsilon_2 A_b \delta} \right]^{1/4} \quad (1)$$

Using the physical values associated with the array (See Section 4, Environment Considerations), the high temperature was evaluated to be 82°C (355°K), corresponding to array position over the subsolar point in the 100 NM (185 Km) orbit with no electrical power being delivered to the spacecraft from the array (n = 0).

The total impact of internally generated heat from semiconductor switches has a minor effect on average array temperature compared to solar input. However, localized switch/substrate temperatures may be high enough to cause malfunction because of the small dissipating volume of the switch and the inherently poor thermal conduction on the kapton array substrate. The following thermal investigation determines the temperature of the local high-dissipation switch by iterative computation.

Heat is removed from the dissipating element by two methods, conduction and radiation. Conduction takes the form of radial heat flow from the microelectronic device to the surrounding isothermal solar array blanket. In general, radial heat flow is expressed by:

$$q_c = \frac{2 \pi h K (T_1 - T_2)}{\ln \frac{r_2}{r_1}} \quad (2)$$

where

q_c = the heat removed by conduction

T_1 = dissipating element temperature

T_2 = array temperature at distance r_2

K = conducting medium thermal conductivity

r_1 = radius of an equivalent, circular area of the heat producing element

r_2 = radial distance from the dissipating element to the heat sink (solar array blanket) temperature, T_2.

h = thickness of the conducting material.

Figure A-1 represents the geometry used to establish the conduction equation. As the value of r_2 is increased, T_2 will approach the array heat sink temperature. In the application under consideration, this is due to the fact that the total power to be dissipated is a small fraction of the total heat input to a given section of solar array blanket. For example, if 2.5 watts of dissipation is generated in an alumina semiconductor substrate having an area of 4 cm^2 and heat transfer is assumed to occur only by radiation from the 4 cm^2 substrate area and by conduction through the rollup solar array blanket, the temperature of the 4 cm^2 substrate will be about 118°C for an array heat sink (blanket) temperature T_2 = 82°C (355°K). About 0.4W will be radiated from the 4 cm^2 area, and neglecting actual additional radiation from the array blanket, 2.1W is conducted through the array blanket, radially away from the 4 cm^2 area. At a radial distance 6 inches (15.2 cm) away from the dissipating alumina substrate, the 2.1W represents less than

2% of the heat input received by the array blanket from solar energy, and hence will have a negligible effect on blanket temperature. Consequently, the value of 6 inches (15.2 cm) was used for r_2 in evaluating Equation (2). Neglecting radiation from the array blanket of the heat conducted away from the dissipating alumina substrate not only greatly simplifies the thermal model, but also produces a somewhat conservative evaluation of maximum semiconductor temperatures, providing a small safety margin. It is also noted that the 82°C (355°K) array blanket temperature is conservative also, in that it is based on an unloaded array (n = 0 in Equation [1]) directly over the subsolar point in a 100 NM (185 Km) orbit. Loading the array to a solar cell efficiency of 8% reduces this temperature about 10°C (10°K) as shown in Section 4, Environment Considerations.

PHYSICAL LAYOUT OF CONDUCTING MEDIUM

Figure A-2 illustrates the conducting medium in the roll-up array. Figure A-3 presents the conducting medium on a nodal basis. Adjacent surfaces in the array "sandwich" construction lie in nearly the same isotherm as the switch/substrate device; the small temperature gradient is due to the relatively thin layers and large surface areas. As shown in Figure A-3, the temperature drops (t_d) through the array cross section are small; less than 1°C (1°K) total. This allows modeling of an isothermal heat-generating source at a temperature T_1 (as shown in Figure A-1) to replace the switch/substrate/array sandwich.

In the plane of the array, heat conduction is poor due to the small cross-sectional area of the materials and dependent largely on the silicon/expanded metal. Heat conduction through the kapton is minimal. Based on the heat conductivity values in Table A-1, assumption is made of a uniform conducting medium with the conductivity of silicon in order to evaluate the model in Figure A-1 with Equation (2).

Surface radiation also removes energy as described by equation (1) where,

$$T_1 = \left[\frac{\alpha_1 A_f S + \bar{\alpha} A_T \bar{\rho} + \bar{\epsilon} A_T \bar{\mu} + q_r}{\epsilon_1 A_f \delta + \epsilon_2 A_b \delta} \right]^{1/4} \tag{3}$$

Here values of A_f, A_b, and A_T are the radiating surfaces of the switch substrate device.

The sum of the semiconductor switch dissipation energy conducted and radiated is,

$$Q_i = q_r + q_c \tag{4}$$

Equation (3) becomes,

$$T_1 = \left[\frac{\alpha_1 A_f S + \alpha A_T \rho + \epsilon A_T \mu + Q_i - q_c}{\epsilon_1 A_f \delta + \epsilon_2 A_b \delta} \right]^{1/4} \tag{5}$$

where q_c is defined in Equation (2); Equation (5) becomes,

$$T_1 = \left[\frac{\alpha_1 A_f S + \alpha A_T \rho + \epsilon A_T \mu + Q_i - \dfrac{2\pi h K (T_1 - T_2)}{\ln r_2/r_1}}{\epsilon_1 A_f \delta + \epsilon_2 A_b \delta} \right]^{1/4} \tag{6}$$

Since T_1 is implicit in Equation (6), an iterative calculation process is necessary to determine the semiconductor switch/substrate temperature as a function of substrate area and power dissipation, as presented in Section 4, Environment Considerations.

Table A-1. Thermal Conductivities of Solar Array Materials

	watts/in. °K	joule/m-sec °K
Silver Expanded Metal	10.6	4.17×10^{2}
Silicon	3.2	1.26×10^{2}
Kapton	4×10^{-3}	1.57×10^{-1}
Coverglass	4×10^{-2}	1.57
Sylgard, SMRD Adhesive	8×10^{-3}	3.15×10^{-1}

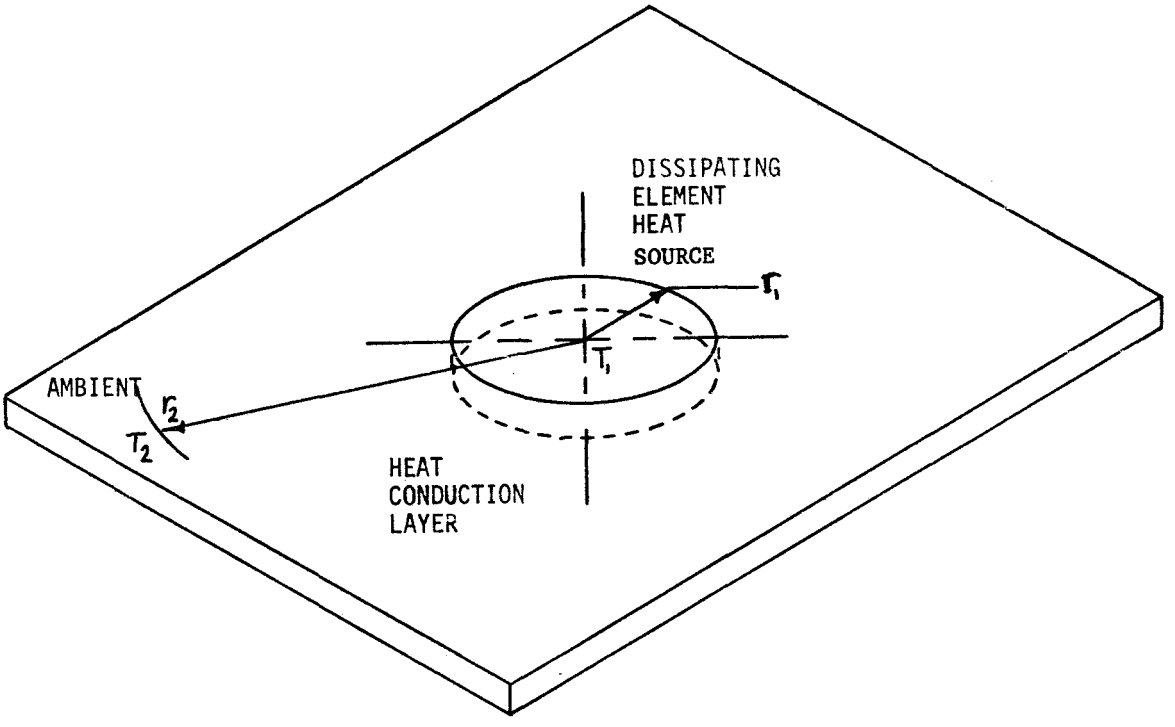


Figure A-1. Physical Model for Conduction Equation

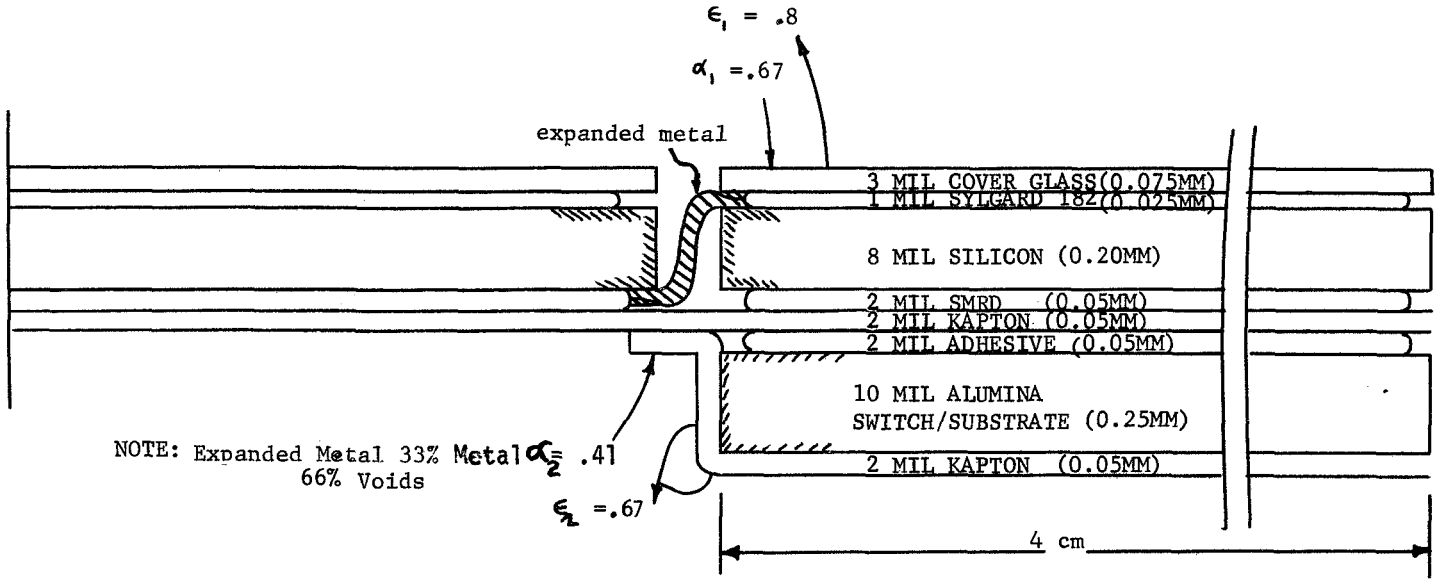


Figure A-2. Physical Layout of Solar Array (Typical)

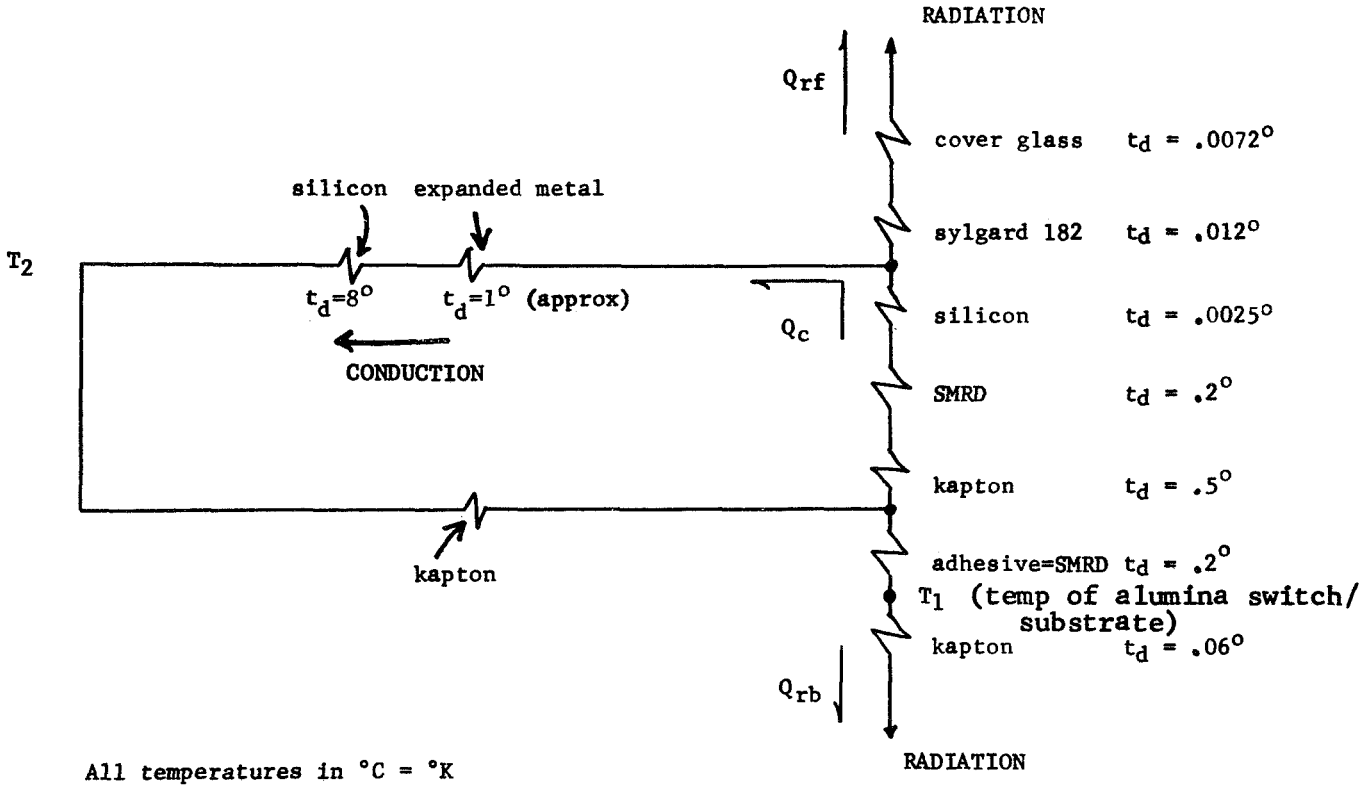


Figure A-3. Nodal Representation of Typical Solar Array Cross Section

APPENDIX B

EFFECT OF COVERGLASS AND BACKSHIELDING THICKNESS OF HVSA WEIGHT AND AREA

The purpose of this effort is to evaluate the effect on solar array blanket weight and area of a range of coverglass and backshielding thicknesses. The populations of the synchronous orbit trapped electrons and protons and the solar flare protons used in the equivalent 1-MeV electron flux determination are presented as a function of particle energy in Section 9.1, Radiation Environment and Effects Predictions.

The analytic effort described throughout this report is based on sizing the solar array to accommodate the charged particle degradation incurred with the use of the shielding provided by the reference GE rollout solar array, i.e., three mils of Microsheet coverglass and two mils of Kapton substrate plus about one and one-half mils of epoxy adhesive constituting the effect radiation backshielding for the solar cells. Additional radiation damage calculations were made for 1, 6, 12 and 18 mil coverglass thicknesses. Backshielding was assumed to be equivalent to the coverglass thickness on a gm/cm^2 basis for all the calculations.

Table B-1 presents the data resulting from the shielding thickness study, showing the damage-equivalent, normally-incident 1-MeV electron flux, the percentage of solar cell power remaining at five years in orbit, the relative solar cell module area needed to provide the same power, the relative solar array blanket (cells, coverglass, interconnections, Kapton substrate) weight on a unit area basis, and the total relative solar array blanket weight on a system level basis. The latter parameter is the product of the relative area and the relative unit weight factors. Figure B-1 presents graphically the relative area and relative total blanket weights as a function of coverglass shielding thickness.

This analysis has not attempted to define the weight of storage drum, boom and deployment mechanism associated with the various shielding thickness. These component weights are a function of blanket weight and require a specific design effort for a given blanket area and weight. The conclusion drawn from this analysis is that a lighter system weight is obtained with the use of thinner coverglass shields. It appears that one-mil thick coverglass is more advantageous than the three-mil glass used for this study, on a total weight basis. However, the solar cell module fabrication processes will be impacted by the requirement to handle very thin shielding, and must be carefully considered, along with environmental (thermal cycling) qualification, to determine optimum system cost effectiveness.

Table B-1. Solar Array Parameters for Various Coverglass Thicknesses

Coverglass Thickness (Mils)	1-MeV Flux ($e/cm^2/5yrs$)	Pwr Remaining at 5 years (Percent)	Relative SA Module Area	Relative Weight per Unit area	Relative Total SA Wt. (blanket)
1	9.4×10^{15}	54	1.09	.735	.80
3	5.3×10^{15}	59	1.0	1.0	1.0
6	1.36×10^{15}	71	.830	1.40	1.16
12	5.84×10^{14}	78	.755	2.20	1.66
18	3.06×10^{14}	83	.710	3.00	2.13

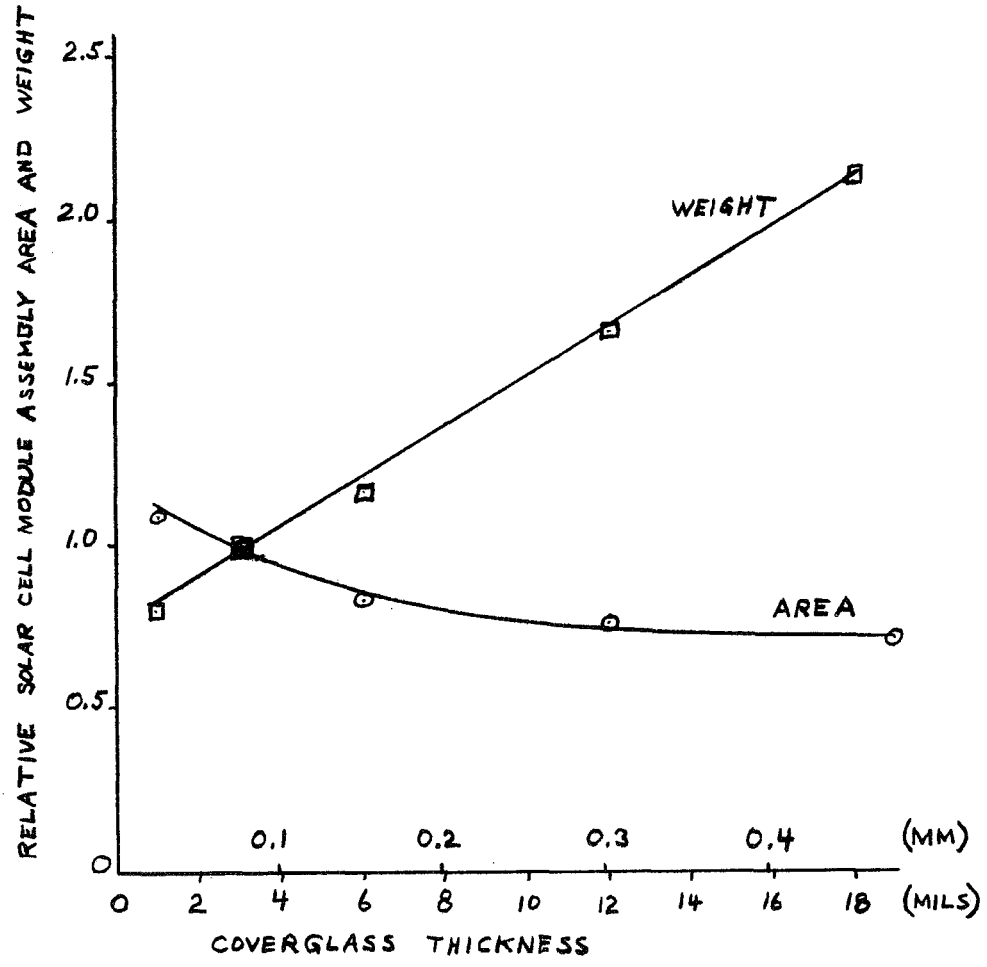


Figure B-1. Effect of Coverglass Thickness on Solar Array Module Area and Weight for a Fixed Power Output at Five Years in Synchronous Orbit

APPENDIX C

NEW TECHNOLOGY

This contract is subject to NASA requirements for New Technology reporting. One item is reported herein as New Technology; it is the technique of "High Voltage Solar Array Regulation by Means of a Binary-Coded Switching System with Controlled Voltage Regulation Switches." This system is described in Section 5.2.3, Techniques for Regulation by Discrete Switching.

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