THERMAL FEEDBACK IN Si JFETs OPERATING AT LOW TEMPERATURES

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ABSTRACT

Thermal feedback modifies the dc and ac characteristics of JFETs operating at temperatures where carrier freeze out occurs. Data for common source operation are analyzed using the thermal feedback theory of Mueller.

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Operation of JFET's (Junction Field Effect Transistors) at temperatures where carrier freeze-out occurs is well known [1], [2]. However, both the dc and ac characteristics are greatly modified by thermal feedback when the carrier concentrations become strongly temperature dependent (below 125°K for Silicon JFET's). This thermal feedback should be considered in the design of low temperature amplifiers. The thermal feedback theories of Burgess [3] and particularly Mueller [4] are directly applicable to JFET's. In bipolar transistors thermal feedback becomes significant only in an unusual voltage driven grounded base configuration [4], while in JFET's at low temperatures it is important in the usual common source configuration.

Causes of Thermal Feedback Effects

The drain current in a JFET operating with fixed bias is proportional to the carrier density in the conducting channel. In commercial devices the shallow donor or acceptor levels in the channel region begin deionizing at temperatures below 125°K thus reducing the carrier density (carrier "freeze-out"). Near 77°K the carrier density n(T) as a function of temperature T is approximately

$$n(T) \propto \exp\left(-q\, E_{cd}/2kT\right) . \tag{1}$$

Here E_{cd} is the energy difference between the conduction band and the donor level (for an n-channel device) and $q\, E_{cd} \gg kT$. The strong temperature dependence of n(T) is primarily responsible for the large positive temperature coefficient of the drain current. The mobility and built-in voltage change relatively slowly with temperature and need not be included in the model.

The active region of the JFET is thermally coupled to the ambient by a frequency dependent thermal impedance $Z_t(\omega)$ where ω is the angular frequency. The power dissipation $P(\omega)$ due to a signal of frequency ω results in a temperature change $T(\omega)$ in the active region given by $T(\omega) = Z_t(\omega) \cdot P(\omega)$. The thermal impedance decreases at high frequencies since the device temperature can not follow high frequency power dissipation variations. The dc thermal resistance $R_t = Z_t(0)$ was determined experimentally by measuring the increase of internal device temperature for various dissipation levels. A measurement of the zero-bias channel conductance g_{ds} during a 10μs "off" pulse was used to determine the internal temperature under operating bias conditions by comparing this g_{ds} to a curve of equilibrium g_{ds} versus temperature. From a plot of the internal temperature as a function of the power dissipation, R_t was found to be typically 150-960°K/watt depending upon the device type and the ambient temperature.

Effect on dc Characteristics

Most models for the dc characteristics assume a constant device temperature and thus a constant carrier density in the conducting channel region. To include the thermal effects due to the dependence of $n(T)$ on the device dissipation, the temperature T is taken as $T = T_A + V_{DS}I_DR_t$ where T_A is the ambient temperature and V_{DS} and I_D are the dc drain-source voltage and current respectively. When (1) is valid the drain current may be written in the form

$$I_D \simeq I_{DN} \exp\left[\frac{E_{cd}}{2kT_A}\left(\frac{1}{\frac{T_A}{V_{DS}I_DR_t} + 1}\right)\right] \tag{2}$$

where I_{DN} is the drain current obtained neglecting heating effects. In Fig. 1 measurements at T_A = 77°K are compared with calculations from (2). The drain current without heating I_{DN} is measured using short pulses. Agreement is very good except at high dissipation levels where the high internal temperature makes (1) invalid.

Effect on ac Parameters

Using the expressions developed by Mueller the y-parameters with thermal feedback $\bar{y}_{21}$ and $\bar{y}_{22}$ are related to the constant temperature y-parameters y_{21} and y_{22} by

$$\bar{y}_{21} = \frac{y_{21}}{1 - D_D I_D V_{DS} Z_t(\omega)} \tag{3}$$

$$\bar{y}_{22} = \frac{y_{22} + I_D^2 D_D Z_t(\omega)}{1 - D_D I_D V_{DS} Z_t(\omega)} \tag{4}$$

where $D_D = \frac{1}{I_D} \frac{\partial I_D}{\partial T}$. The other JFET y-parameters y_{11} and y_{12} are not significantly affected by thermal feedback. The voltage gain $\bar{A}_v(\omega)$ for a common source stage becomes

$$\bar{A}_v(\omega) = \frac{y_{21}}{y_{22} + R_D^{-1} + D_D I_D^2 Z_t(\omega)[1 - V_{DS}(I_D R_D)^{-1}]} \tag{5}$$

where R_D is the drain load resistor.

Experimental results for $\bar{y}_{21}$ and $\bar{y}_{22}$ of two electrically similar devices having widely different thermal resistances are shown in Fig. 2. The device with the lower thermal resistance has a much smaller variation of $\bar{y}_{22}$.

The voltage gain for a common source JFET stage is shown in Figure 3 for three values of drain load resistor R_D. The dc voltages and currents are identical for each case but the different frequency responses observed represent different thermal feedback conditions. A nearly frequency independent $\overline{A}_v$ is obtained at a sacrifice in voltage gain when the drain resistor load line is tangent to the curve of constant dissipation at the operating point.

To avoid thermal feedback at low temperatures, devices must be selected having low thermal resistances and must be operated at low bias levels. Alternatively, devices can be operated at higher ambient temperatures so carrier freeze-out is not present.

REFERENCES

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3. R. E. Burgess, "The a.c. admittance of temperature-dependent circuit elements," Proc. Phys. Soc. (London), Vol. 68B, pp. 766-774, 1955.

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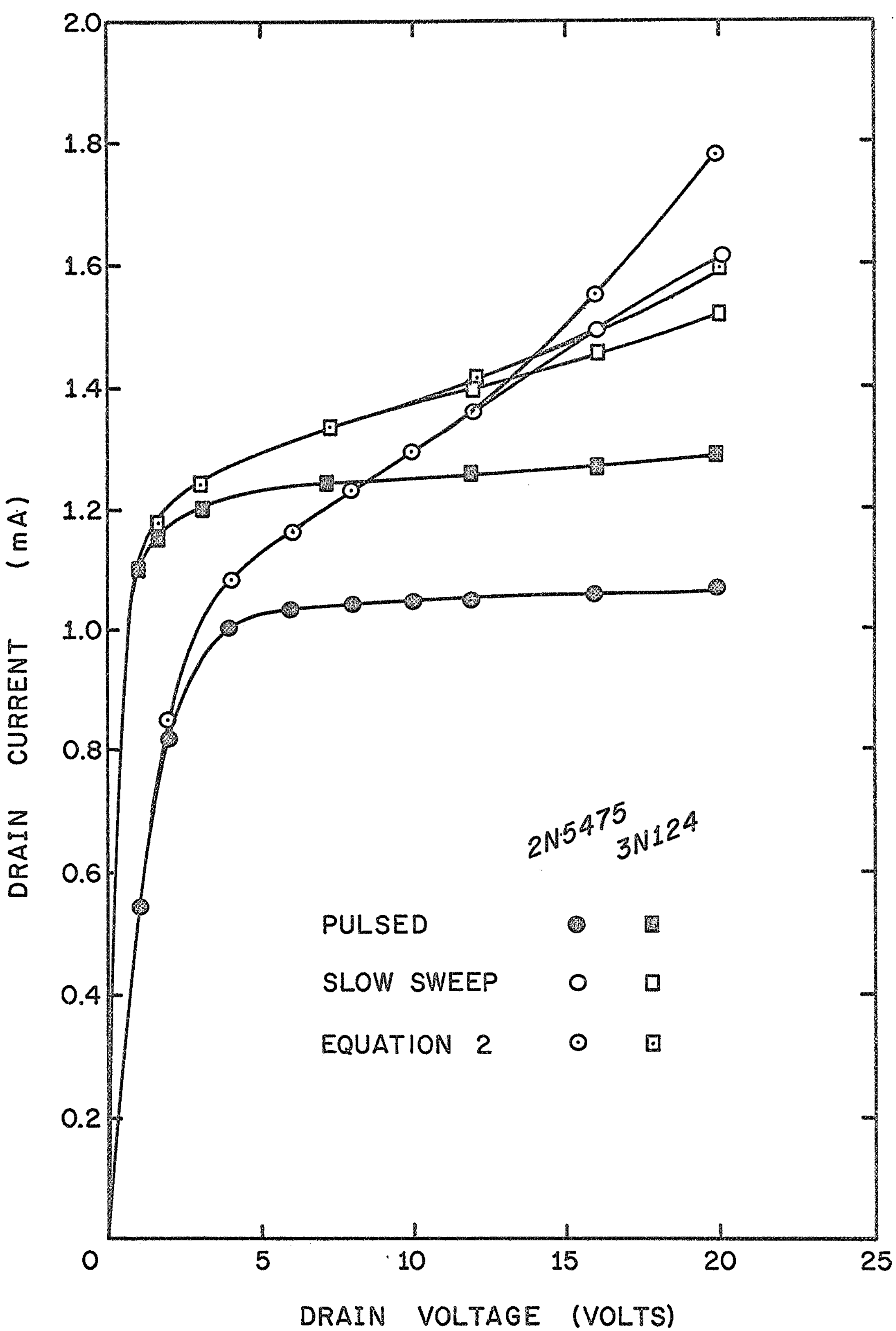
FIGURE CAPTIONS

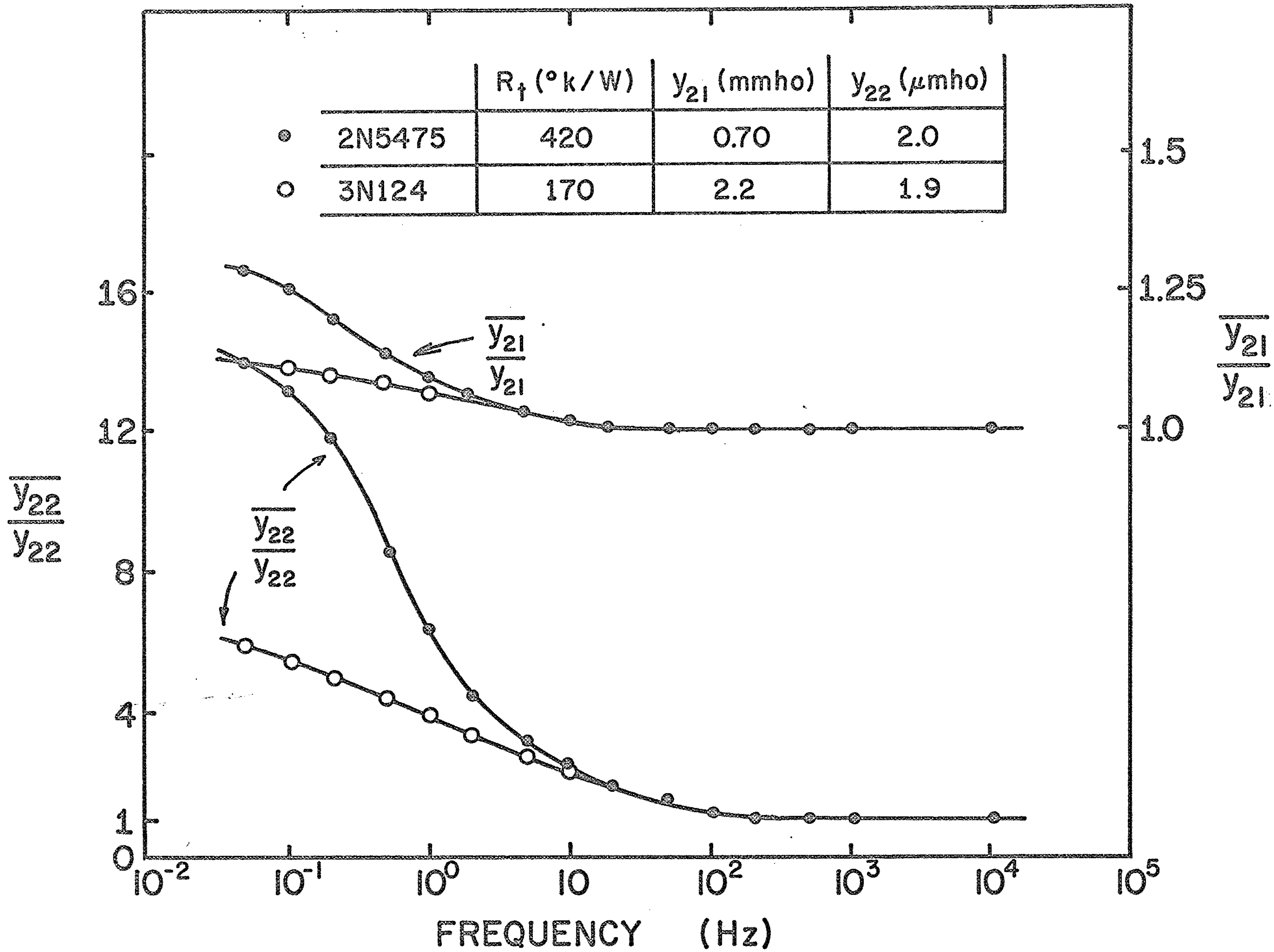
Figure 1: Current-voltage characteristics for JFETs with different thermal resistances. R_t = 420°K/W for 2N5475, R_t = 170°K/W for 3N124. T_A = 77°K, V_{GS} = 0.

Figure 2: Frequency dependence of normalized $\overline{y}_{21}$ and $\overline{y}_{22}$ for JFETs with different thermal resistances. Bias V_{GS} = 0, V_{DS} = 20 volts, $I_D \simeq$ 1.6mA. T_A = 77°K.

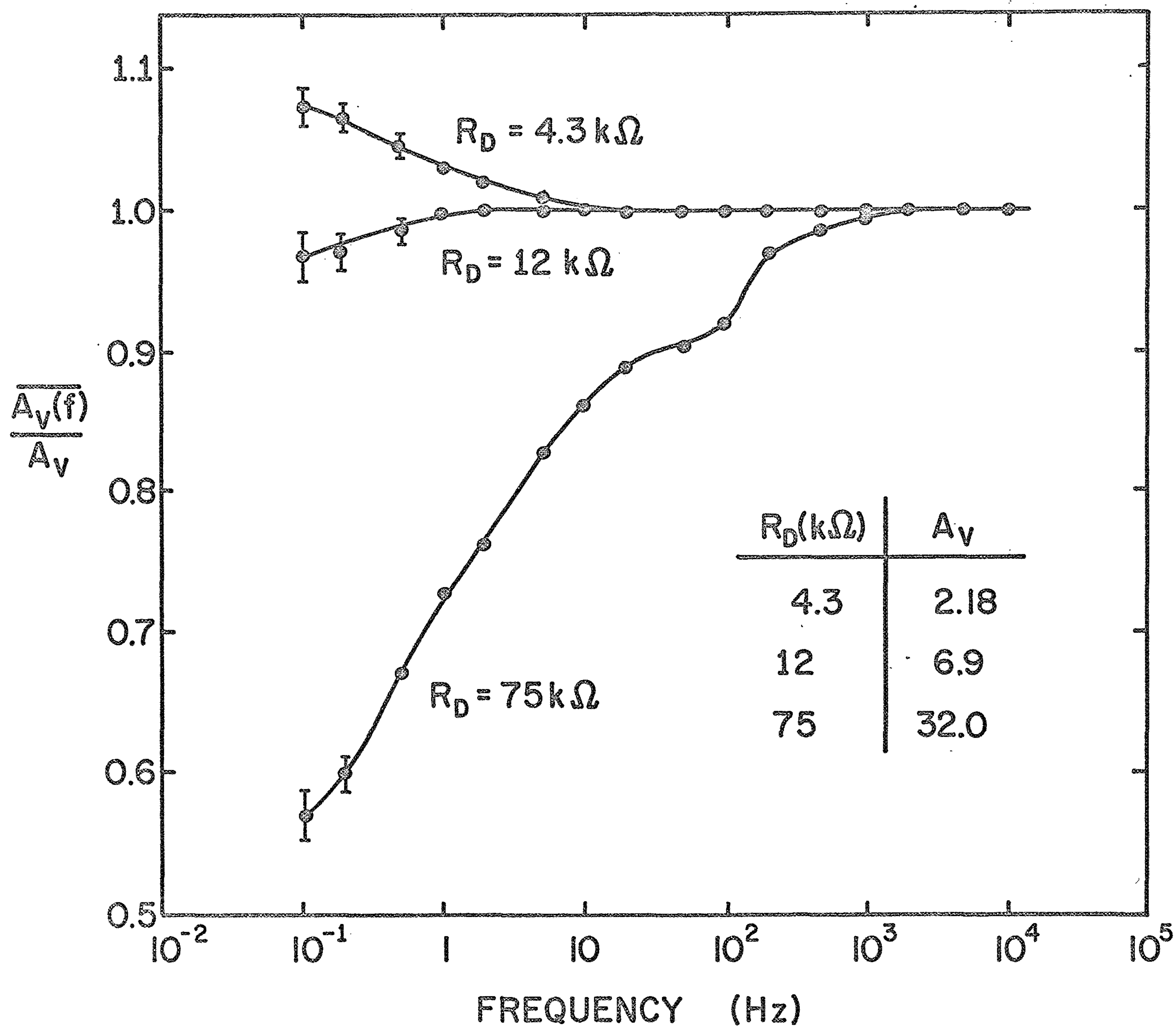
Figure 3: Ratio of frequency dependent common source voltage gain $\overline{A}_v$ (f) to its high frequency value A_v for various drain load resistors R_D. Device 2N5475: V_{GS} = 0, V_{DS} = 20 volts, I_D = 0.9 mA, T_A = 77°K.



2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0
5
10
15
20
25
DRAIN CURRENT (mA)
DRAIN VOLTAGE (VOLTS)
2N5475
3N124
PULSED
SLOW SWEEP
EQUATION 2



R_t (°k/W)
y21 (mmho)
y22 (μmho)
2N5475 420 0.70 2.0
3N124 170 2.2 1.9
16
12
8
4
1
0
1.5
1.25
1.0
y21 / y21
y22 / y22
10^-2 10^-1 10^0 10 10^2 10^3 10^4 10^5
FREQUENCY (Hz)



$R_D = 4.3\,k\Omega$
$R_D = 12\,k\Omega$
$R_D = 75\,k\Omega$
$R_D(k\Omega)$ | A_V
4.3 | 2.18
12 | 6.9
75 | 32.0
$\overline{A_V(f)} / \overline{A_V}$
1.1
1.0
0.9
0.8
0.7
0.6
0.5
10^{-2} 10^{-1} 1 10 10^2 10^3 10^4 10^5
FREQUENCY (Hz)