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Engineering College
Department of Electrical Engineering
Computer Science Research Laboratory

(in print)

CSRL Memo No. 208

A Solid-state Crossbar Switch for Automatic Analog-computer Patching

by

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Abstract

An all-electronic crossbar switch consisting of FET series-shunt switches inside the feedback loops of monolithic operational amplifiers was designed and constructed.

As the application, time-shared solution of five different differential equations was obtained by using four integrators on ASTRAC II, with a new solution being generated 250 times per second.

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NGR-03-002-024

Introduction

Among current problems relating to analog and hybrid computers, one of the most interesting is that of automatic analog-computer patching, which will replace the conventional analog patch board. A set of 20 to 50 relatively small (4 X 4 to 6 X 8) crossbar switches, which change the connections of analog s' ap would permit not only the automatic patching or storage of analog programs, but also the time sharing of analog computers.[5] From the viewpoint of hardware, low-cost integrated circuit switches and operational amplifiers will provide the means of constructing such a crossbar switch.

This paper describes the design and construction of a 4 X 4 crossbar switch and its application to analog patching. The crossbar switch consisting of monolithic operational amplifiers employs series-shunt switches inside feedback loops of operational amplifiers; therefore high accuracy is e.sured. Each crossbar matri› consists of four multiplexers, which can change the connections of analog computing elements. The solutions of five differential equations are obtained by using four integrators. This scheme was successfully tried on ASTRAC II, a very fast iterative analog computer.

The Design of the, Analog-patching Crossbar Switch

Configuration Selection of the Multiplexer

There are various methods of multiplexing analog signals. One method is to switch analog signals by switches placed in the input computing resistors of an operational amplifier as in Fig. 1 (a). The disadvantage of this method lies in the fact that the ON resistance of the switch causes computing errors. Adjustment of network resistances will improve the accuracy, but this is cumbersome and expensive.

If the operational amplifier is used as a voltage-follower as in Fig. 1 (b), the ON resistance of the switch tends to be negligible compared to the very high-input follower impedance. However, no more than one switch must be ON at any one time.

A better method is to place the switches in the feedback loop of the operational amplifier to eliminate the effect of the ON resistance. (Fig. 1 (c)). It has the advantage that the number of operational amplifiers required is one and more than one switch is allowed to close at a time.

Considering these points, the last method was adopted for an analog-patching multiplexer. For this purpose, the 4 X 4 matrix switch shown in Fig. 2 was designed and tested.

Analog Switch

Although this multiplexer does not require switches

with low ON resistance, it does require low offset-voltage. Therefore FET series-shunt switches (Fig. 3) are desirable. When the FET is OFF, and the transistor is ON, the collector voltage of the transistor is small (less than 50 mV), so this shunt transistor makes analog signal current flow to ground and the switched node is disconnected to the summing junction. When the FET is ON and the transistor is OFF, the node is connected to the summing junction. The gate leakage current of the ON FET is not the problem, because the gate to source voltage of JFET is kept at 0 V by a resistor (Fig. 3). The OFF shunt transistor produces leakage current which flows into the summing junction, but this effect is within 0.1% of half scale, if a silicon transistor is used and proper value of computing resistors of the operational amplifier is selected.

N channel junction FET 2N5555 and PNP silicon transistor 2N3703 were selected for the reason of availability and low cost. The ON resistance of the FET (0V gate voltage) is about 140 ohms, and the leakage current of the OFF transistor is specified to be less than 100nA and the resistance of the ON transistor is less than 20 ohms. In order to ensure the operation of this series-shunt switch, a driving signal swing between -9 volts and 3 volts is required.

Switch Driver

For use with our particular analog computer, the switch

driver is designed to convert the 0 to -6 volts logic level on the ASTRAC II digital patch bay to the -9 volts to +3 volts levels. Among various kinds of circuits available, monolithic operational amplifier MC 1709 (±10 V output voltage swing) was selected (in Fig. 4), because it costs less than commercially available FET drivers, and save construction; a sufficiently large output swing is easily obtained, and especially fast switching is not required for automatic patching, which always takes place between analog-computer runs.

The amplifier is equalized so that the maximum frequency for rated output is more than 35 KHz and the amplifier is stable.

Output Operational Amplifier

As for the output operational amplifier, the monolithic operational amplifier MC 1433 (±10 V output voltage swing) was selected for simplicity of circuit construction and low cost. For higher accuracy, a chopper-stabilized discrete circuit would be substituted. The circuit diagram is as in Fig. 5. The diodes at the input terminal protect the operational amplifier if the summing-junction voltage should rise because of a damaged switch. All computing resistors are selected to be 27 KΩ.

Because of stray capacitances associated with the

switching circuit, the operational amplifier had to be equalized for stability so that the maximum frequency for rated output is about 35 KHz, and the noise is within 0.05% of half scale.

Construction and Results

The 4 X 4 crossbar circuit and switch drivers were constructed on an 8.5 in. X 17 in. perf board sheet. The most serious problem is that of crosstalk which affects the accuracy of the multiplexer. In the construction of the circuit, attention is paid to good short ground connections.

The crosstalk characteristics are shown in Fig. 6. The curve (a) shows the case where the input sine wave signal (20 V_{pp}) is applied to one of the OFF state analog inputs, and curve (b), (c) shows the case of two and three of the OFF state analog inputs respectively. It is also shown that the circuit will work with two switches ON and the crosstalk becomes smaller because the feedback resistance is the half (13.5 KΩ); this connection could be used to compute one-half the sum of two inputs, if desired.

The Application of the Crossbar Switch

Statement of Problem

By using this multiplexer, we can change the connections of analog computing elements in a short time. In a

large automatic patching system several crossbar switches would be used as "telephone exchanges". Here, as a demonstration of the operation of the multiplexer, the iterative patching of five setups is tried on ASTRAC II. The problem is to generate five solutions of five different differential equations at a rate of 250 per second for each problem. These problems are:

(1) First order differential equation, $\dot{x} + a_1 x = 0$

(2) Harmonic oscillation, $\ddot{x} + a_2 x = 0$

(3) Damped harmonic oscillation, $\ddot{x} + a_3 \dot{x} + b_3 = 0$

(4) Mathieu's equation, $\ddot{x} + a_4(1-\cos \omega_m t)x = 0$

(5) Vandder Pol's equation, $\ddot{x} + a_5(x^2-1)\dot{x} + x = 0$

The 4 X 4 matrix switch (Fig. 2) is not sufficient to connect each computing element independently. Therefore some fixed connections and tricks must be employed to overcome this restriction.

Method of Solution

Analog Computer Setup. In general, one would change coefficient (digital attenuator settings as well as patching connections for each problem in order to set the proper value of time scale, amplitude scale and initial conditions. For simplicity, however, settings of potentiometers are kept constant for each problem, so time scale and amplitude scale must be compromised.

The setup diagram is shown in Fig. 7. Each switch is denoted as A1, A2, B1, B2 etc. The number near the switches [(1), (2), ...] shows that each switch closes only at the computing time corresponding to the problem [(1), (2) ...] and opens at other computing time.

Each problem setup is shown in Fig. 8, where the shaded amplifiers A, B, C, D are the output amplifiers of the cross-bar switch. As the output to CRT is taken from the output of integrator #2, the solution shown for problem (1) (first-order differential equation) is the integral of X (Fig. 8(a)). As described earlier, it is allowed that two switches of a multiplexer become ON at a time, but the gain of the multiplexer is 1/2 (Fig. 8). Initial conditions for linear differential equations are large, but those for nonlinear equations are small. A constant initial-condition voltage is added with a summer in the case of linear equations.

Control Signals for Multiplexer Switches

In order to set up five differential equations successively, each multiplexer switch must be furnished with a proper control signal. Referring to Fig. 7, these control signals become those in Fig. 9 (ON and OFF levels, -6v 0 V). The transition of the signals must take place at the end of the COMPUTE period of ASTRAC II.

There are two methods for generating such pattern signals.

One is to use ASTRAC II logic elements; the alternative is to use the digital computer (PDP-9).

Pattern Generation by ASTRAC II Logic Elements

Shift registers on ASTRAC II are available to compose a five-bit ring counter. It operates at the ASTRAC II reset rate (in this case 250 Hz) and produces a periodic pulse sequence whose period is 5 times of the compute/reset period of ASTRAC II (20 ms). By combining the shift-register outputs properly, the pattern signals of Fig. 9 are obtained (Fig. 10).

When ASTRAC II is in INITIAL RESET mode, the multiplexer switches produce the connection corresponding to problem (1) with the aid of the INITIAL RESET level obtained on the ASTRAC II digital patch bay.

Pattern Generation by PDP-9

In this case, ASTRAC II is placed in SINGLE RUN mode, and control registers on the linkage patch bay are loaded from the PDP-9 accumulator, which contains the number corresponding to one of the problem connections. After that, one of the free IOT pulses on the LPB initiates SINGLE RUN.

Fig. 11 shows the necessary patch connections on digital and linkage patch bays. Because there are only eight trunk lines from LPB to DPB, some free logic on DPB is needed. (The signals on LPB (0,-3 V logic) can be used,

however, it is noisy).

Seven control signals (A1, A2, A3, B1, B2, B4, C1) out of twelve redundant signals (Fig. 9) correspond to the bits of AC11 through AC17. Because the inverter is in the trunk line (LPB to DPB), the number for each problem's connection is as follows.

Problem (1)	0110111	(67)
Problem (2)	1011001	(131)
Problem (3)	1010011	(123)
Problem (4)	1101101	(155)
Problem (5)	1101010	(152)

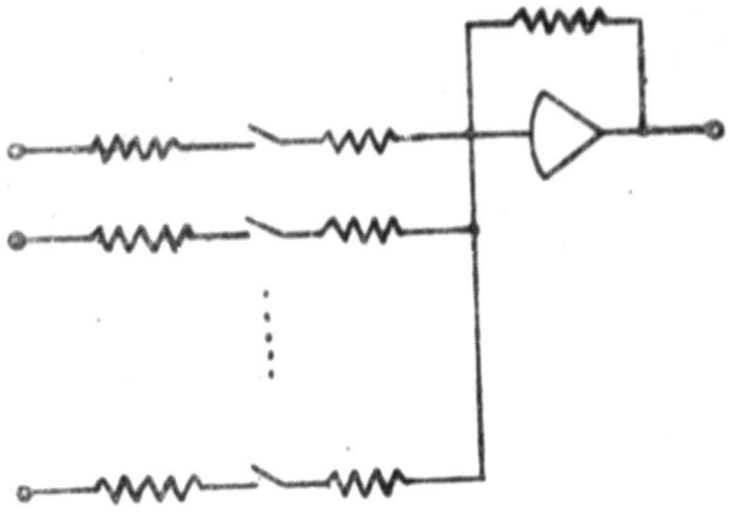
The PDP-9 program is listed in Table 1. When ASTRAC II is in the RESET mode, the program is waiting at CLOCK FLAG TEST and the crossbar-switch power is on. The program starts when the compute push button on ASTRAC II is depressed.

Results

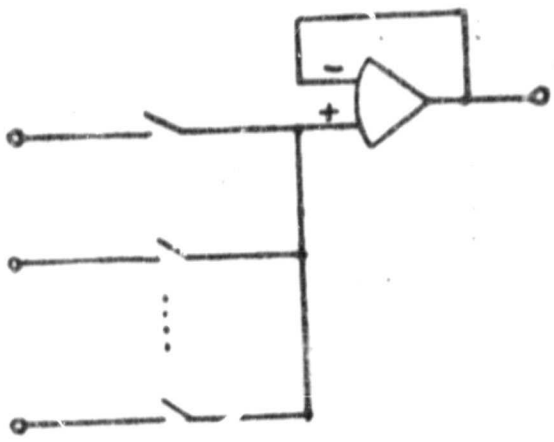
Fig. 2(a) shows the five kinds of waveforms and one of the control signals (B1). The expanded waveforms are in Fig. 12 (b) - (d).

The number of computing elements of ASTRAC II is as follows.

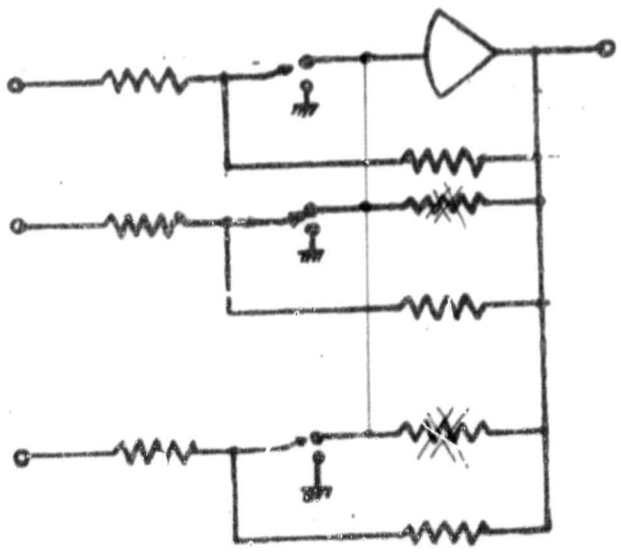
Integrator	; 4	(2 for function generation)
Summer	; 14	(6 for multipliers)
Multiplier	; 3	
Potentiometer	; 11	



(a)



(b)



(c)

Figure 1. Multiplexer Configuration

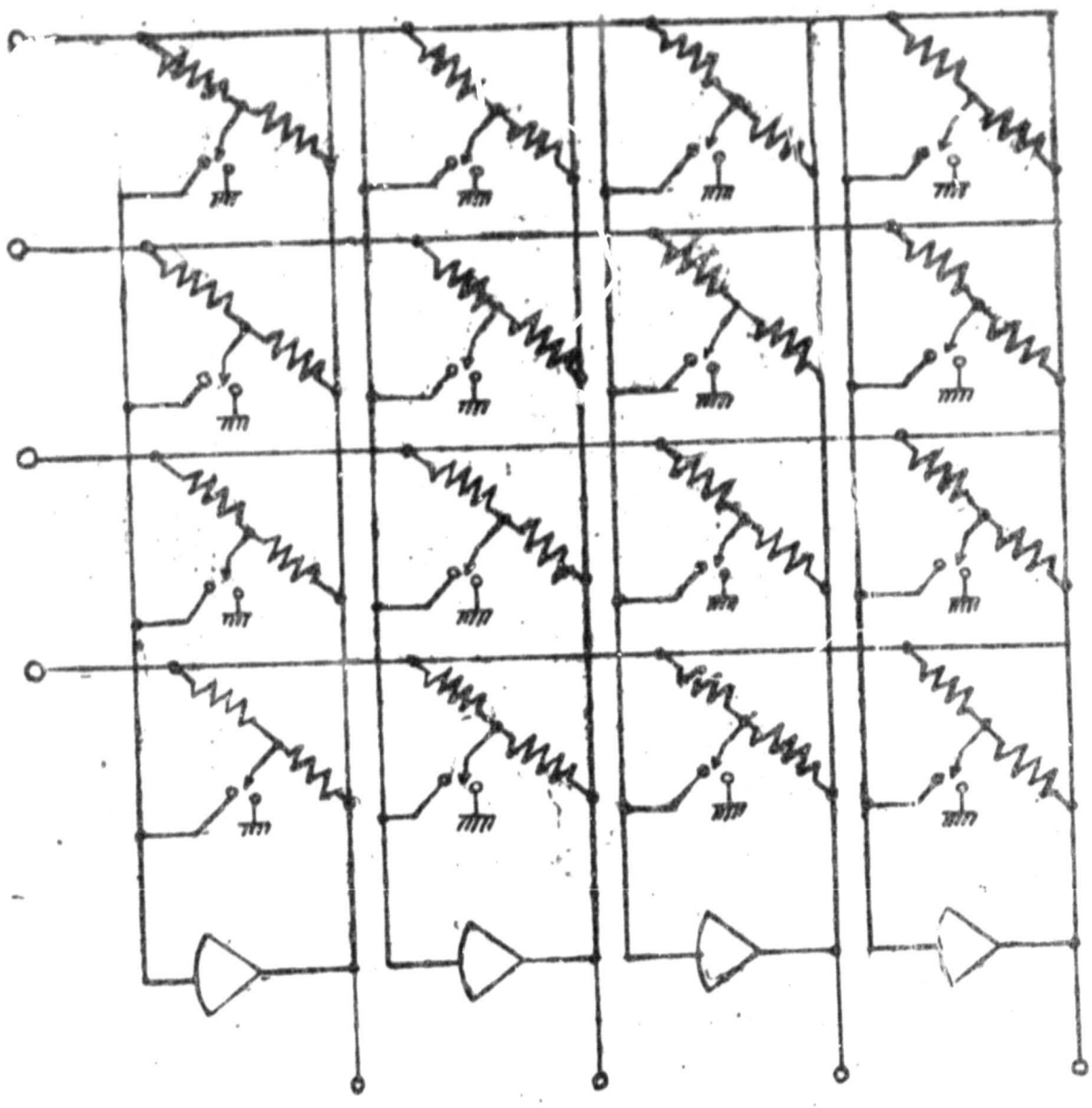


Figure 2. 4 x 4 Matrix + Multiplexer

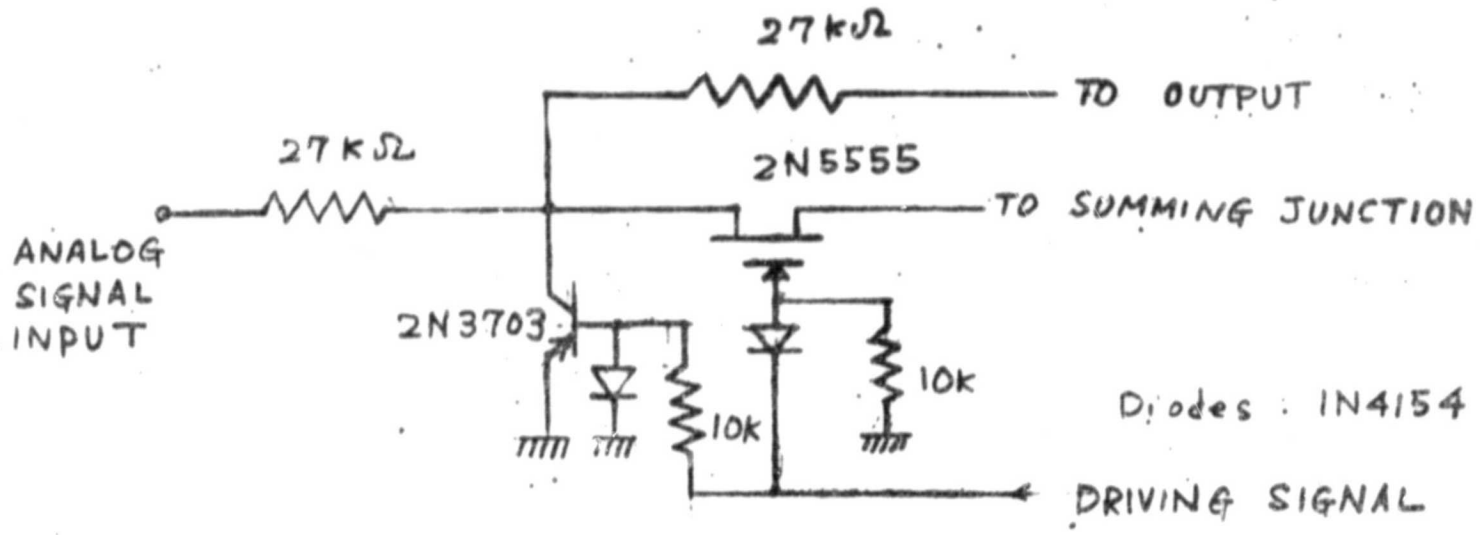


Figure 3. FET Series-Shunt Switch

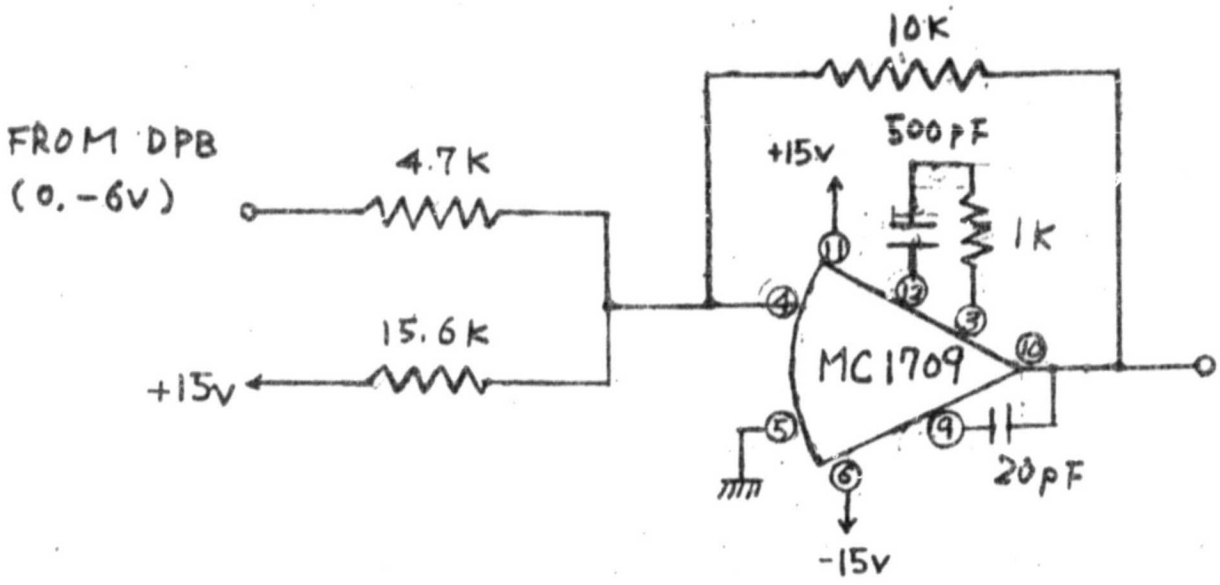


Figure 4. Schematic Diagram of Switch Driver

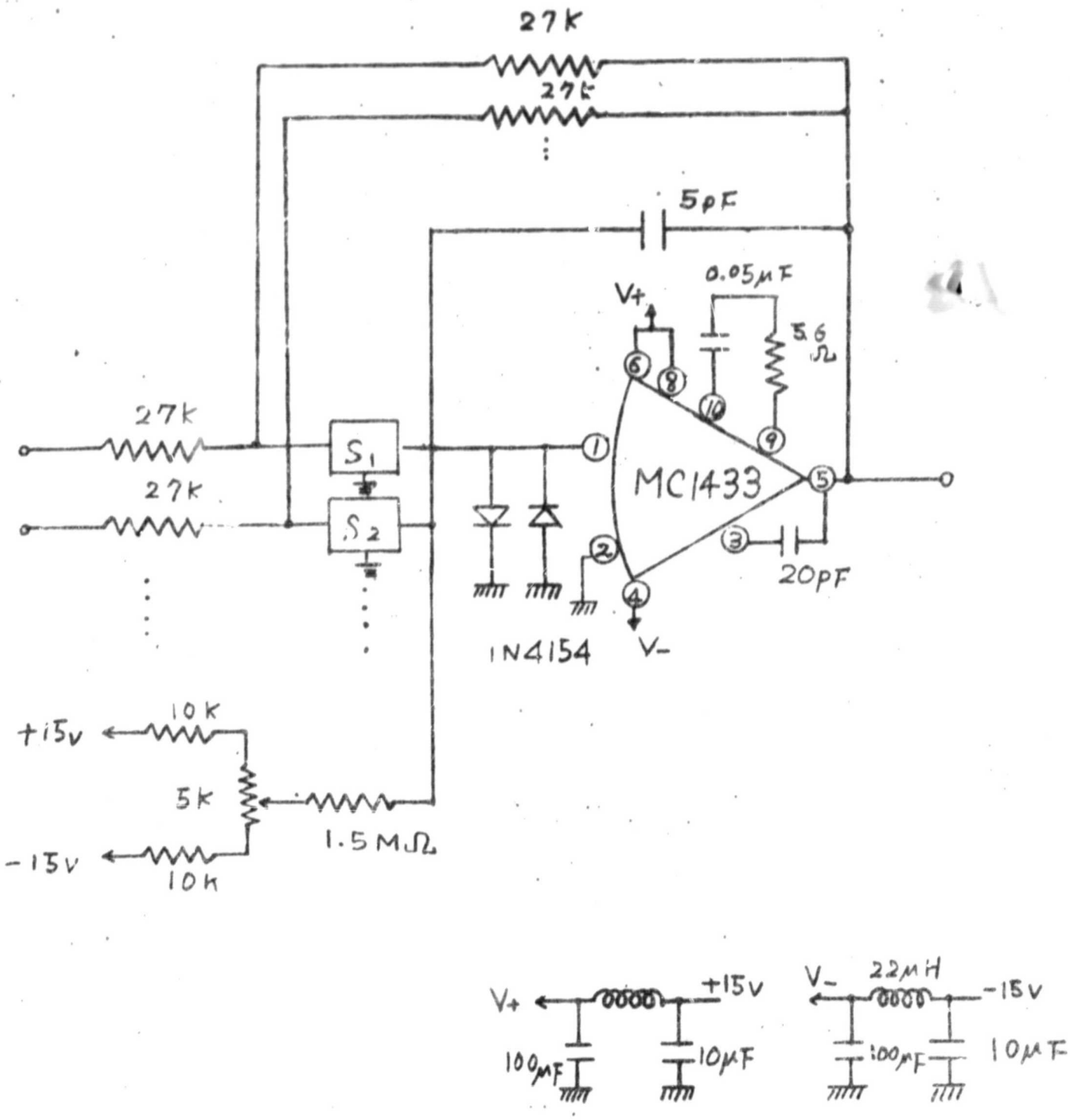


Figure 5. Schematic Diagram of Output Operational Amplifier

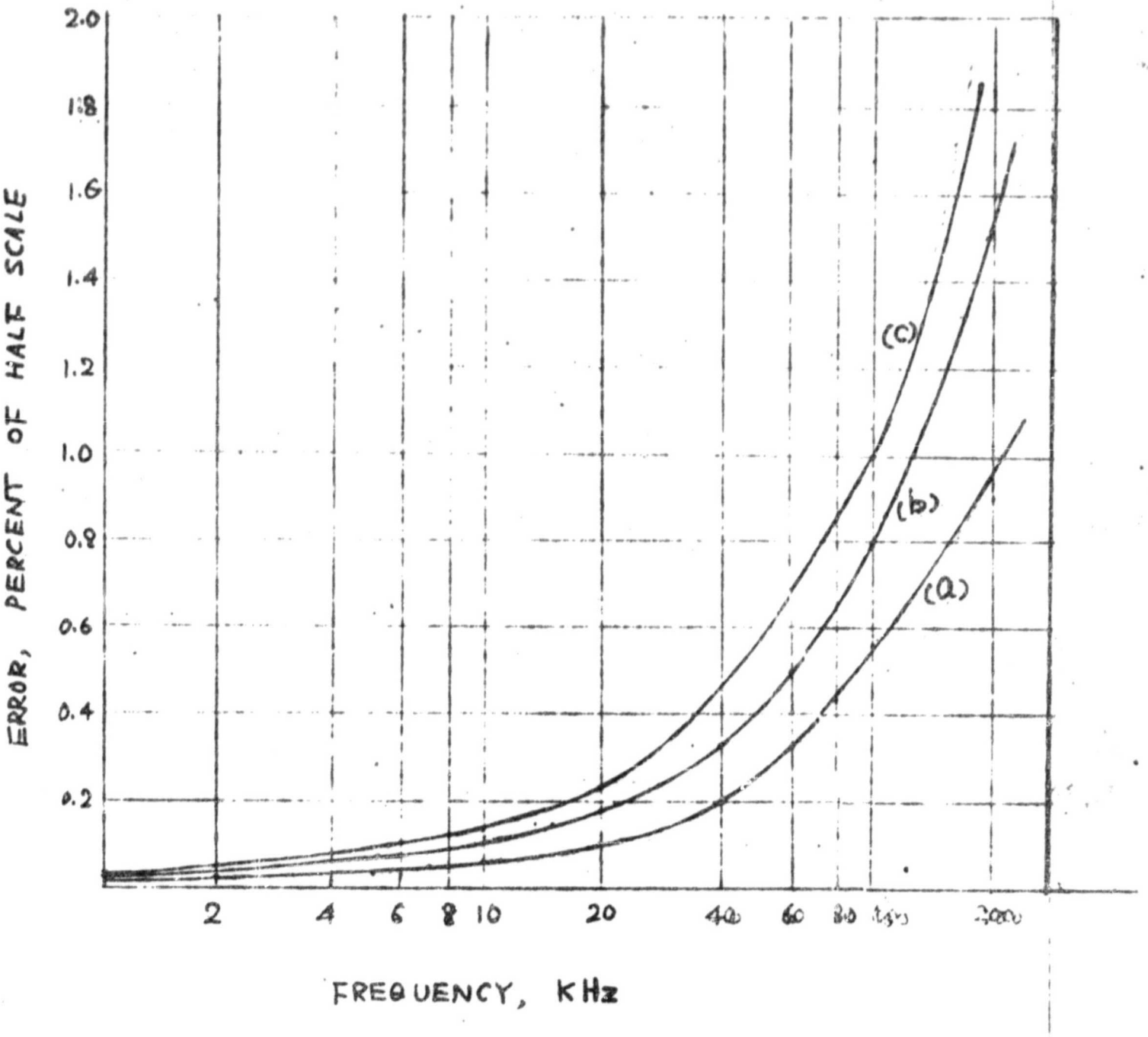


Figure 6. Crosstalk Characteristics of the Multiplexer

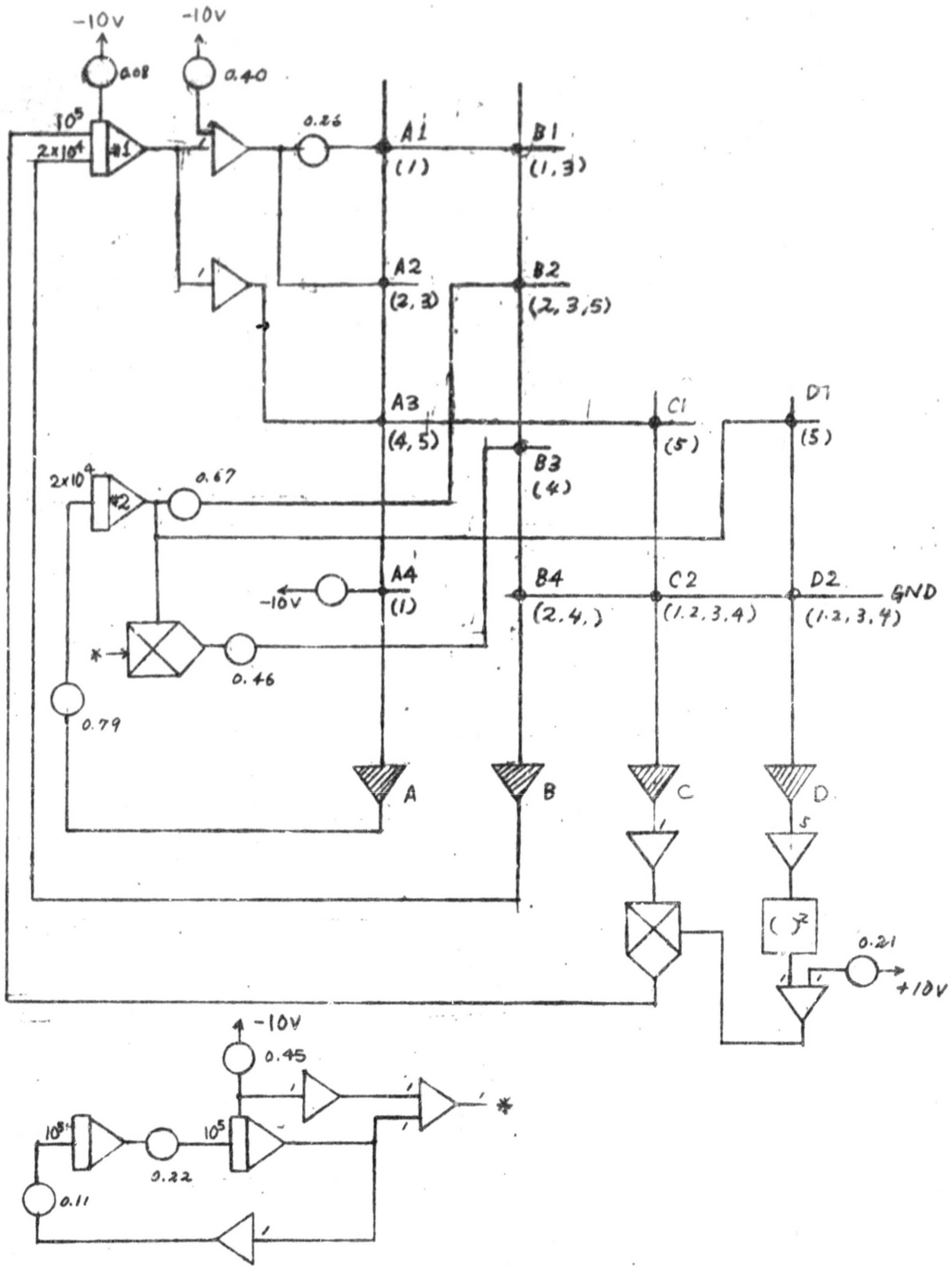
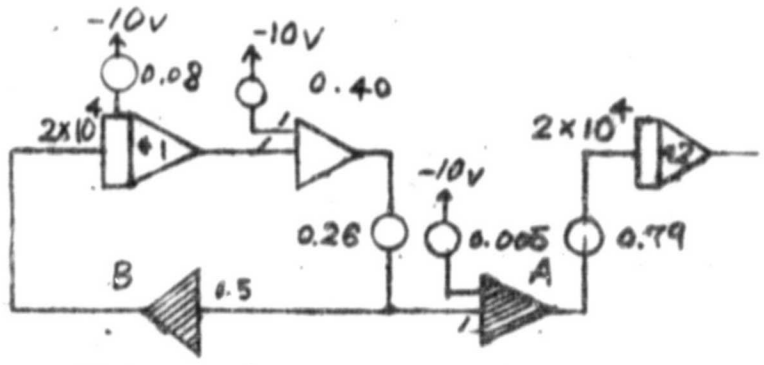
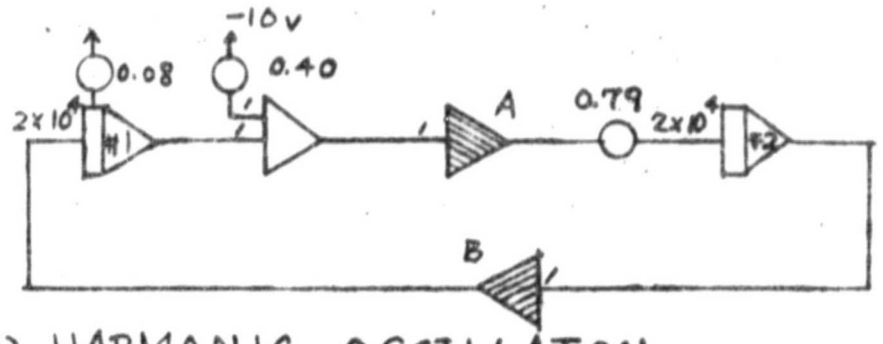


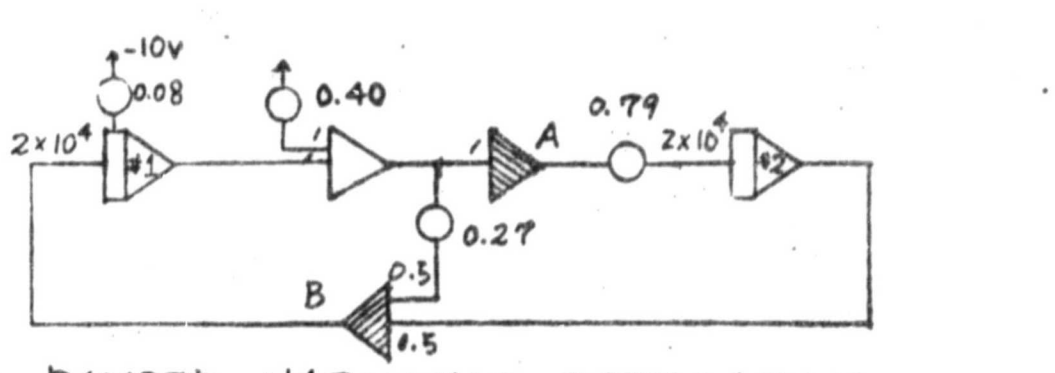
Figure 7. Setup Diagram of Five Differential Equations



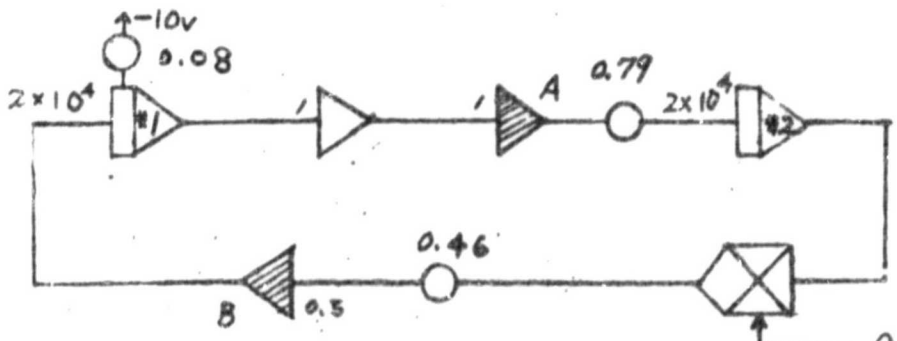
(1) FIRST ORDER DIFFENTIAL EQUATION



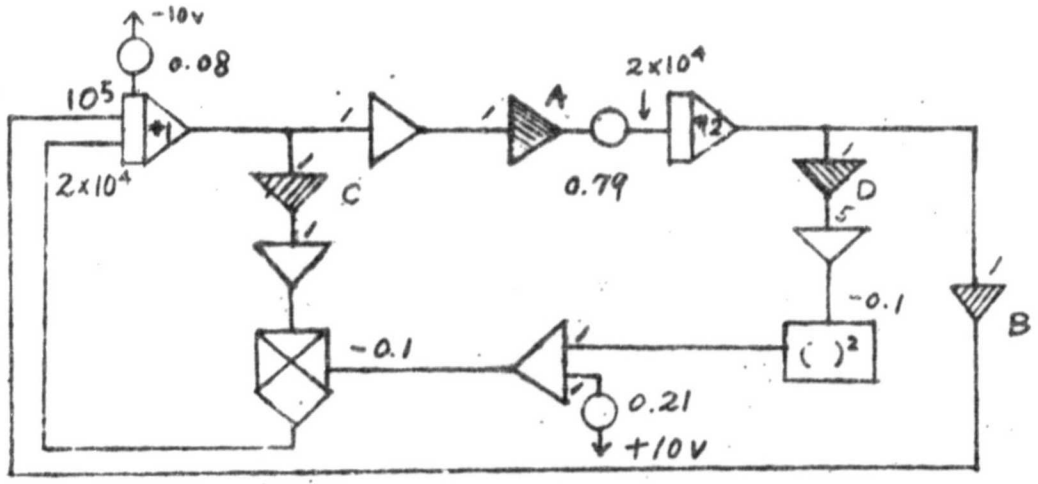
(2) HARMONIC OSCILLATON



(3) DAMPED-HARMONIC OSCILLATION



(4) MATHIEU'S EQUATION



(5) VAN DER POL'S EQUATION

Figure 8. Setup Diagrams of Each Equation

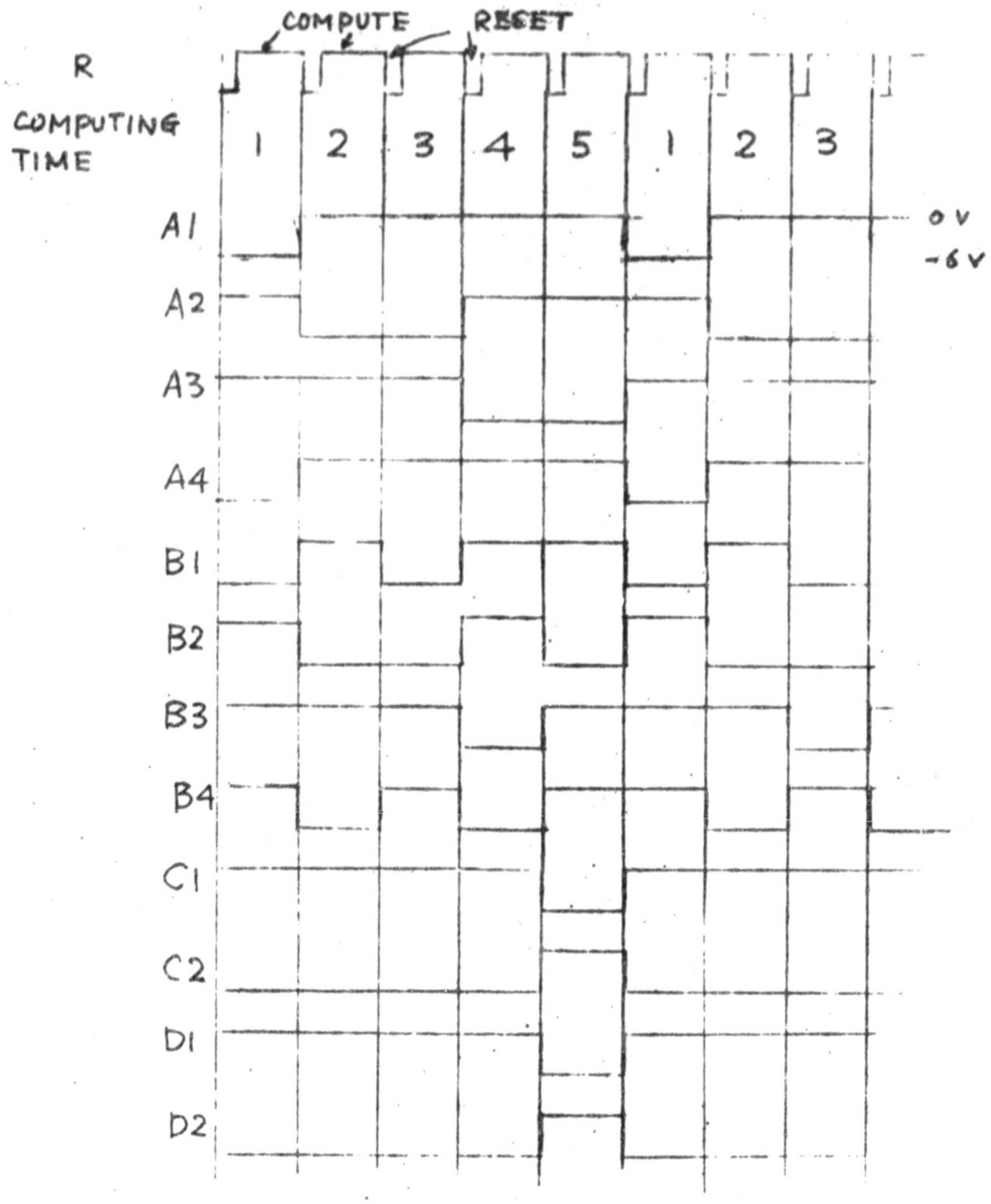


Figure 9. Control Signals to Multiplexer Switches

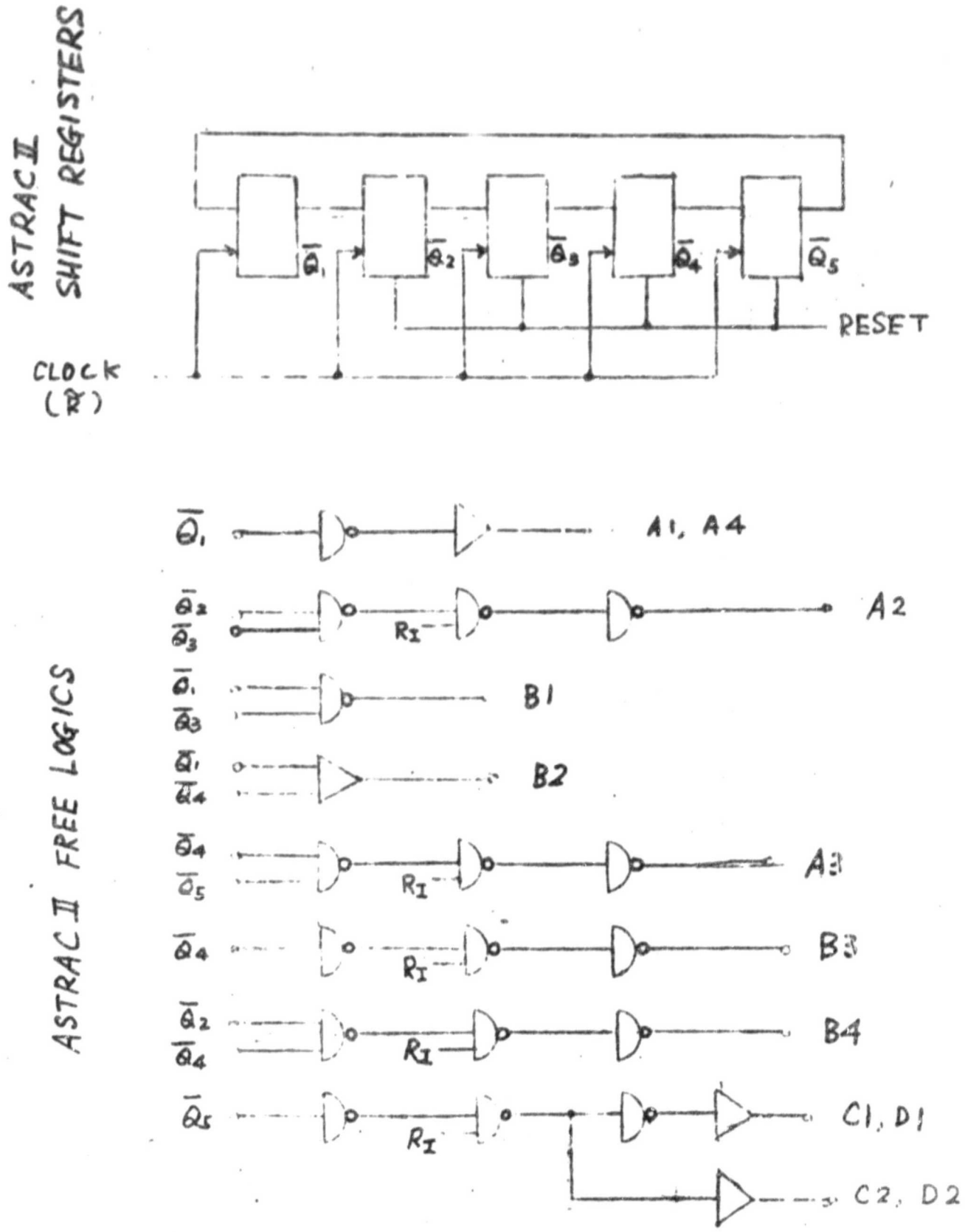


Figure 10. Pattern Generation by Shift Registers and Free Logics

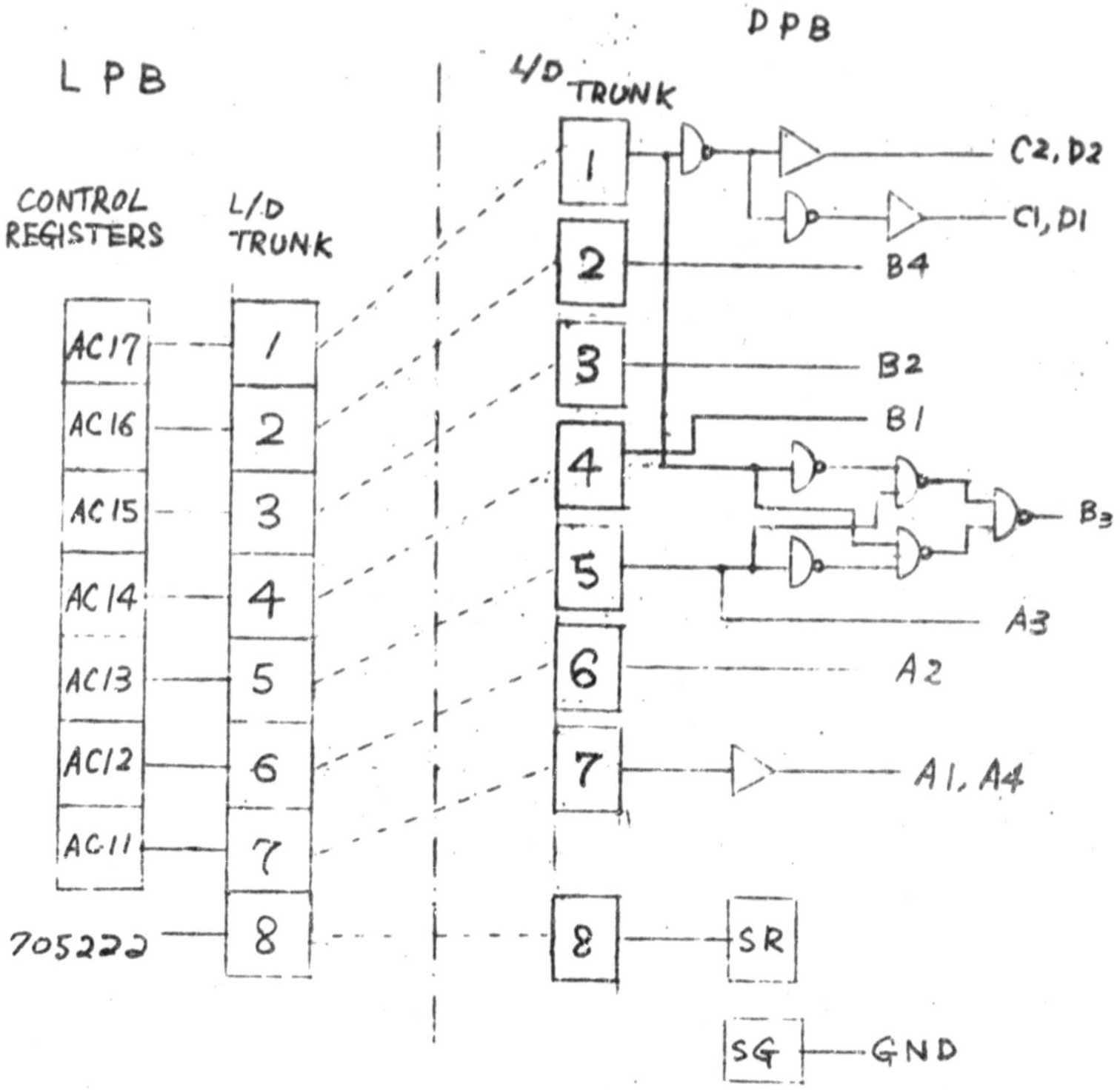
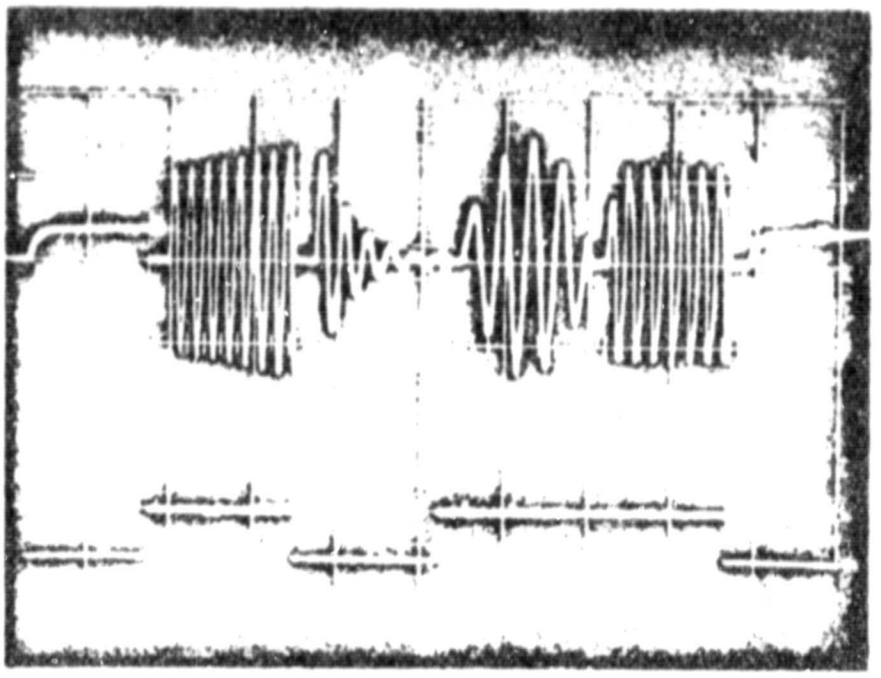


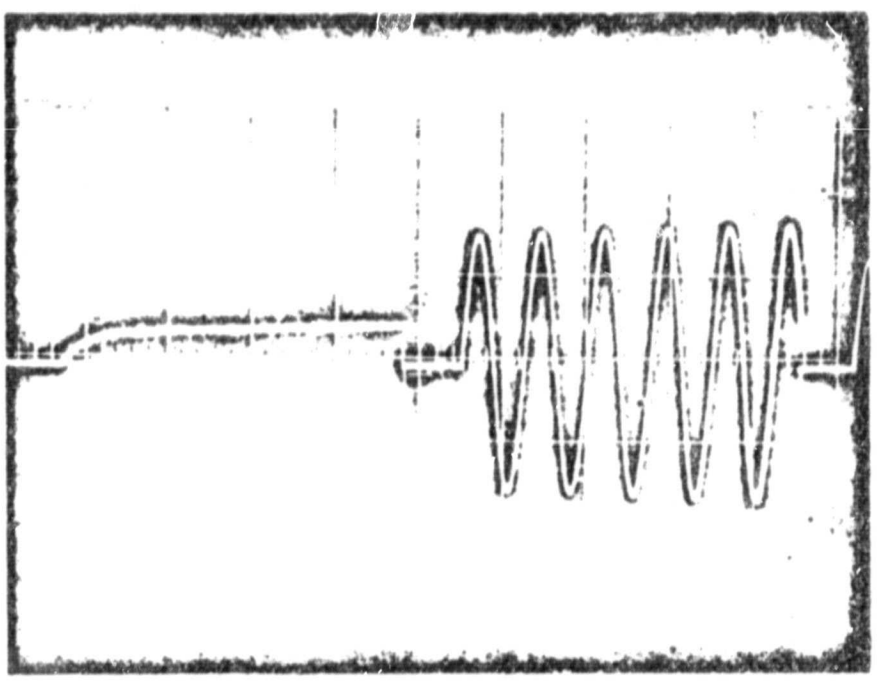
Figure 11. Patch Connections on LPB and DPB

```
                                     /AY-6 JULY 2,1970
                                     /ITERAIVE PATCHING
00000   200023  R                    BGN     LAC     (FIRST-1
00001   060024  R                            DAC*    (10)
00002   200014  R                            LAC     CONST
00003   040015  R                            DAC     COUNT
00004   220010  A                    LOOP    LAC*    10
00005   705204  A                            705204          /LOAD C.R WITH A.C
00006   705021  A                            705021          /TEST CLOCK FLAG
00007   600006  R                            JMP     .-1     /
00010   705222  A                            705222          /MAKE SINGLE RUN
00011   440015  R                            ISZ     COUNT
00012   600004  R                            JMP     LOOP
00013   600000  R                            JMP     BGN
                                     /
00014   777773  A                    CONST   -5
00015   000000  A                    COUNT   0
00016   000067  A                    FIRST   067             /PLOBLEM.1
00017   000131  A                            131             /PLOBLEM.2
00020   000123  A                            123             /PLOBLEM.3
00021   000155  A                            155             /PLOBLEM.4
00022   000152  A                            152             /PLOBLEM.5
        000000  R                            .END    BGN
00023   000015  R *LIT
00024   000010  A *LIT
                                                  NO ERROR LINES
```

TABLE. 1. PDP-9 Program for Pattern Generation

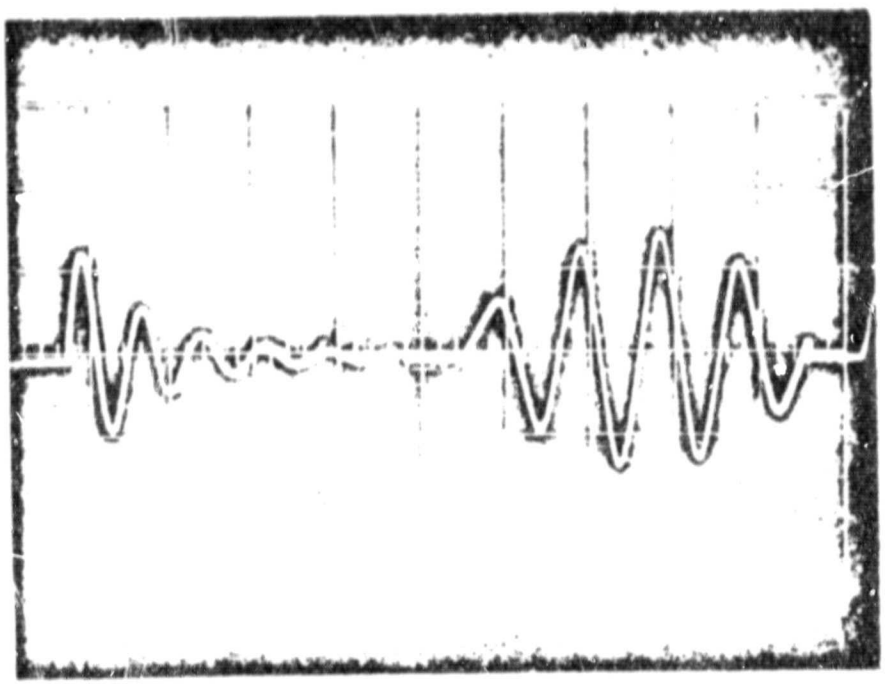


(a) Solution of 5 Differential Equations
CONTROL SIGNAL B1
VERTICAL SCALE 5V/cm
HORIZONTAL SCALE 2.4 MS/cm



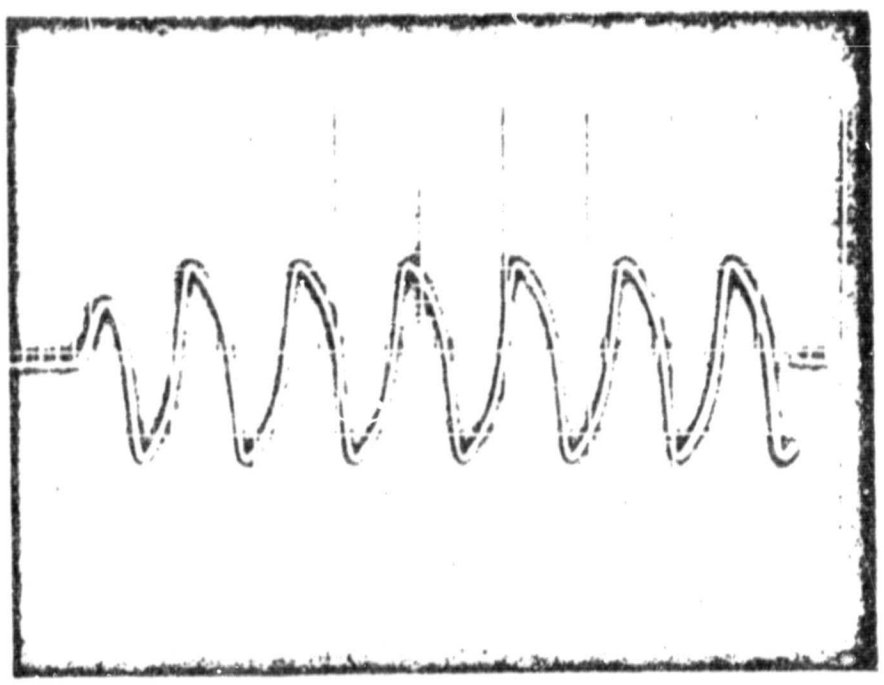
(b) Problem (1) and (2)
VERTICAL SCALE 5V/cm
HORIZONTAL SCAL 1ms/cm

Fignre 12.



(c) Problem (3) and (4)

VERTICAL SCALE 5v/cm
HORIZONTAL SCALE 1ms/cm



(d) Problem (5)

VERTICAL SCALE 5v/cm
HORIZONTAL SCALE 0.5ms/cm

Figure 12. Wave forms of the Solution of 5 Differential Equation

ACKNOWLEDGEMENTS

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