NASA CR-111806

DEVELOPMENT OF ION IMPLANTATION TECHNIQUES FOR MICROELECTRONICS

BY

O. J. MARSH, H. DUNLAP, R. HART,

AND R. G. HUNSPERGER

PREPARED UNDER CONTRACT NO. NAS 12-124 BY

HUGHES RESEARCH LABORATORIES

A DIVISION OF HUGHES AIRCRAFT COMPANY

3011 Malibu Canyon Road

Malibu, California 90265

FOR

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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FOREWORD

This is the Final Report on Contract NAS 12-124. The work reported herein was accomplished by Hughes Research Laboratories, 3011 Malibu Canyon Road, Malibu, California 90265. This report covers the period of September 1, 1969 to August 31, 1970. Three previous reports concerning Development of Ion Implantation for Microelectronics are dated October 1967, October 1968, and October 1969. The NASA-ERC program monitors for the 1970 contract were, in chronological order, Dr. J. Shier, Dr. K. Behrndt, and Dr. K. Haq. Dr. J. Robertson of NASA Langley was appointed Contracting Officer during the latter period of this contract. The principal investigators on this contract were O.J. Marsh, H.L. Dunlap, R.R. Hart, and R.G. Hunsperger. Technical assistance was provided by D.M. Jamba, R.G. Wilson, and E. Wolf.

ABSTRACT

This report presents the results of a study on the application of ion implantation to the formation of conducting layers and p-n junctions in GaAs and SiC. Considerable attention has been given to the analysis of the formation and annealing of disorder introduced by ion implantation. Techniques such as Rutherford backscattering, reflectivity, and electron channeling patterns have been used to analyze disorder. Electrical evaluation of implanted layers, through Hall effect and sheet resistivity measurements, has been investigated as a function of annealing conditions. Conducting layers of n- and p-type, with electrical properties similar to bulk grown material, have been formed in GaAs by implanting standard n- and p-type dopants and subsequently annealing in the layers at 800°C. Conducting n-type layers of good electrical quality have been formed in SiC by implanting impurities from column V of the Periodic Table after the layers have been annealed at 1600°C. Similar anneal procedures performed on layers implanted with standard p-type dopants have not resulted in p-type layers in SiC.

We have evaluated p-n junctions produced in GaAs and SiC ion implantation and found them to have excellent characteristics from 23° to 300°C.

SECTION I

INTRODUCTION

We have investigated ion implantation and its development for use as a doping process in materials with greater bandgaps than silicon. We have found that the ion implantation process can be used to fabricate excellent quality p-n junctions in gallium arsenide (GaAs) and silicon carbide (SiC). In addition, conducting layers can be controllably formed with a wide range of sheet resistivities. This control will find great use in device applications for forming ohmic contacts, resistors, or regions of controlled carrier concentrations.

In the preceding contract report of October 1969, we described the beginning of a program to determine the characteristics of doped layers produced in GaAs by ion implantation at room temperature. The work of the past year has demonstrated that good quality p-type layers can be formed by implantation of cadmium or zinc at room temperature followed by annealing at elevated temperature, while n-type layers can be produced by similar implantation and anneal procedures using sulfur ions. In general, annealing at 700°C for as little as 10 min is sufficient to yield useful carrier concentrations and relatively high mobilities in these layers.

A detailed study has also been made of the lattice damage produced in GaAs by implantation of 60 keV cadmium ions at room temperature and its anneal behavior. Measurements performed by three independent experimental techniques are in good agreement with each other and show that an ion dose 5×10^{13} Cd^{+}/cm^{2} produces an essentially amorphous

layer. Samples implanted with less than this saturation dose exhibit substantial annealing of damage at temperatures below 300°C, while samples implanted with greater ion dose require annealing at higher temperatures.

In the interim contract report of October 1969 we described the measures we had taken to control or eliminate semi-insulating layer formation in ion implanted GaAs p-n junctions. During this year we have investigated the possibility of intentionally creating such a layer for purposes of electrical isolation. Semi-insulating layers as much as 1.1 μ in thickness have been produced by implantation of 60 keV protons at room temperature.

We have produced a number of ion- implanted GaAs diodes that exhibited good rectification characteristics with unusually low leakage current, when operated at temperatures up to 300°C. The leakage current at 300°C was significantly less than that observed for GaAs diodes prepared by conventional diffusion or by iso- and hetero-epitaxial vapor growth techniques.

We have formed n-type conducting layers in n- and p-type hexagonal SiC and n-type cubic SiC by implanting ions from column V of the periodic table; nitrogen (N), phosphorus (P), antimony (Sb), or bismuth (Bi). The implantations were performed at room temperature and with energies ranging from 5 to 300 keV. The implanted layers have been evaluated for electrical properties by the van der Pauw-Hall effect and sheet resistivity measurements. Studies of disorder in the layers were accomplished with the measurement of Rutherford backscattered 140 keV protons and 280 keV He^{++} and with the scanning electron microscope. Evaluation of the annealing behavior of the layers after implantation showed that reordering is observed after a 500°C anneal. The most significant reordering takes place at around 800°C and is

nearly complete after a 1200°C anneal. p-n junction behavior between the implanted layer and a p-type substrate is first observed after an anneal at approximately 800°C, although Hall effect measurements can only be performed after anneals of 1100°C or higher. The carrier mobility continues to improve with annealing to 1700°C, while the carrier concentration in the layer remains constant at about 1/2 to 1/3 the implanted dose. Anneals above 1700°C results in decomposition of the SiC and a loss of carriers.

We have attempted to form p-type layers in n-type SiC by implanting beryllium (Be), boron (B), aluminum (Al), gallium (Ga), and thallium (Tl). Application of anneal procedures identical to those used to form n-type layers have not resulted in measurable p-type layers. Rutherford backscattering measurements were performed to determine the lattice position occupied by implanted Tl ions but were inconclusive due to possible impurity solubility effects.

The p-n junctions formed by the donor-implanted layers have been evaluated as a function of anneal temperature. After annealing at 1200°C, there is direct evidence of a thick semi-insulating region beneath the n-layer and the substrate which produces a p-i-n diode characteristic. The thickness of this i-layer can be substantially reduced with additional annealing, resulting in abrupt junction behavior for the diode.

Well annealed p-n junctions have been characterized as a function of operating temperature over the range of 23° to 400°C. The forward current-voltage behavior of these diodes is dominated by generation and recombination of the carriers in the depletion layer over most of the temperature range. There is some indication of diffusion currents at the highest temperatures. Avalanche breakdown behavior is observed for reverse bias.

The following publications are related to work accomplished under this program:

1. R.R. Hart, H.L. Dunlap, and O.J. Marsh, "Disorder Produced in SiC by Ion Bombardment," accepted by Radiation Effects.
2. R.G. Hunsperger, E.D. Wolf, G.A. Shifrin, O.J. Marsh, and D.M. Jamba, "Measurement of Lattice Damage Caused by Ion-Implantation Doping of Semiconductors," submitted to Radiation Effects.
3. O.J. Marsh and H.L. Dunlap, "Ion Implanted Junctions and Conducting Layers in SiC," accepted by Radiation Effects.
4. R.G. Hunsperger and O.J. Marsh, "Electrical Properties of Cd, Zn, and S Ion-Implanted Layers in GaAs," Radiation Effects, accepted for publication.
5. J.E. Westmoreland, O.J. Marsh, and R.G. Hunsperger, "Lattice Disorder Produced in GaAs by 60 keV Cd Ions and 70 keV Zn Ions," Radiation Effects, accepted for publication.
6. G.A. Shifrin and R.G. Hunsperger, "The Effect of Ion Implantation Damage on the Optical Reflection Spectrum of GaAs," Applied Physics Letters, accepted for publication (Oct. 1, 1970 - tentative date).
7. R.G. Hunsperger and O.J. Marsh, "Anneal Behavior of Defects in Ion Implanted GaAs Diodes," Metallurgical Trans. 1, 603 (1970).
8. R.G. Hunsperger and O.J. Marsh, "Electrical Properties of Zinc and Cadmium Ion Implanted Layers in Gallium Arsenide, J. Electrochem. Soc. 116, (1969).
9. H.L. Dunlap and O.J. Marsh, "Diodes in Silicon Carbide by Ion Implantation," Appl. Phys. Letters 15, 311 (1969).
10. R.G. Hunsperger, O.J. Marsh, and C.A. Mead, "The Presence of Deep Levels in Ion Implanted Junctions," Appl. Phys. Letters, November 1968.
11. J.W. Mayer, O.J. Marsh, R. Mankarious, and R. Bower, "Zn and Te Implantations into GaAs," J. Appl. Phys. 38, 1975 (1967).

The capacitance-voltage behavior of these diodes as a function of frequency and temperature indicate the presence of a deep level which can be explained in terms of the bulk properties of the material. The manner we have chosen to present the material resulting from the work on this contract is to describe separately the work on GaAs (Section II) and SiC (Section III).

SECTION II

ION IMPLANTATION STUDIES IN GaAs

A. ELECTRICAL PROPERTIES OF ROOM TEMPERATURE IMPLANTED LAYERS

Previous reports have described the electrical properties of layers formed by implantation of Zn, Cd, Te, and Sn ions at 400°C (Ref. 1,2) and by room temperature implantation of C (Ref. 1), S (Ref. 2,3), and Zn (Ref. 2) ions. In subsequent paragraphs we will discuss continuation of this work, involving measurements on layers formed by room temperature implantation of Cd or S ions.

The following experimental procedure was used for both Cd- and S-implanted samples.

The samples were prepared from gallium arsenide <111> oriented wafers approximately 15 mils thick, with the B-face etch-polished in a solution of methyl alcohol and bromine to remove sawing and lapping damage prior to ion implantation. Ion implantation was performed, with the substrates at room temperature, using a magnetically-mass-separated ion beam. Prior to annealing the samples were coated with a sputtered layer of SiO_2 about 2000 Å thick to prevent outdiffusion of dopant atoms and decomposition of the GaAs. Annealing was performed in a nitrogen atmosphere.

The p-type dopant Cd was implanted into n-type substrates and S ions were implanted into p-type substrates, so that the resulting p-n junction would provide electrical isolation of the implanted layer during measurement. Substrate background impurity concentrations were $\sim 1 \times 10^{16}/cm^3$. The electrical characteristics of the implanted layers (sheet resistivity

ρ_s, effective surface carrier concentration N_s, and effective mobility μ) were determined using the van der Pauw-Hall measurement technique.[4] Square shaped Hall samples ($\sim$4 mm on a side) were diced from the ion-implanted substrate wafers prior to annealing. All Hall measurements were made at room temperature, after the samples were quenched in air from whatever temperature at which they were annealed. The maximum possible error in the Hall measurements is estimated to be approximately 10%. This maximum error could occur only in cases in which the sheet resistivity is large ($> 10^4$ $\Omega/\square$), consequently the Hall voltage is difficult to measure because of background noise voltage. Otherwise, error is limited to the accumulative instrument error of approximately 3%.

A group of samples was implanted with 60 keV cadmium ions, with doses ranging from 1.5×10^{13} ions/cm^2 to 1×10^{15} ions/cm^2. These samples were then annealed for 10 min at temperatures in the range 100° - 900°C. The surface carrier concentrations that were measured in these samples after annealing are shown in Fig. 1. No measurable p-type layer was formed in any sample until after it was annealed at 600°C (for samples implanted with a large ion dose) or 700°C (for samples implanted with a relatively small ion dose). The lower values of N_s in samples implanted with ion dose = 1×10^{15}/cm^2 and annealed at 700° or 800°C compared with those in samples with ion dose = 8×10^{14}/cm^2 may indicate that residual defects are producing some compensating centers. A greater concentration of such defects would be expected in the case of samples implanted with the larger ion dose. However, after annealing at 800° or 900°C samples implanted with $\leq 10^{14}$ ions/cm^2 exhibited essentially 100% electrical activity; thus no significant compensation occurred in these samples. The dependence of surface carrier concentration on ion dose is shown in Fig. 2. In samples

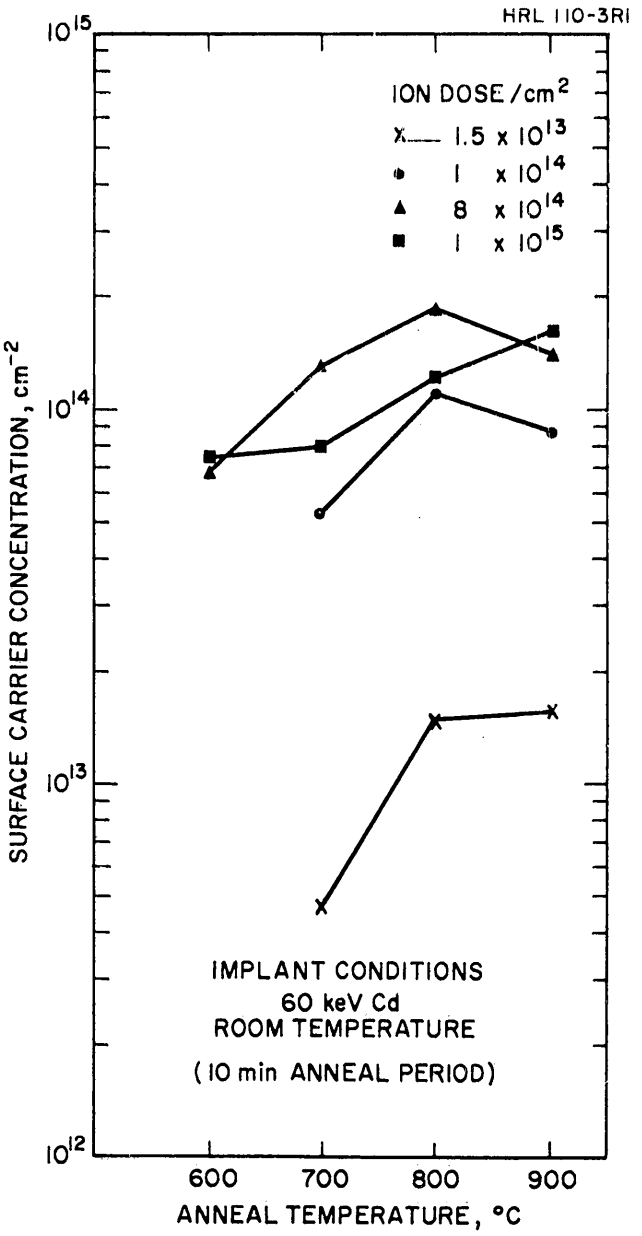

Fig. 1. Dependence of surface carrier concentration on anneal temperature for 60 keV Cd^+ ion-implanted layers.

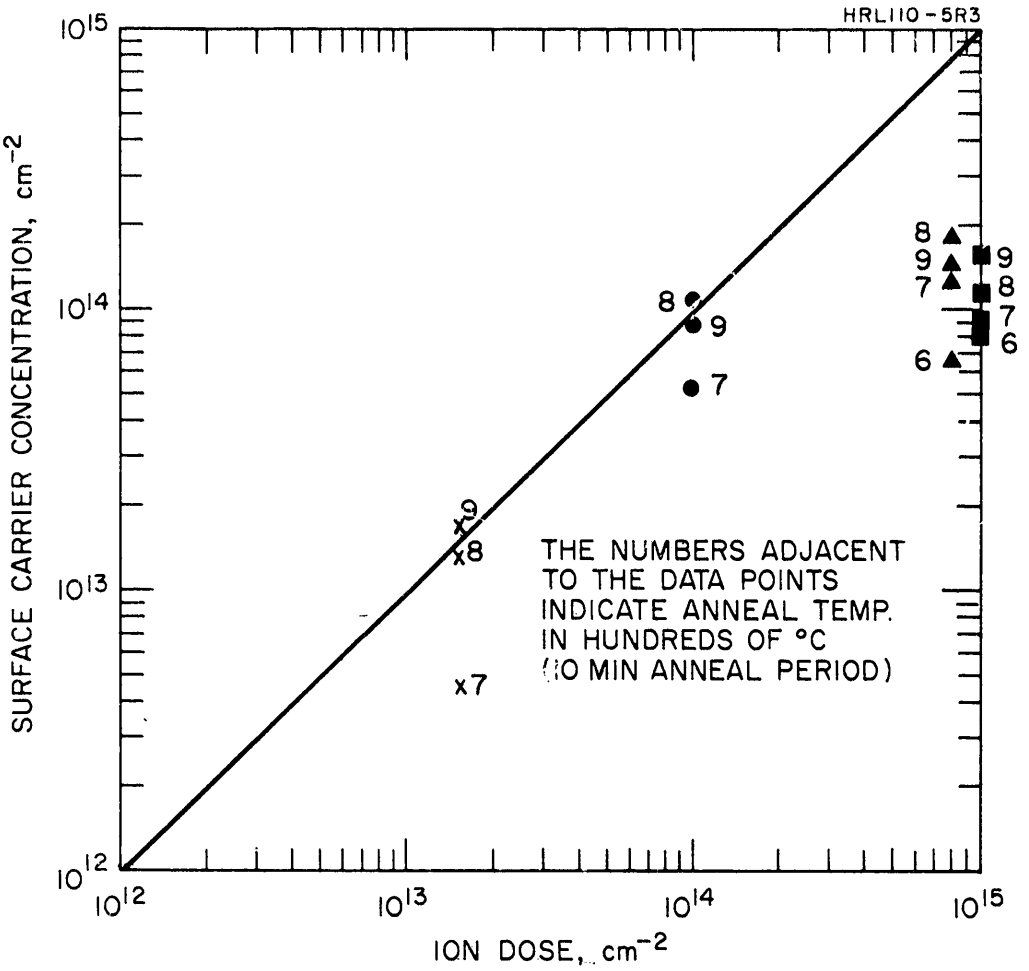

Fig. 2. Dependence of surface carrier concentration on ion dose for 60 keV Cd^+ ion-implanted layers.

annealed at 800° or 900°C there is a 1:1 correspondence of the two, up to a dose of approximately 1 x 10^{14} ions/cm^2; for larger doses N_s tends to saturate at about 2 x $10^{14}/cm^2$. Some samples with ion dose > 2 x $10^{14}/cm^2$ were annealed for as long as 2 hours at 800°C and N_s still remained ≈ 2 x $10^{14}/cm^2$, thus the saturation does not appear to be the result of insufficient anneal time. Measurement of the thickness of the p-type layer by sputter-stripping layer removal has shown it to be approximately 0.1 μm thick. Thus the average carrier concentration saturates at about 2 x $10^{19}/cm^3$. Goldstein[5] has reported 2 x $10^{19}/cm^3$ as the maximum Cd concentration obtainable in GaAs by diffusion at 900°C from a vapor source. Thus the saturation of N_s in the ion implanted samples may result from reaching the solubility limit of Cd in GaAs at the anneal temperature.

The values of mobility in these Cd ion implanted samples are shown in Fig. 3. Mobility generally increased with increasing anneal temperature, and μ was lower in samples with larger ion dose. In the case of ion dose = 1.5 x $10^{13}/cm^2$, the decrease in μ as anneal temperature was raised from 700° to 800°C was caused by increased carrier concentration and resulting ionized impurity scattering. This fact can be seen in Fig. 4, in which the mobility data are plotted as a function of carrier concentration. The theoretical curve shown in Fig. 4 assumes that ionized impurity scattering and lattice scattering are the only mechanisms affecting mobility, with ionized impurity scattering determined by the Brooks-Herring relation[6,7] and lattice mobility taken as 450 cm^2/V-sec, following the work of Rossi, et al.[8] Since the ionized impurity scattering is a function of the concentration of ions/cm^3, it has been assumed that the ions are uniformly distributed over a depth of 0.1 μm to allow plotting of the

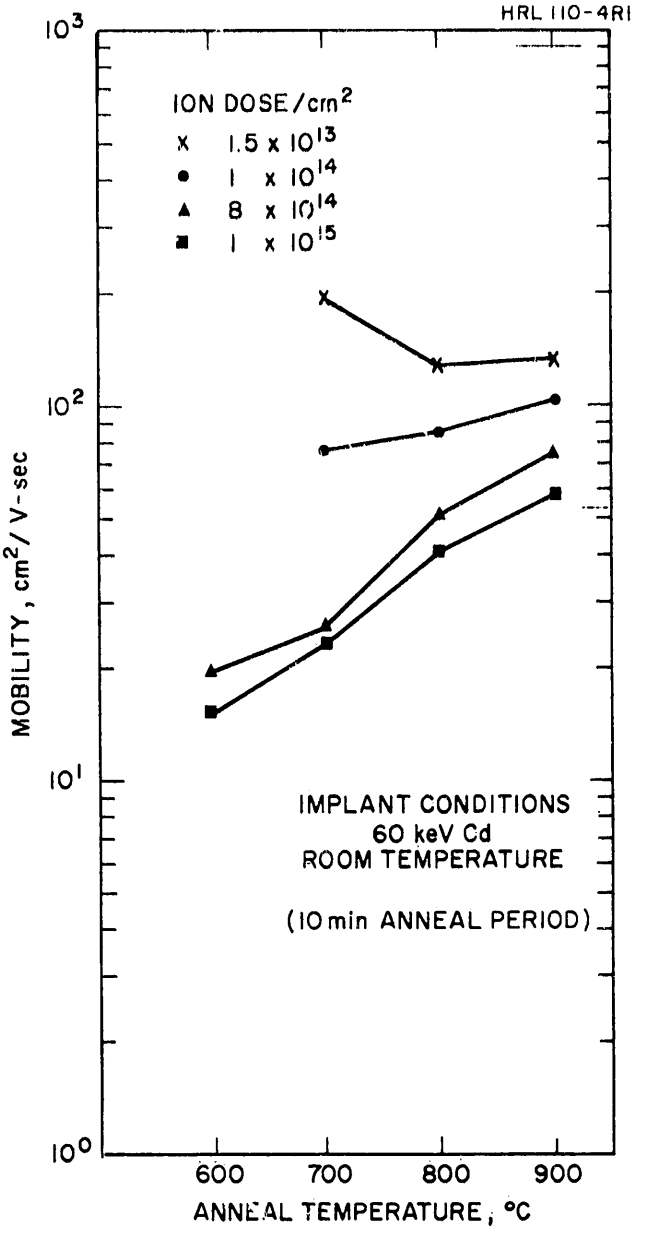

Fig. 3. Dependence of mobility on anneal temperature for 60 keV Cd^+ ion-implanted layers.

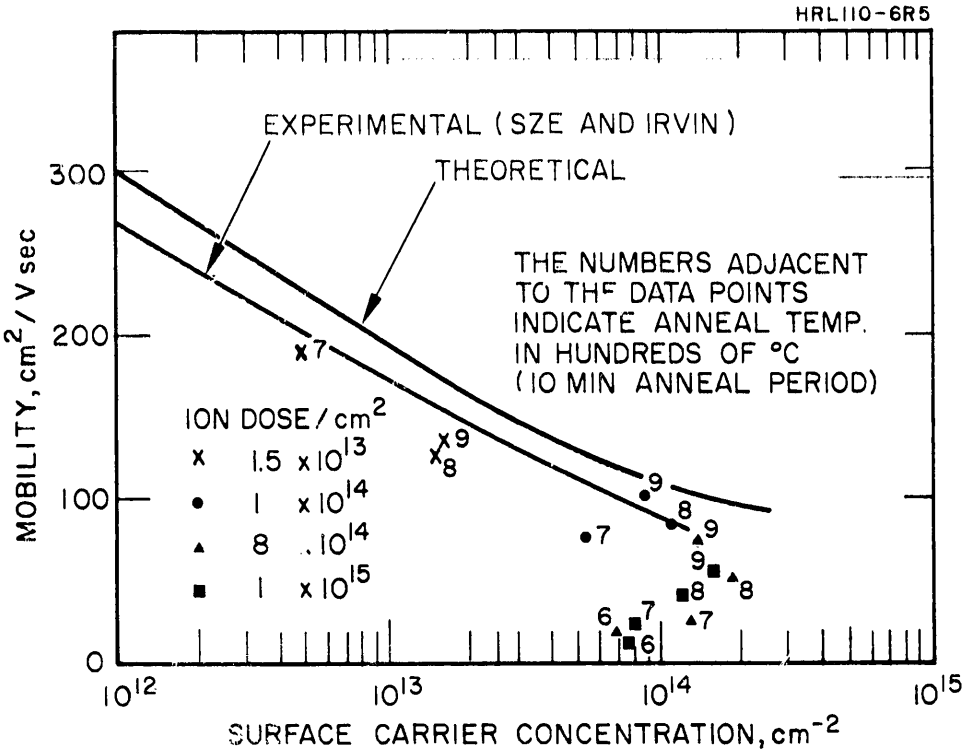

Fig. 4. Dependence of mobility on surface carrier concentration for 60 keV Cd^+ ion-implanted layers.

theoretical curve as a function of concentration/cm^2. This same assumption has also been made to permit comparison of the mobility in ion implanted layers with the experimental data of Sze and Irvin[9] for bulk GaAs single crystals. The data of Fig. 4 indicate that mobility in the ion-implanted layers decreased as a function of increasing carrier concentration, following the theoretical ionized impurity scattering curve. Even after the samples were annealed at 800° or 900°C, mobilities were somewhat lower than the theoretical values, possibly because of scattering from dislocations or other defects. However, the mobilities observed in ion-implanted layers annealed at 800° or 900°C agree very well with those reported by Sze and Irvin[9] for bulk crystalline GaAs, indicating that any residual lattice damage from the implantation process does not greatly affect mobility. The weighting of the measured Hall mobility by the more lightly doped portions of the ion concentration profile does not appear to be significant in this case, as evidenced by the close agreement between the measured values of N_s and the implanted ion concentration. (Reference 10 discusses weighting of the measured μ and N_s in ion-implanted layers.)

Since sheet resistivity is an important parameter in device fabrication, the values of ρ_s in these cadmium-implanted layers are presented in Fig. 5. In a given sample, sheet resistivity depends on both the surface carrier concentration and the mobility. It can be seen from the data that a high ρ_s is likely to result from implantation of either a high ion dose (because of low mobility) or a low ion dose (because of low carrier concentr on). In all cases, annealing at a higher temperature resulted in a lower sheet resistivity. However, the difference between 800° and 900°C annealed samples (implanted with the same ion dose) was not large.

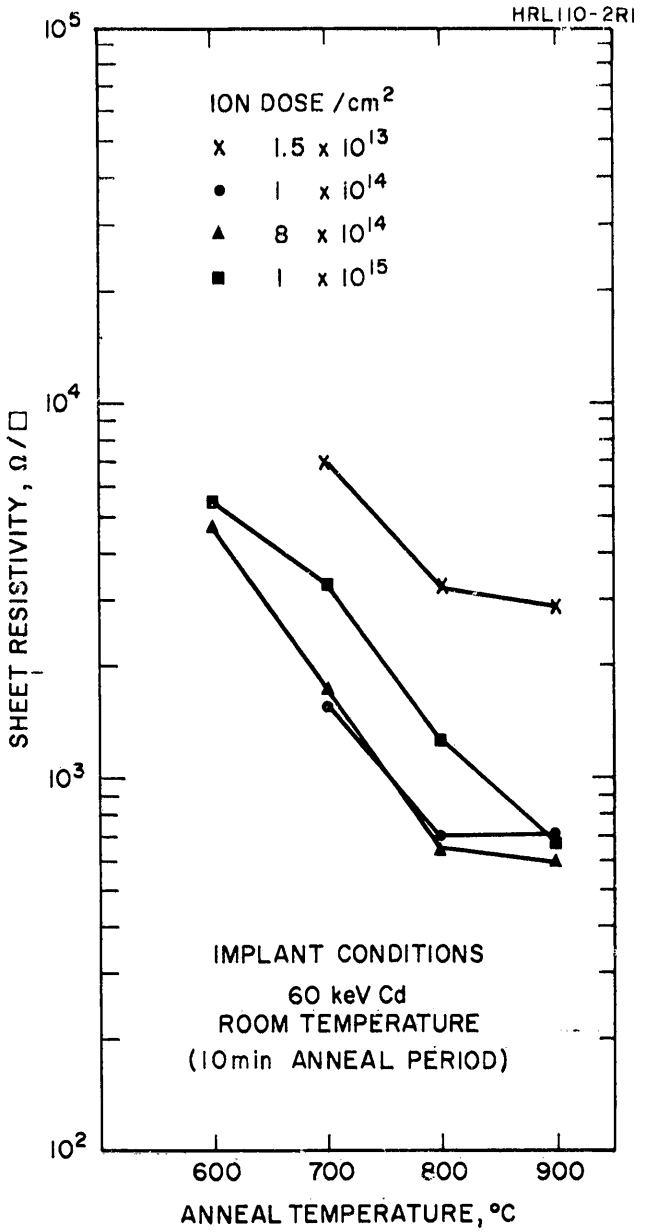

Fig. 5. Dependence of sheet resistivity on anneal temperature for 60 keV Cd^+ ion-implanted layers.

The anneal behavior of N_s, ρ_s, and μ was also measured for some 84 keV Zn^+, room temperature implanted samples with ion doses ranging from 1×10^{13} to $1 \times 10^{16}/cm^2$.

The properties of p-type layers produced by implantation of zinc ions are similar to those of layers produced by 60 keV cadmium implantation, in that no p-type layer was observed in samples annealed below a relatively high temperature (600°C for ion dose $\leq 10^{14}/cm^2$, 500°C for ion dose $\geq 10^{15}/cm^2$). In samples annealed below these temperatures, Hall voltage could not be measured, and sheet resistivity was on the order of 10^4 or 10^5 Ω/□ in all cases. (This contrasts somewhat with the behavior of 20 keV Zn^+, room temperature implanted samples which exhibited measurable Hall voltages after low temperature annealing.[3]) When the 84 keV samples were annealed at 600°C or higher, p-type layers were formed in which the Hall voltage was measurable.

The electrical properties of n-type layers created in p-type substrates by implantation of sulfur ions contrast somewhat with those of Cd and Zn implanted layers. Implantation of sulfur ions (with energy in the range 30 to 100 keV and ion dose from 10^{12} to $10^{16}/cm^2$) into a p-type substrate at room temperature resulted in the formation of an n-type layer without any annealing being required. (This effect has been previously reported in References 2 and 3.) The layers had a high resistivity (typically $\sim 10^4$ Ω/□), low mobility (~ 1 cm^2/V-sec), and $N_s \sim 10^{14}/cm^2$, for samples implanted with more than 10^{14} ions/cm^2. ρ_s was higher for samples implanted with $< 10^{14}$ ions/cm^2 and Hall measurements were impossible. The low mobility was probably caused by the lattice damage which is present in layers implanted at room temperature. (Section B discusses lattice damage produced by room temperature implantation of GaAs.)

There were definitely n-type layers present, as evidenced by rectifying V-I characteristics between implanted layer and substrate and by injection electroluminescence under forward bias. The peak wavelength of the light emission was at 1.04 μ (at 77°K). Photoluminescence emission at this wavelength from sulfur doped GaAs has been reported by Williams and Blacknall[11] and attributed to recombination through centers resulting from complexes of sulfur atoms with lattice vacancies. It is interesting to note that the electroluminescent spectrum of Zn ion implanted diodes, annealed at 500°C or higher, (as previously described)[12] also contains an emission peak which appears to be associated with vacancy complexes, as well as the bandedge emission peak. Electroluminescence from cadmium ion-implanted diodes (annealed at 600°C or higher) has been observed in the near infrared portion of the spectrum, but no accurate determination of peak emission wavelength has been made as yet.

Annealing of these sulfur implanted layers at 100° and 200°C reduced sheet resistivities to $\sim 10^3$ Ω/□, but annealing in the range 300° to 500°C eliminated the n-type layer. Annealing at 600°C or above resulted in n-type layer formation again in relatively heavily doped samples.

Samples of p-type GaAs implanted with 100 keV sulfur ions at room temperature were annealed at various temperatures from 600° to 900°C. In samples with ion dose $\geq 4 \times 10^{14}/cm^2$, an n-type layer resulted after annealing at temperatures in the above range, while no such layer was observed in samples with dose $< 4 \times 10^{14}$ ions/cm^2. (Ion dose ranged from $1 \times 10^{12}/cm^2$ to $4 \times 10^{15}/cm^2$ in this set of samples.) When pressure-probe contacts were applied to these annealed samples, rectifying surface barriers resulted. Such surface barrier contact behavior is indicative of the presence of an n-type layer, since ohmic contacts would be expected to

result on p-type gallium arsenide. In addition, the behavior of the implanted layer-substrate n-p junction under reverse bias conditions was what would be expected for an abrupt junction. The leakage current was reasonably low and had the normal light sensitivity caused by photogeneration of minority carriers; breakdown voltage was approximately 35 V. This value agrees well with theoretical breakdown voltage[13] for an abrupt junction in a substrate with background doping concentration $\approx 2 \times 10^{16}/cm^3$, as was used in this case. Contact pads, which eliminated the surface barriers at the contacts, were formed on the samples by implantation of a dose of $10^{15}/cm^2$, 30 keV sulfur ions at room temperature. However, the resulting contacts had an extremely large effective series resistance. Hall measurements made using these implanted contacts erroneously indicated very low values of mobility in the sulfur implanted layers. Thin-sectioning measurements of electrical properties of sulfur implanted layers as a function of depth (made by Sansbury[14]) indicate very low mobility and high resistivity in that portion of the layer lying within several hundred angstroms of the surface. Since our implanted contacts were made to the top surface of the samples and did not penetrate more than a few hundred angstroms, a high resistivity surface layer could explain why these contacts were inadequate in this case. (Room temperature implanted contacts previously have been used effectively to contact tin implanted layers as well as bulk n-type GaAs.) To permit accurate Hall measurement it was necessary to provide contact pads by evaporating a layer of tin followed by a layer of nickel, heat treated for 2 min at 450°C. The carrier concentrations measured after proper contacts were made are shown in Fig. 6. Doping efficiency was very low ($\sim$1%), even in the best samples. Sansbury[14] has also reported low doping efficiency in sulfur-implanted

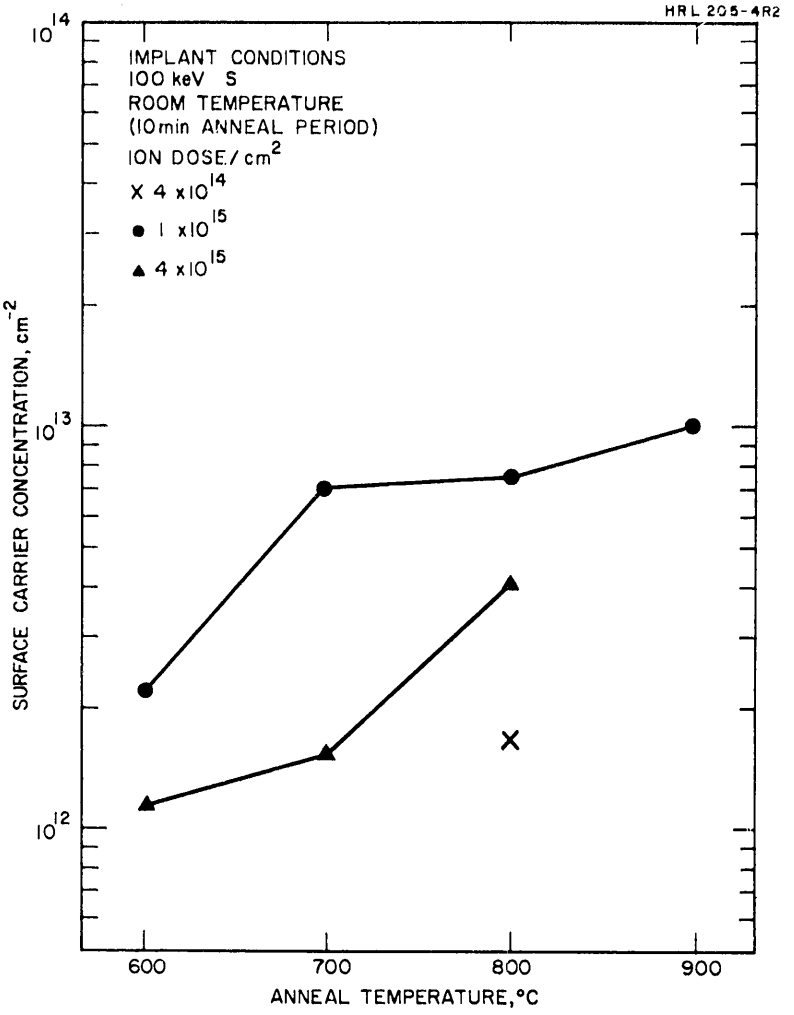

Fig. 6. Dependence of surface carrier concentration on anneal temperature for 100 keV S^+ ion-implanted layers.

GaAs (Cr doped, semi-insulating substrates). We have observed mobilities as high as 1740 $cm^2/V\text{-}sec$ in the implanted layers (see Fig. 7). Mobility in samples annealed at 700°C was significantly improved compared with identically implanted samples annealed at 600°C. However, increasing the anneal temperature to 800° or 900°C did not improve mobility significantly.

Production of n-type layers in GaAs by sulfur implantation is of great interest, since deep penetration of the ions can be expected compared with penetration of other n-type dopants as tin and tellurium. Angle section and stain measurements on a sample implanted with $4 \times 10^{15}/cm^2$ sulfur ions and annealed at 800°C for 10 min indicated a junction depth of 0.6 μm. This depth is considerably greater than the theoretical (LSS) projected range[15] of 100 keV S^+ ions in GaAs (700 Å); thus it appears that some channeling or diffusion took place during implantation. We anticipate that the ability to produce such deep n-type layers (with relatively high mobility) will be very useful in the fabrication of p-n-p transistors by ion implantation.

In summary, it has been established that p-type layers can be formed in GaAs by Cd or Zn ion implantation at room temperature, followed by annealing at elevated temperature. The anneal temperature required to produce the layer depends on the type of dopant ion and on the ion energy and dose. Also, n-type layers can be formed by implantation of sulfur ions at room temperature with no annealing and with annealing at 600°C or higher. For all three dopants there appears to be a significant anneal stage at approximately 700°C. Annealing above this temperature greatly improves mobility and increases surface carrier concentration. It is not

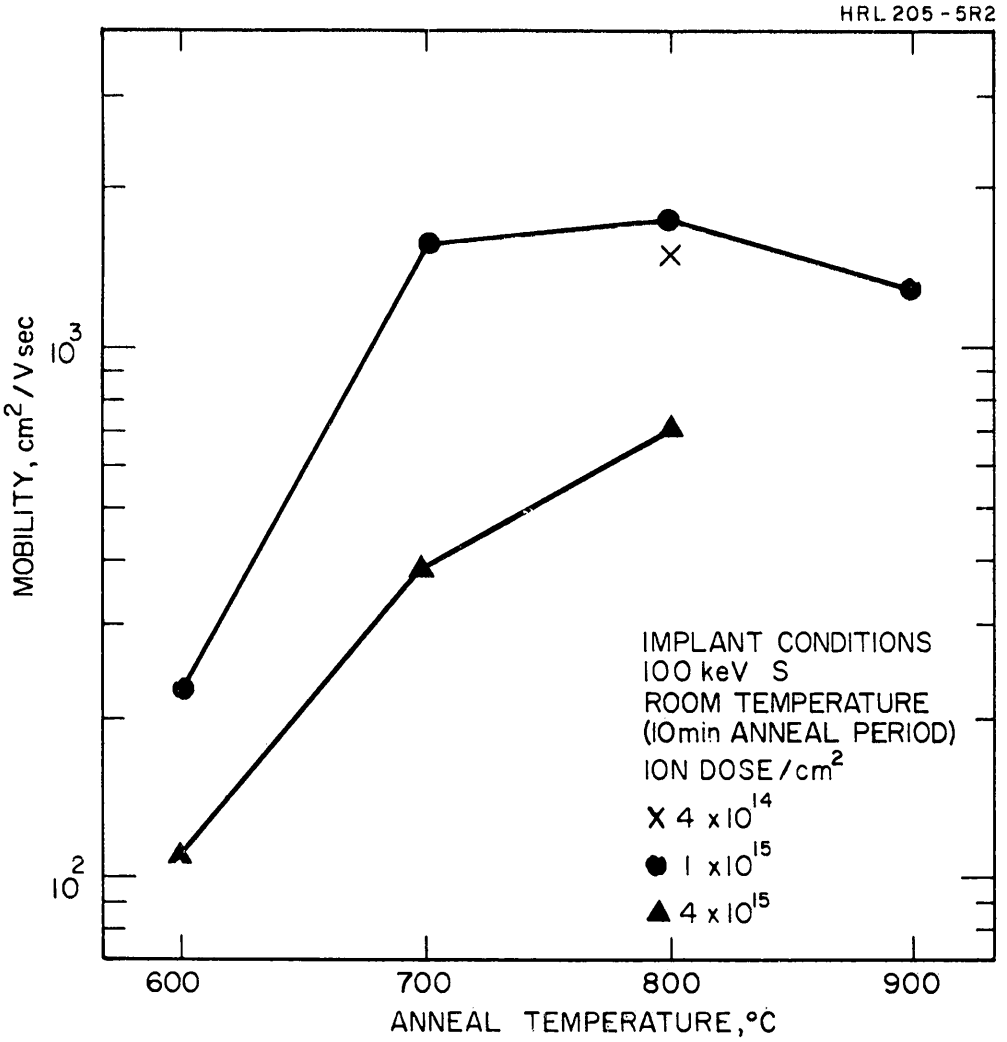

Fig. 7. Dependence of mobility on anneal temperature for 100 keV S^+ ion-implanted layers.

surprising that an anneal temperature of 700°C is required to produce high mobility, since studies of implantation-caused lattice damage (reported in Section B) indicate that a significant amount of damage remains after annealing at lower temperatures (except in the case of lightly doped samples).

B. LATTICE DAMAGE STUDIES

The study of lattice damage resulting from 60 kV Cd^+ ion-implantation of GaAs was begun in 1969 (Ref. 3) and completed this year. Three independent damage measurement techniques were employed: (1) Rutherford scattering measurements (in collaboration with E. Westmoreland, California Institute of Technology); (2) spectral reflectivity measurements (performed with G. Shifrin, HRL); and (3) scanning electron microscope observations (made in conjunction with E. Wolf, HRL). Some of these damage studies were performed under related Hughes Research Laboratories funded programs, but the work is reported here in its entirety.

1. Disorder Formation Studies

The lattice damage produced during the process of doping a semiconductor by ion implantation most often has been measured by observing the Rutherford backscattering of He^+ ions,[16] which is an extremely useful technique for establishing the relative amounts of lattice disorder present in samples and for identifying the location of implanted ions (substitutional or interstitial). However, the method involves time consuming critical alignment of the sample with the analysis beam. Thus we have investigated two new techniques to measure lattice damage that are more simple to employ, using either a scanning electron microscope or a

spectrophotometer. Measurements of lattice damage produced in gallium arsenide by implantation of 60 keV Cd^+ ions and its anneal behavior have been used as the basis for comparison of the two newer methods with the more established backscattering technique.

The samples similar to those used for the electrical measurements described in Section II-A, were prepared from GaAs <111> wafers, with the B-face etch-polished in a solution of methyl alcohol and bromine to remove damage from cutting and lapping. The substrates (0.? Ω cm, n-type) were implanted at room temperature with a 60 kV mass separated Cd^+ ion beam. Doses ranged from 1×10^{12} to $1 \times 10^{15}/cm^2$ in different samples, while Cd^+ ion beam current was $\sim 10^{-7}$ A/cm^2. Samples implanted at low dose levels were tilted ~8° off axis to minimize channeling effects.

The scanning electron microscope can be used to measure lattice disorder in the following manner. Patterns very similar to Kikuchi electron diffraction patterns are obtained when the secondary and/or backscattered electron intensity is displayed in the scanning-electron microscope as a function of the angle of incidence of the electron beam on a single crystal surface.[17,18] The quality of these Coates-Kikuchi patterns is sensitive to any chemical or physical process which tends to destroy or shift the periodicity of the first few hundred angstroms of a single crystal surface. In particular, the lattice damage resulting from ion implantation doping causes pattern degradation as shown in Fig. 8. Along with the photographs that illustrate qualitative changes in pattern resolution are shown line-scan plots of the angular dependence of backscattered electron intensity, corresponding to the horizontal white lines in the photographs. To obtain a parameter which is a measure of pattern quality, the fractional change in intensity ($\Delta I/\Delta I_{ref}$) across the (0 $\bar{4}$ 4) bandedge (line) was determined by dividing the change

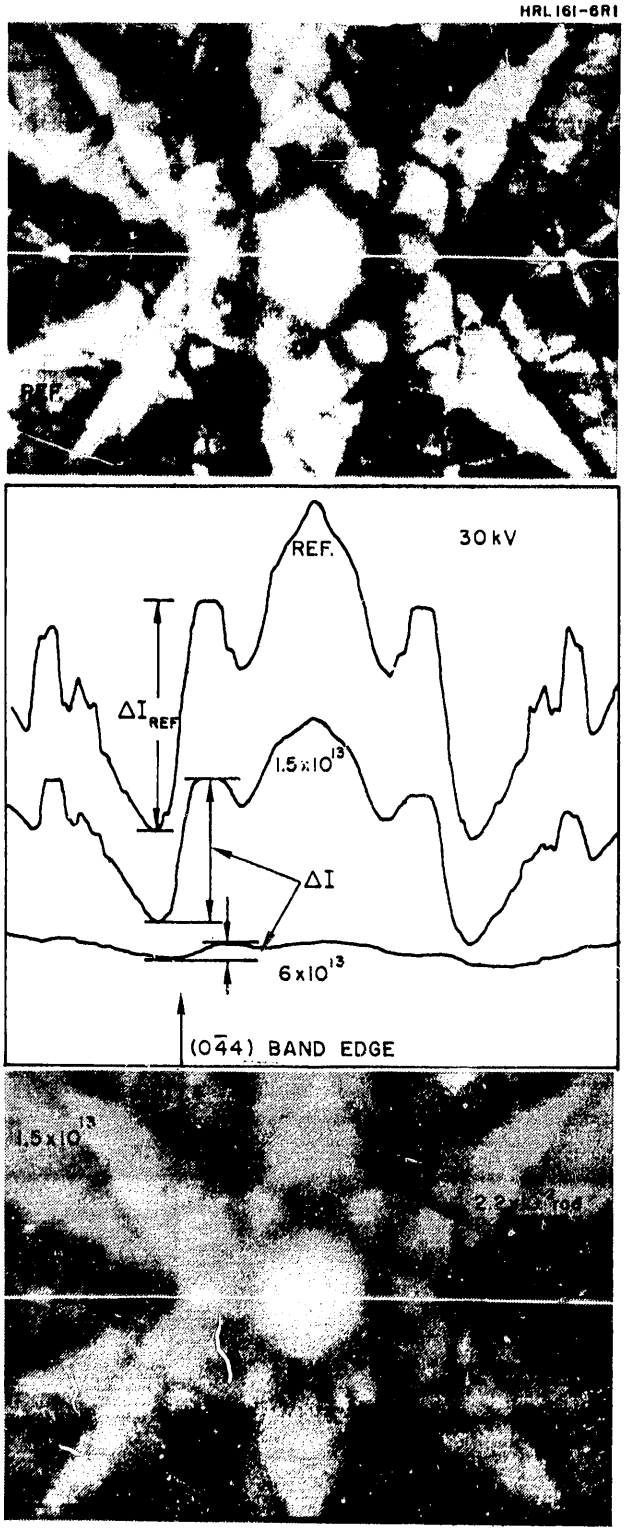

Fig. 8.
Coates-Kikuchi patterns of the reference standard (top) and 1.5×10^{13} Cd^{+}/cm^{2} ion dose (bottom). The line scans (center) of detector signal versus incident angle of the 30 kV electron beam were taken at the location indicated by the bright horizontal lines (top and bottom).

observed for an ion implanted sample (ΔI) by the intensity change for the reference crystalline sample (ΔI_{ref}). This fractional intensity change ($\Delta I/\Delta I_{ref}$) has been defined[19] as the normalized pattern quality I*. A plot of the parameter (1 - I*) in Fig. 9 shows Coates-Kikuchi pattern degradation as a function of implanted ion dose for electron beam acceleration voltages of 5.6, 10, and 30 kV. Also included are the data obtained from Rutherford backscattering of 1 MeV He^+ ions.[20] The ordinate on the right in Fig. 9 is a measure of lattice disorder in relative units as determined by the Rutherford backscattering measurements, and the data are plotted here so that total disorder coincides with complete loss of Coates-Kikuchi pattern detail; i.e., where I* = 0 and (1 - I*), the complement of the normalized pattern quality is equal to unity.

The two most significant features of Fig. 9 are that all curves show a break point or saturation at about 5×10^{13} Cd^+/cm^2 dose, and the lattice damage for a given dose caused a greater degradation of the Coates-Kikuchi pattern quality at lower primary electron beam acceleration voltages. It is not yet clear just how the parameter (1 - I*) is related to the lattice disorder, but it is apparent that there is good agreement between the variation of (1 - I*) with implanted ion dose and the relative lattice disorder as determined by the standard He^+ backscattering technique. We do know from earlier experiments (see Fig. 3, Ref. 19) that the backscattered electron intensity level for the completely amorphous condition (i.e., no pattern) was approximately the midpoint between all maxima and minima. That is, as lattice disorder destroys the identity of a direction of high penetration (i.e., originally a direction of minimum backscattered signal), the backscattered electron intensity increases.

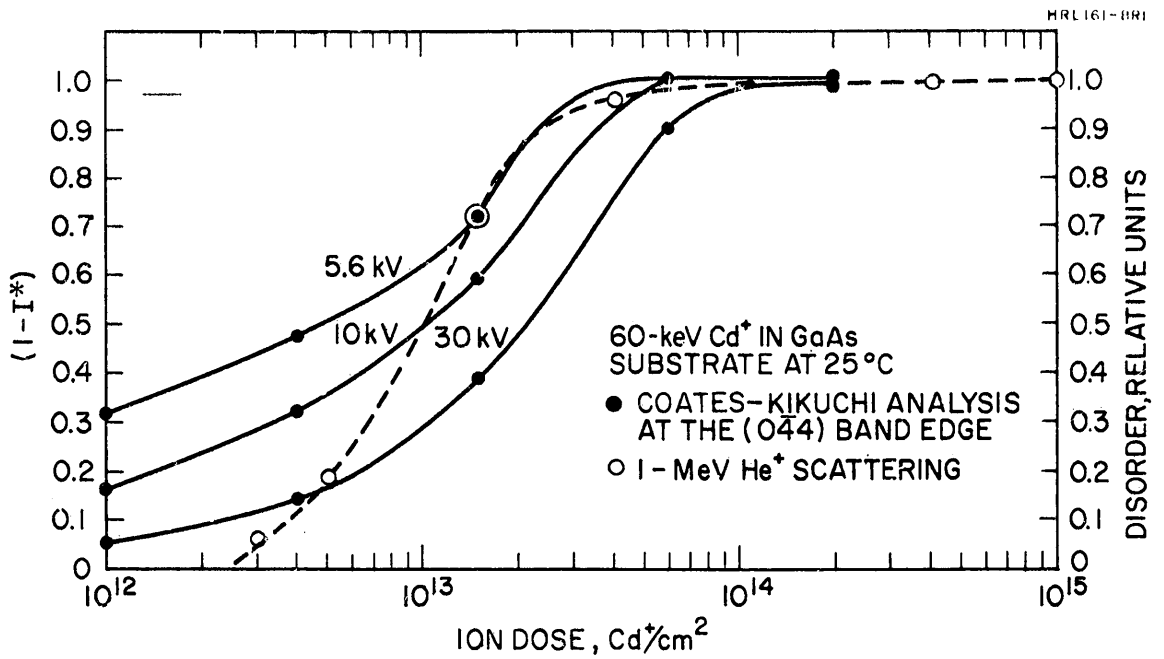

Fig. 9. Pattern degradation as a function of dose for 5.6, 10, and 30 kV electron beam accelerating voltages.

Conversely, the backscattered electron signal decreases from its maximum when the beam is aligned along a low index direction (e.g., within the (220) band) as the string-effect is destroyed by the lattice disorder.

A further important point evident in Fig. 9 is that the range of measurement can be increased by using different electron energies. If the electron beam acceleration voltage is lowered, the low dose regime $< 10^{12} Cd^+/cm^2$ can be explored, and if the voltage is increased, the high dose regime $> 10^{14} Cd^+/cm^2$ can be examined. However, one must be careful in interpreting these results in terms of an amorphous layer thickness. The thickness of the implantation-caused damage layer in these samples was always much less than the maximum electron range even at 5.6 kV, and it did not enter the measured value of I* merely as a weighted average of the electron penetration depth. For example, if the damage is extensive enough (dose $> 4 \times 10^{14}$) over the thickness of the theoretical 60 keV Cd^+ ion penetration depth (about 400 Å), then there is only random electron scattering and no pattern appears even for the 30 kV electron beam acceleration voltage.

Optical reflectivity measurements in the near ultraviolet portion of the spectrum have also been used to examine damage in these ion implanted layers, and they indicate essentially the same dependence of damage on implanted ion dose as was observed with the scanning electron microscope. Reflectance measurements were performed on a Cary Model 14 double beam spectrophotometer with a specular reflectance attachment. (Details of this measurement technique have been published.[21-23]) Spectra of reflectivity as a function of photon energy for typical samples of Cd^+ ion-implanted GaAs are shown in Fig. 10. The spectrum of unimplanted crystalline GaAs obtained on the same apparatus is shown

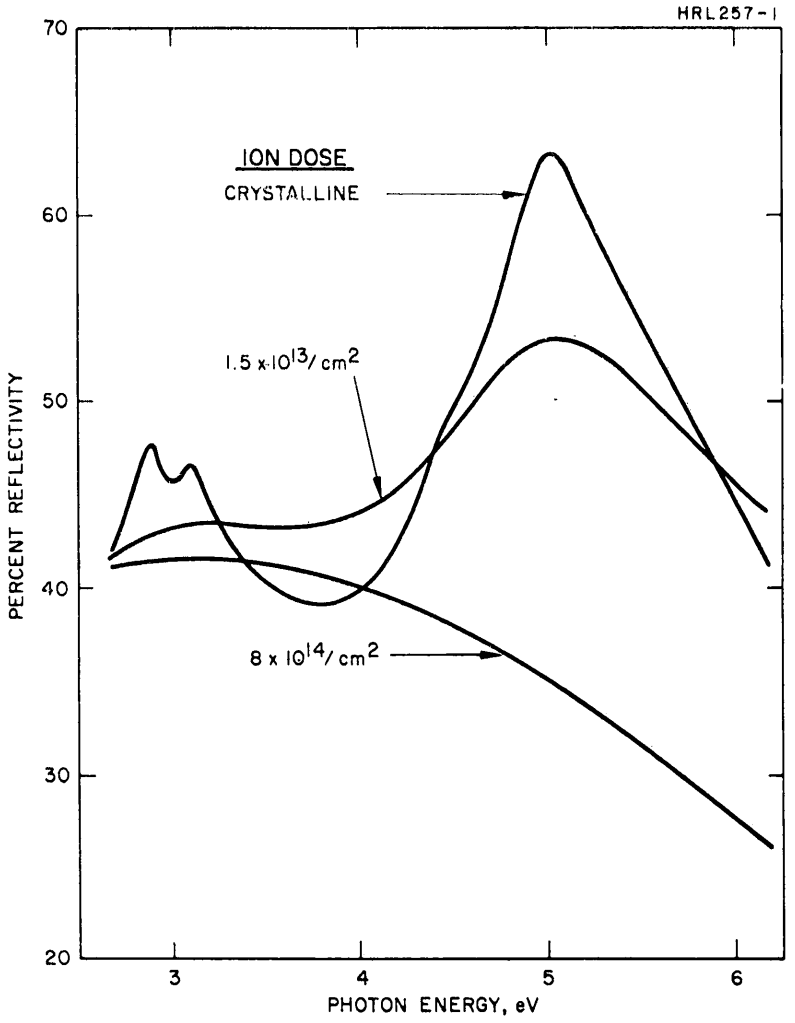

Fig. 10. Optical reflectivity spectra of 60 keV Cd^+-implanted layers in GaAs (in the 3-6 eV range of photon energy.

for reference; prominent peaks occur at approximately 5.1 eV and 3 eV. The decrease in reflectivity at these peaks with increasing ion dose can be used as a measure of relative lattice damage in much the same way that the normalized pattern quality I* was used in the scanning electron microscope measurements. Figure 11 shows the fractional change in reflectivity $(R_o - R)/R_o$ at the 5.1 eV (2450 Å) peak as a function of ion dose, where R is the reflectivity of an ion-implanted sample and R_o is the reflectivity of a nonimplanted crystalline sample (approximately 62%). Note that a dose of 10^{12} ions/cm^2 only slightly damaged the GaAs, while doses greater than approximately 10^{14} ions/cm^2 caused much damage. Saturation of the damage versus dose curve begins at a dose of about 5×10^{13} ions/cm^2. For ion doses in this saturation range the characteristic maxima and minima of the reflectivity spectra are eliminated, and spectra show a marked decrease in the rate of change of reflectivity with increasing dose. However, for the maximum dose used, a true saturation effect (i.e., no further spectral change) was not reached. Comparison of the reflectivity data with the relative lattice disorder determined by backscattering measurements[20] shows that both methods indicate saturation of lattice disorder for ion doses $\gtrsim 5 \times 10^{13}$/cm^2, corresponding to formation of an essentially amorphous layer.

2. Disorder Annealing Studies

To verify that the observed changes in reflectivity and Coates-Kikuchi pattern quality were the result of lattice disorder and not merely caused by roughening of the sample surface (with resultant diffuse scattering of light[23]) or by formation of a surface oxide or contaminant layer, post-implantation annealing of the Cd^+ ion bombarded samples was performed in a series of isochronal (15 minute) cycles at

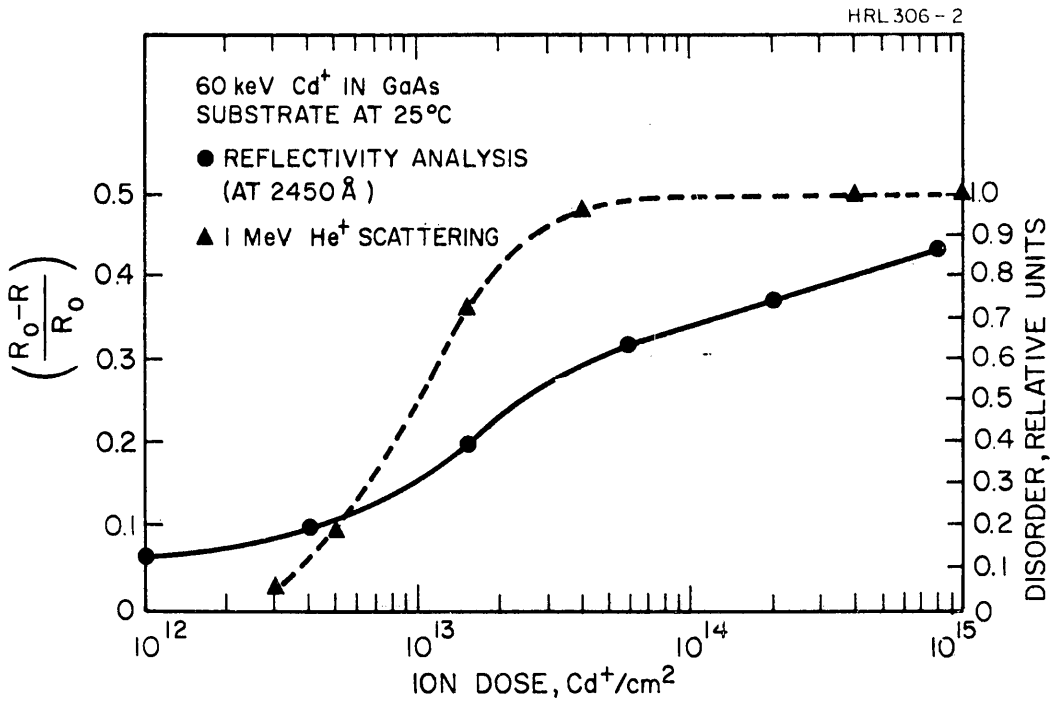

Fig. 11. Fractional change in reflectivity caused by implantation of 60 keV Cd^+ ions. (R_o = reflectivity of non-implanted crystalline sample = 62%; R = reflectivity of ion-implanted samples.)

temperatures ranging from 100° to 450°C in 50°C steps. (Annealing at 500° or 600°C was also performed in some cases.) The annealing oven was slightly pressurized with a flowing nitrogen atmosphere to avoid contamination. As lattice damage was removed by annealing, the reflectivity and the Coates-Kikuchi patterns of the samples were restored.

The reflectivity spectra for annealed samples tended to progress toward that of crystalline GaAs as the anneal temperature was increased; characteristic peaks and valleys began to emerge. The effect of annealing on reflectivity at a photon energy of 5.1 eV is indicated in Fig. 12 for three different ion doses. At 1.5×10^{13} ions/cm^2 (less than saturation) the implantation did not reduce the reflectivity much below the crystalline value. With annealing the reflectivity tended to return toward, and almost reach, the crystalline value, but after about 300°C there was relatively little change up to 600°C. At 6×10^{13} ions/cm^2 (just above saturation) the implantation initially reduced the reflectivity substantially below the crystalline value. However, annealing between 200° and 250°C produced a rapid increase in reflectivity and (above this range) a gradual increase up to the maximum annealing temperature of 600°C. The value of reflectivity even after the 600°C anneal was significantly less than the crystalline value and was not much greater than that for the more lightly implanted layer (1.5×10^{13} ions/cm^2) before annealing. The layer implanted with the largest ion dose (8×10^{14}/cm^2) showed yet a different characteristic. The reflectivity before annealing was quite low. Annealing increased the reflectivity, but even after 450°C it had only just reached the value which the intermediate sample had prior to annealing. However, upon further annealing at higher temperature this sample showed a marked decrease in reflectivity. This decrease is believed to be associated with decomposition of the crystal (perhaps through the loss of

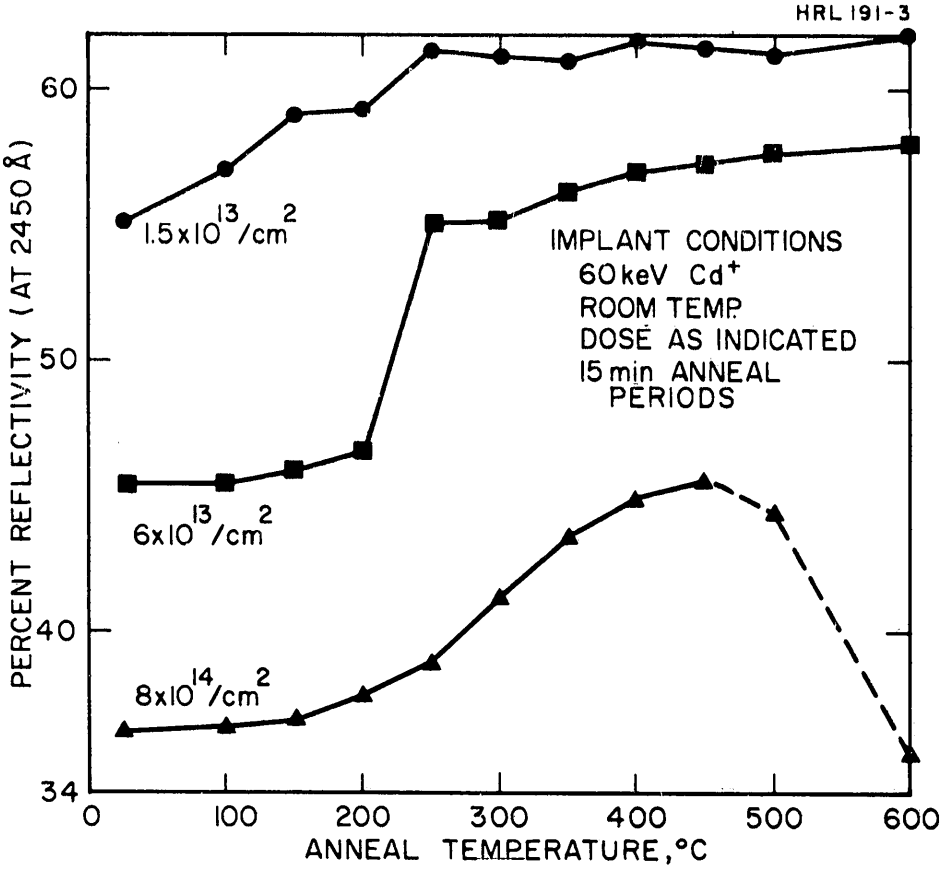

Fig. 12. Anneal behavior of reflectivity at a photon energy of 5.1 eV.

arsenic) when annealed above 400°C, after having received an implanted dose sufficiently high to produce much lattice disorder. It is possible that the decomposition might have been prevented or reduced if the sample had been protected with an oxide layer before being annealed at this temperature; thin layers of SiO_2 (≈2000 Å thick) have been proven effective in limiting decomposition during annealing to the extent that certain electrical properties of ion-implanted GaAs layers[24] are not measurably affected.

The anneal behavior of samples examined with the scanning electron microscope was essentially the same as that observed by reflectivity measurements. As lattice damage was removed by annealing, the Coates-Kikuchi patterns of the samples were restored. A quantitative measure of restored pattern quality is shown in Fig. 13 where I* is plotted as a function of anneal temperature for a number of samples. Comparison of the data of Figs. 12 and 13 shows that both techniques of measurement indicate that substantial damage annealing occurred at temperatures below 250°C for samples implanted with 1.5×10^{13} Cd^+/cm^2. An anneal stage at about 200° to 250°C was observed in samples implanted with 6×10^{13} Cd^+/cm^2, while the samples implanted with a dose of 8×10^{14} Cd^+/cm^2 exhibited only slight restoration after annealing even at 300°C. (Mazey and Nelson have observed an anneal stage between 270° and 300°C in Ne bombarded GaAs, using transmission electron microscopy.[25])

Rutherford scattering measurements of lattice disorder[20] following annealing confirm this pattern. As shown in Fig. 14, the lattice disorder (in terms of the number of scattering centers/cm^2 for an aligned He^+ beam) was reduced almost to the background value (≈ $1 \times 10^{16}/cm^2$) in a sample implanted with 5×10^{12} Cd^+/cm^2 after annealing at 300°C. A sample implanted with 4×10^{13} Cd^+/cm^2 exhibited gradual

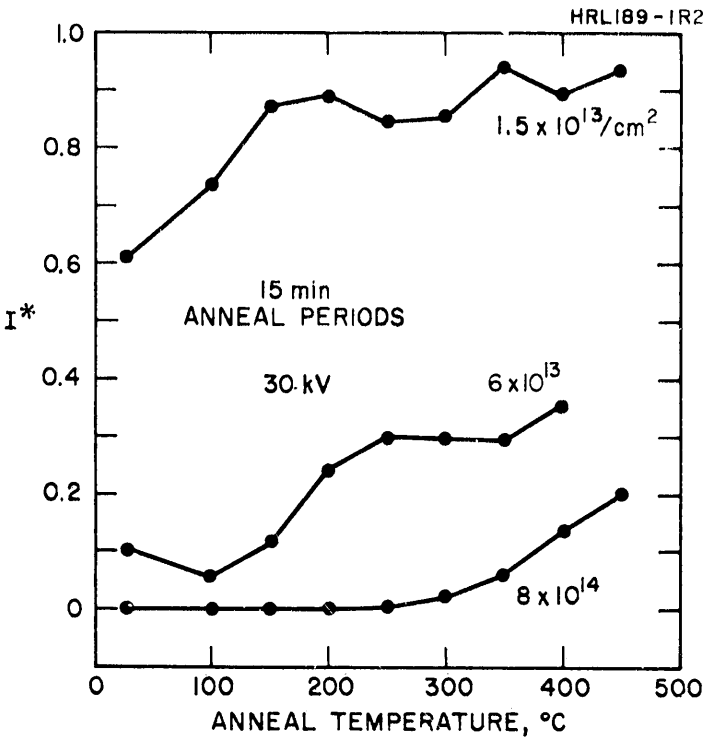

Fig. 13. Normalized Coates-Kikuchi pattern quality as a function of anneal temperature. (30 kV electron energy.)

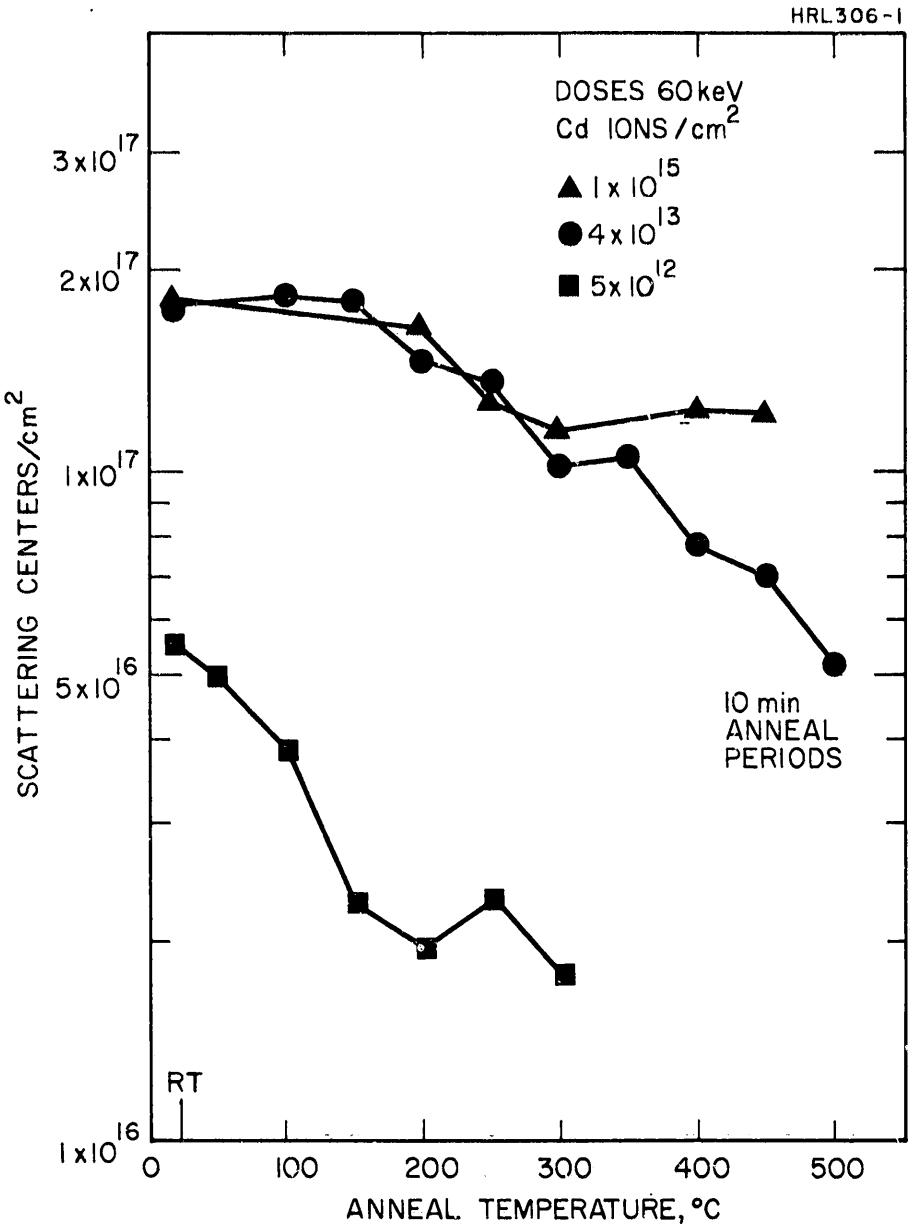

Fig. 14. Effect of annealing on the scattering centers (lattice disorder) produced in GaAs by 60 keV Cd^+ ions implanted at room temperature.

annealing at temperatures above 200°C, while restoration of crystallinity was relatively slight in the sample implanted with 1 x 10^{15} ions/cm^2 even after annealing at 450°C. Surface decomposition of the samples implanted with the largest Cd ion dose was not observed. In Rutherford backscattering measurements, surface decomposition appears as increased crystallinity and hence is difficult to distinguish from annealing of damage.[26]

The ion dose dependence and anneal behavior of lattice damage, as measured using the spectrophotometer or the scanning electron microscope, agree well with results of similar measurements made by the standard Rutherford scattering technique. This agreement suggests that the newer methods of measurement of spectral reflectivity or Coates-Kikuchi pattern quality provide a convenient way to investigate lattice damage produced by ion implantation. The theory and technology of these methods have not yet been developed to the extent that determinations of damage versus depth profiles or implanted-ion lattice locations can be made, as they can by the Rutherford scattering method. However, the two newer methods have advantages (in addition to convenience) such as the fact that 30 keV electrons and 5 eV photons do not produce additional lattice disorder during the measurement process, while 1 MeV He^+ ions do. Also, the spectral reflectivity method gives a clear indication of surface decomposition which cannot be mistaken for annealing of lattice damage.

C. INVESTIGATION OF THE SEMI-INSULATING LAYER IN SOME IMPLANTED DIODES

Previous measurements of the anneal behavior of the semi-insulating layer in cadmium-implanted diodes[3] showed a decrease in I-layer thickness with increasing anneal

temperature for substrates (with background concentration $n = 1 \times 10^{16}/cm^3$) implanted with 20 kV Cd^+ ions at room temperature; while I-layer thickness increased after identical annealing for diodes implanted at 400°C in substrates with background concentration $n = 1.2 \times 10^{14}/cm^3$. In order to separate the effects of implantation temperature and substrate background concentration, the thickness of the I-layer was measured for a series of samples implanted with 20 kV Cd^+ ions at 400°C into a substrate with $n = 1 \times 10^{16}/cm^3$. As anneal temperature was increased from 600° to 900°C, the thickness of the I-layer decreased from 39 μm to 4.1 μm (see Fig. 15). Thus the previously observed increase in I-layer thickness appears to be associated with the very low substrate background concentration rather than with the 400°C implantation temperature. A possible explanation for the effect is the following: In the case of very low background concentration, a correspondingly low concentration of defect centers is sufficient to fully compensate the substrate material; hence the I-layer thickness can increase substantially if diffusion of implantation-caused defects occurs during annealing. In more heavily doped substrates diffusion also would move defect centers deeper into the material, but the concentration of defect/cm^3 would be reduced to a level insufficient to produce total compensation over much of the depth profile; thus the thickness of the I-layer would decrease.

As part of the investigation of the semi-insulating layer found in some ion implanted diodes, we have examined the semi-insulating layer which results when bulk GaAs is implanted with protons. (Foyt, et al.,[27] have used proton bombardment to produce high resistivity isolating regions.) We implanted substrates of both n- and p-type GaAs at room temperature with 60 keV protons; the proton dose was $1 \times 10^{13}/cm^2$. Gold surface-barrier dots (of approximately

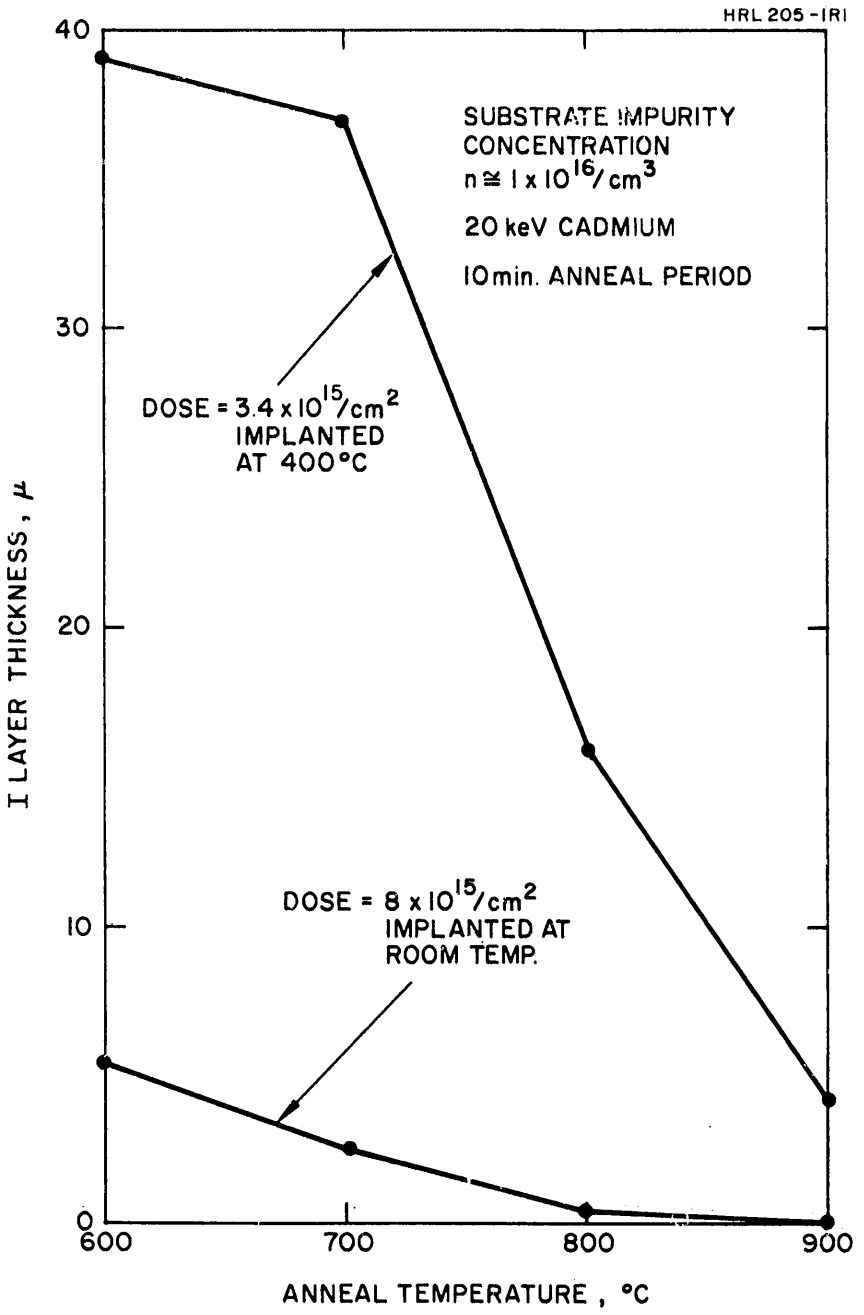

Fig. 15. Thickness of the semi-insulating layer in cadmium-implanted diodes.

0.125 mm^2 area) were evaporated onto the implanted surface of the samples; ohmic contact was made to the back surface prior to implant, using tin-nickel alloy for n-type substrates and indium solder for p-type substrates. The C-V characteristics of the surface barrier diodes were measured at a bridge frequency of 100 kHz. A typical $1/C^2$ versus V curve for diodes formed on an n-type substrate with background concentration equal to $1.5 \times 10^{17}/cm^3$ is shown in Fig. 16. For both p- and n-type substrates the C-V data indicated the presence of a semi-insulating layer between 0.56 and 1.1 μm thick. The thickness data (measured by the capacitance-voltage method) are compared in Fig. 17 with the theoretical depth distribution profile of the protons as determined by the LSS theory.[15] The thickness of the I-layer was found to be greater in substrates with lower background impurity concentration, probably because fewer defect centers/cm^3 were required to fully compensate the substrate material. The point at 0.68 μm was checked by angle-sectioning and staining the sample. The I-layer was clearly visible in contrast to the p-type substrate material which stained dark after etching with 6 parts HNO_3 to 1 part H_2O; the apparent thickness of the layer was approximately 0.6 μm. Thus relatively good agreement exists between the values of I-layer thickness determined by the two different measurement techniques.

The C-V data for diodes formed on n-type substrates also indicated a rather surprising apparent peak in carrier concentration at a depth equal to the thickness of the semi-insulating layer. In some cases this peak concentration exceeded the substrate doping concentration by a factor of as much as 2 to 3. (The concentration peak corresponds to the flattened portion of the $1/C^2$-V curve of Fig. 16 in the range of 0 to 2 V bias, since carrier concentration is inversely proportional to the slope of the curve. For bias

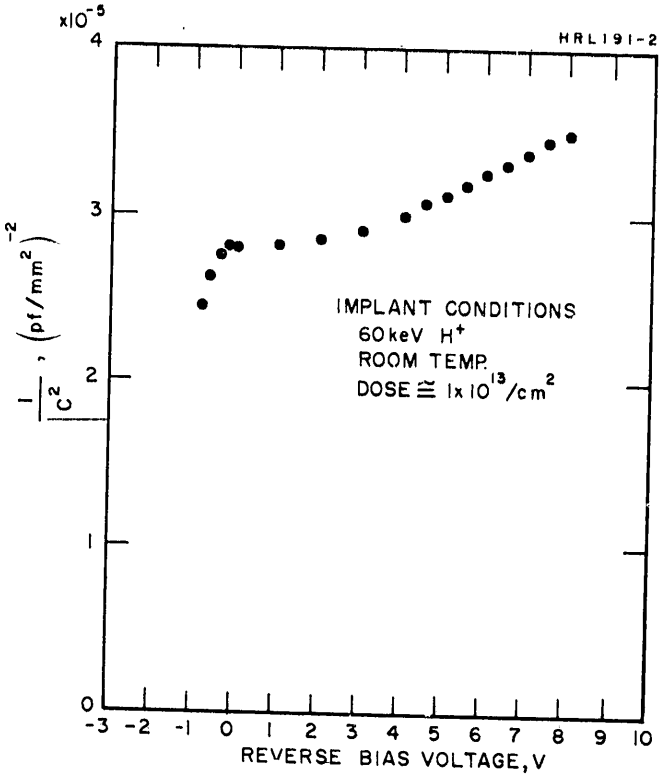

Fig. 16. $1/C^2$ versus V for a reverse biased Schottky diode formed on a proton-implanted GaAs substrate.

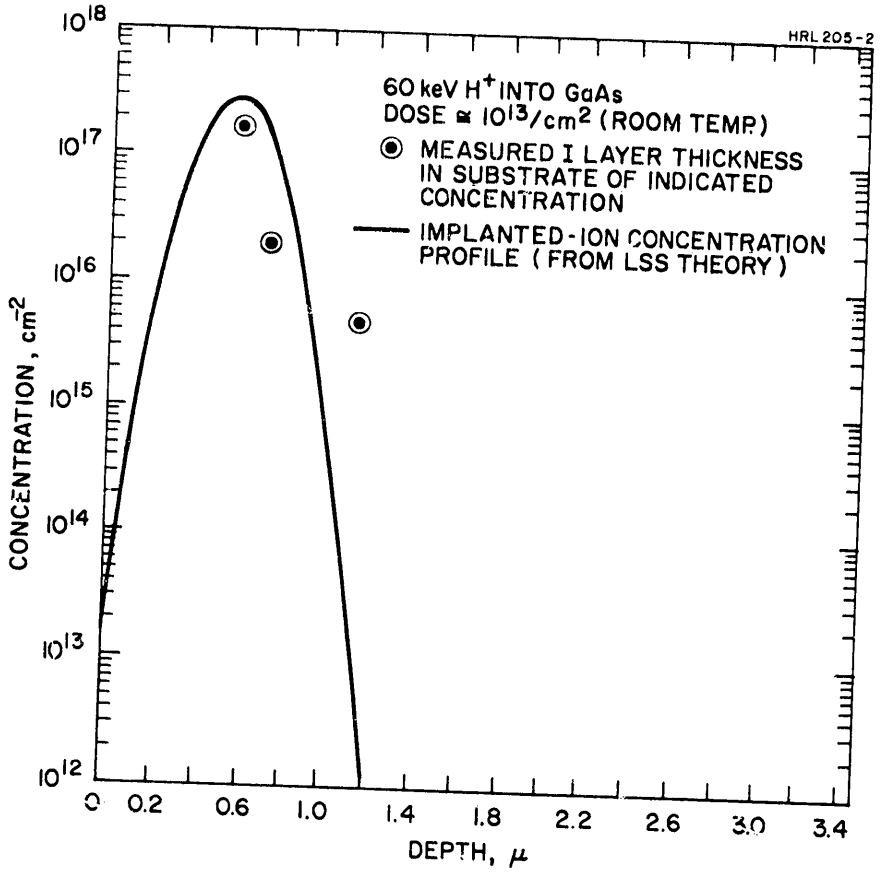

Fig. 17. Thickness of the semi-insu ating layer in proton-implanted GaAs as a function of substrate background doping concentration.

values greater than 3 V, the slope of the curve correctly indicates the substrate background doping concentration.)

The forward bias V-I characteristic is plotted in Fig. 18 for this same diode. Again the results are indicative of the presence of a semi-insulating layer, with forward current having a power law dependence rather than the exponential behavior that would be expected from a normal Schottky barrier diode. For voltages greater than about 0.1 V the current varies as V^4. This is the same dependence observed for zinc implanted diodes which contained a semi-insulating layer.[2]

D. VOLTAGE-CURRENT CHARACTERISTICS OF IMPLANTED DIODES

We have produced a number of ion-implanted GaAs diodes that exhibited good rectification characteristics, with unusually low leakage current, when operated at temperatures up to 300°C. The dc voltage-current characteristics of one of these diodes are shown in Fig. 19. The diode was made by implanting an n-type substrate ($n \approx 5 \times 10^{15}/cm^3$ at room temperature with a dose of $1 \times 10^{15}/cm^2$, 85 keV Zn^+ ions and subsequently annealing at 650°C for 3 hours. Prior to anneal the sample was coated with SiO_2 (to prevent substrate dissociation and vacancy generation). A mesa diode (area = 1.75 mm^2) was formed by etching. Contact to the p-type implanted layer was made using a gold probe, and the n-type substrate was contacted through a nickel-tin alloy pad. The dc V-I characteristics under reverse bias showed a smooth increase in current with increasing voltage up to breakdown (see Fig. 19). The breakdown voltage was 25 V, remaining relatively constant as operating temperature was changed in the range 23° to 300°C. The leakage current at 10 V reverse

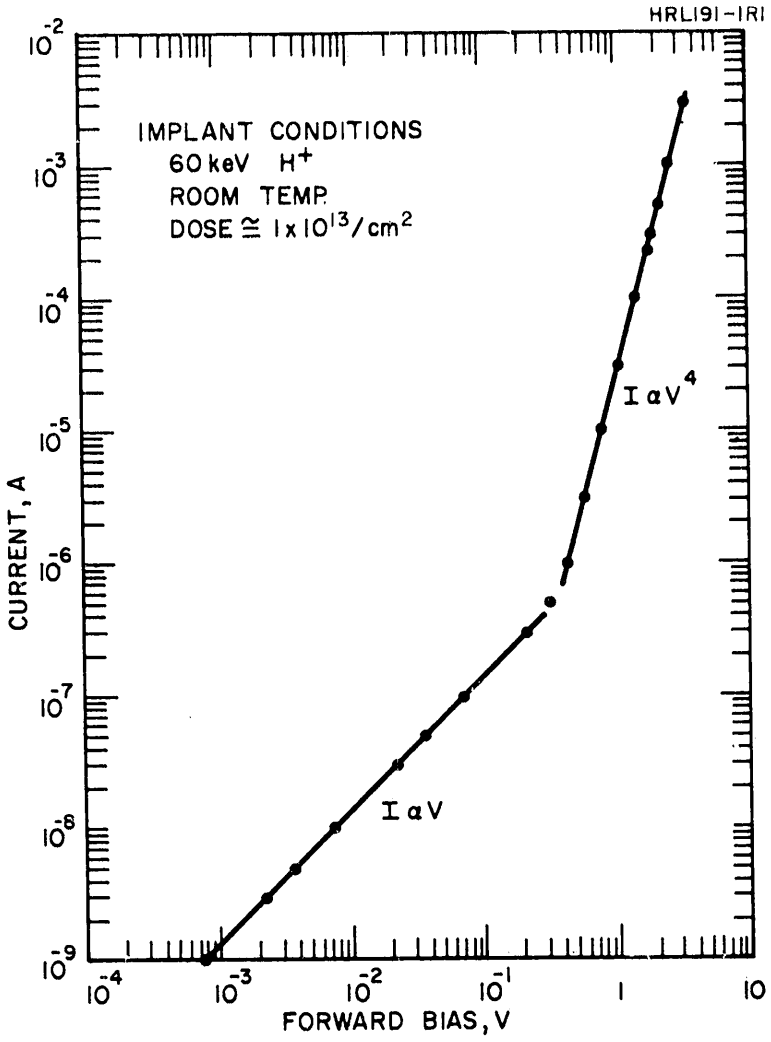

Fig. 18. V-I characteristic of a forward biased Schottky diode formed on a proton-implanted GaAs substrate.

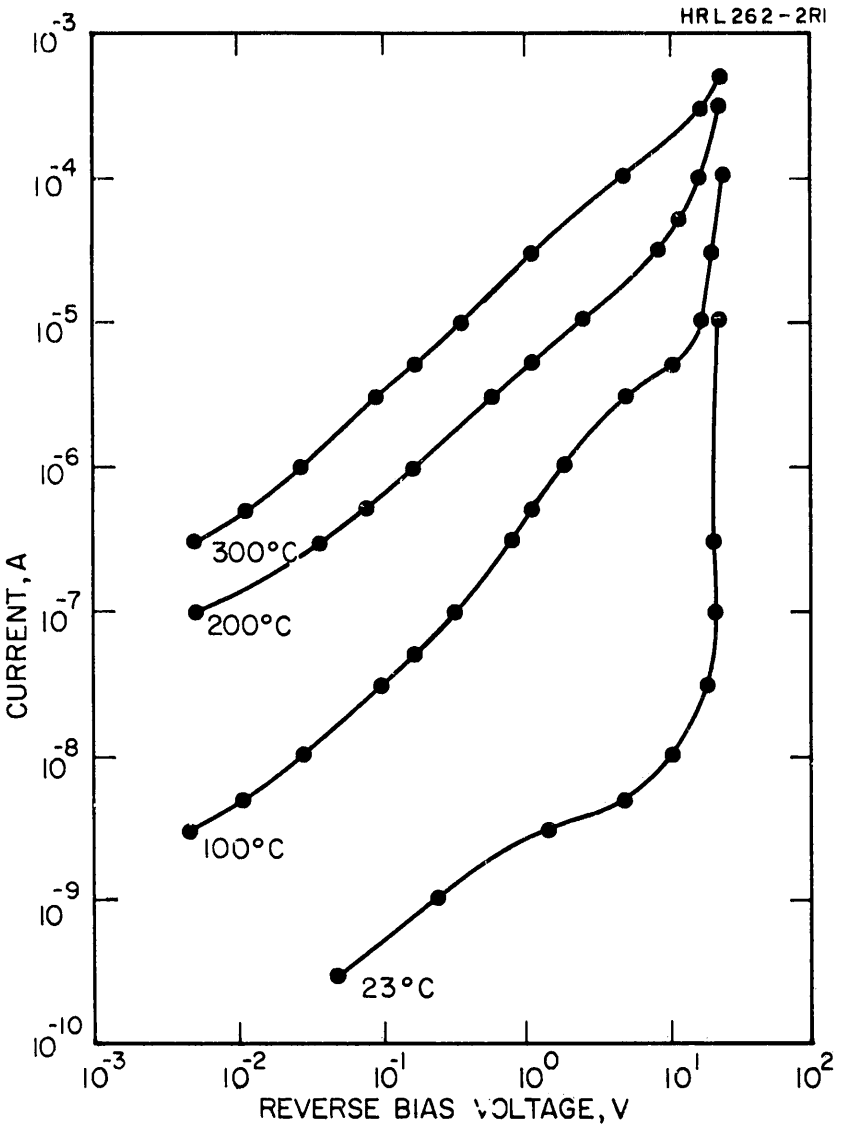

Fig. 19. Reverse bias V-I characteristics of a Zn-implanted diode at high temperature.

bias was 10^{-8} A at room temperature and increased to 2 x 10^{-4} A at 300°C. This leakage current is significantly less than that observed for GaAs diodes prepared by diffusion or by iso- and hetero-epitaxial vapor growth techniques.[28]

For conditions of forward bias, as shown in Fig. 20, the current-voltage relationship could be described over several orders of magnitude of current by the familiar expression $i = I_o [\exp (eV/nKT) - 1]$, with $1 \leq n \leq 2$. The current limiting effect of series resistance was observable for current above approximately 10^{-4} A.

It should be noted that this diode does not represent the best that can be made by ion implantation. For example, C-V measurements indicate that this diode contains a semi-insulating layer of the type that has been described in Section II-C. The semi-insulating layer contributes to the forward resistance of the diode and also may contain generation centers that increase reverse leakage current. Diodes annealed at 800°C or above (to eliminate the I-layer) can be expected to have lower forward resistance and possibly less leakage current.

E. IMPROVEMENTS IN PROCESSING AND FABRICATION TECHNIQUES

1. Stripping of Ion Implanted Layers

A method for thin-sectioning of ion implanted layers is currently being perfected under a Hughes Research Laboratories sponsored program in collaboration with Dr. Hugh Garvin. Because the technique promises to allow profiling of implanted-ion distributions, we believe it should be reported in connection with this contract program.

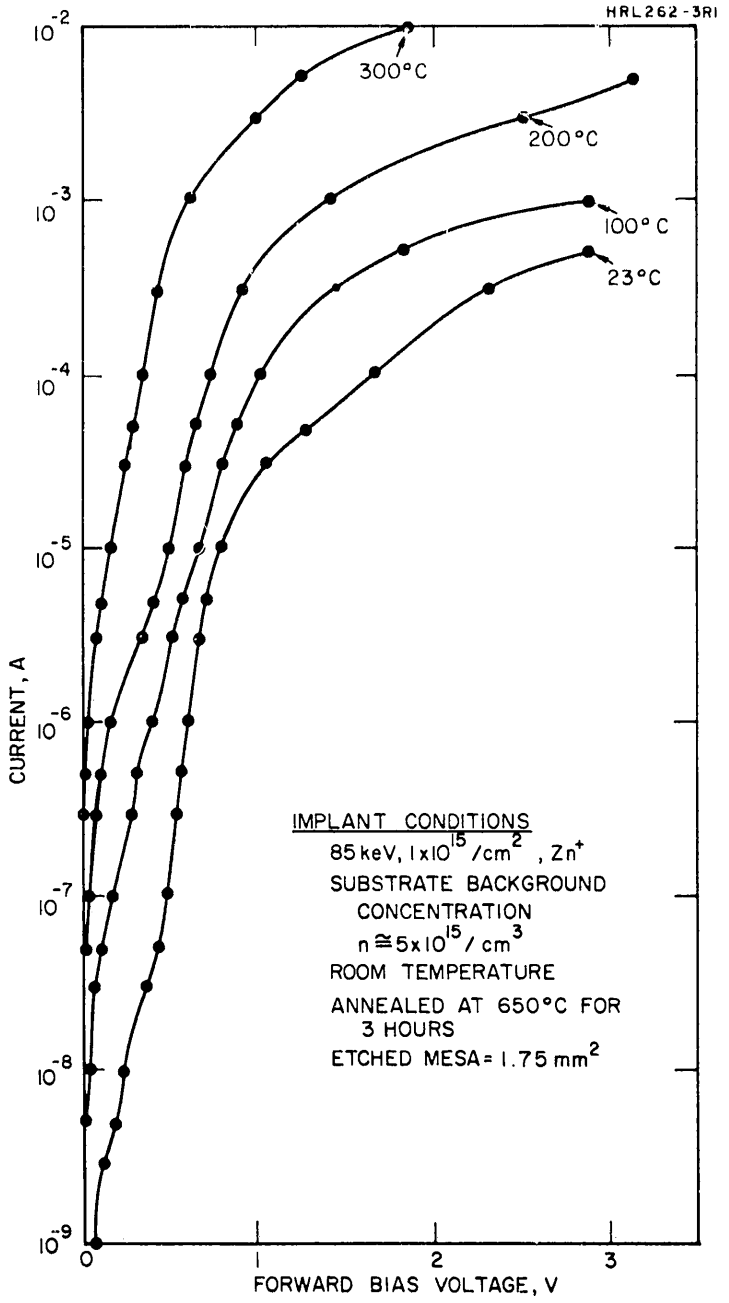

Fig. 20. Forward bias V-I characteristics of a Zn-implanted diode at high temperature.

The thin-sectioning is accomplished by sputtering off surface material from the ion-implanted substrate by bombarding it with a relatively high current beam of low energy argon ions. Using this method we have made Hall measurements of sheet resistivity ρ_s, surface carrier concentration N_s, and mobility μ as functions of layer removal from a GaAs substrate which had been implanted with a dose of $1 \times 10^{14}/cm^2$, 60 keV Cd^+ ions at room temperature and subsequently annealed at 800°C for 10 min to produce electrical activity. The implanted layer was removed in steps of 150 Å by sputtering with a $\approx 200\ \mu A/cm^2$ beam of 2 keV argon ions for 5 min (per step). The values of ρ_s, N_s, and μ measured after each layer removal step are shown in Table I.

TABLE I

Carrier Profile

Thickness Removed, Å	ρ_s, Ω/□	N_s, cm^{-2}	$cm^2\mu$, cm^2/V-sec
0 —	815	1.03×10^{14}	74.5
150	2,520	4.19×10^{13}	59
300	5,150	2.7×10^{13}	45
450	10,000	3×10^{13}	20.8
600	13,000	5.3×10^{13}	9.05
750	not measurable		
750 (After anneal, see text)	7,300	1.87×10^{13}	45.7

T5

The thickness removed was determined by measurement with an interference microscope. The steady decrease in mobility with layer removal and the anomalous increase in N_s after removal of 450 Å of material both apparently result from damage introduced by the argon ion sputtering. They are not characteristic of the originally implanted (and annealed) cadmium-doped layer. The damage produced by the 2 kV ion sputtering was not very persistent. It diminished significantly (as evidenced by increasing mobility) when the sample was annealed for one hour at 500°C following the removal of 750 Å. At present we are quite optimistic that a suitable sputter-stripping procedure can be developed which will eliminate sputter-ion damage and allow measurement of the true electrical characteristics of the ion implanted layer as a function of depth. For example, 2 keV argon ion sputtering for layer removal, followed by annealing at 500°C for 2 or 3 hours, may be sufficient to produce a thinned but undamaged ion implanted layer. In any case, the data of Table I indicate that low energy ion sputtering is a useful method of tailoring the resistivity of ion implanted layers, and hence merits further investigation.

2. Surface Protection Techniques

Our usual methods of providing surface protection against outdiffusion or decomposition during annealing are to coat the sample with a thin film of SiO_2 by either sputter deposition or chemical reaction of tetraethyl orthosilicate. These techniques work well, but the coating process is time-consuming when a number of processing steps are required as in bipolar transistor fabrication. For that reason we evaluated a new coating technique in which the SiO_2 film is spun on, using a photoresist-type spinner. The coating material is a low viscosity alcoholic solution (manufactured

by Emulsitone Co., Livingston, N.J.) which forms hydrous SiO_2 when applied to a surface in air. We found that films (1000 to 6000 Å thick) could be formed quickly by this method, but that they were generally inferior to those deposited by sputtering or thermal decomposition of tetro ethyl ortho silicate (TEOS); more pinholes were present and adhesion was not as good.

SECTION III

ION IMPLANTATION STUDIES IN SiC

A. EXPERIMENTAL

1. Substrate Material

Crystals of SiC were obtained from Westinghouse Astronuclear Laboratory, the Carborundum Company, and Stanford Research Institute. Most crystals were platelets of the 6H polytype of α-SiC. A few were of the 3C or β variety, and some unidentified poly types were observed. p-type crystals typically were doped with aluminum and n-type crystals with nitrogen; both types to a level on the order of $10^{18}/cm^3$. Implantations generally were made into crystal faces that were cleaned in acids but were not otherwise altered. However, some crystals exhibited obvious surface inhomogeneities, which were removed before implantation by polishing, oxidation, etching in molten Na_2O_2, or combinations of these processes.

Certain crystal inhomogeneities are not immediately obvious. We have observed, using Coates-Kikuchi patterns, that opposite faces of many of the crystal platelets have entirely different stacking orders rather than appearing as just A and B faces of a single polytype. Barrett[29] has recently reported similar observations on SiC. We have observed this on as-grown material as well as on samples where one face has been optically polished and cleaned by oxidation and oxide removal. A study of the subtle effects of polytypism upon evaluation of ion implanted layers has not been attempted under this program.

2. Ion Implantation

a. Implantation Procedure – Implantations into the SiC crystals routinely were performed in a vacuum in the low 10^{-6} Torr range, or better, by using a mass-separated beam. The beam incidence angle was such that both channeled and random angle implants were made on various crystals. The majority of implantations have been made with no special effort to enhance channeling. The ion beam was swept over the substrate to insure homogeneity of the implanted layers. Ion dose for the implantation levels used has been measured with 20% accuracy, and implant energies have ranged from 5 keV to 300 keV. Ions implanted at constant energy result in a Gaussian distribution if channeling is neglected. This requires multiple implants to approximate a linear distribution. For example, Fig. 21 shows the predicted profile[15] for a double nitrogen implant of $10^{15}/cm^2$ at 84 keV and $10^{15}/cm^2$ at 25 keV. The profile is far from linear, but can be considered as approximately $10^{20}/cm^3$ throughout the region of peak concentration. The degree of linearity can be improved by using a greater number of implant steps. Substrates customarily were held at room temperature during implantation although some were maintained at 500°C.

b. Channeling Technique – The study of ion channeling in crystalline targets requires accurate alignment (less than 0.1°) of a major crystallographic axis of the crystal with the ion beam. In order to accomplish this alignment, it is necessary to determine the angle between the beam and the crystal axis; i.e., the θ, ϕ coordinates of the axis with respect to the beam. At these settings of θ and ϕ, the beam is then aligned with the crystal axis. Figure 22 shows the goniometer built by this laboratory to control these values to within 0.02°.

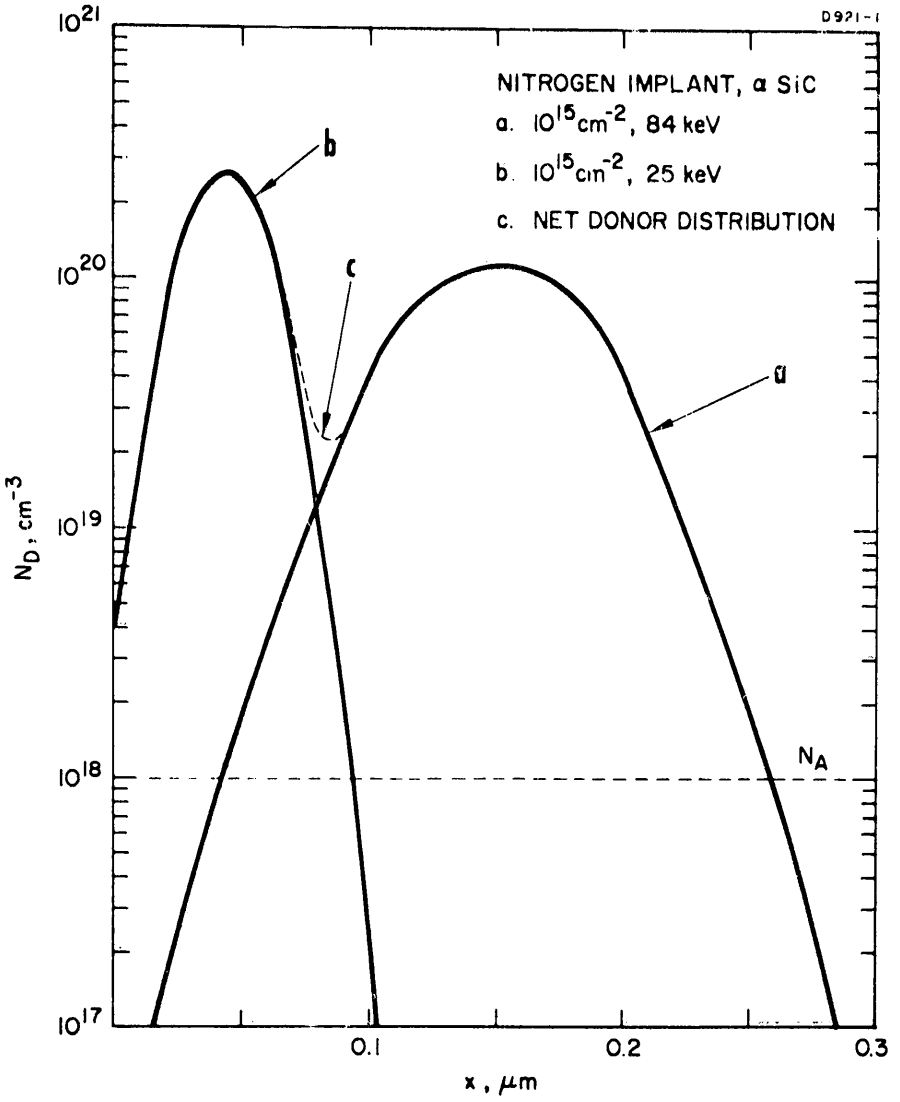

Fig. 21. Theoretical distribution of nitrogen ions implanted in SiC. Junction depth seen to by 0.26 μm with presumed bulk doping of 10^{18} cm^{-3} acceptors. (Calculation, courtesy H. Schiøtt.)

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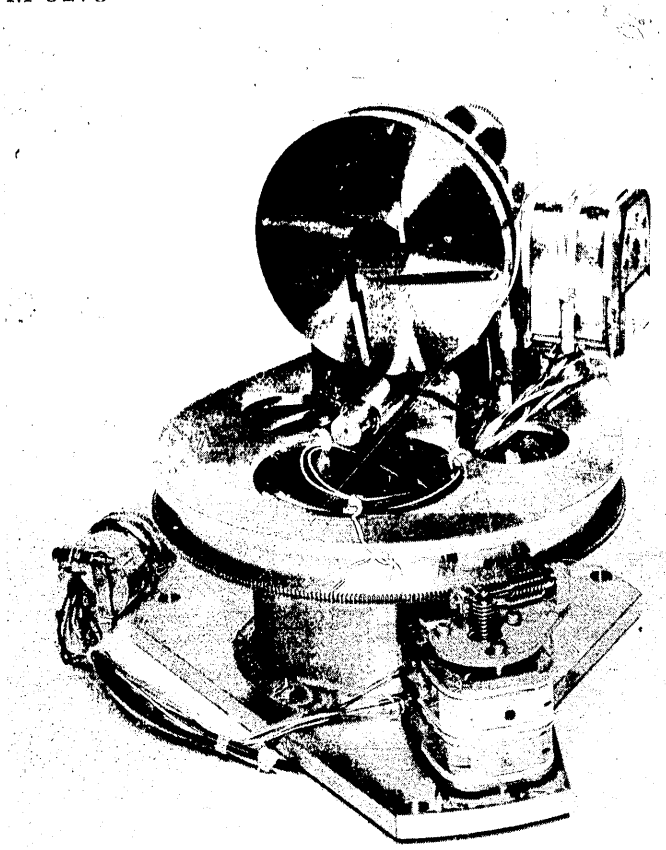


Fig. 22. Crystal goniometer constructed for use with the channeling apparatus.

The technique for determining the coordinates of the crystal axis is based on the measurement of the decrease in backscattered proton yield as the major crystal planes are rotated through a proton beam.[30] For detection of the backscattered protons, a surface barrier detector (7 keV FWHM) is located about 10 cm from the goniometer face, as shown in Fig. 23. The pulses from the detector are first amplified and then discriminated to remove low energy pulses. They are then counted by a count-rate meter whose output is monitored by a strip chart recorder. A 400 channel analyzer in parallel with the count-rate meter gives the energy spectrum of the backscattered protons.

The backscattered yield as a function of azimuthal angle ϕ at constant tilt angle $\theta = 3.5°$ is shown in Fig. 24 for 140 keV protons incident on the {111} face of a silicon crystal. The discriminator is adjusted to permit only protons scattered near the surface to be counted. Distinct dips or decreases are observed whenever a major crystal plane is rotated through the beam. The most pronounced dips ($\sim$3:1) correspond to {110} planes, and the smaller dips correspond to {112} planes.

A polar coordinate plot showing the {110} planes is given in Fig. 25; the intersection of these planes locates the <111> axis with respect to the center of rotation, which is aligned with the beam axis. In this case the coordinates of the <111> axis are $\phi = 270°$, $\theta = 0.9°$. At these settings the beam is aligned with the <111> axis to less than 0.1°. However, in order to tilt through the <111> at various values of ϕ, the front face of the goniometer is adjusted <u>in situ</u> to bring the <111> axis into coincidence with the center of rotation. The dashed lines in Fig. 25 represent the adjusted positions of the {110} planes, showing that the <111> is at the center of rotation and thus aligned with the beam at $\theta = 0$ for any value of ϕ.

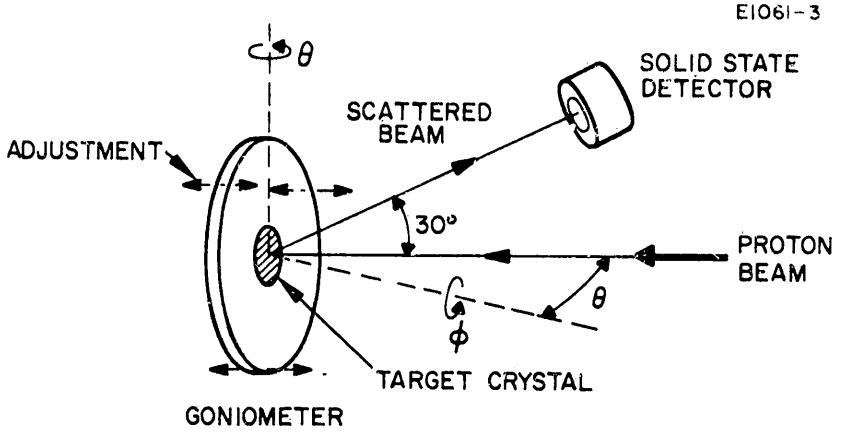


Fig. 23. Schematic of scattering assembly used for backscattering analysis and alignment of the target crystal.

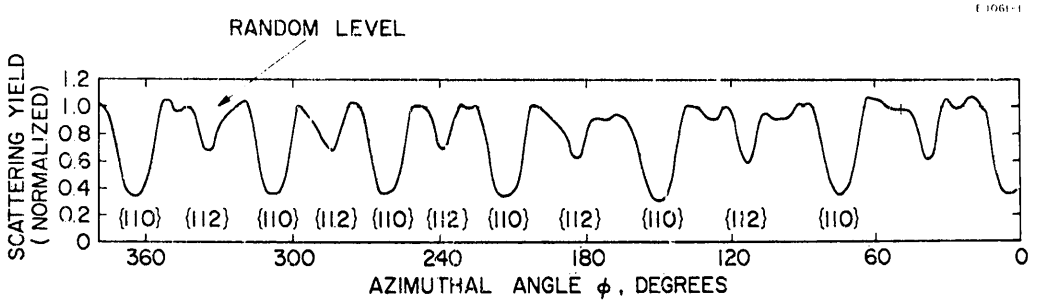


Fig. 24. Scattering yield as a function of ϕ at constant $\theta = 3.5°$ for 140 keV protons incident on the {111} face of silicon. The major planar dips are indicated.

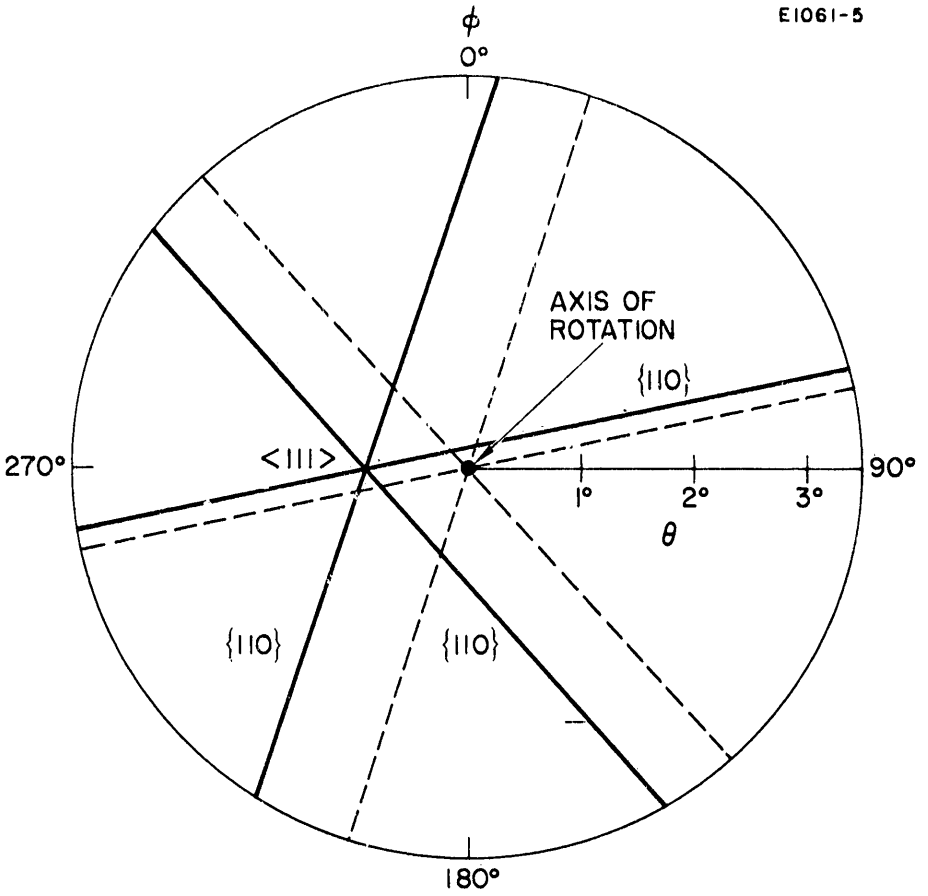


Fig. 25. Polar coordinate plot of the data in Figure 5 showing the {110} planes (solid lines). The interaction of the planes determines the coordinates of the <111> direction (ϕ = 270°, θ = 0.9°). The dotted lines represent adjusted positions of the {110} planes showing that the <111> is at the center of rotation O.

After alignment has been achieved, it is then possible to perform either channeled implants or aligned H or He ion backscattering analysis.

3. Disorder Annealing

a. Annealing Procedure – To remove the implantation-caused damage and restore the crystalline quality of the lattice and the attendant semiconducting qualities, it is necessary to anneal the sample.

As a precaution against oxidation, annealing at temperatures of 1300°C, or below, was done in a nitrogen atmosphere. A vacuum of 2×10^{-6} Torr, or better, was used at temperatures up to 1800°C in order to prevent nitrogen diffusion as well as crystal oxidation.

The vacuum annealing oven consisted of two wide carbon heater strips a few millimeters apart, with the crystal sandwiched between them. The sample essentially was surrounded by the heater walls, but was in contact only on the side opposite the implanted surface. Vacuum conditions were kept at 2×10^{-6} Torr or less by an ion pumped system in order to reduce oxidation.

b. Decomposition – While undergoing vacuum annealing, the surface of SiC had been observed to decompose at temperatures as low as 1600°C. This decomposition results in an increased surface conductivity which confounds the measurements of the implanted layer characteristics.

Figure 26(a) shows the effect of vacuum annealing on the surface of a diode. The high leakage current is obvious when comparison is made with the cleaned diode shown in Fig. 26(b).

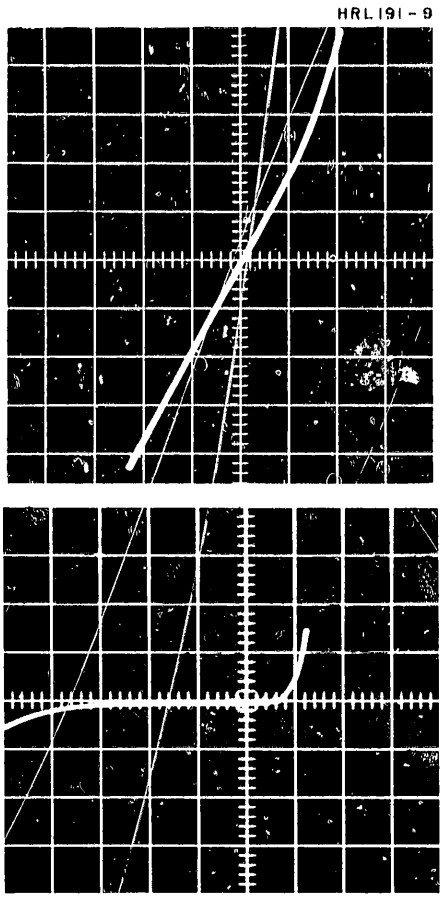


Fig. 26. Current-voltage trace of nitrogen-implanted diode showing effects of decomposed surface and oxidation.

Some ineffective attempts to prevent this surface decomposition by geometric means were described in Quarterly Progress Report No. 8. A method effective on GaAs was using a coating of SiO_2 as a surface container, but this material has too low a melting point to be useful on SiC. This suggests the possible use of covering films of aluminum oxide and silicon nitride. These films were applied using a sputtering process.*

An n-type crystal was prepared with part of the surface unprotected, while the other areas covered with the Al_2O_3 and Si_3N_4 films. The crystal was then heated for 2 min at 1200°C in a vacuum of 5×10^{-7} Torr. The alumina film cracked and peeled severely, and there appeared to be an excessive mismatch of expansion coefficients. Visual inspection revealed no change in the nitride films, and there was no darkening of the uncovered crystal.

The crystal was then heated for 2 min at 1600°C in vacuum. This darkened the unprotected surface of the crystal, indicating surface decomposition. The nitride-coated area was considerably darker, and appeared to have undergone accelerated decomposition.

Since the use of protective films was not effective, it was necessary to examine the decomposition and to eliminate its residue. A sample of p-type α-SiC was given a multienergy nitrogen implant. The implants were all done at room temperature, and dose and energy values were as follows: 10^{15} ions/cm^2 at 300 kV, 10^{15}/cm^2 at 100 kV, and 5×10^{14}/cm^2 at 40 kV. These parameters were chosen so that the net concentration of donors would be distributed evenly throughout the implanted region, with an average concentration of

*We are indebted to Hugh Garvin for these films.

about $10^{20}/cm^3$. The substrate crystal was doped with aluminum and clearly showed bands of varying doping densities, but was considered to have a medium doping level. The crystal was supplied by John Shier of NASA ERC; he had optically polished and oxidized the crystal from the Carborundum Company to insure a clean, damage-free $(000\bar{1})$ surface. We then cleaned this surface of oxides and used it for the implantation.

Because the substrate doping level is not known, the depth of the implanted p-n junction cannot be predicted accurately; however, a rough estimate is that the implanted region is 0.6 μm thick if the substrate doping is of the order of $10^{19}/cm^3$, as might be indicated from the color of the sample.

As in previously implanted samples, the implanted area was darkened and easily distinguished from areas masked during implantation. The condition of the darkened area is from heavily damaged to amorphous, and soldered contacts did not function adequately to permit sheet resitivity or Hall voltage measurements.

Annealing this sample at 1000°C in vacuum changed the surface so that ρ_s was determined to be about 1.8×10^4 Ω/□, although a Hall voltage still could not be obtained. A strong photocurrent was obtained under ultraviolet illumination, indicating that a p-n junction had been created in the crystal although the surface of the implanted region was still greatly disordered.

After annealing at 1300°C, Hall measurements could be obtained to evaluate carrier concentration and mobility, as well as sheet resistivity. Table II summarizes the average values of data obtained after each annealing stage and surface cleaning treatment.

TABLE II

Data Summary-Decomposition

Anneal Temperature, °C	ρ_s, Ω/□	V_H/I	N_s, ion/cm^2	μ, cm^2/V-sec
1100	1.78×10^4	—	—	—
1300	6.4×10^3	—	—	—
O_2 bake	7.4×10^3	—	—	—
1400	2100	0.765	7.4×10^{14}	4.0
O_2 bake	2200	0.68	8.2×10^{14}	3.4
1500	553	0.430	1.3×10^{15}	8.7
O_2 bake	612	0.48	1.15×10^{15}	8.9
1600	315	0.51	1.1×10^{15}	18.0
O_2 bake	478	0.46	1.2×10^{15}	12.0

T22

Data denoted as, O_2 bake, in the above table were taken after the initial measurements of the sample at each anneal stage, and after the sample was baked in oxygen for about 15 hours at 500°C. Further oxidation caused no change in surface measurements. Studies of oxidation of SiC have shown that this substance will not oxidize measurably at this low temperature.[31,32] The effect of this treatment is seen more clearly after the higher temperature anneals. If the layer were of silicon, which might oxidize at this low temperature, the resulting SiO_2 probably would be seen as an insulating layer which would interfere with making contacts to the SiC. Such difficulties were not observed. We infer that the oxygen bake is burning off a carbon layer

left on the surface by the anneal cycle. The sample is routinely annealed in vacuum of about 10^{-6} Torr while sandwiched between two graphite heater strips. Because the vapor pressure of carbon is on the order of only 10^{-10} Torr at 1500°C, we believe the carbon layer on the SiC is the result of decomposition of the SiC with silicon boil-off, and is not deposited from the heater strips. Further evidence supporting the argument for decomposition is presented in Section III-B.

Surface data taken for anneal temperatures of 1400°C and below are essentially unaffected by the decomposition, while above that temperature the increased surface conductivity serves to inflate mobility values.

The decomposition at temperatures of 1500 °C or above also affects measurement of device characteristics in that a clean p-n junction diode will be essentially shorted out by the carbon layer. Figure 26 shows the V-I characteristics of such a diode immediately after annealing and then after the oxidation treatment. Clearly the decomposed layer must be removed before diode characteristics can be examined.

c. Oxidation of Implanted SiC – Oxidation of SiC has been studied by many investigators,[31,32] but most of the work was done on granular SiC and data were therefore averages of crystal orientation effects. Work on single crystal SiC has indicated that the growth of SiO_2 is more rapid on the silicon face than on the carbon face.[33] Work has been done on silicon[34] showing that the doping level of the substrate affects the rate of oxidation. To determine the effect, if any, of doping on the oxidation rate of SiC, a crystal was prepared with both a low- and high-dose implant. Part of a p-type, α-SiC crystal, grown with about $2 \times 10^{18}/cm^3$ aluminum atoms was implanted with $5 \times 10^{13}/cm^2$ nitrogen

ions at 30 keV. Another area of this same crystal was given a double implant of 10^{15} N^+/cm^2 at 100 keV and 5 x 10^{14} N^+/cm^2 at 40 keV. Following the room temperature implantations, the crystal was annealed at temperatures to 1700°C. As shown later, implanted regions are considered to be completely annealed after the 1700°C cycle, and damage effects will be negligible. Oxidation was then carried out in dry oxygen at 1200°C for 4-hour periods. The crystal underwent three such periods, and the amount of oxidation was estimated by observing the interference colors which have been fairly well calibrated as to color-thickness relationship.[36] Before each oxidation, the sample was washed in HF so that a clean surface would be presented to the gas.

After each cycle the highly doped region was a brownish-purple, the lightly doped region was yellow-brown, and the nonimplanted areas had no detectable change in color. From this we infer that while the nonimplanted SiC did not oxidize, the implanted regions oxidized in proportion to the dose. The interference colors remained the same after each of the three cycles, and corresponded to oxide thicknesses of about 900 Å and 500 Å. SiO_2 grown on SiC is essentially twice as thick as the layer of SiC which is incorporated into the film.[36] This means that while a total of 2700 Å oxide was grown on the highly doped region and 1500 Å on the lightly doped one, only 1350 Å and 750 Å of SiC were removed from the respective regions. Interferometry confirmed the existence of a 600 Å step at the border between the two regions of different implant dose.

Jorgenson, Wadsworth and Cutler[32] reported that the oxidation rate was not affected by impurity concentration (for rather impure stock). While our measurements are inexact at present because of the small dimensions involved

and the subjective quality of color description and interpretation, we believe the results are good qualitative data and suggest the need for more study to determine the influence of doping concentration on oxidation rate. Even though some of the implanted regions may be highly susceptible to oxidation, we feel that our annealing procedures did prevent oxidation, although surface decomposition remains a problem.

4. Measurement Procedures

a. Etching – As discussed by Johansson, et al.[37] the implanted layer must be electrically isolated from the bulk crystal before meaningful measurements can be obtained. The p-n junction formed by donor implantation into p-type substrates provides this isolation. To reduce leakage current and to define areas under study, we have used electrolytic etching.[36] While this etchant can be used only on p-type material, the implanted n-type layers are thin enough to fracture away, causing a cleaved-etched condition in the vicinity of the junction, with a resultant low leakage current. With appropriate masks, this same process serves to form small mesas for use as diodes for examining the characteristics of the p-n junction.

Sputtering in a low pressure argon atmosphere was tried in an attempt to remove SiC which was too poorly annealed to support electrolytic etching. The SiC was removed cleanly, but the newly exposed surface was observed to be n-type upon subsequent annealing. Trace nitrogen in the argon sputtering beam was suspected, and the process was not refined for dependable use.

Molten Na_2O_2 has been used to remove large amounts of crystal, but this leaves a pitted and unevenly etched surface and was avoided when feasible.

b. Contacts to Implanted Layers -- Point contacts usually will serve for quick examination of measurements made on surfaces with a sheet resistivity on the order of 1000 Ω/□. Accurate measurements require more intimate contact. Shier[38] has discussed alloy contacts to SiC, but these were considered unsuitable for studies requiring repeated anneal cycles. For n-type layers with sheet resistivities on the order of 10^4 Ω/□ or less, we found that indium-silver alloy could be soldered in place and would perform adequately. Contacts to the p-type bulk were either broad-area soldered indium-silver or alloyed aluminum-silicon, applied after each anneal cycle.

c. Electrical Evaluation – Following a donor implantation in p-type SiC, several tests were used to verify the existence of a p-n junction: broad-area photovoltaic response to ultraviolet light, visible injection luminescence over a broad area, rectifying current-voltage curves, and confirmation by Hall measurement that the implanted layer was n-type. An implanted surface can be examined using a thermal hot probe,[39] but this instrument has been undependable on SiC except in the case of a high conductivity n-type layer. Hall measurements, made as discussed by Johanssen, et al.,[37] also determined the sheet resistivity and Hall voltage of the implanted layer. The number of active carriers and their average mobilities could then be calculated from these data. p-n junction qualities were examined by measuring diode current-voltage, capacitance-voltage and capacitance-frequency characteristics at operating temperatures from 23° to 400°C. These diodes were adjacent to the

larger areas used for Hall measurements to insure that both sets of measurements reflected the same implantation and annealing processes. The sample test mount was a large carbon block maintained at the desired temperature. The SiC sample was pressed firmly to this heat reservoir, which also served as the electrical connection to the alloyed contacts on the bulk SiC. Voltage measurements were made with a Keithley 610B electrometer, and currents were monitored by a Keithley 153 microvolt-ammeter. Junction capacitance was measured over a range of 5 to 500 kHz on either a Boonton Model 75A-S8 or 75C capacitance bridge.

5. Surface Considerations

A primary difficulty in the evaluation of p-n junction behavior is to assure that leakage currents do not dominate the I-V characteristics of the junction. The influence of leakage currents upon the analysis of I-V characteristics of SiC diodes is made strikingly evident in Fig. 27. Here, the current-voltage behavior of a nitrogen-implanted device, operating at 100°C, is shown after 1500°C anneal for two different surface preparations. Case A was taken immediately after the diode mesa formation using the anodization etch. Case B was obtained after surface cleaning with aqua-regia. In both cases the current-voltage behavior is closely approximated by

$$J = J_s \left(\exp \frac{eV}{kKT} - 1 \right) \qquad (1)$$

where $n = 2$ and J_s is different for the two curves. It is shown in Section B that the device behavior in condition B can be interpreted in terms of known diode behavior, whereas condition A cannot.

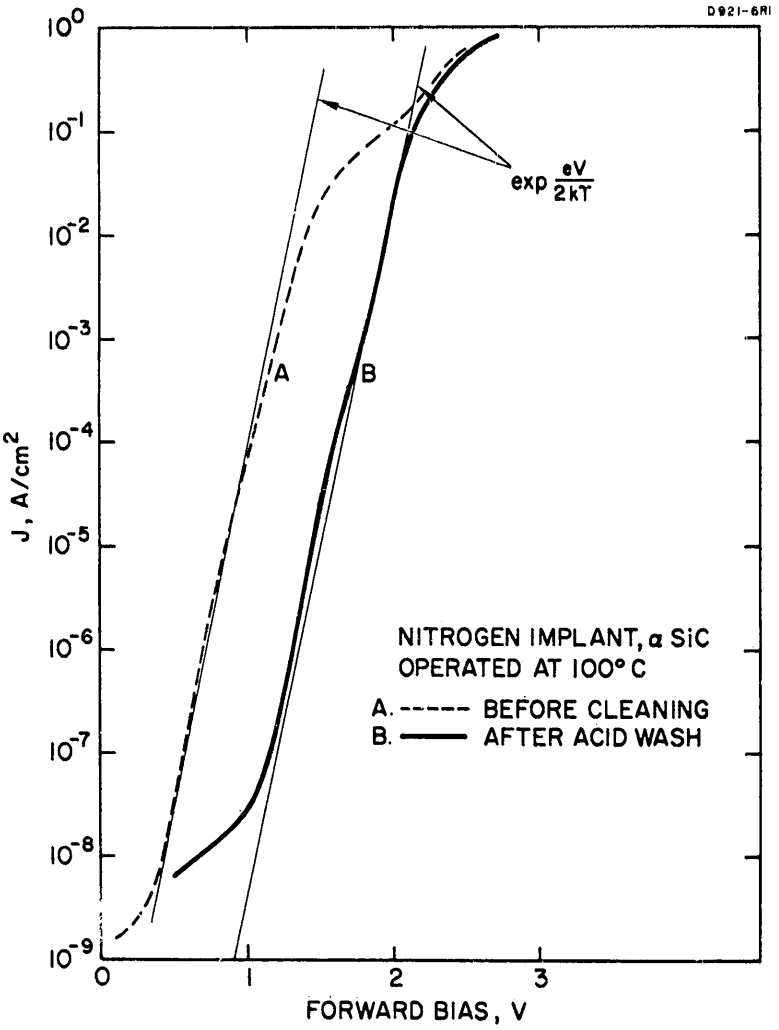


Fig. 27. Log J versus forward bias for a diode operating at 100°C after two types of cleaning processes. Curve A was obtained after the mesa diode was formed by anodization etch. Curve B was obtained after a subsequent surface cleaning with aqua-regia and has substantially reduced leakage currents.

Additional experiments are necessary to eliminate or control these leakage currents on a dependable basis. This is particularly necessary if incompletely annealed implanted junctions are to be examined with reasonable confidence.

One technique which can be used to determine the presence of surface leakage components is to measure the I-V characteristics as a function of temperature. The forward I-V of an ideal SiC diode is expected to be dominated by recombination current[40] which is proportional to the intrinsic carrier density. One therefore expects to observe $I_o \sim \exp((E_g)/(2\ kT))$. We have observed that this is not the case when leakage currents dominate.

6. Materials Characterization

Capacitance-voltage measurements of evaporated surface barriers have been used to evaluate the uniformity of carrier concentration in the SiC crystals.[41,42] Mead[41] has stated that a gold surface barrier can be constructed on SiC, and we have used this material in our investigation. A crystal of α-SiC which is doped to a level of 10^{17} nitrogen ions/cm^3 was chosen as being apparently homogeneous and having a smooth surface consistent with good masking and metal film deposition. Gold discs were evaporated on the surface, and C-V measurements were taken. Data were not similar for surface barriers at different locations on the small crystal, and surface contamination was suspected. All metallic substances were removed in aqua-regia, followed by washing with $HF\text{-}HNO_3$ combinations, to prepare the surface for more careful study.

A regular array of gold dots of 1.37×10^{-4} cm^2 diameter was evaporated onto the surface. Indium-silver solder was applied over a broad area of the opposite face to serve as

contact to the bulk. The crystal is approximately 2 mm x 3 mm and about 140 dots are evenly distributed over the surface. Except for the dots along the perimeter, C-V data are consistent and reproducible, and indicate that the crystal is not homogeneous.

For a carrier concentration which is constant with depth in the crystal (the condition of an unimplanted crystal) a plot of $1/C^2$ versus bias voltage should be a straight line, the slope of which is proportional to the carrier concentration. Figure 28 shows such a plot for two widely separated surface barriers, and the carrier concentrations to be inferred. If these lines are extrapolated to $1/C^2 = 0$, a diffusion potential of 1.75 V is obtained from the voltage intercept. The activation energy of nitrogen in hexagonal SiC has been determined as approximately 0.2 eV. Assuming this value for the Fermi energy, one obtains a barrier height of 1.95 V in close agreement with the value obtained by Mead.[41] In a survey, data for many other surface barriers were taken at zero bias and 1 V reverse bias. Calculations based on the voltage intercept and these capacitance values provide the values of N, rounded to two-figure accuracy (shown in Fig. 29), which indicate the nonhomogeneity of the crystal.

B. RESULTS AND DISCUSSION

1. Conduction Properties of Implanted n-Type Layers

a. Nitrogen Implants – Ion-implanted regions can be located more simply in SiC than in most semiconductors, because after room temperature implantation of any ion species used here the implant site is easily visible as a dark stain in the transparent crystal. For all of the ions investigated,

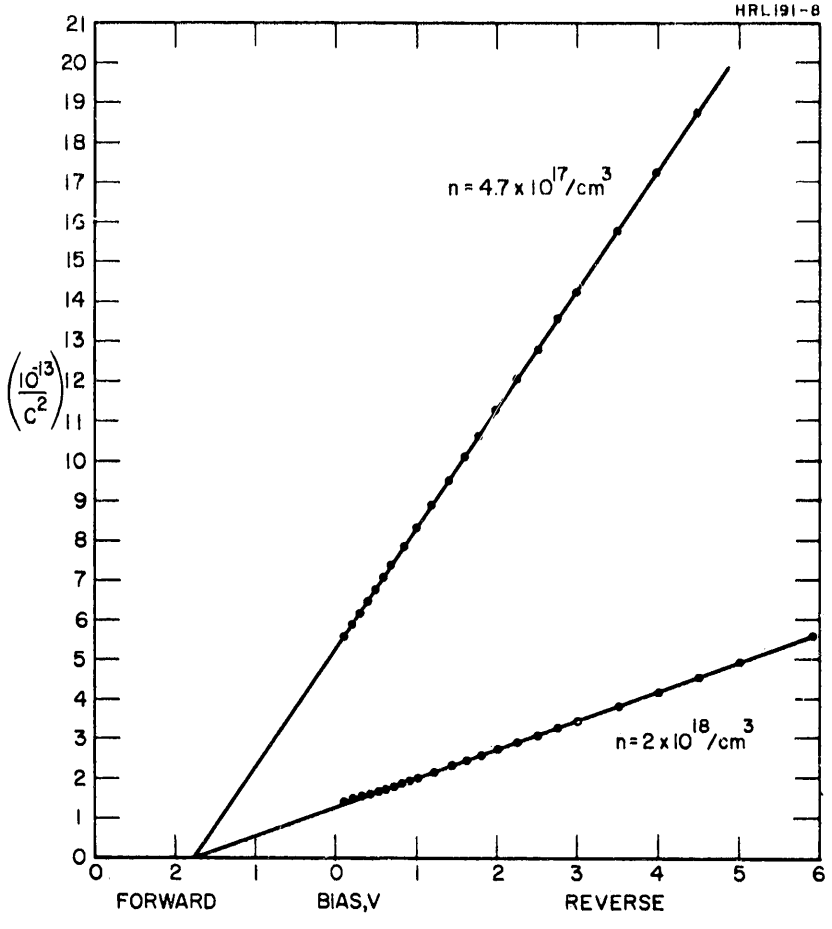


Fig. 28. $1/C^2$ versus V for surface barrier diodes on n-type SiC.

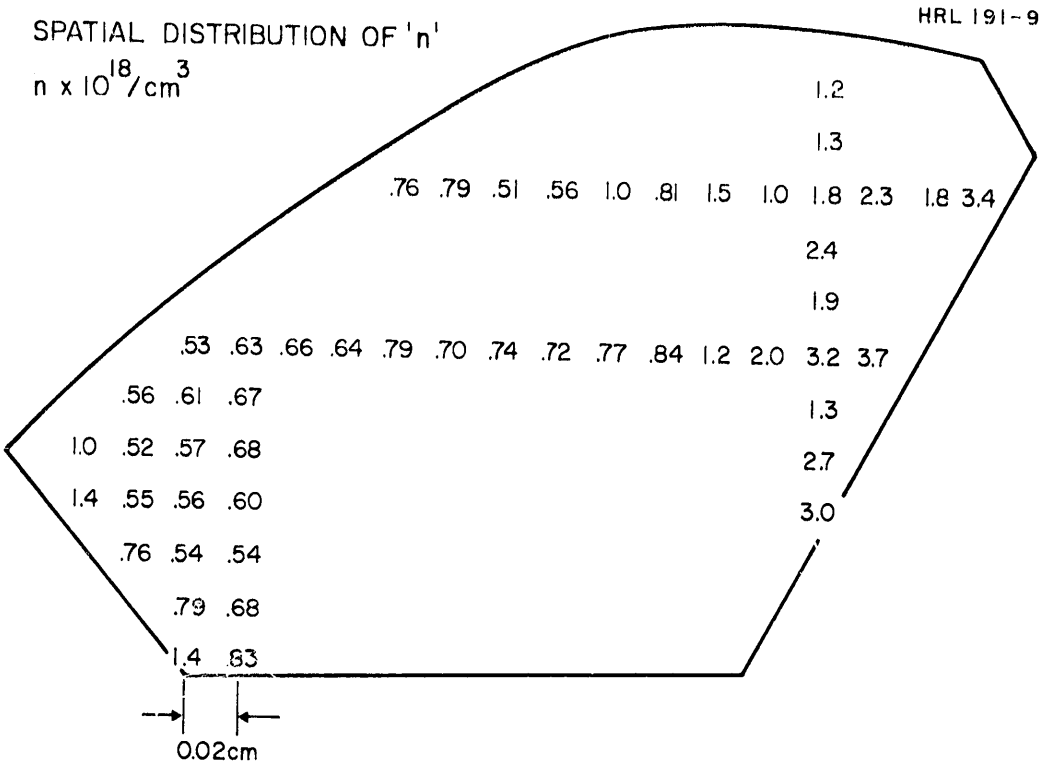


Fig. 29. Map of carrier concentration over crystal surface, as determined by capacitance measurements.

the implanted surface appeared to have very high resistivity immediately after implant. Annealing for 15 min in a nitrogen atmosphere at 500° to 1000°C substantially reduced the dark coloration observed after implantation, but did not eliminate it. The electrical behavior of the implanted layers appeared to be sensitive to the ion species following annealing in this temperature range.

A p-type SiC sample implanted with nitrogen at a dose of 10^{15} N^+/cm^2 at both 25 and 85 keV (see Fig. 21 for the predicted impurity distribution) showed a photoresponse to ultraviolet light after a 500°C, 15 min anneal in a nitrogen atmosphere. (We will refer to this sample as 77 A.) This suggested the presence of a p-n junction. Annealing at 750°C in nitrogen for 15 min produced positive indications of an n-type layer when tested with a thermal probe and uv photoresponse measurements. Annealing at 1100°C for 2 min in vacuum produced an n-type layer with a sheet resistivity that was sufficiently low that ohmic contacts could be made and Hall measurements performed. Current-voltage measurements from the implanted layer to the substrate revealed the presence of a p-n junction.

Studies of disorder annealing in SiC obtained from Rutherford scattering measurements, described in Section III-B-5, have shown that a substantial amount of annealing takes place after a 750°C anneal, particularly in the region of greatest depth where the p-n junction would be expected to form and that the lattice order is nearly completely restored after a 1100°C anneal.

The results of Hall effect and sheet resistivity measurements on this implant, as a function of annealing temperature for 2-min anneals in vacuum, are shown in Fig. 30(a). The notable features are that the number of donors measured is essentially constant with a value of one-half the implanted

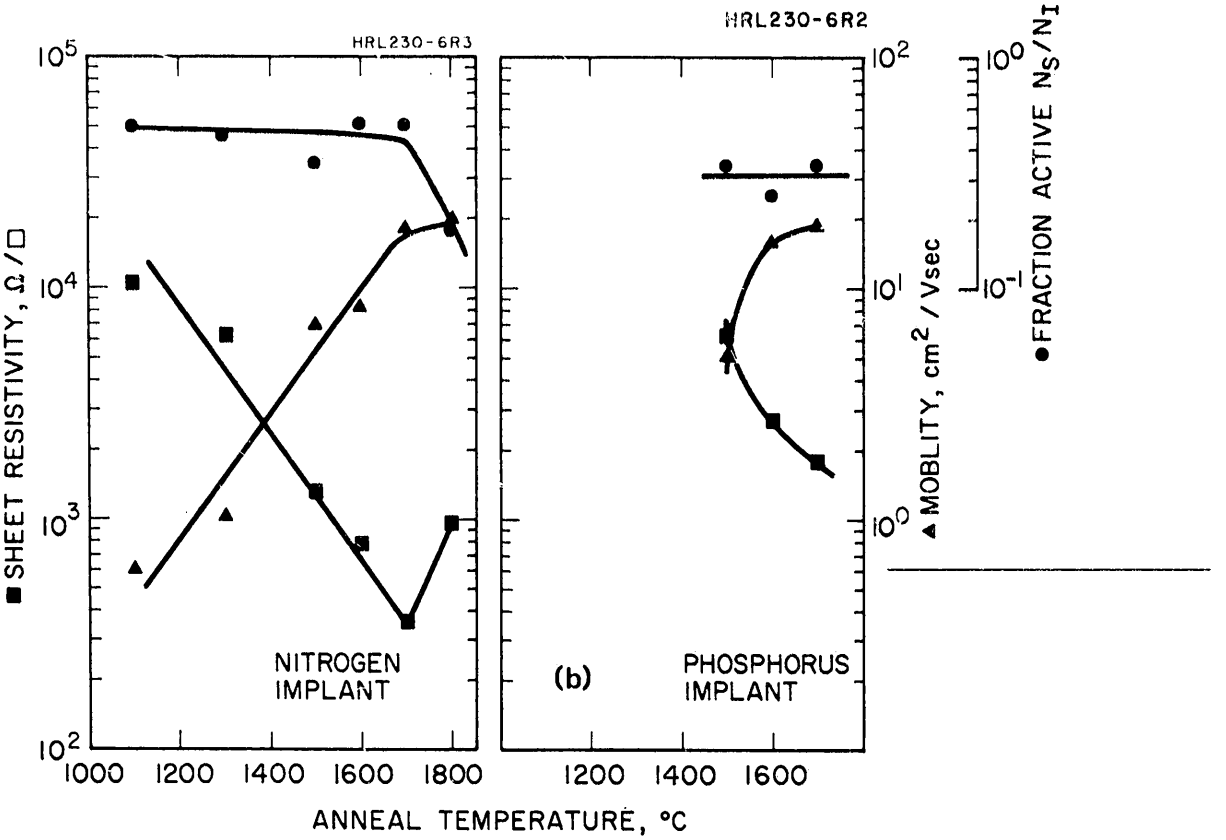


Fig. 30. Electrical carrier parameters of implanted ions in α-SiC versus annealing temperature. (a) With a nitrogen fluence of 10^{15} cm^{-2} at 84 keV and 10^{15} cm^{-2} at 25 keV. (b) With a phosphorus fluence of 5 x 10^{14} cm^{-2} at 145 keV and 10^{14} cm^{-2} at 50 keV.

nitrogen dose of 2 x $10^{15}/cm^2$ for anneal temperatures up to 1700°C, and that the decrease in sheet resistivity with increasing anneal temperature results entirely from an increase in the effective carrier mobility. The increase in carrier mobility with anneal temperature is probably associated with annealing of disorder in the implanted layer, although the backscattering measurements show little additional annealing taking place in this annealing temperature range. The decrease in donor concentration after anneal at 1800°C and the corresponding increase in sheet resistivity result from two factors: the loss of SiC surface due to dissociation at 1800°C, and the loss of additional SiC surface during a subsequent oxidation step intended to remove the carbon residue left on the surface as a decomposition product. Normally we have performed the oxidation step at 500°C, which removes carbon but not SiC (Ref. 31). This particular oxidation was performed at 1200°C, which removed some additional SiC. No further increase in mobility is observed above 1700°C; indicating that the annealing of disorder is complete.

An attempt to reproduce the previous data led only to qualitative agreement. This experiment was performed on two crystals from the same growth batch as the earlier sample. A pair of these α-SiC crystals with $10^{18}/cm^3$ aluminum centers was prepared for nitrogen implantation. This original preparation was exclusively chemical in order to avoid possible mechanical damage. Both crystals were oxidized in dry oxygen at 1200°C for 18 hours. Oxide thickness was judged by interference colors to be 3000 Å. The oxide was removed in HF, and a double implant of 1.1 x $10^{15}/cm^2$ at 85 keV and 1.05 x $10^{15}/cm^2$ at 25 keV nitrogen ions was performed at room temperature.

Hall measurements were not possible on the implanted surface of either sample before annealing, but ρ_s of one surface was measured to be 8.1×10^5 Ω/□. Mesas were formed at one corner of each crystal by ion sputtering since the unannealed SiC resisted electrolytic etching. Diode characteristics of these mesas could not be measured at that stage due to our inability to make contacts to the SiC without also causing some annealing.

One of the crystals, which will be referred to as 100B, was measured after annealing at temperatures through 1500°C and exhibited changes in electrical characteristics in keeping with previous samples studied. The sputter-formed mesa structures were not satisfactory after annealing since the residual surface was still n-type. The SiC had been sputtered using a 3 kV Ar beam with 8 mA current for 5 hours. SiC was removed to a depth beyond the original implant range and mesa structures were formed. However, after annealing, the SiC surface cleaned by the sputtering beam was found to be n-type itself. The cause of such a condition has not been determined, but might be due to trace nitrogen in the argon sputtering beam with a resulting low-energy nitrogen implant. These areas were avoided in subsequent work on these samples, and electrolytic etching was used when mesa formation was required.

Hall and sheet resistivity measurements of the implanted layer were not possible until the sample was annealed at 1200°C. This situation has been common in examination of implanted layers in which the sheet resistivity is much above 10^4 Ω/□ and merely reflects the inadequacy of soldered contacts on such a surface. Annealing was carried out in nitrogen for temperatures through 1300°C, and in vacuum of 10^{-6} Torr or better for higher temperatures. The results of the series are shown in Table III.

TABLE III

Data Summary – Sample 100B

Anneal, Temperature, °C	Cumulative Duration at Given Temperature, min	ρ_s, Ω/□	V_H/I	N_s/cm^2	μ, $cm^2/V\text{-}sec$
1200	5	3.6×10^4	48	1.2×10^{13}	15
1200	35	3.3×10^4	12.3	4.6×10^{13}	42
1300	5	2.4×10^3	7	8.0×10^{13}	33
1400	2	2.6×10^3	7.3	7.7×10^{13}	31
1500	2	1.5×10^3	5.0	1.15×10^{14}	36

T13

Distinct differences in anneal behavior can be seen by comparing this data with that of sample 77 A (Fig. 30(a)). The two samples have had the same dose-energy-temperature relationships during the implant process; such differences seem irregular, but upon detailed examination these differences appear to be in keeping with work done in ion implantation in other materials. In brief, the differences are:

- N_s for 100B is observed to be two orders of magnitude below the implanted dose and to increase with annealing temperature, while in sample 77A it remained essentially constant at about half the implanted dose.
- Carrier mobility quickly rises to its highest value in 100B whereas 77A required high anneal temperatures to obtain high mobility.

- Although not seen in the data yet presented, the capacitance-voltage behavior of diodes made in the 100B sample are unusual.

While the two implanted layers are, of course, made in different crystals, the crystals are of the same growth batch. However, there is always the possibility that the observed differences in donor concentrations are due to compensation from different bulk acceptor concentrations.

On implant parameter which has been substantially changed between the two nitrogen implantations was dose rate. The implants for 100B required 2.7×10^3 sec and 4.0×10^3 sec for the 85 keV and 25 keV implants, respectively, while the 77A implants were for 1.8×10^3 sec and 0.72×10^3 sec, respectively. The dose rate of 100B is seen to be significantly lower than those described for 77A.

The effects of dose rate have not been studied in SiC, but have been studied in silicon. Work by Eisen[43] has shown that for room temperature implants of a low-mass ion (Boron) in silicon, the amount of crystal damage is proportional to the dose rate. Investigation of annealing processes in silicon[44] has established that, when comparing a heavily damaged crystal with a lightly damaged crystal, the effects closely approximate the situation that has developed in our SiC program. Considerable work must be done to establish this analogy as fact, but the disparity of annealing results in nitrogen-implanted SiC may be explainable in terms of dose rate variation.

(Another possible explanation for the differences in the anneal behavior would be that sample 100B did not receive the ion dose of $2 \times 10^{15}/cm^2$ indicated but an order of magnitude less. A check of the implant conditions recorded at the time of implant did not reveal any errors or indications

of problems during this implant or other implants made during this period.)

Incidental results of annealing nitrogen implantations into heavily doped SiC were discussed in Section III-A-3. The data tabulated there resembles that of 77A rather than that of 100B, and the implant times of 4×10^2, 10^3 and 1.3×10^3 seconds for the 300 keV, 100 keV, and 40 keV energies, respectively, show that the dose rate also more nearly resembles that of 77A rather than 100B.

Recent work in our laboratory on damage versus produced dose by nitrogen implants into SiC has shown a super linear behavior which would tend to support the belief that dose rate effects have caused the observed differences between nitrogen implanted samples. (See Section III-B-5.)

A sample was also prepared with a much lower dose so that the percentage of electrically active donors could be compared. To insure adequate electrical contacts to the relatively lightly doped SiC, pads (which had been nitrogen implanted to a dose of $10^{15}/cm^2$ at 100 keV and $5 \times 10^{14}/cm^2$ at 40 keV) were located at the corners of a region subsequently implanted with $5 \times 10^{13}/cm^2$ nitrogen ions at 30 keV implant energy. All implants were done at room temperature.

The implants were made into the SiC surface with no preliminary polishing or oxidation. The surface was cleaned thoroughly in acids, but otherwise it was in its as-grown condition.

After implantation, the sample was initially annealed at 1500°C in vacuum and was then baked in oxygen at 600°C. The results of Hall measurements after this and subsequent anneals are shown in Table IV.

TABLE IV

Hall Measurement Results* – Low Implant Dose

Anneal Temperature, °C	ρ_s, Ω/□	V_H/I	N_s carrier/cm^2	μ, cm^2/V-sec
1500	3.45×10^3	3.65	1.5×10^{14}	12.1
1600	3.3×10^3	4.9	1.15×10^{14}	16.5
1700	4.23×10^3	5.05	1.1×10^{14}	13.4
*All measurements made after oxidation-cleaning.				

T14

Referring to the 1700°C anneal, the data appear to reflect the increased surface decomposition at this temperature; i.e., the amount of implanted material lost may no longer be negligible.

For this sample, it appears that we have detected more donors in the implanted region than were put there by the implantation; there are several possible explanations for this, however. The most obvious cause of excessive numbers of carriers is that the implanted dose was actually twice that recorded, but more subtle factors can also account for this. The ratio V_H/I is inversely proportional to N_s, and any shunting path or geometric feature which will reduce the measured Hall voltage will effectively increase the measured carrier concentration. Other measurements must be made to determine the existence and/or cause of this apparent discrepancy in the carrier concentration.

The mobility of the carriers in the implanted region appears consistent with earlier implants. For a 30 keV nitrogen implant, with random incident beam angle to avoid lattice channeling effects, the implanted layer is expected to be about 0.1 μm thick. This implies an average carrier concentration for this sample on the order of $10^{19}/cm^3$. Data published by Kamath[45] indicate that an electron mobility of about 30 cm^2/V-sec can be expected to be the maximum attainable for this concentration. Because the actual carrier concentration is not constant but is greater than $10^{19}/cm^3$ in some regions, our measured mobility is considered to be in reasonable agreement.

Examination of Kamath's data suggests that above a concentration of about $10^{19}/cm^3$, the mobility is only slightly dependent on concentration. Comparison of data taken from nitrogen-implanted layers tends to confirm this. While the implanted ion concentration presumably has a Gaussian distribution as a function of depth in the crystal, a peak concentration can be determined. For implanted layers containing more than one distribution profile as a result of multiple implants, we have taken an arithmetic average of the peak concentrations, and have used this concentration as a parameter in Fig. 31. This figure shows the carrier mobility as a function of anneal temperature for three concentration parameters. It is apparent that the annealing temperature has much more effect on mobility than does the average concentration.

b. Phosphorus Implants – As described in the October 1969 Annual Report, phosphorus has been used to create n-type regions and p-n junctions in α-SiC. p-type SiC doped to a level of $10^{18}/cm^3$ was used as a substrate, and two room-temperature implants were made into the same face with

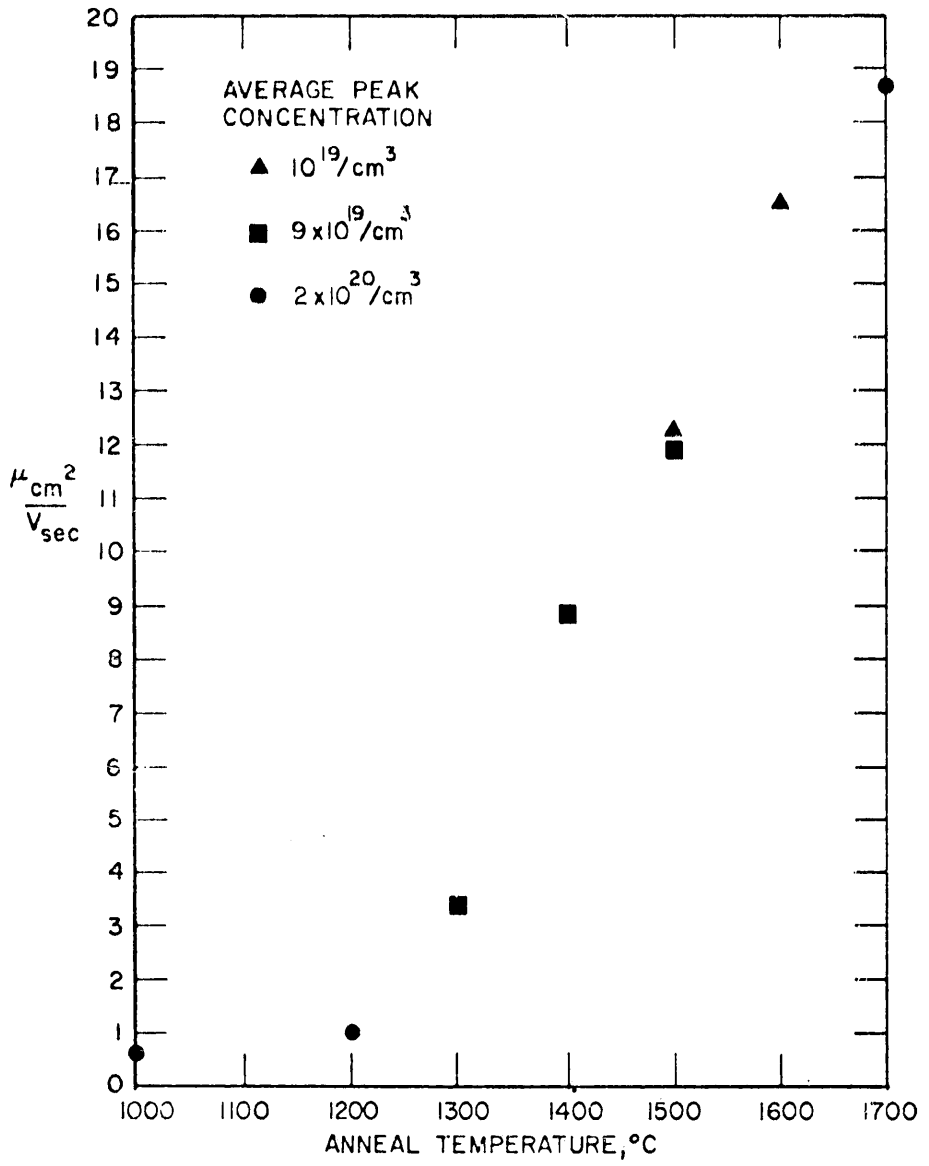


Fig. 31. Electron mobility as a function of anneal temperature.

$5 \times 10^{14}/cm^2$ at 145 keV and $1 \times 10^{14}/cm^2$ at 50 keV. The calculated doping profile shows that there are two regions with peak concentrations of $2.7 \times 10^{19}/cm^3$ and $5.5 \times 10^{19}/cm^3$ at 0.04 μm and 0.12 μm, respectively, with the p-n junction about 0.2 μm beneath the surface. Reference 39 discusses the pertinent calculations.

Following the implant and prior to anneal, the sheet resistivity was measured to be on the order of 2×10^5 Ω/□. This measurement was possible only at currents ≤ 1 μA, and contact noise prevented any Hall measurement. Annealing at 1000° and 1200°C produced no significant change, but Hall measurements were possible after a 2-min anneal at 1400°C. Data from these measurements and from others made following higher temperature anneals are shown in Fig. 30(b). The measured number of electrically active carriers is about one-third of the net implanted donor level.

c. Disorder Analysis – In addition to the Rutherford backscattering analysis of disorder discussed later in this section, annealing of disorder in implanted layers has been analyzed further with the scanning electron microscope (SEM), using Coates-Kikuchi pattern generation.[46] The pattern observed from a SiC surface after a high dose implant similar to the nitrogen implant denoted as 77A is shown in Fig. 32(a). The lower right hand corner of the sample was masked against the implant with a thick metal mask, and the Coates-Kikuchi pattern of single crystal SiC is evident in this region. The implanted surface shows no pattern, indicating a high state of disorder. An anneal in vacuum at 1600°C for 2 min produces a surface as shown in Fig. 32(b), where it can be seen that crystallinity has been restored in the implanted layer; essentially in agreement with the observations of mobility in Fig. 30(a) and (b).

(a) After implantation before annealing.

(b) After 1600°C, 2 min anneal.

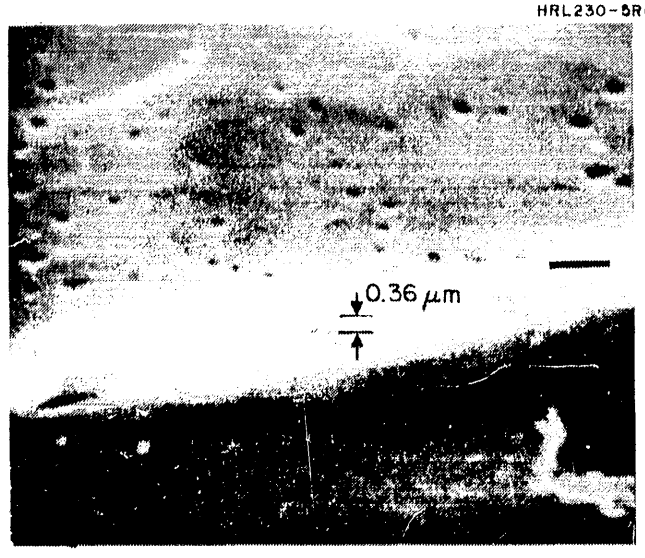
Fig. 32. Coates-Kikuchi lines from ion-implanted α-SiC showing restoration of surface crystallinity by annealing.

d. Impurity Profile by Junction Depth Measurements - The assumption that the profile of the nitrogen implant is approximated by the calculated distribution, has been partially checked by measuring the depth of the junction using the SEM. The junction etching technique of anodization described above was used to delineate the n-type region. The fractured edge of the n-type layer can be seen with the SEM used in the secondary electron emission mode, as shown in Fig. 33(a). The implanted surface is visible in the top half of Fig. 33(a). The spotted appearance is a result of the Na_2O_2 etch used on this sample to prepare the surface before implantation. The p-type substrate is seen in the lower half of the figure. The fractured edge is identified by arrows. The measured junction depth for this implant is 0.36 μm, while the predicted depth is ∿ 0.25 μm (see Fig. 21). This discrepancy could easily have been brought about by ion channeling that took place during the implant as no precautions were taken to avoid channeling.

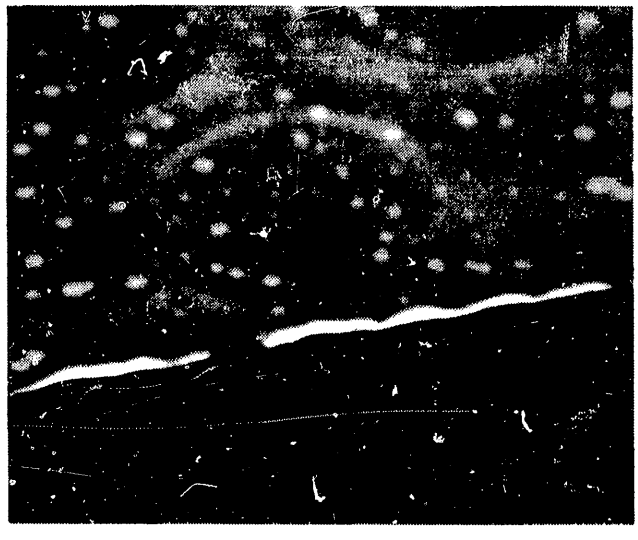
The position of the p-n junction was verified using the SEM in the electron bombardment induced current mode and is displayed in Fig. 33(b) with the same magnification and sample position used for Fig. 33(a). In this mode the electron-hole pairs generated by the high energy incident electrons are collected by the p-n junction and measured as a current which modulates the z-axis display of the SEM. The peak in collected charge occurs in the vicinity of the lower portion of the fractured edge, indicating the surface position of the p-n junction.

2. Conduction Properties of Implanted p-Type Layers

The column III elements of the Periodic Table are expected to behave as acceptors in SiC. Aluminum and boron have been used extensively in both growth and diffusion to



(a) Shows topographical features through secondary electron emission.



(b) Shows charge collection at the junction through electron beam induced current. The magnification and region viewed by the SEM are the same for both photographs.

Fig. 33. Scanning electron microscope display of junction region in nitrogen implanted α-SiC.

form p-type SiC (Ref. 47,48). We have studied B and Al, as well as Ga, Tl, and Be implants made with energies from 10 to 100 keV into n-type SiC at dose levels calculated to form a p-type layer doped at $10^{19}/cm^3$ or above. The implanted regions were darker in color and thus were easily identified after implant of any of these dopants. This darkening would decrease considerably after a 15 min anneal at 500°C and was nearly undetectable after a 1000°C anneal; similar to the behavior observed on n-type implants. The implanted layers appeared to be of high resistivity, and except in a very few cases, either measured n-type by a thermal probe or gave no response to thermal probing after the 500° or 1000°C anneals. Continued annealing to as high as 1700°C did not result conclusively in a p-type layer for any of the elements tried. The implanted surface was either high resistivity or weak n-type.

a. Aluminum Implants — Repeated attempts have been made to create p-type region in both α- and β-forms of n-type SiC by aluminum implantation. These have been discussed in Interim Reports for 1967, 1968, and 1969, of this contract. With a single exception, only high resistivity regions were formed.

The single exception observed was an Al implant into an n-type piece of β-SiC obtained from the Stanford Research Institute. Hall measurements confirmed that this crystal was n-type with approximately $10^{17}/cm^3$ nitrogen donors. Aluminum ions with 20 keV energy were implanted at 500°C in a small disk-shaped area in the center of one crystal face. Following anneal at 1300°C a definite p-type indication was obtained from the implanted region by Hall measurements. None of the other tests indicated the presence of a p-type layer. We have not yet succeeded in reproducing this condition in other SiC crystals, and we include these results only for completeness.

b. Beryllium Implants – Kal'nin et al.,[49] and Maslakovits et al.,[50] have reported that beryllium (Be) in SiC forms deep acceptor levels and is an activator for red luminescence. We have attempted to create p-type layers by implanting beryllium. Two crystals used in these experiments were grown doped with about $2 \times 10^{18}/cm^3$ nitrogen atoms and implants were done at room temperature, but different implanting systems were used. One crystal was implanted using the spark-gap ion source, which did not allow measurement of implant dose. The implant voltage was 30 kV and estimates of range-energy parameters would place the greatest concentration of implanted ions about 0.1 μm beneath the surface. Another crystal was implanted with a mass-separated beam at two energies.* A dose of $10^{15}/cm^2$ at 60 kV and $10^{15}/cm^2$ at 20 kV was obtained. We expect from this an implanted layer about 0.2 μm thick. As has been found in other acceptor-specie implants, no p-type response has been obtained from either implanted layer following anneal at temperatures to 1700°C.

c. Thallium Implants – In a continuing effort to form a p-type layer in n-type SiC through ion implantation, we have also implanted thallium (Tl) into two α-SiC crystals. While annealing conditions have not established acceptor action, the high resistivity layer obtained after implanting other acceptor-type ions, i.e., aluminum or boron, has not been formed. A heavy implant of $10^{15}/cm^2$ at 100 keV plus $10^{15}/cm^2$ at 40 keV, and a light implant of $10^{14}/cm^2$ plus $5 \times 10^{13}/cm^2$ at the same respective implant voltages were performed at room temperature on two crystals of α-SiC. These crystals had been grown with nitrogen donors at a concentration of about $2 \times 10^{18}/cm^3$.

*This implant was performed by R. Hart.

Annealing the heavy thallium implant at 1200° and 1500°C did not activate any potential acceptor ions. Hall measurements on the implanted surface were found to be of the bulk crystal, since there was no p-n junction present to isolate the implanted layer. The light implant has not been annealed, but the implantation-induced crystal damage does not prevent Hall measurements with essentially the same results as for the heavy implant. So far, aside from a darkening of the crystal, the thallium has had no measured effect on the SiC.

Rutherford backscattering measurements of disorder formation and annealing and lattice location determination have been performed on Tl implants into SiC. No substitutional Tl was observed after high temperature annealing which may explain the absence of p-type behavior, although the particular implants may have greatly exceeded the solubility limit for Tl in SiC.

d. Boron Implants – As was the case with aluminum. Interim Reports for the preceding three years of this contract have recounted ineffective attempts to form p-type regions in n-type SiC through the use of boron implantations. We have been able to form insulating regions in the SiC which will have eventual device application.

While our earlier implants involving aluminum or boron ions failed to produce p-type SiC they did form high resistivity layers in the n-type substrate crystals. Such layers can be of great value in device fabrication if they can be formed in highly doped SiC.

To establish that an acceptor-type implant can be used to compensate highly doped n-type SiC, a small piece of nitrogen-implanted, p-type SiC was annealed at 1600°C in vacuum and baked in oxygen at 500°C. The N implant had been

performed at room temperature with a total dose of 2×10^{15} ion/cm^2 and implant energy up to 84 keV. Surface resistivity was determined to be 850 Ω/□.

Two small regions of the n-type implanted layer, 0.5 mm apart, were then masked with indium metal and the sample was implanted with boron for a total of 10^{15} ion/cm^2 at 80 keV and 5.6×10^{14} ion/cm^2 at 20 keV. This dose-energy series was intended to penetrate beyond the nitrogen-implanted layer and form a high-resistivity layer which would isolate the remaining n-type islands. With no anneal of the boron implant, there is a measured resistance of 5 MΩ between the two dots. This 5 MΩ is the total resistance between the two n-type regions and is constant over ±30 V bias. Beyond this bias the p-n junction breakdown of the two back-to-back nitrogen implanted diodes causes current to flow in the p-type bulk and shorts out the implanted insulating layer.

3. Summary of Electrical Effects of Implanted SiC Layers

The results of our investigations on various ion species and their dopant behavior in SiC after annealing from 1000° to 1700°C for 2 to 10 min are summarized in Table V. The column V elements are expected to be donor impurities in SiC, and donor-type behavior has been observed for N, P, Sb, and Bi in p-type α-SiC. Hall effect measurements have been made on N, P, and Sb layers, confirming n-type behavior as indicated by the thermal probe and the presence of p-n junction behavior. The Bi implanted layers were not evaluated by Hall effect, but showed n-type behavior with thermal probing and the presence of a broad area p-n junction. Sb implants have been used to form n^+ contacts to n-type α and β SiC. These implants generally were performed at 500°C and annealed at 1300°C or greater.

TABLE V

Tabulation of Tested Ions

Substrate	Implanted Ion*					
	Column V	Electrical Behavior	Column III	Electrical Behavior	Other	Electrical Behavior
α-SiC	N	n	B	High ρ	Be	High ρ
(n- or p-type)	P	n	Al	High ρ	H	——
	Sb†	n	Ga	High ρ	He	——
	Bi	n	Tl	——	—	——
β-SiC (n-type)	Sb†	n	Al	p(?)	—	——

*Implanted at room temperature; annealed at 1900°C to 1700°C for 2 to 10 min.

†Also implanted at 500°C and annealed at 1300°C.

T15

The donor behavior observed in SiC for the column V elements is believed to result from the chemical nature of the elements rather than from defects generated by implantation. Two factors support this belief. Implantations of elements other than those from column V, such as column III, do not create highly doped n-type layers. In addition, the measured number of carriers/cm^2 for nitrogen and phosphorus implanted layers is generally within a factor of three of the implanted dose over a range from 5×10^{13} to 2.5×10^{15}/cm^2. The fact that the surface carrier concentration is measured to be less than the implanted dose may be due to the activation energy of $\simeq$ 0.10 eV for nitrogen in SiC (Ref. 51). It would be necessary to perform Hall effect measurements as a function of temperature to establish this and this has not been done on these samples at present.

When the electrical behavior of donors implanted at 23°C into SiC is considered as a function of annealing temperature, a distinct difference from that obtained with implants into Si is observed. The anneal behavior of SiC shown in Fig. 30(a) and (b) suggests that at an early stage in the annealing of disorder, most of the implanted ions reside in lattice sites that result in donor action. Such behavior indicates that most of the gross disorder in the SiC layer has substantially annealed by 1100°C for nitrogen implants and 1500°C for phosphorus implants. However, at these temperatures sufficient disorder remains to substantially reduce the carrier mobility below the levels expected for bulk crystals. By comparison, the recrystallization of an amorphous layer in Si at 600°C results in a high electrical activity of the implanted species similar to that observed for SiC. However, the carrier mobilities in Si are equivalent to those obtained in bulk materials, indicating that little residual damage remains which is contrary to the behavior of

SiC. At temperatures less than 600°C the implanted Si layers show carrier densities considerably below the maximum attainable at 600°C but the electrical properties are still measurable, again in contrast to SiC.

The inability to form p-type layers in SiC using implant and anneal procedures similar to those used to form n-type layers is not understood at present. Although a detailed analysis of the anneal of disorder in the layers implanted with p-type dopants has not been conducted, the visual indications of disorder (i.e., the dark stain observed after implant) give evidence of annealing in a fashion similar to that of donor implanted layers. Possible reasons for the absence of p-type behavior are that enough of the implanted ions do not occupy normal substitutional sites after the lattice has annealed, or if they do occupy these lattice sites some form of a compensating donor defect is still present. It is additionally possible that the implanted impurity outdiffuses during the regrowth of the amorphous layer although Rutherford scattering studies on Tl implants have shown no evidence of this behavior, (see Section III-B-5.) Outdiffusion of implanted impurities during annealing has been observed in Si (Ref. 52). We are now investigating, through use of the Rutherford backscattering measurements, the lattice location of various impurities implanted into SiC in an effort to determine whether the lack of doping is associated with improper lattice location or compensating defects (Section III-B-5). It is possible that substantially higher anneal temperatures may be required to produce substitutional dopants or eliminate defects. Such anneals cannot be carried out in vacuum because of the decomposition of SiC. Thus, an entirely different annealing system is required, with a capability of maintaining a gaseous overpressure.

4. Ion Implanted Junctions

a. p-n Junction Behavior versus Annealing – The diode characteristics of p-n junctions obtained with implanted donor species into p-type α-SiC were evaluated as a function of annealing, along with the Hall effect and sheet resistivity studies discussed in prior paragraphs. The diodes were constructed within the same implant used for Hall effect evaluation by etching an island to form a mesa device.

The current-voltage characteristics measured at room temperatures plotted as log J and linear V are shown versus anneal temperature in Fig. 34 for an implant of nitrogen. The doses and energies used were similar to those illustrated in Fig. 21, and refer to the device identified as 77A. The J-V curves of Fig. 34 can be divided into two conduction regimes. At a voltage of less than 1.5 V the current is controlled by p-n junction behavior or junction behavior plus leakage currents. Above 1.5 V the current is limited by a resistance which is strongly affected by annealing; decreasing in value with increasing anneal temperature. Investigation proved that this resistance was not associated with contact drop, and resistance spreading in the implanted layer was avoided by metallizing the entire mesa surface. The source of this resistance is suggested from the capacitance-voltage behavior of these diodes at 100 kHz, as shown in Fig. 35. The $1/C^2$ versus V curve, after 1100°C anneal, is characteristic of a diode that contains a semi-insulating layer and behaves as a p-i-n structure. The notable feature of p-i-n structures is the voltage intercept of the $1/C^2$-V plot at a large value compared with the voltage equivalent of the bandgap (~3 V for the SiC used here). Annealing at 1300° and 1500°C progressively decreases the thickness

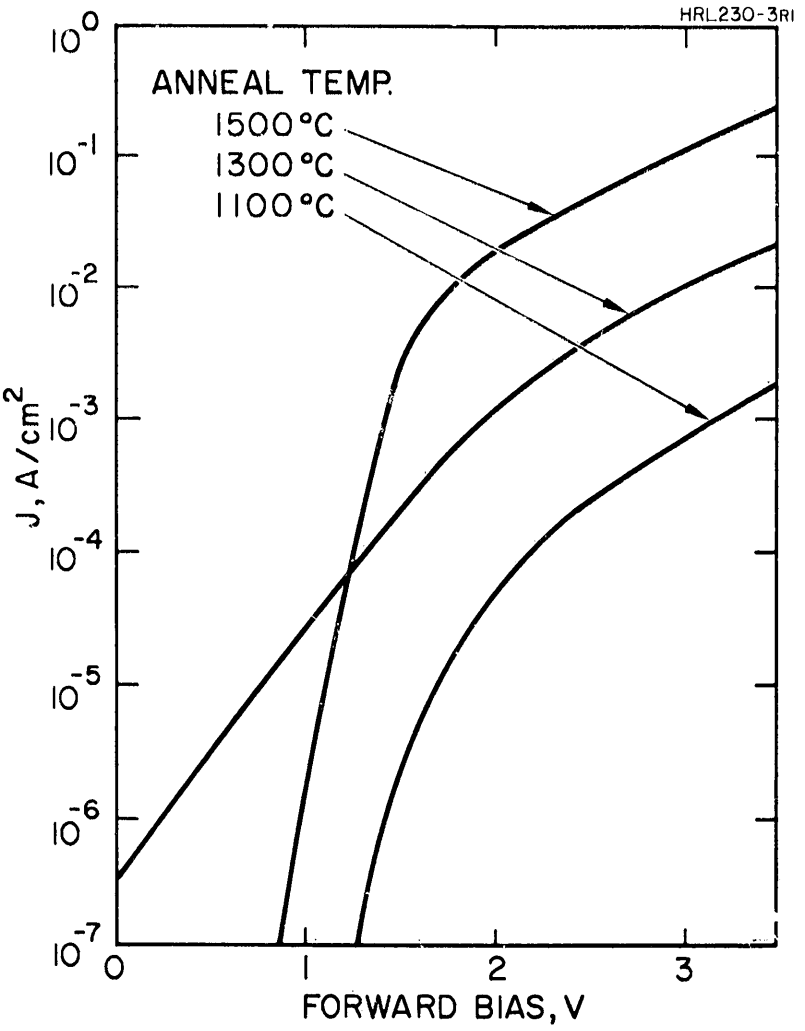


Fig. 34. Log J versus forward bias for a mesa diode of nitrogen-implanted α-SiC for increasing anneal temperature.

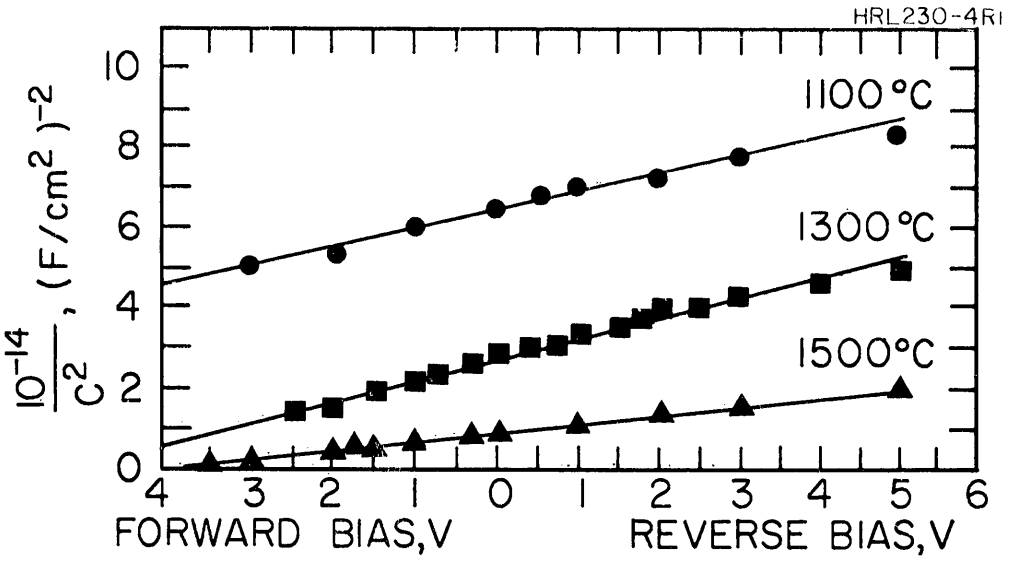


Fig. 35. $(1/C^2)$ versus V for the device described in Fig. 34 for increasing anneal temperatures.

of the semi-insulating region and increases the capacitance. The change in series resistance observed in the J-V data of Fig. 34 can then be explained in terms of the presence of a semi-insulating layer that decreases in thickness with increasing anneal temperature.

The thickness of the semi-insulating layer can be estimated from the capacitance data of Fig. 35 by using the offset of the 1100°C anneal curve from the 1500°C curve to calculate the effective series capacitance of the i-layer.* From this capacitance a thickness of 0.22 μm is calculated for the semi-insulating layer. Using the value of the dc series resistance observed in the J-V curve for the 1100°C anneal of Fig. 34, a resistivity of $\sim 6 \times 10^7$ Ω-cm is calculated for the i-layer. Using these same procedures, the calculated thickness after the 1300°C anneal is 0.1 μm and the resistivity of the semi-insulating layer is 10^7 Ω-cm.

A preliminary investigation of the frequency dependence of the capacitance-voltage behavior of devices in which a large i-region is present indicates that the determination of the i-layer thickness is sensitive to the measurement frequency, and some caution must be used here in interpreting results where ac and dc measurements are combined.

As described in the appropriate section of this report and in Ref. 53, semi-insulating layers have been observed in ion implanted junctions in GaAs and i-layers were attributed to the presence of trapping levels introduced by defects. These defects were either generated during implantation or diffused from the damaged layer into the sample during anneal. Later studies revealed that these semi-insulating regions could be annealed away, yielding abrupt junctions of excellent quality.

*It is assumed here that the 1500°C anneal curve is nearly that expected for an abrupt p-n junction. This assumption will later be shown to be reasonable.

It would appear, then, that an i-region is generated in SiC which is positioned at a depth within the crystal that is considrably beyond the amorphous range of the implanted ions and is presumably generated by defects which diffuse from the implanted region either during implantation or annealing.

b. Well-Annealed Junctions – Measurements of the device characteristics of diodes formed by electrolytic etching have determined that annealing the crystal may change the characteristics of the p-n junction without significantly changing the characteristics of the conduction layer. In particular, the junction measurements of the layer discussed in Table III as 100B changed considerably when the anneal temperature was raised from 1300° to 1400°C, whereas little change in the Hall effect and sheet resistivity of the implanted layer is shown in Table III. This is to be expected if defects generated by the implantation are present in sufficient quantity to affect the electrical properties in the more lightly doped p-layer but not of sufficient number to affect the properties of the heavily doped implanted n-layer. The diode measurements are consistent with those previously reported[3] on nitrogen implanted SiC diodes with one exception. The current-voltage and capacitance-voltage characteristics reinforce the existence of a semi-insulating region at the junction observed previously, but C-V measurements are affected by contact size and spreading resistance to a much greater degree than the sheet resistivity would justify. This last difference between the samples being compared seems to be due to the variation in the conducting layer rather than a p-n junction effect, and is possibly a result of the change in dose rate.

The forward and reverse current-voltage behavior of the diode 77A discussed in regard to Fig. 27 is shown in Fig. 36 as a function of operating temperature following surface cleaning. A major portion of each curve contains a current proportional to exp eV/2kT. Extrapolation of these straight line portions to zero voltage yields values of the saturation current J_s at various temperatures. In Fig. 37 the activation energy of the saturation current is shown to be very close to one-half the bandgap of the SiC used here.

At lower operating temperatures (23° and 100°C), an excess current is observed at low bias voltages, apparently as a result of surface leakage.* At operating temperatures of 300° and 400°C the higher current values increase more rapidly than exp eV/2kT; approaching exp eV/kT. At the highest values, the current is limited by series resistance.

The value of this resistance agrees closely with that calculated from the device geometry and the bulk resistivity of the substrate material. If an i-region exists in this device, similar to that observed in devices annealed at lower temperatures (see Fig. 34), its resistance is much less than that of the bulk material.

The forward current-voltage behavior of these diodes at low currents appears to be explainable in terms of the model, developed by Sah, Noyce, and Shockley,[54] of recombination of injected carriers in the space charge region. A component due to diffusion current is observable at high operating temperatures and currents. Finally, at higher operating currents the series resistance of the bulk material limits the current and the i-layer observed for lower anneal temperatures is not apparent.

*The dependence of these excess currents upon temperature has been investigated. J_s values obtained for a device in condition A of Fig. 27 show a small temperature dependence and no simple activation energy.

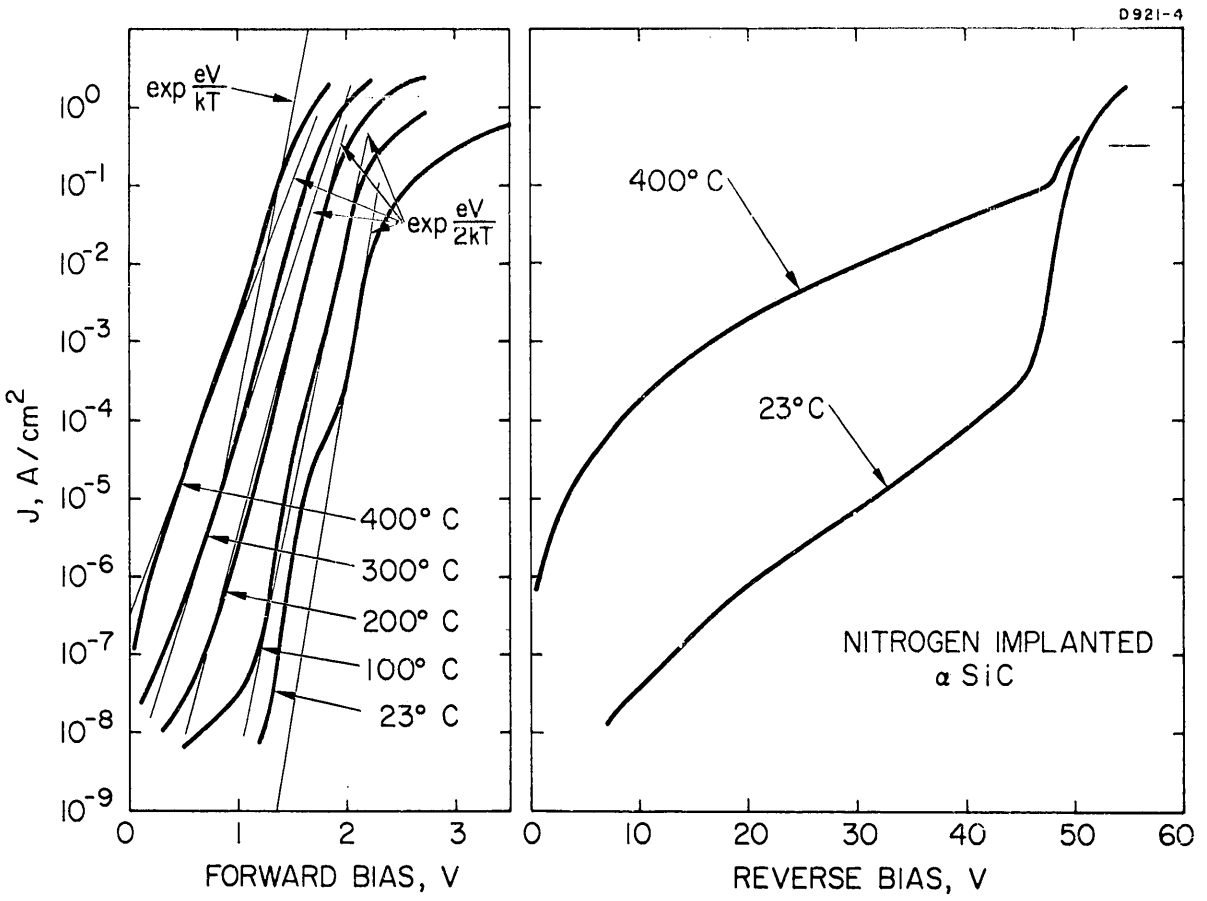


Fig. 36. Log J versus forward and reverse bias for diode of well-annealed nitrogen-implanted α-SiC at various operating temperatures.

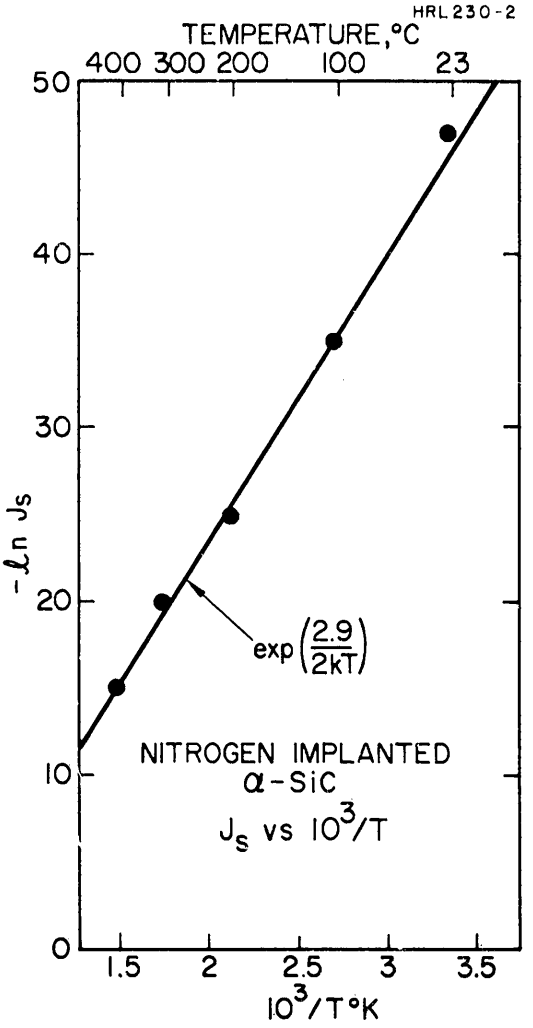


Fig. 37. Log J_s versus 1/T for the diode described in Fig. 36.

The emission spectrum of a forward-biased, ion implanted SiC diode was measured using a Jarrel-Ash, 1/4 m monochromator. The diode was fabricated by implanting nitrogen ions into a p-type substrate of aluminum-doped ($10^{18}/cm^3$), α-type SiC. Implantation at room temperature of a dose of $1 \times 10^{15}/cm^2$, 80 keV ions and of $1.2 \times 10^{15}/cm^2$, 25 keV ions as followed by anneal for 2 min at 1400°C. Contacts to the resulting p-n junction diode were made using silver epoxy. At room temperature the diode was found to emit radiation in a broad band of wavelengths, with the peak intensity at approximately 5400 Å (2.3 eV) (see Fig. 38). The half width of the emission peak was about 800 Å, but there was a "shoulder" on the long wavelength end of the curve which extended to about 6500 Å. No quantitative measurement was made of total emitted power, but the light could be observed visually in a semi-darkened room with as little as 20 μA of current flowing in the diode.

The reverse current-voltage behavior of these diodes is shown in Fig. 36 for operating temperatures of 23° and 400°C. No saturation of the reverse current is observed; there is merely a gradual increase in leakage current as the voltage is increased. The onset of breakdown between 45 and 50 V is correlated with the appearance of small blue microplasmas[47,55,56] at visible defects in the original surface of the device. The breakdown voltage does not appear to be strongly sensitive to temperature.

The capacitance-voltage behavior of these devices at 100 kHz is shown in Fig. 39 for two operating temperatures, 23° and 300°C. A calculation of the carrier concentration obtained from the slope of the $1/C^2$-V curves indicates an acceptor concentration in the p-region of $6 \times 10^{17}/cm^3$ in fair agreement with the value reported by the crystal suppliers.

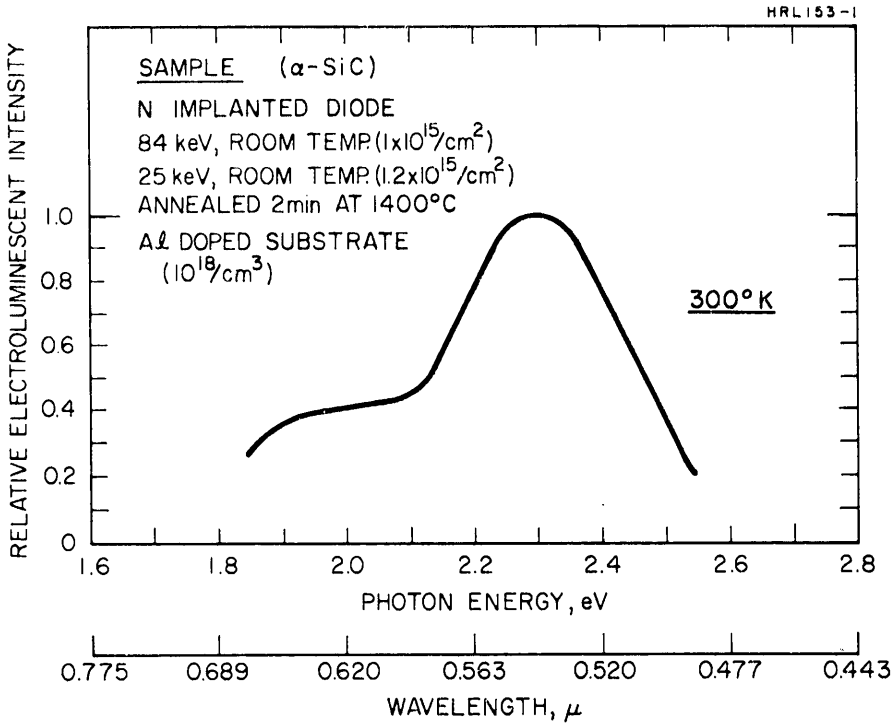


Fig. 38. Emission spectrum of forward-biased nitrogen-implanted SiC diode.

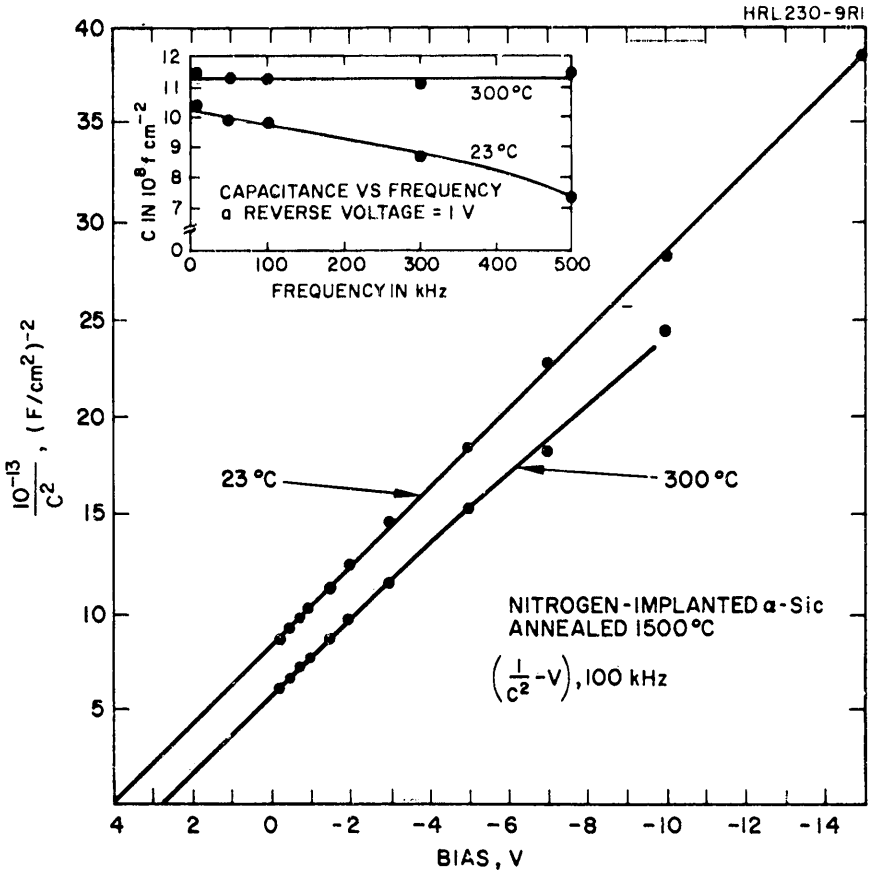


Fig. 39. Capacitance characteristics of the device described in Fig. 36 as a function of operating temperature. The inset shows the frequency dependence of this device for the two operating temperatures.

The voltage intercept of the 23°C curve at 4.1 V forward bias is greater than the predicted value of ∿3 V for a simple abrupt junction in SiC. However, the intercept of the 300°C curve occurs at slightly less than 3 V. The inset of Fig. 39 shows the capacitance variation with frequency of this device at 1 V reverse bias for the two operating temperatures. The capacitance is essentially independent of frequency at 300°C over the frequency range investigated here. The 23°C capacitance measurement is sensitive to frequency, decreasing in value with increasing frequency. At the lower frequencies the measured capacitance at 23°C approaches the value obtained at 300°C.

The voltage intercept at 23°C being greater than the voltage equivalent of the SiC bandgap of ∿3 V might suggest that at this temperature an i-region is present in the device as had been present in lower temperature anneals shown in Fig. 34. This can indicate incomplete annealing of defect centers generated during implantation and annealing. However, the observed capacitance behavior may be explained in terms of a simple abrupt junction consisting of a highly doped n-region and a more lightly doped p-region in which the acceptors have a deep energy level. The effects of deep impurity levels upon reverse bias capacitance behavior of n^+p junctions has been considered by Schibli and Milnes.[57] As a result of their model they predict capacitance frequency and temperature behavior which closely parallel those observed in these SiC devices annealed at temperatures of 1500°C or greater. Their predictions are based upon a p-layer doped with a deep acceptor level. The dopant in the SiC substrates used here is aluminum which has an activation energy ≥0.3 eV (Ref. 58) and behaves as a deep level dopant at 23°C.

Kholuyanov and Gavrilovski[59] have observed similar capacitance-voltage characteristics in SiC p-n junctions, and concur that a deep level is at least partly responsible. In addition, they have shown that the existence of three inequivalent lattice positions[51] of SiC can contribute to this effect.

As described above, the well-annealed SiC diode exhibits a series resistance corresponding to the resistivity of the bulk SiC, with no indication of the presence of an i-region. Therefore, we believe that the C-V behavior of these devices is satisfactorily explained in terms of the bulk properties of the SiC rather than by the presence of defects introduced by implantation.

The I-V and C-V data versus operating temperature obtained on diodes made by implanting P, Sb, or Bi into p-type SiC behavior in nearly identical fashion after annealing at 1700°C to that reported here for well-annealed nitrogen implanted diodes. The quality of these devices is excellent; comparing favorably with the best reported junctions prepared by other means.

5. Channeling Studies in SiC

The inability to form p-type layers by ion implantation may be due either to improper lattice position of the acceptor type impurities or, if located in a proper lattice site, to compensation caused by unannealed defects.

The channeling technique, i.e., measurements of backscattered energy spectra of 280 keV alpha particles and 140 keV protons incident in random and <0001> channel directions, has been used to investigate certain physical aspects of ion implanted SiC. We have measured: (1) the <0001> channel critical angle, (2) the amount of heavy impurities residing on or near the target surface, (3) the

amount and depth distribution of lattice disorder produced by 40 or 100 keV Sb^+ and 200 keV Tl^{++} as a function of implantation dose and anneal temperature, (4) the depth distribution and substitutional fraction of the implanted atoms as a function of anneal temperature.

a. Channeling Critical Angle – As discussed in Section III-A, the orientation dependence of backscattering provides a means for alignment of the <0001> channel direction to better than 0.1° with the incident beam axes. Then, half the width of the characteristic dip in the backscattered yield, as the <0001> is tilted through the incident beam, gives the critical angle. For 280 keV He^{++} and 140 keV H^+, the measured <0001> channel critical angle in SiC is 1.3°. A similar measurement for the <111> Si channel gives 1.2°. Thus, the <0001> channel in SiC is a strong channeling direction. However, the orientation of the <0001> varied as much as 0.5° across the target, indicating possible non-uniform crystal growth.

b. Surface Impurities – Backscattered energy spectra with a 280 keV He^{++} analysis beam, incident on the as-grown SiC crystal, are shown in Fig. 40. Only the higher energy region is shown, and for convenience, the energy scale is converted to a mass scale. The two peaks observed in the random spectrum indicate the presence of heavy impurities on or near the target surface with masses around mass 47 and mass 104. The areas give about 10^{15} and 5×10^{13} impurity atoms/cm^2, respectively. The peaks are not seen in the aligned spectrum, suggesting that these impurities are located along the <0001> lattice rows and possibly in substitutional sites. The Si peak is caused by displaced Si atoms in the surface oxide. Approximately 1500 Å of the target surface was removed by oxidation and stripping. The random spectrum was remeasured and is also shown in Fig. 40.

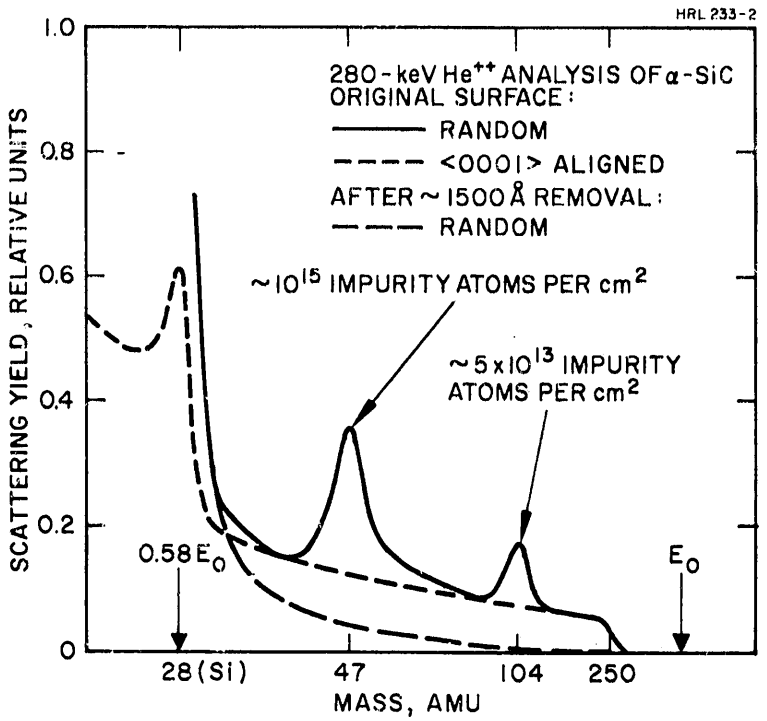


Fig. 40.
Backscattered yields for 280 keV He^{++} from as-grown SiC and after removal of 1500 Å from the surface. The peaks at mass 47 and mass 104 are caused by surface impurities. The peak at mass 28 in the aligned spectrum is caused by Si atoms in the surface oxide.

The heavy impurity peaks were removed, and the background level was reduced significantly by the surface treatment. Consequently, such a surface treatment is recommended whenever surface impurities may be important.

c. Production of Lattice Disorder – Backscattered energy spectra for both random and aligned orientations after implantation to various doses of 40-keV Sb^+ are shown in Fig. 41. The pronounced peaks near the Si surface edge at ∿160 keV are caused primarily by backscattering of the aligned He^{++} from disordered Si atoms, i.e. Si atoms displaced greater than approximately the Thomas-Fermi radius, a ∿0.2 Å, from normal lattice sites.[16,60] It can be seen that the peak height increases with increasing dose and coincides with the random level at a dose of ∿9 x 10^{13} Sb^+/cm^2, indicating a near-saturation level of disorder as measured by backscattering. The peak near 240 keV represents He^{++} backscattered from the implanted Sb atoms after a dose of 9 x 10^{13} Sb^+/cm^2 and is seen to be well separated from the Si edge.

Similar measurements were made for SiC implanted with 200 keV Tl^{++} and are shown in Fig. 42. After the 3 x 10^{13} Tl^{++}/cm^2 implant, the disorder is largely submerged below the target surface (channel 115) and peaks several hundred angstroms below the surface, nearly corresponding to the projected range of the Tl^{++}. The peak rises to the random yield after about 5 x 10^{13} Tl^{++}/cm^2. This dose then represents the critical dose for the formation of totally disordered or amorphous SiC. The amorphous zone then spreads both deeper into the target and toward the surface until, after 1 x 10^{14} Tl^{++}/cm^2, the SiC is totally disordered from the surface to a depth of about 700 Å. The implantation dose was continued to 5 x 10^{14} ions/cm^2 to give good accuracy for substitutional fraction measurements.

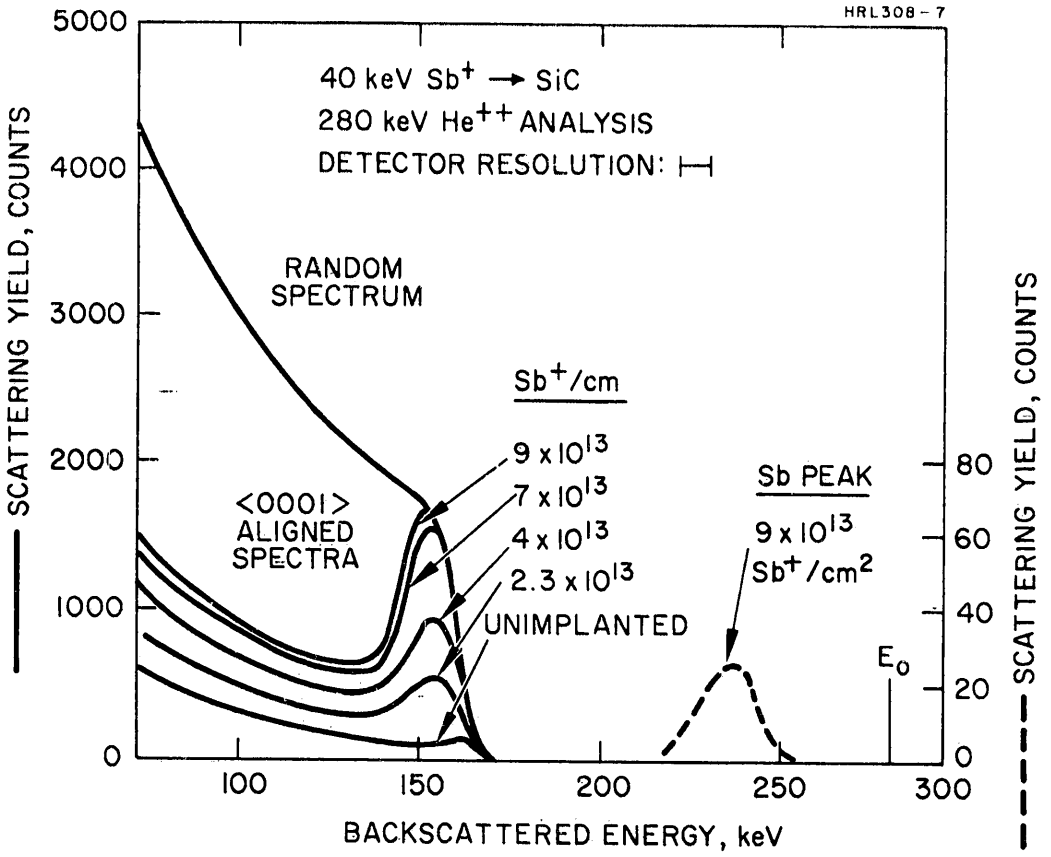


Fig. 41. Backscattered energy spectra as a function of dose for E_o = 280-keV He^{++} incident on c-SiC after implantation of 40 keV Sb^+. A random-equivalent spectrum and an aligned spectrum from unimplanted crystal are included for comparison.

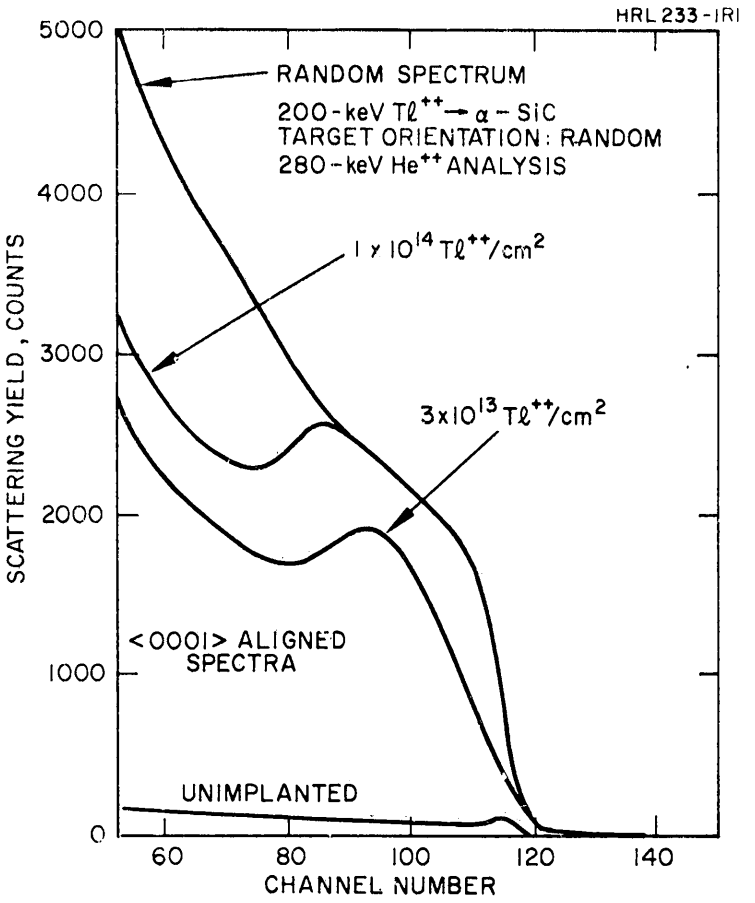


Fig. 42. Aligned backscattered energy spectra for 280 keV He^{++} after implantation of SiC with 200-keV Tl^{++}. A random spectrum and an aligned spectrum from the unimplanted crystal are also included.

The disorder was calculated for the Sb^+ implantations from the areas of the disorder peaks in Fig. 41 according to the procedure discussed in Ref. 60 and is shown in Fig. 43. The disorder increases linearly with dose to the near-saturation level at 9×10^{13} Sb^+/cm^2. This behavior is similar to the production of disorder by 40-keV Sb^+ implantations of Si. (Refs. 16, 60). From the slope of the curve the number of displaced Si atoms per incident ion is ∿1200. 140 keV proton backscattering measurements have shown that the ratio of displaced Si atoms to displaced C atoms is approximately one. Therefore, ∿2400 Si and C atoms are displaced per incident ion. This result is lower than that measured after 40 keV Sb^+ implantations of Si, i.e., ∿3000 to 5000 displaced Si atoms per incident ion.[34,35] Consequently, the diplacement threshold energy E_d of SiC may be 1.2 to 2.1 times greater than that of Si, which is ∿14 eV (Ref. 36). Thus, E_d in SiC may be 17 to 30 eV.

d. Disorder Annealing – The disorder produced by the 9×10^{13} Sb^+/cm^2 implantation was subsequently annealed for 15 min periods in a N_2 atmosphere for temperatures to 1300°C and for 2 min periods in vacuum (10^{-6} Torr) at 1500° and 1700°C. After each anneal the amount of residual disorder was measured at 23°C by the backscattering technique. Before each measurement, the target was washed in HF to remove any thick surface oxide which may have been formed during annealing. In addition, any C deposits, formed by surface decomposition of the SiC during the two high temperature vacuum anneals was removed by oxidation at 600°C. No measurable oxidation of SiC takes place at this temperature.[31] Although not presented, the backscattered spectra for the 9×10^{13} Sb^+/cm^2 implanted layer show regrowth first from only the underlying substrate and then a disorder peak decreasing with increasing anneal temperature.

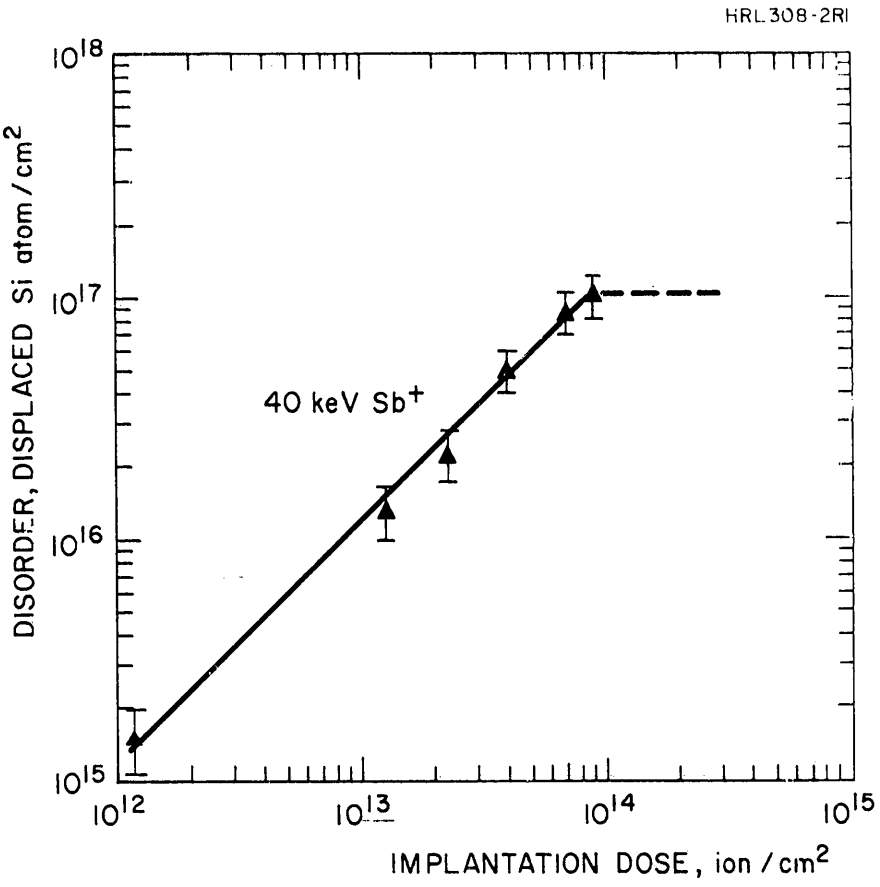


Fig. 43. Disorder in SiC produced by 40 keV Sb implants.

To obtain quantitative anneal data, the disorder was analyzed after each anneal in the same manner as discussed earlier. Figure 44 gives the relative disorder remaining for the Sb implant as a function of anneal temperature. An annealing stage centered around ∿750°C is observed; leveling off to a small amount of residual disorder even after the highest temperature anneals studied here. The dashed line indicates surface decomposition which will be discussed later. The annealing behavior is somewhat less abrupt than that measured after 40 keV Sb^+ implantation into Si at a dose sufficient to produce a saturation level of disorder.[16] In addition, the SiC anneal stage is ∿200 °C higher than the Si anneal stage at ∿550°C. Other investigators have also reported an anneal stage as measured by electrical properties at approximately 800°C in SiC damaged by electrons,[62] protons,[63] and neutrons.[64] It is also interesting to note that the first strong indications of a p-n junction formed by nitrogen implants into p-type SiC are found after a 750°C anneal. Although there appears to be little measurable annealing taking place at temperatures above 1200°C, as shown in Fig. 44, the measured electron Hall mobility of nitrogen-implanted layers in SiC continues to increase significantly with annealing to 1700°C, indicating a strong reduction in the density of electron scattering centers.

e. Decomposition – In order to determine whether implanted heavy ions might significantly diffuse during high temperature anneals, as well as to determine the decomposition temperature, the depth distribution of implanted Tl^+ and Sb^+ ions was also measured by backscattering after each anneal. He^{++} backscattered from Tl atoms implanted at 200 keV to a dose of 8×10^{14} ions/cm^2 and after 1450° and 1650°C vacuum anneals are shown in Fig. 45. The spectra closely

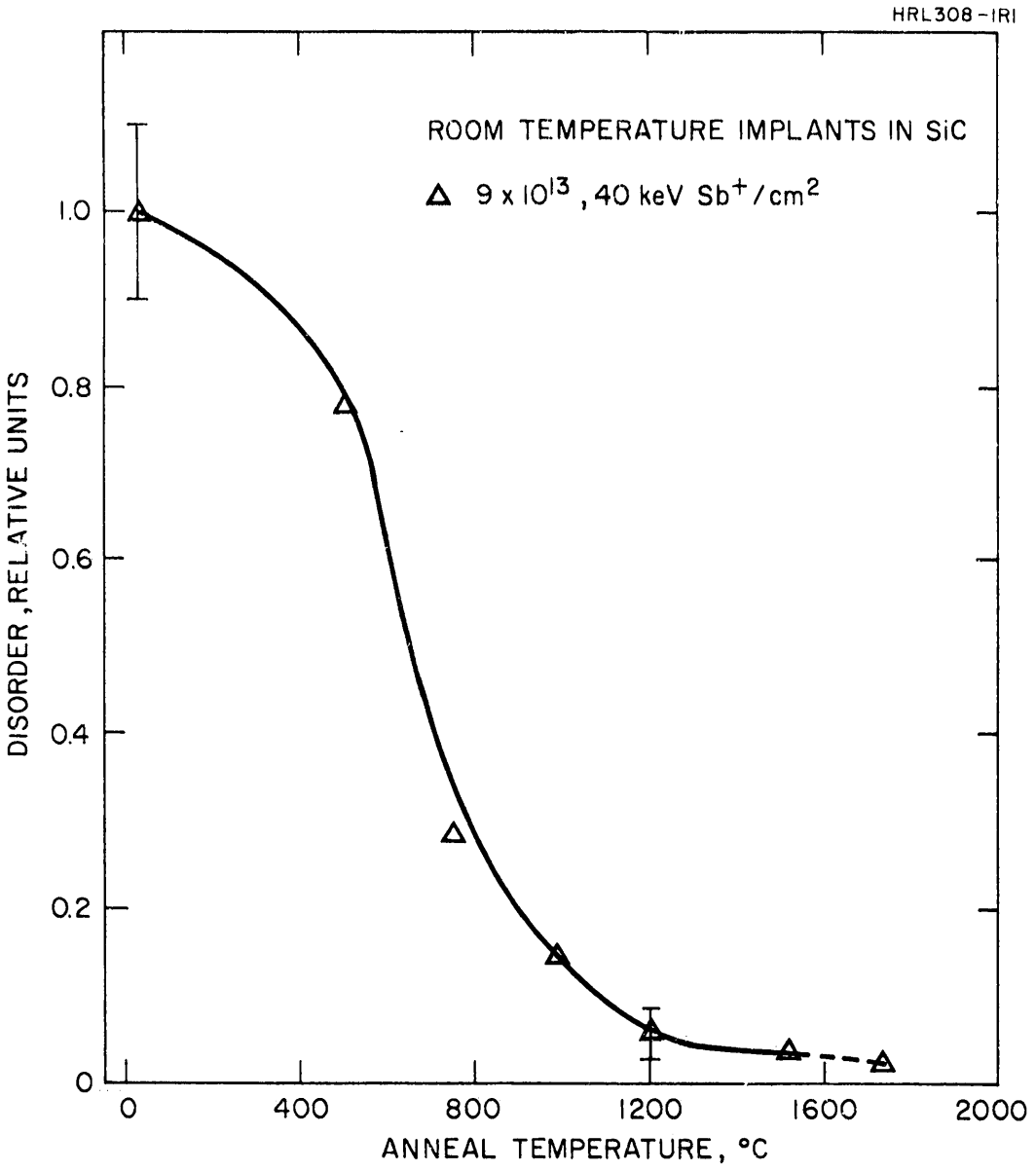


Fig. 44. The annealing of disorder in SiC introduced by 9×10^{13} Sb^+/cm^2.

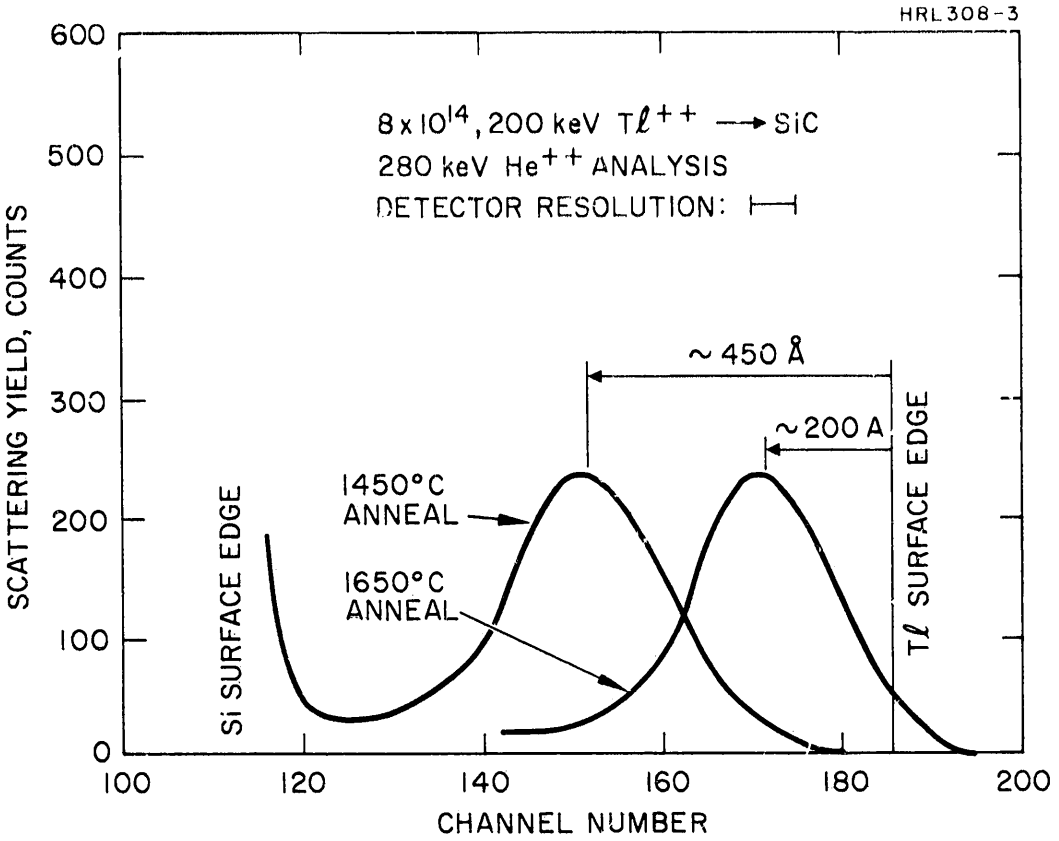


Fig. 45. Spectra of 280 keV He^{++} ions backscattered from Tl implanted at 200 keV to a dose of 8 x 10^{14} Tl^{+}/cm^2 in SiC and after anneal at 1450°C and 1650°C.

represent the depth distribution of the Tl atoms except at the Tl surface edge where the detector resolution must be considered. The Tl surface edge, representing the backscattered energy for Tl atoms on the target surface, was calculated from elastic collision theory, based on the energy of the Si surface edge. The depth scale was obtained from the projected range calculations for Tl in SiC of Johnson and Gibbons.[65] The Tl distribution did not significantly change up to an anneal temperature of 1450°C. However, after 1650°C ∿250 Å of the surface was decomposed. Evidence for this was a visible discoloration of the surface caused by the carbon decomposition product. In addition, there was a significant energy loss of the incident He^{++} before backscattering from Si atoms as shown by a shift to lower energy at the Si surface edge. Removal of the carbon by a 500°C oxidation step eliminated the discoloration and returned the Si surface edge to its normal value. The Tl edge had now moved to the surface with little change in the shape of the distribution. Also there was little loss of Tl atoms since the areas under the two peaks in Fig. 45 are approximately equal. This indicates that the decomposition halted at the leading edge of the implant.

Somewhat similar results were obtained for the 40 keV 9×10^{13} Sb^{+}/cm^{2} distribution as are shown in Fig. 46 after 1500° and 1700°C anneals. Again, no significant change in the Sb distribution was observed, indicating that little diffusion occurred up to 1500°C. After the 1700°C anneal, approximately 75 Å of the surface decomposed, but the decomposition again halted at the leading edge of the implant. Since the shape and area of the Sb peak appears to have changed, some diffusion and loss of Sb may have occurred after the 1700°C anneal. However, the counting statistics for this low dose implant preclude a definitive statement.

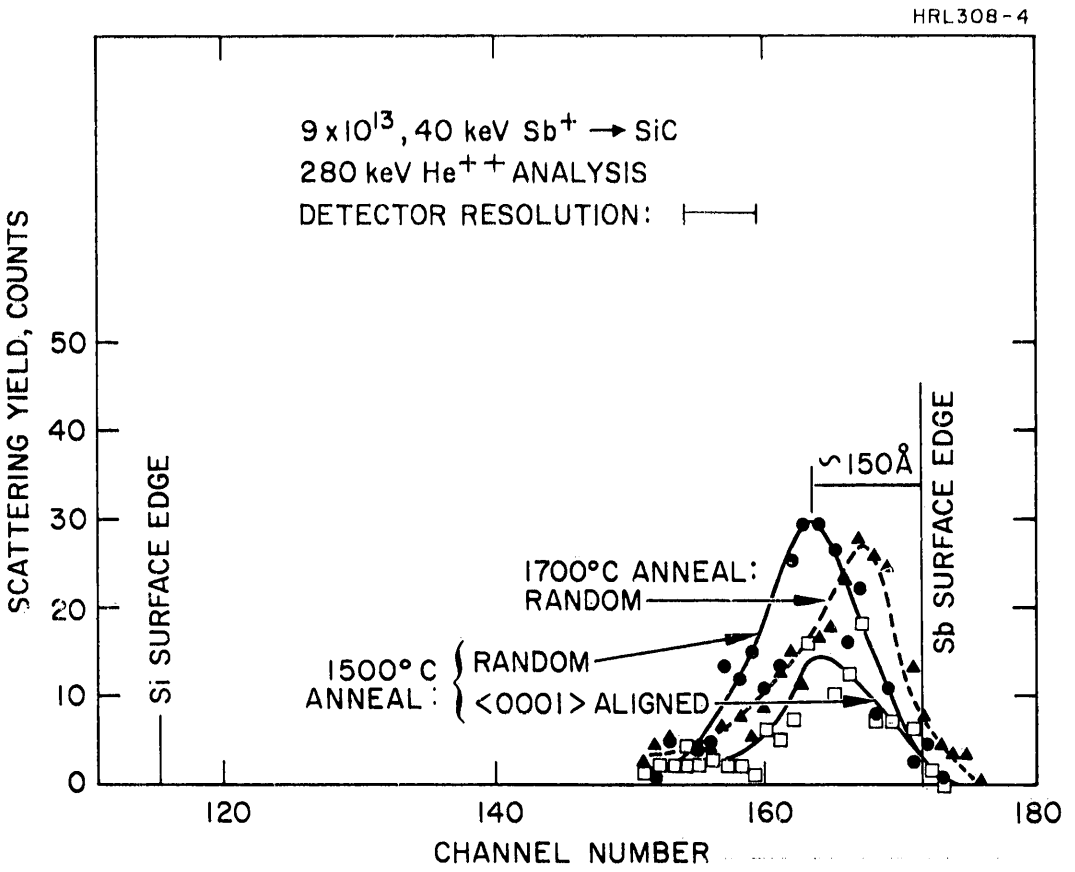


Fig. 46. Spectra of 280 keV He^{++} ions backscattered from Sb implanted at 40 keV to a dose of 9 x 10^{13} Sb^{+}/cm^{2} in SiC and after anneal at 1500°C and 1700°C.

f. Lattice Location of Impurities – Also included in Fig. 46 is an aligned spectrum for the Sb peak after 1500°C anneal. Since the area of the aligned peak is less than the area of the random peak by about a factor of 1/2, approximately 50% of the Sb atoms are along the <0001> atomic rows and appear to be substitutional. This is suggested by a similar reduction in the Sb peak along a channeling direction other than the <0001> (Ref. 16). Previous studies of the electrical behavior of Sb implanted layers in SiC have indicated that an n-type layer is formed.[3] The channeling studies tend to confirm that the n-type behavior is due to donor behavior of Sb in a normal substitutional lattice site.

Analysis of the electrical behavior of layers in SiC implanted with acceptor-type dopants (Column III of the Periodic Table) after annealing at ≈1700°C have not indicated p-type conduction. A possible explanation is that the dopants do not occupy a substitutional site. The Tl implants of Fig. 45 after 1650°C anneal showed no change of the Tl spectrum with aligned and random orientation indicating that no measurable substitutional Tl was present. Although this result tends to confirm the above hypothesis, the dose implanted may substantially exceed the solid solubility for Tl in SiC.

C. CONCLUSIONS

Implantations of the column V dopants N, P, Sb, and Bi have been used to form n-type regions in both α- and β-SiC. Process temperatures of 1100° to 1500°C are required after implantation at either 23° or 500°C in order to obtain a p-n junction and an n-layer with sufficient conductivity to perform Hall effect measurements. Surface carrier concentrations of 1/2 to 1/3 the implanted dose are found, and this

value does not change with additional annealing. These values are somewhat dependent upon dose rate. Anneal temperatures of 1600° to 1700°C are required in order to obtain carrier mobilities that are equivalent to bulk values measured for similar doping levels.

Scanning electron microscope analysis of the disorder introduced by implantation indicates that a reordering of the lattice is complete after annealing at 1600°C.

Little or no success in creating p-type SiC has been obtained as yet using implant and anneal procedures similar to those used for the n-type dopants. Most of the common dopants of Column III (B, Al, Ga, and Tl), as well as other known p-type dopants (Be) have been tried. A number of possibilities exist to explain the absence of p-type behavior in these layers. Some possibilities are improper location of the impurity in the lattice, compensating donor defects, or outdiffusion of the impurity during anneal.

The diode behavior of implanted junctions annealed at 1100°C are characteristic of a p-i-n structure. The i-region decreases in thickness with increasing anneal temperature. The current-voltage characteristics for diodes annealed at 1500°C or above are of excellent quality with forward I-V characteristics determined by recombination in the space charge region over most of their operating range. Avalanche breakdown has been observed at ∿45 reverse bias and is caused by microplasmas which occur at visible defects in the material. The temperature and frequency dependence of the C-V data indicate the presence of a deep level which is satisfactorily explained in terms of the bulk properties of the SiC rather than to the presence of defects introduced by implantation.

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