The Schwaigerian Driver Transfer Technique and The Thevenin's and The Norton's Theorem

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SUMMARY

Schwaiger[12] introduced a graphical technique in order to analise series-parallel networks in the form of rectangular diagrams with the aid of these in a forward process he was able to obtain equivalent drivers while in the reverse process he obtained the solution of the network. In this article it is shown that the equivalent drivers, that Sch... er obtained by a step-by-step graphical transfer of drivers is nothing else ... ... equivalent. Subsequently the rectangular diagram proofs of the Thevenin's and the Norton's theorem's are deduced.

INTRODUCTION

Rectangular diagrams were first introduced by Schwaiger[12]. His method will be exposed in this article, an indirect form of rectangular diagrams to solve power distribution systems. In his indirect form, the diagrams are used like a slide rule to aid the solution. In the direct reading form, that we will also use in this article, the element values, voltages, currents, and even the consumed and supplied powers, can be directly read from the diagrams. These type of diagrams were used by Magyari[10] to solve linear resistive and reactive networks, by Kovattana[9], Cherry[1] and Erdey[5] to solve non-linear resistive networks. Linear and non-linear network properties and theorems in rectangular diagram form were exposed by Cherry[1], Erdey[2,3,4,7], Magyari[10] and Mayne[11].

On Fig. 1-a a linear resistive network is given. Its rectangular diagram is given on Fig. 1-b. On this diagram each element is represented with a component rectangle, the vertical side of which represents the voltage across, and the horizontal side represents the current through, while its area gives the power through the element. In cases of linear resistors as in the given example the slope of the diagonal gives the element value while the non-linear elements are represented with their general v-i characteristic curves. Studying rectangular diagrams with dual non-linear elements with the aid of rectangular diagrams led Cherry[1] to his "Classes of 4-Pole Networks having Non-Linear Transfer Characteristics but Linear Iterative Impedances".

In cases of linear resistive networks there is a straight forward construction technique coined by one of the authors as "locus method" since the loci of the vertices of the individual rectangles move on straight lines, as the size of the rectangle is proportionally increased or decreased. Fig. 2 shows the case when the size of a rectangle is proportionally enlarged into the rectangle drawn with the broken sides. The proportionality ensures that the diagonals will have the same slopes, which ensures that the element value of the resistor is not changed by this process. The loci of the four vertices always intersect each other in one common point (point P on Fig. 2). The physical meaning of this is that in the case when no current is flowing through a resistor the voltage across it will also become zero (rectangle shrinks into a point). This method is a routine operation in case of planar networks but becomes a little more cumbersome in case of non-planar networks[8].

The Schwaigerian Method of Step-byStep Transfer of Drivers

Let's take the two series connected R_1 and R_2 elements of Fig 3-a in which only R_1 is excited by the ideal current driver i_g. On Fig 3-b an equivalent current driver i_e is given which produces the same voltage across nodes A and C that i_g produces across the terminals on Fig. 3-a. The Schwaigerian graphical solution of the equivalent current is given on Fig. 3-c. On this diagram the two series connected elements are treated as if the same i_g current is flowing through both of them in order to define the R_{12} resultant resistance. The operating point of the R_1 resistance of Fig. 3-a is at point P_1. Since the R_2 element in this network is idling the voltage across the terminals A and C is the same as that of the B and C. In order to obtain the same voltage across the A and C nodes on Fig. 3-b, we have to move the P_1 point to the left until it intersect the R_{12} resultant resistance line at P_2. The perpendicular from P_2 to the base cuts the length of the i_e equivalent current, and which we will show that is equal to the Nortonian equivalent current, which is obtained by short - circuiting the pair of terminals. By short - circuiting terminals A and C we obtain Fig. 3-d, where the short - circuit current is equal to the current flowing through element R_2. We have to show that this current is equal to the one in Fig. 3-b. This is obtained graphically on Fig. 3-e.

On Fig. 3-e the excited resistor of Fig. 3-a is given by $P_1P_2P_3P_4$ ▱, while Fig. 3-b is represented by the $P_8P_2P_3P_9$ ▱. Since both the rectangles have the same height $(\overline{P_2P_3})$ the terminal voltages are the same in both the cases as required. The parallel connected R_1 and R_2 resistors of Fig. 3-d are given by $P_1P_2P_5P_7$ ▱. It can be noticed that the current through R_2 element (represented by $\overline{P_8P_2}$ remained the same in Figs. 3-b and d, and thus we have shown that the Schwaigerian equivalent driver and the Nortonian are the same for this particular case.

The Schwaigerian graphical driver transfer technique was demonstrated for a series connected elements on Fig. 3. It is very east to demonstrate that the same technique can be applied to any series parallel connected network.

The Thevenin's and The Norton's Theorem.

It was just pointed out with a particular example the Schwaigerian equivalent current driver, which is obtained by a step-by-step transfer of drivers to a preditermined pair of terminals is nothing else but current driver in the Norton's equivalent. Since the Thevenin's and The Norton's equivalents of a two terminal active networks are closely interrelated to each other, we will expose these theorems in their graphical forms in order to obtain a visual image and understanding of these basic equivalencies.

Let's take the two-terminal linear active network N of Fig. 4 which a load L (which may be a second network) is connected across its terminals. The active network N can be represented with a voltage driver in series with an impedance (Thevenin representation) or with a current driver shunted by the same impedance (Norton's representation). When the load is disconnected the terminal voltage of N is equal to the terminal voltage of the ideal voltage driver in the Thevenin's equivalent. When the load is replaced with a short - circuit, the current through the short - circuit is equal to the terminal current of the ideal current driver in the Norton's equivalent. The series impedance in the Thevenin representation and the shunt impedance of the Norton's representation are equal to each other and equal to the input impedance of network N, looking into it at its terminals, when all internal drivers have zero value.

It can be shown that simisoidally excited RLC networks can be represented with rectangular diagrams too since their vector diagrams can be broken into inphase and quadrature components. Since the components themselves are real quantities, naturally the component rectangular diagrams have the same characteristics as the rectangular diagrams of resistive networks. Therefore, without any loss from generality we can confine ourselves to the rectangular diagrams of resistive networks when we prove The Thevenin's and The Norton's theorem.

The simplest case of the Thevenin's and The Norton's equivalent is usually referred by driver or source transformation in the literature. Its simple graphical proof is given on Fig. 5 as follows: Let us consider a practical voltage driver. As indicated on Fig 5-a it can be decomposed into an ideal driver series with a resistor (Thevenin equivalent). This decomposition can be justified by measurements. If we measure the open circuit voltage of the practical driver, we can assign this v_0 value for the ideal driver on Fig 5-a. When a load is connected across its terminal (Fig 5-b) then from the load resistance R_2 and the v_L voltage across the load according to the rectangular diagram of Fig. 5-c, the R_i internal resistance can be defined. When the terminals of this practical driver are short - circuited its corresponding diagram is given in Fig. 5-d. Further, when this driver is loaded by another resistor R_L Fig 5-e the diagram for the complete network can be constructed as shown in Fig. 5-f. In this figure, the broken lines complete the diagram into that given in Fig. 5-d and one can see that given in Fig. 5-d and one can see that the terminal conditions for R_L will not change if R_i were connected in parallel to R_L rather than series to it and also if the voltage driver v_o is replaced by a current driver i as is shown in Fig. 5-h. This diagram corresponds to the network in Fig. 5-g and its left sides is called the Norton's equivalent of the practical driver which is loaded by R_L.

We will prove the general case of the Thevenin's and The Norton's Theorem with the aid of superposition theorem; that is we are taking into account the effects of each driver separately. We can assume that all drivers are current drivers. If this would not be the case with the given driver transformation technique, that we have just seen on Fig. 5. In case if we take into account each driver separately we have two possibilities:

a. The equivalent driver has a common node with the original driver

b. The equivalent driver has no common node with the original driver.

SOLUTION OF THE TWO SUBCASES

If we have the first case at hand then we can eliminate all vertices with the aid of of $Y-\Delta$ or Rosen's transformation*, except the 3 vertices that are involved in the problem. After this process the network will have the form of Fig. 6-a. The rectangular diagram solution to this problem is given on Fig. 6-c. When nodes B and C are shorted the network has the form of Fig. 6-b, the solution of which is given in Fig. 6-c by $P_3P_4P_5P_6$ ▱. In Fig. 6-d an equivalent driver is connected across terminals B and C. The rectangular diagram solution of the network with the equivalent driver is given in Fig. 6-c with $P_2P_7P_8P_9$ ▱, the width of which is the same as the width of the R_2 rectangle in the short - circuited case. Thus, we have proved that the short - circuit current Is equal to the Norton's equivalent current.

In the case of the Thevenin's equivalent we have to find the open circuit voltage at the required pair of terminals. In Fig. 7-c with the $P_1P_2P_3P_4$ ▱, the conditions of the origianl loaded network of Fig. 6-a are repeated. When the terminals are open circuited (R_L removed) Fig. 7-a is obtained. The form of the solution in this case is given by $P_1P_{14}P_{15}P_4$ ▱. In order to adjust the diagram to the applied current I_a the diagram has to be proportially enlarged into $P_1P_2P_{12}P_{13}$ ▱. In this enlarged diagram the open circuit voltage (voltage across the R_3 element) is given by $\overline{P_2P_0}$. Let's show that the voltage V_0 thus obtained is as an ideal voltage driver connected in series to the internal resistance of the network of Fig. 7-a

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* The graphical form of the $Y-\Delta$ and of its generalization, the Rosen's transformation, was presented by the authors in another paper[7].

and applied to the R_L, load (as given on Fig. 7-b) then the solution for R_L remains the same as the one we had in the orginal network. Let's add in series R_2 of the $P_8P_5P_3P_{11}$ ▱ to R_1 of the $P_{11}P_3P_6P_7$ ▱ Where the resultant R_{12} line intersects the R_3 line we obtain the point Q_L. It can be shown that Q is at the same level of P_0. Thus the rectangular diagram solution of the network in Fig. 7-b is given by $P_2P_0P_9P_{10}$ ▱. Since the original rectangle of R_L is an intact subrectangle of the obtained solution we have just verified the validity of the Norton's equivalent for the case a.

In the case of b after the elimination of the vertices to which neither the given driver nor the load is connected we obtain the form in Fig. 8-a. Note that in the given form any of the five G_1 to G_5 conductances can be zero. This will mean that the pertinent rectangle will have a zero width, but otherwise the procedure will be the same.

In Fig. 8-c the $P_{24}P_{27}P_{28}P_{31}$ ▱ is the solution of the network of Fig. 8-a. When nodes B and C are short circuited, in order to obtain the Norton's equivalent current, the Fig. 8-b is obtained. In this case in the rectangular diagram the intersection point of the resistance lines of the parallel R_1 and R_2 lines is at P_{21} and similarly the R_3 and R_4 lines intersect each other in point P_2. The horizontal distance between these two pointsis equal to $\overline{P_1P_2}$ and is equal to the short - circuit current. On Fig 8-e this current is used in the Norton's equivalent across the B and C terminals parallel to the internal resistance of the de-energized network of Fig. 8-a looking into it at terminals B and C. This equivalent network is driving the R_L load. The rectangular diagram solution except relative positions of the rectangles of the network on Fig. 8-e is given by the $P_6P_7P_8P_5$ ▱ on Fig. 8-c. Just for the sake of clarity the solution is redrawn on Fig. 8-d once again. Since the size of the R_L rectangle on this diagram remained the same as before, thus it is proved that as far as the load is concerned the two networks (Figs 8-a and e) are equivalent.

It is sufficient to obtain the Norton's equivalent to any configuration, since the driver transformation shown on Fig. 5 can convert it into the Thevenin's form. Just to show the reader how the Thevenin's equivalent is obtained the additional construction lines in Fig. 8-c are related to the finding of the Norton's equivalent voltage is found in the particular case when $G_5 = 0$ and R_L is the resultant of the previous parallel R_L and R_5. In this particular case, the open circuiting procedure makes R_1 and R_3 and similarly R_2 and R_4 elements series to each other. The intersection of the pertinent resistance lines is at P_{22} and P_{23}. In order to eliminate the gaps between the left and right sections the resultant R_{13} and R_{24} rectangles are proportionally enlarged till they intersect each other at P_o.

After the enlargement P_{22} moved to P_4 and P_{23} to P_3. Thus the open circuit voltage for this particular case is given by $\overline{P_3P_4}$. The reader should notice that the Norton's equivalent in this particular case is the same as before. Thus the $P_{17}P_{18}P_{19}P_{20}$ ▱ represents the I_s V_o rectangle the diagonal which should represent the input resistance across terminals B and C. This can be seen from the fact that this rectangle breaks down into a series of subrectangles of elements R_3 and R_4 and parallel to them are the series rectangles of elements R_1 and R_2.

The General Case

In the above procedures the drivers were taken into account individually. This is possible since we were dealing with linear networks and thus superposition theorem is applicable. Since the equivalents each time are taken across the same pair of terminals the input impedance of the network remains the same and the short - circuit current will be the same as the short - circuit currents with the individual drivers.

REFERENCES

1. Cherry, E. C. : "Classes of 4- Pole Networks Having Non-Linear Transfer Characteristics but Linear Iterative Impedances", Proceedings I.E.E. vol. 107, part B, pp. 26-30 (1960).

2. Erdey, M. R.A.: "Rectangular Diagrams and Their Applications to Network Theorems", Proceedings of the Sixth Midwest Symposium on Circuit Theory, pp. F-1 to F-17, Madison, Wisconsin (1963).

3. Erdey, M.R.A.: "The Misrepresented Duality and the Rectangular Diagram", Proceedings of the IEEE Region III Convention, pp. 9.51-9.5.10, New Orleans, Louisiana (1968).

4. Erdey, M.R.A.: "Rectangular Diagrams in Graph Theory", Proceedings of the Eleventh Midwest Symposium on Circuit Theory, pp 441-456, Notre Dame, Indiana (1968).

5. Erdey, M.R.A.: "Iterative Solution of Same Non-Linear Resistive Networks with the Aid of the Rectangular Diagrams", Proceedings of the Eleventh Midwest Symposium on Circuit Theory, pp. 371-388, Notre Dame, Indiana (1968).

6. Erdey, M.R.A. and Murty, B. V.G.K.: "Graphical Methods in the Design of Resistor - Transistor - Logic Circuits", Proceedings of the 12-th Midwest Symposium on Circuit Theory, pp. XIV 4.-1 - XIV. 4.10, Austin, Texas (1969).

7. Erdey, M.R.A. and Ding, J. L.: "Graphical Form of Rosen's Transformation", Proceedings of the 12-th Midwest Symposium on Circuit Theory, pp. XIV.3.1-XIV 3.14, Austin, Texas (1969).

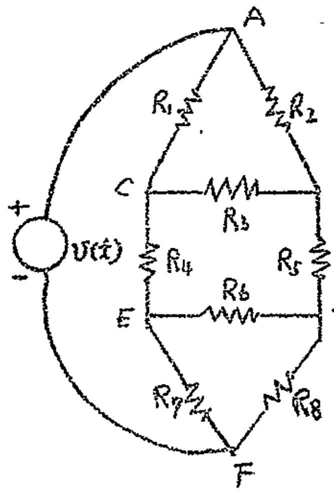
8. Erdey, M. R. A. and Ding, J. L.: "Graphical Solution of Non-Linear Networks", First Southeastern Symposium on System - Theory pp. F4-1 to F4-19 (1969).

9. Kovattana, T. and Barker, J. R. : "Solution of Ladder Networks Containing Non-Linear Resistance", British Journal of Applies Physics, Vol. 11, pp. 437-439, (September 1960).

10. Magyari, E.: "Grafijus Szamitasok a Hiradas Technikaban", Muszaki Konyvkiado, Budapest, Hungary (Vol. I. in 1958, Vol.II in 1966).

11. Mayne, D.Q.: "An Analogy Between Non-Linear Resistive and Linear A. C. Networks", Proceedings I.E.E., Vol. 107; part B, pp. 410-411 (1960).

12. Schwaiger, A. : "Elektrische Leitungen, "Leibnitz-Verlag, Munchen 1948.


A
B
C
D
E
F
R_1
R_2
R_3
R_4
R_5
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R_7
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+
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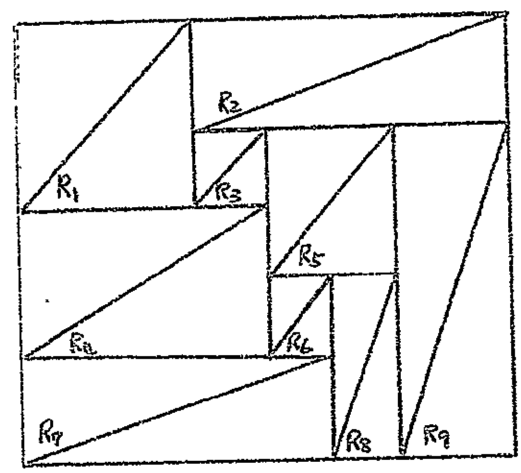
$v(t)$

(a)

FIG. 1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R_4
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R_8
R_9

(b)

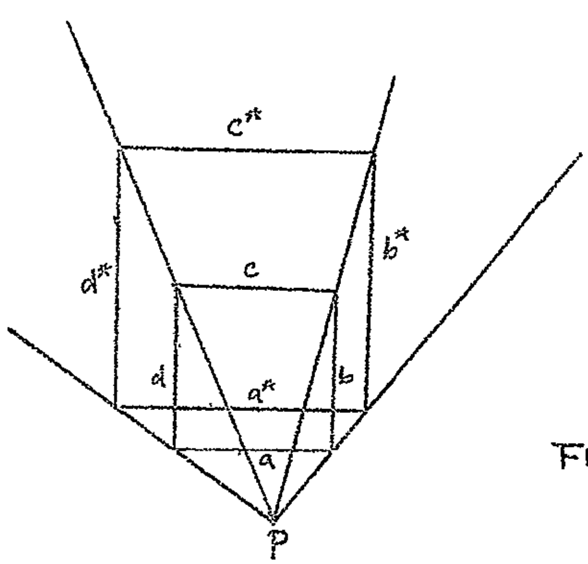
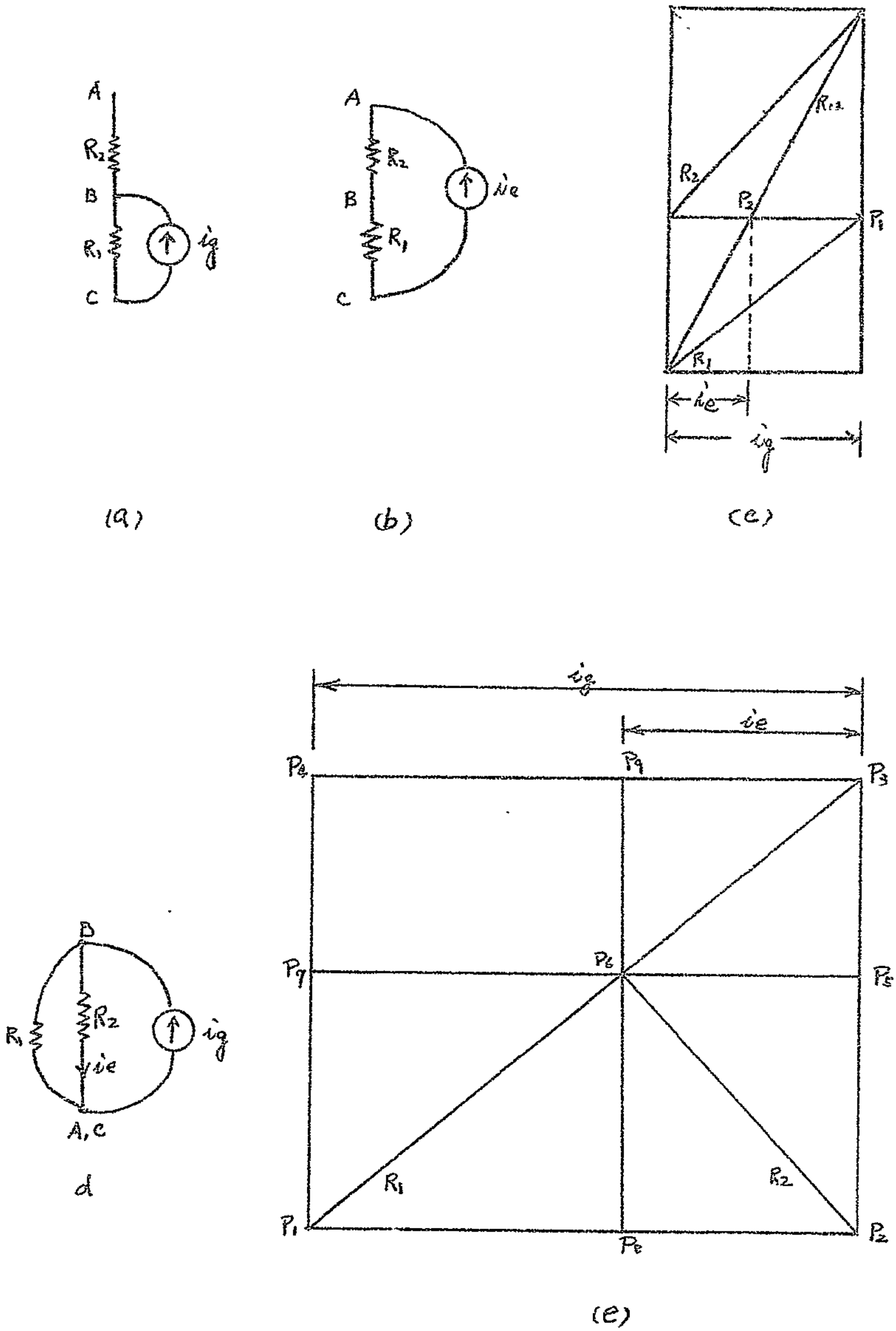

c^*
d^*
b^*
c
d
b
a^*
a
P

FIG. 2



A
R2
B
R1
C
ig
(a)
A
R2
B
R1
C
ie
(b)
R12
R2
P3
P1
R1
ie
ig
(c)
B
R1
R2
ie
ig
A, C
d
ig
ie
P8
P9
P3
P7
P6
P5
R1
R2
P1
P8
P2
(e)

FIG. 3

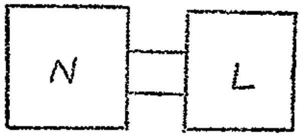
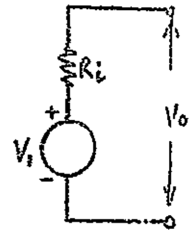
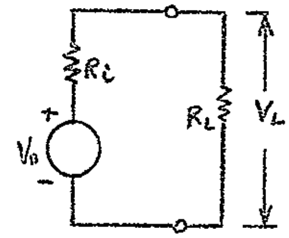


FIG. 4



(a)



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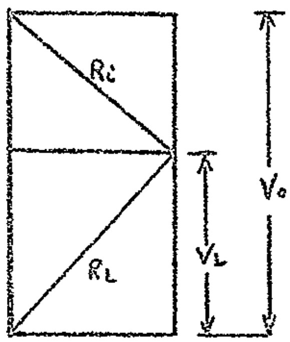

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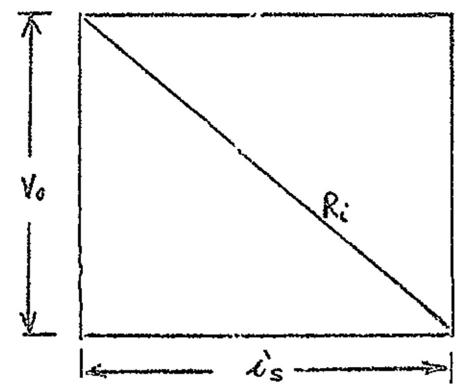

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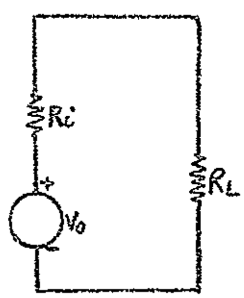

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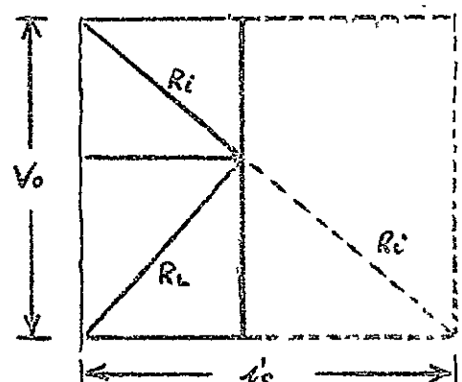

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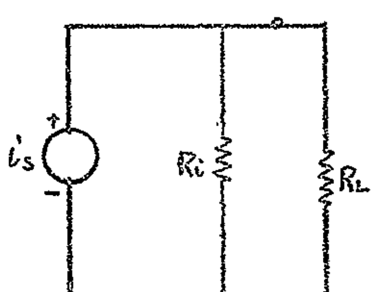

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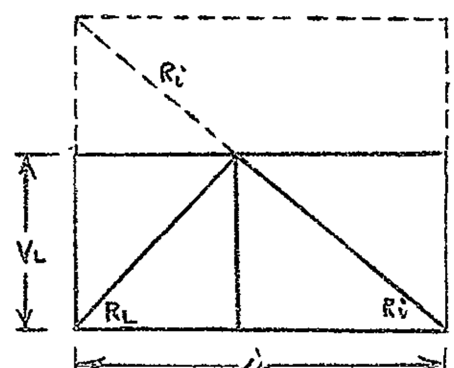
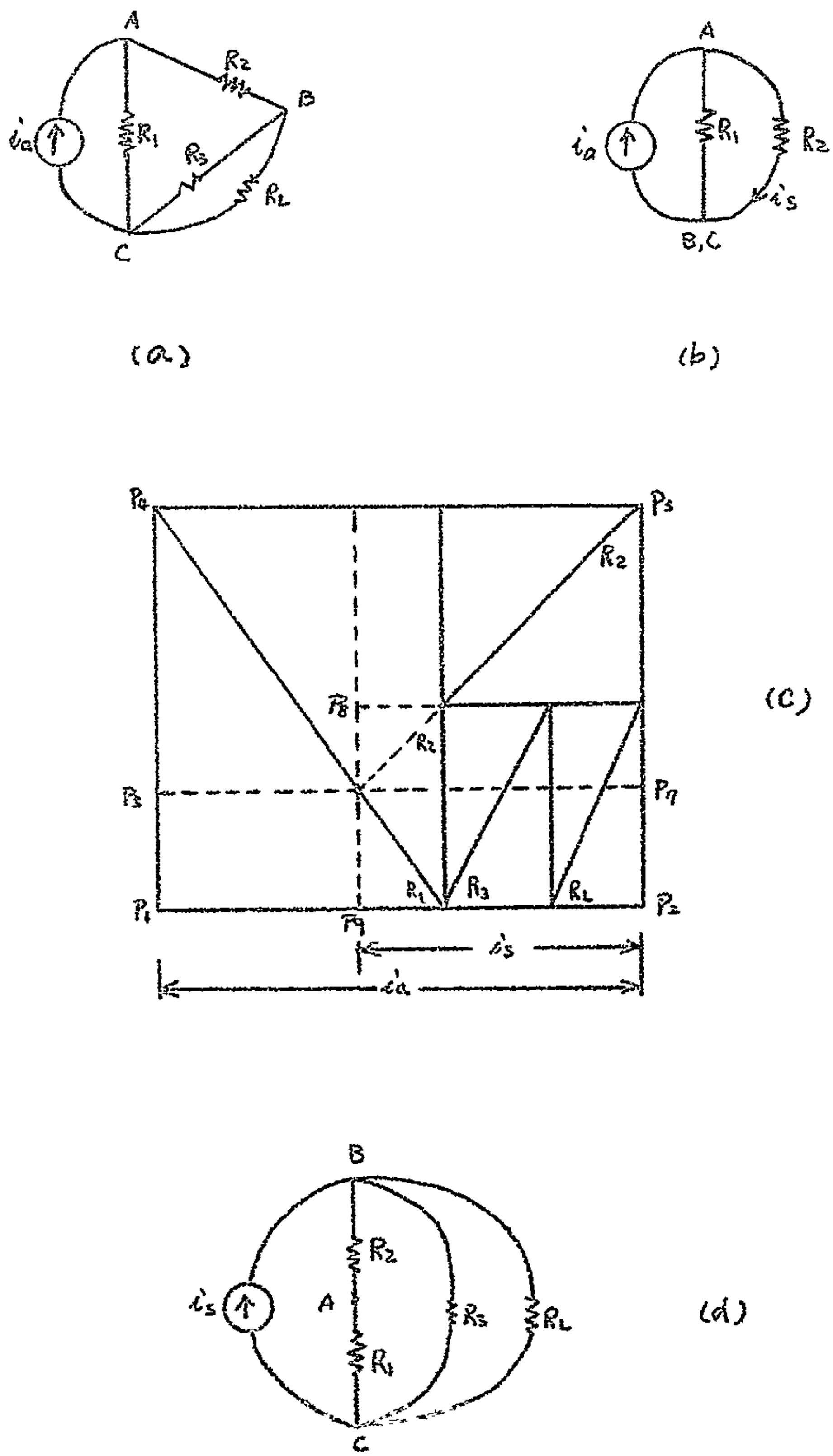


(h)

FIG. 5



A
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C
R2
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(a)
A
R1
R2
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(b)
P4
P5
P3
P7
P8
P9
P1
P2
R1
R2
R3
RL
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(c)
B
A
C
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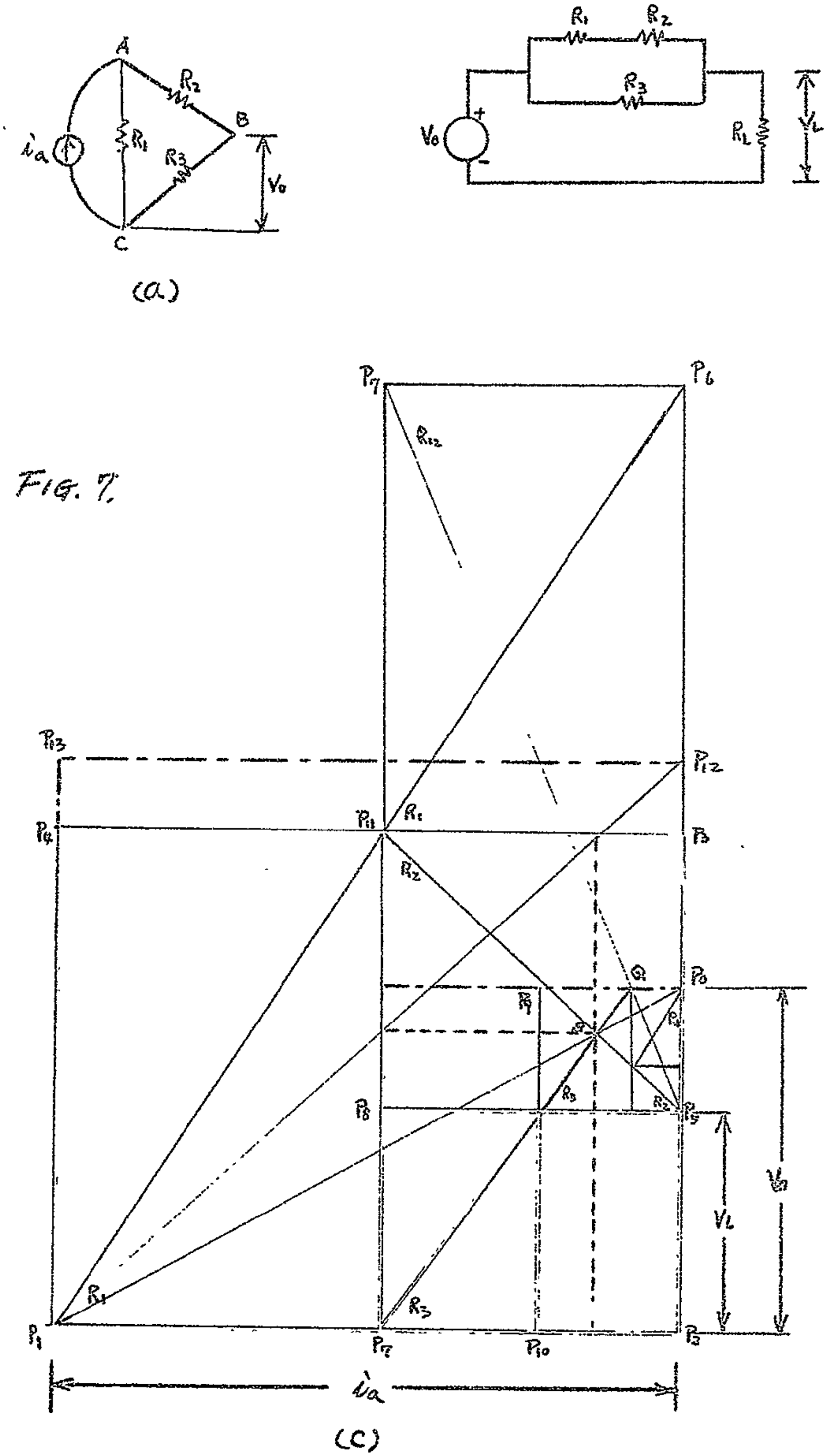
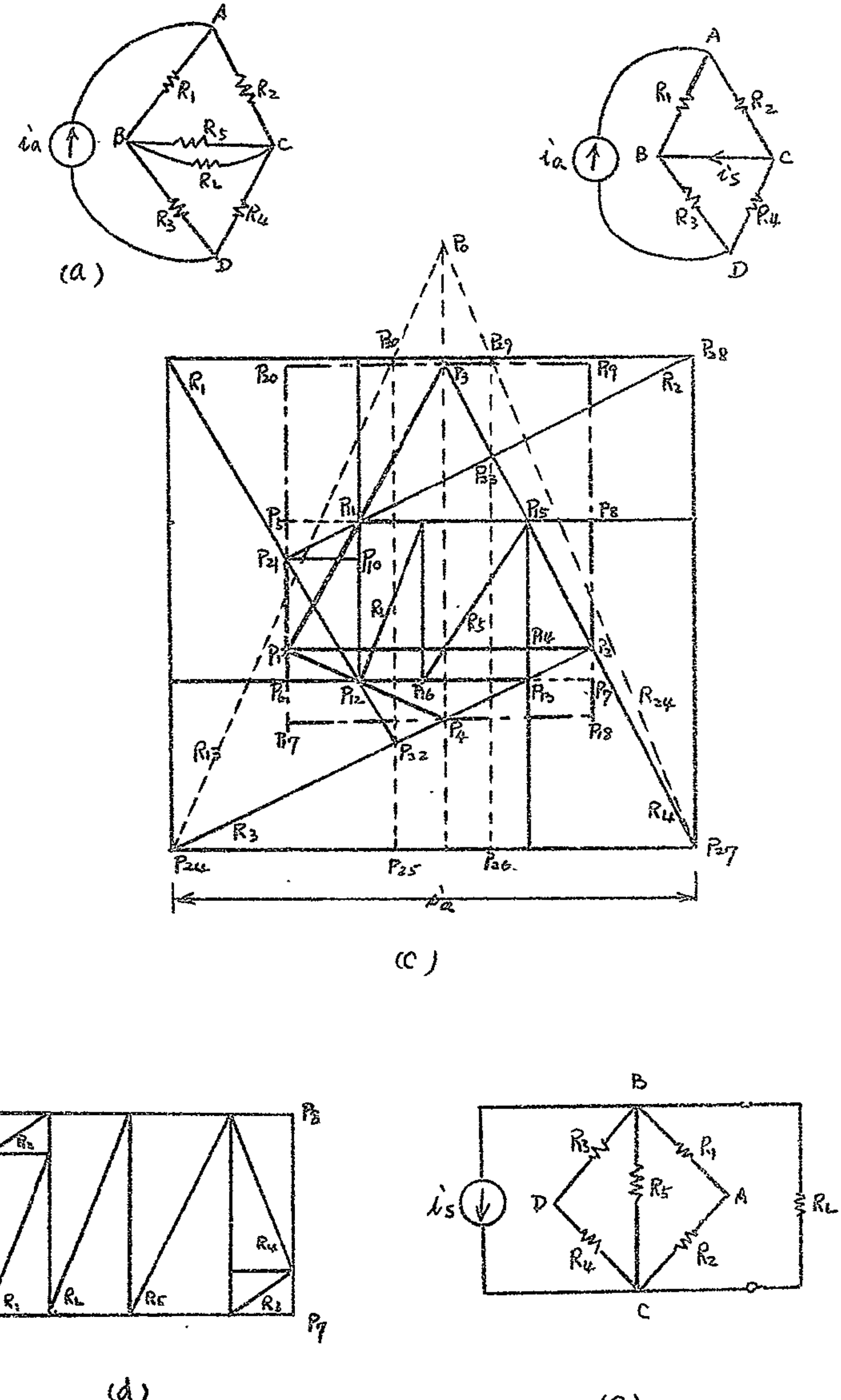
R1
R3
RL
is
(d)

FIG. 6

FIG. 7.


A
B
C
i_a
R_1
R_2
R_3
V_0
(a)
R_1
R_2
R_3
V_0
+
-
R_L
V_L
P_7
P_6
R_{12}
P_{13}
P_{12}
P_4
P_{11}
R_1
P_3
R_2
Q
P_0
P_9
R_3
R_2
P_8
P_5
V_L
V_0
R_1
R_3
P_1
P_{2}
P_{10}
P_3
i_a
(c)



(a)
A
B
C
D
R1
R2
R3
R4
R5
RL
ia
is
P0
P1
P2
P3
P4
P5
P6
P7
P8
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P10
P11
P12
P13
P14
P15
P16
P17
P18
P19
P20
P21
P24
P25
P26
P27
P28
P29
P30
P32
(c)
(d)
(e)

FIG. 8