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VOLUME II OF II

FINAL REPORT

FOR

DESIGN AND DEVELOPMENT STUDY FOR A SPACE BASE MULTIPLE SOCIAL MODEL (SBMS)

DECEMBER 1970

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N71-21459 (ACCESSION NUMBER)
92 (PAGES)
CR-114927 (NASA CR OR TMX OR AD NUMBER)
(THRU)
(CODE)
07 (CATEGORY)

FOR

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
MANNED SPACECRAFT CENTER
HOUSTON, TEXAS

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VOLUME II OF II

FINAL REPORT

FOR

DESIGN AND DEVELOPMENT STUDY FOR A SPACE BASE MULTIPLE SIGNAL MODEM (SMDS)

DECEMBER 1970

CONTRACT NO: NAS9-10417

MANNED SPACECRAFT CENTER
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abstract

VOLUME II OF THIS REPORT FOR A "DESIGN AND DEVELOPMENT STUDY FOR A SPACE BASE MULTIPLE SIGNAL MODEM" CONTAINS THE BASIC TECHNICAL DESCRIPTIONS AND SPECIFICATIONS FOR THE MODULES NECESSARY TO IMPLEMENT SUCH A SYSTEM. ADDITIONALLY AREAS FOR CIRCUIT, MICROCIRCUIT, AND COMPONENT DEVELOPMENT ARE IDENTIFIED.

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SECTION 6.0

SMDS SUBSYSTEMS

6.0 SMDS SUBSYSTEMS

This second volume of a Study for a Space Base Multiple Signal Modem contains the technical descriptions and development specifications for modules and subunits required to mechanize the Space Base Telecommunications System described in volume I of this report. This system has been designed with a maximum of commonality and modularity and, as a result, a minimum of central (or systems) controls. The elements comprising the Signal Multiplex Demultiplex System (SMDS) are virtually self-contained and require a minimum of systems description.

Technical descriptions and specifications for the six major building blocks used in the SMDS, appear in sections 7 through 12 of this report. The equipments which use these building blocks as their component parts are the Pilot and Terminal Modem, Base Level/Dock Level Interface Unit, the Video Camera Modem, and the Video Monitor Modem. The development specifications for these pieces of equipment appear in this section. The material discussing system design problems and their resolutions have been previously described in volume I of this report, particularly in section 4.0. The remaining development specifications appearing in this section are for the coupling devices necessary for complete systems implementation (the VHF Main Bus Bidirectional Coupler and the UHF Signal Power Divider/Combiner specifications).

6.1 DEVELOPMENT SPECIFICATIONS

The following development specifications are provided as a part of this section:

1. SMDS Pilot and Terminal Modem
2. SMDS Base Level/Deck Level Interface Unit
3. SMDS Video Terminal (Camera Video Terminal) (Monitor Video Terminal)
4. SMDS Bidirectional Coupler

SMDS

PILOT AND TERMINAL MODEM

DEVELOPMENT SPECIFICATION

1.0 SCOPE

This specification describes the development design goals and major performance specifications of a SMDS major module building block identified as the Pilot and Terminal Modem.

2.0 APPLICABLE DOCUMENTS

a. The guidelines, trade-offs, and functional descriptions included as part of the SMDS Final Report shall be considered as part of the Module specification.

b. SMDS Modulator Group Development Specification

c. SMDS Demodulator Group Development Specification

d. SMDS Wideband UHF Amplifier Development Specification

e. SMDS UHF Signal Power Divider/Combiner Development Specification

3.0 ELECTRICAL PERFORMANCE SPECIFICATIONS

The SMDS Pilot and Terminal Modem serves four basic functions. These are:

1. To receive and demodulate both the SMDS master clock signal and the loop clock signal.

2. To phase lock the loop timing signal to the master clock signal.

3. To modulate and output the loop timing signal.

4. To compare the loop timing signal output with the loop timing signal input for error conditions.

3.1 UHF Input Signal Interfaces

a. The Pilot and Terminal Modem shall accept a UHF VSB modulated Master Timing Signal in the 300 to 500 MHz spectrum from the SMDS Main Bus UHF Power Divider.

b. The Pilot and Terminal Modem shall accept a UHF VSB modulated loop timing signal from the SMDS Main Bus UHF Power Divider.

3.2 UHF Output Signal Interface

a. The Pilot and Terminal Modem shall provide a UHF VSB modulated Loop Timing signal to the SMDS Main Bus UHF Power Combiner.

3.3 Interface Characteristics

The Pilot and Terminal Modem shall have electrical interfaces corresponding to those defined for the individual subunits comprising the unit. The conceptual Block Diagram shows the interfaces of these subunit building blocks.

3.4 Phaselock Loop Requirements

The phaselock loop static phase error shall be less than .1 radian.

The phaselock loop time constant shall be greater than 1 millisecond and less than 100 milliseconds.

3.5 Size, Weight, and Power Consumption

The size, weight, and power consumption of the Pilot and Terminal Modem shall be consistent with the recommended mechanical and maintainability guidelines recommended for the SMDS and within the packaging and interconnection constraints imposed by the redundant integral subunits which comprise the SMDS unit.

3.6 Redundancy Requirements

The subunits which comprise the Pilot and Terminal Modem shall incorporate block redundant subunits in such a manner as to allow required switching of units and individual replacement of failed units on a non-interference basis with operating basis. The size, weight, and power consumption requirements for this unit (Paragraph 3.5) shall include packaging, weight, and power considerations for implementing the redundancy and associated switching implementation described in the SMDS Final Report.

3.7 Miscellaneous Design Guidelines

The Pilot and Terminal Modem development specifications must be considered flexible in terms of developing a totally integrated SMDS design. Trade-offs not considered or problems not recognized in this conceptual phase of the SMDS study may require deviations from the specifications stipulated above.

SMDS VIDEO TERMINAL DEVELOPMENT

(VIDEO CAMERA TERMINAL)

(VIDEO MONITOR TERMINAL)

DEVELOPMENT SPECIFICATION

1.0 SCOPE

This specification describes the design goals and major performance specifications of two SMDS major modules identified as SMDS Camera Video Terminal and as SMDS Monitor Video Terminal.

2.0 APPLICABLE DOCUMENTS

a. The guidelines, trade-offs and functional descriptions included as part of the SMDS Final Report shall be considered as part of the Module Specification. References cited in the Final Report shall be used for developmental guidance.

b. SMDS Modulator Group Development Specification

c. SMDS Demodulator Group Development Specification

3.0 ELECTRICAL PERFORMANCE REQUIREMENTS

The SMDS Camera Video Terminal consists solely of a SMDS Modulator Group co-located with its associated color camera or other color television video signal source interface; i.e., ground to space link video interface. The SMDS Monitor Video Terminal consists solely of a SMDS Demodulator Group co-located with its associated color television monitor or other color television signal processing interface; i.e., video recorder or space to ground video link interface unit. Appropriate mechanical mounting provisions of the SMDS Modulator and Demodulator Groups for Video Terminal applications shall be provided at the associated camera and monitor equipments. Electrical Performance Requirements of the Camera and Monitor Video Terminals are identical to those of the SMDS Modulator and Demodulator Groups, respectively. These specifications appear in sections 7.0 and 8.0.

SMDS BASE LEVEL/DECK LEVEL

INTERFACE UNIT

DEVELOPMENT SPECIFICATION

1.0 SCOPE

This specification describes the devleopment design goals and major performance specifications of a SMDS major Module building block indentified as the Base Level/Deck Level Interface Unit.

2.0 APPLICABLE DOCUMENTS

a. The guidelines, trade-offs, and functional descriptions included as part of the SMDS Final Report shall be considered as part of the Module specification. References cited in Final Report shall be used for developmental guidance.

b. SMDS Modulator Group Development Specification

c. SMDS Demodulator Group Development Specification

d. SMDS Wideband UHF Amplifier Development Specification

e. SMDS UHF Signal Power Divider/Combiner Development Specification

3.0 ELECTRICAL PERFORMANCE REQUIREMENTS

The SMDS Base Level/Deck Level Interface Unit serves five basic functions as a deck level equipment assembly. These are:

a. To demodulate UHF VSB modulated telecommunications signals (telephone, intercom and digital data) originating at other space base deck levels.

b. To distribute UHF VSB modulated television signals originating at other space base deck levels to deck level Video Monitor Terminals.

c. To VSB modulate baseband telecommunications signals originating at the deck level (telephone, intercom and digital data) on separate UHF carriers for coupling to the main SMDS distribution bus for distribution to remaining space base deck levels.

d. To combine VSB modulated UHF television carriers originating at deck level Camera Video Terminals with other UHF VSB modualted telecommunications signals originating at the deck level for coupling to the main SMDS bus for distribution to remaining space base deck levels.

e. To demodulate master "READ" and "WRITE" clock signals appearing on main SMDS distribution bus for operation of the deck level time division multiplexing telecommunications equipment (telephone, intercom, and digital).

3.1 Baseband Input Interfaces

The Base Level/Deck Level Interface Unit shall accept baseband signals from the following SMDS equipments:

a. Central Telephone Electronics- PAM (time division multiplexed) deck level telephone audio dialing and supervisory signals.
b. Central Intercom Electronics- PAM (time division multiplexed) deck level intercom audio and supervisory signals.
c. Digital Stations- Bi-level digital data (time division multiplexed) signals.

These three baseband TDM information signals interface directly with corresponding SMDS Modulator Groups which constitute the "baseband" send Signal Processing section of the Base Level/Deck Level Interface Unit.

3.2 UHF Input Signal Interfaces

a. The Base Level/Deck Level Interface Unit shall accept a 300 to 500 MHz input signal spectrum of VSB modulated frequency division multiplexed television signals from the deck level Camera Video Terminals via the deck level signal distribution cable.
b. The Base Level/Deck Level Interface Unit shall accept a UHF VSB modulated Master Timing "READ" Signal in the 300 to 500MHz spectrum form the SMDS Main Bus "Send Line" UHF Bi-Directional Coupler Group.
c. The Base Level/Deck Level Interface Unit shall accept a 300 to 500 MHz input signal spectrum from the SMDS Main Bus "Receive Line" UHF Bi-Directional Coupler Group for recovery of telecommunications and "WRITE" clock VSB modulated UHF channels originating from all other space base deck levels and Pilot and Terminal Modems respectively.

3.3 Baseband Output Interfaces

The Base Level/Deck Level Interface Unit shall provide baseband signals to the following SMDS equipment.

a. Central Telephone Electronics- PAM (TDM) Space Base telephone audio, signaling and supervisory signals in addition to READ and WRITE master clock signals.
b. Central Intercom Electronics- PAM (TDM) Space Base intercom audio and supervisory signals in addition to READ and WRITE master clock signals.
c. Digital Stations- Bi-Level digital data (TDM) signals in addition to READ and WRITE master clock signals.

3.4 UHF Output Signal Interfaces

a. The Base Level/Deck Level Interface Unit shall provide a 300 to 500 MHz output signal spectrum of VSB amplitude modulated UHF telecommunications channels originating at the deck level for coupling to the Main Bus for distribution to remaining space base deck levels.
b. The Base Level/Deck Interface Unit shall provide a 300 to 500 MHz output signal spectrum of UHF VSB modulated carriers appearing on the Main Bus Receive Line (from Receive Line Coupler) to the deck level Video Monitor Terminals via the deck level UHF television monitor distribution cable.

3.5 UHF Output Level and Level Equalization

The Base Level/Deck Level Interface Unit shall have provisions for UHF signal output level adjustment (composite UHF output signal levels appearing at the UHF signal port described in 3.2 above) in 1 dB steps over the range of -5 dBm to -30 dBm. This 25 dB level adjustment is intended to provide for equalization of signal levels as signals are coupled onto the main bus at deck levels between main line amplifier locations. Signal amplitude adjustments at each Base Level/Deck Level interface unit are made in such a manner as to ensure that individual signal levels appearing at the input to the main line amplifiers are within ±1 dB of the main line amplifier optimized signal input level. It is recommended that level adjustment be accomplished by manual gain control of the output buffer amplifier using a passive interstage current controlled attenuator similar to that described in the SMDS Main Line Amplifier functional description given in section 4.2.1.4 of the Final Report.

3.6 Interface Characteristics

The Base Level/Deck Level Interface Unit shall have electrical interfaces corresponding to those defined for the individual subunits comprising the unit. The conceptual Block Diagram shows the interfaces of these subunit building blocks.

3.7 Size, Weight and Power Consumption

The size, weight and power consumption of the Base Level/Deck Level Interface Unit shall be consistent with the recommended mechanical and maintainability guidelines recommended for the SMDS and within the packaging and interconnecting constraints imposed by the redundant integral subunits which comprise the SMDS unit.

3.8 Redundancy Requirements

The subunits which comprise the Base Level/Deck Level Interface Unit shall incorporate block redundant subunits in such a manner as to allow required switching of units and individual replacement of failed units on a noninterference basis with operating units. The size, weight, and power consumption requirements for the unit shall include packaging, weight, and power considerations for implementing the redundancy and associated fault/manual transfer implementation described in the SMDS Final Report Redundancy Implementation Recommendations.

3.9 Fault Monitoring

Suitable indicators shall be provided on the Base Level/Deck Level Interface Unit to indicate the operating mode and condition of subunits which comprise the unit.

3.10 Miscellaneous Design Guidelines

The Base Level/Deck Level development specifications must be considered flexible in terms of developing a totally integrated SMDS design. Trade-offs not considered or recognized as problems in this conceptual phase of the SMDS study may require deviations from the specifications stipulated above.

SMDS BI-DIRECTIONAL COUPLER

DEVELOPMENT SPECIFICATION

1.0 SCOPE

This specification describes the performance requirements of a SMDS functional building block identified as a UHF Bi-Directional Coupler.

2.0 APPLICABLE DOCUMENTS

The guidelines, trade-offs, and functional descriptions included as part of the SMDS Final Report shall be considered as part of this subunit specification.

3.0 ELECTRICAL PERFORMANCE REQUIREMENTS

The UHF Bi-Directional Coupler is a passive (reactive) signal coupling device that is used in the SMDS to couple and sample modulated UHF carriers on and off the SMDS wideband distribution cables. Their primary application is coupling signals on and off the Space Base main distribution bus at each deck level. In addition, the couplers are used at each deck level Video Terminal to couple television camera and monitor signals on and off the deck level UHF video signal distribution cables. Additional uses are found at the Rotary Joint Electronics for signal coupling and isolation application.

3.1 Frequency Range and Amplitude Response

The UHF Bi-Directional Coupler shall exhibit a flat amplitude response for both mainline and coupled arms within $\pm$0.5 dB over a minimum frequency range of 300 to 600 MHz.

3.2 Coupling Characteristics

The coupler shall be a four port device with two mainline ports and two coupled arm directional ports. The coupled arms shall exhibit a minimum directivity of 30 dB over the specified frequency range for main line signals flowing in opposite directions through the main line connections. The coupling between main line and coupled arms shall be 6 dB $\pm$0.5 dB. Main Line insertion loss shall not exceed 0.6 dB.

3.3 Impedance Characteristics

The coupler port impedances shall be 50 ohms with a maximum VSWR of 1.3 to 1.

3.4 Power Handling Capabilities

The unit shall be capable of processing signal levels of 1 watt maximum without damage.

3.5 Size and Weight Characteristics

The coupler shall be of subminiature design with maximum dimensions of 2" x 1/2" and a maximum weight of 2 ounces.

3.6 Miscellaneous Design Guidelines

Bi-Directional couplers with the above characteristics are currently available and, therefore, development effort for this item is considered to be minimal.

SMDS UHF SIGNAL POWER DIVIDER/COMBINER

DEVELOPMENT SPECIFICATION

1.0 SCOPE

This specification describes the performance requirements of SMDS functional building blocks identified as UHF Signal Power Divider/Combiners.

2.0 APPLICABLE DOCUMENTS

The guidelines, trade-offs and functional descriptions included as part of the Final Report shall be considered as part of this subunit specification.

3.0 ELECTRICAL PERFORMANCE REQUIREMENTS

The UHF Signal Power Divider/Combiner is a passive (reactive) signal splitting and summing device that is used in the SMDS to combine (sum) or split (divide) the wideband UHF signals appearing throughout the telecommunications system for simultaneous or independent signal processing depending on the direction of signal flow through the single "common" port of the device. As a divider, it produces duplicate but attenuated replica of a single UHF input signal spectrum at each of its output ports. (In the case of the SMDS, the number of input/output ports are two or eight.) As a combiner, the device produces a composite but attenuated replica of signals applied at each of its independent input ports at the common signal output port. The unit is used in the Base Level/Deck Level Interface Unit (8-way divider/combiner), SMDS Main Line Amplifier, Pilot Terminal Modem and at the SMDS Rotary Joint Electronics.

3.1 Frequency Range and Amplitude Response

The UHF Signal Power Divider/Combiner shall exhibit a flat amplitude reponse at output ports (port) within ±0.2 dB over a minimum frequency range of 300 to 600 MHz.

3.2 Insertion Loss

The Divider/Combiner units shall exhibit a maximum internal dissipative insertion loss above theoretical power division loss of 0.5 dB for two way divider/combiner units and 1.5 dB for eight way units.

3.3 Port-to-Port Isolation

The output (input) port-to-port isolation shall be 30 dB minimum across the specified frequency range.

3.4 Input/Output Impedance Characteristics

The Divider/Combiner shall exhibit a 50 ohm terminating impedance at each device port with a maximum VSWR of 1.3 to 1 over the specified frequency range.

3.5 Power Handling Capability

The device shall process composite signal levels to 1 watt without damage.

3.6 Size and Weight Characteristics

The units shall be designed for minimum size and weight and shall not exceed the following limits:

2-Way (with connectors)

Size: 1.0 x 1.5 x 0.75 inches Weight: 2 ounces

8-Way (Printed Circuit)

Size: 2.0 x 2.5 x 0.75 inches Weight: 4 ounces

3.7 Miscellaneous Design Guidelines

Reactive subminiature power divider/combiners with the above characteristics are currently available and, therefore, development effort for these units is considered minimal.

SECTION 7.0

SMDS MAIN LINE AMPLIFIER

7.0 SMDS MAIN LINE AMPLIFIER

7.1 ACCOMPLISHMENTS

This study has resulted in a recommended configuration for a SMDS Main Line Amplifier which will meet the overall main line amplification requirements needed to achieve desired SMDS performance. The functional description of this unit is provided in Volume I, section 4.2.1.4, of this report.

The distribution and control of wideband telecommunications signals throughout Space Base required the investigation of many different system implementation techniques. Any particular implementation scheme studied had certain advantages over the other, but almost always in a different respect depending upon which parameter or system characteristic was under consideration. The use of multiple transmission lines for instance, to independently process the various Space Base telecommunications signals, was the subject of a comprehensive trade study (details of which have been summarized in section 4.0). This approach demonstrated that actual hardware implementation to achieve desired performance was simpler if time division multiplex (TDM) signals were processed separately from frequency division multiplex (FDM) signals. This approach also provided a degree of redundancy that obviously is not an inherent feature of a common or single distribution bus approach, which was ultimately selected for implementing the recommended Baseline System.

It was recognized early in the study, and subsequently concluded, that Space Base video distribution requirements (a specified minimum of 20 video channels requiring a minimum of 6 MHz bandwidth) would have a major impact on the evolution of a final system design. If an optimal system configuration was to even be approached within some of the overall SMDS major design constraints (size, weight, complexity, and minimum power requirements along with maximum system reliability, component commonality, and performance) it became apparent that the SMDS video distribution requirements must necessarily influence final system design.

A major design consideration, that required resolution, was making the selected TDM audio and digital signal distribution techniques compatible with FDM video distribution so as not to require separate types of equipments for each type of signal. In other words, the

selected approach was to achieve maximum equipment commonality and compatibility in order to minimize unique pieces of hardware. System reliability was postulated on incorporating block redundancy of these common building blocks and system availability was enhanced by minimizing the number of unique spare modules needed for system maintenance.

The problems of wideband signal distribution through cable systems carrying video signals have become more and more a concern of the CATV industry, which is constantly being faced with increased performance demands. These problems are similar to those encountered in the SMDS wideband cable distribution system, due to the large number of wideband modulated UHF carriers that must be distributed throughout the Space Base. The TDM/FDM compatibility problems, unique to the SMDS system, do not significantly affect the design of the SMDS Main Line Amplifiers, since these compatibility interfaces occur at the SMDS Modulator/Demodulator Group interfaces and are discussed in section 4.2.5.2 and 4.2.5.3, respectively. It follows, that the problems of signal distribution throughout Space Base can be considered essentially independent of the type of modulation appearing on the individual frequency division multiplexed UHF carriers.

The study has selected active signal amplification in the main distribution line over passive distribution. Primarily, this is from the standpoint of maintaining the relatively high signal-to-noise requirements (>40 dB) imposed on the system by the television equipments. Adequate design margins were not possible when a strictly passive system was studied for the "Y" Space Base concept nor was the desirability of system configuration flexibility considered adequate for a passive distribution system.

The entire problem of signal distribution in any system from one point to another is signal attenuation or loss. In a wired system such as the SMDS, it is not possible to overcome all system losses by using a single high-gain amplifier; especially, due to the distributed nature of the SMDS which has signals both originating and terminating at many locations simultaneously. It becomes necessary to use the concept of repeater amplifiers to overcome signal losses as the signals are routed over various paths throughout Space Base. As pointed out earlier in section 4.2.1.1, the cascading of these amplifiers results in signal degradation due to noise and signal distortions generated internally by each individual amplifier.

7.2 PROBLEMS

The SMDS Main Line Amplifier is categorized as a major module building block of the Space Base Telecommunications System. The major implementation problems to be considered in the design of the Main Line Amplifier are primarily those itemized below:

a. Main Distribution Line Design Considerations

b. Gain and Slope Control Considerations

c. Redundancy Implementation

d. Size Weight and Power Considerations

These problems and the designers approach to the resolution of these problems are addressed separately in sections 7.3.1 through 7.3.4, respectively.

7.3 RESOLUTIONS

7.3.1 Main Distribution Line Design Considerations

The function of the SMDS Main Distribution Line is to assure that information signals originating at one Space Base deck level arrives at all other deck levels with sufficient amplitude and minimum signal degradation to provide high-quality telecommunications capability, both to and from any point within Space Base. The wideband nature of the telecommunications signals, to be routed around Space Base, imposes stringent performance on the main bus distribution lines and amplifiers. Implementation trades have shown that coaxial cables of a subminiature variety (see Transmission Media discussion, section 2.5) offer the most advantages for Space Base application. The primary consideration in choosing the subminiature cable was that active amplification in the main line bus could be used to boost main line signal levels at selected locations within the Space Base. As a result, the additional attenuation of subminiature cables compared to larger and bulkier low-loss cables can be overcome with these line amplifiers. Main line amplification provides a means of reducing the signal level variations that would appear on the main bus if periodic gain compensation was not employed. It is possible to design and build demodulation units which will operate with automatic gain control circuits that can operate over ranges in excess of 60 dB. However, it is intended that the signal levels on the main bus not be required to approach this level variation, since deck level UHF distribution

losses result in the need for even more demodulator dynamic range. These dynamic ranges even become larger unless some means of equalizing carrier-to-carrier level variations such that all carriers appear at a demodulator at approximately the same level regardless of where they originated.

Although signal level variations of 20 to 30 dB can be tolerated on the main bus, individual signal-to-signal level variations of 10 dB maximum have been determined to be a realistic design goal. Analysis of a total passive main line distribution system has shown that this signal level variation, even assuming the use of a very low-loss transmission cable (0.50-inch diameter or more) is not feasible. Signal levels on the bus, to provide a main line signal-to-noise ratio of 50 dB, requires levels on the order of 100 milliwatts (+20 dBm) at a modulator output compared to less than 1 milliwatt if active main bus amplification is utilized. The additional complexity and performance requirements placed on the wideband ultra-linear UHF amplifiers required to process these higher levels, is outweighed by the advantages of using lower levels and main line amplification from a hardware development point of view and from EMI considerations.

System design objectives must be directed toward meeting the minimum allowable signal-to-noise ratios and holding intermodulation and cross-modulation distortion levels below maximum tolerable levels.

Extensive subjective testing, conducted within the television industry, has shown that what might be described as studio quality video transmission can be achieved if the main distribution bus and deck level interface units can deliver signals to the demodulators with the following ratios:

Signal-To-Noise Ratio (4.5 MHz)	50 dB	(40 dB Min)
Cross-Modulation Ratio	60 dB	
Intermodulation Ratio	60 dB	
Hum-Modulation Ratio	60 dB	

While somewhat flexible, the above design objectives are based on the results of a long series of complex subjective tests conducted in the past several years by the commercial television industry and conform to present system design objectives established for current community cable television distribution systems. The two major considerations affecting the

above established performance criteria are: (1) thermal noise levels present in the system and (2) amplifier output overload levels which determines the intermodulation or output distortion introduced into the system by the cascaded main line amplifiers.

7.3.1.1 System Thermal Noise Effects

Thermal noise imposed on a video signal appears as "snow" in the background of the video monitor picture presentation. The problem in the system design is to keep the thermal noise sufficiently lower than the desired video signal level so that the picture presentation meets studio-quality performance. The principle source of thermal noise in a closed circuit system above theoretical levels, is from the active line amplifiers that are operated in series with the main transmission line. These repeater or line amplifiers contribute noise to the signal passing through it by an amount equal to the amplifier noise figure, which is generally expressed in decibels. The output noise power of an amplifier is the sum of the amplifier gain (GdB), noise figure (FdB), and available input noise power [(kTB)dBm].

$No = G + F + kTB$

where:

No = Amplifier noise output power in dBm

G = Amplifier gain in dB

F = Amplifier noise figure in dB

$(kTB)dBm = 10 \log k + 10 \log T + 10 \log B$

k = Boltzmann's Constant

$= 1.38 \times 10^{-23}$ joules/°K

= 198.6 dBm/°K/Hz

T = Absolute Temperature

$= 273°K + 50°C = 323°K$

B = Video Bandwidth

= 6.0 MHz

kTB = -198.6 dBm + 25.1 dB + 67.7 dB

kTB = 105.8 dBm

The noise output of a single amplifier is then (assuming a nominal amplifier gain of 15 dB and a noise figure of 10 dB)

$$N = 15\ dB + 10\ dB - 105\ dBm = -80\ dBm$$

The signal level at the output of the amplifier must then exceed the thermal noise level by 50 dB for a 50 dB signal-to-noise ratio, or have a signal output level of -30 dBm.

Since the distribution system consists of more than just one amplifier in the signal path there is a build up of noise power at amplifier outputs. In the example above for a single amplifier (with a given noise output power), a series of these amplifiers will contribute an equal amount of noise to the system assuming all amplifiers are operating with the same gain and have the same noise figure. This results in a cascaded amplifier noise level degradation factor K which can be shown to be equal to:

$K = 10 \log n$ where K is the increase in noise level at the output of n amplifiers expressed in dB.

Thus, for a series of cascaded amplifiers, it is necessary to take into account the increase of system thermal noise by the factor K. For the case of 10 amplifiers in cascade compared to only one single amplifier, it is necessary to increase the minimum amplifier output signal level from -30 dBm to [-30 dBm + 10 log 10] or a -20 dBm signal level to maintain the desired 50 dB signal-to-noise ratio.

7.3.1.2 System Amplifier Overload Effects

It would seem at first, that the above described noise degradation due to cascading amplifiers could be overcome merely by increasing the bus signal level to maintain the signal 50 dB above the noise, regardless of whether one or more amplifiers are connected in cascade. The absolute main bus signal maximum output becomes a limitation however, in that present state-of-the-art (and that in the near future) does not provide the high power output, ultra-linear amplifiers needed for main line amplification. There is presently considerable development activity in this area by the semiconductor industry. Currently, the industry is producing thin film ultra-linear amplifiers with moderate output power of the type needed for Space Base applications. Although the 300 to 500 MHz range has not been made available at this time,

similar amplifiers covering this frequency band are now under development; but still, their output powers will be limited to something on the order of a few milliwatts. The performance parameter limiting signal output power is amplifier linearity. Whereas high-level distribution could be advocated, the distribution system intermodulation and cross-modulation requirements more than likely could not be met at the milliwatt power levels especially when as many as 30 wideband multiple carriers are anticipated. An important consideration in establishing a main bus signal level, is to set the maximum distribution bus level below that level which produces undesirable intermodulation and cross-modulation distributions in the bandpass of any of the multiple signal carriers.

The presence of extraneous single frequency and/or cross-modulation effects can produce a very noticeable pattern on a Television screen. These extraneous single frequencies are produced as beat products between the various carriers present on the system transmission bus or by a cross-modulation effect, where the modulation on one carrier is imposed on the modulation of another. Where beat products fall outside the transmission spectrum or in ground bands there is no problem with these interferences. However, when they appear inband, amplifier linearity must be such that their level is far enough below the desired signals as to make their presence indistinguishable.

Various studies have been performed which show that the amount of interference that can be tolerated in the received video channel varies widely as a function of the portion of the band in which it appears. Primarily the most sensitive portions of the video spectrum are near the carrier, about 1 MHz away from the carrier and at 3.58 MHz which is the color subcarrier frequency in the NTSC system. Although it has been possible in the past to minimize the effects of these interference signals through judicious carrier frequency selection (six video channels or less), this approach is totally unfeasible in a system requiring 30 channels or more. The overall system performance must be obtained by using amplifiers which display the necessity linearity without regard to special frequency assignments. In the case of the SMDS frequency assignments however, second order intermodulation effects have been avoided by choosing a single frequency band where all operating carriers are within a one octave band (2:1 frequency range) of 300 to 600 MHz. As a result, the linearity of the wideband amplifiers must be actually concerned with third order effects namely intermodulation and cross-modulation.

As indicated earlier, it was stated that wideband amplifiers have been produced which exhibit the required intermodulation and cross-modulation performance as required for this Space Base application.

Just as for the case of noise build-up in cascaded amplifiers and the need to increase main bus signal levels to overcome this noise, it is necessary to derate the single amplifier nonlinear distortion performance characteristics for a cascade of these amplifiers. If a single amplifier has intermodulation products down 80 dB from the desired signal output level for a given output level, then a cascade of 10 of these amplifiers will have cross-modulation products at only 60 dB below the desired output signal due to the fact that for a quantity of N amplifiers in cascade, the cross-modulation ratio will increase by direct addition on a voltage basis of cross-modulation products:

$$\text{Cross-modulation (N Amplifiers)} = \text{Cross-modulation (Single Amplifier)} + 20 \log N$$

However, it is possible to maintain distortion products at the level of a single amplifier for a series of cascaded amplifiers by reducing the amplifiers output levels in a ratio of 1 dB level reduction to 2 dB reduction in cross-modulation. Stated in another way, for a well behaved amplifier, cross-modulation products decrease 2 dB for every 1 dB decrease in output level. Therefore, by operating a wideband amplifier which will provide output signal levels of -20 dBm and intermodulations 80 dB down, a 0 dBm output level would result in distortion products at -60 dBm.

It can be seen from the above discussion that cascading and signal level of wideband amplifiers play an important role in specifying wideband amplifier performance, and correspondingly in choosing main bus signal levels.

7.3.1.3 Selection Of Optimum Main Bus Levels

The cumulative effects of thermal noise build-up and output power level reduction required to maintain a high quality transmission in a series of cascaded amplifiers is depicted in figure 7.3.1.3. The lower figure curves show the increase of amplifier noise input levels versus number of cascaded amplifiers (assume identical amplifiers with 10 dB noise figure gain = 15 dB).

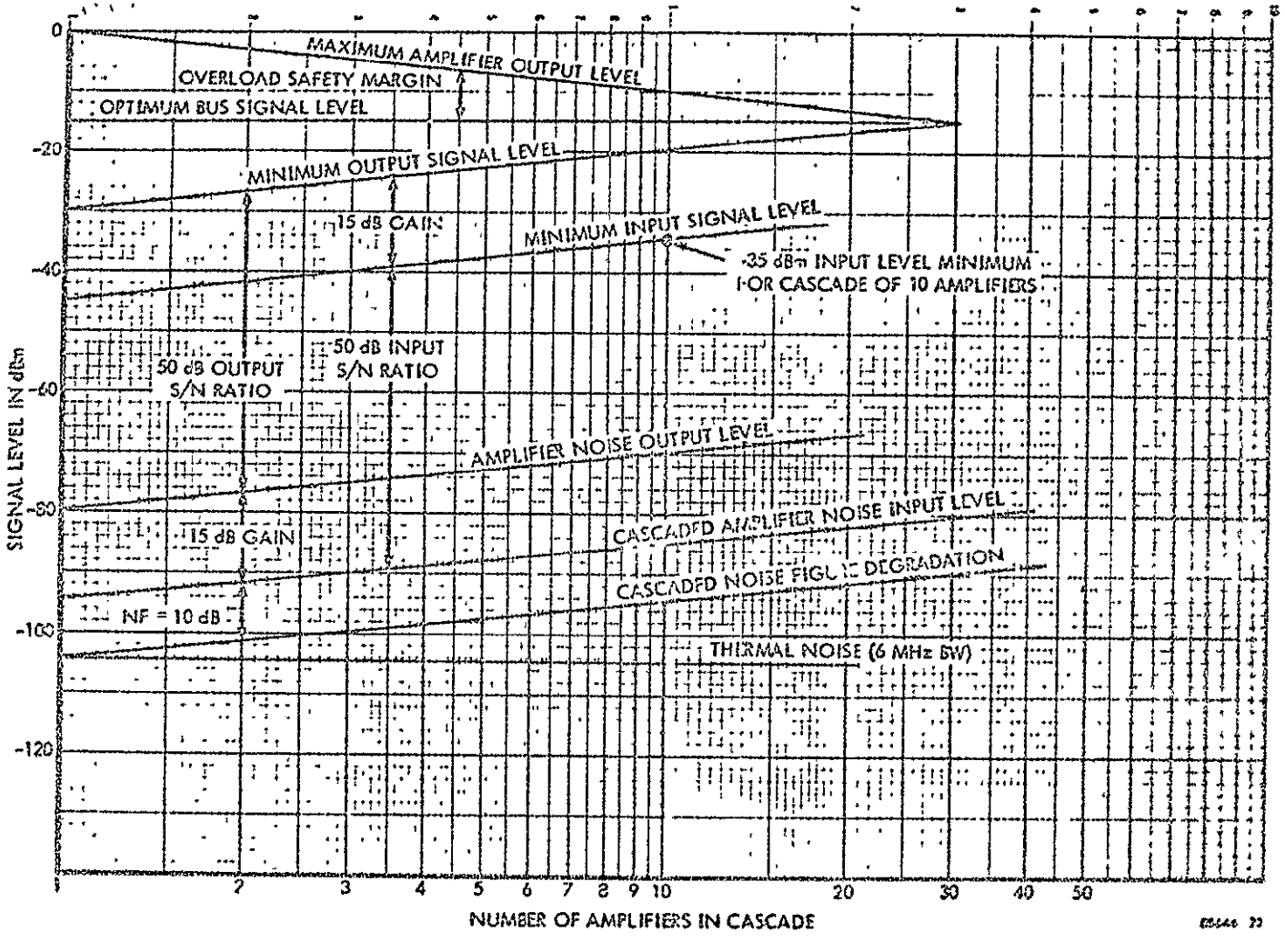


Figure 7.3.1.3. SMDS Main Distribution Bus Derating Diagram

The required 50 dB main bus signal-to-noise ratio is plotted above the cascaded amplifier noise output level. This plotted line represents the minimum amplifier output signal level that can support the main telecommunications bus requirements. Shown above this line is the cascaded output level degradation curve which assumes a 0 dBm single amplifier output level with distortion products down 60 dB. By not allowing output levels to exceed this indicated uppermost maximum output level boundary, distortion products can be maintained 60 dB below output signals and therefore, meet system design objectives.

The optimum system level is not necessarily set at equal safety margins from the maximum signal overload point and the minimum signal-to-noise ratio objective. Experience has shown that overload is much more critical than noise in establishing system performance. The overload margin from what could be termed excellent video transmission to totally unsatisfactory is on the order of 5 to 8 dB. This corresponds to a noise (signal-to-noise) degradation of 15 dB, assuming that the maximum number of amplifiers to be cascaded in the system would be on the order of 10 for most of the proposed Space Base configurations. As seen from figure 7.3.1.3, a main bus level of -15 dBm would provide an equal overload/noise margin of 2.5 dB. By moving this main bus level down to -20 dBm, it provides less noise margin in favor of a greater overload margin and could represent a more realistic main bus level. The final optimum bus signal level will be a factor which must be ultimately determined during the final prototype system implementation but for present purposes, a level of -15 dBm on the main bus will be assumed. This correlates to a total composite multicarrier power level of approximately 0 dBm:

[-15 dBm + (30 x 0.032 mW) = 1 mW or 0 dBm].

7.3.2 Gain and Slope Control Considerations

The method of gain and slope control implemented in a main line amplifier design will necessarily be the result of several compromises. As discussed in the previous section, noise and distortion are the primary factors in setting the performance capabilities of a particular amplifier. The method of gain and slope control implementation have considerable impact on the noise and distortion produced by an amplifier.

It can be shown by analysis, that the optimum gain for an individual amplifier to overcome the maximum cable loss and achieve the longest distribution system using these amplifiers in cascade would require an amplifier with a gain of 8.69 dB. Since the intent in

the SMDS is not to achieve the longest cascaded system using ultra low-loss cable but to optimize other system parameters (such as size, weight, power consumption commonality, and reliability), it is necessary to choose amplifier gains which allow for wider spacing of amplifiers; thus, resulting in a reduction in the number of amplifiers required.

Wideband solid amplifiers with gains in excess of 40 dB over octave bandwidths impose design problems that do not have feasible solutions. This leaves realizable gain in the range of approximately 10 to 30 dB. Modeling of the "Y" Space Base concept, has shown that there are requirements for gains nominally in the 15 to 25 dB range. This necessarily calls for an amplifier consisting of more than one stage and, in fact, for a thin-film integrated circuit configuration, a 30 dB amplifier with a push-pull output configuration uses four stages.

If gain control of an amplifier were achieved through the use of fixed attenuation pads placed on the input or output of a flat fixed gain amplifier, two distinct affects would be noted. A pad on the input would degrade the amplifier noise figure by an amount equal to the pad loss. Placing the same pad on the amplifier output does not affect the overall amplifier noise figure; however, the amplifier overload level is decreased. Both affects result in decreased amplifier dynamic range and has resulted in designs that use interstage gain control and slope equalization. In this manner it is possible to realize a low noise, low distortion amplifier which can meet system requirements.

The proposed implementation of the gain control and slope control using passive voltage controlled "bridged tee" networks, results in gain and slope controls which introduce negligible intermodulation or cross-modulation distortion. The variable elements in these networks are currently available PIN diodes, that have the characteristics of an almost perfect variable resistor with achievable attenuation ranges of 30 dB.

Refer to sections 4.2.1.1 and 4.2.1.3 of the Baseline system description and the discussion on active microwave filters under the SMDS Group Demodulator preselect filter discussion in section 4.2.5.3 for additional information on gain and slope equalization.

7.3.3 Redundancy Implementation

The requirement for operating mainline amplifiers with automatic switching of a block redundant standby unit (in case of on-line amplifier failure), to meet system reliability

requirements, imposes further constraints on the amplifier design. The conceptual design has proposed that these block redundant amplifiers be fed in parallel via a two-way power divider. The output of the good amplifier would then be connected to the main bus by means of a solid-state SPDT diode switch, or by means of a two way power combiner. In either case further study must be made to determine the best approach. In case of failure, a switch operating under the control of a pilot signal level detector would connect the standby amplifier to the main bus and simultaneously apply power to that unit and remove power from the failed unit. In the case of the two amplifiers operating into a power combiner, that fault detector would apply power to the standby unit and remove power from the failed unit. The on-line unit would then compensate for additional losses caused by combiner mismatching due to the failed unit with its automatic gain control circuits. The approach, it is believed, would cause impedance mismatching problems with associated main line signal reflections that cannot be easily compensated due to the impedance changes which occur at an amplifier output port in the powered and unpowered states. For the same reasons and the additional consideration of noise figure degradation, the use of the power divider on the amplifier input port could be a design risk. The present availability of solid-state diode switches with a possible 60 dB of isolation would make switching of both input and output the perfect approach with the only disadvantage of the somewhat lower reliability of the switching devices themselves. Nevertheless, further study in this area is warranted during the hardware development phase of the SMDS before a definite approach is selected.

7.3.4 Size, Weight, and Power Considerations

Present technology has demonstrated the feasibility of size and weight reduction that is possible for wideband amplifiers meeting the overall requirements for the SMDS. The problem remaining which restricts further reduction in the size and weight of a main line amplifier assembly is the periferial components, especially the AGC and slope equalizers and associated pilot channel bandpass filters. The rapid advancement of microstrip technology however, will play an important role in both of these areas. The AGC and slope equalizers, along with the potential use of recently developed active microwave filters as pilot filters, can result in a very compact mechanical design and could be undertaken at the present time. Therefore, size and weight are not considered to be a problem requiring any special development efforts.

Power consumption in ultra-linear wideband amplifiers is a problem that must be carefully considered. The currently available thin-film amplifier, which has been referred to several times during this report, has an extremely low efficiency. The manufacturer has quoted input power dissipation of nearly 5 watts per 15 dB gain block. Although the present thin film design has the necessary host sink provisions to internally dissipate this power, the problem must be given additional study to make overall system power consumption reasonable. The literature has described several approaches to solving the problem of achieving ultra-linear amplification at low-power levels but has not as yet been conclusive.

7.4 MATHEMATICAL ANALYSIS OF DESIGN

Mathematical analyses of the main line amplifier are contained in the resolution section of the SMDS Main Line Amplifier Description (section 7.3.1). These analyses consist of:

a. System Thermal Noise Analysis (see section 7.3.1.1)

b. Optimization of Amplifier Gain and Placement (see section 7.3.1.3)

7.5 THEORETICAL PERFORMANCE OF DESIGN

The theoretical performance of the SMDS mainline amplifier is described in section 7.3.1. The desired transmission characteristics are summarized as follows:

Signal-to-Noise Ratio (4.5 MHz)	50 dB (40 dB Min)
Cross-Modulation Ratio	60 dB
Intermodulation Ratio	60 dB
Hum-Modulation Ratio	60 dB

7.6 EXPERIMENTAL PERFORMANCE OF DESIGN

No actual experiments were performed as part of this study. However, much of the experimental work performed by the television industry is referenced throughout the study.

7.7 TRADE OFFS

Several trade offs were performed as part of the mainline amplifier design and are described in the noted sections, volume I of this report.

a. Section 2.3, Video Implementation

b. Section 4.1.3, Active Versus Passive Distribution Systems

c. Section 4.1.4, Cable Routing Trades for SMDS

d. Section 4.1.6, Carrier Frequency Selection for SMDS

e. Section 4.2.1, U.H.F. Distribution Subsystem

One area requiring further study is the extension of bandwidth to allow DSB modulation of the various information channels. This extension of bandwidth would impose a greater demand on the SMDS main line amplifier design. A further description of this study task is given in section 5.2.3.1.

7.8 SUMMARY

The characteristics of the SMDS main line amplifier have been studied in considerable detail. A discussion of the amplifier implementation has summarized what is considered to be the primary considerations to be made in configuring an automatic gain and slope equalizing main distribution amplifier. The recommended amplifier meets the study objective of defining an amplifier configuration that can be adapted for use in almost any SMDS configuration. It is felt that the only major development problem centers around the reduction of power consumption of thin-film integrated amplifiers, since development to date would show that all other necessary performance parameters can be achieved using presently available techniques.

SUMMARY NOTES

1. The SMDS wideband amplifier is a component of the SMDS main line amplifier. Therefore it is not discussed separately since its design has been predicated primarily upon main line amplifier requirements. See the Wideband UHF Amplifier Subunit Specification and section 4.2.5.1.2 for functional description.

2. Discussion of the Base Level/Deck Level Interface Unit consists of SMDS subunit building blocks and is not discussed as a separate unit. See discussions and specifications of SMDS Demodulator Group. See Development specification on SMDS Power Combiner and Base Level/Deck Level Interface Unit functional description in section 4.2.3 of volume I.

3. Discussion of the SMDS Video Terminals consists of SMDS Modulator Groups and SMDS Demodulator Groups. See discussions on these units and the development specification on the SMDS Video Terminals. See section 4.2.4 for functional description.

7.9 SCHEMATICS AND DRAWINGS DEVELOPED

The drawings relating to the main line amplifier implementation appear in section 4.2.1.4, Main Line Amplifier Description, of this report.

7.10 DEVELOPMENT SPECIFICATIONS

The following development specifications are provided as a part of this section:

1. SMDS Mainline Amplifier Module
2. SMDS UHF Amplifier Subunit

SMDS MAIN LINE AMPLIFIFP

MODULE

DEVELOPMENT SPECIFICATION

1.0 SCOPE

This specification describes the development design goals and major performance specifications of a SMDS major module building block identified as a SMDS Main Line Amplifier.

2.0 APPLICABLE DOCUMENTS

a. The guidelines, trade-offs, and functional descriptions included as part of the SMDS Final Report shall be considered as part of this module specification. References cited in the Final Report shall be used for developmental guidance.

b. SMDS Wideband UHF Amplifier Specification

c. SMDS UHF Bi-Directional Coupler Specification

d. SMDS UHF Power Divider/Combiner Specification

3.0 ELECTRICAL PERFORMANCE REQUIREMENTS

The SMDS Main Line Amplifier shall provide low noise/distortion amplification and level equalization of up to 30 separate vestigial sideband, amplitude modulated, UHF telecommunications carriers appearing on the Space-Base main telecommunications bus. The main line amplification and level equalization (across the 300 to 500 MHz frequency spectrum) is provided to overcome main bus coaxial cable attenuation and the insertion/coupling losses of deck level directional couplers.

3.1 Operating Frequency Range

The Main Line Amplifier shall accept UHF carriers in the frequency range of 300 to 500 MHz.

3.2 Operating Gain and Slope Equalization

The Main Line Amplifier Gain at 500 MHz shall be adjustable from 12 to 25 dB. The amplifier gain at 300 MHz shall be adjustable over a range of ±10 dB of the 500 MHz 15 dB gain setting by means of an appropriate interstage cable equalization (tilt) control.

3.3 Gain and Slope Equalization Accuracy

The Main Line Amplifier gain and slope equalizations shall be maintained within ±1.0 dB of a flat response across the 300 to 500 MHz operating bandwidth when measured at the amplifier signal output port. This shall occur when the amplifier has been properly adjusted for the specific main bus coaxial cable attenuation versus frequency (slope) characteristic and flat insertion losses of coupling devices between the output of the preceding main line amplifier and

the input of the specific amplifier under test. An equal amplitude swept test signal from 300 to 500 MHz inserted at the output of the preceding main line amplifier (main bus cable input) at the normal amplifier output level shall produce the specified responce gain flatness over all operating modes (i.e. redundant standby amplifier in operate mode) and environmental operating conditions.

3.4 Automatic Gain Control

Automatic gain control of the main line amplifier shall be provided to compensate for input signal level changes of ±5 dB. The automatic gain control shall operate on the composite signal level of the highest frequency UHF Master Timing Channel appearing at the top UHF spectrum band edge (480 to 500 MHz). Output levels shall not change more than ±1.0 dB for input level changes over this range.

3.5 Automatic Slope Equalization

Automatic slope equalization of the main line amplifier transfer characteristic shall be provided to compensate for input signal level changes of ±5 dB. The automatic slope control shall operate on the composite signal level of a Master Timing Channel appearing near the middle or lower edge of the UHF (300 to 500 MHz) spectrum. Slope equalization shall be maintained within ±1.0 dB for input signal changes over the specified range.

3.6 Noise Figure

The noise figure of a redundant Main Line Amplifier configuration shall not exceed 10 dB over the operating frequency of 300 to 500 MHz and all specified operating conditions.

3.7 Multichannel Overload Level

The intermodulation and crossmodulation distortion products produced under all specified operating conditions shall not exceed a level of -80 dB below a multichannel (thirty, 6 MHz channels) overload level of 0 dBm. Crossmodulation levels shall be the amount of modulation appearing on any single unmodulated UHF carrier as a result of simultaneous 90% modulation of all other SMDS UHF carriers.

3.8 Input/Output Impedance Characteristics

The Main Line Amplifier shall have input and output impedancy of 50 ohms with a corresponding VSWR which shall not exceed 1.5 to 1.

3.9 Redundancy Provisions

The Main Line Amplifier shall be implemented with automatic block redundant switching of a parallel standby amplifier unit by means of appropriate threshold detection of a present AGC master timing (pilot) minimum allowable signal level.

3.10 Fault Detection Provisions

In addition to the automatic redundant amplifier transfer requirements specified in section 3.9 above, appropriate indicator signals shall be provided to indicate redundant unit operational status (i.e., abnormal operation or unit failure) and the occurance of automatic transfer shall be provided.

3.11 Power Supply Requirements

The Main Line Amplifier shall accept maximum of two dual polarity DC input voltages with a maximum level of 30 volts. Total input power shall not exceed 12 watts with a design goal of 8 watts. Primary DC power supply overloads due to internal unit faults shall be prevented by use of appropriate overload and surge protective devices or cirultry.

3.12 Size and Weight Requirements

The Main Line Amplifier shall have a maximum weight of 3 pounds with a design goal of 2 pounds. Unit volume shall not exceed 36 cubic inches with a design goal of 24 cubic inches. Unit form factor shall be made compatible with overall system maintainability and packaging constraints to be specified.

3.13 Miscellaneous Design Guidelines

Modulator Group development specifications must be considered flexible in terms of developing a totally integrated SMDS design. Tradeoffs not considered or recognized as problems in this study shall be made as required as a part of the SMDS hardware development phase.

SMDS UHF AMPLIFIER SUBUNIT

DEVELOPMENT SPECIFICATION

1.0 SCOPE

This specification describes the development design goals and major performance specifications of a SMDS functional building block identified as a UHF Wideband Amplifier.

2.0 APPLICABLE DOCUMENTS

The guidelines, trade-offs, and functional descriptions included as part of the SMDS Final Report shall be considered as part of this subunit specification. References cited in the Final Report shall be used for developmental guidance.

3.0 ELECTRICAL PERFORMANCE REQUIREMENTS

The UHF Wideband Amplifier shall be utilized as an universal UHF gain element throughout the SMDS. Its design shall be compatible with the requirements of wideband, low distortion amplification for applications in the SMDS Main Line Amplifier Group in addition to uses as a buffer amplifier/preamplifier for the processing of UHF signals in the Base Level/Deck Level Interface Unit, Pilot and Terminal Modem, and Rotary Joint Electronics.

3.1 Amplifier Operating Frequency Range

The UHF Wideband Amplifier shall have a minimum 1 dB bandwidth of 250 MHz extending from 275 MHz to 525 MHz with a maximum in-band ripple of $\pm$0.5 dB.

3.2 Gain and Noise Figure Characteristics

The amplifier shall consist of two gain blocks, both mounted on a single thin film substrate, the intent being the development of a universal amplifier device suitable for applications described in 3.0 above. The first gain block (low noise) shall have an absolute gain of 15 dB $\pm$1 dB with a noise figure of 6 dB maximum. The second gain block (high power output) shall have a gain of 15 dB $\pm$1 dB with a noise figure of 10 dB maximum. The input and output ports of each gain block shall be individually accessible externally to the amplifier package.

3.3 Power Output Capability

The individual gain blocks shall meet specified intermodulation and crossmodulation performance requirements when processing 30 VSB amplitude modulated carriers when individual carrier output levels are as specified below:

Low Noise Gain Block	-15 dBm
High Power Gain Block	0 dBm

3.4 Intermodulation and Crossmodulation Distortion Products

Each gain block shall not produce intermodulation or

crossmodulation distortions greater than 80 db below desired signal levels when operating at specified maximum output signal levels for a total of thirty 6 MHz spaced channels. Standard measurement techniques using synchronous (simultaneous) modulation of all channels shall be used for crossmodulation measurements.

3.5 Reverse Isolation

Each Amplifier Gain Block shall exhibit a minimum of 30 dB reverse isolation.

3.6 Input/Output Impedance Characteristics

The UHF Amplifier gain blocks shall have input and output impedances of 50 ohms with a maximum VSWR of 1.5 to 1. The amplifier shall be unconditionally stable for all termination impedances from open to short at any phase angle. It shall be possible to connect and operate each gain block separately or in cascade with passive gain and slope equalization networks between gain blocks. Direct connection of the Low Noise block output to the high power block input shall result in an amplifier with an overall gain of 30 dB minimum and -3 dBm maximum output power with distortions 80 dB below desired signal output levels.

3.7 Power Consumption

The power consumption of each stage shall not exceed 2 watts for 30 volts maximum input voltage.

3.8 Size

The amplifier shall be of thin film construction with suitable thermal heat sinking provided. The device shall be packaged in a standard TO-3 package or equivalent maximum volume.

3.9 Miscellaneous Design Guidelines

If additional study of the SMDS should reveal that two or more separate thin film amplifiers are more desirable than a single universal unit, this flexibility should be considered in determining the final SMDS Wideband UHF Amplifier configuration(s) to meet all system applications.

SECTION 8.0

SMDS MODULATOR GROUP

8.0 SMDS MODULATOR GROUP

8.1 ACCOMPLISHMENTS

This study has resulted in a recommended configuration for a SMDS Modulator Group which will meet the overall modulation requirements needed to achieve desired SMDS performance. This unit was functionally described in section 4.2.5.2.

It was recognized early in the study that one of the functional requirements of hardware to be developed for the SMDS was a group of hardware that would permit the multiplexing of wideband (4.5 MHz) video channels onto a common transmission medium to be distributed throughout the Space Base, with the transmitted information originating at various deck level locations.

Trades conducted throughout the study have led to a baseline system configuration which uses a frequency division multiplex (FDM) technique to couple approximately 30 of these wideband modulated carriers to a unidirectional coaxial cable transmission bus loop. Due to the distributed nature of the SMDS, opposed to a system where frequency multiplexing (stacking) functions for all channels are performed at one location, it became apparent that some functional single-channel equipment was needed that could be operated independently of other frequency multiplexing equipment but still achieve the same function of conventional multiple-channel FDM equipment, which normally operates at a central location.

In conventional FDM equipment, multiple baseband information signals feed individual channel modulators physically grouped together at a single location whose outputs are combined and fed into a single transmission medium from the combiner output, whether the transmission medium be a coaxial cable or RF radio link. This again, is for the case where all baseband signals to be transmitted are routed from a single location where all input signals are present at the combined equipment location.

The purpose of the SMDS is to distribute wideband information signals (video and high-speed time division multiplexed telephone, intercom, and digital data) originating at any Space Base deck level to all other deck levels. The method selected for performing this function is to place the individual channel frequency multiplexing transmitters physically adjacent to the telecommunications signal sources at each deck level of the Space Base. These signal transmitters

are identified as SMDS Modulator Groups and are functionally described in section 4.2.5.2. These units translate wideband data onto modulated UHF carriers which are subsequently coupled onto the main transmission bus.

The primary goal of specifying the function and performance of the SMDS Modulator Group is to ensure compatibility of the modulator, especially the modulator wideband video input circuits, with both the composite analog video and the PAM audio and digital data pulse streams. This approach eliminates the use of separate units for each function and provides a degree of equipment commonality that if not implemented would considerably compromise the overall SMDS equipment design goals. This is not to say that there will ultimately be complete function interchangeability between video, PAM, or digital but that the required compatibility be achieved at least by a modulator function selector switch which is a part of a single SMDS module, designated a Modulator Group.

8.2 PROBLEMS

The compatibility problems are addressed in more detail in the resolution section (8.3) which describes solutions to the problems encountered in the design of a distributed multiplex system such as the SMDS. The Modulator Group is one of the fundamental building blocks of the SMDS.

Primarily the problems encountered by the Modulator Group designer are:

a. Input/Output Signal Processing Compatibility.

b. Vestigial Sideband Filter/Delay Equalizer Implementation.

c. Frequency Upconversion Techniques.

d. Spurious Output Signal Suppression.

e. Size and Weight Minimization.

f. Power Consumption Minimization.

g. Testing Techniques.

Detailed discussion of these recognized problems with potential resolutions are covered simultaneously in the following section.

8.3 RESOLUTIONS

8.3.1 Video and PAM Input/Output Signal Processing Compatibility

The use of a common functional signal processing equipment to modulate similar, yet in some ways dissimilar, input signals on a UHF carrier creates a dilemma for arriving at a collection of specifications for the Modulator Group. The primary problem is one of resolving the differences in input signal characteristics and specifying overall performance and test requirements to be compatible with all types of signals to be processed. Whereas, one particular performance parameter may be of little significance in television video performance, this same parameter may require stringent control for the transmission of audio or digital information in a satisfactory fashion. And finally, even if specifications are successfully determined, testing to these requirements may be unfeasible, time consuming, and perhaps unmeaningful, especially in attempting to correlate the subjective performance evaluations of audio and video to tested performance parameters.

The common transmission link through which all telecommunication information is processed on the Space Base can be considered to begin and end with a SMDS Modulator Group and Demodulator Group. All parts of this overall link have certain performance requirements in common. The link must be able to carry the signal with minimum degradation which means that signal levels over the amplitude and frequency of the system and the relative phase of all frequency components of the baseband telecommunications signal must be preserved. As a minimum, it follows that the general characteristics of the end-to-end link performance that must be specified are:

a. Transmission linearity (the amplitude frequency response of the link)

b. Phase linearity (normally specified in terms of envelope delay)

Depending on the particular method of transmission selected, the intermediary interfaces may require various forms of compensation and equalization. In the case of the modulator, where vestigial sideband modulation is used, the attenuation of the lower sideband while passing the upper sideband at full amplitude does not constitute a flat response at the modulator output. Overall flat amplitude response may be restored by compensating for this assymetrical modulator output in the demodulator.

The VSB filtering is an intentional amplitude distortion introduced into the modulation system to conserve transmission bandwidth. A second type of distortion present is that introduced into the system to compensate or equalize inherent nonlinear distortions produced by the non-ideal transfer characteristics of equipment components. For example, all pass delay compensation networks must be used to equalize envelope delay of the baseband signal across the input signal passband.

It has been suggested by this study that the NTSC color television system be used for color television transmission throughout Space Base. As indicated earlier in a color system trade study (see section 2.3), there are several alternative systems that could be utilized that are at various stages of development and perhaps even a more optimum color system not even considered or yet developed. There are known advantages and disadvantages of each color system and these must be weighed carefully before a final system choice is made taking into account the overall desired performance versus simplicity, size, weight, etc.

Regardless of which system is finally selected, it is a fact that all of these systems share many common features and, as a result, require similar transmission channel characteristics. Very briefly, television transmission is accomplished by transmitting a series of still pictures or "frames" at a rate which is fast enough that these pictures appear continuous to the eye when they are reproduced on a television monitor. The individual picture frames are formed by scanning the image to be transmitted that has been focused on a light sensitive image target of the television camera pickup tube. The scanning is accomplished by an electron beam which produces a voltage (at the camera tube output) proportional to the value of image luminance or brightness at the corresponding position of the beam spot as it strikes the tube target image. By scanning an image with three separate camera tubes simultaneously, or a single tube sequentially, each tube being sensitive only to one of the primary spectral colors (red, blue, or green), it is possible to convert color images into electrical signals. By periodically interrupting the rapidly varying image luminance voltage with suitable scanning synchronizing signals, and coding the color information onto a subcarrier signal which is summed with the luminance and synchronizing signals, the composite video signal is formed. Generally, it is only the color coding technique used in the various systems that makes any one particular color system unique. The color coding technique and the desired image resolution affect overall system bandwidth. The color coding technique primarily sets the amplitude and phase linearity requirements for the video system.

Whereas, the color video signal is a very complex waveform made up of several signal types (luminance, color hue and saturation, blanking, synchronizing, etc.), the PAM audio and digital data signals are a stream of multilevel constant width (RZ - return-to-zero) pulses. The amplitude and phase linearity requirements for the transmission and recovery of these signals by analogy with the video signals are intuitively of the same degree. The multilevel (PAM) pulses that would be driving a SMDS Modulator from a telephone or intercom can be equated to the transmission of a monochrome "checkerboard" television test pattern where the "tone" of each square represents a different light intensity ranging from white through various shades of gray to black. The transmission of bilevel digital data would correspondingly compare with the transmission of a monochrome black and white checkerboard television test pattern.

For a standard VSB television transmitter, the carrier amplitude is varied between modulation percentages of 12.5 and 87.5. The level of modulation is controlled by the instantaneous magnitude of the composite video waveform. Negative polarity modulation is used which simply means that for an increase in image brightness, the transmitter carrier is correspondingly reduced in amplitude. The composite television signal levels are allocated in the following manner. Active picture luminance values are transmitted with peak white representing 12.5 percent of maximum carrier level and peak black information representing 75 percent of maximum carrier level. Modulation levels between 75 and 87.5 percent are used to transmit blanking and synchronizing pulses. (Blank and synchronizing pulses do not appear on the monitor screen since they are transmitted at levels corresponding to blacker than normal peak image black levels. In fact, these pulses are of such an amplitude as to completely bias the monitor electron scanning beam off.) Commercial or standard television minimum carrier level is limited to 12.5 percent since it is required for the recovery of the accompanying audio signal. Since an SMDS system does not carry simultaneous audio in the 6 MHz channel along with the video signals, there are no restrictions on preventing carrier cutoff. However, this should not be a normal SMDS video transmission mode except as required for the PAM pulsed information described below.

Carrier cutoff is a mode of operation required of the SMDS Modulator when processing PAM or bilevel digital data; therefore, the modulator should be designed to provide for linear operation all the way from 0 to 100 percent modulation. In this mode of operation, the modulator must operate as a pulsed amplitude modulator whose output is a pulsed RF carrier

with an envelope amplitude corresponding to the amplitude of the sampled audio or digital signal level. Employing On-Off keying of the modulator carrier under the control of an incoming pulse stream requires that the modulating pulses be superimposed on a direct-current voltage bias level which corresponds to a carrier off condition. This requires direct-current coupling, of some form, through the modulator input stages to key the carrier On and Off. This is not compatible with standard video requirements.

It is a fact that direct-current transmission is employed in standard television. This is accomplished by sampling the level of the constant amplitude composite video waveform synchronizing pulses. This sampled level is then used at the transmitter and receiver to insert a direct-current bias level at the video modulator and detector, respectively, to re-establish the average picture brightness of the transmitted signal. This is accomplished without using direct-current transmission throughout the system. Infact, the normal video system usually requires only a minimum lower cutoff frequency of several Hertz below the video picture field rate of 60 Hz. (Recall that the upper transmitted video cutoff frequency is approximately 4.5 MHz.) Stated in a different way, direct-current transmission is used for conventional video but the carrier is always present. This is not compatible with the system requirements for a modulator with On-Off pulsed carrier operation.

The requirement for pulsed On-Off AM carrier operation might be better understood if the overall system technique of telephone, intercom, and data transmission between deck levels on the Space Base was reviewed at this point. Digital data and PAM audio (phone or intercom) are transmitted on the Space Base main transmission bus using a form of time division multiple access. In this technique, a single 6 MHz portion of the main bus transmission spectrum is assigned for each of these functions. That is, all Space Base telephone audio information is transmitted and received in a single 6 MHz bandwidth. All intercom audio information is transmitted in a second, but identical, 6 MHz transmission channel and similarly, all Space Base digital data is carried in a third 6 MHz transmission channel. These 6 MHz transmission channels have characteristics identical to those used for Space Base video transmissions, except that a separate 6 MHz channel is assigned for each camera since the entire 6 MHz bandwidth channel is required to transmit a single NTSC color television image.

In the case of telephone, intercom, and digital data each individual telephone, intercom, and digital station is assigned a specific time slot in which it may transmit information on the main bus (in its respective 6 MHz channel). This is to say that each transmitter has exclusive use of the main transmission bus during this preassigned time interval. As long as each unit transmits in its preassigned time interval there is no interaction among all of the units transmitting on the main line. Taking telephone operation as an example, the main bus access time for a particular telephone is a function of the Nyquist rate at which the audio voltage output of the telephone micorphone is sampled to produce a pulse-amplitude modulated data stream. These voltage samples are then assembled into a continuously interleaved data stream on the main bus, representing instantaneous telephone audio, dialing, and supervisory control information of all telephones.

The data information for a particular phone then occurs periodically at a definite repetition frequency which is the frame repetition rate of the system. The frame repetition rate for all other telephone channels would be the same but would occur at different times. The control of the time slot assignments of particular phones is accomplished by means of the master clock/frame signal routed around the Space Base in another 6 MHz channel dedicated for that purpose.

The preceding paragraphs of this section reveal the major problems faced by the modulator designer in achieving video and PAM data signal processing compatibility. The discussion only briefly touched upon the subject of definitive transmission link equipment, namely modulator performance requirements. The designer must know very precisely the characteristics of both types of transmitted waveforms to determine the most practical approach to implementing the SMDS Modulator Group as a piece of hardware.

Transmission linearity can be specified in a number of ways. For instance, harmonic distortion or intermodulation distortion measurements which are meaningful for audio frequency systems could also be performed on wideband video systems. However, the results of such testing would have little bearing on the observable effect of a video signal as displayed on a television monitor. On the other hand, the system amplitude and phase linearity performance required by the SMDS PAM time division multiplexing equipment would require perhaps a greater degree of system linearity than that for the video signal to meet overall system

performance objectives. It would be desirable to make the ultimate system performance and the performance testing techniques compatible and identical for both types of modulator input signals.

Definition of the performance requirements of the video transmission link for the NTSC color television system have been the subject of years of research and analysis. Methods of correlating these performance requirements to actual observed system performance have been refined extensively and have resulted in a variety of test methods which allow system design and maintenance to be performed in a relatively straightforward manner. Required system performance parameters of frequency versus amplitude and phase linearity are known and can be measured, compared, corrected, and controlled. Types of distortions, such as frequency response and phase response, are obviously detrimental to both video and PAM signals. Distortions such as differential phase, likewise, could be much more detrimental to NTSC color video than PAM transmission. The basic problem at hand is that while video performance can be predicated and tested, pulse amplitude modulation performance (especially in the proposed SMDS Baseline System) has not been correlated to video performance when the transmission link is characterized by video performance specifications. With a real transmission channel, intersymbol interference and related disrortions in the PAM equipment will always be present. The degree depends upon the designers ability to optimize the channel. At this time, without further study, it is anticipated that the bounds or approximations of actual PAM performance would be extremely tedious to derive without having some amount of empirical experimental data obtained from a working feasibility model of the system.

For the purpose of this study, the video and PAM transmission link requirements will be assumed to be compatible and in terms of the video performance objectives. In those instances where compatibility is not known, these areas will be identified. The ultimate resolution of the Modulator Group signal processing compatibility must be identified as a problem that will demand further study. This study may show that the Modulator Group implementation will require two completely different swirch-selectable modulator input processing circuits. See block diagram of Modulator Group, figure 4.2.5.2.1, which shows a separate "Data Processor" functional circuit block as part of the "Video Modulation Assembly." The SMDS Modulator Group testing criteria will be assumed compatible with present state-of-the-art video performance testing techniques.

8.3.2 Vestigial Sideband Filter/Delay Equalizer Implementation

The implementation of the vestigial sideband filtering in the SMDS Modulator can basically be accomplished using either of two basic techniques. This implementation also has a great deal of influence on the technique used for amplitude modulating the UHF carrier.

The Modulator Group could have taken the form of a continuous-wave (CW) UHF signal source whose amplitude was varied at the video rate by a high frequency wideband modulating stage functioning essentially as a voltage-controlled variable attenuator. The output of the modulating signal would then be a conventional double-sideband AM signal. This signal is then processed through a UHF filter (tuned to the appropriate UHF modulator output frequency) having the required lower sideband attenuation requirements needed for vestigial sideband transmission. Because of the required sharp cutoff characteristics of this filter, it is also necessary to equalize the group (envelope) delay across the passband.

In a multichannel system (such as the SMDS where a primary goal is equipment commonality) the implementation of the VSB filter and equalization at the final UHF operating frequency would require that every modulator in the system have interchangeable channel filters, each one tuned for a specific operating channel. This would require over 20 different filters and equalizers for the system. The physical realization of these filters at UHF frequencies is considerably more difficult than for some lower frequency.

For these reasons, it was determined that the best approach for SMDS Modulator implementation would be to accomplish amplitude modulation VSB filtering and equalization functions at a common intermediate frequency for all of the SMDS Modulators. All SMDS VSB filter and equalization circuits are then identical. The disadvantages of implementing the VSB filtering at the lower frequency will be physical size. As indicated above, the design of the filter at the lower frequency should lead to improved filtering characteristics and provide the necessary sideband attenuation for successfully achieving adjacent channel operation on the main transmission bus within the allocated 6-MHz channel-bandwidths.

Considerations in implementing the group delay equalizers necessary for required transmission fidelity should be briefly noted. The phase response of a transmission system should be linear with frequency, which means that there should be constant time delay for all baseband

frequencies up to 4.5 MHz and beyond. Phase linearity is especially critical in the vicinity of the color subcarrier frequency. Deviations from this linear characteristic causes lack of clarity and hue shift in television transmission. The received pulse fidelity of a PAM data stream is seriously degraded by differential propagation delays of the various frequency components which constitute the original transmitted pulse. Knowing that equalization is required, the only question remaining is the method of implementation. It is possible to perform this equalization at baseband (prior to modulation) or at the IF frequency. In either case, the transversal equalizer is a candidate, for it is an adjustable equalizer that produces harmonically related cosine variations of both gain and delay with frequency. This gives the designer flexible control over the optimization of the modulator group transfer characteristics since it is seldom that both amplitude and delay distortions occur independently of each other. Adjustable all-pass filter networks are also used for delay distortion compensation. The selected technique should be made based upon circuit complexity and the degree of equalization actually required. Current developments indicate that an adjustable three section equalizer at the IF frequency prior to the VSB filter would be a recommended approach.

One important constraint on modulator design that must be made is that of controlling the absolute signal propagation delay through the unit in processing signals on and off the main bus. Propagation delay of signals on the main bus is overcome by propagating a master clock on the main bus with the data signals. Absolute delay tolerances are a necessity to meet the unit interchangeability requirements that have been defined for SMDS system components.

Absolute signal propagation delay of the system modulator and demodulator units is almost totally a function of the transmission channel bandwidth. This bandwidth is established by the SMDS Modulator and Demodulator Groups since the remainder of the system is extremely wideband. The channel bandwidth is a direct function of the number of cascaded low-pass and bandpass amplifier stages used to process the signal through these equipments. Control of the absolute signal delay through these units is essential to proper operation of the telephone, intercom, and digital terminal equipments.

The design of the baseband signal processing equipments, for time division multiplexing of these signals, relies on the recovery of a master read and write clock signal from the main bus. The same modulator and demodulator groups used for transmission and recovery of the

the baseband data are used for transmission and recovery of the master clock and synchronizing signals on the main bus. Significant differences in the absolute signal delays, of the more than 80 modulator and 130 demodulator groups needed to implement the SMDS, would make variable delay compensation for data/clock time skew a necessity for each unit interface. This would create an almost insurmountable problem in system alignment and reliable operation. Obviously, this would defeat the entire system design goal of interunit commonality and interchangeability.

In summary, the modulator group design (also demodulator group) must have both absolute signal envelope delay control specified in addition to the normal envelope delay equalization over the wideband data channel to meet pulse and video transmission fidelity requirements. This compensation and control must be maintained over the system environmental operating conditions in addition to normal allowances for long term aging effects. This control can be only realized through the close manufacturing tolerance control made possible through the use of microcircuits and highly accurate testing made possible by recent advances in computerized network analyzer test instrumentation.

8.3.3 Frequency Upconversion Techniques

Since it has been determined that the ideal approach to creating the VSB signal is by means of using the common IF frequency technique, it is then necessary to translate the modulated IF signal to the final UHF operating frequency using some form of variable frequency upconversion technique. From a reliability, weight, and size point of view, it is desirable to avoid the use of electromechanical switching to connect a suitable mixing frequency (local oscillator) source to the upconverting mixing device. From a performance point of view, the use of crystal oscillator sources, or some equivalent form of direct or indirect frequency synthesis, to generate the 30 separate 6 MHz spaced channel frequencies was intuitively desirable. From a commonality view point, it would be advantageous if the upconverting local oscillator frequency signal source could be made identical to the downconverting local oscillator source needed for the SMDS Demodulator Group. This can be done if the modulator and demodulator IF frequencies are selected to be the same and the designer takes appropriate steps to eliminate potential EMI leakage from modulators and demodulators operating in close proximity. This may not be possible and separate upconverter and downconverter local oscillators may be required. Both units would still be identical in design but merely operate at frequencies offset from one another by some fixed amount.

It should be emphasized that the approach recommended for local-oscillator generation is one that meets the system design goal of commonality. By operating an appropriate channel selector switch on a modulator unit, any of the 30 UHF operating frequencies may be selected. Thus, making all modulators completely interchangeable by merely selecting the appropriate operating channel frequency for the particular application of that unit (video, telephone, intercom, digital, or master clock signal modulator).

The recommended approach for upconversion local-oscillator implementation is the use of 30 separate crystal sources which are selected by an appropriate selector switch. The trades and detailed explanations of this technique are given in the SMDS Demodulator Group discussion, section 4.2.5.3.4. Since the units are anticipated to be of identical design, the discussion does not bear repeating here.

8.3.4 Spurious Output Signal Suppression

In and out-of-band spurious outputs produced within the modulator group must be controlled by implementation of appropriate bandpass filtering to remove signal products resulting from the upconversion mixing and local oscillator signal generation. The local oscillator spurious products are fairly easy to suppress by using a group of fixed-tuned filter networks. The decision to implement a modulator that would operate on any of the 30 required output frequencies requires the development of a voltage-tunable bandpass filter that will track the desired output frequency of the upconversion mixer.

The requirement for an identical filter to operate as a voltage-tunable preselector in the SMDS demodulator makes development of this filter, needed for modulator output signal spurious suppression, a common task just as for modulator and demodulator upconversion and downconversion local oscillator units. This filter, when integrated into the modulator assembly, effectively suppresses the original IF frequency, LO-frequency, upconversion image signal (F_{LO}-F_{IF}), and mixer generated spurious products, and prevents them from falling on top of any other 6 MHz signals distributed on the SMDS main line distribution bus. The determination of these spurious mixing products is possible using computerized spurious product analytical techniques, which are used to solve the general equation:

$$F_{out} = n F_{IF} \pm m F_{LO}$$

where n and m are intergers.

Such a program is in use at Radiation Incorporated and a sample of this analysis technique is given in section 9.0, SMDS Demodulator. Since the demodulation preselector requirements are more stringent than for the modulator, a spurious analysis for the upconversion process was not performed during this study. Experience has shown that this effort would have been redundant for purposes of the hardware definition. It is recommended as a design precaution, that this proposed conversion process be verified prior to final hardware implementation.

8.3.5 Size and Weight Minimization

The physical size and weight of the SMDS Modulator Group is controlled primarily by those components which cannot be adapted to some type of hybrid microcircuit development. Since present state-of-the-art techniques are rapidly advancing in the frequency ranges of interest (DC to UHF), it is anticipated that all functions can be miniaturized except for the filter elements, in particular the VSB filter. This unit is conventionally a cavity type, high Q, 5-section filter that would be difficult to miniaturize. With this unit constraining modulator size, it is essential that all circuitry be implemented using microcircuit techniques.

The specific microcircuit development required for the modulator group will be entirely dependent on function implementation. At this time, no special requirements are foreseen that could not be undertaken. Specific development requirements recommended for special additional study are in the following areas:

a. Voltage Tunable Bandpass Filter

b. Local Oscillator Synthesizer

c. Delay Equalizer Circuitry

Due to the large number of modulator groups required in the system, the design goal of converting all discrete circuitry to hybrid microcircuits will be, of necessity, a design requirement.

Television modulators (performing equivalent functions of a SMDS Modulator) designed for CATV use have the following size and weight characteristics:

Width:	19 inches
Height:	3-1/2 inches
Depth:	12 inches
Volume:	800 cubic inches
Weight:	10 pounds

If volume could be reduced by approximately a factor of 10 (for 80 to 100 cubic inches), projected modulator group size could be 5 by 4 by 5 inches. A weight reduction of 1/4 to 1/5 would produce a unit weighing 2 to 2.5 pounds. Size and weight reduction beyond this point would become extremely expensive.

8.3.6 Power Consumption Minimization

Due to the large number of SMDS Modulator Groups required to implement the proposed telecommunications system, it is absolutely necessary that power consumption of these units be minimized. Even though completely redundant modulators are proposed, the total power requirement of the system modulators remains approximately the same since redundant units will be in a standby mode and draw a minimum of power. Since transfer to the redundant unit is intended to be a manual transfer operation, input power switches could be interlocked to prevent simultaneous powering of both the on-line and redundant unit (except for cases where the override of this feature is intentional). This technique, when applied to the entire system (except for the redundant main line amplifiers where simultaneous powering of redundant main bus lines may be necessary) can significantly reduce the overall system power consumption. The power consumption of individual modulator units must still be minimized to make the system feasible.

Currently, commercial modulator units which perform a similar function as that required for the SMDS modulator have advertised maximum input power requirements of around 8 watts for a regulated input voltage of 20 Vdc. The degree to which this power dissipation will be reduced or increased by further circuit simplification and improved performance refinement is extremely difficult to predict since these units are taking full advantage of currently available MSI circuits, wherever possible. The ultra-linear performance required by the modulator group is actually not consistent with minimum power consumption or, in other terms, maximum operational efficiency.

It is predicted however, that some degree of power consumption reduction can be realized by using total microcircuit implementation of the circuit functions and minimization of overall circuit complexity in the modulator group. This is intuitive by virtue of the fact that, unless power consumption is reduced with the inherent high density component packaging that is achieved with microcircuits, heat dissipation in such small packaging volumes will become a thermal design problem. It will be seen later that to achieve the ultra-linear wideband amplification necessary in the SMDS buffer and main-line amplifiers, a great deal of power must be dissipated in the active devices to meet system intermodulation and cross-modulation requirements. Fortunately, both for modulator and demodulator wideband amplification requirements, only single channel-modulated carvers are processed by bandpass filtering of the desired transmitted or received signal. High power consumption is not required to suppress distortion products over the transmitted or received channel bandwidths.

It appears that a power consumption budget of 6 watts would be realistic for a SMDS Modulator Group and this estimate will be used for computing overall SMDS power requirements.

8.3.7 Modulator Group Testing Techniques

8.3.7.1 Performance Requirements

The specifications necessary to guarantee the minimum required performance of the SMDS Modulator as given in the developmental specifications (located at the back of section 8.0) ultimately established at the completion of the hardware implementation phase of the SMDS development will undoubtedly be well defined. As discussed earlier under Input Signal Compatibility Considerations, the definitive performance requirements of the modulator group cannot be considered absolute and final. These specifications must necessarily be the starting point from which the final performance specifications will evolve. However, there are several measurement techniques that verify video performance specifications which should be briefly discussed. The measurements, normally associated with these specifications, are somewhat complex and require test equipment not normally catagorized as standard when color television transmission is involved. Specialized color television test waveform/pattern generators, waveform time/frequency domain analyzers, and monitors are required for comprehensive testing of video transmission channels.

Since it is often standard practice to perform baseband-to-baseband (video-to-video) measurements on transmission equipment (such as for microwave links) by connecting modulators and demodulators back-to-back, this approach would seem easiest for SMDS applications. This is not practical however, unless an "ideal" or known performance demodulator is available for testing the modulator or, conversely, an ideal or known modulator is available for testing a demodulator. Therefore, although the majority of SMDS measurements can probably be made on a video-to-video basis, operating a "standard" demodulator with a "modulator under test" connected in a back-to-back arrangement, a certain number of video-to-RF measurements must be made to characterize, calibrate, and maintain the performance characteristics of the "standardized" unit. This is necessary simply because of the large number of modulator and demodulator units which comprise the SMDS and the tolerances on certain parameters that must be closely controlled. This ensures that transmission paths among any and all of the more than 20 model Space Base deck levels can be continuously maintained in all modes of operation, especially for the PAM and digital data signals. It also guarantees the success of the common module interchangeability concept whenever repairs must be made by module replacement, minimizing the necessity for alignment, which should be avoided if at all possible.

The specifications which are important to color video transmission are baseband frequency response, envelope delay, differential gain, and differential phase.

8.3.7.2 Frequency Response

The frequency response output characteristics of a standard VSB modulator are shown in figure 2.3.4. At the modulator output, frequencies of $\pm$0.75 MHz on either side of the carrier are transmitted double-sideband. Below -0.75 MHz, the lower sideband is attenuated and above +0.75 MHz on out to 4.5 MHz, the upper sideband has a flat response. The ideal detected output of a standard vestigial modulator is shown in figure 2.3.4. The required demodulator response characteristic needed to restore constant gain to all transmitted frequencies and properly reproduce transmitted signal waveforms is shown in figure 2.3.4. Departure from flat gain at low frequencies causes "streaking" in the observed monitor image just as high-frequency gain variations cause loss of detail, spiking, ringing, and inaccurate color saturation. The amplitude response characteristics can be measured by sweep techniques on a video-to-video basis or measured at the RF output of the modulator on a video-to-RF basis using a spectrum

analyzer. This method is often supplemented with the measurement of low-frequency performance with a modulator and demodulator connected back-to-back and measuring the amplitude variations (tilt and sag) of a 60 Hz squarewave processed through the units.

8.3.7.3 Envelope Delay Distortion

Envelope delay distortion is the result of variations in the propagation time of video signal components across the video passband. This distortion significantly alters the time coincidence of the luminance and chrominance portions of a color video signal resulting in misregistration in the colors of the reproduced image. This distortion also causes overshoot, undershoot, and ringing of the video signal. Envelope delay distortion is commonly caused by sharp or sudden nonlinearities in the system amplitude passband characteristic. In the case of the SMDS modulators and demodulators, absolute envelope delay must be specified, measured, and controlled. This measurement may be performed on a video-to-RF, RF-to-video, or video-to-video basis. Envelope delay measurement equipment is produced and is currently available.

8.3.7.4 Differential Gain

Differential gain is the change in gain of the modulator/demodulator signal processing circuits as the level of the signal is varied over the full dynamic range of the allowable input signal levels. For color television, differential gain causes the amplitude of the color subcarrier to change as it "rides" on the luminance signal which can vary from a "white" level to a "black" level amplitude. This causes color saturation to change as a function of picture brightness.

In the NTSC system, differential phase is a change of color subcarrier phase as a function of luminance level and causes the color "hues" to change as a function of picture brightness. Differential gain and phase measurements are made with a special "modulated staircase" waveform generator. The generator output is applied to a modulator input and recovered at a demodulator output with a television waveform monitor (similar to an oscilloscope) and a unit known as a "vectorscope." Differential gain and phase through the units is then interpreted from the resulting displays.

8.3.7.5 Other Tests

Other tests which are performed on modulators and demodulators on a video-to-video basis are multiburst signal, window signal, and sine-squared pulse; all of which are produced

by currently available waveform generators designed specifically for television performance testing. Sine squared pulse testing is perhaps the most used total system performance test and is considered to represent the equivalent transient response, resulting from a peak white to peak black level within the duration of the smallest picture element. If the half-amplitude width of a sine squared pulse is equal to the reciprocal of the baseband high frequency limit, then any amplitude or delay distortion within the video bandpass (4.5 MHz) will distort the pulse since its entire frequency spectrum is contained within the system bandwidth. Waveform distortion characteristics can be used as an indication of the type of distortion present. A numerical performance rating system, based on subjective tests and the sine squared pulse waveform distortion known as the "K" rating measurement (K = 1, 2 . . . . 10, where 1 is considered best), is often used to specify overall system performance.

The above described tests relate to video performance. The remaining unfinished task is to specify the additional PAM/digital compatibility tests needed to completely characterize modulator/demodulator performance. These tests could include bit error rate, harmonic distortion, rise and fall time, and other related functional tests.

The designer must become completely acquainted with the testing tools available to him in implementing the SMDS modulator/demodulator units. The above discussion has reviewed the major test techniques that are recommended for use in the development of the SMDS Telecommunications Equipment.

8.4 MATHEMATICAL ANALYSIS OF DESIGN

Mathematical analysis of the recommended SMDS Modulator Group design has been restricted by the fact that its function and theoretical performance as a color television modulator have been specified to be identical to that of current NTSC color television system design. The analysis of design on a television basis is well documented in the cited reference literature and will not be repeated here. If future study of television systems for Space Base applications should indicate that a television system having significantly different characteristics from those of the NTSC system is desirable, the extent of additional analysis of the SMDS design must be determined at that time.

As discussed in section 8.3.1, there is a recognized problem in assuring video and PAM transmission compatibility. Although analysis has been performed on the use of a VSB video transmission channel (modulator/transmission link/demodulator chain) from a system viewpoint (see section 4.2), this compatibility problem has not been addressed specifically through analysis for the modulator group. PAM and digital data interface compatibility between the modulator and other SMDS equipments (Central Telephone Electronics, Central Intercom Electronics, and Digital Terminals) has been assured through overall system design.

A spurious analysis technique for the upconversion function of the modulator is similar to the analysis used for downconversion spurious analysis used for downconversion spurious analysis described in section 9.3.2. This analysis is not repeated here.

Analysis required that will be unique to the modulator group design will be dependent on the actual hardware implementation. The functional description of a recommended modulator design describes the general guidelines to be followed by the designer. It is important that the concept of a totally integrated system be retained in the final design and this will be an important task in systems management during the SMDS hardware development phase.

8.5 THEORETICAL PERFORMANCE OF DESIGN

The theoretical performance of a SMDS Modulator will be that performance specified or required by the modulator as a part of overall system specified performance. The theoretical performance of the modulator must necessarily be related and compatible with the corresponding demodulator. This was discussed in more detail under Modulator Group Testing Techniques (section 8.3.7) and will not be repeated here. The theoretical performance of the Modulator Group and all other system subcomponents are more appropriately discussed under the classification of overall system theoretical performance and will not be discussed at this equipment level.

8.6 EXPERIMENTAL PERFORMANCE OF DESIGN

No actual experiments were performed as part of this study. However much of the experimental work performed by the television industry is referenced throughout the study.

8.7 TRADE-OFFS

The trade-offs made in arriving at a recommended SMDS Modulator Group design are included as part of the section covering Modulator design problem resolutions (section 8.3) and will not be treated under a separate category of design trade-offs for a system subcomponent.

8.8 SUMMARY

The SMDS Modulator design should generally use present state-of-the-art television modulator circuit design techniques to develop workable breadboard units that are functionally compatible and meet specified system performance requirements for all telecommunications systems operating modes; i.e., television, PAM audio, and bilevel digital data. Specific attention must be given to this interface compatibility to meet the design goals of maximum equipment modularity and commonality. This equipment breadboard and system feasibility phase of the SMDS Modulator and Demodulator subunits could conceivably rely heavily on rapidly developing technology of equipments used for CATV systems. In addition to more detailed paper analysis of the system design, the modification of commercial equipments to meet specific SMDS applications would minimize the developmental costs associated with proving system feasibility. It is emphasized that the final system feasibility can only be demonstrated by the construction of an actual breadboard system. This should be done prior to what might be considered the second phase of SMDS Modulator and Demodulator development; i.e., subunit size, weight, and power consumption minimization. The development of hybrid microcircuits and performance requirements shall be dictated by the results of feasibility system testing.

In summary, specific areas identified as a result of this study that will require further study of recommended techniques prior to hardware implementation are:

1) Television/PAM Audio/Bilevel Digital Signal Processing Compatibility
2) VSB Filtering and Delay Equalization Circuit Implementation
3) Local Oscillator Synthesizer Implementation
4) UHF Voltage Tunable Filter Implementation

8.9 SCHEMATICS AND DRAWINGS DEVELOPED

The drawings relating to the Modulator Group appear in section 4.2.5.2, volume I, of this report.

8.10 DEVELOPMENT SPECIFICATION

The following development specification is provided as a part of this section:

SMDS Modulator Group

SMDS MODULATOR GROUP

DEVELOPMENT SPECIFICATION

1.0 SCOPE

This specification describes the development design goals and major performance specifications of a SMDS functional building block identified as a Modulator Group.

2.0 APPLICABLE DOCUMENTS

The guidelines, trade-offs and functional descriptions included as part of the SMDS Final Report shall be considered as a part of this subunit specification. References cited in the Final Report shall be used for developmental guidance.

3.0 ELECTRICAL PERFORMANCE REQUIREMENTS

The SMDS Modulator Group shall accept baseband color television or pulse amplitude modulated (including bilevel) digital data as an input signal and translate the input information signals to a UHF vestigial sideband amplitude modulated output signal for transmission via a coaxial cable distribution system to a remotely located SMDS Demodulator Group appropriately tuned to the Modulator Group UHF output frequency.

3.1 Input Signal Requirements

The Modulator Group shall accept input signals as described below and provide specified performance. Input signal compatibility, if necessary, may be accomplished through a "mode" switching function which is to be an integral part of the Modulator Group design.

3.1.1 Input Signal Equipment Interfaces

The Modulator Group shall accept input signals from the following equipments:

a. Color Television Camera
b. Central Telephone Electronics
c. Central Intercom Electronics
d. Pilot and Terminal Master Clock Generator
e. Digital Station Terminal
f. Central Time Unit Format Control Unit

3.1.2 Input Signal Characteristics

The input signals to be processed by the Modulator Group shall be of three general types described below and are referred to as operating "modes".

a. Composite Color Television Signal - The Modulator Group shall accept a NTSC composite color television signal with a peak-to-peak amplitude of 1.0 ± 0.1 volts which contains all necessary luminance, synchronizing, and color information necessary to

recover the televised image with a NTSC compatible color television monitor. (The monitor receives this compatible signal via a SMDS Demodulator Group)

b. Pulse Amplitude Modulated Audio and Bilevel Digital Data - The Modulator Group shall accept a PAM data stream at a maximum rate of 640 Kbps. The signal shall be unipolar with a positive DC component of an amplitude sufficient to cause the modulator to operate in a pulsed ON-OFF keying mode. The presence of an input level of a magnitude less than the input signal carrier cutoff bias shall cause the Modulator Group to transmit a VSB modulated UHF carrier with a carrier amplitude proportional to the input pulse amplitude. The unitary input pulse amplitude variation shall not exceed 1.0 ± 0.1 volt peak-to-peak fro the carrier cutoff input bias level. The Modulator Group shall also operate in this pulsed ON-OFF keying mode when transmitting a bilevel data stream at a maximum rate of 2.56 Mbps.

c. Bilevel Master Timing (Clock) Data - The Modulator Group shall accept a bilevel master timing signal that operates at a constant frequency of 2.56 MHz with periodic interruption with a frame synchronization code. The Modulator Group does not operate in a pulsed ON-OFF keying mode as in b. above and in the absence of an input signal provides a continuous wave (CW) unmodulated RF output carrier at the selected channel operating frequency. The peak-to-peak amplitude of the input signal shall not exceed 1.0 ± 0.1 volt peak-to-peak.

3.1.3 Input Impedance Characteristics

Input impedance of the Modulator Group for all operating modes shall be 124 ohms balanced with a maximum input VSWR of 1.5 to 1.

3.1.4 Input/Output Signal Bandwidth-Rise Time Requirements

The input signal/output signal bandwidth-rise time requirements for the SMDS Modulator, when measured on a baseband-to-baseband basis with a Modulator Group output connected to the input of a properly performing SMDS Demodulator Group, shall be flat from 50 Hz to 4.5 MHz ± 0.5 dB with a maximum square wave pulse rise time of 100 nanoseconds with less than 3% overshoot. Low frequency tilt/sag shall be 1% maximum for a 60 Hz square wave. Where internal DC restoration or processing of a DC bias on the input/output signal is required, this shall be provided as required. To minimize phase-linearity distortions, input and output video stages shall have a bandwidth in excess of 10 MHz.

3.1.5 Input Signal Common Mode Rejection

Input signal circuitry common mode rejection to hum and noise shall be 60 dB minimum.

3.2 Modulation Requirements

The modulator Group shall modulate the three input signal types described in section 3.1.2 and provide the specified performance as described below.

3.2.1 AM Modulation Capability

The Modulator Group shall have a modulation capability of 0 to 100% for input signal levels between 0.5 to 1.0 volt peak-to-peak (via adjustable modulation level control) and be properly compensated to provide 2 degrees maximum differential phase and 1 dB maximum differential gain for modulation depths ranging from 10% to 90%.

3.2.2 Vestigial Sideband Characteristics

The Modulator Group shall attenuate the lower or upper sideband responses of the conventional double sideband AM signal in accordance with standard NTSC vestigial sideband characteristics.

The transmitted sideband attenuation characteristics shall be such that all transmitted modulated signal energy greater than 1.25 MHz below the UHF carrier appearing in the next lower adjacent channel shall be a minimum of 60 dB below the desired adjacent channel peak signal level. All signal energy greater than 4.2 MHz above the UHF carrier appearing in the next upper adjacent channel shall be a minimum of 60 dB below the desired peak adjacent channel signal level.

Amplitude response between the limits of 1.25 MHz below and 4.2 MHz above the transmitted UHF carrier frequency for any channel shall not vary (ripple) more than ± 1 dB from the level of a 200 KHz sinewave reference signal.

3.2.3 Absolute and Relative Envelope Delay Characteristic

The absolute envelope delay versus frequency characteristic of an input signal applied at the Modulator Group input terminals and appearing at the modulator output terminals shall be fully equalized across the frequency band of 0.010 to 4.20 MHz to 200 ± 20 nanoseconds when measured using standard video-to-RF envelope delay measuring equipment.

3.3 Output Signal Requirements

The Modulator Group shall provide the specified output performance as described below.

3.3.1 Output Signal-to-Noise Ratio

The Modulator Group shall provide a minimum output signal-to-noise ratio of 50 dB when measured between peak output signal level and rms noise.

3.3.2 Output Spurious Frequency Suppression

The Modulator Group output spurious signals, both harmonically and nonharmonically related to the desired signal, shall be suppressed a minimum of 60 dB below the peak output signal level.

3.3.3 Output Carrier Frequency Range and Selection

The Modulator Group shall have provisions for switch selection and operation on any one of 30 separate UHF carrier frequencies in the frequency range of 300 to 500 MHz. Carrier frequency separation shall nominally be 6.0 MHz. Carrier frequency deviation shall be ± 1000 Hz. Exact operating center frequencies within the 300 to 500 MHz bandwidth shall be selected to minimize Modulator Group complexity as determined by the method of generating upconversion mixing frequency and modulator intermediate frequency.

3.3.4 Output Carrier Frequency Stability and Accuracy

The output carrier frequency stability and accuracy shall be ± 0.003% over the operating temperature range.

3.3.5 Output Power Level

The Modulator Group shall be capable of providing a maximum modulated output level of -5 dBm with provisions for reducing this level a total of 12 dB in 1 dB steps. Unit shall not be damaged by accidental output-signal port short circuits.

3.3.6 Output Power Level Stability (Long Term)

The Modulator Group shall not cause the measured peak output signal level to vary more than ±0.5 dB for a periodic input signal of constant amplitude when measured over a 30-minute time interval.

3.3.7 Output Impedance Characteristics

The Modulator Group output impedance shall be 60 ohms unbalanced with a maximum output VSWR of 1.5 to 1.

3.3.8 AM Hum and Noise

Hum and noise in the band of 30 Hz to 15 kHz of the modulated signal shall be 60 dB minimum below the level which would be produced by 100% modulation of the carrier with a single frequency sine wave.

3.4 Internal Fault Detection Provisions

The Modulator Group shall be designed to include built-in fault detection circuitry with an appropriate indicator signal to indicate abnormal operation or unit failure by monitoring key DC power and signal levels within the unit.

3.5 Power Supply Requirements

The Modulator Group shall accept a maximum of two dual-polarity DC input voltages with a maximum level of 30 volts. Total input power shall not exceed 6 watts with a design goal of 4 watts.

Power supply overloads, due to Modulator Group circuit faults, shall be protected against by suitable overload and surge protection.

3.6 Size and Weight Requirements

The Modulator Group shall have a maximum weight of 4 pounds with a design goal of 2.5 pounds. Unit volume shall not exceed 100 cubic inches with a design goal of 60 cubic inches. Unit form factor shall be made compatible with overall system maintainability and packaging constraints.

3.7 Miscellaneous Design Guidelines

Modulator Group development specifications must be considered flexible in terms of developing a totally integrated SMDS design. Trade-offs not considered or recognized as problems in this study may require deviations from the specifications stipulated above.

SECTION 9.0

SMDS DEMODULATOR GROUP

9.0 SMDS DEMODULATOR GROUP

9.1 ACCOMPLISHMENTS

This study has identified the functional requirements of a system subunit which has been designated the SMDS Demodulator Group. This basic building block of the overall system performs the inverse function of the SMDS Modulator Group described in section 4.2.5.3. This unit demodulates any single VSB (vestigial sideband) amplitude modulated television or PAM/digital signal distributed throughout the Space Base via any of the 6 MHz wide UHF main bus transmission channels.

Just as with the implementation of the modulator group, the distributed nature of the SMDS requires that each demodulator group operate as a single channel unit, independent of all other system demodulators. It retains complete interchangeability with other SMDS Demodulator Groups through appropriate and UHF channel tuning provisions, which are incorporated into the design. However, on a collective basis the demodulator groups perform the demultiplexing function of the individual "channel modem" of a conventional frequency division multiplexing terminal where all multiplexed signals are received at a single location.

As determined during system hardware grouping trades, the desirability of using a building block approach to configure the baseline SMDS for the "Y" Space Base concept allows for a great deal of system configuration flexibility if the SMDS should be implemented for a Space Base of a different design. In any configuration conceived, the suggested demodulator group hardware implementation would be directly compatible. As with other SMDS building blocks, this recommended maximum functional commonality approach has strongly influenced the proposed developmental specifications. Also this approach serves to minimize SMDS spares provisioning required to maintain the overall system fully operational throughout an anticipated 6-month resupply cycle.

9.2 PROBLEMS

The SMDS Demodulator Group is categorized as a major module building block of the Space Base Telecommunications System. The major hardware implementation problems associated with the design of a SMDS Demodulator Group, that meets the performance and functional interchangeability requirements defined for the equipment, are as follows:

a. Voltage Tunable Preselect Filtering

b. Frequency Downconversion Techniques and Spurious Signal Suppression

c. IF Amplifier and Video Detection Techniques

d. Size, Weight and Power Minimization

e. Testing Techniques

These problems and the designers approach to the resolution of those problems are addressed separately in sections 9.3.1 through 9.3.5, respectively.

9.3 RESOLUTIONS

9.3.1 Voltage Tunable Preselect Filtering

The requirement for preselect filtering of multiple carrier signals (occupying nearly an octave bandwidth from 300 to 500 MHz) is one that is dictated by achieving adequate suppression of undesired spurious mixing products resulting from the downconversion process. The ideal preselection filter would pass the desired modulated signal to be demodulated with minimum attenuation, and to attenuate all other signals appearing at the demodulator input below some maximum allowable level. Fortunately, ideal preselector filter characteristics with extremely sharp bandpass cutoff skirts are not required for the SMDS Group Demodulator; primarily, due to the proposed use or a balanced mixer to accomplish the downconversion. Determination of the required preselect filter characteristics is one which can only be made after the type and level of spurious products for various input signal frequency ranges and intermediate frequencies are evaluated. This is an extremely lengthly process unless some computerized analysis technique is used. Even then, many different and usually conflicting hardware implementation constraints are imposed on the designer and must be, at least tentatively, resolved before the spurious analysis for the demodulator begins. These primary constraints are discussed below.

It has been previously concluded that the SMDS transmission channels will start at 300 MHz and could potentially extend to 600 MHz before second order intermodulation products would fall in this band due to main distribution amplifier nonlinearities. Therefore, the design of the demodulator could feasibly require operation with input frequencies over the 300 to 600 MHz range. However, the projected SMDS bandwidth requirements place the upper

limit near 500 MHz for approximately thirty 6 MHz channels. The operating input frequency range over which the demodulator circuits must operate then is constrained to the 300 to 500 MHz range and, as a result, the tuning range of the preselector filter is defined.

In choosing a suitable intermediate frequency for the demodulator, conventional spurious mixing products, image responses, IF amplifier fabrication limitations, and special vestigial sideband signal response equalization techniques must be considered. It is commonly accepted that high IF frequencies tend to minimize image frequency problems. Low IF frequencies allow for increased channel selectivity, both of which are requirements for eliminating adjacent and interchannel interference problems in the SMDS such as 150 MHz would minimize spurious and image problems along with preselection filtering requirements. An IF frequency in this range is not compatible with the performance requirements of currently realizable monolithic integrated circuit IF amplifier stages. The necessity for the use of microcircuits has been selected for use in the demodulator to achieve size, weight, and power consumption minimization. With these hardware constraints, the IF frequency becomes a problem of selecting a suitable frequency, tentatively in the 40 to 70 MHz range. It should be noted that 45.75 MHz is the standard commercial television receiver intermediate frequency.

There are three general techniques for achieving preselection filtering over a very wide bandwidth.

Technique 1: Switchable filters having necessary preselect bandwidth with overlapping ranges to cover the required input frequency range. This is the conventional method used in commercial television receivers.

Technique 2: Continuous or step type filter tuning using variable or discrete DC voltages to bias varactor tuned filter elements.

Technique 3: Tunable microwave (UHF) active filters using the internal inductive properties of transistors operating in the inverted-common collector mode (ICC) as the variable reactance.

Of these three techniques (while all functionally equivalent) the voltage tunability and small size associated with 2 and 3 are the most feasible approaches for the SMDS bandpass filtering applications. It should be emphasized that there are two additional applications for a

UHF bandpass filter in the system in addition to the bandpass preselection application in the demodulator group. These are (1) the UHF upconversion mixer output filtering of the modulator group and (2) the AGC (automatic gain control) and ATC (automatic tilt control) pilot channel filters required for the SMDS Main Line Amplifiers (See sections 4.2.1.4 and 4.2.3.1.1 The design of a single voltage tunable UHF bandpass filter covering the 300 to 500 MHz range, which will satisfy UHF filter requirements for all three SMDS equipments, is obviously desirable. The application of a precision regulated bias tuning voltage (derived from a ladder type voltage divider network) under the control of a channel selector switch will center the filter around the desired 6 MHz channel. In the case of the Main Line Amplifiers where master timing (pilot) channels must be monitored for leveling and line equalization purposes, the filter networks can be identical. However, the tuning bias voltage (channel select) switching network can be simplified due to the limited number of channels involved.

The tunable microwave active filter appears to show the most promise as a universal filter that will meet all SMDS requirements. The development of units similar to SMDS requirements have been successful to date and have decided advantages over the varactor tuned filter. Although cavity type helical resonator, varactor tuned filters are available now, the narrower bandwidth (selectivity) characteristics, significantly smaller size and weight, direct adaptability to microcircuit fabrication techniques, wide dynamic range, low insertion loss and noise figure make the active filter the preferred device. These devices also exhibit low-temperature sensitivity and high-tuning stability despite their active nature, thus minimizing the problems facing the designer in this area.

With the overall system filter constraints known, it is possible to proceed with a spurious analysis and select the appropriate preselect filter requirements for the demodulator group, to control the level of undesired spurious responses. When the spurious analysis results are discussed (section 9.4.1), it is shown that by using the spurious suppression properties of balanced mixers, the filter design is not extremely critical. Also, this analysis shows that the filter can be a single resonator having 3 dB and 20 dB bandwidths of 12 MHz and 60 MHz, respectively. However, it will probably be necessary to use a two resonator filter design to guarantee meeting all filter application requirements in the SMDS, especially if the final implementation uses this filter for pilot filtering in the Main Line Amplifier.

9.3.2 Frequency Downconversion Techniques

As discussed earlier, the advantage of double balanced mixers in suppressing spurious products makes this device a superior choice over other mixing techniques available in extremely small physical packages and make their application here compatible with size and weight constraints placed on the demodulator group design.

The remaining design trades which must be made are primarily in the area of selecting an appropriate method for generation of the mixer local oscillator injection frequency. The discussion of these hardware trades has been deferred to this time as it is the demodulator group that will determine the design of an all-channel UHF local oscillator synthesizer since, at least for the Monitor Video Terminals, the demodulator must be tunable over all of those SMDS channels carrying television video signals. From a maximum commonality point of view, the use of this all-channel synthesizer has been an important premise to SMDS design for both modulator group and demodulator group UHF upconversion and downconversion applications, respectively. Alternate techniques that would compromise this commonality are available and are discussed below.

There are five general techniques available for generating the required frequency conversion local oscillator signal.

Technique 1: Direct or indirect local oscillator synthesis for each channel using switch selection control.

Technique 2: Separate crystal oscillator/multiplier chain sources for each SMDS channel. These can be separate plug-in units for the case of all modulators and demodulators only required to operate in a single channel. (Those demodulators used for PAM/digital and master clock applications in the Base Level/Deck Level Interface Units and the Pilot Terminals.) However, the Video Monitor Terminal demodulators would require switch selection of separate oscillators to enable reception of any video channel originating in the Space Base at a single monitor location.

Technique 3: Single LC local oscillator with mechanical switching (servo tuning) of oscillator resonant tank circuit elements to produce the appropriate output frequency. (This is the conventional technique used in commercial television receivers.)

Technique 4: Continuous variable tuning of LC oscillator using variable reactive element.

Technique 5: Detent or pushbutton tuning of LC oscillator frequency using switch selected DC bias voltages applied to varactor elements of the oscillator resonant tank circuits.

Detailed study of the above techniques shows that determination of a preferred technique of local oscillator generation must be made on the basis of desired performance, circuit complexity, operational simplicity, reliability, and general suitability for Space Base equipment applications.

Except for technique 4 above, the final output frequency of the LO frequency source would be a form of switch selection. The overwhelming disadvantage of the variable tuning approach along with any of the single LC (free running) local oscillator techniques is frequency channel setability and long term stability. This is in addition to the temperature induced frequency drift problems associated with these techniques. The reliable switching of circuit elements suitable for use at UHF frequencies would be inherently unstable due to the difficulty of controlling stray circuit capacitances, and it is for this reason that present commercial UHF television tuners have been of variable tune design. Recently, several UHF signal sources using varactor tuned LC oscillators have been introduced to the commercial market. However, these tuners still are susceptible to frequency drift, although not to the extent of the variable tuners since DC bias voltages are used to change the oscillator operating frequency. Automatic frequency control circuitry is also used to overcome drift problems in these commercial units.

For modulator applications, a stable modulator output frequency is a must to maintain control over transmission channel assignments. This necessarily dictates crystal control for both television modulators and modulators operating as PAM/digital modulators. This limits the modulator local oscillator generation to techniques 1 or 2 above. The disadvantages of technique

1 lie in the fact that the synthesis technique is somewhat more complex and unreliable than is justified to generate the relatively low number of LO channels (approximately 30) for the modulator. The advantages of technique 1 are the simplicity and reliability of separate crystal/multiplier sources. This is especially true if modulator channels are preassigned by location such that rather than switch selection of output frequency, frequency selection is accomplished by plug-in LO sources capable of operating on a single frequency. This approach complicates the spares provisioning problem for then the modulator groups are not directly interchangeable without changing output operating frequency. Moreover, lack of switch selection of LO frequency for the modulator makes this LO source incompatible with SMDS Demodulator Group requirements which must be capable of tuning all SMDS channels, at least for all channels carrying video information. Separate plug-in crystal oscillator/multiplier sources used for the modulator groups could be used for non-video demodulator applications.

The use of any of the LC oscillator approaches for demodulator applications can be essentially ruled out on the basis of an additional fine-tune control needed by the operator to compensate for local oscillator drifts that will occur due to temperature, voltage variations, and aging effects.

The above trades have shown the preferred approach for both modulator and demodulator local oscillator generation to be a choice between techniques 1 or 2. Implementation of these techniques is discussed in more detail below.

A digital frequency synthesizer (technique 1) has the advantages of a large number of available channels, a high degree of stability (since only one standard is used), and small size/channel ratio for a large number of channels. Technique 2 is a set of crystal oscillator and multiplier chains, each of which will be capable of generating ten channels.

The synthesizer approach requires an initial degree of complexity to generate even a few channels. To increase the number of channels requires only a minimal change to the logic, providing that the original design has the possible expansion taken into consideration. In the simplest configuration, the synthesizer is indeed feasible with present-day technology. The most difficult area would be that of the first prescaler shown in figure 9.3.2-1.

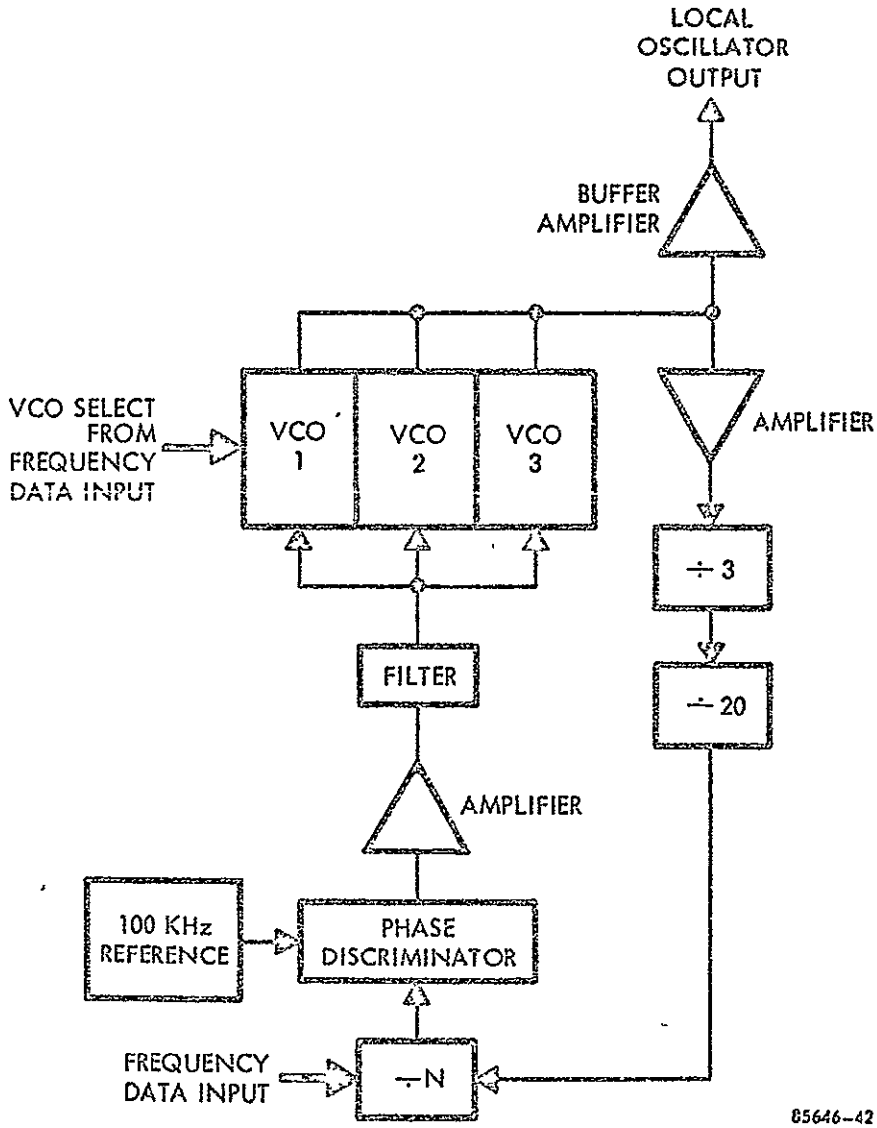


Figure 9.3.2-1. Frequency Synthesizer Implementation

The three VCO's are selectable to divide up the range. The first prescaler divides the output of the buffer by three which ranges from 84 to 144 MHz. The second prescaler is an emitter coupled logic divider, to divide the output down to the range of 4.2 to 7.2 MHz. This range is well within that of MSI program dividers. The output is phase-locked to the 100 kHz reference oscillator through the feedback signal processed by the amplifier and lag filter.

The synthesizer will produce an output frequency of 252 to 432 MHz which implies that the IF must be 48 MHz rather than 50 MHz. This is the condition imposed with this form of synthesizer; i.e., that the output frequency be a multiple of the channel spacing.

A possible approach for implementing technique 2 (shown in figure 9.3.2-2), would be to use a set of three multiplier chains each driven by a set of 10 oscillators. Crystal oscillators are now manufactured in the 20 MHz region in TO-5 cans which produce a sine or square-wave output of a 30 ppm temperature characteristic from -55°C to +105°C. It would not seem unreasonable to expect square-wave oscillators up to 50 MHz to become available. The third harmonic would then be prominent with the second and fourth harmonic suppressed by square wave action and additional filtering. It is anticipated that the worst-case filtering requirements would be that of a four-pole, 0.3 dB ripple, Chebishev bandpass filter which would reduce the fourth order harmonic by an additional 40 dB and the second order harmonic by an additional 54 dB. If the duty cycle of the square wave is held to 50% ±10%, then the total rejection would be greater than 70 dB. The second tripler should be designed to provide the greatest even-order suppression and the requirements on the following filter would then be based upon its performance. In any case, it should not be necessary to use any filter of a higher order than that of a 0.1 dB, 5-pole Chebishev bandpass filter.

In view of the comparatively small number of channels to be generated (approximately 30) and the inherent partial redundancy of the individual crystal oscillators, it is recommended that it be implemented. A failure in any chain will still allow the use of a local oscillator on other channels. This freedom is not available in the indirect digital frequency synthesis approach described for technique 1. For these reasons, the development of a common UHF local oscillator source for both modulator and demodulator appears to be justified.

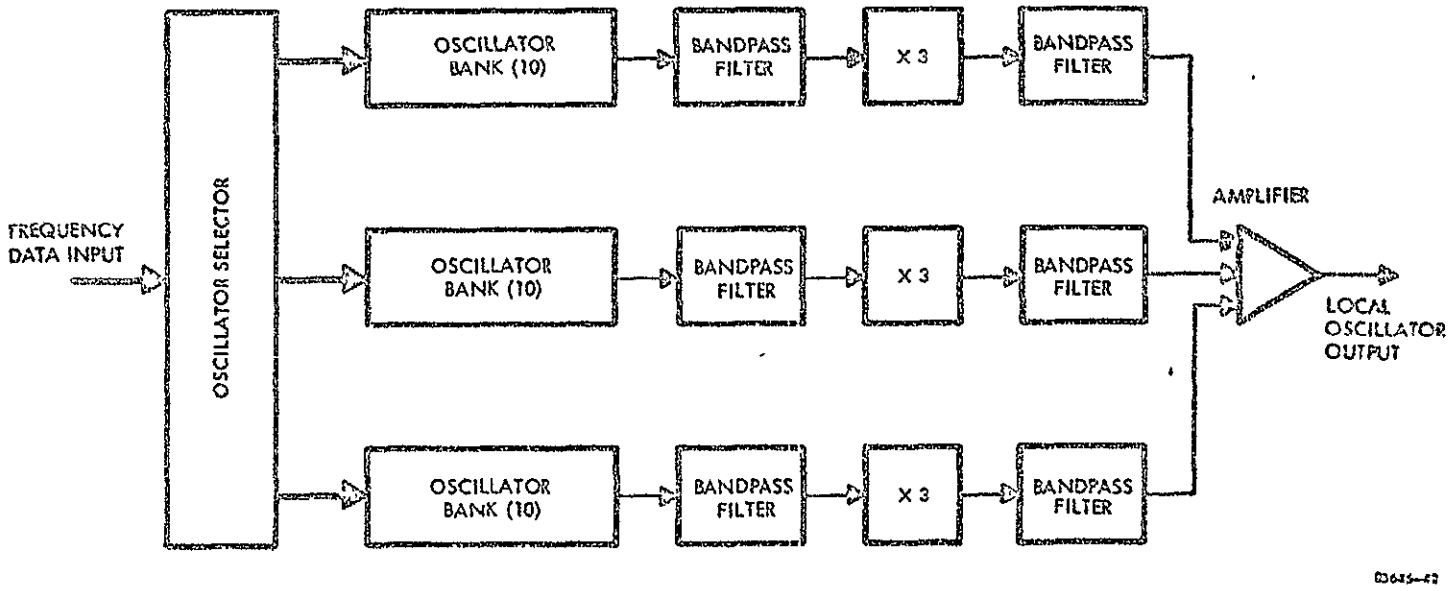


Figure 9.3.2-2. Crystal Oscillator Implementation

9.3.3 IF Amplifier and Video Detection Techniques

The IF Amplifier becomes a critical area of design, in that it is in these gain stages that most of the gain necessary for demodulation, along with amplitude response and delay equalization, are incorporated. These stages must amplify the incoming video or PAM/digital signals with as little distortion as possible. Furthermore, this means that this performance should be maintained for variable incoming signal strengths and under Space Base environmental conditions. Maintaining a constant IF selectivity characteristic over variable signal strengths and a constant signal level at the video detector input by means of automatic gain control circuitry is a difficult design task.

Achieving this performance using integrated circuit components, while minimizing discrete components from the design (especially the use of variable reactive tuning elements to create the desired bandpass response), represents a significant design challenge. However, it is important to note, that at least two major semiconductor manufacturers have been pursuing these problems and using separate techniques, namely monolithic and thick film. The monolithic amplifiers use discrete interstage coupling and tuning networks to achieve 75 dB gain with an AGC range in excess of 60 dB. The thick film approach has emphasized techniques of using specially developed thick film compatible reactive elements that are fix tuned, using air abrasive processing techniques to adjust values of inductors and capacitors and provide necessary frequency control. In both cases, the miniaturization of IF amplifiers suitable for wideband video applications has been demonstrated. The SMDS IF amplifier development problem is that of adapting present technology to the specific requirements of the SMDS demodulator. It is important to note also, that the SMDS does not use simultaneous FM sound transmission in the video channel which will significantly ease the IF amplifier selectivity requirements and resultant delay equalization problems.

The successful demodulation of the transmitted VSB modulated signal, whether the modulating signal was a composite video signal or PAM/digital signal, poses a signal processing compatibility problem of the same nature as that described for the Modulator Group in Section 8.0. Although the demodulator compatibility problems are considered nearly as challenging as those for a modulator, the major considerations are discussed below.

One area requiring attention is the method of implementing automatic gain control in the demodulator. This circuitry compensates for changes in individual demodulator input signal amplitude resulting from signal level variations induced by other system losses and gain variations of associated SMDS equipment components. By this means, the peak-to-peak signal level at the output of the demodulator group is held constant for changes in the incoming UHF carrier levels. It is common practice to use some form of "keyed-AGC" in television receivers to sample the amplitude of incoming horizontal synchronizing pulses, which are transmitted at constant amplitude. This is done to compensate for noise spikes or rapid fading effects that occur when receiving an antenna radiated and received RF television signal. Since the SMDS is a totally "wired" system a "fast acting AGC" IF amplifier response is not required and the AGC implemented is needed only to compensate for relatively slow signal-level variations such as those which occur in changing from channel to channel or variations due to other long term amplifier gain drifts due to temperature, level equalization, or voltage variations. The required AGC amplifier bandwidth should be somewhere on the order of few hertzs so as not to respond to the longest time period durations of the amplitude modulated video waveform such as the 60 Hz vertical synchronizing pulses. The use of a keyed AGC system is not justified due to the high signal-to-noise ratio that will be maintained throughout the SMDS; therefore, a sophisticated AGC circuit is not required. This approach appears to be generally compatible with PAM, however, in both cases, the AGC must be slow enough to be "blind" to the desired amplitude modulated information.

Achieving proper baseband response in the VSB demodulator can be accomplished in a number of different ways.

a. The amplitude characteristic of the VSB signal can be shaped in the IF amplifier with the video detector and subsequent amplifiers having flat amplitude response. Phase delay equalization for conventional television receivers is achieved by predistortion of the envelope delay of the transmitted signal in such a manner as to compensate for the receiver IF bandpass induced delay distortion. This predistortion has no distinct advantage in the SMDS since there are approximately the same number of modulators and demodulators. This precorrection of demodulator delay distortion is considered to impose a

restriction on building block design interchangeability and inter-unit compatibility. Predistortion at the transmitter is not required if suitable delay equalization is incorporated in the IF amplifier interstage coupling circuits.

b. A second approach to demodulator design is to employ amplitude and envelope delay correction after detection with a flat IF amplifier bandpass characteristic.

c. More sophisticated techniques such as exalted carrier and synchronous detection are theoretically feasible for equalizing baseband response and avoiding quadrature distortion effects produced by envelope detection of the VSB signal.

The currently available wideband synchronous video detector, on a monolithic integrated circuit which was developed for television applications, indicates that improved performance over simple envelope detection can be realized by using this circuit in conjunction with a compatible monolithic integrated circuit IF amplifier. The increased sensitivity of this detector circuit can allow for a savings in IF amplifier power consumption since the amplifier operates at a lower overall gain.

The development of a totally integrated circuit IF amplifier/video detector combination using this technique, is anticipated by the television industry in the near future. A hybrid version of this circuitry would appear to have direct application in the SMDS Demodulator Group. This hybrid circuitry would include the necessary IF amplitude and envelope delay compensation to be compatible with the proposed SMDS Modulator Group discussed in section 8.0. The selection of a SMDS intermediate frequency in the vicinity of 50 MHz further supports this proposed solution since this bandwidth is in the near vicinity of current integrated circuit operating frequencies. The implementation of the IF amplifier/video detector combination must necessarily be determined by additional study of video PAM/digital signal compatibility.

9.3.4 Size, Weight, and Power Minimization

Study of possible hardware implementation methods for the SMDS Demodulator has shown that most circuitry can be realized using microcircuit techniques. The preselector filter could possibly be physically large unless the active microwave filter approach is taken. Due to the large number of demodulator groups required in the system, it is recommended that conversion of all circuitry to some type of hybrid microcircuits be a design goal.

Present television demodulators (performing equivalent functions of a SMDS Demodulator) designed for CATV service have the following size and weight characteristics:

Width:	19 inches
Height:	2.50 inches
Depth:	12 inches
Volume:	800 cubic inches
Weight:	10 pounds

It will be noted that this is the same size and weight quoted for a CATV modulator. The proposed SMDS Demodulator Group is considered to be somewhat more adaptable to miniaturization than the modulator; therefore, engineering estimates project a possible size of 3 by 4 by 5 inches and a weight of 2 pounds.

Power consumption of present CATV demodulators is on the order of 6 watts. For the same reasons cited under the modulator group power consumption discussion, this can be anticipated to drop to 4.0 watts as a conservative estimate.

9.3.5 Testing Techniques

The subject of testing the SMDS signal transmission performance was covered in considerable detail under Modulator Group Testing Techniques (see section 8.0). The ultimate performance of the demodulator unit can only be evaluated on an end-to-end basis when the performance of the modulator is known. It is recommended that the methods described earlier be applied to demodulator tests to access overall demodulator performance and assure that required performance tolerances are maintained. This will guarantee interunit compatibility and interchangeability.

9.4 MATHEMATICAL ANALYSIS OF DESIGN

A detailed analysis of the SMDS Demodulator Group design was limited to a spurious analysis to demonstrate the feasibility of the downconversion technique proposed. The results of this analysis are summarized below.

9.4.1 Spurious Analysis

In any consideration of signal conversion in the presence of undesirable signals, it is necessary to consider the possible mixing products which may arise.

In the case of the demodulator unit, the input level to the balanced mixer will determine the level of a spurious product. It is important however, to locate the spurious responses to ascertain the effect on the output. A computer program was utilized to construct a spur plot for several IF frequencies. A sample output of the program is shown in figure 7.3.1.3 and includes a tutorial of the operation of the program. Basically, the program produces information to construct the graphs shown in figures 9.4.1-1, -2, and -3, which represent spurious responses for 40, 50, and 60 MHz IF center frequencies, respectively.

Examination of the graphs show a trade-off problem between the even ordered terms and the odd ordered terms as a function of frequency F(RF), while the odd ordered terms approach F(RF).

At this point, it is necessary to examine the effect of the balanced mixer on the orders of responses thus found. From a set of specifications for a double-balanced mixer with a RF drive level of -10 dBm and an LO drive level of greater than +5 dBm.

9.4.2 Explanation of Spur Chart Computer Program

Spurious responses in a mixer are found by testing each value M and N in the basic equation: F(IF) = M x F (LO) +N x F(X); where, F(IF) is a fixed IF center frequency, F(LO) is the local oscillator and, F(X) is the frequency of the spur.

The value F(X) is fixed to be within the range: F(RF) -FB $\leq$F(X) $\leq$F(RF) +FB; where, FB is selected to be wider than one-half of the worst-case RF preselection filter bandwidth. Thus, any signal which can pass through the preselection must be contained within the interval -FB to +FB about the center frequency F(RF), if one expects to get the maximum amount of information.

Since most downconversion applications in receivers require that the received frequency F(RF), be tunable across some band, the additional equation F(IF) = $\left[F(RF) - F(LO)\right]$ is used. For example, F(IF) = $\left[F(RF) - F(LO)\right]$ is used for low side injection. The value of F(IF) will be held constant.

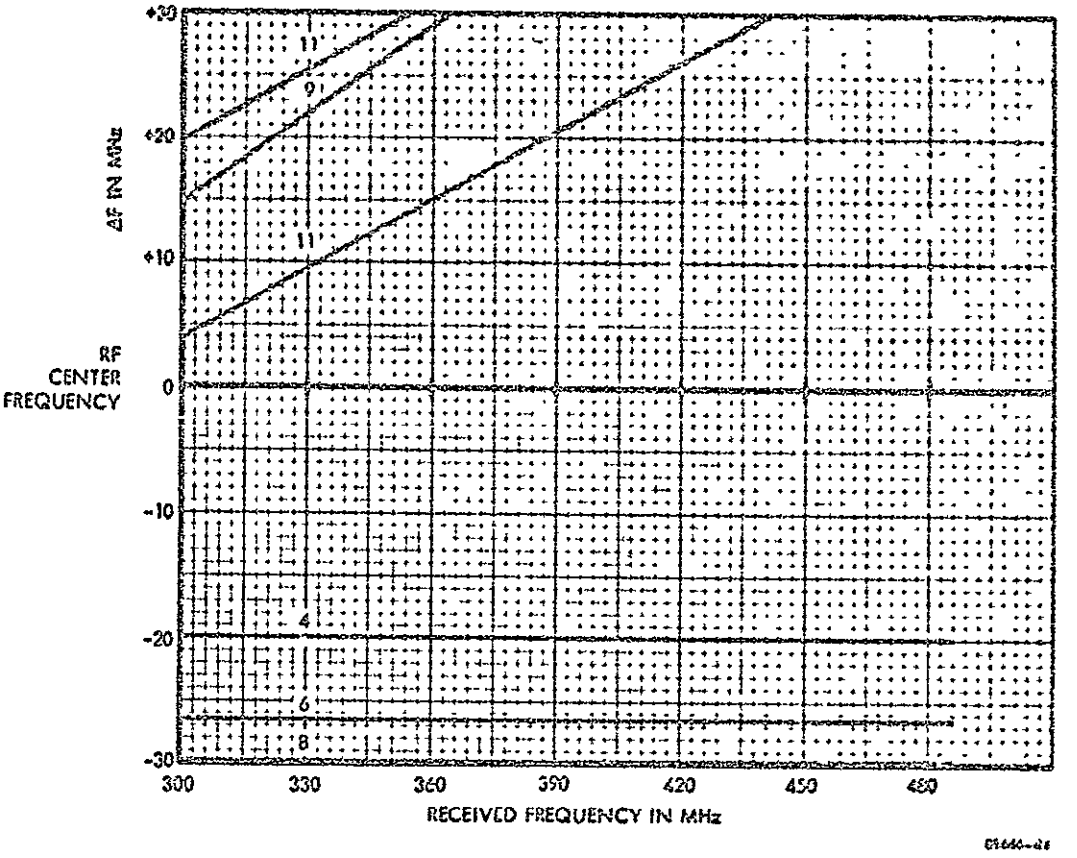


Figure 9.4.1-1. Spurious Response — F(IF) = 40 MHz

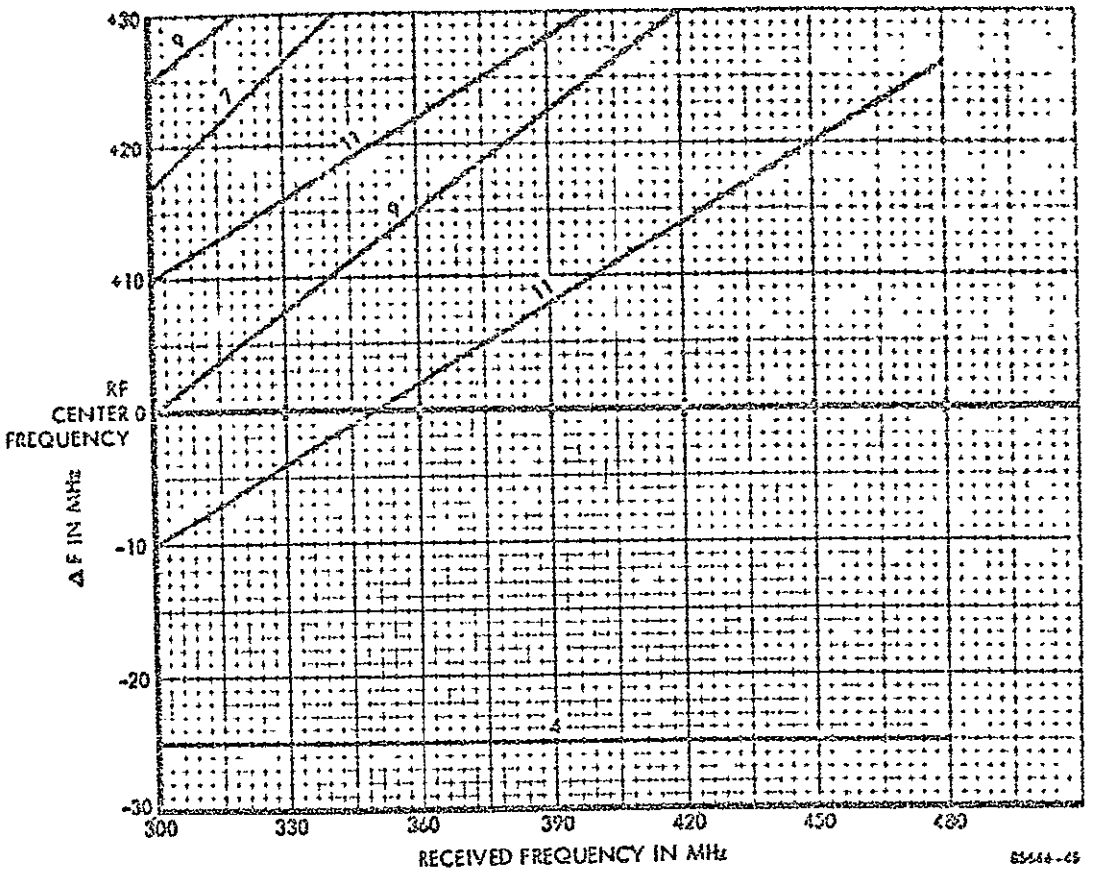


Figure 9.4.1-2. Spurious Response — F(IF) = 50 MHz

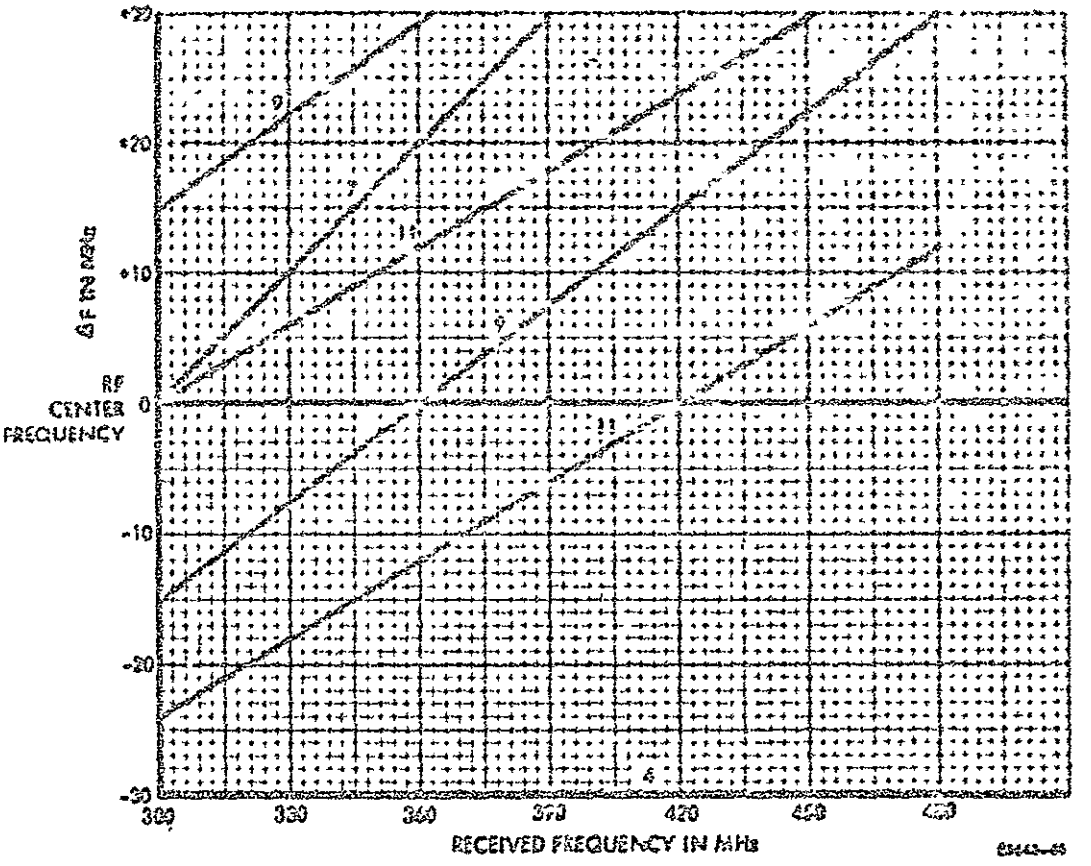


Figure 9.4.1-3. Spurious Response — F(IF) = 60 MHz

IF $\Delta F = F(X) - F(RF)$, then the equations for F(X) and F(LO) can be substituted to give: $\Delta F = -F(RF) + F(IF)/N - M/N \left[F(RF) - F(IF)\right]$ or $\Delta F = F(IF) \left[(1+M)/N\right] - F(RF) \left[(M+N)/N\right]$.

If the values for M and N are known and F(IF) is constant, the equation becomes that of a line where the slope is $-(M+N)/N$. A graph can be plotted with each line representing a given spur. The end points of each line are the values for ΔF at the band limits F(RF) (1) and F(RF) (2). As an example, suppose it is desired to find the spurs encountered for a receiver which can be tuned from 300 to 480 MHz and has a 50 MHz IF frequency. We can look in a ± 30 MHz strip about the received frequency and note that if the receiver is tuned to 300 MHz, that a signal at 316.667 MHz will produce a seventh order product in the IF passband. Notice also that a signal 25 MHz below the received signal will always produce a fourth-order product. The magnitudes of the spur products for two commercially available mixers are given in table 9.4.2.

Table 9.4.2. Magnitudes of Spur Products

Spur Order	Factor		Mixer Type	
	RF	LO	Relcom M1	Relcom M1E
4	2	-2	74	75
6	3	-3	50	>90
7	-3	4	77	>90
8	4	-4	88	>90
9	-4	5	85	>90
11	-5	6	>90	>90
11	5	-6	>90	>90
Product in dB below F(RF)				

Minimum allowable magnitude to meet specification is -50 dB. Note that the Relcom type M1 has almost equal degradation for the fourth and seventh order, whereas the M1E has marked improvement at orders 6 and above. It would not be advisable to select an IF freauency based upon the spurious analysis except to state, that below 40 MHz the even ordered responses approach too closely to the RF center frequency, and above 60 MHz the odd order responses will become severe.

Based upon the data at this point, one would conclude that a single-pole tank with a loaded Q of at least 40 should provide sufficient selection. This would amount to about 10 dB reduction to fourth order and 15 dB reduction to the sixth order product.

It should be mentioned that the signal levels given will be degraded by a few dB. However, at the higher frequencies the degradation can be compensated by a reduction in input signal level into the RF input of the mixer. The final selection of a local oscillator drive should be based upon the actual performance of the mixer.

The pretune network need not be of sophisticated design, the loaded Q should be greater than 40 which would require an unloaded Q of several hundred. Unloaded Q's of lumped element varactor tuned tanks in this region, are definitely feasible.

9.5 THEORETICAL PERFORMANCE OF DESIGN

The theoretical performance of the Demodulator Group and all other SMDS system subcomponents are more appropriately discussed under the classification of overall system theoretical performance and will not be discussed at this equipment level.

9.6 EXPERIMENTAL PERFORMANCE OF DESIGN

No actual experiments were performed as part of this study. However, much of the experimental work performed by the television industry is referenced throughout the study.

9.7 TRADE-OFFS

The trade-offs made in arriving at the recommended SMDS Demodulator Group design are included as part of section 9.3, covering demodulator design problem resolutions and are not to be repeated here.

9.8 SUMMARY

The SMDS Demodulator Group design should generally use current state-of-the-art television demodulator circuit design techniques to develop workable breadboard units that are functionally compatible and meet specified system performance requirements for all telecommunications systems operating modes; i.e., television, PAM audio, and bilevel digital data. Specific attention must be given to this interface compatibility to meet the design goals of maximum

equipment modularity and commonality. This equipment breadboard and system feasibility phase of the SMDS Modulator and Demodulator subunits could conceivably rely heavily on rapidly developing technology of equipments used for CATV systems. In addition to more detailed paper analysis of the system design, the modification of commercial equipment to meet specific SMDS applications would minimize the developmental costs associated with proving system feasibility. It is emphasized, that the final system feasibility can only be demonstrated by the construction of an actual breadboard system. This should be done prior to what might be considered the second phase of SMDS Modulator and Demodulator development; i.e., subunit size, weight, and power consumption minimization. The development of hybrid microcircuits and performance requirements will necessarily be dictated by the results of feasibility system testing.

In summary, specific areas identified as a result of this study, which will require further study of recommended techniques prior to hardware implementation, are:

1) Television/FAM Audio/Bilevel Digital Signal Processing Compatibility

2) VSB Filtering and Delay Equalization Circuit Implementation

3) Local Oscillator Synthesizer Implementation

4) UHF Voltage Tunable Filter Implementation

9.9 SCHEMATICS AND DRAWINGS DEVELOPED

The drawings relating to the Demodulator Group appear in section 4.2.5.3, volume I, of this report.

9.10 DEVELOPMENT SPECIFICATION

The following development specification is provided as a part of this section:

SMDS Demodulator Group

SMDS DEMODULATOR GROUP

DEVELOPMENT SPECIFICATION

1.0 SCOPE

This specification describes the development design goals and major performance specifications of a SMDS functional building block identified as a Demodulator Group.

2.0 APPLICABLE DOCUMENTS

The guidelines, trade-offs, and functional descriptions included as part of the SMDS Final Report shall be considered as part of this subunit specification. References cited in the Final Report shall be used for developmental guidance.

3.0 ELECTRICAL PERFORMANCE

The SMDS Demodulator Group shall accept and demodulate a UHF vestigial sideband amplitude modulated, telecommunications signal which has been originated by any SMDS Modulator Group. The Demodulator Group shall receive the modulated UHF signal via the Space Base SMDS wideband UHF distribution equipment (Base Level/ Deck Level Interface Unit, Pilot and Terminal Modem, Lines, and Couplers). Depending upon the operating channel to which the demodulator has been tuned, the output of the unit shall be a baseband composite color television, PAM audio, or digital bilevel information signal as the particular operating mode or application may require.

3.1 Input Signal Cnaracteristics

The Demodulator Group shall provide the specified performance for input signals having the following characteristics:

3.1.1 Input Frequency Range

The Demodulator Group shall be capable of specified operation on any of 30 separate discrete receive frequencies in the approximate range of 300 to 500 MHz.

3.1.2 Receive Channel Selection

Demodulator Group receive channels shall be selected by a channel selector switch easily accessible to Space Base personnel. Channel selection shall be accomplished by a set of thumbwheel or pushbutton switches (or equivalent) and shall be accompanied by an appropriate channel indicator which displays the channel to which the unit is tuned. The selector switches shall preferably activate or switch DC bias control voltages so as to allow for remote tuning capability of the demodulator.

3.1.3 Receive Channel Characteristics

The 300 to 480 MHz bandwidth shall consist of 30 separate 6 MHz wide vestigial sideband (AM) modulated RF channels. These channels shall contain composite color television, PAM audio, or bilevel digital information signals. The information bandwidth of these signals shall not exceed 4.5 MHz.

3.2 Receive Channel Tuning Time

The demodulator shall be capable of specified operation on any of the 30 SMDS frequency channels within 5 seconds after channel selection.

3.3 Spurious Responses and Image Rejection

The demodulator shall incorporate suitable voltage-tunable UHF preselection filter and downconversion mixer of such design as to ensure that spurious signals, including image signals, appearing in the intermediate amplifier passband as a result of 30 modulated carriers in the 300 to 500 MHz spectrum are a minimum of 60 dB below the peak desired received signal when measured at the input to the demodulator second detector. The actual preselector filter requirements must be determined on the basis of demodulator mixer performance and design commonality considerations. A design goal of the preselector filter implementation shall be to make its performance characteristics compatible with SMDS Modulator and Main Line Amplifier UHF filtering requirements for application in these units.

3.4 Local Oscillator and Spurious Signal Leakage

The design shall ensure that the level of the internally generated local oscillator and any other spurious signals appearing at the demodulator UHF input port in the 300 to 500 MHz range are 60 dB below normal input signal levels.

3.5 Local Oscillator Stability and Accuracy

The demodulator local oscillator shall exhibit an overall stability and accuracy of ±0.003% over the operating temperature range.

3.6 Input Impedance Characteristics

The demodulator shall exhibit an input impedance of 50 ohms with a maximum input VSWR of 1.5 to 1.

3.7 Noise Figure

The demodulator input noise figure shall not exceed 10 dB over the operating temperature range and frequency band with a design goal of 6 dB.

3.8 Adjacent Carrier Rejection

The demodulator response to adjacent carriers 6 MHz on either side of the desired signal shall be suppressed a minimum of 60 dB below the desired peak signal level.

3.9 Input Signal Dynamic Range

The demodulator shall accept signal levels from -55 to -25 dBm minimum for a minimum automatic gain control (AGC) range of 30 dB. The video output level shall not vary more than +1 dB for an RF input level change over these specified ranges.

3.10 Intermediate Frequency Rejection

The demodulator shall exhibit a radiated and conducted intermediate frequency rejection of 80 dB minimum.

3.11 Vestigial Sideband Amplitude and Delay Compensation

The demodulator shall incorporate appropriate VSB and envelope compensation compatible with SMDS Modulator Group characteristics necessary to meet specified system requirements for recovery of VSB amplitude modulated television, PAM, and bilevel digital data signals. For conventional NTSC,VSB, the demodulator IF passband shall exhibit a flat amplitude response within ±1.0 dB from 0.75 to 4.2 MHz above the UHF carrier with the IF response suppressing the IF carrier to 50% of the nominal flat amplitude level. Demodulator Group envelope delay shall be compensated to be within ±20 nanoseconds of an absolute delay of 200 nanoseconds across the frequency band of .010 to 4.20 MHz when measured using standard RF to baseband envelope delay measuring equipmont.

3.12 Sensitivity

The sensitivity of the demodulator shall be such that any signal with a predetection C/N (carrier-to-noise) ratio in the range of 30 to 60 dB, is not degraded by more than 3 dB when measured at the demodulator video output terminals on the basis of post-detection signal-to-noise ratio.

3.13 Differential Gain and Phase

The demodulator differential gain and phase shall not exceed 1 dB and 2 degrees, respectively, for modulation depths ranging from 10% to 90%.

3.14 Tilt and Sag

Demodulator low frequency tilt and sag for a 60 Hz square wave shall be 1% maximum.

3.15 Output Signal Characteristics

The demodulator output shall be 1.0 ±0.1 volt peak-to-peak for a 90% modulated input signal for frequencies from 40 Hz to 8.2 MHz. The rise and fall times of demodulated pulse modulated carriers shall not exceed 100 nanoseconds.

3.16 Video Output Impedance

The demodulator output impedance shall be 124 ohms balanced with a maximum VSWR of 1.5.

3.17 Internal Fault Detection Provisions

The demodulator group shall be designed to include built-in fault detection circuitry with an appropriate indicator signal to indicate abnormal operation or unit failure by monitoring key DC power and signal levels within the unit.

3.18 Power Supply Requirements

The demodulator group shall accept a maximum of two dual polarity DC input voltages with a maximum level of 30 volts. Total input power shall not exceed 6 watts with a design goal of 4 watts.

Power supply overloads, due to demodulator group circuit faults, shall be protected against by suitable overload and surge protection.

3.19 Size and Weight Requirements

The demodulator group shall have a maximum weight of 4 pounds with a design goal of 2 pounds. Unit volume shall not exceed 100 cubic inches with a design goal of 60 cubic inches.

3.20 Miscellaneous Design Guidelines

Demodulator group development specifications must be considered flexible in terms of developing a totally integrated SADS design. Trade-offs not considered or recognized as problems in this study may require deviations from specifications stipulated above.

SECTION 10.0

SMDS CENTRAL TELEPHONE ELECTRONICS

10.0 SMDS CENTRAL TELEPHONE ELECTRONICS

10.1 ACCOMPLISHMENTS

The objectives of a study and conceptual design of an appropriate telephone system for the Space Base was accomplished. The functional requirements of 75 telephone stations was implemented. This implementation uses 36 full duplex channels to interconnect Space Base's 75 phones with each other as well as the 24 channels for ground conversation.

Time division multiplexing and pulse amplitude modulation was the techniques employed to yield the minimum complexity in the telephone system from both a circuit and a wiring complexity viewpoint. Still the Space Base telephone system enjoys the likeness of the commercial telephone systems in that it interfaces readily with external telephone equipment such as the handset and dialer.

The telephone system is not limited to 75 telephones either as a minimum or as a maximum since the system is limited by the number of crewmen and their usage of the phone system. Therefore, additional telephones can be added with no degradation to the system.

10.2 PROBLEMS

Of several problem areas uncovered in the study of the telephone system, the major problems are discussed here and in the resolutions section.

10.2.1 Interchannel Interference

Interchannel interference or crosstalk is a potential problem in any multichannel communications system. In a TDM-PAM system the problem is not only related to the stray pickup (be it inductive or capacitive) but also the timing uncertainty. Cable delays, as well as circuit delays, become serious problems. Knowledgeable crosstalk, such as interchannel interference, has an acceptable threshold far below the tolerable threshold of noise since the ear listens to this other conversation occurring on the interfering channel. Noise can be quite high before interfering sufficiently with the conversation to make the communication link unacceptable. Thus, interchannel interference is potentially even a greater problem.

10.2.2 Flexibility

The problem of no flexibility or rather no expandibility becomes apparent with the assigned time slot scheme. The only way telephones could be added would be to add the same number of time slots. The problem of increasing the number of time slots is more of a problem than simply changing the timing to allow for more slots. The real problem is that the sample rate is fixed and increasing the number of telephones decreases the time slot width to a point of possibly nonrecovery of the data contained in the time slot.

10.2.3 Telephone Positioning

The placement of phones throughout the deck was also a problem since any additional cable results in the timing delay, which adds to the timing uncertainty. The most important consideration in obtaining a configuration for each deck is not that the telephone interconnection be made with the minimum length. Rather the telephone system should be such that any possible deck configuration could be serviced by the telephone system with no impact on the quality of the communication system.

10.3 RESOLUTIONS

10.3.1 Interchannel Interference

Interchannel interference was found to be possibly 37.1 dB below the channel reference. (This is if both the reference channel and the interfering channel are of the same level, which may not be the case; in fact, the interfering channel can be at a level above the reference channel in which case there would be even more interference.) This is true for certain conditions such as a limit of a 1 MHz pole due to the transmission line, of a sample and hold amplifier with a gain bandwidth product in the order of 20 MHz, and of a sample and hold charging time constant of 300 nanoseconds. Since this problem is due to time slots actually overlapping because of the line delays, two solutions could possibly resolve the problem. The first would be to reduce the delays, preferably to zero, but this would force the location of each telephone to be as close to the main bus interface box as possible. This relates to another problem pointed out above. The second approach would be to reduce the sample time so that the time "data" carrying width of each time slot is sampled. Thus, any overlap that would occur in

not used on the hold by operation and no interference would be detected. This approach also has disadvantages in that the recovery time is reduced, possibly by twice the expected delay uncertainty. The solution selected actually employed both solutions. The telephone permanency problem was overcome as described in section 10.3.2.

10.3.2 Flexibility

The flexibility problem associated with the preassigned time slot scheme was resolved by implementing a nonassigned scheme that requires a vacant time slot pair to be found by the telephone initiating the call. Instead of a telephone always having a talk time slot preassigned and the listen slot variable to any slot commend by the particular call, both the talk and listen time slots are varied from call to call depending upon which channels of the 30 two-way channels or time slot pairs are in use. This adds some complexity to the telephone, but more telephones can be serviced with fewer time slots with this approach. The flexibility of accepting additional phones is also obtained with this approach.

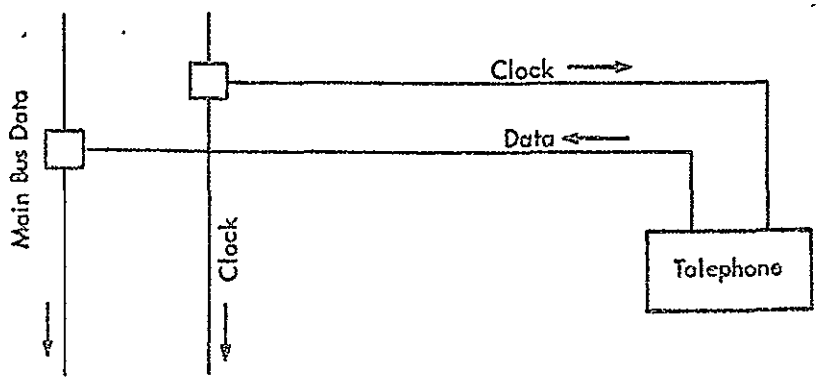
10.3.3 Telephone Positioning

The positioning of the telephones throughout the deck should be subject to change without any impact to the quality of the telephone services. This became a problem when considering the timing delays resulting from the added length of transmission line. This problem is only common to the "party line" system; that is, a system in which no switchboard is used but rather a system in which any single telephone can communicate with any other telephone in the system and over a single transmission line. The transmission line is shared by all the telephones within the system and thus the name of the "party line." The switchboard resolution produced other problems, namely increased complexity in a vital area. Should the switchboard fail, the whole system would fail. Instead, the positioning problem was resolved by splitting the telephone into two portions. The remote portion of the telephone would be placed anywhere on the deck and the central portion would be placed in the vicinity of the modem that links the deck with the main bus, and thus the rest of the Space Base. The central telephone will contain the majority of the electronics needed to complete the capability that each telephone has to communicate with any other telephone. The remote telephone will contain just enough electronics to make the interference between the central portion and the remote portion, with as few wires as possible and still accept the inputs of the commercial-like telephone equipment, such as the dialer and

handset. To reduce the number of duplicate circuits in each central telephone, five central telephones are grouped together into a single package with just one set of interface lines with the modem. This grouping reduces the number of transmission line drivers, transmission line receivers, and clock countdown circuits from five to one on decks where five telephones are needed, a second central telephone electronics group will be added. It should also be noted, that the reduction in line length from the central telephone to the modem reduces the timing uncertainty related to the interchannel interference and reduces the amount of twisted-shielded pairs required to connect all the telephones.

10.4 MATHEMATICAL ANALYSIS OF DESIGN

Interchannel interference or crosstalk between adjacent channels comes primarily from data overlap in a TDM-PAM system. The overlap in this system comes from the inability to "write" the data with no delay. The delay from the cable connection alone is approximately 1.5 nanoseconds-per-foot of cable. Examining the deck layout of a noncentralized telephone system yields a possibility of 125 feet of cable or 375 nanoseconds of delay. The scheme is shown below, and it can be seen the telephone receives a clock delayed 187.5 nanoseconds from the clock conducted down the main bus. Even if the data and clock are perfectly synchronized at the telephone, the data will be delayed another 187.5 nanoseconds in getting back to the main bus. Thus, the data from that telephone is delayed a total of 375 nanoseconds at the main bus.



Receiving the data in a 300 nanosecond time constant sample and hold circuit with a 1560 nanosecond time slot width yields:

$$V_{out}(t) = V_1\left(1 - e^{-\frac{t}{\tau_s}}\right) + V_2\left(1 - e^{-\frac{t-T_D}{\tau_s}}\right)$$

where:

V_{out} is the sample and hold output

τ_s is the sample and hold time constant

V_1 is the overlap voltage

V_2 is the desired voltage contained in the sampled time slot

The amount of overlap voltage then present at the end of the sample is:

$$V_1\left(e^{\frac{T_D}{\tau_s}} - 1\right) e^{-\frac{T_s}{\tau_s}}$$

The residue is

$$= V_1\left(e^{\frac{375}{300}} - 1\right) e^{-\frac{1560}{300}} = 0.0139\ V_1$$

or the residue is down 37.1 dB from the original V_1 level.

The whole idea of TDM-PAM rests on the assumption that the pulse amplitudes can be received and stored accurately. The problem of reception for the 1560 nanosecond wide pulses is analyzed below and shows the assumption is valid.

Let us approximate the attenuation of the transmission media, both the line and the modem, by a single order 1 MHz pole. Also the receiving amplifier is assumed to have a gain bandwidth product of 20 MHz, and the time constant associated with the sample and hold circuit is placed at 300 nanoseconds. Thus,

$$V_{out}(s) = \frac{1}{s}\left[\frac{W_l}{s + W_L}\right]\left[\frac{G\,W_A}{s + W_A}\right]\left[\frac{W_s}{s + W_s}\right] V_{in}(s)$$

where:

V_{in} is the applied voltage

G is the gain of the receiving amplifier

W_A is the receiving amplifier bandwidth

W_L is the line pole

W_s is the sample and hold pole

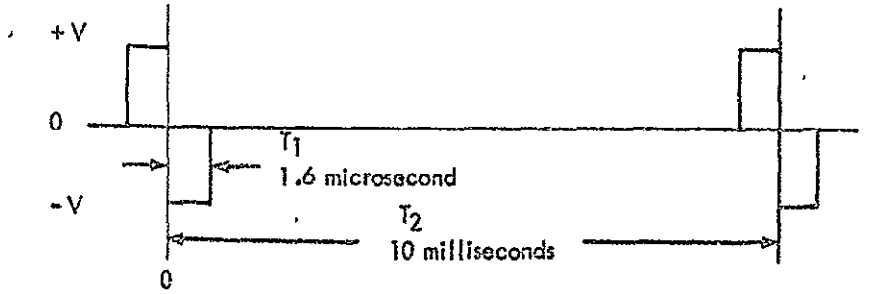
V_{out} is the voltage at the output of the sample and hold

Taking the inverse Laplace transform of the previous equation and solving at t = 1560 nanoseconds and allowing G to be approximately 4, yields:

$$V_{out}\ (1560\ ns) = [1 + .0000733 - 0 - .013]\ G\ V_{in} = (1 - .013)\ G\ V_{in}$$

thus only 1.3% is not recovered by the sample and hold. This should present no problem in degrading the fidelity of the audio data.

Pulses are inserted at major frame intervals in all time slots which are in use. These "in use" pulses allow the system to recognize the "in use" slots when no audio is present. These pulses would prefer to be inaudible with the fundamental frequency below the audio bandwidth of the telephone system. The Fourier analysis of an in-use pulse occurring every 10 milliseconds is shown below.



$$V(t) = \frac{2V}{\pi} \sum_{k=1}^{\infty} \frac{1}{k} \left(\text{Cos } 2\pi k \frac{T_1}{T_2} - 1\right) \left(\text{Sin } 2\pi k \frac{t}{T_2}\right)$$

Since $\frac{T_1}{T_2} = 1.6 \times 10^{-4}$ the cosine may be approximated by the first two terms of its series expansion. The amplitude coefficients for the various harmonics become:

$$A_k = 8\pi k \left(\frac{T_1}{T_2}\right)^2 V = 6.44 \times 10^{-7} \text{ kV}$$

$$A_3 = 19.3 \times 10^{-7} V \text{ or } 114 \text{ dB below V (300 Hz)}$$

$$A10 = 64.4 \times 10^{-7} V \text{ or } 103 \text{ dB below V (1000 Hz)}$$

$$A_{30} = 193.2 \times 10^{-7} V \text{ or } 94 \text{ dB below V (3000 Hz)}$$

These calculations show that for k = 30 the signal is 94 dB below V, thus, the 30th harmonic or the 3000 Hz component is 94 dB below the pulse reference. Therefore, the in-use pulses should not produce tones in the audio band loud enough to interfere with the conversation.

10.5 THEORETICAL PERFORMANCE OF DESIGN

The Space Base telephone system uses an amplitude modulated RF carrier to complete the communication link from deck-to-deck. The time division multiplexed data from the telephones on each deck are used to modulate the RF carrier, with the frequency of this carrier assigned for telephone communication only. The telephone RF carrier is demodulated on each deck to form the time division multiplexed pulse amplitude modulated waveform, that is received by each of the telephones on that particular deck. Thus, each deck has a PAM data line that is used to drive a modulator (the Write PAM line) and each deck has a PAM data line that is the output of the deck demodulator (the Read PAM). The Write PAM contains only the data entered by the telephones on that deck while the Read PAM contains the summed data, or rather the data written by all the telephones on all the decks. The delays resulting from the deck-to-deck transmission of the data are overcome by the technique of also transmitting a clock from deck-to-deck. This causes somewhat of an internal timing problem since there are two clock signals, Write and Read, for each telephone. However, this problem is not of the same magnitude as the ones encountered in using a single clock signal to perform both the writing and the reading function.

Each telephone can communicate with any other telephone via the deck-to-deck RF link. This eliminates the need for a switchboard since all of the telephones are common to the time division multiplexed data stream. The only centralized signal needed by the telephones is the clock. No other centralized processor, such as a switchboard, is necessary.

To multiplex all the telephone outputs into one data stream, sampling techniques had to be employed. A sample rate of at least 8000 samples-per-second is needed to accurately recover the audio data within the bandwidth of the telephone system. Due to the nature of the audio (primarily voice information), a bandwidth of 250 to 2000 Hz should be sufficient to pass the data. A multipole maximally flat or Butterworth filter that limits the high end of the bandwidth at 2000 Hz is required before sampling and the writing of the data on the Write PAM line, and a multipole Butterworth filter is necessary for interpolation of the sampled data from the Read PAM line. The cut-off frequency of the interpolation filter should be about 3200 Hz for ideal recovery of the audio, if both the presampling filter and the interpolation filter are third order and the audio data also contains a pole at roughly 2000 Hz.

The PAM data streams also contain digital information as well as sampled audio. The digital information, besides the ring command and in-use-pulses, are basically confined to just two channels of the data stream. The data stream has a frame rate equal to the sample rate of 8421 Hz. Each frame contains 76 time slots with a width of 1.5625 microseconds. To arrive at the concept of a channel, two time slots are grouped together. Thus each frame has 38 channels or 38 time slot pairs. As part of the implementation study it was found the 75 telephones on the Space Base and 24 ground link telephones could be serviced adequately with 36 two-way channels. The other two channels are for conveying dialing information to all telephones and for priority calls. The dialing channel is used to transmit the telephone numbers and the time slots assigned for this particular call from the telephone initiating the call to all the other telephones. The telephone or telephones being called will recognize its own identification number and thus use the assigned time slot to write the audio samples in and the time slots assigned to the other telephone or telephones will be sampled from the Read PAM line for recovery of the audio. The priority channel can be activated by a priority device that can be installed in each telephone. The telephone initiating the priority call inserts the telephone number of the telephone being called in the priority time slot pair instead of in the dialing time slot pair as other calls are made.

The telephone being called recognizes its identification number in the priority channel and interrupts the present call, if the called telephone is engaged in a conversation at the time; if not in use the called telephone rings. The time slots used for the priority call are the priority time slot pairs.

The telephone initiating the call, after dialing is completed, must first make sure no other telephone is using the dialing time slot pair. After finding the dialing time slot free, the telephone must then find enough of the 72 possible time slots to completely facilitate the call just dialed before any information can be written in the dialing time slot pair. The telephone being called will recognize its own identification number and thus use the proper time slot that was found by the calling telephone, and assigned as the talk time slot of the called telephone. The other assigned time slots involved in this call are decommutated by the called telephone as listen time slots.

10.6 EXPERIMENTAL PERFORMANCE OF DESIGN

No direct experiments were performed on the design concepts. However, this field of aerospace communications is not new to the designers, and past knowledge obtained empirically and through analysis was used in reaching the concertual design.

10.7 TRADE-OFFS

The trades performed in this study were:

a. Hardware Implementation

b. Remote Electronics/Central Electronics Interconnection

c. Implementation of Additional Telephone Functions

10.7.1 Hardware Implementation

A major trade-off was one complete telephone versus the remote telephone and central telephone, or a single telephone contained in one box versus a two box approach with the second box facilitating more than one telephone. The most important factor was the positioning of the complete telephones. Positioning is critical and location of the telephones on each

deck would probably be limited to positions close to the Base Level/Deck Level interface unit. By increasing the complexity somewhat and using the remote telephone-central telephone approach, the telephone position desired on any deck can be serviced with no degradation to the communication system.

10.7.2 Remote/Central Electronics Interconnection

The second trade was between the increased complexity of the remote telephone and central telephone versus the number of wires necessary to connect the two groups of electronics. Conveying the dialing information was the problem. If the dialer were to be connected directly to the central telephone, ten additional wires per telephone had to be added to complete the interface. However, by encoding the dialer information in the remote telephone and decoding the information in the central telephone the interface would only need one line. This line could also be the audio talk line so in effect no additional wires had to be added. The trade-off would then be the additional complexity of encoding and decoding the dialing data versus the additional wiring. The complexity is not that much extra, but on a deck with ten telephones the extra wire of a direct dialer to a central telephone scheme would result in 3700 feet of wire. Thus, the trade was made in favor of the added complexity but less wire.

10.7.3 Implementation of Additional Telephone Functions

The third trade-off involved the extra features or frills of the telephone system. In each case the tradeoff was between having the extra feature and its extra electronics versus a less complex system. In all the cases the decision was to make the telephone system as simple as possible and still maintain enough flexibility to adequately service the communication needs of the Space Base. The features omitted were the capability of increasing the conference call by any telephone involved in the call, the capability of a priority call joining in on a conference call, the conference call limited to a maximum of five telephones to one conference call, the search within a preassigned group for a not-in-use telephone should the number that was dialed be busy, the emergency override of the present conversation, and the off switch should an emergency condition be present. In the conference call all parties must be dialed by the party initiating the call. The priority call cannot join any call but only interrupt calls. Since there is only one priority channel, only one priority call can be made at any one time. Thus the time of a priority call should be limited so the priority capability is not tied up for a lengthly

conversation. The search within a preassigned group of numbers for a non-intercom telephone, is a luxury that can be replaced with a list of telephone numbers and another try at dialing. The emergency override of the telephone system would be a feature that could help in an emergency situation. However, other methods of emergency indications are superior to the use of the telephone override to attract attention. The intercom system provides one means of transmitting emergency audio instructions effectively. If other ways of broadcasting audio are necessary, then another emergency system is needed. The handset of a telephone does not work well as a loudspeaker. An ideal listening level when placed next to the ear is hardly audible a few feet away.

10.8 SUMMARY

The 75 telephone system conceptual design was concluded and only three major problems needed to be resolved in the area of the telephone. The problem of interchannel interference was resolved by eliminating the majority of the timing uncertainty by physically positioning the countdown and sampling circuitry closer to the main bus interface. This was accomplished by way of the remote telephone/central telephone configuration. Also the sampling time can be controlled so sampling of the time slot overlap is minimum. The lack of flexibility was overcome by using a non-preassigned time slot numbering scheme. The time slots used for a call must be found by the initiating telephone directly following the dialing of the call. Both the talk time slot and the listen time slot for each telephone are assigned at that time. The third problem, the problem of critical telephone positioning, was also solved by the remote telephone/central telephone implementation. As a result, the telephone can be arranged throughout the deck in any configuration with no degradation to the communication system.

10.9 SCHEMATICS AND DRAWINGS DEVELOPED

The drawings relating to the Central Telephone implementation appear in section 4.3.2, volume I, of this report.

10.10 DEVELOPMENT SPECIFICATIONS

The following development specifications are provided as a part of this section:

1. SMDS Central Telephone Electronics Module
2. SMDS Remote Telephone Electronics Subunit
3. SMDS Telephone Number Plug Subunit
4. SMDS Telephone Interface Specification

SMDS CENTRAL TELEPHONE ELECTRONICS

MODULE

DEVELOPMENT SPECIFICATION

1.0 SCOPE

This specification describes the development design goals and major performance specifications of a SMDS major module building block identified as the Central Telephone Electronics.

2.0 APPLICABLE DOCUMENTS

a. The guidelines, trade-offs, and functional descriptions included as part of the SMDS Final Report shall be considered as part of this module specification.

b. SMDS Remote Telephone Subunit Specification

c. SMDS Telephone Number Plug Subunit Specification

d. SMDS Telephone Interface Specifications

3.0 ELECTRICAL PERFORMANCE REQUIREMENTS

3.1 General Requirements

The Central Telephone Electronics processes the information of up to five remote telephones and multiplexes the information into a single output (the Write PAM) that drives the deck telephone modulator. The Central Telephone Electronics also accepts an output from the deck telephone demodulator (the Read PAM) and the pulse amplitude modulated data is decommutated and supplied to five remote telephones. Each remote telephone has four wire interface with the central telephone. Two lines are for supplying power and ground to the remote telephone and two lines are talk and listen interfaces with the remote telephone. The Base Level/Deck Interface unit (the telephone modulator/demodulator) will have a four twisted-shielded pair interface with the central telephone. Two are the Write PAM and the Read PAM and two are the Write Clock and the Read Clock. The central telephone also accepts up to five number plugs that identifies the telephone number of each of the five remote telephones.

3.2 Power Requirements

The Central Telephone Electronics shall not exceed more than 20 watts of power dissipation per telephone circuit from the following voltage supplied: +15 volts ±5%, -15 volts ±5%, +5 volts ±5%, and -5 volts ±5%. The total power consumed on all four lines shall not exceed 20 watts (20 watts is not allowed per supply line). This power does not include the 2 watts supplied to each remote telephone that is powered by the central telephone.

3.3 Input Requirements

3.3.1 Remote Telephone Inputs

The five remote telephone inputs shall each have a nominal input impedance of 600 ohms. The source impedance of each signal shall be less than 30 ohms. The central telephone shall recognize the different bias levels on the talk inputs. Bias greater than 1.50 volts shall indicate an off-the-hook condition; a bias less than -1.50 volts shall indicate a priority call condition; and a bias of 0.0 ±0.5 volts shall indicate an on-the-hook condition. Because of the other signals conducted on the talk line, the bias thresholds shall be +1.00 ±0.25 volts and -1.00 ±0.25 volts. Thus, any bias above 1.25 volts shall indicate an off-the-hook condition; any bias below -1.25 volts shall indicate a priority call condition; any bais from +0.75 to -0.75 volts shall indicate an on-the-hook condition. The central telephone shall also receive dialing information in the form of a Manchester code. The bit rate shall be 500 ± 100 bits-per-second and the peak-to-peak amplitude shall be 2.0 ± 0.5 volts. The data shall consist of four bit words in the 1-2-4-8 binary code of each decimal number dialed, with the most significant bit first. The audio data shall be processed from the talk input. The audio shall have a minimum bandwidth of 250 to 2000 Hz. Signals above 2000 Hz shall be eliminated by a maximally flat 3-pole presampling filter. The sampling of the audio rate shall be at least 8000 samples-per-second (8421 samples-per-second is a convenient rate, since the clock rate is 2.56 MHz and there are at least 38 channels of communication). The samples shall be transposed into a current sample such that the amplitude of the current sample is equal to the product of the analog input voltage amplitude and a transconductance factor of 2.0 milliamperes ±10% per volt of input signal.

3.3.2 Read and PAM Line Input

The Read PAM line input shall be decommutated for both analog amplitude audio samples and digital information. The Read PAM data shall contain at least 76 time slots to a frame, and the frame rate is equal to the audio sample rate. The telephone shall sample the correct time slot or slots and convert the audio samples into a continous audio signal with a gain of 2.0 volts ±10%, per-volt of input signal. The input impedance shall be greater than the 100 kilohms differential and 1.0 megohms common mode. The differential signal range shall be +1.0 to -1.0 volts and the common mode signal range shall be +2.0 to -2.0 volts. The digital information contained in the data stream could be "in-use" pulses, dialing information priority information, or the ring command.

3.3.3 Write Clock Input

The Write Clock input from the telephone write demodulator shall be differential signal with an amplitude of 0.5 to 1.5 volts peak-to-peak. The frequency of the clock is 2.56 MHz. The synchronization space, the absence of the two clock cycles, shall occur every 19,456 clock cycles. The input impedance shall be greater than 10,000 ohms differential and 10,000 ohms common mode. The common mode voltage

range shall be from -1.5 to +1.5 volts. The Read PAM data stream shall not be delayed with respect to the Read Clock by more than 200 nanoseconds.

3.3.4 Read Clock Input

The Read Clock input from this telephone read demodulator shall be a differential signal with an amplitude of 0.5 to 1.5 volts peak-to-peak. The frequency of the clock is 2.56 MHz. The synchronization space, the absence of two clock cycles, shall occur every 32,456 clock cycles. The input impedance shall be at least 10,000 ohms differential and 10,000 ohms common mode. The common mode voltage range shall be -1.5 to +1.5 volts.

3.3.5 Number Plug Inputs

The 12 programmable number plug inputs for each number plug, provides the binary code for the three decimal numbers that comprise the telephone number. The Central Telephone Electronics shall have 5 number plug slots. Each number plug slot shall have 12 digital inputs that are either connected to common or +5 volts through an impedance of less than 10 ohms. Additionally, each number plug slot shall have four inputs that connect the power lines to the particular telephone circuit assigned to that number plug slot. The impedance of the power jumpers shall be less than 50 milliohms. Four additional connections are required to supply the power that is connected to the central telephone circuit through the number plug.

3.4 Output Requirements

3.4.1 Write PAM Output

The Write PAM output shall supply a differential current into a 128 ohm twisted-shielded wire pair that shall be terminated at both ends with 128 ohms. The common mode load impedance shall be less than 100 ohms. The audio input appearing on the talk input shall be converted to a current with a transconductance factor of 2.0 milliamperes per volt, ±10%, when the audio signal is sampled. When the audio is not sampled, the transconductance shall be less than 0.2 microamperes per volt. The digital samples shall have an amplitude of +3.0 ±0.6 milliamperes for a digital "one" and -3.0 ±0.6 milliamperes for a digital "zero". The "zero" sample time varying current shall be less than 0.2 microamperes and the direct current offset current shall be less than 200 microamperes. The output admittance shall be less than 5.0 microamperes per volt.

The ring command shall be a series of four alternating bits, one-zero-one-zero.

The "in use" pulse shall be an alternating one-zero signal.

The Write PAM output shall be synchronized with the Write Clock with no time slot in the Write PAM data stream delayed or advanced more than 100 nanoseconds.

3.4.2 Talk Outputs

The output of each of the five telephone circuits, within the Central Telephone Electronics, shall drive a remote telephone load impedance of 600 ohms. The output impedance shall be less than 30 ohms. The voltage gain from the Read PAM line to the talk output shall be 2.0 ±10%.

The audio samples of the audio signal between 230 and 2000 Hz shall be reconstructed into an audio signal with a gain variation of less than 1.0 dB over the frequency range. The intermodulation product of the 8421 Hz sampling frequency and the audio frequency shall be at least 26 dB below the reconstructed audio level.

The ring tone shall have an amplitude of 2.0 ±0.5 volts peak-to-peak. The ring frequency shall be 1052.6 Hz scynchronized with the incoming Read Clock. The ring tone shall last 2.0 ±0.25 seconds followed by a no-tone period of 6.0 ±0.75 seconds before it is repeated. The waveform may either be sinusoidal or a square wave.

The audio clear tone shall have a peak-to-peak amplitude of 2.0 +0.5 volts. The frequency of the audio clear tone shall be 16,842 Hz synchronized with the Read Clock input. The waveform may be either square wave or sinusoidal. The audio clear tone shall last between 5 to 10 milliseconds.

A busy signal shall be an interrupted tone of 500 ±100 Hz, 1.0 ±0.25 volts peak-to-peak. The interruption shall be 4 to 7 times-per-second with the interruption time being equal to the uninterrupted time ±25%.

A priority signal shall be an interrupted tone of 1500 ±300 Hz. The amplitude shall be 1.0 ±0.25 volts peak-to-peak with the same interruption characteristics as the busy signal.

The dial tone shall have a frequency of 500 ±100 Hz. The amplitude shall be 1.0 ±0.25 volts peak-to-peak.

3.5 Operational Requirements

3.5.1 Data Stream

The PAM data stream contains 38 time slot pairs or channels. Four time slots are the dialing time slot pair and the priority time slot pair. The other 72 time slots are for 36 two-way communication channels used for the telephone calls. The repetition rate for this 72 time slot frame is equal to the sample rate of 8421 Hz. Every 64 frames or every 7.60 milliseconds, a clock reset occurs. The first frame of the major frame, the first frame following the clock reset shall be used for time slot usage indication. An "in-use' pulse shall be placed in every time slot that is being used, including the priority time slots and the dialing time slots, during the first frame of every major frame. The telephone that initiated the call

shall produce the "in use" pulses for all the telephones involved in the call.

3.5.2 Call Initiation

The initiating of a call starts with the bias on the talk line changing from 0 to +2 volts or -2 volts. A -2 volts bais indicates a priority call, and a +2 volt bias indicates a normal call. With the change in bias on the talk line, a dial tone is produced on the listen line until the bias returns to "zero" or the first bit of dial data is received on the talk line. The dialing data shall be the binary coded decimal numbers that identify the type of call being placed, followed by the telephone number or numbers wanted in the call.

The type of call will indicate the number of other telephones wanted in the call. The conference call capacity shall be five total phones. Thus, the maximum number that can appear in the "type-of-call" information is four.

When the dialing is completed, the Read PAM line shall be monitored for "in-use' pulses in the dialing time slot pair. If 'in-use' pulses appear, a busy signal shall be produced on the listen line. If no "in-use" pulses appear in the dialing time slots, then at the beginning of the next major frame, the telephone shall drive the Write PAM line with "in-use" pulses in the dialing time slots followed by the 12 binary bits contained in the number plug. The Read PAM line shall receive the number and compare it to the number in the number plug. If there is no comparison, a busy signal shall be produced on the listen line. If the numbers compare, the Read PAM line is monitored through the next major frame for vacant time slots. If there are not enough vacant time slots to process the call, a busy signal shall be produced on the listen line. If enough vacant time slots are found, then following the next series of "in-use' pulses, the following information shall be placed on the Write PAM line in the dialing time slots and in the following order.

a. The type of call being made.

b. The time slot assigned to the telephone initiating the call, as its talk time slot.

c. The telephone number of the telephone dialed followed by the time slot assigned as that telephone's talk time slot. If more than one telephone number is dialed, then the telephone number and its assigned talk time slot shall be placed on the Write PAM line in the dialing time slots, in the order in which the telephone numbers were dialed.

Following the dialing information transfer, the ring command shall be placed in the talk time slot of called telephone at the beginning of the major frame. If the call is a conference call, then the talk time slot of the first telephone dialed shall be activated with a ring command. The other telephones shall be sent a ring command

only after the bias changes on the talk input to 0 volt and then back to +2 volts.

The telephone shall receive a ring tone on the Read PAM line after a ring command is sent or a busy signal shall be produced on the listen line.

The talk input shall be sampled directly after ring command is produced on the Write PAM line; and these audio samples shall appear on the Write PAM output in the assigned talk time slot. The assigned listen time slots shall be sampled on the Read PAM input at this time, and these audio samples shall be reconstructed into an audio signal with a voltage gain of 2.

When the bias of the talk input returns to 0 volt for more than 2 seconds, the talk input shall no longer be sampled and shall be placed on the Write PAM output. Also, the listen time slots shall no longer be sampled at this time.

When the bias changes to 0 volt for more than 2 seconds, the "in use" pulses in the assigned time slots stop and the telephone is then ready to make another call or accept a call.

3.5.3 Priority Initiation

The initiation of a priority call shall be made when the bias on the talk line changes to -2 volts. The change in bias on the talk input line shall produce a dial tone on the listen output line until the first bit of dial data is received on the talk line, or the bias of the talk line changes. The dial data received on the talk input shall be a telephone number, three decimal numbers coded into 12 binary bits. After all three numbers are received, the Read PAM line shall be observed for "in use" pulses in the priority time slots. If "in use" pulses occur, a busy signal shall appear on the listen output. If no "in use" pulses occur, then at the beginning of the next major frame, "in use" pulses shall be produced on the Write PAM line in the priority time slots, followed by the number contained in the number plug. If the number transmitted is not received on the read PAM line, then a busy signal shall be produced on the "listen" output. This indicates a coincidental initiation of priority calls. If the same number is received on the Read PAM line then after the next series of "in use" pulses, the telephone number of the phone dialed shall be produced on the Write PAM line in the priority time slots.

After the next series of "in use" pulses, the audio from the talk input shall be sampled and placed on the Write PAM line in the first slot of the priority pair. In the same manner, the Read PAM shall be sampled in the second slot of the priority time slot pair, and the audio samples shall be reconstructed into an audio signal and placed on the listen output line.

If the bias on the talk input changes from -2 volts for more than 2 seconds, then the talk input shall not be sampled.

The "in-use" pulses shall not be generated and the telephone shall then be made ready to receive or to initiate another call.

3.5.4 Call Peception (Nonpriority)

Reception of a call can only be made with a 0-volt bias on the talk input (except for priority call reception). The dialing data in the dialing time slots, shall be monitored on the Read PAM input line after the third consecutive set of "in-use" pulses in the dialing time slots. If any of the telephone numbers compare to the number contained in the number plug, the time slot that was received directly after the number shall be used as the talk time slot. The other time slots shall be used as the listen time slots.

Directly following the beginning of the next major frame, after the talk and listen time slots have been recognized by all the telephones involved in the call, the Read PAM shall be monitored for a ring command in the time slot assigned as its own talk time slot. After reception of the ring command, the talk input shall be sampled and placed on the Write PAM output in the time slot assigned as the talk time slot, and the Read PAM input shall be sampled during the time slots assigned as the listen slots and placed on the listen output as interpolated audio.

When the ring command is received on the Read PAM input, a ring tone shall be placed on the listen output. The ring tone shall be repeated until the bias on the talk input changes from 0 to +2 volts or, until the "in-use" pulses in the talk time slot stop.

The talk input signal shall continue to be samples and the samples placed on the Write PAM output until either the bias on the talk input returns to 0 volt for 2 seconds or the "in-use" pulses in the talk time slot stop. Also the listen time slots shall be sampled on the Read PAM input until either the bias on the talk input changes to 0 volt for 2 seconds or the "in-use" pulses in the talk time slot stop.

3.5.5 Call Reception (Priority)

Reception of a priority call shall be made with the talk input bias in either the 0 or +2 volt condition. On the second consecutive set of "in-use" pulses in the priority time slots, the Read PAM input is monitored. If the number contained in the priority time slots compares to the number contained in the number plug and the bias on the talk input is +2 volts, a priority signal shall be produced on the listen output until the bias on the talk input changes to 0 volt. When the bias goes to 0 volt, the talk time slot and the listen time slots shall no longer be sampled. When the bias returns to +2 volts, the talk input shall be sampled and placed on the Write PAM output in the second priority time slot, and the Read PAM shall be sampled during the first priority time slot. If the bias on the talk input is 0 volt when the number plug number is received in the priority time slot, a ring tone shall be produced on the listen output until the bias on the talk input changes to +2 volts or the "in-use" pulses

in the second priority time slot stop. Like other calls, if the bias on the talk line returns to 0 volt for 2 seconds or the "in use" pulses stop in the second priority time slot, the talk input and Read PAM input shall no longer be sampled, and the telephone shall be made ready to accept another call or initiate a call.

SMDS REMOTE TELEPHONE ELECTRONICS

SUBUNIT

DEVELOPMENT SPECIFICATION

1.0 SCOPE

This specification describes the development design goals and major performance specifications of a SMDS subunit building block identified as the Remote Telephone Electronics.

2.0 APPLICABLE DOCUMENTS

a. The guidelines, trade-offs, and functional descriptions included as part of the SMDS Final Report shall be considered as part of this subunit specification.

b. SMDS Central Telephone Electronics Module Specification.

c. SMDS Telephone Number Plug Specification.

d. SMDS Telephone Interface Specification.

3.0 ELECTRICAL PERFORMANCE REQUIREMENTS

3.1 General Requirements

The Remote Telephone Electronics shall interface with the normal telephone support equipment, such as the dialer, handset, earphone, mouthpiece, bell, hook-position switch, and the priority key switch in the Space Base Telephone System. The remote telephone is connected to the central telephone electronics by a four-wire cable, two wires for power and ground and two wires for the talk and listen connections. The talk line conducts amplified mouthpiece audio to the central telephone in a high-level fashion. The priority-key switch and hook-position switch information are sent to the central telephone by means of different voltage biases applied to the talk line. The dialer information is relayed on the talk line to the central telephone, in the form of a digital code generated by the remote telephone. The listen line receives audio from the central telephone, as well as the ring tone and the audio clear tone that clears the talk path.

3.2 Power Requirements

The remote telephone electronics power dissipation shall not exceed 2 watts. The remote telephone electronics power shall be supplied from the central telephone. The input voltage shall be +15 ±0.8 volts.

3.3 Input Requirements

3.3.1 Inputs From Support Equipment

The remote telephone will receive the following inputs from the telephone support equipment.

3.3.1.1 Priority Key Switch

Three lines are needed to interface with the priority key switch. A contact impedance of less than 100 ohms between the bias line and the switched line shall cause a priority condition, and a contact closure impedance of less than 100 ohms between the common line and the switched line shall keep the priority call inactive.

3.3.1.2 Hook Position

Three lines are required to connect the hook position switch. A contact impedance of 100 ohms or less between the bias line and switched line shall be the off-the-hook state, and a contact impedance of 100 ohms or less from the common line to the switched line shall be the on-the-hook position.

3.3.1.3 Dialer

Twelve lines are required from the pushbutton dialer. Two lines are bias and common; the other ten lines correspond to the ten number pushbuttons. A number shall be encoded by the remote telephone when the contact corresponding line is changed from the common line to the bias line through an impedance of less than 100 ohms. The normal state for no numbers to be encoded shall be with the number lines to be switched to the common line through an impedance of less than 100 ohms.

3.3.1.4 Mouthpiece

The handset mouthpiece connection shall be made with two lines; one line shall be common and the other line shall carry the audio signal. The input impedance shall be greater than 10 kilohms and the input signal range shall be from 5 to 100 millivolts. The source impedance shall not exceed 600 ohms.

3.3.2 Listen Input Line

The remote telephone shall receive the listen input line from the central telephone unit. The listen line shall have a source impedance of less than 30 ohms. The range of the audio shall be from 50 millivolts to 1.0 volt. The nominal input impedance shall be 600 ohms. The ring-tone frequency shall be 1052.6 Hz with an amplitude of 2 ±0.5 volts peak-to-peak. The audio-clear tone shall have a frequency of 16,842 Hz with an amplitude of 2 ±0.5 volts and a burst width of 5 to 10 milliseconds.

3.4 Output Requirements

3.4.1 Outputs to Support Equipment

The remote telephone shall produce the following outputs to the support equipment.

3.4.1.1 Earphone

The handset earphone shall present a load impedance of 600 ohms between the two lines to be driven with the amplified listen audio signal. The amplification shall be 20 ±1 dB. The bandwidth shall be limited on the lower end by a -3 dB frequency of 200 ±50 Hz and on the upper end by a -3 dB frequency of 2700 ±700 Hz. The harmonic distortion at 1000 Hz shall be less than 1 percent. The output impedance shall be less than 15 ohms.

3.4.1.2 Bell

The bell load shall be 150 ohms and shall require a voltage of 15 ±1 volts on the power line. The control line shall switch the 150 ohm load to 0 ±0.5 volts when the ring tone is received on the listen line. With no ring tone, the control line shall have an off impedance of at least 1 megohm.

3.4.1.3 Headset Plug

The remote telephone interface with the headset plug shall require six wires. The audio pickup and its return shall be similar to the handset mouthpiece characteristics; the earphone and its return shall be similar to the handset earphone. The other two wires shall provide a current path when the plug is plugged in with an impedance of less than 1 ohm. These two control wires shall provide the necessary signals to route the audio paths onto the headset instead of the handset when the plug is plugged in.

3.4.2 Talk Output

The remote telephone shall produce a talk output to the central telephone unit. The output impedance of this line shall be less than 30 ohms and shall be capable of driving a nominal load impedance of 600 ohms. The audio gain from the handset or headset pickup shall be 26 ±1 dB. The bandwidth shall be limited by a lower end -3 dB frequency of 200 ±50 Hz and by an upper end -3 dB frequency of 2700 ±700 Hz. The harmonic distortion of 1000 Hz shall be less than 1 percent. The talk output shall also produce biases of 2 ±0.5 volts when the hook position switch line is in the off-the-hook state or the headset plug is engaged. A bias of -2 ±0.5 volts shall occur on the talk line when the priority key line is in the priority call state and either the hook position input line is in the off-the-hook state or the headset plug is engaged. A bias of 0 ±0.5 volt shall occur when the hook position input line is in the on-the-hook position and the headset plug is disengaged. The dialer numbers shall also be encoded and placed on the talk line in the form of a 1-2-4-8 binary Manchester code, at a rate of 500 ±100 bits-per-second, with an amplitude of 2 ±0.5 volts peak-to-peak. Each number line input placed in the command position shall produce this 4-bit word, most significant bit first.

3.5 Operational Requirements

3.5.1 Call Reception

Reception of a call shall be made only when the hook-position switch input is in the on-the-hook position and the headset plug disengaged. With the hook position switch in the on-the-hook position and a dial tone is received, the bell control line shall be switched to the 0-volt state until either the hook position changes (or the headset plug is engaged) or the dial tone ends. When the bell control line is switched to the 0-volt state, the ring tone shall be placed on the talk line output with an amplitude of 0.5 ± 0.25 volts peak-to-peak and a frequency equal to the frequency of the ring tone received on the listen line. When the hook position input changes to the off-the-hook condition, or the headset is engaged after having received a ring tone, the following shall occur:

a. The bell control line is placed in the off state.
b. The path that connected the ring tone to the talk output line, with a typical attenuation of 12 dB below the level received on the listen input, shall be attenuated by at least 60 dB below the level received on the listen line.
c. The audio channel between the listen input and earphone output shall be connected with a gain of 20 dB.
d. The audio channel between the mouthpiece pickup and the listen output shall be connected with a gain of 26 dB.
e. The bias on the talk output goes to +2.0 volts.

When the hook position input is returned to the on-the-hook state or when the headset plug is disengaged both audio paths shall be closed or disconnected so the gain is at least 40 dB below the normal gains, 26 dB for the talk channel and 20 dB for the listen channel. The bias on the talk output shall return to 0 volts. The dialer inputs shall remain inhibited (no code is produced on the talk output when the input is in the command state) while the hook position input is on and the headset is disengaged. When the ring tone is received and then either the hook position input changes to the off-the-hook position or the headset plug is engaged, the dialer inputs shall remain inhibited.

3.5.2 Call Initiation

The initiation of a call is split into two parts; the priority call and the normal call.

3.5.2.1 Normal Operation

For normal operation, the priority key switch input shall not be in the priority call position. When the hook position input changes from the on-the-hook to off-the-hook position, or the headset plug is engaged but no ring tone received (the hook position input

was placed in the "on" position) the following shall occur:

a. The gain from the listen input to the earphone output shall change from a maximum of -20 to +20 dB.
b. The bias on the talk output shall change from 0 to +2.0 volts.
c. The dialer pushbuttons can then enter the dialing information and the Manchester code, encoding the numbers pushed, appears on the talk output.

When the same condition exist as above and an audio clear tone is received on the listen input, the following shall occur:

a. The gain from the mouthpiece pickup shall go from a maximum of -14 to +26 dB.
b. The dialer pushbutton inputs shall be inhibited so no code is produced when an input is placed in the command state. When the hook position input returns to the on-the-hook position and the headset plug is disengaged, the audio channels shall be disconnected, and the bias on the talk output shall return to 0 volt.

3.5.2.2 Priority Operation

A priority call shall be initiated when the priority key switch input is in the priority call position. When the hook position input changes from the on-the-hook to off-the-hook position or the headset plug is engaged and the priority switch input is in the priority call position, the following shall occur:

a. The bias on the talk output shall change from 0 to -20 volts.
b. The gain from the listen input to the earphone output shall change from a maximum of -20 to +20 dB.
c. The inhibit on the dialer pushbutton inputs shall be removed so the dialer inputs can be encoded into a Manchester code and applied to the talk output.

When the same condition appears as mentioned above, and an audio clear tone is received on the listen input, the following shall occur.

a. The gain from the mouth piece pickup shall go from a maximum of -14 to +26 dB.
b. The dialer inputs shall be inhibited so no code is produced on the talk output when an input is placed in the command state.

When the hook position input returns to the on-the-hook position and the headset is disengaged, the audio channels are

disconnected, and the bias on the talk line shall return from -2 to 0.0 volts.

3.5.3 Headset Override

The headset shall override the handset when its plug is engaged. The mouthpiece pickup and earphone in the handset shall be disconnected when the headset is engaged.

SMDS TELEPHONE NUMBER PLUG

SUBUNIT

DEVELOPMENT SPECIFICATION

1.0 SCOPE

This specification describes the development design goals and major performance specifications of a SMDS subunit building block identified as the Telephone Number Plug.

2.0 APPLICABLE DOCUMENTS

a. The guidelines, trade-offs, and functional descriptions included as part of the SMDS final report shall be considered as part of this subunit specification.

b. SMDS Central Telephone Electronics Module Specifications.

c. SMDS Remote Telephone Electronics Subunit Specifications.

d. SMDS Telephone Interface Specification.

3.0 ELECTRICAL PERFORMANCE REQUIREMENTS

3.1 General Requirements

The number plug shall connect to the central telephone unit. As many as five number plugs shall interface with the central telephone, but only one number plug shall connect to a single telephone circuit. The number plug shall provide the single circuit with a unique telephone number that is programmable and power through jumper wires.

3.2 Power Requirements

Power lines shall be routed through the number plug. No current shall be drawn from the power lines by the number plug except for insulation leakage to common which shall be less than 1 microampere per-power-line.

3.3 Input Requirements

The number plug shall accept four power lines, as listed below, and the common line:

+15 ± 0.75 volts
-15 ± 0.75 volts
+ 5 ± 0.25 volts
- 5 ± 0.25 volts

3.4 Output Requirements

3.4.1 Power Output

The power lines shall be jumpered through an impedance of less than 0.01 ohms to form the following power outputs.

+15 ± 0.75 volts at 500 mA maximum
-15 ± 0.75 volts at 300 mA maximum
+ 5 ± 0.25 volts at 1.0 A maximum
- 5 ± 0.25 volts at 1.0 A maximum

3.4.2 Programmable Outputs

The 12 programmable outputs shall be grouped into three groups of four each. Each group of four shall represent a 1-2-4-8 binary code of a decimal number. The three decimal numbers shall indicate the telephone number assigned to this plug. The programming shall be achieved by connecting the appropriate "one" bits to +5 volts through an impedance of less than 10 ohms and the "zero" bits to common through an impedance of less than 10 ohms. The 12 programmable outputs shall be capable of conducting 100 milliamperes with no loss in performance.

SMDS TELEPHONE

INTERFACE SPECIFICATION

1.0 SCOPE

This specification describes the electrical interface requirements for the SMDS Telephone Electronics consisting of the Central Telephone Electronics, Remote Telephone Electronics, and the Telephone Number Plug.

2.0 APPLICABLE DOCUMENTS

a. The guidelines, trade-offs and functional descriptions included as part of the SMDS final report shall be considered as part of this interface specification.

b. SMDS Central Telephone Electronics Module Specification

c. SMDS Remote Telephone Electronics Subunit Specification

d. SMDS Telephone Number Plug Specification

3.0 ELECTRICAL INTERFACE REQUIREMENTS

3.1 Central Telephone and Base Level/Deck Level Interface Units Interface

The Central Telephone Electronics is connected to the Base Level/Deck Level unit by four twisted shielded wire pairs, with a characteristic impedance of 128 ohms. The signal level of each shall be 1 volt peak to peak maximum. Figure 4.3.2.3-1 (Volume I) shows the interfaces. Each line shall be terminated at the Central Telephone end with a 128-ohm plug. Should more than one Central Telephone be needed on a deck, each line shall be extended and the terminating plugs shall be placed at the end of the lines.

3.1.1 Write PAM

The Write PAM line shall carry 640 kHz PAM data from the Central Telephone.

3.1.2 Read PAM

The Read PAM line shall conduct the demodulated, 640 kHz PAM data to the central telephone.

3.1.3 Write Clock

The Write Clock line shall conduct the demodulated, 2.56 MHz Write Clock to the Central Telephone.

3.1.4 Read Clock

The Read Clock line shall conduct the demodulated Read Clock to the Central Telephone. The frequency of the Read Clock shall be 2.56 MHz.

3.2 Central Telephone/Remote Telephone Interface

The Central Telephone may be connected to as many as five Remote Telephones. Each Remote Telephone shall be connected to the Central Telephone with a four-wire cable. Two wires shall supply power and ground and two wires shall carry the audio-tone data.

3.3 Remote Telephone/Telephone Support Equipment Interface

The Remote Telephone shall be connected to the support equipment with a 30-wire cable. These 30 lines shall be connected as follows:

a. 12 lines shall connect the dialer

b. 3 lines shall connect the hook switch

c. 3 lines shall connect the priority key

d. 2 lines shall connect the bell

e. 2 lines shall connect the handset earphone

f. 2 lines shall connect the handset mouthpiece

g. 6 lines shall connect the headset

The Remote Telephone interfaces are provided in Figure 4.3.2.2 of Volume I.

SECTION 11.0

SMDS CENTRAL INTERCOM ELECTRONICS

11.0 SMDS CENTRAL INTERCOM

11.1 ACCOMPLISHMENTS

The study of the intercommunication requirements resulted in a conceptual design that implemented 10 channels plus a paging channel of audio communication. The intercom system employs pulse amplitude modulation (PAM) and time division multiplexing (TDM) in achieving a minimum-wire system that facilitates 75 intercom stations. A usable bandwidth of 300 to 3300 Hz was maintained by sampling the audio data at a sufficiently high frequency to place the sum and difference products of the sampling frequency and the audio data well below the level of the audio. In implementing the intercom design, a configuration similar to the telephone system was found to be better than the party line configuration. The final configuration consists of a remote intercom and a central intercom on each deck. There must be a remote intercom for each intercom station on each deck, but the central intercom can facilitate up to five remote intercoms. If more than five intercoms are required on a deck, a second central intercom unit is used.

11.2 PROBLEMS

One major problem was encountered in the design of the intercom system which resulted from making the configuration of the intercom system similar to the telephone system. The problem was relaying the channel selection information to the central intercom from the remote intercom. The remote intercom/central intercom configuration has advantages in that many similar circuits can be used in both the intercom and telephone systems. The other problems such as interchannel interference and timing uncertainty, that were experienced in the telephone system, are not of the same magnitude since the intercom system has a slower PAM data rate even though the sample rate is higher than the sample rate of the telephone system.

11.3 RESOLUTIONS

The channel selection problem was resolved by setting the bias on the audio line from the remote intercom to the central intercom proportional to the channel selection. The bias level encoded by the digital-to-analog (D/A) converter in the central intercom and the appropriate channel or time slot is sampled. The addition of the A/D converter adds to the

complexity of the central intercom by not as much as might be anticipated, since the central intercom has only one converter that can detect the channel selection for all five of the remote intercoms connected to one central intercom. The employment of a variable bias, and encoding the bias, eliminates the need of 10 additional wires per remote intercom. As can be seen by the trade-off section of the telephone report (section 10.7), eliminating the 10 wires on a deck that has 10 intercoms would save 3700 feet of wire.

11.4 MATHEMATICAL ANALYSIS OF DESIGN

The bias signal which denotes the selected intercom channel is a DC signal superimposed on the audio data. An A/D converter is used to decode this bias information. A low-pass filter must precede this A/D converter to prevent the audio signal from interfering with the channel selection signal. The minimum lower cutoff frequency for the remote intercom pre-amplifier is 200 Hz. For a ±1.0% of full-scale tolerance or ±50 millivolts on both the bias and encoder, the minimum window is 150 millivolts. The audio would then be allowed to have an amplitude of only 150 millivolts. The audio would then be allowed to have an amplitude of only 150 millivolts peak.

For a maximum audio input of 2.00 volts peak and assuming no more than a single-order filter, the cutoff frequency of the filter can be found.

$$\frac{150\ mV}{2V} = 0.075 \geq \frac{1}{\sqrt{1+\left(\frac{W}{W_o}\right)^2}}$$

Solving yields:

$$\frac{W}{W_o} \geq 13.3$$

For $W = 2\pi(200\ Hz)$

$W_o \leq 2\pi(15.04\ Hz)$

Which corresponds to a single order filter time constant of

$$T = \frac{1}{W_o} \geq 10.6\ m\ Sec$$

11.5 THEORETICAL PERFORMANCE OF DESIGN

The Space Base Intercom System uses an amplitude-modulated RF carrier conducted from deck-to-deck via coaxial cable to establish the communication link. Time division multiplexed data from the intercoms on each deck is used as the modulator of the RF carrier. On each deck, a demodulator extracts the summed pulse amplitude modulated data from the carrier and supplies the data to the intercoms on that deck. Thus, each deck modulator will be driven by a Write PAM line, and each deck demodulator will have an output of a Read PAM line. The timing uncertainties of the deck-to-deck transmission of the intercom PAM data, are minimized by also transmitting a clock signal through the same media as the data.

Each intercom station is connected to every other station by means of this RF link. The PAM data stream is multiplexed into 11 time slots so there are 11 channels of communication available among the 75 intercom stations. Since a bandwidth of 300 to 3300 Hz was a requirement, the sampling rate of at least 13,300 samples-per-second is necessary to adequately recover the audio data. To achieve desirable results with a minimum of complexity, reconstruction of the audio samples is accomplished through a maximally flat third-order filter with a cutoff at 5280 hertz.

Since each PAM stream contains 11 time slots or channels and each channel must be sampled at a rate equal to or greater than 13,300 samples-per-second, the PAM "bits" would be a maximum of 6.85 microseconds wide. With a 2.56 megahertz clock, a more convenient width of 6.25 microseconds was selected, and the resulting sample rate is 14,545 samples-per-second. The time slots correspond to particular channels. Selecting a channel implies the Read PAM is sampled during its corresponding time slot and the Write PAM is driven with sampled audio during that slot. This system is different than the telephone system, since both transmission and reception by the intercom is done in a single time slot. Then any number of intercoms can be dialed to any channel. The normal push-to-talk switch is located on each station so that no channel can be accidentally left in the transmit mode. The station is either in the transmit or receive mode but not both simultaneously. Each station can accept a paging key that overrides the channel selection and allows the transmission to be made in the paging channel. All stations in the receive mode, will automatically receive the paging channel as well as the selected channel.

11.6 EXPERIMENTAL PERFORMANCE OF DESIGN

No direct experiments were performed on the conceptual design. However, this field of communications is not new to Radiation Incorporated. Past knowledge obtained empirically and through analysis was used in reaching the conceptual design.

11.7 TRADE-OFFS

Implementation of the intercom design required in the areas involving the configuration of the intercom system. The trade-offs were made between the remote intercom/central intercom configuration, such as the telephone system configuration and the deck party line configuration. The deck party line configuration would have all the electronics located at the intercom station. Each station would be connected to the Base Level/Deck Level interface unit by four transmission lines that are shared with the other intercoms on that deck. This presents a problem in cable routing and the timing delays involved in the cable length. Although the timing delays of the party line configuration are not as critical for the intercom system as for the telephone system, the interchannel interference problems would cause the party line system to have a smaller sample time. It appears that this is not as much of a problem as the routing of the four transmission lines. Since PAM is a form of the data, the number of terminations must be uniform on each deck or the amplitudes would be of different magnitudes. Thus the input impedance of each intercom interface must be much greater than the characteristic impedance of the transmission line so the line attenuation is different for each intercom on a deck. The much higher impedance interface causes a reflection problem that can only be eliminated by making the tap-off of the transmission line as short as possible. Thus there can be no splits in the lines and the same lines must run to every intercom. On a 10-intercom deck, at least 500 feet of transmission line (in this case twister-shielded pair), would be needed to connect all intercoms to the Base Level/Deck Level unit.

The remote intercom/central intercom configurations have minimum timing delays since only 10 feet of transmission line is needed to interface the central intercom with the Base Level/Deck Level unit. Also, on a 10-intercom deck, the length of twisted-shielded pair cable is only 50 feet maximum. The disadvantage of this configuration is the problem of channel selection. In the party line configuration, the electronics are located with the channel selection switch. However, for the remote intercom/central intercom configuration the channel selection

switch is located at the remote intercom, and the channel selection must be relayed to the central intercom with the minimum number of cables. As described in the problems and resolutions, this problem was resolved by a variable bias and an encoder. The extra complexity as a result of the encoder is the disadvantage, but the central intercom contains the electronics to handle five intercom stations. This grouping of five actually reduced the complexity since the repeated circuits in the party line configuration, such as the countdown circuits, the clock detectors, and the PAM interfaces circuits (the driver and receiver), are shared by the five intercoms and the remote intercom/central intercom configuration.

11.8 SUMMARY

The conceptual design of a low complexity, minimum wire intercom system was accomplished. Seventy-five intercom stations can be serviced with this system, but the system is designed so it is not limited to just 75 stations. The bandwidth of 300 to 3300 Hz was maintained, and the system has 10 channels of communication plus a paging channel that reaches all stations. The only major problem involved the transmission of the channel selection with a minimum number of wires and minimum complexity to the central intercom. The problem was resolved by the use of a selectable bias on one of the audio lines that ran from the remote unit to the central unit, and an encoder that detected the bias. Since the central intercom contains five intercom circuits, duplication of the A/D converter was minimized, since five intercoms could share one encoder.

11.9 SCHEMATICS AND DRAWINGS DEVELOPED

The drawings relating to the intercom implementation appear in section 4.3.3, Intercom Subsystem description, of this report.

11.10 DEVELOPMENT SPECIFICATIONS

The following development specifications are provided as a part of this section:

1. SMDS Central Intercom Electronics Module
2. SMDS Remote Intercom Electronics Subunit
3. SMDS Intercom Interface Specification

SMDS CENTRAL INTERCOM ELECTRONICS

MODULE

DEVELOPMENT SPECIFICATION

1.0 SCOPE

The specification describes the development design goals and major performance specification of a SMDS major module building block identified as the Central Intercom Electronics.

2.0 APPLICABLE DOCUMENTS

a. The guidelines, trade-offs, and functional descriptions included as part of the SMDS Final Report shall be considered as part of this module specification.
b. SMDS Remote Intercom Electronics Subunit Specification
c. SMDS Intercom Interface Specificaton

3.0 ELECTRICAL PERFORMANCE SPECIFICATIONS

3.1 General Requirements

The Central Intercom Electronics samples the audio from up to five remote intercoms and multiplexes the audio samples into a single output (the Write PAM output) that is used as the modulation signal in the intercon modulator in the Base Level/Deck Level Electronics. The central intercom also accepts a PAM signal (the Read PAM input) from the intercom demodulator in the Base Level Electronics that reconstructs the audio samples into audio signals which drive the remote intercoms. The Base Level/Deck Level Electronics also supplies the central intercom with the timing signals (the Write Clock and the Read Clock) that are synchronized with the PAM input and output signals. The five remote intercom interfaces each consist of four wires. Two conductors are power and ground, and the other two conductors are talk input and listen output. The talk input contains the audio to be sampled and placed on the Write PAM output and the bias that indicates the channel selection. The listen output contains only the processed audio samples received on the Read PAM input.

3.2 Power Requirements

The Central Intercom Electronics power dissipation shall not exceed more than 6 watts. The power lines available are:

+15 ±0.75 volts
-15 ±0.75 volts
+ 5 ±0.25 volts
- 5 ±0.25 volts

This power dissipation does not include the 1 watt supplied to each remote intercom.

3.3 Input Requirements

3.3.1 Talk Input

Each of the five talk inputs from the remote intercoms shall have an input impedance of greater than 600 ohms. The source impedance of each talk source shall be less than 2.0 volts with a maximum bandwidth of 200 Hz and the bias level shall vary from +5.1 to -0.1 volts. There are 11 discrete bias levels. The 11 levels shall be every +500 millivolts starting with +0.00 volts. The tolerance of each bias shall be ±50 millivolts.

3.3.2 Read PAM Input

The Read PAM input shall have a differential input impedance of 100,000 ohms or greater and a common mode input impedance of 1,000,000 ohms or greater. The differential signal level shall be +1.0 to -1.0 volts and the common mode signal range shall be +2.0 to -2.0 volts. The signal is a PAM data stream with a sample width of 6.25 microseconds. Eleven different samples are made before the frame is repeated. The Read PAM data signal shall be delayed from the Read Clock no more than 250 nanoseconds.

3.3.3 Write Clock Input

The Write clock input is a differential signal that shall have a minimum differential input impedance of 10,000 ohms and a minimum common mode input impedance of 10,000 ohms. The clock amplitude shall be 1.0 ±0.5 volts peak-to-peak and the frequency of the clock shall be 2.56 MHz. The common mode voltage shall be within +1.5 to -1.5 volts. Every 16,896 clock cycles a synchronization space appears. The absence of a clock cycle will be used for synchronization.

3.3.4 Read Clock Input

The Read clock input is a differential signal that shall have a minimum differential input impedance of 10,000 ohms and a minimum common mode input impedance of 10,000 ohms. The clock amplitude shall be 1.0 ±0.5 volts peak-to-peak. The clock frequency shall be 2.56 MHz. The synchronization space, the absence of a clock cycle, shall be used for synchronization and will occur every 16,896 clock cycles. The common mode voltage range shall be +1.5 to -1.5 volts.

3.4 Output Requirements

3.4.1 Write PAM Output

The Write PAM output is a differential current that drives a 128 ohm twisted-shielded pair. The transmission will be terminated at both ends with 128 ohms. The common mode impedance will be less than 100 ohms. The audio signal appearing on the talk input shall be sampled and converted into a differential current with a transconductance of 2.0 milliamperes per volt +10% when the audio is commanded to be sampled. When the audio is not sampled, the transconductance shall be less than 0.2 microamperes per volt. The zero sampling time varying current shall be less than 0.2 microamperes, and the direct

current offset current shall be less than 200 microamperes. The output admittance shall be less than 5.0 microamperes per volt. The Write PAM output shall be synchronized with the Write Clock with no time slot in the Write PAM data stream delayed or advanced more than 100 nanoseconds. The bandwidth of the talk input must be limited on the upper end by at least a third-order maximally flat filter with a -3 dB point at 3300 ±150 Hz and on the low end by a -3 dB point not above 300 Hz.

3.4.2 Listen Output

The listen output to each of the five remote intercoms must drive an impedance of 600 ohms. The output impedance must be less than 30 ohms. The voltage gain from the Read PAM input to the listen output shall be 1.0 ±10% for the normal channels and 2.0 ±10% for the paging channel. That is, the audio samples received at the Read PAM input shall be amplified and reconstructed into the audio signal at the listen output with a variation in gain less than 1.0 dB over the bandwidth of the audio. The intermodulation products of the 14,545 Hz sampling frequency and the 300 to 3300 Hz audio frequency shall be at least 26 dB below the output audio level.

3.5 Operational Requirements

3.5.1 Data Stream

The data stream is comprised of 11 time slots, each 6.25 microseconds wide. The first time slot is the paging time slot; it will be sampled on the Read PAM continously. Audio samples will be written on the Write PAM output in this first time slot only. When the bias on the talk input is 0.00, the other 10 time slots will be sampled on the Read PAM input and written on the Write PAM output. When the corresponding bias on the talk input is detected, the different bias levels and the corresponding time slots or channels are listed below:

BIAS	TIME SLOTS	CHANNELS
0.0 volts ± 50 millivolts	1	Paging channel
0.5 volts ± 50 millivolts	2	Channel 1
1.0 volts ± 50 millivolts	3	Channel 2
1.5 volts ± 50 millivolts	4	Channel 3
2.0 volts ± 50 millivolts	5	Channel 4
2.5 volts ± 50 millivolts	6	Channel 5
3.0 volts ± 50 millivolts	7	Channel 6
3.5 volts ± 50 millivolts	8	Channel 7
4.0 volts ± 50 millivolts	9	Channel 8
4.5 volts ± 50 millivolts	10	Channel 9
5.0 volts ± 50 millivolts	11	Channel 10

The bias of each of the five talk line inputs must be determined at least every 10 milliseconds. The audio at a frequency of 700 Hz and an amplitude of 2.0 volts peak shall not cause the bias to be encoded erroneously.

current offset current shall be less than 200 microamperes. The output admittance shall be less than 5.0 microamperes per volt. The Write PAM output shall be synchronized with the Write Clock with no time slot in the Write PAM data stream delayed or advanced more than 100 nanoseconds. The bandwidth of the talk input must be limited on the upper end by at least a third-order maximally flat filter with a -3 dB point at 3300 ±150 Hz and on the low end by a -3 dB point not above 300 Hz.

3.4.2 Listen Output

The listen output to each of the five remote intercoms must drive an impedance of 600 ohms. The output impedance must be less than 30 ohms. The voltage gain from the Read PAM input to the listen output shall be 1.0 ±10% for the normal channels and 2.0 ±10% for the paging channel. That is, the audio samples received at the Read PAM input shall be amplified and reconstructed into the audio signal at the listen output with a variation in gain less than 1.0 dB over the bandwidth of the audio. The intermodulation products of the 14,545 Hz sampling frequency and the 300 to 3300 Hz audio frequency shall be at least 26 dB below the output audio level.

3.5 Operational Requirements

3.5.1 Data Stream

The data stream is comprised of 11 time slots, each 6.25 microseconds wide. The first time slot is the paging time slot: it will be sampled on the Read PAM continously. Audio samples will be written on the Write PAM output in this first time slot only. When the bias on the talk input is 0.00, the other 10 time slots will be sampled on the Read PAM input and written on the Write PAM output. When the corresponding bias on the talk input is detected, the different bias levels and the corresponding time slots or channels are listed below:

BIAS	TIME SLOTS	CHANNELS
0.0 volts ± 50 millivolts	1	Paging channel
0.5 volts ± 50 millivolts	2	Channel 1
1.0 volts ± 50 millivolts	3	Channel 2
1.5 volts ± 50 millivolts	4	Channel 3
2.0 volts ± 50 millivolts	5	Channel 4
2.5 volts ± 50 millivolts	6	Channel 5
3.0 volts ± 50 millivolts	7	Channel 6
3.5 volts ± 50 millivolts	8	Channel 7
4.0 volts ± 50 millivolts	9	Channel 8
4.5 volts ± 50 millivolts	10	Channel 9
5.0 volts ± 50 millivolts	11	Channel 10

The bias of each of the five talk line inputs must be determined at least every 10 milliseconds. The audio at a frequency of 200 Hz and an amplitude of 2.0 volts peak shall not cause the bias to be encoded erroneously.

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SMDS REMOTE INTERCOM ELECTRONICS

SUBUNIT

DEVELOPMENT SPECIFICATION

1.0 SCOPE

This specification describes the development design goals and major performance specification of a SMDS major subunit building block identified as the Remote Intercom Electronics.

2.0 APPLICABLE DOCUMENTS

a. The guidelines, tradeoffs, and functional descriptions included as part of the SMDS Final Report shall be considered as part of this subunit specification.
b. SMDS Central Intercom Electronics Module Specification
c. SMDS Intercom Interface Specification

3.0 ELECTRICAL PERFORMANCE SPECIFICATIONS

3.1 General Requirements

The Remote Intercom Electronics will interface with a speaker, a 10-position channel selection switch, a paging key switch, and a talk/listen switch. The Remote Intercom is connected to the Central Intercom with a four-conductor cable. Two conductors supply the Remote Intercom with power and ground. The other two wires conduct audio signals and various bias voltages to and from the Central Intercom. The talk output supplies to the Central Intercom an audio signal that is amplified from the speaker and a selectable bias level that the audio is centered about. The bias is controlled by channel selection switch position. The listen input, from the Central Intercom, contains the audio signal that is to be amplified and applied to the speaker. The talk/listen switch controls the mode of operation; that is, whether the speaker is driven by the Remote Intercom as in the listen mode, or whether the speaker drives the Remote Intercom which is the talk mode. The paging key switch overrides the channel selection bias.

3.2 Power Requirements

The Remote Intercom Electronics shall not dissipate more than one watt of power. The input power shall be supplied from the Central Intercom. The line will be +15 ±0.8 volts with respect to the common or signal return also supplied by the Central Intercom.

3.3 Input Requirements

3.3.1 Support Equipment Inputs

The Remote Intercom will receive the following inputs from the support equipment of the intercom.

3.3.1.1 Paging Key Switch

The paging key switch supplies three input lines. A

closure impedance of less than 100 ohms between the bias line and the switched line will cause the talk output bias to go to zero, indicating a paging condition. A closure impedance of less than 100 ohms between the common line and the switched line will cause no override.

3.3.1.2 Channel Switch

The 10-position channel switch inputs shall have no more than 1 ohm of impedance between the switched input and the selected position input. Each position input shall be isolated from all other position inputs greater than 10 megohms.

3.3.1.3 Talk/Listen Switch

The talk/listen switch supplies two lines to the Remote Intercom. One line is an input and the other is an output discussed in 3.4.1. The input shall be connected to the speaker for the switch in the talk mode. The input impedance shall be greater than 10 kilohms and the source impedance, including the switch contact impedance, shall be less than 600 ohms. The input signal range shall be from 5 to 100 millivolts in amplitude and DC to 50 kHz in frequency.

3.3.2 Listen Input

The input to the Remote Intercom from the Central Intercom is the listen input. The input impedance shall be greater than 600 ohms and the source impedance will be less than 30 ohms. The signal shall be from 25 millivolts to 1.0 volts in amplitude and from 100 to 10,000 Hz in frequency.

3.4 Output Requirements

3.4.1 Intercom Output

The Remote Intercom must supply only one output to the speaker via the talk/listen switch line. The load impedance would then vary from a load of 600 ohms to no load. The source impedance shall be less than 15 ohms. The amplification from the listen input to the speaker output shall be 20 ±1 dB. The bandwidth shall be limited by -3 dB points (single order roll-offs) at 240 ±60 Hz and 4400 ±1100 Hz.

3.4.2 Talk Output

The Remote Intercom shall provide one output to the Central Intercom, the talk output. The talk output shall be capable of driving a load of 600 ohms. The output impedance shall be less than 30 ohms. The amplification from the speaker input to the talk output shall be 26 ±1 dB. The bandwidth of this amplification shall be limited by at least single order rolloffs with -3 dB points occurring at 250 ±50 Hz and 4400 ±1100 Hz. The DC bias on the talk output shall be controlled by the channel selection switch position and the paging key switch. If the paging key switch is in the "paging"

position, the bias on the talk output shall be 0.0 volt ±50 millivolts. If the paging key is not in the "paging" position, the bias on the talk output shall correspond to the channel selected by the switch position listed below:

SWITCH POSITION	TALK OUTPUT BIAS
Channel 1	0.5 ± 0.050 volts
Channel 2	1.0 ± 0.050 volts
Channel 3	1.5 ± 0.050 volts
Channel 4	2.0 ± 0.050 volts
Channel 5	2.5 ± 0.050 volts
Channel 6	3.0 ± 0.050 volts
Channel 7	3.5 ± 0.050 volts
Channel 8	4.0 ± 0.050 volts
Channel 9	4.5 ± 0.050 volts
Channel 10	5.0 ± 0.050 volts

3.5 Operational Requirement

The operation of the Remote Intercom is implied from the above sections. The separation of the audio applied on the listen input and the audio appearing at the talk output shall be greater than 40 dB from DC to 5000 Hz. This implies the attenuation from the speaker output of the Remote Intercom to the speaker input must be at least 86 dB.

SMDS INTERCOM

INTERFACE SPECIFICATION

1.0 SCOPE

This specification describes the electrical interface requirements for the SMDS Intercom Electronics consisting of the Central Intercom Electronics and Remote Intercom Electronics.

2.0 APPLICABLE DOCUMENTS

a. The guidelines, trade-offs, and functional descriptions included as part of the SMDS Final Report shall be considered as part of this interface specification.

b. SMDS Central Intercom Electronics Module Specification.

c. SMDS Remote Intercom Electronics Subunit Specification.

3.0 ELECTRICAL INTERFACE SPECIFICATIONS

3.1 Central Intercom and Base Level/Deck Level Interface Unit Interface

The Central Intercom Electronics is connected to the Base Level/Deck Level Interface Electronics by four twisted-shielded pairs each with a characteristic impedance of 128 ohms. The signal level of each is a maximum of 1 volt peak-to-peak. Figure 4.3.3.4-1 (volume I) shows the interfaces. Each line is terminated at both ends with its characteristic impedance.

3.1.1 Write PAM

The Write PAM line carries 160 kHz PAM data from the Central Intercom.

3.1.2 Read PAM

The Read PAM line conducts demodulated 160 kHz PAM data to the Central Intercom.

3.1.3 Write Clock

The Write Clock line conducts the demodulated Write Clock to the Central Intercom. The frequency of the Write Clock is 2.56 MHz.

3.1.4 Read Clock

The Read Clock line conducts the demodulated Read Clock to the Central Intercom. The frequency of the Read Clock is 2.56 MHz.

3.2 Central Intercom and Remote Intercom Interfaces

The Central Intercom can be connected to as many as five

Remote Intercoms. Each Remote Intercom is connected to the Central Intercom by four wires. Two of the wires contained in the four-wire cable, supply the Remote Intercom with power and ground. The remaining two conductors carry the audio and bias to and from each unit as described in sections 3.3.2 and 3.4.2 of the SMDS Central Intercom Electronics Module Development Specification and section 3.3.2 and 3.4.2 of the SMDS Remote Intercom Electronics Subunit Development Specification. Figures 4.3.3.3 , 4.3.3.4-1, and 4.3.3.4 -2 illustrate the interconnections.

3.3 Remote Intercom and Intercom Support Equipment Interfaces

The Remote Intercom is connected to the support equipment by 17 wires including the return lines. Eleven lines connect the channel selection switch to the Remote Intercom. Three lines connect the Remote Intercom to the paging key switch. Three lines connect the speaker and talk/listen switch to the Remote Intercom. Figure 4.3.3.3 illustrates the interfaces and signals and impedance levels of the interfaces, which are discussed in sections 3.3.1 and 3.4.1 of the Remote Intercom Electronics Specification.

SECTION 12.0

DIGITAL STATION

12.0 DIGITAL STATION

12.1 ACCOMPLISHMENTS

As a result of this portion of the SMDS study effort for Space Base, a digital data network was conceptually designed. This network has the capability of transferring high-speed digital data between 256 spatially separated stations without requiring a complex central control and monitoring unit.

The digital stations employ specially developed, high-speed bipolar LSI chips and utilize power strobing to minimize system power consumption. Data rate to the bus is approximately 5000 bps while monitoring capability can be equal to 1.28 Mbps, if desired. The proposed system utilizes a unique clock implementation which eliminates the effects of level modem and level spatial delays.

Assigned time slot operation was selected as the basic operating mode. In this manner, each digital station is assigned a unique time slot during which it can transmit up to 32 bits (plus parity) of data. Synchronizing action, controlled by the system clocks, is accomplished once every major frame.

12.2 PROBLEMS

Several major technical problems had to be considered in detail prior to completion of the proposed digital station system. Each of these problems is discussed briefly below.

12.2.1 Implementation Trade

The following four implementations were considered as potential candidates for the SMDS digital requirements:

a. Interrogate/Reply

b. Two-Pass Polling

c. Unassigned Time Slot

d. Assigned Time Slot

Each of these has features which make it suitable for the required application.

12.2.1.1 Interrogate/Reply

This candidate operates in a command response mode. A central control unit is established which controls the digital station operation through a controlled format of commands transmitted to all digital stations. The commanded station then transmits data on the bus, making it available for all interested stations.

12.2.1.2 Two-Pass Polling

A polling implementation operates in a fixed-format mode in which each station is polled for potential data requests. This is transmitted, if data is desired, after which the poll is passed to the next station. During the second pass, those stations from which data was previously requested transmit data under the same poll control. In this manner, data is transmitted only by those stations whose data is currently required at other locations.

12.2.1.3 Unassigned Time Slot

This potential implementation would be designed very similar to the SMDS telephone system. A fixed number of time slots would be established by a central timing unit (CTU). Any station requiring data would acquire a time slot, if available, and transmit control information to the station processing the data needed. The interrogated station would then reply.

12.2.1.4 Assigned Time Slot

The assigned time slot digital station candidate would use a rigidly controlled format. A CTU would generate 256 time slots. Each station would transmit data upon coincidence of the current time slot with the time slot assigned (permanently) to each station. Stations requiring data from the currently transmitting unit would simply enable their receivers during this interval.

12.2.2 System Delays

Perhaps the most significant problem encountered in development of the SMDS digital stations was that of dealing with system delays. The delays may be classified as interlevel (main bus) delays and intralevel. The main bus delays are mainly spatial; generated by the requirement to interconnect digital stations at 21 different levels, involving transmission distances of up to 350 feet. The intralevel delays are due to both distance and equipment. The

effects of spatial delays in excess of 45 feet combined with coupler, receiver, and transmitter delays had to be overcome to obtain a workable digital system.

12.2.3 Level Distribution

The preferred system for conveying data from the Base Level/Deck Level Modem to the individual level digital stations presented a significant problem. The effects of spatial delay, EMI performance, and fail-safe operation requirements had to be considered in detail. In addition, a data code had to be selected which was compatible with the above level-distribution characteristics.

12.3 RESOLUTIONS

12.3.1 Preferred Implementation

As outlined, four candidate systems were considered to embody the basic concepts of a suitable digital system. Each was found to possess some characteristics which would be of use in a multiport digital station system. Based on a review of the salient characteristics of each candidate and a subsequent comparison of these with the Statement of Work guidelines, it was decided that the assigned time slot candidate was preferred for use on Space Base. The assigned time slot digital implementation has the advantage of minimal station complexity, low percentage of overhead data, high data reception rate, and negligible central control complexity. A potential disadvantage, rigid format with fixed sample rate (5000 bps/station) is difficult to access without detailed information about the digital station interface equipment.

12.3.2 System Delays

The interlevel spatial delay problem was resolved through adoption of a time directional data transmission bus, in which data is only propagated in one direction - each level generates signals which are propagated "down" the bus. The bus is arranged in a round-trip configuration enabling all levels to obtain data from all other levels. By generation of a 1.28 MHz clock at the beginning of the bus, all levels are synchronized; that is, if response to the bus clock at the level interface were instantaneous, all data would be exactly in sync with clock at all levels.

The intralevel delays problem was resolved by the introduction of a second 1.28 MHz clock (read clock) delayed from the original clock (write clock) by an amount equal to the worst-case level delay. By incorporation of this clock, presence of data at the read clock transition was assured.

12.3.3 Level Distribution

For the delayed read clock concept to work successfully, it was necessary for all delays from the Base Level/Deck Level Modem to the digital station output interference to be both minimized and controlled. The minimization of delay was effected by using two semicircular buses for level distribution. This enabled spatial delays to be kept within the limits of 52 to 122 nanoseconds. Also the digital station delay was minimized through use of high-speed, power strobed logic. The total station delay is estimated as 175 to 75 nanoseconds, worst case.

In addition to delay control, the level distribution network must be immune from EMI (susceptibility and generation), as well as short circuits at the digital stations. EMI tests run on several cable types resulted in the selection of twinaxial cable for the level bus and the stubs connecting the individual stations to this bus. This prevents shorts within the individual stations from affecting operation of the level bus. A fail-safe transformer coupling was selected as the stub-bus coupler. A final consideration of the level distribution problem was that of selecting a suitable code for data encoding. Manchester code was selected to eliminate the possibility of significant direct current on the bus.

12.4 MATHEMATICAL ANALYSIS OF DESIGN

The only significant analysis required for the proposed digital station was the detailed level delay analysis. As mentioned, the minimization and control of all delays in the level path is essential to the operation of the delayed read clock concept.

The delays expected on the level distribution are listed below. Analysis of each delay is presented.

a. Base Level/Deck Level Demodulator

b. Deck Level Distribution Bus (2X)

c. Digital Station Demodulation

d. Digital Station Modulation

e. Base Level/Deck Level Modulator

12.4.1 Base Level/Deck Level Demodulator

In conventional RF analysis of an envelope detector, preceded by a bandpass filter, it is usually assumed that the resultant waveform rise time is related to bandwidth as

$$\tau_A = \frac{0.85}{\text{Bandwidth}}$$

For the 6 MHz video channels, a 4.5 MHz usable bandwidth is expecred. Thus, the write clock rise time from its demodulator will be approximately

$$\tau_r = \frac{0.85}{4.5 \times 10^6} = 189 \text{ nanoseconds}$$

Actual delay of the write clock for level distribution will be a function of the switching level selected. It is reasonable to expect the signal-to-noise ratio at the demodulator output will be such that the delay can be held to 100 nanoseconds. Assuming this to be the maximum delay, variations in signal level and detector characteristics are assumed to reduce this delay to a minimum of 50 nanoseconds.

12.4.2 Deck Level Distribution Bus

A delay is created in the write clock signal as it propagates along the level bus. A value of 1.5 nanoseconds delay per foot of bus has been measured for several twisted shielded pairs. A maximum distance between the Base Level/Deck Level Interface unit and a digital station on a level is approximately 41 feet. This results in a one-way delay of 63 nanoseconds. A minimum distance is 17 feet with a resultant minimum delay of 26 nanoseconds. Since both the clock and the resultant level data encounter this spatial delay, these delays must be doubled.

12.4.3 Digital Station Demodulation

A high signal-to-noise ratio at all digital station is assumed. Use of high-speed detectors and high-speed nonsaturating logic makes it seem reasonable that the total delay from write receiver input through time slot recognition to be effectively controlled within the range of 25 to 75 nanoseconds.

12.4.4 Digital Station Modulation

All data for transmission is contained in a 32-bit bipolar LSI device. The delay from data clock to modulator data output is estimated to be within the limits of 50 to 100 nanoseconds.

12.4.5 Base Level/Deck Level Modulation

Premodulation filtering of data will be required to reduce transmission of data harmonics above the third; thereby, reducing adjacent channel crosstalk. This high-pass filtering will result in a data rise time to modulator input as follows:

$$\tau_r = \frac{0.35}{BW}; \text{ or for Space Base } \tau_r = \frac{0.35}{4.5 \times 10^6} = 78 \text{ ns}$$

The modulated carrier might therefore be delayed by 50 nanoseconds (maximum and 25 nanoseconds (minimum) under conditions of signal and carrier level variation. In summary, the level delays are shown below:

	Max (ns)	Min (ns)
Base Level/Deck Level Demodulator	100	50
Deck Level Distribution Bus (2X)	126	52
Digital Station Demodulation	75	25
Digital Station Modulation	100	50
Base Level/Deck Level Modulator	50	25
	451	202

Based on this level delay analysis, the system read clock must be delayed by at least 450 nanoseconds (say 500) from the write clock.

12.5 THEORETICAL PERFORMANCE OF DESIGN

The theoretical performance of the SMDS digital design is described, in detail, in sections 2.4 and 4.3.4 of this report.

12.6 EXPERIMENTAL PERFORMANCE OF DESIGN

No experimental performance evaluation of the proposed SMDS digital station complex was performed directly as a result of this study. However, a 1 megabit, 200 foot, data distribution system was implemented for a 32 station system. Further experiments were performed on a 300-foot section of twisted shielded pair using a 5 megabit Manchester data transmission. This experimentation was carried on concurrently with the SMDS study and much of the information gained was utilized for the SMDS study.

12.7 TRADE-OFFS

The trade studies performed in selection of the proposed system were:

a. Determination of the preferred method of digital station operation (assigned time slot versus unassigned time slot, handshaking, etc.)

b. Determination of the maximum possible bit rate as it is affected by video channel width and level distribution delays.

c. Optimization of the Level Distribution configuration.

These trade studies are presented in section 2.4 of this report.

12.8 SUMMARY

A feasible 256 station, digital data distribution system has been conceived for the Space Base SMDS. The system permits communication of any station with all others, with data reception rates in excess of 1 Mbps. Data transmission rate is fixed at approximately 5 kbps, a rate which appears to be adequate for the housekeeping nature of the SMDS digital requirements. Digital stations may be located anywhere on the Space Base without concern about proper operation. No complex central control is required to coordinate the station transactions, which enhances system reliability and permits attainment of the high information rates outlined above.

12.9 SCHEMATICS AND DRAWINGS DEVELOPED

The drawings relating to the Digital Stations appear in section 4.3.4, volume I, of this report.

12.10 DEVELOPMENT SPECIFICATION

The following development specification is provided as a part of this section:

SMDS Digital Station Module

SMDS DIGITAL STATION

MODULE

DEVELOPMENT SPECIFICATION

1.0 SCOPE

This specification describes the development design goals and major performance Specifications of a SMDS major Module building block identified as the Digital Station Module.

2.0 APPLICABLE DOCUMENTS

The guidelines, trade-offs, and functional descriptions included as part of the SMDS final report shall be considered as part of this Module Specification.

3.0 ELECTRICAL PERFORMANCE REQUIREMENTS

3.1 General

The Digital Station Module (DSM) is the major element in a digital data transfer system for use on Space Base. The system is configured to permit each of 256 stations to transmit 32 bits (plus parity) of digital data onto a common one-way bus; each station transmitting at a time uniquely determined by its Time Slot Plug (TSP) wiring. In addition to data transmission as described, the DSM must have the capability of decoding any 33 bit word of serial-digital data on the data bus. Control of the read/write capability of the DSM is accomplished by two clocks; the read clock and the write clock. Synchronization is performed by controlled interruption of these same two clocks.

3.2 Digital Station Input and Output Requirements

3.2.1 Digital Station Module User Interface

Refer to figure 1, DSM Interface, for this and the following sections. The user interface is comprised of 75 single conductor lines which control the operation of the DSM, as well as provide input/output (I/O) data. These lines shall be compatible with MECL III logic or equivalent (Logic 0 = 0±.250 volt; logic 1 = -1 to -1.5 volts).

3.2.1.1 Output Request Enable

This single line shall, when a logic 1, cause the DSM to decommutate 33 bits of data from the data stream existing at the Receiver Data input to the DSM. The time slot location of the 33 bits shall be controlled by the status of the Output Data Address.

3.2.1.2 Output Data Address

The 8 Output Data Address lines are used to determine which time slot data shall be decommutated.

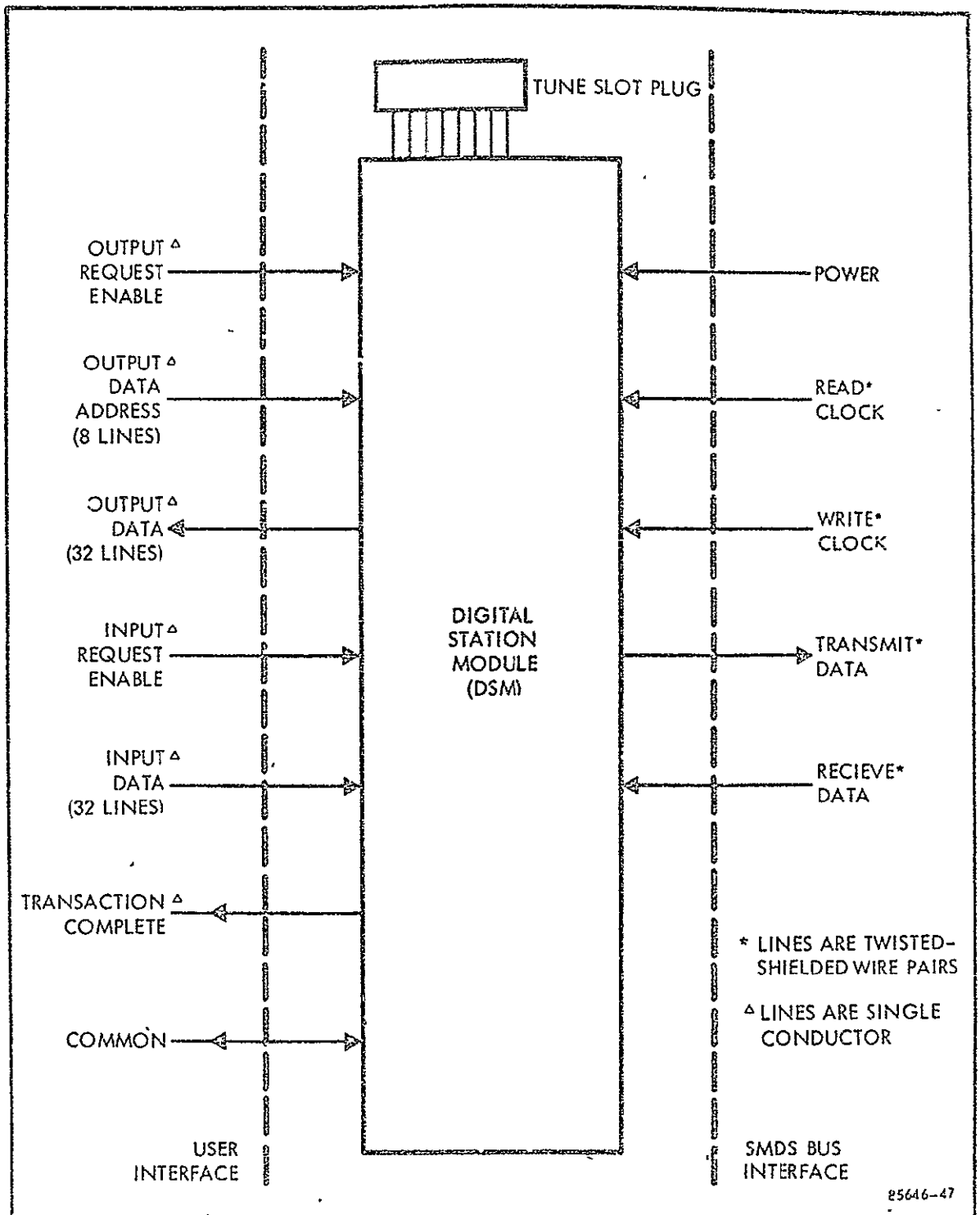


Figure 1. Digital Station Module (DSM) Interface

PAGE 3 REV

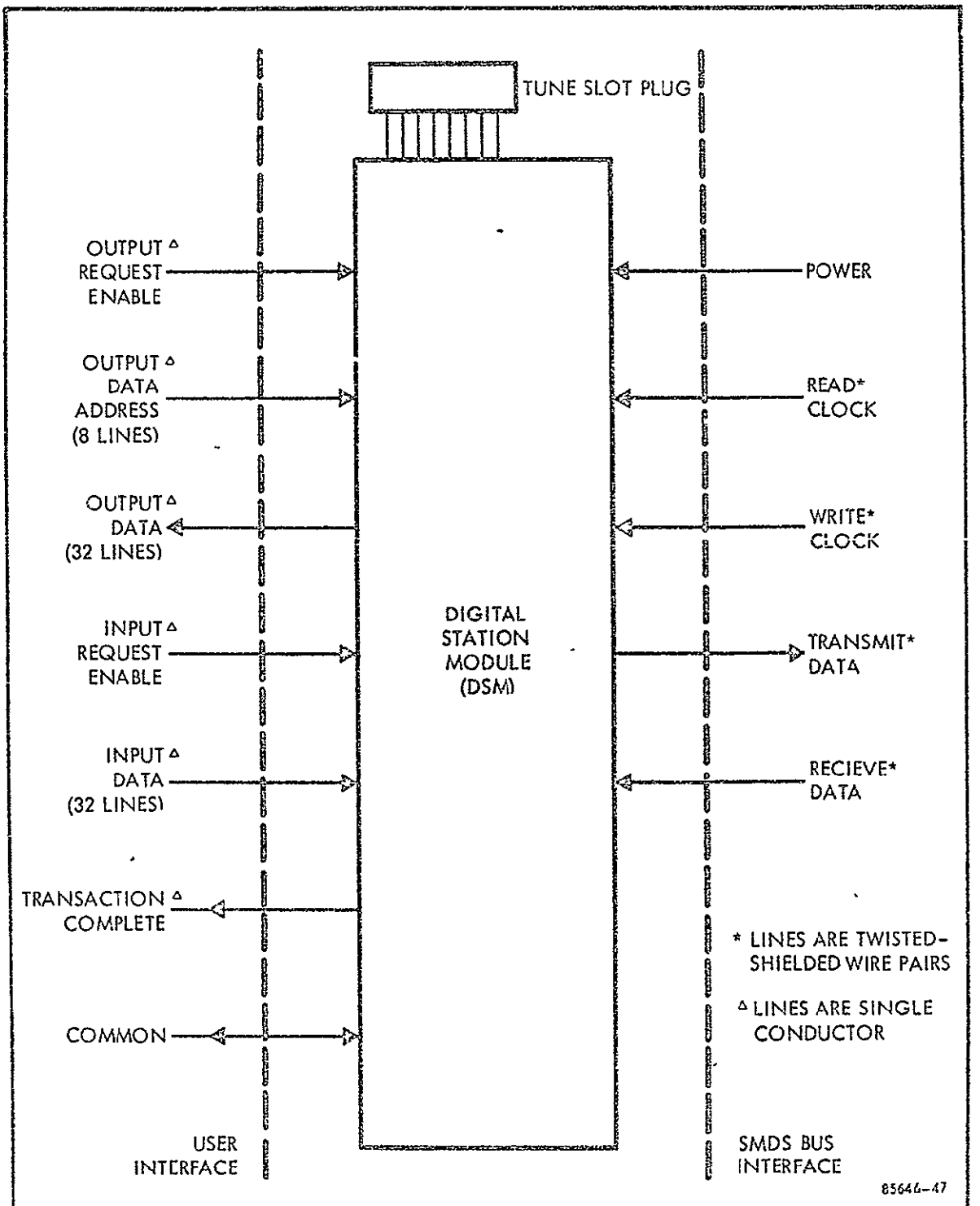


Figure 1. Digital Station Module (DSM) Interface

PAGE 3 REV

3.2.1.3 Output Data Lines

These 32 lines shall display the data contained in the time slot designated by the Output Data Address lines if the Output Request Enable line is a logic 1. The data shall be held until the Output Data Address is again coincident, at which time the data shall be updated if a change is found in the addressed time slot. When the Output Request Enable goes to a logic 0, the Output Data Lines shall be cleared to zero.

3.2.1.4 Input Request Enable

This line, on going to a logic 1, shall be used to initiate data transmission by the DSM. The DSM shall transmit the 32 bits of data at the Input Data Lines upon coincidence of the DSM write time slot counter with the time slot data contained by the time slot plug. The data existing at the transition of the Input Request Enable shall be stored by the DSM within 1 clock cycle of the Input Request Enable transition.

3.2.1.5 Input Data Lines

These 32 lines shall contain MECL III (or equivalent) logic compatible signals for transmission on the Transmit Data Line. The relationship of these lines and the Input Request Enable is specified in 3.2.1.4 above.

3.2.1.6 Transaction Complete

The DSM shall be required to signal the completion of either a 32-bit transmission or reception of 32 bits as requested. After data transmission, the DSM shall generate a pulse of approximately 1 clock cycle duration, coincident with the transmission of bit 33 (parity). After reception, if parity is correct, the DSM shall output a similar pulse coincident with the reception of the parity bit.

3.2.1.7 Signal Characteristics

All signals shall be derived from MECL III (or equivalent) logic and shall be compatible with MECL III.

3.2.2 Digital Station Module/Bus (DSM/B) Interface

The DSM/B interface consists of four twisted shielded pairs (excluding power). The function of each connection (refer to figure 1) shall be as specified below.

3.2.2.1 Read Clock

Due to spatial delays encountered in the Space Base distribution systems, two clocks are required to maintain synchronism

of the system. The Read Clock line provides timing data to permit the DSM to correctly decommutate data. All timing for the processing of data received on the Receiver Data Line shall be derived from this clock line. Once every 256 time slots (8448 cycles) at least one clock cycle will be skipped. The "skip" shall be sensed by the DSM and the DSM-receive circuitry shall reset to time slot zero.

3.2.2.2 Write Clock

The Write Clock line provides timing and synchronization signals in a manner analogous to that of the Read Clock. All timing for the transmission of data on the Transmit Data/Line shall be derived from this clock.

3.2.2.3 Read Clock, Write Clock Signal Characteristics

The sinusoidal frequency of the received clock signals will be 2.56 ± 0.06 Mbps. The amplitude of these signals will be within the range of 0.5 to 2 volts peak-to-peak, depending on the location of the DSM and the status of the level distribution bus. The DSM shall accept signal amplitude variations within this range without degradation of performance.

3.2.2.4 Receive Data

Data shall be transmitted throughout Space Base in Manchester (II + 180°) format. The DSM, in conjunction with timing from the Read Clock and control signals from the user interface, shall receive and decode serial-digital data from this line and output the resulting data as required by control.

3.2.2.5 Transmit Data

The DSM shall transmit serial-digital data as required by the user interface control signals. The data shall be encoded into Manchester (II + 180°) format prior to transmission.

3.2.2.6 Transmit Data Signal Characteristics

The DSM shall be capable of generating a Manchester (II + 180°) serial-data stream with voltage amplitude of 2 volts peak-to-peak into a 78 ohm ± 10% cable. The amplitude of this signal shall not vary more than ± 5% with worst-case variations of power, temperature, or cable impedance.

3.2.3 Bit Rate

The DSM shall operate at a nominal data rate of 1.28 Mbps at read and write clock frequencies of 2.56 Mbps. The DSM shall operate without degraded performance at bit rate (and corresponding clock) reduction to 640 kbps.

3.2.4 DSM Delay Requirements

Application of the DSM in a spatially distributed complex requires that delays be minimized and controlled. This can only be accomplished by extreme care in design and the use of high-speed (MECL III or equivalent) non-saturating logic. The maximum allowable delay from the appropriate write clock transition to the appearance of the first transmitted bit shall be .70 to 175 nanoseconds under all operating conditions.

3.2.5 Power Requirements

The DSM shall require no more than two power supply voltages with supply tolerances better than ± 5% over all operating conditions. Every effort shall be made to minimize power consumption which shall not exceed 5 watts, maximum.

3.3 DSM Multiplexer

3.3.1 Basic Operation

The Input Multiplexer (IM) shall be a 32-bit parallel-to-serial converter capable of operating at a 1.28 Mbps rate. The IM shall, upon being enabled, transmit 33 bits of NRZ data in synchronism with an externally applied clock. Bit 33 shall be an odd-parity bit, the computation of which shall be done within the IM. A block diagram of the IM is shown in figure 2.

3.3.2 Input Requirements

Thirty-five input lines shall be required for proper operation of the IM. The functions of these lines shall be as specified below.

3.3.2.1 Data Input

Thirty-two MECL III signals shall be parallel coupled into the IM. This data shall be present prior to activation of the Enable 1 line.

3.3.2.2 Enable 1

The Enable 1 line is provided by the equipment which generates the data to be transmitted. When this line is a Logic 1 data shall be outputted in synchronism with the clock, provided the Enable 2 line is active.

3.3.2.3 Enable 2

The Enable 2 line is generated within the DSM, indicating time slot coincidence. With both enables active, NRZ data shall be transmitted on the Serial Digital Output line.

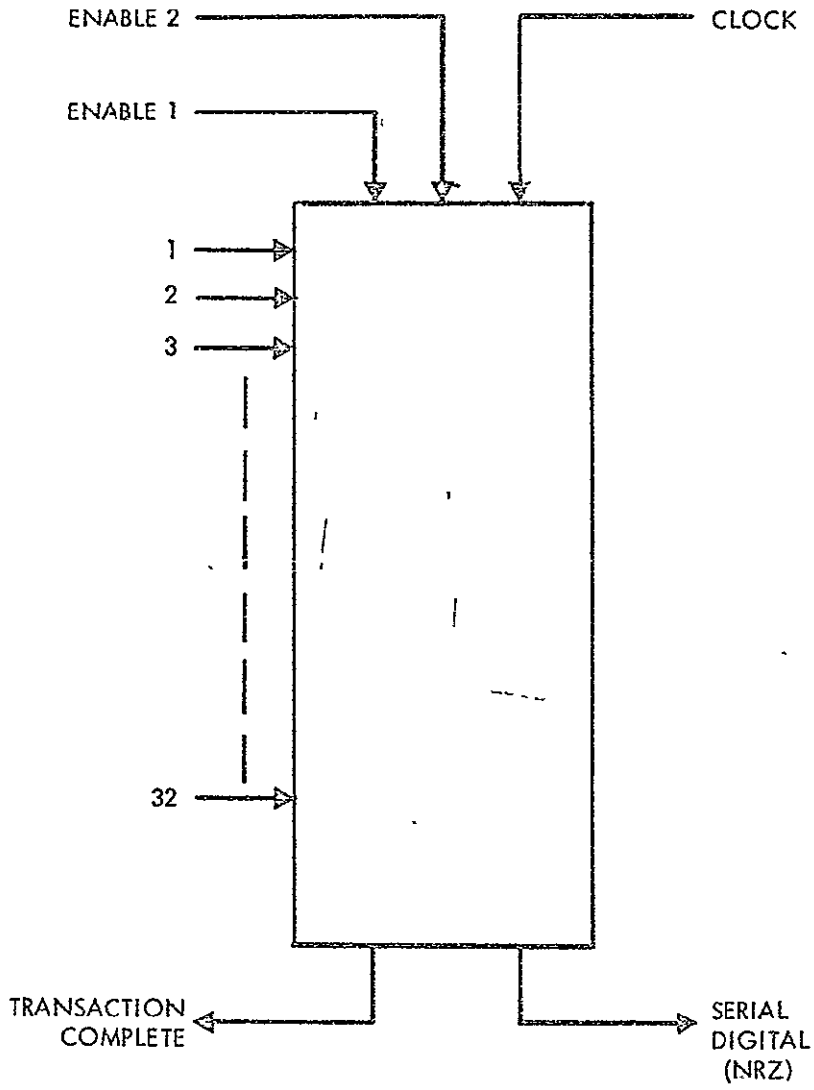


Figure 2. Input Multiplexer (Parallel-to-Serial Converter)

3.3.3 Output Requirements

Two output lines are required form the IM microcircuit. The functions of these lines shall be as specified below.

3.3.3.1 Serial Digital

Serial-Digital (NRZ) data shall be outputted on this line (if Enable 1 and Enable 2 are active) in synchronism with the clock. The levels shall be: "zero" 0 ± 0.5 volt and "one" -2.5 ±0.5 volts into 1000 ± 10%.

3.3.3.2 Transaction Complete

This line, normally low, shall be active during the transmission of bit 33 (parity).

3.3.4 Critical Delays and Timing

3.3.4.1 Throughput Delay

Throughput delay is defined for the IM as the delay (50% points) between the application of Enable 2 and the appearance of the first data bit. In use, the clock may or may not be in a logic 1 state at the time of the Enable 2 excursion. The IM throughput delay shall be no greater than 20 nanoseconds. A maximum of 20 nanoseconds delay between successive clock cycles and data output is also specified.

3.3.4.2 Latch Delay

The data at the 32 data input lines may change after one clock cycle. The IM shall store the data existing within the first clock cycle after enable.

3.3.5 Power Requiremnnts

A maximum of two power supplies with voltage tolerances of ± 5% shall be required for operation of the IM. The maximum power dissipated by the IM shall be less than 1.0 watts.

3.4 DSM Multiplexer

3.4.1 Basic Operation

The Output Demultiplexer (OD) shall be a 32-bit serial-to-parallel converter capable of operating at a 1.28 Mbps rate. The OD shall, upon being enabled, receive 33 bits of NRZ data. An external clock is provided to establish timing for decommutation of the input serial data. Bit 33 shall be an odd-parity bit, the validity of which shall be checked within the OD prior to parallel output of the received data. A block diagram of the OD is shown in Figure 3.

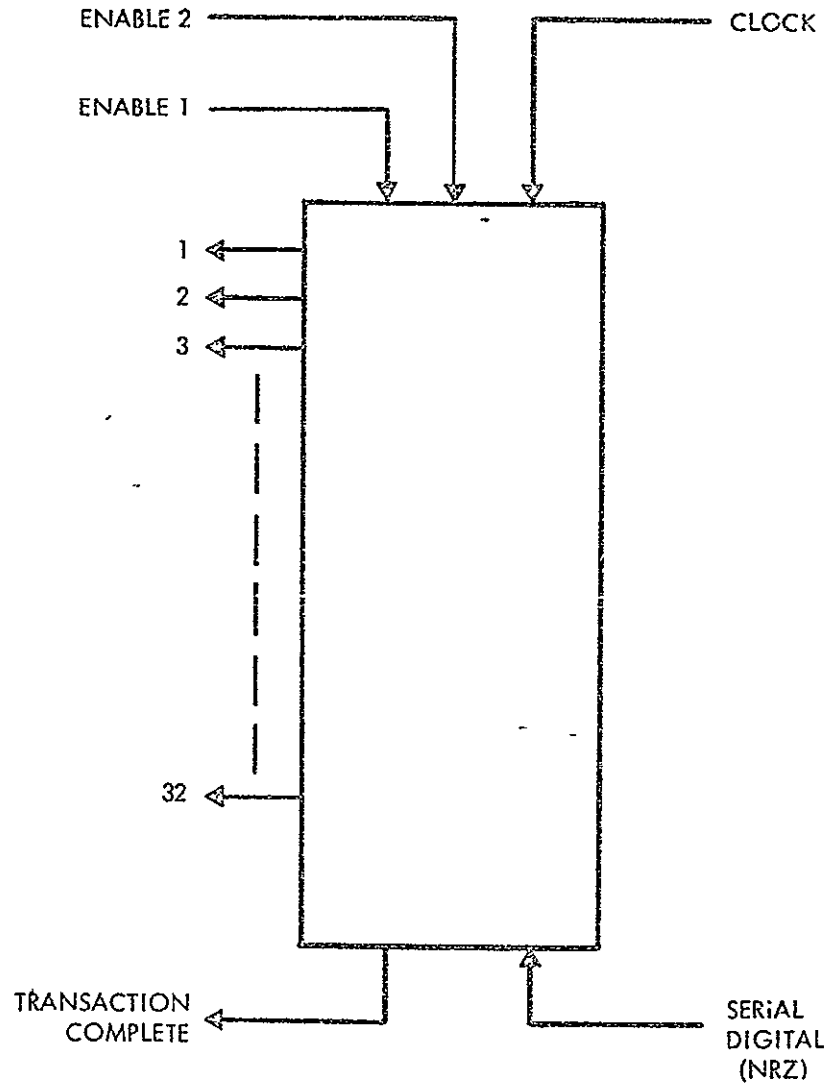


Figure 3. Output Demultiplexer (Serial-to-Converter)

3.4.2 Input Requirements

Four input lines shall be required for proper operation of the OD. The functions of these lines shall be as specified below.

3.4.2.1 Enable 1, Enable 2

The OD shall be inoperative until both these enable lines are activated by setting to a logic 1 state. Upon activation, NRZ data present at the Serial-Digital input shall be shifted into the OD under control of the Clock Input.

3.4.2.2 Clock

The OD shall operate with a clock frequency of 1.28 MHz. Operation shall not be affected by reduction of the clock frequency to 640 kHz.

3.4.2.3 Serial Digital

This input terminal of the OD shall receive NRZ serial-digital data generated within the DSM. After being enabled, the OD shall receive 33 bits (1 parity) under control of the clock input.

3.4.3 Output Requirements

Thirty-three lines shall be required to perform the desired function of the OD. The functions of these lines shall be as specified below:

3.4.3.1 Output

Thirty-two output lines shall be required for presentation of the received serial-digital data. These lines shall be MECL III compatible. Data shall be presented on these lines for the remainder of the 33rd clock cycle period once parity has been verified. The data shall be held indefinitely, regardless of the state of Enable 2, but shall be updated if the enable and clock criteria are met subsequently. If Enable 1 is deactivated after the Transaction Complete line is enabled, the data shall be held only for the duration of the 33rd clock cycle (900 nanoseconds). If parity is incorrect, the output lines shall not be changed from the latest state.

3.4.3.2 Transaction Complete

This line, normally low, shall be active the remainder of the 33rd clock cycle after parity has been verified.

3.4.4 Throughput Delay

The throughput delay is defined for the OD as the delay (50% points) between the application of the enable commands and the start of the data received operation (internal measurement). This delay shall not exceed 100 nanoseconds. A maximum delay between parity bit arrival and data output of 100 nanoseconds is also specified.

3.4.5 Power Requirements

A maximum of two power supplies with voltage tolerances of ±5% shall be required for operation of the OD. The maximum power dissipated by the OD shall be less than 1.0 watts.

SECTION 13.0

CIRCUIT DEVELOPMENT

13.0 CIRCUIT DEVELOPMENT

A number of circuits which require further development for use in the SMDS, have been identified during the course of this study. Where appropriate, discussions of these circuits were included in the technical description of the modules or subunits where they were used. The remaining units are described in the following paragraphs.

13.1 CRITICAL CIRCUIT DESCRIPTIONS

13.1.1 UHF Mainline Amplifier

The circuits required for AGC and slope equalization of the Mainline UHF Amplifier (see section 7.3.4) have been identified as circuits which will require additional development.

Active filters are also desirable for filtering the pilot channels and their development is encouraged.

Ultra-linear wideband amplifier at UHF frequencies are identified as requiring further development in section 7.3.4 and their desirable characteristics are specified in the section 7.0 specifications.

13.1.2 UHF Modulator and Demodulator

Voltage tunable UHF bandpass filters are identified in section 9.3.1 as requiring additional development.

Frequency synthesizer design is identified in section 9.3.2 as requiring additional development.

13.1.3 Telephone and Intercom

The Telephone and Intercom possess similar circuitry which may be developed as one unit. The Transconductance Amplifier and the Differential Receiver are identified as requiring additional development. These requirements are discussed more fully in section 13.2

13.1.4 Digital Station Modem

The concepts involved in transmission and reception of digital data at the digital stations, are not complex from a logic design point of view. The operation of a Manchester

encoder-decoder/receiver-transmitter at 1.28 Mbps is straightforward. Counting and comparison for determination of time slot coincidence are also relatively well practiced digital techniques. Serial-to-parallel and parallel-to-serial converter technology is well developed, and 8-bit units of these devices are currently marketed as MSI components by the semiconductor industry.

Thus, in one sense, there are no critical circuits incorporated in the conceptual design of the SMDS digital station modem. However, because of a need to keep the level delay variation to a minimum, it is necessary to accomplish the above functions at the highest possible speeds. As shown in the mathematical analysis of section 12.4, the total turn-around time for the Digital Station (from write pulse to data on line) must be less than 175 nonoseconds. This requires that Manchester decoding, counting, comparison, shifting, and encoding operations be extremely fast. This can only be accomplished by straightforward design and the use of high-speed, nonsaturating logic.

In the interest of high speed as well as low cost, the functions of data conversion (serial/parallel/serial) have been incorporated in LSI bipolar chips. It is considered that these are the two critical circuits for design of the SMDS digital station. The specifications for these units are provided as part of the Digital Station Module Specifications, section 12.0.

13.2 MICROCIRCUIT DEVELOPMENT

13.2.1 UHF Amplifier

The SMDS UHF Amplifier Subunit Development Specification in section 7.0 of this report, is a microcircuit specification. Development of microcircuit UHF amplifiers is currently in progress within the semiconductor industry (section 4.2.5.1).

13.2.2 Telephone and Intercom

13.2.2.1 Transconductance Amplifier

The transconductance amplifier that drives the write PAM transmission line is a critical circuit. Driving a transmission line in a current mode is often desired, if the driving element does not have the matched impedance of the line. The transconductance amplifier converts a single-ended voltage into a differential current which is proportional to the applied

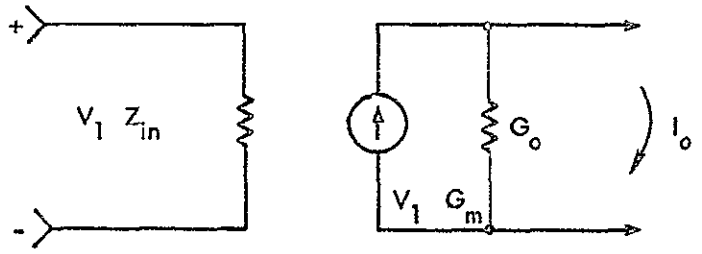
input voltage. High transconductance accuracy and low-output admittance are the critical parameters of this circuit. The transconductance should be 2.0 milliamperes per volt, ±5 percent, and the output admittance should not be greater than 5.0 microamperes per volt. Other parameters of this circuit are listed below: -

a. The input voltage range shall be within +2.5 to -2.5 volts.

b. The input impedance shall be greater than 50 kilohms.

c. The maximum load impedance shall not exceed 1000 ohms differential and 1000 ohms common mode.

A model of the circuit is shown below.



where:

V_1 is the input voltage

Z_{in} is the input impedance

G_m is the output transconductance

G_o is the output admittance

13.2.2.2 Differential Receiver

The read PAM differential receiver is considered a critical circuit. It must have good differential operational amplifier parameters, and the gain bandwidth product must be at the state-of-the-art limit of 15 to 20 MHz. The input voltage range is +1.0 to -1.0 volts differential and +2.0 to -2.0 volts common mode, and the differential gain is 2.0 ± 3 percent. However, a problem exists in achieving a bandwidth of at least 4.0 MHz. Other required parameters are listed as follows:

a. The input impedance must be at least 100 kilohms differential and at least 1 megohm common mode.

b. The common mode to differential conversion must be no greater than 100 microvolts differential output per volt of common mode.

c. The output impedance should not exceed 100 ohms.

The similarity between the transconductance amplifier and the receiver circuit should be exploited to minimize development costs.

13.2.2.3 Clock Detector

The clock detector is considered a critical circuit because of its requirement to detect the reset condition within the clock signal for synchronization. The clock signal must be amplified and converted into a logic level, which is subsequently counted down. The clock detector will generate a counter reset command upon the absence of two clock cycles. Required parameters of this circuit are listed below:

a. The input impedance must be greater than 10,000 ohms differential and 10,000 ohms common mode.

b. The peak-to-peak amplitude of the clock will be 500 millivolts to 1.50 volts.

c. The frequency of the clock is 2.56 megahertz. The outputs must be a logically compatible clock signal and reset signal.

13.2.3 Digital Station

The Digital Station Module Multiplexer and Demultiplexer, appearing in the specifications portion of section 12.0 of this report, are both considered microcircuit elements. These circuits are also discussed in section 13.1.4.

SECTION 14.0

FUTURE SMDS DEVELOPMENT

14.0 FUTURE SMDS DEVELOPMENT

The preceding sections of this report have conceived, analized, developed, and specified hardware which, when implemented, will comprise a Space Base Telecommunications System. Several recommendations are made at the conclusion of volume I (section 5). The first of these recommendations is for further study in the areas of extended bandwidth, bus routing, and TDM transmission via video channels. These tasks must precede the development of any of the SMDS UHF modems. The second recommendation, for further survey and research into parallel and related development efforts by industry, may be carried on concurrently with the three study tasks described previously. The hardware development for the modules and subunits specified in sections 7 through 12 of this report, may begin only after the execution of the first two recommendations.

The level of effort for the three study tasks is on the order of 8,000 to 10,000 dollars each, for a period of 6 to 9 months. The implementation of the second recommendation may be conducted at several levels, ranging from a vendor survey to a large-scale components evaluation program. The approximate cost and schedule for a program of this type is dependent upon the level of effort desired. The third recommendation for hardware development should proceed on those items which can be identified as necessary for future space vehicle telecommunications requirements. Again, costs and schedules are dependent upon the level of effort desired, which may range from breadboard development models to deliverable prototype equipment.

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