PROCESS TECHNIQUES STUDY OF INTEGRATED CIRCUITS FINAL SCIENTIFIC REPORT

By

Jerry V. Brandewie and C. W. Scott

June 1970

Prepared under Contract No. NAS 12-4 by
NORTH AMERICAN ROCKWELL CORPORATION
Anaheim, California

Electronics Research Center

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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(See Table X, page 50)

CONTENTS

CONTENTS (Cont)

ILLUSTRATIONS

TABLES

PROCESS TECHNIQUES STUDY OF INTEGRATED CIRCUITS

By J. V. Brandewie and C. W. Scott

Autonetics Division of North American Rockwell Corp.

Anaheim, California

SUMMARY

The purpose of this program was to investigate and resolve some of the dominant problems of modern planar technology, particularly those tending to impede its evolution into a large scale integration and ultimate reliability. A further purpose was to provide instrumental support services to NASA-ERC in failure analysis and instrumental capabilities.

Major program effort was directed toward the determination of why structural defects are produced in thermally grown oxides and the definition of corrective actions for their elimination. A dielectric defect detection tool was developed for use in location of defects in oxides. This technique was then successfully utilized to isolate potential process and structural parameters which effected defect densities. Results confirmed that a significant cause of oxide defects was the thermal expansion mismatch between silicon and silicon oxide. An improved surface preparation technique was developed which significantly reduced defect densities.

An evaluation was made of impurity contamination in oxide layers. Techniques utilized included C-V measurements, solids mass spectrometry, Auger analysis, ion microanalyzer analysis, and dielectric relaxation. Results obtained were not conclusive, however the possibility of elements other than Na (ie Li), which could effect device properties was indicated. Of the instrumental techniques utilized the ion microanalyzer appeared to have the greatest future potential for the analysis of impurities in similar structures at the desired detection limits.

Other investigations were conducted including gas ambient studies in which the effects of hydrogen and water on the performance of various transistor samples were evaluated. A group of integrated circuits was exposed to various ambient conditions. Other studies performed provided insight into the origin of atomic species contributing to inversion. A compilation of failure analysis techniques and package hermeticity test methods are included.

Routine failure analysis services were provided and analyses were completed on several groups of devices including 89 npn transistors and 65 integrated circuits.

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INTRODUCTION

Objectives

The primary objective of the investigations under Contract NAS 12-4 has been, from its inception, the development of advanced process techniques for the fabrication of high reliability silicon integrated circuits. This objective initially was formulated under two task items. The first item called attention to an instrumental investigation of planar processing techniques, with special emphasis on device surfaces, for the purpose of discovering and correcting failure modes in the following seven categories:

1. Effects of gas ambients during fabrication
2. Effects of traces of materials deposited during fabrication
3. Application of photoresist and photoetch techniques
4. Processing of the oxide
5. Scribing
6. Contact attachment
7. Effects of contact between the processing tools and the wafer during fabrication.

The second item formulated specific studies relating to interactions between the silicon and the highly insulating material in contact with it, and to the effects of such interactions on integrated circuit performance, including long term drift, which is of major concern in extended space missions.

The broad area of activity covered by this statement of work was made so deliberately, to provide flexibility in the attack on emerging problems in a rapidly advancing field, such as those relating to large scale integration, and to provide latitude in the assessment of the relative importance of such problems so that the work could be directed at all times to meaningful ends. A further advantage of this philosophy lay in the opportunity it afforded in the full utilization of the considerable instrumental capabilities and interdisciplinary skills of Autonetics without risking compartmentalization in specific areas. This type of approach is indeed necessary in dealing with a technology as complex and sensitive to minor perturbations as silicon planar processing. The broad approach also brings to bear Autonetics extensive operations and industrial knowledge viewpoint on reliability problems, a factor which is crucial to its satisfactory performance on major contracts with the Government. As a result, the massive records and compilations of data developed on previous component reliability programs have been accessible to serve as guidelines for investigations under the present program.

Redefinitions of Objectives

As work progressed, however, objectives were crystallized in certain areas and phased out in others, either because a satisfactory conclusion had been reached or because a solution to the problem had been reached within the industry itself. In general, these new Statement of Work items were drawn to more specific areas which could, however, still be categorized within the broader range first formulated, the intent being to reflect more precisely the content of current program activities and to provide a formal mechanism for support of new and important problem investigations.

In time, however, the rate of accumulation of new task items began to exceed their rate of completion. The apparent resulting extension of available personnel over many areas was, to a certain extent, exaggerated because of the presence of a certain degree of overlap among some items. While this attested to the consistency of the overall program it also created a somewhat over-ambitious picture of the activities undertaken which could lead to a potential dilution of accomplishment. Consequently, the objectives of the program were redrawn into five categories of investigation as follows:

Investigational Activities:

1. Failure Mechanisms related to Oxide Passivation Defects
2. Failure Mechanisms Associated with Silicon Oxide Impurities
3. Miscellaneous Failure Problems

Services:

1. Failure Analysis Service and Consultation
2. Instrumental Capability Profile.

These categories reflect the overall purpose of the program, which is to investigate some of the dominant problems confronting planar technology and to seek solutions to these problems, as well as to provide NASA-ERC with instrumental support and consulting services. At the same time the reporting format was changed to reflect more clearly the resulting program consolidation.

Program emphasis in terms of time, manpower, and priority was heavily weighted on Item 1 – silicon oxide dielectric defects. Substantial data was accumulated on the origin of oxide defects which could result in significant reductions in defect densities if appropriate process changes are made by suppliers.

Acknowledgments

Numerous Autonetics personnel contributed to the information reported here. Dr. J.E. Meinhard was the original principal investigator on this program and hence a large proportion of the work reported was contributed by him. Major contributions were provided by Dr. P.J. Besser, P.H. Eisenberg and R.A. Meyer. Others contributing were J. Kersey, S. Higashi, L. Gillete, Dr. P. Palmberg, T. Hagey, S. O'Donnell, Dr. J.M. Axelrod, and W.W. Weller.

CONCLUSIONS

The objectives achieved under Contract NAS 12-4 have been significant in a diversity of investigational areas. In many instances potential innovations and improvements in process techniques have been clearly indicated. In others certain conclusions, though currently useful, should be regarded as temporary because of the viable nature of planar technology as a whole. In still other areas, potential conclusions are emerging as a result of progress in the solution of specific problems or as a result of reports of such progress in evoking additional investigations elsewhere. The complexity of integrated circuit processing, which is a direct result of the multiplicity of scientific and engineering disciplines on which the technology has been erected, generally has proved an effective stimulant to these advances. These accomplishments, and their process implications, are enumerated below:

1. Accomplished: Proof of strong entrapment of hydrogen from steam, by radiotracer technique, in thermally grown silicon dioxide layers. Process implications: The trapped hydrogen may contribute to the inversion of planar pnp transistors and to the instability of MOS-FET gate threshold voltages by proton migration.

2. Accomplished: Demonstration of sodium contamination, by neutron activation analysis, in silicon dioxide layers grown by conventionally "clean" methods. Process implications: Steps should be taken to exclude sodium in planar processing as an additional contributor to inversion. This effect has been abundantly confirmed elsewhere.

3. Accomplished: Demonstration of a slight initial difference in inversion recovery kinetics between a group of deuterated transistors and a comparable group of hydrated transistors. Process implications: Proton migration may be a source of inversion in planar transistors using oxides grown under moist conditions.

4. Accomplished: Development of progressive resistance to inversion by repeated inversion and deinversion of planar transistors. Process implications: Tends to confirm an electrochemical ion transport model for inversion, thereby achieving improved long-term reliability.

5. Accomplished: Proof of a strong EPR signal from the interaction of vacuum-deposited aluminum on silicon dioxide layers, indicating reduction by the aluminum and the formation of oxygen vacancies. Process implications: The formation of oxygen vacancies by this mechanism can be avoided by using less active metals (e.g., gold) for intraconnections, thereby reducing the possibility of inversion and contributing to long-term reliability.

6. Accomplished: Demonstration of an absence of an EPR signal corresponding to oxygen vacancies at the $Si-SiO_2$ interface. Process implications: Inversion from this specific source is highly improbable.

7. Accomplished: Demonstration of the same characteristic EPR signal from either sodium or fluoride contamination of silicon dioxide. Process implications: Traces of fluoride, as well as trapping states and contribute to inversion. Steps should be introduced after etching treatments to remove residual fluoride.

8. Accomplished: Proof that the effect of hydrogen on transistor betas, by environmental testing, is nonspecific and tends to be curative rather than degradative. Process implications: The presence of hydrogen in package atmospheres is not inimical to the long-term reliability of planar bipolar transistors.

9. Accomplished: Demonstration that propagation of significant crystal damage, by etch-pit count technique, into adjacent sensitive device areas as a result of conventional scribing procedure is improbable. Process implications: Scribing done with appropriate equipment, combined with precise registry and proper maintenance, does not appear to constitute a reliability hazard. Continued alertness in this area, however, is recommended as the investigation was not exhaustive and did not cover such contingencies as diamond wear, registry deviations, etc.

10. Accomplished: By calculation, in diffusion steps complete mixing of input gases occurs in the first 4 inches of furnace tube. Process implications: Introduction of baffles, or other mechanical means to create turbulence, will not avail in improving the uniformity of diffusion doping as conventionally practiced. This exercise, however, ignores potential streaming effects across the wafers themselves, particularly in situations where the diffusant is an extremely dilute component of the gas phase.

11. Accomplished: Demonstration that dielectric defects in oxide layers generally are cumulative with processing. Process implications: Innovations should be sought that minimize the thermomechanical flexing caused by high-temperature treatments.

12. Accomplished: Demonstration that the higher the compressive stress in an oxide layer, the higher the defect abundance. Process implications: Compressive stress can be moderated by additives that reduce the glass set temperature and the thermal expansion mismatch with silicon. This approach, however, is beset with certain difficulties, such as the avoidance of unwanted impurity (trapping) states and the exact control of composition. Rather than attempt to manipulate the compressive stress in this fashion, it is recommended that defect occurrence be brought under control by identifying and eliminating the physical irregularities which activate local ruptures in the oxide.

13. Accomplished: Demonstration that a higher defect incidence in oxide grown on mechanically polished than on chemically polished substrates. Process implications: One of the physical irregularities contributing to oxide defects may be embedded lapping grains or crystal damage sites caused by lapping. Wafer pretreatments therefore should be terminated by some form of chemical polish.

14. Accomplished: Demonstration that superficial etching by HF increases significantly the oxide defect population to thickness ratio. Process implications: Control of MOS gate oxide thicknesses, which are typically of the order of 1000Å, should be accomplished by growth techniques rather than HF thinning techniques. This would require additional precautions to prevent or remove outer-skin sodium contamination normally eliminated in HF thinning.

15. Accomplished: Observation that a significant localization of defects at abrupt steps in oxide thickness. Process implications: Fortunately a large proportion of such steps are located at windows where metallization contact with the substrate is desired. However, cognizance of this potential failure mode should be a factor in integrated circuit design. Metallizations, where possible, should be routed to avoid sharp changes in oxide thickness, and oxide overlap at contact windows should be sufficient to provide impervious protection to surrounding junctions and substrate.

16. Accomplished: Proof that repeated heating and cooling of oxidized silicon wafers in an inert ambient produces a substantial increase in defect density. Process implications: This observation provides some insight as to why continued processing contributes to defect incidence (Item 11) as well as arguing against manufacturing decisions to reprocess in an effort salvage, for example, the results of an inadequate diffusion.

17. Accomplished: Demonstration that gentle mechanical wiping of oxide layers increases the incidence of dielectric defects. Process implications: As in Item 16 this provides further insight into the structural character of oxide defects, implying that a spalling effect is involved that loosens material sufficiently at certain sites to render it susceptible to subsequent removal by mechanical means. It also indicates that the handling of wafers during manufacture must be minimized as much as possible and done with great care. This would apply to almost any tool used in handling, since the referenced wiping experiments were done with cotton swabs.

18. Accomplished: Proof that removal of one oxide layer (by etching) produces a significant increase in the defect density of the oxide layer remaining on the opposite face of the wafer. Process implications: The wafer is mechanically flexed by this treatment, as amply demonstrated by experiment, imparting a convex curvature to the opposite layer, which contributes to the postulated spalling effect adduced in Item 17, above. If a wafer could be processed completely symmetrically, using the same masks, etching steps, etc, on both sides, dielectric defects from this source could be minimized. A more practical recommendation is to process only one side while maintaining intact oxide on the other.

19. Accomplished: Proof that defect density decreases exponentially with increasing oxide thickness and with the square root of oxidation time. Process implications: Use as thick oxide layers as economically feasible where other design criteria are not thereby compromised.

20. Accomplished: Demonstration that existing defects in thermal oxides often can be reduced significantly by a pyrolytically deposited oxide. Process implications: This procedure is an expensive extra step and does not really solve the basic defect problem. The effectiveness of this procedure varies considerably among processors. Uniform thickness control of the deposited oxide is difficult to achieve.

21. Accomplished: Proof that the presence of water during oxidation, or at the termination of a dry oxidation, produces a lower defect incidence than in oxides grown dry. Process implications: This effect of water is interpreted as a result of a reduction of bond strain from the introduction of hydroxyl groups into the silica network in a manner analogous to that of other oxide additives. The so-called hydroxyl groups, however, are really acidic and capable of yielding protons that may contribute to inversion, as indicated in Items 1 and 3. Nevertheless, the use of water as an oxidation additive is recommended for most planar processing on the basis that proton migration is a minor problem relative to that of oxide defects.

22. Accomplished: Demonstration that variation in wafer cooling rates after oxidation has a negligible effect on dielectric defect incidence. Process implications: Control of cooling rates is unessential. This effect is consistent with a thermal expansion mismatch mechanism that is dependent only on ΔT and not the derivative of ΔT with respect to time.

23. Accomplished: Demonstration that addition of nonvolatile mineral salts to steam source does not increase defect densities. Process implications: Water quality with respect to nonvolatile constituents is not critical. Spray carryover either is negligible or is trapped by the hot furnace tube before reaching the wafers.

24. Accomplished: Proof that oxide growth rate variations do not affect defect densities significantly. Process implication: Control of such parameters as oxidation temperature, or steam concentration in the process gas, is not critical from the standpoint of defect densities. However, such control remains critical for other reasons, such as control of layer thickness, diffusion boundaries, etc. Moreover, oxidation rate at the very beginning of oxidation is emerging as an important parameter affecting defect densities in very thin oxides.

25. Accomplished: Demonstration that substrate doping has little effect on defect densities. Process implications: None of significance, unless high boron doping is encountered.

26. Accomplished: Proof that oxide defect densities are not associated with dislocation densities or stacking faults pre-existing in the substrate. Process implications: Adjustments in substrate crystal perfection, or epitaxial deposition perfection, will not avail in improving oxide defect densities, probably because oxide defects generally are at least a

thousand times larger than the substrate crystal imperfections. More recent work indicates that macro defects in the substrate may determine the loci of subsequent oxide rupture.

27. Accomplished: Demonstration that particulate contamination on silicon wafers, unless exceedingly dense or reactive, does not contribute significantly to oxide defects. Process implications: In process lines where an oxide defect problem exists, the origin of the problem probably need not be sought in air particle counts or potential dust deposits on wafers prior to oxidation. Other wafer contaminants of a more adherent character, however, may be contributing factors. The above recommendation should not be construed as suggesting the relaxation of general cleanliness standards. In photolithographic procedures, for example, ambient dust may become a source of "artificial" dielectric defects created in subsequent etching steps. The essential purpose here is to rank failure sources according to their relative probability in order to save costly engineering time in real situations.

The above experimental observations were compiled on the basis of their more or less direct relevance to process techniques. Many additional experiments, however, were directed toward questions of mechanism which, if properly answered, might provide direct, logical process improvements. Some of the more important observations are especially pertinent to the successful evolution of large scale integration because they deal with the physical nature and origin of oxide dielectric defects. These are summarized below:

1. Accomplished: By replicate electron photomicrography, the detailed definition of the morphology of oxide defects identified independently by electrophoretic decoration. Mechanism implications: Pileups of oxide at the defect site (see Figure 1) suggest a process of compressive upheaval.

2. Accomplished: Demonstration of initial (virtual) defect densities of the order of 100 to 1000 per cm^2. Mechanism implications: Suggests an initial distribution either of substrate surface irregularities or of process induced inhomogeneities.

3. Accomplished: Proof of a kinetic anomaly at the initiation of oxidation. Mechanism implications: Initial distribution of defects may be oxidation rate dependent.

4. Accomplished: Demonstration of a typical defect decay rates versus growth in oxide layers of 750 Å or less. Mechanism implications: Not clear, but suggests manipulation of oxidation rates during the first few hundred Å of growth may have a controlling effect on subsequent growth.

5. Accomplished: Demonstration that oxidative precleaning of wafers (with HNO_3) prior to oxidation tends to reduce defect densities except in the very thin oxide range. Mechanism implications: This was first regarded as an indication that moderation of the initial oxygen diffusion rate would become an important defect control parameter. However, see below.

6. Accomplished: Special nonoxidative precleaning techniques equal to oxidative treatments in reducing defect densities and superior in the very thin oxide range. Mechanism implications: Initial diffusion rate (or thin oxide distribution) is not an important control parameter, but oxidation rate control still may be important on the basis of achieving and initial "equilibrium" distribution of oxide.

7. Accomplished: A chemical polish pretreatment with HCl which tends to reduce defect densities. Mechanism implications: Present results are not yet quantitative but indicate that macroscopic promontories (of the order of one micron) may be substrate features that determine subsequent oxide defect sites.

Other accomplishments on this program are related to the accumulation of information associated with process techniques or with the process origins of component reliability problems. As such, these compilations are of more general applicability to process problems than the discrete observations derived from experimental studies as outlined above. The information in these compilations is derived in part from previous failure analysis programs at Autonetics and in part from the current literature. They are summarized briefly below:

1. Accomplished: "Instruments for Failure Analysis" (Appendix J). Process implications: Tabulation provides instrumental techniques applicable to the examination of component abnormalities and failure modes. The compilation should be of particular assistance to management decisions required in initiating failure investigations in established processes.

2. Accomplished: "Thermodynamic Analysis of Ambient Gas Effects" (Appendix H). Process implications: Useful in settling questions of materials compatibility, particularly at the design stage, by specifying, among those materials in most common use, those gas-solid interactions which are, and those which are not, thermodynamically allowed. Also useful in discovering or predicting possible slow reactions that may contribute to long-term drift.

3. Accomplished: Comparison of dielectric defects in wafers from three major vendors.

4. Accomplished: Testing of the special wafer pretreatment in a device pilot line operation.

5. Accomplished: Evolution of new techniques for analysis of silicon oxide impurities. Development of a "spinning disc" method for oxide analysis.

6. Accomplished: Completion of failure analysis on approximately 200 various electronic devices submitted by NASA during the program.

It is clear that the observations and conclusions enumerated above pertain to a still vigorously evolving technology. Also obvious is the corollary fact that reliability and process control problems will continue to abound in such a dynamic situation. One of the more important problems, and an item of particular concern to this program, is the reproducible achievement of the compositional uniformity and physical integrity of dielectric layers. Once this objective is achieved, the foundation for large scale integration will have been laid. It is believed that significant progress in this direction has been made and that further efforts will be extremely rewarding. On a more general scale, however, there is no doubt that new problems will arise and that constant vigilance should be maintained for their detection and ultimate correction.

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SILICON OXIDE DIELECTRIC DEFECTS

Preliminary Evaluations

The objectives of this effort were to discover why structural defects are produced in thermally grown oxides and to learn how they may be prevented. In order to reach these objectives it was first necessary to develop a tool (described in Appendix A) for the reliable location and identification of oxide defects. This technique was then successfully utilized to isolate those process and structural considerations which contribute significantly to increased defect densities. Early program results confirmed that the inherent thermal mismatch between silicon and silicon dioxide was a significant cause of oxide defects and provided a lower limit of defects which could not be reduced by processing changes. It was later determined that one of the most critical process related factors is the initial condition of the silicon surface in terms of cleanliness and smoothness. As a result, an improved surface preparation technique was developed which significantly reduced defect densities.

One of the most frustrating and widespread problems in planar technology is that caused by dielectric defects, or "pinholes," in oxide layers. The characteristic failure mode introduced by oxide defects is an electrical discharge through the defect from an overlying metallization to the substrate. The metallization need not fill the hole for failure to occur; plasma breakdown can occur in the intervening space. In the case of very small diameter holes, the discharge current may not be large enough initially to constitute a failure. But redistribution of metallization throughout the hole as a result of prolonged plasma discharge ultimately may create a much more highly conductive path and a clearly defined failure. This supports the fact that not all pinhole failures are recognized as such at initial burn-in or early systems test stages but show up later as long term effects in the field. The importance of eliminating this processing problem is clearly evident, not only for high reliability guidance systems, but also for increasing component yields, particularly in the case of LSI and MOSFET gate oxides.

Although numerous remedial innovations in materials and process techniques have been attempted, no reliable solution to this problem has yet been found. Because of the general convenience and superiority of thermally grown oxides for most masking and passivating purposes, and because this application of silicon dioxide has been successfully optimized in most other respects, it seems important to take full advantage of these characteristics by determining the process requirements needed to remove this remaining major problem in its use. During this program a comprehensive evaluation of the available literature was made and utilized where possible. A summary of this information is given in Appendix K.

Initial activity on this portion of the program sought to relate the origin of dielectric defects to various process factors and structural considerations. These results may be summarized as follows:

1. Factors tending to increase dielectric defects.
   a. Extended processing (generally)
   b. Higher compressive stress in the oxide

c. Embedded lapping grains in the substrate

d. Superficial HF etching

e. Abrupt oxide steps

f. Thermal cycling

g. Mechanical wiping

h. Removal of back oxide layers

2. Factors tending to decrease dielectric defects.

a. Growth of oxide to higher thicknesses

b. Chemical etch of initial wafer

c. Pyrolytic oxide, uniformly applied and properly densified

d. Additives tending to reduce bond strain in silica glass

e. Addition of steam to oxidation process gas

The results noted above are consistent with a compressive stress model as the principle source of dielectric defects in oxide layers. The compressive stress in the oxide layer is introduced during cooling from the oxidation temperature as a result of an approximately tenfold mismatch in thermal expansion coefficients between substrate and dielectric. This model was confirmed in a number of subsequent experimental observations. Replicate electron microscopy of a known defect revealed oxide outcroppings suggestive of a compressive stress relief process. Measurements of the compressive stress gave values of the order of 4×10^4 psi. Quantitative comparison of oxide defect densities before and after cooling to room temperature demonstrated that the bulk of the defects (90 to 98 percent) were introduced during the cooling process. Removal of one oxide layer from a wafer introduced a significant warping of the wafer which resulted in an increase in the measured defect population in the remaining oxide layer.

A tool developed on this program for locating and identifying oxide defects is based on a functional test originated by James Lytle of Westinghouse. This test, known as "Electrophoretic Decoration," is particularly applicable to wafers in the beginning stages of manufacture. The test utilizes the oxidation of a metal anode to form positively charged colloidal particles which are propelled through an organic electrolyte toward cathodic sites on an oxide coated silicon wafer situated below the anode. The accumulation and discharge of the colloidal salt particles around oxide defect sites occurs as a result of electron transfer through the defects from the negatively charged silicon wafer. Thus the functional mode of the test is identified with the failure mode sought. The accumulated insoluble matter surrounding each defect serves as a many-fold magnification of the defect location which, for documentary purposes, is readily photographed at low magnifcation. (A detailed description of the test developed is given in Appendix A.)

Electron photomicrographs (Figure 1) showed pile-ups of oxide layers at defect sites, thereby indicating compressive stress in the oxide as the major cause of defects. This idea was confirmed by comparing oxide defect densities existing at the oxidation temperature with those existing after cooling. Briefly, the technique consists of terminating an oxidation with a short HCl etch which attacks any exposed silicon (Figure 2), producing an etch pit at each defect site. After cooling the additional defects are located by electrophoretic decoration (Figure 3). In an oxide layer grown to 8000Å the ratio of defect densities before and after cooling was found to be 1:195 (Appendix B).

The approaches to continued investigation on this program consisted of examining in detail the inhomogeneities in oxide distribution evidently present at the initial stages of oxidation using the techniques described above. Experiments have shown that a significant number of defects may exist at the processing temperature after only a brief oxidation period, thus predisposing oxides to a distribution of thin spots at later stages of oxidation. It is postulated that a portion of these thin spots yield to the compressive stress produced on cooling and that the remainder constitute the latent defect sites opened up by light etching in hydrofluoric acid. It is further postulated that if initial oxidation irregularities could be removed through appropriate process control the finished oxide layers would be free of thin spots and capable of withstanding the existing stresses without rupture.

The following mechanism research discussion indicates that this technique has been used successfully on two kinds of investigations. The first investigation is an evaluation of oxides from various sources for silicon wafer lots oxidized to 10,000 Å by three different processors. The second investigation assesses the effect of various wafer pretreatments, reflecting various methods of preparing the wafer prior to oxidation and yielding thereby essential process control information.

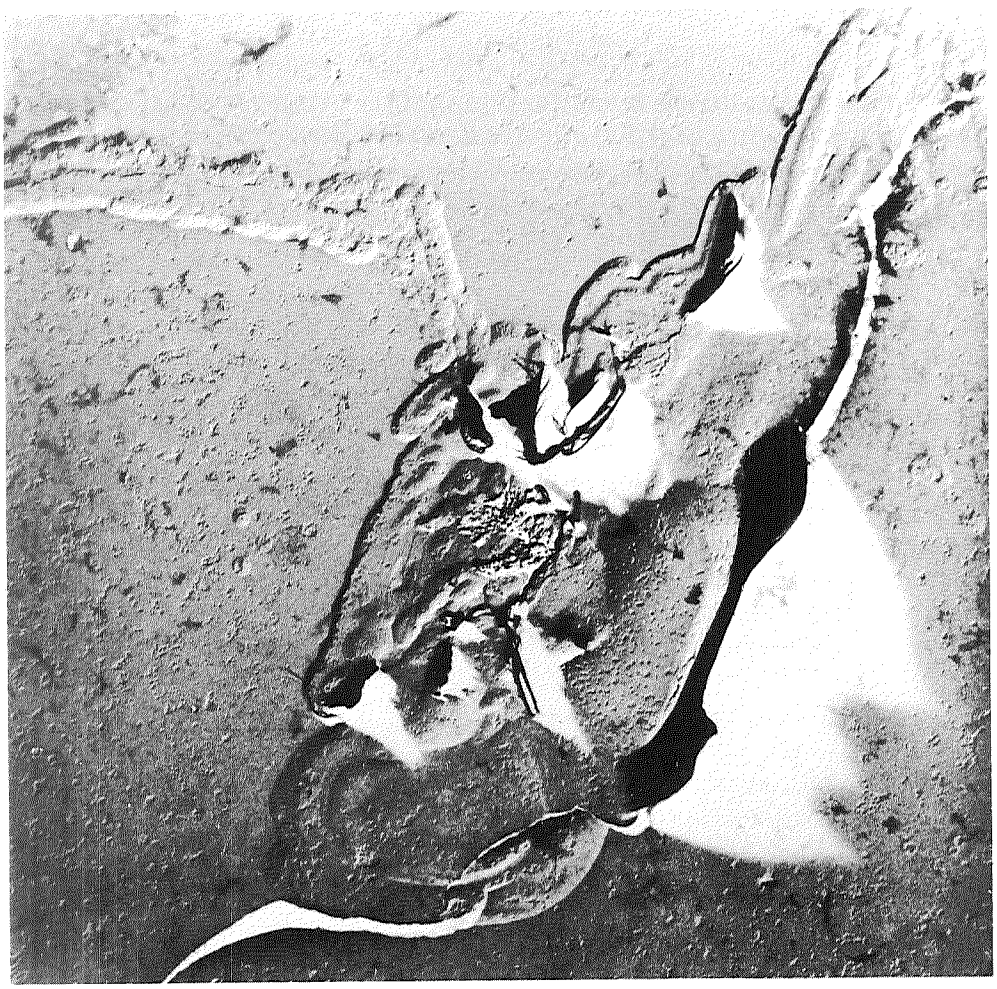
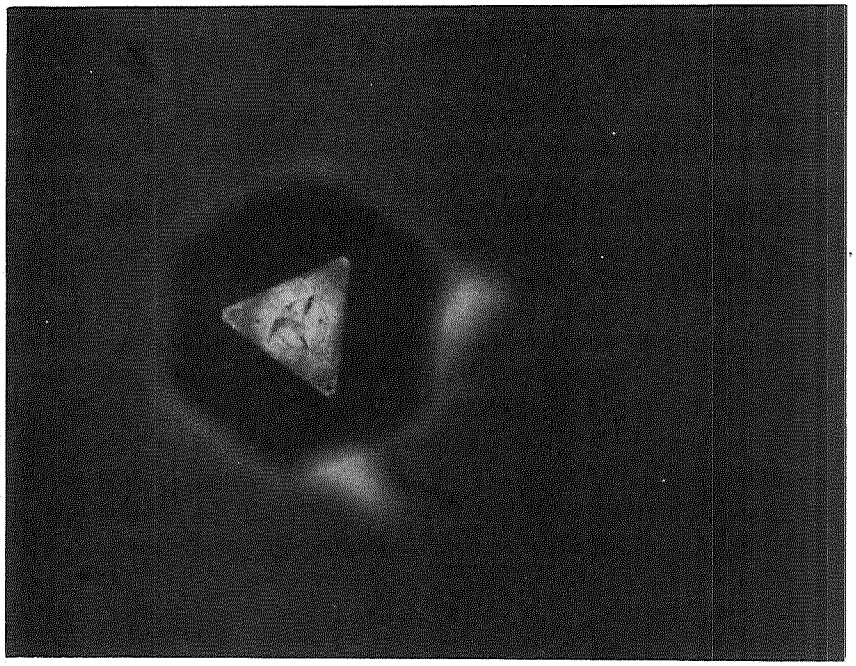
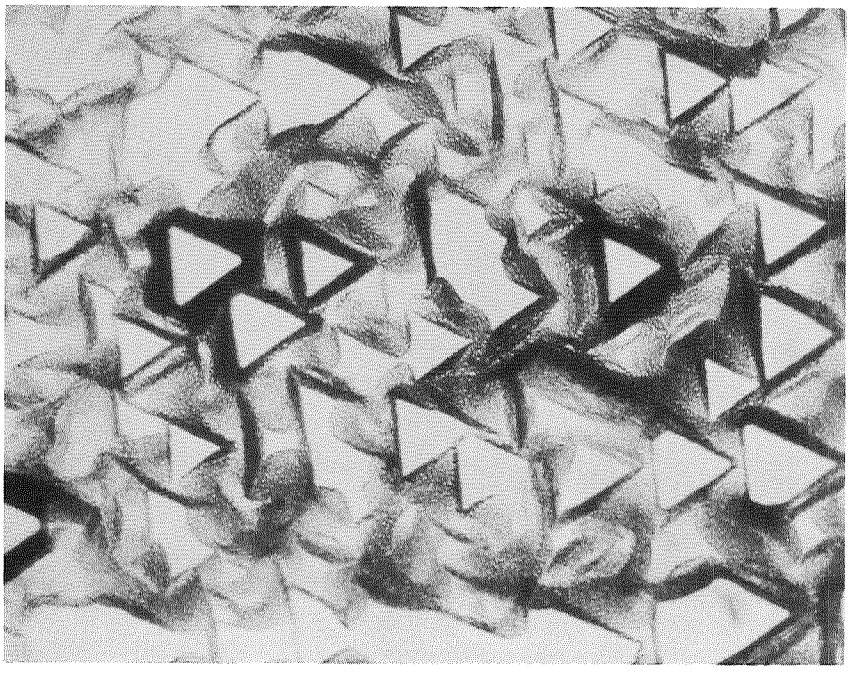


Figure 1.-Electron Photomicrograph of Replica of an Oxide Defect (Black Region)
Approximate Length: Twelve Microns



a. Silicon Etching of Oxide Defect Site



b. Etch Pattern of Unoxidized "Control" Wafer

Figure 2.-High Temperature HC1 Etching Test

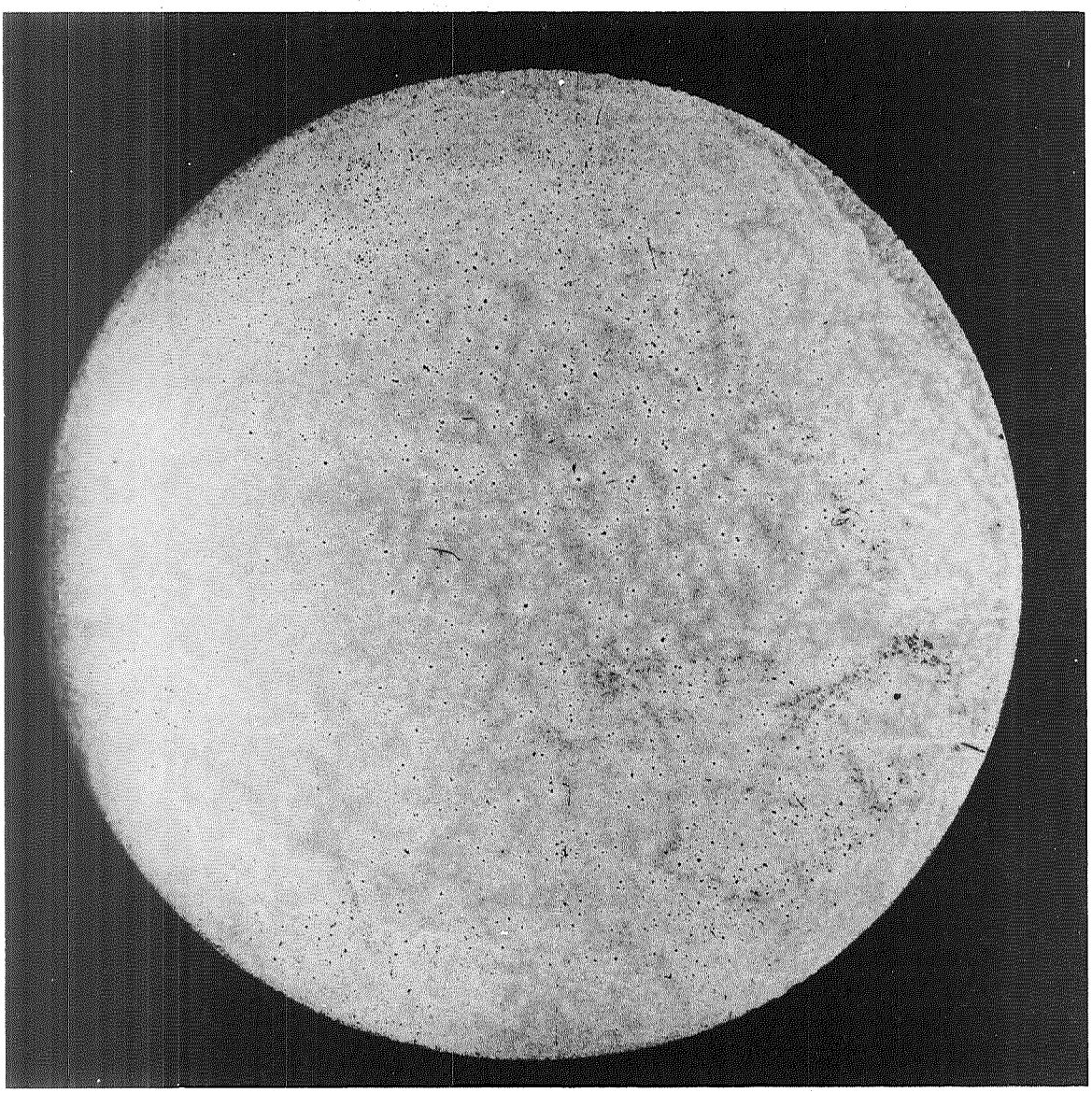


Figure 3.-Electrophoretically Decorated Wafer of Very High Oxide Defect Density

Effects of Oxide Thickness and Stress

A series of experiments were conducted in an attempt to determine the mechanism and thus the origin of oxide dielectric defects. As previously discussed, tests conducted in this laboratory and confirmed by other work established beyond reasonable doubt that the origin of physical forces were due to the thermal mismatch compressive stress in the coated oxide. However, no direct indication of the local factors contributing to their formation was known.

Additional experiments were undertaken to examine in detail the kinetics of the oxidation process. Investigations were conducted to compare defect densities at no stress (before cooling), at full stress (after cooling), and at partial stress relief (after removal of the back oxide layer). These data are listed in Table I and Figure 4 for a series of oxide thicknesses. Conventional oxide growth technique was used (N_2:245 cc/min; O_2:245 cc/min passed through water at slightly less than 100 C; temperature: 1180 C) followed by HCℓ-He etching before removal from the growth zone. Defect densities were evaluated by standard etch pit and decoration counts. The exponential decrease in the number of defects with oxide growth is apparent from Figure 4. Decay of this number, N, may be expressed in terms of layer thickness

$$N = N_z e^{-\phi z} \tag{1}$$

where N_Z is the preexponential factor (ordinate intercept) and ϕ is the decay factor. Decay factors appropriate to Figure 4 are 2.22, 1.08 and 0.83 respectively for no stress, full stress, and partial stress.

The decay factors followed an exponential law and were largest prior to wafer cooling (unstressed condition) and smallest after warping the wafer by removal of one oxide layer. The general nature of these results indicated the existence of latent defects in the oxide prior to cooling which were progressively strengthened and rendered less vulnerable to rupture as oxide thickness was increased. The assumed presence of such latent defects, however, implied the existence of structural or distributional irregularities in the oxide-substrate system introduced either before or during the oxidation process.

The existence of a virtual defect density (N of Eq 1) of the order of $10^3/cm^2$ is significant. However, one must still assume a very large defect density at some small $t > 0$ which increases exponentially with thinner oxides. This problem is especially critical to MOSFET technology where gate oxides of 1000 Å, or less, are generally required. It seems more important, therefore, to understand the physical basis for the virtual defect density, so that it can be manipulated downwards, rather than attempting to increase defect decay factors.

TABLE I
CORRELATION OF DEFECT DENSITIES WITH VARIOUS STRESS CONDITIONS

Oxide (Å) Thickness	Run No.	Oxidation Time, t (minutes)	$t^{1/2}$	Defects: Per cm^2 *		
				No Stress (vapor etch pits)	Full Stress (decorated)	Partial Stress (decorated)
1720	A	5	2.24	39	161	292
1995	B**	10	3.16	10	151	190
2590	C	15	3.87	3.0	101	142
3125	D	20	4.47	1.5	33	43
2945	EJ	25	5.00	1.2	55	93
3760	I	25	5.00	1.2	26	40
4010	F**	40	6.32	0.3	9	42
5325	G	60	7.81	0	12	29

*All entries represent an average of four wafers
**Runs selected for initial Proficorder study

Silicon Surface and Initial Oxidation Aspects

Further investigation revealed that a kinetic anomaly in oxide growth rate existed at the beginning of oxidation (during the first 300 to 600 Å) after which a square root law characteristic of a diffusion controlled process was followed. Attention, therefore, was focused on the beginning phase of oxidation in the expectation that moderation of the reaction kinetics at this point might remove an assumed distributional irregularity in the oxide and thereby reduce the latent defect density. Such a moderation was achieved (and kinetically demonstrated) by application of an oxidative pretreatment (using hot nitric acid) which developed a very thin oxide layer on the wafers prior to high temperature oxidation. A significant drop in the latent defect density (extrapolated to oxidation time zero) was observed as a result of this treatment.

Accordingly, wafers were pretreated in a manner designed to produce diffusion attenuation layers on the surfaces. These layers consist primarily of silicon dioxide in the 200 Å or less thickness range produced by a wet chemical method consisting of treating the wafers with HF (to remove old oxide), KOH solution (to remove residual fluoride), and hot concentrated nitric acid (to remove residual KOH and initiate uniform oxidation). Each step was followed by thorough rinsing with distilled water. The exact nature of the layers so produced still is unknown. Boundaries in such layers

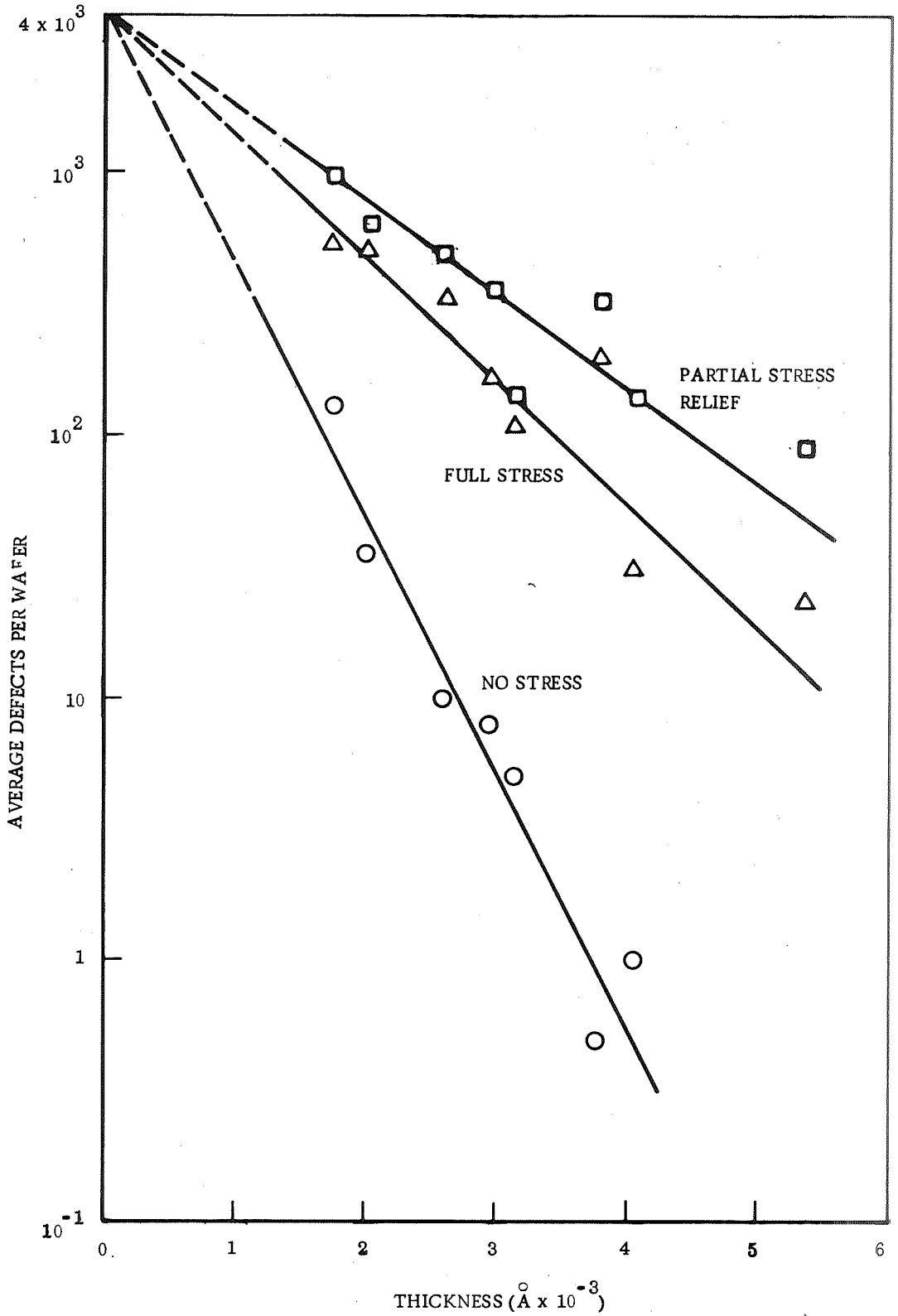


Figure 4. Defects as a Function of Oxide Thickness For Various Stress Conditions

produced by controlled (masked) HF etching are readily revealed by moisture condensation from a humid environment. Attempts to measure the thickness of the layers by Proficorder and Tally-Surf tracing, and by interferometry, however, failed. Although the layers are suspected of being a porous and partly hydrated silicon dioxide, the possibility of a small component of nitride cannot be ruled out.

High temperature oxide defect densities on wafers so treated (termed hereinafter "oxidative precleaning") were found to be practically nonexistent, even for oxidation time as short as 2.5 min. Room temperature decorated defects, however, were significant. The corresponding defects densities are shown as Set A in Table II.

Nonoxidative vs Oxidative Cleaning

It was not clear from these results whether the decrease in defect density was due solely to the initial oxidative attack on the substrate or to an additional "cleansing effect" caused by the nitric acid treatment. Therefore a "nonoxidative" precleaning technique was developed. In this case the wafers were "nonoxidatively" precleaned using a swabbing technique with HF, preceded and followed by water and alcohol rinses.

Slow oxide growth was achieved by limiting the oxygen to 4 percent of the process gas composition and by reducing the temperature of the water reservoir. The oxidation temperature, however, remained at 1180 C.

All data were taken as a function of oxide thickness grown, as measured (in most cases) by Proficorder tracing. All defect readings are recorded on a cm^{-2} basis. In addition the ratio of etch pits (high temperature defects) to decorations (room temperature defects) were computed for each series, where applicable, as a further test of internal consistency. The "nonoxidative" results are shown as Set B in Table II.

Comparison of Sets A and B in Table II plotted against oxide thickness (Figure 5) indicates that there may be little or no difference in how the initial oxidation rate is moderated. The effect of both on the virtual defect density appears to be significant. Compared with earlier results, which yield a virtual defect density of $\sim 4 \times 10^3$ per wafer ("Full Stress" curve, Figure 4), or $>10^3$ cm^{-2}, the present treatments yield an order of magnitude improvement ($\sim 1.1 \times 10^2$ cm^{-2}). Although the defect decay rate is somewhat smaller than that applicable to Figure 4, this potential modification in process technique may have important implication for thin oxide applications, such as MOS gates. At 1000 Å oxide thickness, for example, Figure 4 yields a density of 410 defects cm^{-2} (taking the wafer area as 3.2 cm^2) while Figure 5 yields a density of 70 cm^{-2}.

This result was taken as potential confirmation that the assumed initial inhomogeneities associated with latent defect densities were, in fact, related to the observed kinetic anomaly at the beginning of oxidation. Further attention was given, therefore, to the effects of the various process parameters on defect densities in the first few hundred Angstroms of growth. It was shown that the nonoxidative precleaning treatment was superior to the oxidative treatment in reducing defect densities in this

TABLE II
DEFECT DENSITIES AS A FUNCTION OF PRETREATMENTS AND GROWTH RATE

Set	Wafer Precleaning	Water Temperature (Deg C)	Oxide Growth Rate	Oxide Thickness (Angstroms)	Etch-Pit Density (cm^{-2})	Decoration Density (cm^{-2})	Etch-Pits/ Decorations
A	Ox.	95	Normal	1300		67.0	
	Ox.			2000		54.0	
	Ox.			2700		27.6	
	Ox.			3000		23.5	
	Ox.			4100		15.7	
	Ox.			5000		12.6	
B	Non-Ox.	34-35	Slow to 400 Å then Normal	1600	0	47.4	
	Non-Ox.			1800	0.079	43.6	0.0018
	Non-Ox.			2800	0	37.7	
	Non-Ox.			3600	0.079	20.0	0.004
	Non-Ox.			4600	0	11.3	

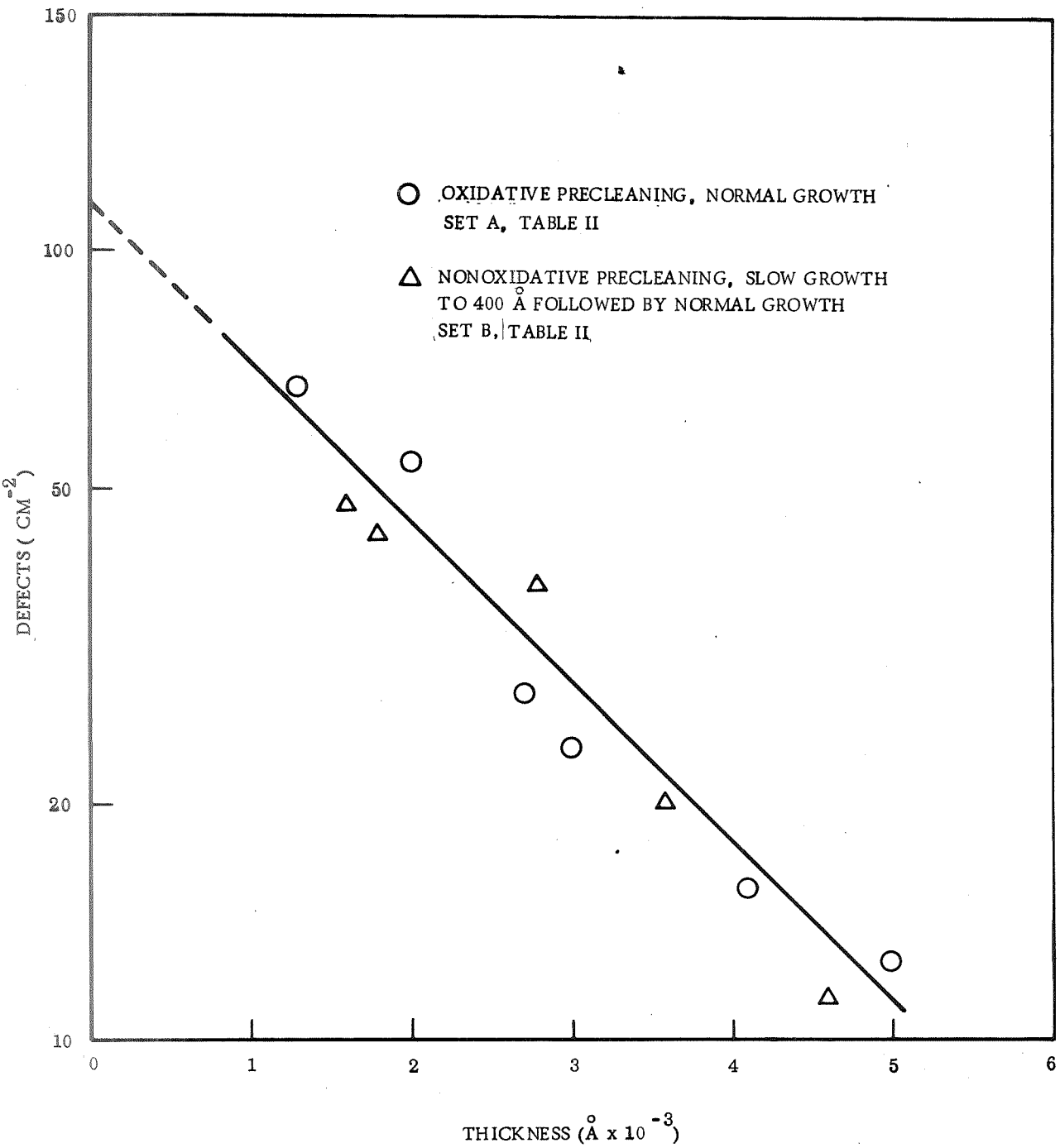


Figure 5. Comparison of Oxidative Precleaning With Nonoxidative Precleaning Plus Initial Slow Growth

region. It also was shown that initial slow thermal oxidation after the nonoxidation precleaning produced additional oxide improvement if dry, rather than wet, oxygen was used. It was possible at this point, therefore, to formulate a tentative set of optimum process conditions for oxide growth. These included an initial nonoxidative precleaning of the wafers (using a wiping technique with HF, as previously described) and an extremely slow initial growth of thermal oxide using dry oxygen, followed by conventional growth with moist oxygen.

In attempting to adduce a physical basis for the effects described above, it became evident that the controlling process parameter might be one of equilibration rather than of oxygen diffusion attenuation. That is, the inhomogeneities determining defect loci might as well be purely structural instead of being confined to the result of kinetic irregularities in the initial oxide distribution. In either case, then, the initial slow oxidation might provide the necessary conditions for the equilibrium distribution of either oxide or substrate material, whereas oxygen diffusion attenuation alone would affect only the oxide distribution. The participating physical irregularities of the oxide-substrate system, regardless of origin, would be in the submicron range; e.g., a significant fraction of the oxide layer thickness and several orders of magnitude greater than the substrate lattice parameter. The appearance of a defect in the oxide layer (after cooling) then would become a function of the particular local stress conditions associated with the radius of curvature of the presumed structural irregularity. As more oxide is grown the ratio of the radius of curvature to the oxide thickness will decrease exponentially with oxide thickness, thus accommodating the corresponding disappearance of dielectric defects. In addition to accounting for the localization of oxide defects a model of this type is more susceptible to physical verification.

The nitric acid pretreatment would be expected to attack microscopic promontories on the silicon surface more rapidly than surrounding smooth areas, thus reducing their effectiveness in creating localized stress anomalies in the subsequent oxide layers. Reconsideration of the "nonoxidative" pretreatment discloses that the opportunity for limited oxidation occurs here, too, because the HF wiping procedure is done in the presence of air. In other words, the treatment is nonoxidative only in the sense that it leaves no additional oxide layer on the silicon surface. The wiping process therefore can be regarded as a chemical lapping in which promontories are more susceptible to erosion than surrounding flat areas. The HF serves the familiar function of removing silicon dioxide as it is formed.

HCl Wafer Pretreatment

The above concept was subjected to further test by applying an HCl vapor etch to wafers (four sets of four each) immediately prior to oxidation.* The decoration densities resulting from the inclusion of this treatment are compared in Table III with

*This treatment differs from one investigated earlier at the Qualification and Standards Laboratory, NASA-ERC, where HCl was admitted during oxidation in an attempt to modify the composition and structure of the oxide layers as they were grown.

a similar set in which the HCl pretreatment was omitted. It is clear that an improvement was thereby achieved (in the 500 Å thickness range) even though both sets of wafers also were pretreated by the chemical lapping ("nonoxidative") method.

Continuing further with the equilibration approach, tests were designed to maximize the redistribution of assumed structural irregularities both in "bare" silicon and in very thin initial oxide layers using various heat-soak periods at the oxidation temperature (1180 C). Because this temperature is well above the set temperature of silica (1000 C) it was felt that the oxide would be sufficiently plastic to conform to any interfacial energy-reducing material migrations. In consideration of the number of process variables of interest a simple matrix was designed in which the normal oxidation periods were given only two values (5 min and 20 min, Table IV). These process variables included a comparison of the effects of initial oxide layers produced by oxidative precleaning technique with those produced by initial thermal oxidation (using 4 percent dry O_2 diluted with helium) (sets C and D), time of heat soak in nitrogen (two values) (sets E and F), and comparison of dynamic with essentially static nitrogen flow during heat-soak (sets D and E). A control omitting the major variable was included with each run. Each charge consisted of four wafers whose etch-pit and decoration counts were averaged to yield the data in the last two columns of Table IV.

TABLE III
EFFECT OF HCl PRE-ETCHING ON
SUBSEQUENT OXIDE DEFECT DENSITIES

Set	Wafer Precleaning	HCl Pre-treatment	Water Temperature (Deg C)	Oxygen Conc. (Percent)	Oxide Thickness (Ångstroms)	Decoration Density (cm^{-2})
A	Non-Ox	None	50	4	470	860
	Non-Ox	None	50	4	480	390
	Non-Ox	None	50	4	600	314
	Non-Ox	None	50	4	650	121
B	Non-Ox	1 min	50	4	500	201
	Non-Ox	1 min	50	4	500	144
	Non-Ox	1 min	50	4	510	278
	Non-Ox	1 min	50	4	560	46

TABLE IV
HIGH TEMPERATURE HEAT-SOAK EFFECTS ON SUBSEQUENT DEFECT DENSITIES

Set	Wafer Precleaning	Thermal Pre-Oxidation (Min)	Heat-Soak in N_2 (Hrs)	N_2 Flow (cc/min)	Normal Oxidation (Min)	Oxide Thickness (Ångstroms)	Etch-Pits (cm^{-2})	Defect Decorations (cm^{-2})
C	Ox	None	2	480	5	1400	9.4	161
	Non-Ox*	None	2	480	5	1400	9.3	61
	Ox	None	2	480	20	3000	2.5	29
	Non-Ox*	None	2	480	20	3100	3.1	12
D	Non-Ox	5	2	480	5	1300	0.63	37
	Non-Ox*	None	2	480	5	1550	8.06	31
	Non-Ox	5	2	480	20	3200	0	19
	Non-Ox*	None	2	480	20	2900	0.08	4.4
E	Non-Ox	5	2	10	5	1700	0.63	17
	Non-Ox*	None	2	10	5	1400	----	15
	Non-Ox	5	2	10	20	3000	1.57	15
	Non-Ox*	None	2	10	20	3100	0.24	9.4
F	Non-Ox	5	16	10	5	2200	1.8	10.3
	Non-Ox*	None	16	10	5	1200	18.3	82
	Non-Ox	5	16	10	20	3300	0	5.7
	Non-Ox*	None	16	10	20	2700	0.6	15.7

*Control: Initial thin oxide omitted

The results obtained are generally superior to the best data previously obtained by HNO_3 treatment (Figure 5), with the exception of the first value of set C. In sets C, D, and E the controls (in which the introduction of a first thin oxide layer was omitted) consistently yielded lower defect densities, whereas the reverse is true for set F in which the heat-soak period was increased to 16 hrs. These results appear to indicate a substrate surface redistribution process at 1180 C which is hindered by the presence of a thin oxide layer unless sufficient time is allowed for the highly viscous accommodation by the oxide. In comparing the results of sets C and D the oxidative precleaning again is shown to be inferior to the HF lapping and appears to be sufficient reason for abandoning further work with the nitric acid pretreatment. Analysis of sets E and F shows a slight improvement from a prolonged heat-soak, set F being superior to all previous runs. Comparison of sets D and E indicate that a slow nitrogen flow rate results in fewer defects than the normal flow rates used throughout the bulk of these investigations. An unidentified component of the nitrogen source may contribute to this effect. The relatively high defect densities from the control runs of set F, where the heat-soak was relatively prolonged, further suggests this possibility. In conclusion, it appears that treatments tending to promote greater smoothness of the substrate surfaces, as well as prolonged periods of equilibration to enhance initial oxide uniformity, may have an important bearing on the reduction of oxide defects.

In continuing experiments all wafers were precleaned by HF wiping, as described previously, and all were exposed to a five-minute treatment with four percent dry O_2 immediately prior to a 16-hour heat-soak in nitrogen. Process variables and resulting defect counts are summarized in Table V.

TABLE V
EFFECTS OF HCl PRETREATMENT AND HEAT-SOAK ON DEFECTS

HCl Pre-treatment (Min)	N_2 Heat-Soak (Hrs)	Normal Oxidation (Min)	Oxide Thickness (Angstroms)	Defects (cm^{-2})
None	16	10	2600	12.3
None	16	40	4500	6.0
None	16	80	6100	3.7
1	16	5	1900	15.8
1	16	20	3300	5.7
2	16	5	2300	6.4
2	16	20	3200	4.0

A log plot of the first three defect counts yields approximately 1 defect/cm^2 when extrapolated to 10,000 Å, which compares with results from Vendors B and C wafers grown to 10,000 Å (see below). The second set of data, which includes a one-minute HCl treatment prior to the dry O_2 preoxidation, when similarly plotted yields less than 0.1 defects/cm^2 at 10,000 Å. The effect of the HCl appears to be to cause a significantly higher defect decay rate with oxide thickness as a result of reducing initial wafer surface irregularities. Increasing the HCl treatment to two minutes produced a further reduction of defect densities as shown in Table V.

The results are clearly superior to those obtained with a shorter HCl pretreatment. Extrapolation to 10,000 Å again yields a defect density of the order of 0.1/cm^2.

This HCl pretreatment, however, was distinctly less than optimum because it introduced clearly visible (at 100 X) etch pits in the wafers. Etch pit sizes lay in the micron and submicron range. A comparison of etch pit counts with defect counts revealed a distinct correlation as shown in Table VI.

The only anomalous results in this progression are the ones starred. This is the first known direct evidence that depressions in the silicon surface, in the micron and submicron range, give rise to subsequently grown oxide irregularities which are incapable of withstanding the compressive stress introduced on cooling from the oxidation temperature. It is well known that vitreous silica is remarkably resistant to compressive stress but yields readily to tension and shear. The abrupt changes in oxide curvature caused by the etch pits introduce tension and shear vectors as resultants of the existing compressive stress.

TABLE VI
OXIDE DEFECTS AS A FUNCTION OF PREVIOUSLY INTRODUCED ETCH PITS

HCl Etch Pits (per wafer)	Ultimate Defects (per wafer)
72	20
77	45*
82	27
98	34
116	16*
125	40
174	58
233	115

Dielectric Defects - Vendor Survey

Defect analyses of 10,000 Å oxides prepared by three manufacturers was performed for comparison with the Autonetics laboratory results obtained. The results obtained are summarized in Table VII.

The superiority of the Vendor A product is clearly evident with 80 percent of the wafers having no defects at all. A Vendor A Representative indicated to Autonetics that its oxidations were preceded by an HCl etch; no other vendor made this claim. In view of the results tabulated in the preceding section of this report it seems likely that neither Vendor B nor Vendor C employ a pre-etch with HCl. The defect levels of the latter two manufacturers are characteristic of those obtained on this program prior to the use of an HCl etch.

Also of interest is the variation represented by Vendor C's lot number 3, indicating a lot-to-lot control problem. This is common to the entire lot, with a standard deviation of ± 1.64 defects/cm^2 (± 46 percent). NASA centers would be well advised to require a test wafer for defect analysis after the first oxidation prior to purchasing planar devices from a given lot. It also would seem prudent for manufacturers to adopt some embodiment of the electrophoretic decoration test (as described in Appendix A of this report) not only to inform themselves of lot-to-lot control problems but also of their standing with the oxide quality of other vendors.

TABLE VII
DEFECT LEVELS IN 10,000Å OXIDES FROM VARIOUS SOURCES

Company	Number of Wafers	Average Defects (cm^{-2})	Wafers With Zero Defects (%)	Maximum Count (wafer^{-1})
Vendor A				
Lot 1	10	0.040	80	1
Lot 2	28	0.057	79	2
Vendor B				
Lot 1	10	0.29	30	9
Lot 2	10	0.69	0	19
Lot 3	10	0.72	10	13
Vendor C				
Lot 1	30	0.73	3.3	11
Lot 2	10	0.55	20	10
Lot 3	10	3.55	0	41

Dielectric Defects - Pilot Line Test

Standard Rel-chip wafers were fabricated on the Autonetics pilot line by three process modifications designated as "Standard," "Interim," and "Experimental." Each modification was represented by 18 wafers which additionally were divided into three pretreatment subgroups of six each comprising standard pretreatment, HF wiping, and HCl pre-etching. Final window opening and metallization was omitted in five out of each set of six wafers and were defect counted by electrophoretic decoration. The sixth wafer was carried through metallization and electrically tested for dielectric breakdown in the capacitor area which was 0.008 in. x 0.008 in. x 1400 Å thick. The wafers contained an average of 435 Rel-chip integrated circuits; all of the IC's on each of the five wafers of each group were defect counted. The results for each process modification and each wafer pretreatment are summarized in Table VIII.

Histograms of the data are presented in Appendix D. The information summarized in the first histograms indicates a "tighter" distribution for the thin oxides of all wafers with a mode of 2 defects per wafer. The thick oxides show a greater spread on the average with a mode also at 2 defects per wafer. (The thick oxide area is of course much larger than the thin oxide layer.) Other histograms in Appendix D show the data for thin and thick oxides as a function of process and pretreatment. The thin oxide distribution by process show a considerable spread for the interim process and thus a possible out-of-control situation. There was also a considerable spread in all of the thick oxide data.

The data summary (average values) shown in Table VIII indicate no significant trends in thick or thin oxide defect density as a function of the variables examined. The additional pretreatments appear to have produced some improvement in the thin (1400 Å) oxide produced by the "Standard" process but this relationship was reversed on the Interim and Experimental process. Both of the pretreatments were accompanied by increased defects on the thick oxides. It appears that more data are needed in order to arrive at statistically significant conclusions. Other factors appeared to be present which confounded the data obtained. This is indicated in Figures 6 and 7 which show respectively a random and nonrandom distribution of defects on two wafers examined.

An attempt was made to compare these data with those previously obtained on this program for three vendor oxides. It was necessary to extrapolate the data since the pilot line oxides were 1400 and 14,000 Å while the vendor oxides were 10,000 Å. By use of the decay constants (slopes) for curves B or C in Figure 8 extrapolation would reveal that the pilot line thin oxides are comparable with Vendors B and C while Vendor A is an order of magnitude better. Also the pilot line oxides were subjected to several thermal excursions not represented in the sample growth of the vendor oxide.

The above results were substantiated by electrical tests on the metallized wafers. Among all capacitors tested not a single electrical breakdown was induced under an applied potential of 100 v. In the present case this amounts to a field of 0.07 v/Å which is about 70 percent of the breakdown strength of sound oxide and considerably higher than fields sustained in normal operation.

TABLE VIII
VARIATION OF DEFECT DENSITIES WITH
PROCESSING AND PRETREATMENTS

Process	Pretreatment		
	Standard	HF Wiping	HCl Pre-etch
Standard			
Thick oxide* (cm^{-2})	1.1	2.9	2.3
Capacitor ** (cm^{-2})	32.4	10.2	13.1
Oxide step (cm^{-1})	0.10	0.09	0.09
Interim			
Thick oxide (cm^{-2})	0.9	0.8	1.7
Capacitor (cm^{-2})	14.8	23.5	52.5
Oxide step (cm^{-1})	0.06	0.15	0.16
Experimental			
Thick oxide (cm^{-2})	0.6	1.0	1.1
Capacitor (cm^{-2})	7.5	8.9	14.2
Oxide step (cm^{-1})	0.02	0.02	0.07

*14,000 Å
**1,400 Å

Terms Used in Table

Standard Pretreatment	Standard Pilot Line cleansing of wafers prior to initial oxidation. (Solvent, HF "rinse" 10 percent dilution.)
HF Wiping Pretreatment	HF experimental technique. (HF swabbing in transverse directions prior to initial oxidation.)
HCl Pre-etch Pretreatment	HCl experimental technique. (Pre-clean No. 1 followed by HCl etching of wafer at oxidation temperature followed by immediate initial oxidation in same furnace.)

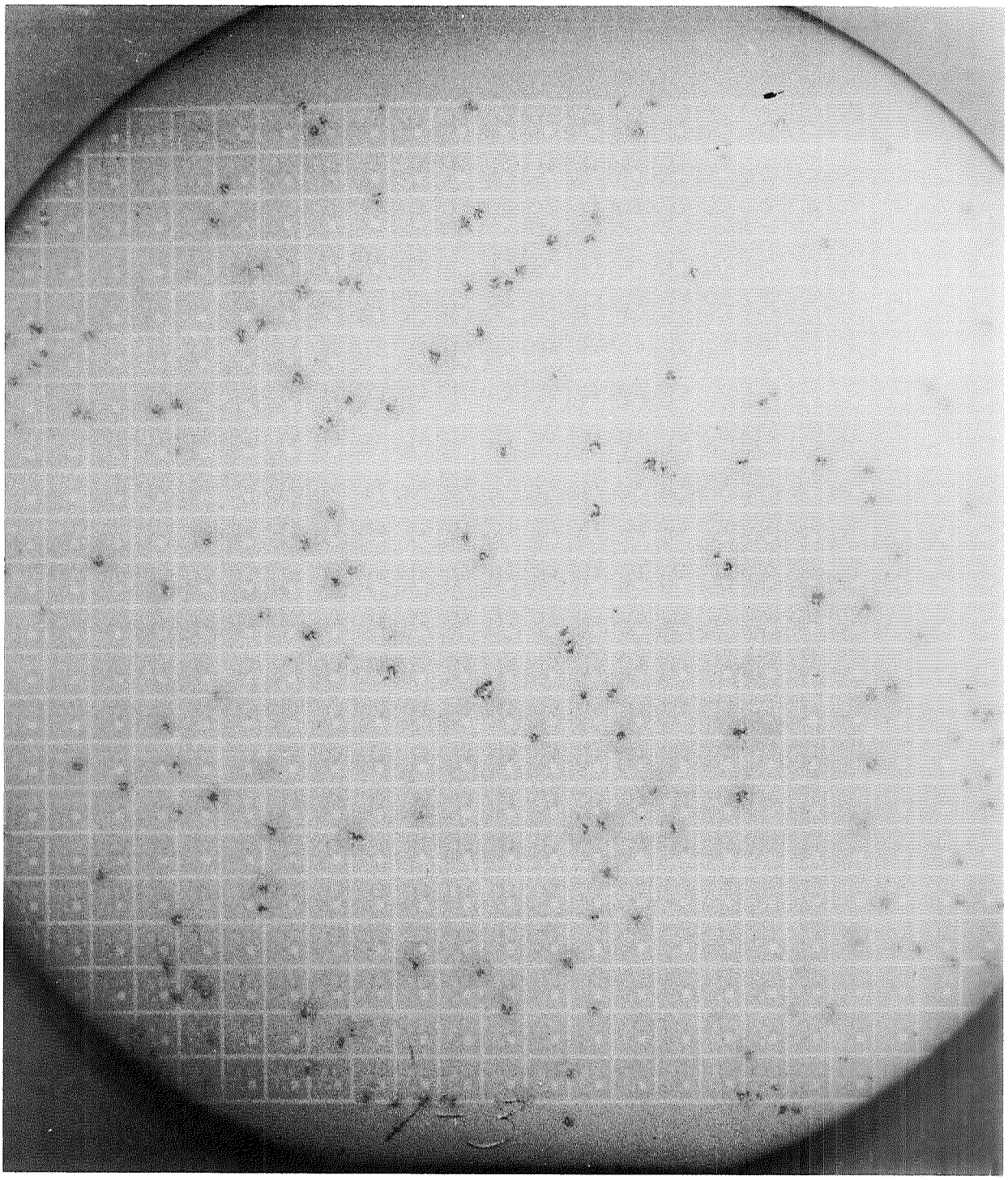


Figure 6. Test Wafer Showing Random Distribution of Dielectric Defects

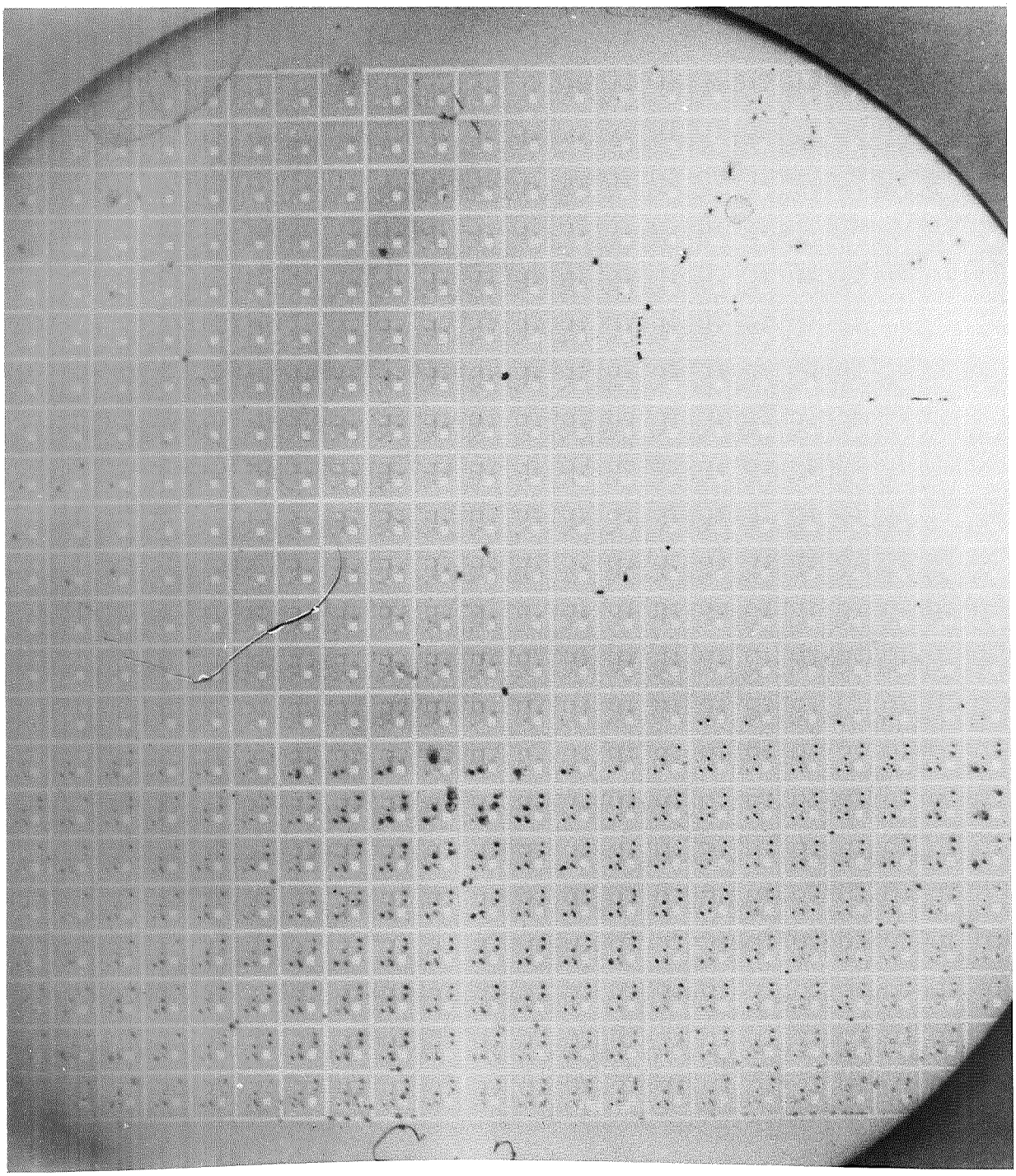


Figure 7. Test Wafer Showing Non-Random Distribution of Dielectric Defects

As observed in the past, a substantial proportion (greater than 50 percent) of the total defects were situated along oxide steps. The linear densities given in Table VII were derived only from the peripheries of the large capacitor regions. It was not determined whether these defects were actually on the step or possibly in a trough of extremely thin oxide believed to be at the base of the step.

Discussion

Figure 8 is a summary of the results obtained, indicating the defect decay curves as a function of oxide thickness for four basic processes. Curve A represents initial wafer treatments as grown early in the program. Curves B and C are subsequent improvements in terms of reduced oxide defects (at low thickness) vs wafer surface pretreatments.

A series of wafers were obtained from three different vendors for comparison purposes. The defects are indicated in the graph at the 10,000 Å level. It is believed that the superiority of vendor A is due to the utilization of a wafer pretreatment similar to that developed on curve C ($HC\ell$ vapor etch).

A special program was also performed to test the developed wafer pretreatment in an actual pilot line operation. The standard pilot line process was compared with two process modifications. The effect of wafer pretreatment on the final oxide integrity was also evaluated. The data obtained at two oxide thicknesses (1400 and 14,000 Å) using a test pattern are also shown in Figure 1. The 14,000 Å data is obviously much higher than any of the other results obtained when extrapolated to comparable thicknesses. These data are comparable, it is felt, since the oxide has been through several thermal cycles which will cause additional defects as determined previously on this program.

The 1400 Å thickness, however, is a regrown area and has seen fewer thermal excursions. These data appear to be comparable with the vendor oxide data except for Vendor A, which is clearly superior. (In this comparison it is necessary to extrapolate using the same decay constant as either curve B or C.)

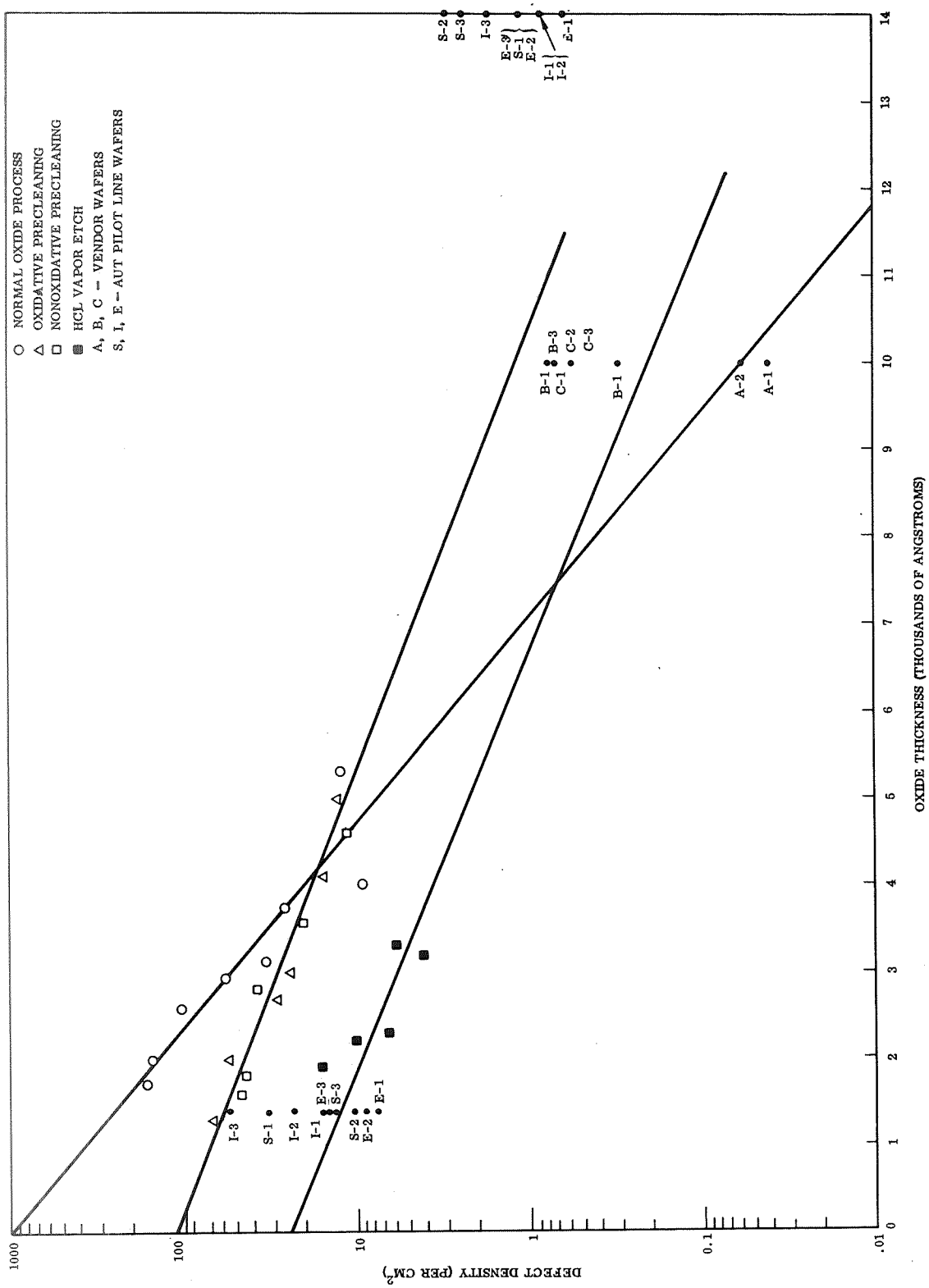


Figure 8. Oxide Defect Dependence on Processing

SILICON OXIDE IMPURITY EFFECTS

Microelectronic device reliability is often reduced through electrical instabilities associated with surface properties. Ionic impurities in the silicon dioxide passivation are well known (Appendix L and Refs 1, 2, 3) to cause electrical parameter drifts during device operation. These impurities can usually be traced to the processing chemicals from device fabrication. An incomplete understanding of the failure mechanisms exists because ordinary chemical analyses of these small area surfaces has been insufficient to detect low levels of impurities. The trend has been toward increased usage of electrical or physical techniques to investigate the nature of these impurities.

During this program an initial evaluation was made of some of the more recent and advanced techniques for potential use including solids mass spectroscopy, Auger spectroscopy, ion microanalysis, and dielectric relaxation. Samples were obtained from a well controlled in-house pilot line facility in terms of both test circuits used for process evaluations and wafers oxidized under various desired conditions. Also possible process origins of oxide impurities were analyzed.

A brief description of the analytical techniques utilized is given below followed by a discussion of the results obtained on the various samples analyzed.

Analyses Techniques Description

C-V Measurements. — A widely used technique for the evaluation of oxide purity is capacitance versus voltage characteristics. The technique has been used on this program to give an initial characterization on various oxide samples. This method involves measurement of the oxide capacitance as the voltage across it is varied. A negative voltage is then applied to the metallization on top of the oxide which drives positive mobile ions toward the oxide surface. This voltage stress is done at elevated temperatures to enable the ions to diffuse more readily. The sample is cooled and capacitance versus voltage data retaken. The shift ΔV in the resulting curve is relatable to the number of mobile charges in the (oxide since this component of the sample capacitance is the only one assumed to vary with this type of stress) by the expression

$$\Delta V = \frac{Q}{\left[\frac{K_o e_o}{d_o}\right]}$$

where:

Q = ionic charge/unit area
K_o = dielectric constant
e_o = permittivity
d_o = oxide thickness

Solids Mass Spectroscopy. — In order to derive ions for subsequent separation and measurement, the solids mass spectrometer uses an RF spark for vaporization and ionization of the solid sample. The ion beam emitted is accelerated by slits and

then passes through an electrostatic field. The ion energy width is restricted by means of an energy defining slit. The ion beam then enters a magnetic field where it is dispersed. Finally each segment is focused at the magnetic field exit in accordance with the mass-to-charge (m/e) ratio.

The sensitivity of the solids mass spectrometer is dependent on the total number of ions reaching the detector. This is related in a reproducible manner to the total number of ions produced, which is also related to the amount of sample consumed by the spark. The total number of ions arriving at the detector (usually a photographic plate) is generally measured in terms of the number of coulombs collected by a charge collector near the detector. Analysis of solids for elemental constituents can be generally performed with detection limits for essentially all elements at approximately the 1 to 10 parts per billion level.

Problems inherent in this technique when applied to thin film layers (i.e., SiO_2) involve the sample removal and penetration depth into the substrate. Techniques to minimize these problems are discussed in the following section.

With an oxide layer 1500 Å thick the detection limit of the mass spectrometer (at 70 parts per billion) is 1.6×10^{15} atoms/cm^3. As the thickness of the oxide layer gets smaller the detection limits increase appropriately. Thus with 1000Å thick oxide, the mass spectrometer detection limit becomes 2.4×10^{16} atoms/cm^3. To get ultimate sensitivity a fairly large surface area is needed. The development of a spiralling spinning sample technique to minimize crater depth and maximize surface sample for the solids mass spectrometer markedly increases (20 - 50 times) the sensitivity. In addition if only one or two elements are of interest rather than the complete spectrum, the use of electrical detection rather than the photographic plate can provide 100 times sensitivity increase.

Ion Microanalyzer. – This instrument combines the operation of a mass spectrometer with that of an ion emission microscope to measure the chemical distribution of elements on a solid surface layer. Ion sputtering is used to produce secondary ions from the surface of the specimen. An electrostatic immersion lens is employed to extract the secondary ion beam and direct it through a special type of mass spectrometer. The mass spectrometer separates those secondary ions which are "characteristic" of a given element or isotope and permits a "characteristic" image of that element or isotope to be formed. The elementary ion images are projected onto an image converter cathode which produces an equivalent electron image. The electron image may be displayed on a fluorescent screen or photographed similar to the way an image is observed with an electron microscope. The spatial resolution obtained is approximately one micron. Because all of the secondary ions do not leave the specimen with the same initial energy, to obtain high mass resolution, it is necessary to use a design permitting both momentum dispersion and energy filtering. The deflection of the beam in the magnetic analyzer provides the momentum filtering. Energy filtering is provided with an electrostatic mirror. After separating ions of selected momentum, the beam is directed onto an electrostatic mirror which is adjusted to reflect only ions with an energy lower than a certain value, thus eliminating ions of higher energy.

The analyzer system provides a mass resolving power sufficient to resolve all the elements of the periodic table, for the type of ionization produced. This technique allows selective removal, by ion sputtering, of angstrom thick layers of material

and thus eliminates or minimizes one of the problems associated with the solids mass spectrometer and electron probe microanalyzer. The resolution in depth of this equipment appears to be between 50 and 100 Angstroms. Because of this unique capability impurity or dopant profiles as a function of distance from the surface can be determined.

Auger Electron Spectroscopy. – Auger electron spectroscopy is a recently developed technique for chemical analysis of solid surfaces. In this method, emission of Auger electrons is stimulated by bombarding the surface of a solid sample with an electron beam of about 3 kev energy. These incident electrons ionize atoms near the solid surface which decay to the ground state either through an emission of X-rays or through ejection of an Auger electron. While Auger and X-ray processes compete, the Auger process generally dominates when the originally ionized level has energy less than about 2 kev. The Auger electron, exhibiting an energy determined by its parent element, may escape into the vacuum without loss of energy, provided that it originates within a few Angstroms of the surface. In the measured energy distributed over all electrons emitted from the surface, one can detect small peaks which correspond to Auger electrons. The location of these peaks in energy is easily related to the elements from which the Auger electrons originate, and thus provide a means of chemical analysis.

Experience has shown that all elements, except hydrogen and helium, can be detected in surface concentrations as small as $10^{13}/cm^2$. For a typical Auger electron escape depth of 10 Å, this corresponds to a bulk concentration of $10^{20}/cm^3$, or about 1000 ppm.

The Auger technique differs from the X-ray microprobe technique in two different respects. The limited escape depth of Auger electrons makes the method sensitive to a surface region only about 10 Å in depth while the large escape depth of X-rays makes the microprobe sensitive to a region about 10,000 Å in depth. Also the dominance of Auger electron emission for low energy ionized states makes the Auger technique very sensitive to elements of low atomic numbers and the X-ray microprobe correspondingly insensitive.

Dielectric Relaxation. – A fundamental way of investigating dielectric materials is to measure the relaxation properties of ionic impurities in the material (Ref 4). In this technique an alternating electric field is applied across the oxide and the dissipation factor is measured as a function of frequency and temperature since these two parameters affect the motion of ionic impurities the most. For a given temperature, one or more frequencies exist where the dissipation factor shows relative maxima. This is caused by ionic motion absorbing energy from the electric field since the dissipation factor is related to the in-phase component of the charging current. For the ionic impurities postulated to exist in thermally grown silicon dioxide this type of migration is associated with interfacial polarization caused by the space charge limited current when the ions pile up at the two oxide interfaces. Of the several polarization mechanisms possible in dielectric material interfacial polarization occurs at frequencies below about 10 KHz in general.

Three different techniques, to be described below, were used to investigate the dielectric relaxation behavior of oxide samples. Relative maxima were found in most of these which indicate mobile ions are removing electrical energy from the applied field at particular frequencies. This data alone cannot identify the type of ionic impurity. Further samples were then contaminated with Na, F, Li, and K. Increased maxima were found for the Na and F. Additional data at higher temperatures should be taken for the purpose of measuring activation energies for the relaxations.

Flame Photometry. – A flame photometer is a device for measuring the intensity of the energy emitted by elements when excited in a flame. Since only a relatively small amount of energy as compared to that in a spark or arc is available in the flame the elements fo not emit a large number of lines. It is necessary to keep the characteristics of the flame source constant throughout each series of measurements. This is accomplished by careful regulation of the gas pressure and rate of flow.

C-V Analysis

One type of oxide samples investigated were capacitors which were part of a test circuit used in Autonetics production of MOS circuitry as shown in Figure 9. The two pads shown are aluminum vacuum deposited over 1400 Å of thermally grown silicon dioxide. One is a substrate capacitor on the n-type silicon while the second is a p-type diffused region The other active elements shown were not used on this program. The oxides were thermally grown silicon dioxide, usually grown wet, on (111) silicon with resistivities between 6 and 10 ohm cm. Dopants were either phosphorus or boron in diffused regions. The capacitance-voltage measurements were made with the method shown in Figure 10. Usually the 100 KHz LC meter was set for full scale deflection of 30×10^{-12} farads, the ramp generator at -14 volts and increased at 1 volt per sec. Figure 11 shows the characteristics of a control sample before and after stressing. Here the stresses shown produced recovery curves which did not exactly duplicate the initial values. This implies the redistribution of impurities does not return to the initial one although the difference is usually small.

Over 100 MOS structures were examined for test samples. Since they were obtained from a well controlled process line it was necessary to seek degraded samples on which further analysis could be performed to detect and identify process impurities. Those found to have the largest ΔV shifts were chosen for further study. It is of interest to note the large spread in capacitance-voltage characteristics of these devices because they usually came from the same process lot and thus were exposed to the same process steps. Figure 11 shows a plot of typical capacitance characteristics. In general the stress shifts and recovery behavior showed the presence of about 10^{+12} charges/cm^3.

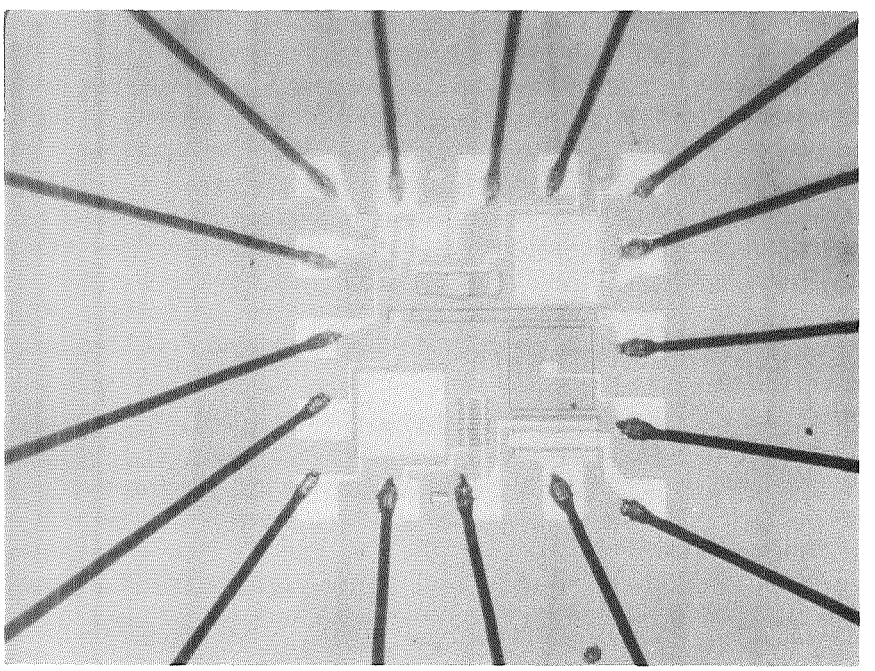


Figure 9. MOS Circuitry

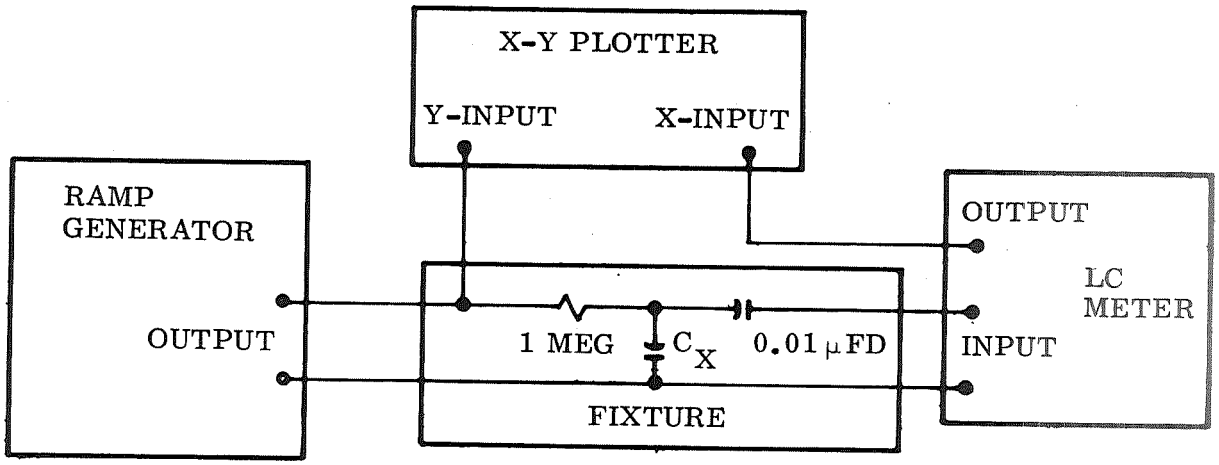


Figure 10. Capacitance - Voltage Test Method

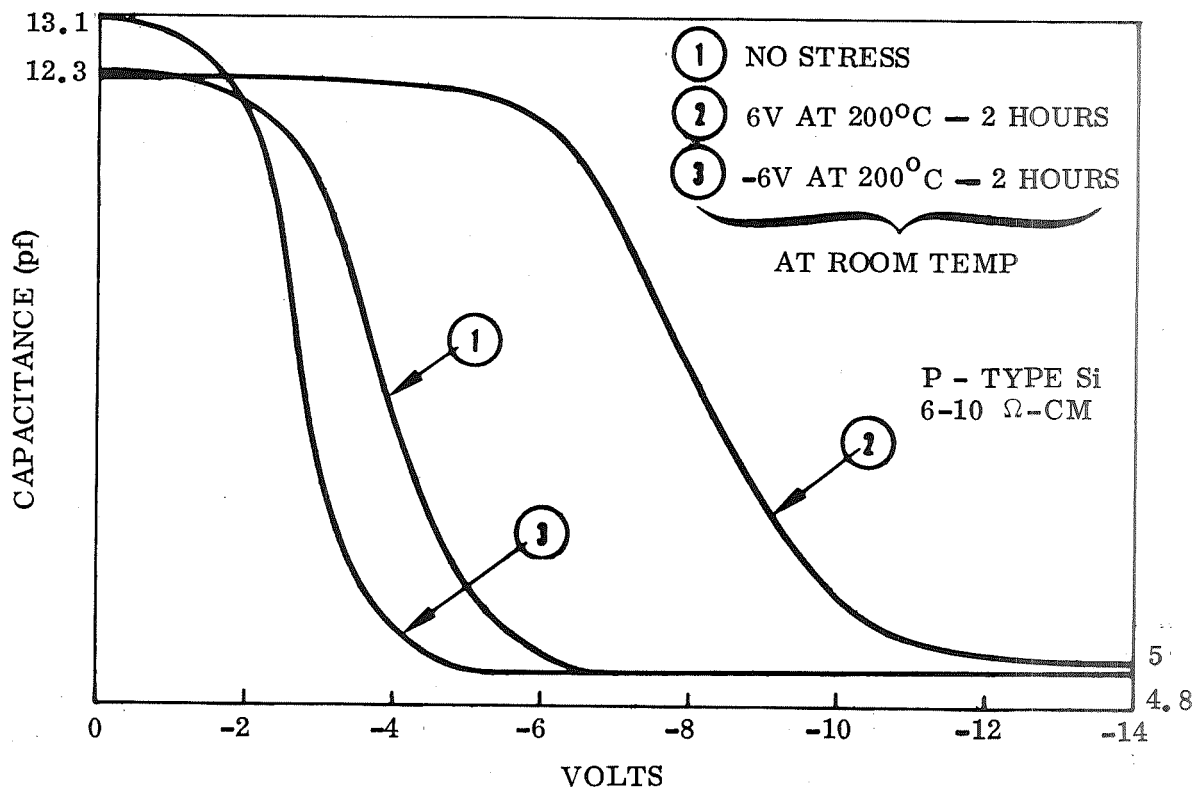


Figure 11. C-V Curve Before and After Initial Stressing

Ion Microanalyzer Results

Consolidated Electrodynamics Corporation (CEC), Monrovia, California was visited to obtain analytical data using the Cameca ion emission microanalyzer. Two of the test devices were selected for analysis. One of the devices was "stable" and the other "unstable" in terms of FET transistor threshold voltage drift and C-V voltage shift on capacitor areas obtained in the previous section.

The table below shows comparative ion microanalyzer data obtained on both the "stable" and the "unstable" device. A 5 micron diameter area was "etched" through the specified capacitor area using the ion sputtering process. Approximately 10,000 Å of aluminum and 1,500 Å of silicon dioxide were removed. The data indicates significantly higher amounts of Cu, Li, K, and Na in the unstable device metallization and oxide than in the stable device. The data also indicates the possibility that the source of the oxide contamination could be the deposited aluminum.

TABLE IX. ION MICROANALYZER DATA* ON REL CHIPS

	Stable Device				Unstable Device			
	Cu	Li	K	Na	Cu	Li	K	Na
Metallization	14	6	32	54	230	68	2140	930
Oxide	11	38	160	320	16	156	1300	5300
*(Relative Data-Peak Height Units)								

Dielectric Relaxation Analysis

Investigation of dielectric energy loss phenomena involves the measurement of the dissipation factor at various frequencies of the applied electric field. Maxima found can be shifted by changes in the sample temperature so that an activation energy can be associated with the interfacial polarization if it is thermally activated (Ref 5). Three different procedures were used to measure for ionic relaxation in silicon dioxide. The first employed a commercial bridge, the second a lock-in amplifier and the third with a simple oscilloscope. The test chamber shown in Figure 12 held both devices and wafers. When sealed, the atmosphere was dry nitrogen with through-electrical connections used for interior heating elements and readings on either the control or test sample.

The first method employed a General Radio 1620A Capacitance Bridge as shown in Figure 13. This instrument has eleven fixed frequencies between 20 Hz and 20 KHz. It is a transformer ratio arm bridge which measures capacitances down to 10^{-5} picofarad and dissipation factor to 10^{-6}. It was found necessary to use a General Radio model 202A function generator to scan more frequencies because dielectric relaxation maxima occur at various frequencies. This method proved to be slow since the bridge had to be rebalanced at each frequency and was limited by the instrument to a maximum potential of 30 volts per kilohertz output. (The larger the electric field the easier it is to detect ionic migration effects.) Some maxima were detected on both wafer oxides and MOS structures. Identification of the impurities involved was made indirectly by intentional contamination of additional samples. Sodium and fluorine

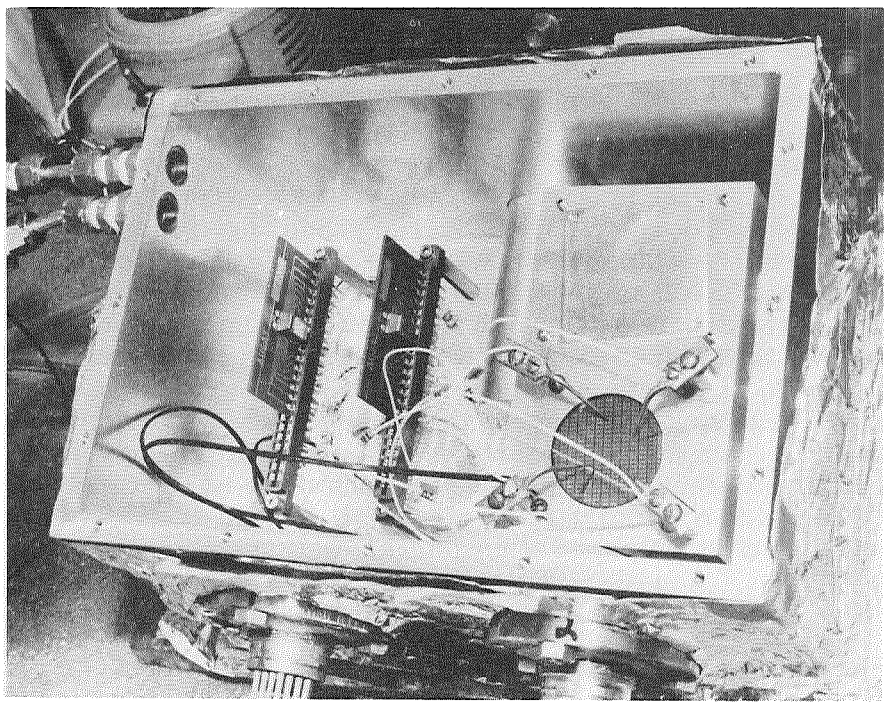


Figure 12. Test Chamber for Dielectric Relaxation Experiments

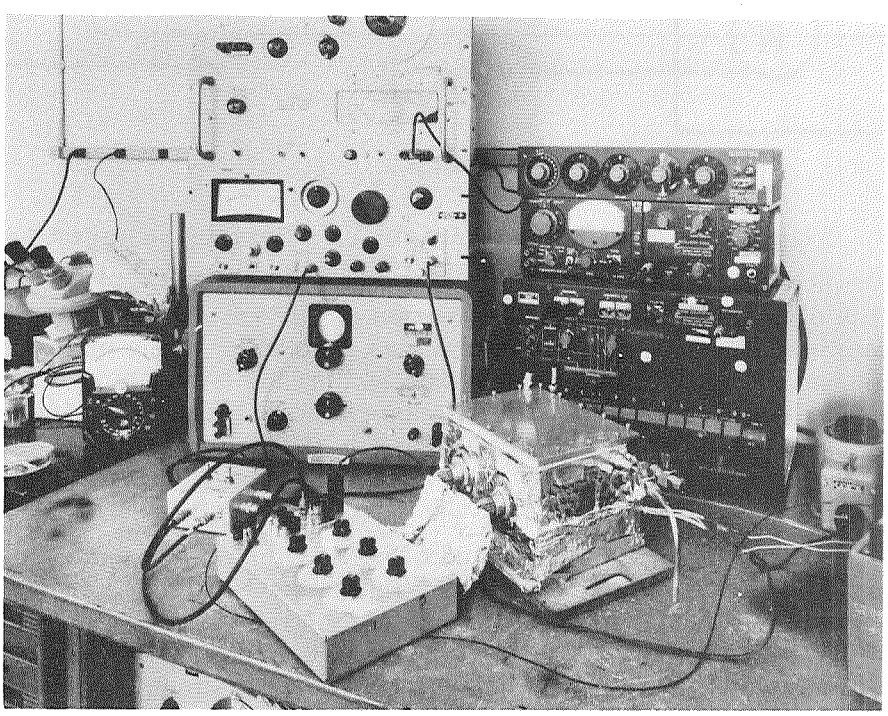


Figure 13. Test Equipment for Dielectric Relaxation Experiment

appeared to increase the relative maxima. Additional data at higher temperatures could be used to calculate activation energies associated with frequency shifts of these maxima. (Impurity identification in this way would be more accurate.)

In the second method an HR8 Lock-in Amplifier was used to apply a signal across the oxide and measure the fraction returned. The HR8 Lock-in Amplifier is essentially a detection system capable of operating with an extremely narrow equivalent noise bandwidth. Its function is to select a band of frequency from a signal spectrum applied to its input circuit and convert the information to an equivalent dc. The basic element of a Lock-in Amplifier is a phase-sensitive detector in which the signal voltage is mixed with a reference voltage. A zero degree phase angle was selected to return the resistive component of the applied signal. The signal applied to the device, as shown in Figure 14, was the same for all comparative readings and was approximately 500 MV rms. This provided an output of 9.90 V dc when applied directly to the detector. This same signal was then placed in series with the sample under study. The signal that was then applied to the detector was the ratio of loss due to dissipation as compared to 9.90 V dc. A series of reference frequencies were used at 25 Hz intervals from 500 to 2000 Hz. Plots were then made of this dissipation vs frequency. The initial study used three wafers. One device was contaminated with sodium, one contaminated with boron, and one was used as a control. These devices were placed on a hot block at 123°C in a dry nitrogen atmosphere.

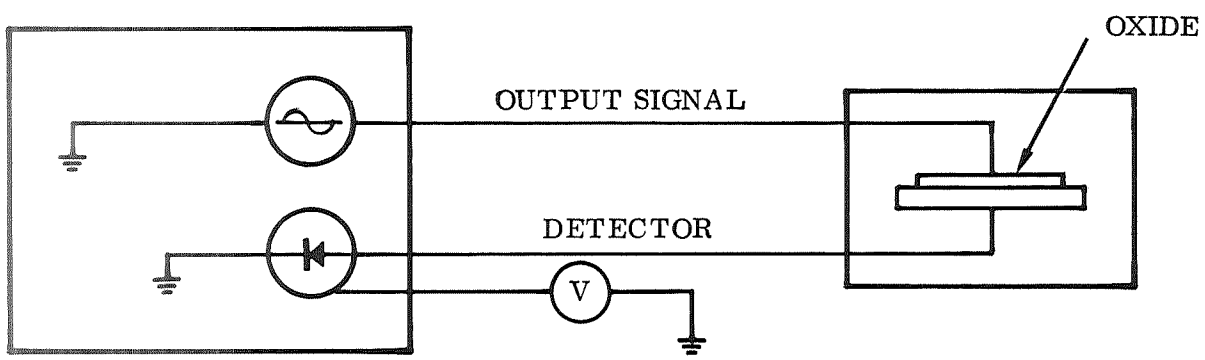


Figure 14. HR8 Lock-In Amplifier – Sample Chamber

Examination of graphical plots of dissipation factor versus frequency showed several small maxima that could be caused by ions migrating in the oxide. However, this data was not repeatable with confidence and further analysis using this technique was not performed. It is felt that the capacitance of the connection wiring and inherent noise outside the HR8 prevented accurate detection of the return signal as the frequency range was scanned.

The third method investigated consisted of putting the oxide capacitor in series with a larger capacitor and applying the alternating current across the combination. Then the two voltages were connected to the horizontal and vertical inputs of an oscilloscope as shown in Figure 15. With vertical and horizontal amplitudes equal the pattern is an ellipse with its major axis at 45 degrees. Measurement of the ratio of the major to minor axes was then used to compute the dissipation factor through

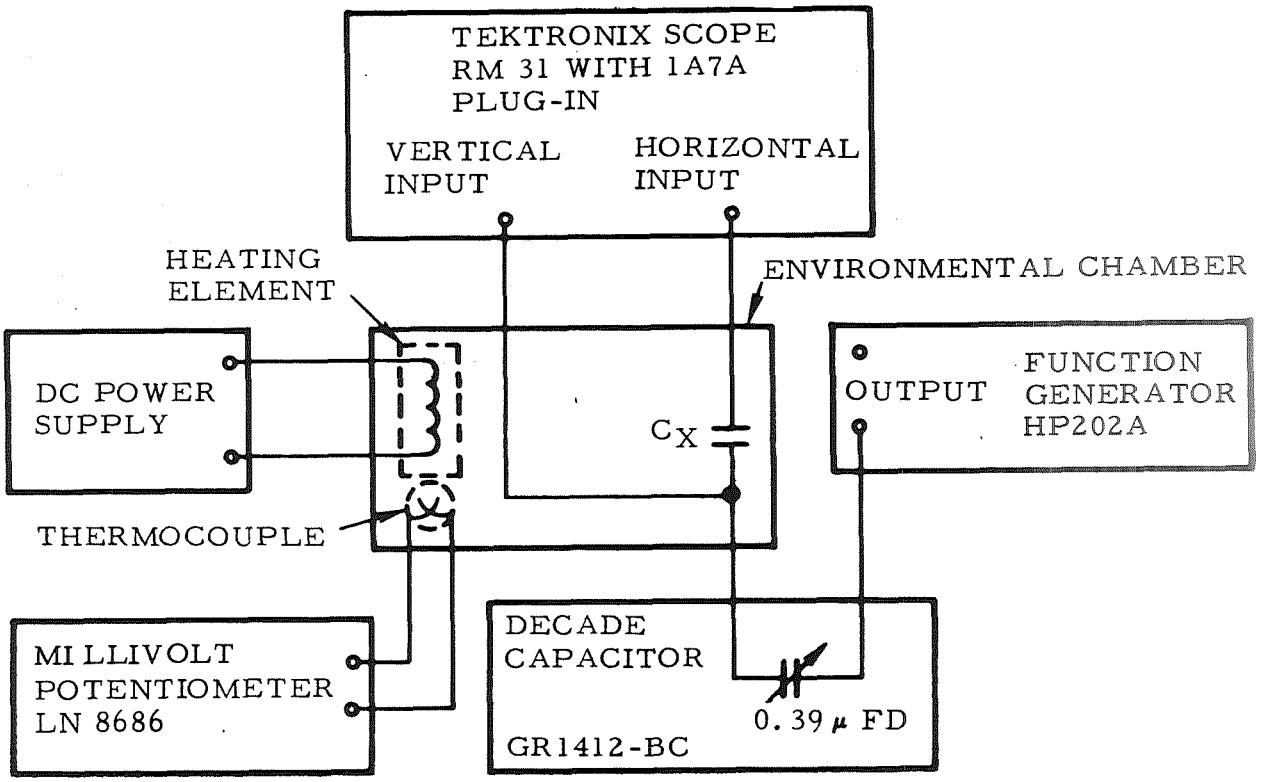


Figure 15. Loop Test Diagram

formulas given in Reference (6). This loop technique has the advantages of working at frequencies below 10 Hz and also being relatively simple. A major factor that has probably prevented dielectric relaxation measurements in silicon dioxide by others is the general need for special low frequency bridges and very accurate reference capacitors. Data taken with this method went to as low as 0.01 Hz.

In developing the loop method, four of the previously discussed MOS test devices were obtained from in-house manufacturing. Initial capacitance vs voltage curves were taken on these four devices to ascertain their characteristics. All four samples showed a ΔV shift indicative of ionic migration.

The lids were removed from the devices and three of the oxides contaminated by first scribing a small area of the aluminum oxide pad and then placing a drop of chemical solution on these areas. The chemicals were NH_4HF_2, Na_2SO_4, and $LiNO_3$ at one mole solution each. The samples were heated for 48 hours at 200 C. C-V curves were retaken—which showed the F and Na contaminated samples still exhibited C-V characteristics.

These two samples and the control sample were measured for dielectric relaxations using the loop method. Each of the samples was placed in the environmental chamber and subjected to the following test.

1. The environmental chamber temperature was set at 23 C.

2. Decade capacitor was set for 0.39 microfarad.

3. The functional generator was set for a sine wave with maximum amplitude, and a frequency range of 0.01 Hz to 1 KHz used.

4. The vertical and horizontal amplification on the oscilloscope were adjusted to make the respective amplitudes as displayed on the oscilloscope equal for each frequency. The data was then recorded by means of photography.

Dissipation factor measurements were taken on the sodium, fluorine and control samples at room temperature and at frequencies between 0.01 and 1000 Hz. Above 10 Hz the curves exhibited the same characteristics. The samples were then stressed again at 200 C with -6 volts for 10 hours. Dissipation factors were remeasured at 23 C and also at 115 C. The sodium sample was electrically damaged so the results shown in Figure 16 are for the control and fluorine samples. Figure 16 shows the data between 0.01 and 1.0 Hz where it is seen that the contaminated sample passed through a low frequency maximum while the control sample did not.

In summary the technique of measuring the dissipation factor behavior may be useful for either wafer or device oxides. Several maxima were detected using both the bridge method and the loop method although an identification of the ionic impurity involved could only be correlated with contaminated samples. The loop method was found to be the easiest to perform and also permitted measurements down to 0.01 Hz. This low frequency range is needed to detect impurity migration around room temperature. Results presented here show the feasability of this technique but further development particularly at higher temperatures is desirable.

Solids Mass Spectrometer Analysis

Several silicon wafers with thermal oxides were prepared for analysis as defined in Table X. Photoresist operations were not included in preparation of these initial samples. Wafer "B" simulates the MOS gate oxide; sample "E" is initial oxide. Sample "A" omits the processing steps after phosphorous deposit.

The analysis data reported in Table XI was obtained using a CEC Model 21-110 solids mass spectrometer. In order to maximize the sampling of oxide and minimize the sampling of silicon, successive small pulses of RF energy (sparks) were applied to different areas of the surface of the wafer. Under these conditions the average sampling depth was approximately 1.5μ. The technique of using many short duration sparks over the surface is somewhat time consuming, and it is difficult to use sufficient sample to obtain the usual sensitivity of 1 to 10 parts per billion. For example in the samples reported, only 10^{-8} coulombs were collected and the detection limit of sodium was 70 parts per billion atomic. The detection limits are sufficiently low however to show measurable impurities in many of the oxides examined as the subsequent data will show.

Referring to Table XI, it appears that in Sample B (simulated gate oxide), the heaviest contamination aside from carbon and fluorine, was lithium. The data reported under Sample B, surface, represent the impurities found to a depth of 1.5 μm. Since the oxide thickness was approximately 0.15 μm thick, a 10 fold dilution of the oxide impurities was obtained. Sample B bulk covers impurities extending 10 to 12 μm into the underlying silicon. Samples A bulk and E bulk cover impurities extending entirely through the wafers, including the back surface. This probably accounts for the observed increase in impurities reported in these two columns.

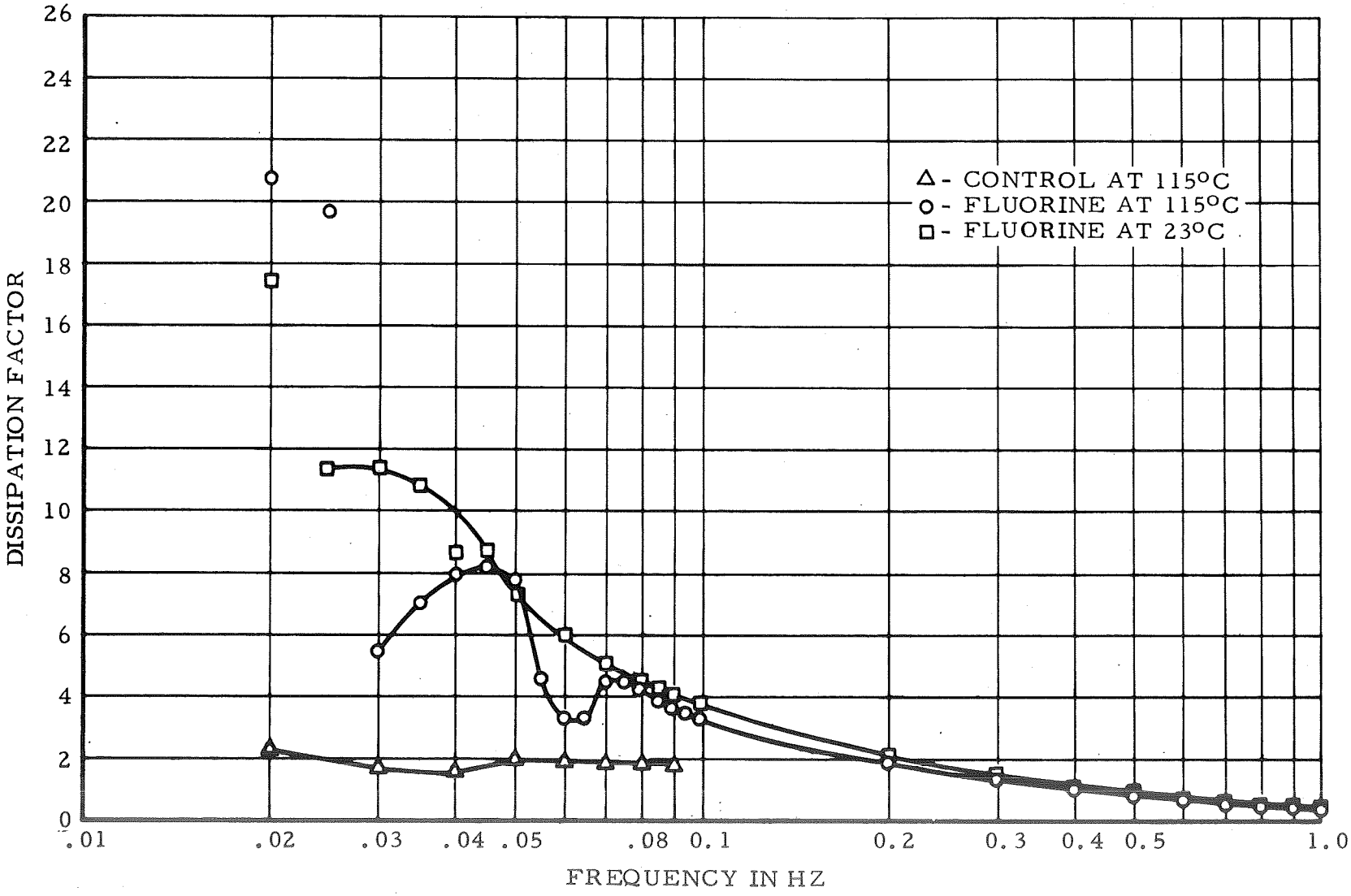


Figure 16. Dissipation Factor Maxima in Contaminated Sample

Samples: A, surface; B, surface; and E, surface cover essentially the grown oxide with slight penetration into the silicon substrate. The amount of Fe reported under samples B and E is close to the detection limit; therefore, this datum is probably not significant. The lithium level in the oxide of Sample B is significantly higher than either A or E.

In order to test the process for possible introduction of lithium during Step 4, * a new set of samples were fabricated and analyzed using an initial oxide (E), simulated gate oxide (B_1), and a simulated gate oxide omitting the phosphorus deposit (B_2). Lithium was not detected in any of these samples as shown in Table XI.

The highest sodium level (2.6 ppm) was found in the simulated gate oxide (B_1) of the new samples. The sodium level was significantly lower in the initial oxides (E) of both groups. The sodium level was also significantly lower in B_2 (without phosphorus) as compared to B_1. This is an unexpected result as the phosphorus has "gettering" and barrier properties (Ref 7) which, when coupled with use of the buffered etch to remove the high concentration phosphorous layer in the oxide, should reduce the total amount of sodium. Sample B_2 was prepared in the same manner as B_1 except that the phosphorus deposition was omitted. It should also be noted that sample B_1 which has the phosphorus deposit and buffered etch had a residual of 130 ppm phosphorus. Because of the high sodium content and high phosphorus content of this sample, it appears that the phosphorus along with the "gettered" sodium was incompletely removed by the buffered etch.**

With the exception of the Table XI Sample E (where the penetration of the test probe extended through to the back surface of the wafer), the sodium level in the silicon was lower than that of the oxide; indicating that the silicon is not a significant source of sodium.*** Most other impurities were also found to be lower in the bulk silicon than in the oxides.

Sample E (Table XI) had the lowest level of contamination except for carbon which may have been introduced by the solvents used for cleaning of the wafers.

The Table XII samples consisted of two wafers of each type (B_1, B_2, E). Of each type, one half wafer was utilized in the solids mass spectrometer analysis and two half wafers were used for MOS capacitance-voltage stress analysis. These half wafers were prepared by evaporating aluminum electrodes $\approx$ 0.030" dia. onto the oxide surfaces. The wafers were then heat treated in a nitrogen atmosphere for 10 minutes at 540°C.

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*Phosphorus Deposition

**The C-V stress data indicates that B_2 had a much larger shift in V_{FB} than B_1 although B_1 was substantially more contaminated. It is possible that the 30 ppm of phosphorus remaining in B_1 tended to stabilize the contaminants. The effective concentration of phosphorus necessary for device stability, however, remains to be established.

***This is in agreement with reported low solubility of sodium in silicon[8].

Several of the MOS capacitors from each half wafer were used to obtain pre-stress data. A Boonton Capacitance-Inductance Meter Model 71A-R (1 MHz) was used in conjunction with an adjustable DC power supply.

Many of the MOS capacitors on wafers B_1 and B_2 "broke down" on initial C-V test. The cause of the breakdown is not well understood; however, oxide defects could account for excessive leakage currents in the MOS capacitors. MOS capacitors which were stable initially, were stressed at 285°C with positive bias. The results are as follows:

Wafer Number	Oxide Thickness	Initial V_{FB}	ΔV_{FB} After 30 min.	Bias	ΔV_{FB} After an Additional 60 min.	Bias
E	1.6 μm	-22V	-88V	+100V	-29V	+100V
B_1	0.14 μm	-1.6V	-0.8V	+10V	-0.6V	+10V
B_2	0.14 μm	-1.5V	-2.5V	+10V	-0.8V	+10V

The stressing and testing of these capacitors has been continued, however the shift in V_{FB} has not saturated. The MOS capacitors on B_1 and B_2, which exhibited good characteristics initially, also exhibited excessive leakage after stressing. (Samples B_1 and B_2 "broke down" during the third hour of bias temperature stress.)

The V_{FB} for Sample E did not stabilize with continued bias temperature stress; however, no "breakdown" of the oxide was evident.

The surface concentrations of the significant impurities are listed in Table XIII. These data indicate that a number of impurities are present in surface concentrations much greater than the approximate 10^{10} cm^{-2} quantity which is the calculated amount necessary based on charge considerations for stress shifting the flat band voltage by 0.1 volt. It has been shown that phosphorus prevents sodium ion mobility. From a chemical viewpoint it is difficult to understand why all sodium in the oxide does not contribute to the stressed flat band voltage shift (in the absence of phosphorus). Since in even very pure oxides the sodium level exceeds the calculated sodium level allowed based on charge, the sodium (and presumably other cations also) present must be immobilized by phosphorus . It therefore might be anticipated that the sodium-phosphorus ratio is of utmost importance.

Rotating Disc Technique Development and Evaluation. - A JMS O1B(M) mass spectrometer was used to develop an improved technique for sample removal in order to increase sample size and minimize depth of penetration.

Hickman and Sandler have reported the use of the point to rotating plane technique (Ref 9). Their work only sampled a very limited amount of the surface. Malm (Ref 10) employs the "slow plow" technique of point to slowly translating plane, and penetrates far into the substrate. Neither of these techniques permit the rapid coverage

Table X. Wafer Oxide Processing

Access*	Grow 15,000Å S_1O_2 (1)	Etch Down to 700Å (2)	Regrow to 1,500Å (3)	Deposit (4) Phosphorous	Argon Bake (5)	Nitrogen Bake (6)	Argon Bake (7)	Buffer Etch (8)	Rinse & Dry (9)
WAFER	A	A	A	A					
	B	B	B	B	B	B	B	B	B
	E								

1. Oxidation - 1,200°C. 5 min. warmup dry O_2. 3 hr. steam only 1 hr. dry O_2 1 hr. N_2.
2. Gate etch - Soln., 5:1 NH_4f: Hf to light brown color.
3. Gate oxidation - 1100°C. 60 min. dry O_2. 15 min. N_2.
4. Deposit phosphorous - Source, $POCl_3$ with argon carrier. 5 min. O_2 & N_2, 1 min. source added, 5 min. O_2 & N_2.
5. Argon bake - 1100°C. 8 min.
6. Nitrogen bake - 1100°C. 8 min. (not in same furnace as argon bake).
7. Argon bake - 1100°C 8 min.
8. Buffer etch - soln., 20:1 NH_4f: Hf. 10 sec., rinse in alcohol.
9. Rinse and dry - running DI water, N_2 blow (zot).

*Process steps did not include any photoresist operations.

NOTE: Sample B analysis is covered in this report.

TABLE XI
ANALYSIS OF SILICON - SILICON OXIDE WAFERS BY SOLIDS MASS SPECTROMETRY

(Concentrations in parts per million atomic)

Element	Detection Limit	Sample B		Sample A		Sample E	
		Surface	Bulk	Surface	Bulk	Surface	Bulk
Li	0.1	61	12	1.9	0.83	ND	ND
B	0.3	0.6	0.3	3.0	-	-	-
C	0.3	800	190	130	140	350	68
F	0.3	75	21	4.5	2.7	0.97	1.2
Na	0.07	1.8	0.23	1.8	0.6	0.44	1.2
Al	0.2	0.2	0.2	0.2	0.2	0.2	0.2
P	0.3	13	2.7	230	54	2.8	0.89
Cl	0.3	0.9	0.8	3.9	4.1	0.7	1.5
K	0.1	0.25	0.15	3.2	0.54	0.39	0.61
Ca	0.2	0.2	0.2	0.9	1.1	0.58	1.4
Cr	0.5	1.3	1.6	-	-	1.7	2.0
Fe	2.0	2.0	2.0	-	-	3.0	3.0
Cu	0.5	3.5	0.8	-	-	-	-

TABLE XII
ANALYSIS OF SILICON - SILICON OXIDE WAFERS BY SOLIDS MASS SPECTROMETRY

(Concentrations in parts per million atomic)

Element	Detection Limit	Sample B_1 (with phosphorous)		Sample B_2 (no phosphorous)		Sample E	
		Surface	Bulk	Surface	Bulk	Surface	Bulk
C	0.3	200	35	270	22	44	57
F	0.3	7.4	0.7	13	0.7	1.0	0.5
Na	0.07	2.6	ND	0.55	0.1	0.1	0.1
Mg	0.3	2.5	ND	1.9	ND	0.5	ND
Al	0.3	3.8	0.5	0.5	0.5	0.3	0.3
P	0.3	130	7.0	3.6	2.1	ND	0.5
Cl	0.3	0.5	ND	0.5	ND	0.5	ND
K	0.1	2.7	ND	0.52	0.2	0.2	ND
Ca	0.2	0.3	ND	0.3	0.3	1.8	0.3
Cr	0.5	-	-	-	-	-	-
Fe	0.2	-	-	-	-	-	-
Cu	0.5	5.9	ND	2.0	ND	0.5	ND

TABLE XIII
SURFACE CONCENTRATIONS OF IMPURITIES IN PROCESSED OXIDES

Impurity	Surface Concentration atoms cm^{-2}	
	Sample B_1	Sample B_2
F	2.5×10^{13}	4.4×10^{13}
Na	8.9×10^{12}	1.9×10^{12}
Mg	8.5×10^{12}	6.5×10^{12}
Al	1.3×10^{13}	-
P	4.4×10^{14}	1.2×10^{13}
Cl	-	-
K	9.2×10^{12}	1.8×10^{12}
Ca	-	-
Cu	2×10^{13}	8.5×10^{12}

of substantially the entire surface of a silicon wafer as dictated by our thin layer and sensitivity requirements. The system to be described has fully met the requirements and is best divided into two parts: the source and the electrical control system.

Source. — The JEOL-JMS 01B RF spark source mass spectrometer incorporates the very desirable feature of completely interchangeable source systems. Thus by simply releasing the source vacuum, everything between the spark accelerating voltage contacts, and the primary slit may be interchanged. Typical source turnaround time from breaking vacuum to sparking the new sample is ten minutes.

The source provides separate rotary and translatory motion systems which, when operated simultaneously, cause the stationary counter electrode to generate a spiral spark path on the sample. The external motor and gear system drives the eccentric bellows-type rotary feed through. Within the evacuated area, anti-backlash bevel gears drive a precision made lead screw having a 10-32-60° threaded. The selection of 304 stainless steel for the carriage body and hardened 17-4 stainless steel for the ways reduced galling to a point where thorough burnishing with dry MoS_2 eliminated the problem. Each revolution of the drive motor translates the carriage .031 inch and the motor speed is dial adjustable from 1/2 to 120 rpm giving a translation speed range from .016 to 3.72 inches per minute. Other speed ranges are easily obtained by interchange of drive gears or even motor change. The manufacturer provides a wide range of speeds in completely interchangeable motors.

External parts and rotary feed through are similar to the translation system, but have a different speed range. Due to the carriage movement, an elastic belt type drive was selected to transfer rotational power to the sample spindle. A single BuNa-N "O" ring has been in use as a belt for several months with no signs of impending failure. Rotational speeds over a 1:500 range may be dial selected, the external gear ratio may be changed, or the internal pulley ratio altered to produce speeds from 3000 rpm to imperceptable movement.

The sample pedestal is mounted on 1-7/8 in. long, 3/8 in. diameter alumina shaft. The electrical insulation properties of this shaft have proven completely satisfactory. An interim shaft of micarta, however, suffered an internal electrical breakdown after a few hours use.

The alumina shaft has two precision ground bearing journal on which the dry MoS_2 lubricated ball bearings are placed with a light push fit. To provide for replaceable sample pedestals while maintaining water surface runout specifications of 0.001" was a difficult design problem. The shaft thread was specified undersize and is only used to hold the pedestal on the two precise journals at either end of the thread. The flat on the spindle top acts as the end stop. Rotation direction is selected to continuously tighten the joint. Electrical contact to the copper pedestal is through two spring wire contacts riding in an external groove.

The counter-electrode holder is a simple clamp end arm attached through a bellows to an external micrometer. The system provides 3/16" of movement to compensate for fine wire electrode consumption during an analysis.

Electrical Control System. - A short period of unsatisfactory manual operation rapidly established the need for a coordinating control system. A micro switch operated in a cam on the translation drive shaft advances the stepping relay one contact for each 0.031 in. of X movement. The total number of steps may be preselected to limit sparking to a desired band. There are a total of 36 steps available while only 33 are necessary to cover an entire 2 in. diameter wafer. The pulse start switch and repetition rate circuits of the mass spectrometer have been connected to the control system. Reduction in surface velocity as the spiral proceeds toward the center requires a constant change in spark pulse repetition rate. This is accomplished with a second stepping relay which, operating in consort with the counting relay, changes condensers with each step. The condenser values were empirically determined to permit approximate constant pulse separation.

The stepping relay may be pre-advanced to any step with a manual push button. When the operate button is depressed, a multi contact control relay is energized. This relay simultaneously energizes the rotational and translational motors, closes the pulse start switch, and energizes the micro switch operated stepping relay circuits. The sparking proceeds automatically (except for manual counter-electrode movement); changing pulse repetition rate each 0.031 in. of radial movement until the preset number of steps have been completed. When the stepping relay reaches that particular contact, the holding circuit of the control relay is opened. This causes a cessation of all movement and sparking and the run is ended. A stop switch is provided to allow operator interruption of the run at any time.

Operational Experience. - Several counter electrode materials have been tried including gold, tungsten, and tantalum. Fine wires would be the natural choice, but the erosion rate of 0.002 to 0.006 inch diameter wires was too large for satisfactory spark gap maintenance. Thus, larger wire such as 0.025 inch gold has been pointed for use. The large wire appears to rapidly absorb the spark generated heat and protect the point from meeting.

Many combinations of rotational and translational speeds have been used in an attempt to entirely cover the surface of the wafer. When speeds were selected to just overlap the spark craters in a continuous spiral pattern, the heat transferred to the wafer caused fracture in a large number of cases. At present the best compromise seems to be a rapidly rotating wafer (2000 rpm), an initial spark rate of 3 KHz and a slow translation rate of 0.031 in./min. In this case the entire wafer is covered with a random overlap of spark craters. The heat is well distributed and wafer breakage is minimal.

Calibration experiments present problems due to the extremely small quantities of material involved (10^{12} atoms Na = 4×10^{-11} grams). Experiments involving the doping of the surface of a wafer with radioactive sodium 22 show that 50 to 70% of the radioactivity is removed during a single sparking pass. These data would be expected to be similar to those obtained in future work where the sodium will be diffused into the surface. Contamination of the 22 a.m.u. line by CO_2^{++} abd SiO^{++}, both of which were unresolved from the Na^{22}, precluded plate calibration during the experiment.

Calibration with LiCl indicated a detection limit between 10^{11} and 10^{12} atoms. The lithium 7 line was well resolved from the silicon 28^{++++} and the nitrogen 14^{++}.

Many survey type runs have been made on silicon wafers with and without oxide coatings. Crater depths appear to be in the 6 to 7×10^3 A range on silicon surfaces and from 1 to 3×10^4 Å in silicon oxide surfaces. Profilometer data indicates a volcano type ring of melted material surrounding the crater. These rings protrude as much as 1×10^4 Å above the surface. The rapid rotation - slow translation technique exposes these peaks to preferential sparking and thus may respark the same surface material several times resulting in better surface consumption. The 50-70% data from the radioactive sodium experiment was obtained under these conditions.

Wafer cleaning prior to sparking has proven to be a major problem in the determination of sodium surface contamination. Typical solvent cleaning in water followed by vapor phase cleaning in acetone produced wafers indicating 10^{13} to 10^{15} atoms of sodium. When a preliminary physical surface scrubbing with a cotton swab in water was added, sodium levels fell to the 10^{12} level. Hydrocarbon contamination is always present and lines at most common C-H combinations such as C, CH, CH_2, CH_3, C_2H_3, etc. are present in large quantities. These may originate in mass spectrometer contamination or may be from the wafer. Since pure metal-metal runs still show some similar contamination lines, these have been dismissed for the present as instrumental contamination. Water is another ubiquitous contaminant and the spectra always includes the 17 and 18 a.m.u. lines.

Auger Electron Analyses

Silicon dioxide samples were specially prepared for Auger electron spectroscopy. Oxides were thermally grown on six wafers by a dry (5 minute), wet (3.5 hours), and dry (1 hour) process resulting in a 17,000 Å initial thickness. The oxides were etched back using a buffered HF solution to a measured 8,000 Å thickness. These steps parallel those of an MOS process line at Autonetics. Aluminum capacitor pads were constructed by vacuum depositing 400 Å onto a 50 mil by 50 mil area. A second strip deposition of 6000 Å overlapped the pad to permit electrical contacts for capacitance voltage measurements. The ΔV shifts measured corresponded to a mobile charge density of 10^{12}. The samples were stressed at 6 volts for 24 hours to move the postulated positive ions to the top of the oxide for Auger analysis. One wafer was then placed in the Auger spectrometer and the Al removed by the controlled Ar^+ sputtering. At the point where the SiO_2 layer was just becoming exposed (where a Si Auger peak was first detected), the surface was carefully analyzed for alkali impurities. No alkali impurities were detected which means they were in concentrations less than $10^{20}/cm^3$ near the surface. Even if all the positive charges initially in the oxide were driven to the interface, the concentration may have been below $10^{12}/cm^2$ which is likely below the limit of detection. Another likely possibility is that sputtering did not expose the interface uniformly so that the average concentration over the cross-sectional area of the incident beam (0.1 mm^2) was much less than that immediately at the interface. In any case, inability to detect impurities in this sample suggests that Auger spectroscopy is not sufficiently sensitive to detect trace alkali impurities in a normally grown silicon dioxide layer.

Flame Photometry

Since the effect of sodium contamination in causing device instability is so well documented, a program to trace possible sources of sodium contamination using new sensitive flame photometric techniques was undertaken. Chemicals for analysis were taken in an "as received" condition in the original containers. Some materials were also taken from a MOS pilot line in a "used" condition; these included:

Oxide (hot) etch (a solution of NH_4F:HF, 5:)
"Chromic" cleaning solution (H_2SO_4:CrO_3, approximately 50:1)
Aluminum etch (80% H_3PO_4, 5% HNO_3, 5% HAC, 10% H_2O)
Aluminum metal button (from E-Beam evaporator)

In addition, a sample of deionized water from a running tap was obtained. Table XIV groups the analyzed materials in order of decreasing sodium content. The contamination found in the "chromic" cleaning solution is due to the sodium concentration of the CrO_3 and H_2SO_4. The largest source of sodium contamination in the aluminum etch is the H_3PO_4. The Shipley developers and resists are all high in sodium. An experimental Shipley developer, AZ-6807-1-XP ("Free of Metallic Ions") is, unfortunately, also in the high-sodium content category. It should be noted, however, that the sodium content of the experimental Shipley developer is 1000 to 4000 times less than the standard Shipley developer. The DI water had the lowest sodium level (1.5 ppb) of all the materials tested.

Depending on the source of contamination and treatment after contamination, it may be possible to remove sodium from the surface of the oxides by HF and/or distilled water treatments.

Alternatives to the "chromic" cleaning solution having less sodium contamination should be considered. A sodium-free aluminum etch would also be very desirable.

Discussion

The cursory evaluations made of the analytical techniques described indicate that the ion microanalyzer could be of greatest potential used in the analysis of silicon oxide impurities. (Unfortunately only brief courtesy data could be obtained since the instrument available at CEC for demonstration purposes was utilized.) Significant problems were detected in the use of both the solids mass spectrometer and the Auger electron spectroscope which enhance the advantages of the ion microanalyzer. Primary solids mass spectrometer difficulties resulted in the sample removal process required. Even with the spinning disc method significant penetration through the oxide existed and thus assumptions must be made about the concentration of impurities in the oxide. Also the use of whole wafers for analysis precludes the evaluation of local failures and/or device areas.

The Auger technique eliminates the depth penetration problem but requires substantial impurity concentrations in the 100 Å region near the surface being analyzed. It is recommended that any future work be oriented toward a full scale evaluation of the ion microanalyzer.

TABLE XIV.

SODIUM CONTENT OF PROCESSING CHEMICALS

Sodium Content	Reagent
High (>1, 000 ppb Na)	CrO_3, $POCl_3$, H_3PO_4, Aluminum etch AZ 111, AZ 6807-1-XP, AZ 303A, AZ 303B, AZ 1350A
Medium (250-1, 000 ppb Na)	HNO_3, H_2SO_4, Chromic "A," Chromic "B," KTFR
Low (50-250 ppb Na)	HF, NH_4F, Oxide (hot) etch, isopropyl alcohol, BBr_3 Acetic acid, acetone
Very low (<50 ppb Na)	Trichloroethylene, KMER Developer, KMER Thinner, D.I. H_2O.

MISCELLANEOUS TECHNICAL PROGRAMS

Inversion Model Investigation

The objectives of this investigation were to employ isotopic tracers to determine the contribution of mobile positive ions to inversion and to use EPR spectrometry to discover whether oxygen vacancies are present and potentially able to participate in inversion. At the time the original proposal was prepared no definitive experimental evidence existed capable of distinguishing between the positive ion model and the oxygen vacancy model. It was believed that more exact knowledge of the mobile species causing inversion would provide a basis for a solution to the inversion problem. Subsequently a number of investigators demonstrated electromigration of sodium ions through oxide layers, to yield devices more resistant to inversion. The general improvements due to sodium control made logical a decreasing emphasis in this area on Contract NAS12-4. The following results have been accomplished on this program and were presented at an Electrochemical Society meeting (Appendix E) in 1966.

Entrapment of hydrogen in thermal oxide grown in a moist ambient was demonstrated by using tritium tracer of 1000 millicuries/gram specific activity in the process gas and counting the weak beta activities in the resulting oxide samples. The oxides were found to contain approximately 10^{17} atoms of hydrogen/cm^3 oxide. The oxide beta activities were stable over a long period of time, showing little or no tendency to exchange with atmospheric water. A later experiment by Burgess and Fowkes using amuch lower specific activity gave a value of 10^{20} H atoms/cm^3, a result that was found to be experimentally unrepeatable on Contract NAS 12-4. The essential objective of the investigation was achieved, however, and later substantiated by the work of others. Hofstein (ref.11) has since demonstrated the contribution of hydrogen ions to drift instability in MOS devices.

Sodium ion occurrence in the oxide was investigated by neutron activation analysis of specimens from the tritium tracer runs. Sodium levels in the range of 10^{18} atoms/cm^3 were found. This result was in substantial agreement with those of Carlson, and others, and the investigation was closed.

Deuterated planar transistors were selected for inversion study with the initial intention of detecting electrochemically liberated deuterium in the package ambient by mass spectrometry. A positive result would implicate hydrogen ion transport in inversion. Following the availability of the tritium tracer results, however, calculations showed that the available deuterium, even if completely freed, would be beyond the limit of mass spectrometric detection. The deuterated transistors then were investigated through their activation energies of recovery from inversion. A difference between them and comparable hydrated transistors again would indicate hydrogen ion participation. An apparent difference between the two sets of transistors indeed was observed initially but was not substantiated in later experiments because repeated inversions and deinversions produced changes in the activation energies. Although the original objective was thereby thwarted the changes observed were in the direction of increasing inversion resistance and led to a proposed process innovation of "inversion hardening" by thermal and bias cycling (Appendix F), later published as Tech Brief 67-10176. The activity in this area was terminated with the achievement of this result.

The electron paramagnetic resonance experiments were performed on thermally grown silicon dioxide to investigate the oxygen vacancy model. Resonance data were taken on many samples grown wet or dry under varying conditions of temperature, ambient, and chemical contamination. Three resonance signals were detected from these oxides. One was from hydrogen entrapment and another from a possible electrode reaction between aluminum and the oxide that has been postulated to generate oxygen vacancies by Burkhardt at IBM. The third signal was shown to be related to both sodium and fluorine retention in the oxide. A detailed report of this work is given in Appendix G.

A further accomplishment in this area of effort was the preparation and delivery of a paper on the subject at the American Physical Society Summer Meeting, Seattle, Washington, 31 August to 2 September, 1967.

Failure Mechanisms Associated with Packaging

The bulk of the work in this area was directed toward an evaluation of the effects of hydrogen ambients on the performance of integrated circuits, partly because of various, and sometimes conflicting, reports of such effects and partly because analytical results at Autonetics frequently have disclosed the presence of hydrogen in integrated curcuit packages. However, a significant degradative effect due to hydrogen was found, and efforts to induce such an effect were abandoned. A further result of this program was a thermodynamic analysis of ambient gas effects (Appendix H) on materials normally present in packaged devices which corroborated the above results with respect to hydrogen interaction with silicon, silicon dioxide, aluminum, and aluminum oxide.

Nonuniform Diffusion Doping

The objective of this investigation was to determine whether incomplete mixing of input gas compositions employed in diffusion steps led to persistent concentration gradients at wafer surfaces and nonhomogeneous doping. If such an effect were found to be present it would indicate a requirement for a process modification, such as a baffle system, to assure complete mixing, or a means to assure uniform wafer exposure as, for example, by mechanical wafer rotation. Calculations showed, however, that complete mixing occurs in the first 4 in. of furnace tube. Because the unoccupied input tube section employed by most processors is three to four times this distance it was concluded that incomplete vapor phase mixing was not a substantial source of doping irregularities and the investigation was abandoned. It is recognized, however, that nonuniform doping is a continuing problem and may become a deterrent to the development of large scale integration after other more pressing problems are resolved.

Failure Analysis Service

The objective of this service was to examine, on request, state-of-the-art components for inhomogeneities arising from process techniques. These analyses were to be performed in detail on components important to NASA-ERC. This effort constituted a support function which was expected to reveal hitherto unsuspected inadequacies associated with fabrication steps as well as to characterize salient

reliability problems pecular to components from specific sources. Component anomalies were examined by established failure mechanism techniques from which performance predictions could be derived appropriate to the long term reliability and environmental requirements applicable to NASA missions.

Appendix I includes the final reports on two of the larger analyses performed under this phase of the program. This discussed analysis of 89 NPN transistors and 65 integrated circuits.

Analysis of the integrated circuits indicated that a major portion of the failures was traced to improper marking of the device package such that the devices were placed incorrectly in the circuits. Electrical overstress evidence was noted due to this misregistration. A separate report describing these results was submitted to NASA.

Instruments for Failure Analysis

The objective of this effort is to apprise NASA-ERC of optimum instrumentation and test sequences from which maximum insight into failure mechanisms may be gained, Original tabulations were presented in the second Monthly Report and Quarterly Report Number One, giving instrumental capability ranges, applications to failure mode and failure mechanisms investigation, and references to pertinent process steps. Supplementary instrumental data have been presented in succeeding reports. Continuing efforts in this area were intended to ensure the awareness of NASA-ERC of current instrumental innovations for extracting maximum failure information. (Appendix J)

Hermeticity Testing

In this section leak test techniques applicable to hermetically-sealed integrated circuit packages are brought under scrutiny. Methods presently in use, including their advantages and shortcomings, are considered as well as new approaches under development designed to improve on those now employed. Because of the previous absence of a single test applicable to the entire leak-rate range, applicable techniques conventionally are categorized as "fine leak" and "gross leak" tests. For convenience these categories are followed below although they may become obsolete in view of a new technology now being evolved.

Fine leak testing. – All of the test methods reviewed and outlined herein, with two notable exceptions, employ the technique of inoculating the package with a tracer gas, usually helium, after it has been sealed, then conducting a leak test of the device with a helium leak detector. The pressure and duration of the tracer gas inoculation varies among users but is of problematical effect on the leak test accuracy. The average pressurization period is four hours at 60 psig. The practical upper limit for helium leak testing appears to be 1×10^{-8} to 1×10^{-9} Std cc/sec He. The practical lower limit appears to be 1×10^{-5} to 1×10^{-6} Std cc/sec He.

The technique of inoculating a package after sealing with a tracer gas in actuality produces a questionable leak rate number which is the product of the leak rate of an unknown gas fraction pressured into the package, and of that fraction of gas in turn being evacuated from the package and tested during the leak test-cycle. Furthermore the helium leak test machine is calibrated for 100 percent helium. The fraction of helium (tracer gas) within the package is obviously unknown. The only way to assure the validity of a tracer gas leak test is to seal the devices to be tested in a gas ambient with a known fraction of the tracer gas to be used.

A new leak test method developed at the North American Rockwell Corporation Science Center requires no special pre-pressurization to inoculate a package with a tracer gas. The packages may be sealed with dry nitrogen or dry air. This leak test method is based on the principle that helium atoms excited to the metastable state will transfer energy to the nitrogen or oxygen atoms presumably leaking from the package under test. The excitations of these N_2 or O_2 molecules can thus be detected by counting the number of ions formed. Leak tests conducted utilizing this principle have demonstrated that leaks as fine as 1×10^{-8} Std cc/sec He and as gross as holes 0.090 in. diameter have been detected in typical IC flat packs. Thus, utilizing this new principle, "fine" leaks and "gross" leaks are detected with one test.

The leak test method reputedly used by Raytheon is one which inoculates a package under pressure with Freon or similar liquid. It is reported that a weight gain of 50 μgram will fail a device. Based on DuPont Corporation, corrosion rate studies of Freon type compounds on aluminum, it has been determined that at room temperature Freon will corrode through the average integrated circuit interconnection in 10 months. This method appears to be a reliability hazard.

It is theorized that all leakage at rates less than 10^{-6} Std cc/sec He is by diffusion and that leakage due to viscous flow is negligible. The fraction of ambient exchange is therefore independent of total and partial pressures, although the absolute amount of exchange of a particular gas is directly proportional to the difference between the partial pressure within and without the package. A 14-lead integrated circuit flat pack with an internal volume of 0.005 cc and a leak rate of 5×10^{-7} atm cc He/sec thus exchanges 10 percent in 0.77 hours, 50 percent in 5.2 hours, and 90 percent in 17.2 hours. The time for exchange is inversely proportional to the leak rate and, for example, is 50 times as great for a leak rate of 10^{-8} atm cc He/sec. The time for an equivalent proportion of exchange in a larger package is greater and is directly proportional to the volume of the package.

Gross leak testing. - Most gross leak detection methods reviewed and outlined herein, and used on opaque packages, employ the simple technique of detecting gas bubbles escaping from a leaking package while immersed in a hot liquid. One method stipulates that the device to be tested be placed in liquid and then a vacuum should be applied while the observer watches for bubbles indicating a leak. This is a ramification of the basic principle employed, however, detectability can be improved as much as one order of magnitude.

There is little agreement on how sensitive the bubble test is. It has been variously rated from $>10^{-3}$ to $>10^{-5}$ Std cc/sec He.

There is agreement however on the fact that this test is very much affected by operator efficiency and operator fatigue. It is recommended that an operator should not work at this test for more than two hours continuously.

More specifically, the formation of bubbles depends on the thermal expansion of the contained gas. Their appearance, however, is easily overlooked by operators in the early stages of familiarization; even among experienced personnel results are likely to vary between individuals and with the same individual at various stages of fatigue. In part this is due to the transient nature of the phenomenon, the fact that not all surfaces of the device can be observed at the same time, the fact that light reflections from the package sometimes may be confused with bubbles and the fact that rechecks of test results are not reliable. A more basic problem is the fact that the internal gas pressure must compete with and exceed the liquid capillary filling pressure due to surface tension. Thus, below a certain pore size no gas exit is possible and the pore fills with the glycol. Multiple pores below the minimum detectable size could result in an extremely leaky package which would pass undetected. Furthermore, operator A using a bath at 150 C would pass a particular device that operator B using a bath at 160 C would reject because at the higher temperature the internal gas pressure is higher and the liquid surface tension lower, thus favoring gas exit in the minimum pore size region. It should be remembered, further, that this minimum pore size region is considerably above the upper limit of the conventional helium leak test.

Tests conducted by NR have proved that the bubble test is not reliable and not repeatable if ethylene glycol is used as the test liquid. Even at relatively high temperatures (125 C) glycol has a high viscosity and high surface tension which causes erroneous leak indications. It is conjectured that mineral oil produces similar problems.

FC-43 and FC-40 have been shown to be ideal substitutes for glycol and mineral oil as a bubble test medium.

Summary. - Presently used leak test techniques are summarized below and are compared in Table XV.

MIL-STD-883 Method 1014

A. He Fine Leak

1. Pressurize device to be tested in 100 percent He one hour minimum at 5 atmospheres minimum.

2. Transfer time between (1) and (3) is 30 minutes maximum.

3. Test device in a mass spectrometer calibrated for Helium.

4. Sensitivity Range 10^{-5} to 10^{-9} Std cc/sec He estimated. Leak rate limits are usually dictated by the application.

TABLE XV
COMPARISON OF VARIOUS LEAK TEST TECHNIQUES

Process Step	Rocketdyne SF_6	Science Center	Raytheon	MIL-STD-883 Method 1014 "A"	"B"	"C"	"D"	Autonetics AC477-0005 (Procurement)	Autonetics AA115-079 AA0607-010 (Process)	MIL-STD-202A	MIL-STD-202B	MIL-STD-202 III A
Evacuate	1 Hour		170°C Vac Bake 4 Hours		0.5 MM Hg	1 Hour 1 Torr						
Pressurization Inoculation	60 psig SF_6		Freon Time Unknown	5 ATM He	5 ATM KR-85	FC-78 90 psig	100 psig Dye Penetrant	65 ±5 psig-He	65 ±5 psig-He			Unspecified
Pressurization Time	1 Hour			1 Hour	12 Minutes Minimum	3 Hours Minimum		4-1/2 Hours He	4-1/2 Hours			Unspecified
Evacuate	He Flush	He Flush			0.5 MM Hg						1.5 inches Hg	
Transfer Time				1/2 Hour Maximum	4 Hours Maximum			20 Minutes	20 Minutes Maximum			Unspecified
Test Method	Gas Chromatograph	Metastable Helium	Weight Gain	He Leak	Geiger Counter	FC-43, -40 Bubble Test	Examine for Dye Penetration	He Leak Bubble Test	He Leak	Bubble Test Bath	Bubble Test Bath	Tracer Gas
Test Limit	5×10^{-7} Std cc/sec	5×10^{-7} Std cc/sec	50 μgram gain	1×10^{-7} Std cc/sec	1×10^{-8} Std cc/sec	Observe for Bubbles	$>10^{-5}$ Estimate	5×10^{-7} Std cc/sec	5×10^{-7} Std cc/sec	Observe for Bubbles	Observe for Bubbles	Unspecified
Sensitivity Range	0.013 Hole to 1×10^{-7}	0.090 Hole to 1×10^{-8}		10^{-5} to 10^{-9}	10^{-5} to 10^{-10}	$>10^{-5}$ Std cc/sec	10^{-2} to 10^{-5} Estimate	10^{-2} to 10^{-5} Estimate	10^{-2} to 10^{-9} Estimate	$>10^{-5}$ Estimate	$>10^{-5}$ Estimate	
Temperature						FC-43 or -40 at 125 C		Glycol at 125 C	Glycol at 150 ± 10 C	Oil at 125 C	25 C	

B. Radioisotope Fine Leak

1. Devices are to be placed in chamber and chamber evacuated to 0.5 mm Hg - time unspecified.
2. Chamber then filled with Kr-85/N_2 mixture to pressure at 5 atm absolute for 12 minutes minimum.
3. Kr-85/N_2 evacuated from chamber to 0.5 mm Hg.
4. Chamber refilled with air to atmos pressure.
5. Devices are then leak tested via scintillation counter within four hours of steps 1, 2, 3, 4.
6. Maximum leak rate allowable 1×10^{-8} atmos cc/sec of Kr-85 Sensitivity Range 10^{-5} to 10^{-10} estimated.

C. Fluorocarbon Fluid Gross Leak Tests

I. Leaks $> 10^{-3}$ std cc/sec

1. Immerse device two in. below surface of FC-43 fluid maintained at 125 C ± 5 C.
2. View device immediately through a magnifier against a black background.
3. A single bubble or stream of bubbles from package constitutes a failure. No evidence of bubbles constitutes a good device.

NOTE: Sensitivity Range 10^{-2} to 10^{-3} estimated.

II. Leaks $> 10^{-5}$ std cc/sec

1. Evacuate devices in vacuum chamber 1 hour (vacuum 1 Torr).
2. Backfill chamber with FC-78 without prior loss of vacuum.
3. Apply pressure of 90 psi for 3 hours minimum.
4. Remove devices and dry 3 ± 1 minutes in air.
5. Repeat steps 1 and 2 and 3 of Item C-I.

NOTE: Sensitivity Range 10^{-2} to 10^{-4} estimate.

D. Penetrant Dye Gross Leak Test

1. This test to be used on transparent glass encased devices only.
2. Devices shall be placed in chamber and completely covered with dye solution.
3. Chamber shall be pressurized to 100 psig for 2 hours minimum.
4. Remove pressure and wash devices with acetone, then with Alcohol, and then air-jet dry.
5. Examine devices with magnification 7 - 20X using UV light as illumination.
6. Any evidence of dye penetration is cause for rejection.

NOTE: Sensitivity range 10^{-2} to 10^{-5} estimate.

Raytheon Corp. leak test. - Information at this time is sketchy and not considered completely reliable.

1. Devices are baked in a vacuum oven at 170 C for 4 hours then weighed.
2. Devices are then immersed in a fluorochemical liquid (presumably freon) for an unstated time at an unstated pressure.
3. Devices are removed from liquid externally dried and weighed again.
4. A weight gain of 50 μgram per device constitutes a failure.

NOTE: Sensitivity - Unknown.

North American Rockwell Corporation - Rocketdyne Division proposed leak test (SF_6). -

1. Place devices one hour in Vac chamber.
2. Backfill vacuum chamber with SF_6 gas without first losing vacuum.
3. Pressurize chamber to 60 psig for one hour.
4. Open pressure chamber.
5. Place test device in test chamber and Helium flush for 5 sec.
6. Evacuate test chamber containing device to be leak tested through a gas chromatograph.
7. Any SF_6 gas escaping from "leaking" test device is detected and analyzed quantitatively by the gas chromatograph.

NOTE: Sensitivity Range = 0.013 in. diameter holes in package to 10^{-7} std cc/sec.

North American Rockwell Corporation proposed leak test. -

1. Place device to be tested in test chamber.
2. Flush lines and test chamber with He.
3. Determine background noise.
4. Read/record leak rate.
5. Remove device.

NOTE: Sensitivity Range = 0.090 in. hole to 10^{-8} std cc/sec He leak.

Autonetics Procurement Spec No. AC 477-0005

1. Fine leak - in accordance with MIL-STD-202 Method 112, condition C, Procedure III A.

2. Gross leak - in accordance with MIL-STD-202, Method 112, Condition A, except use ethylene glycol or H_2O instead of mineral oil.

3. The allowable leak shall not exceed 5×10^{-7} cc/sec.

Autonetics Process Spec AA0607-010 and AA0115-079

1. Pressure bomb in He at 65 ± 3 psig for 4 ± 1/2 hours.

2. Leak test devices within 20 minutes of removal.

3. Leak limit is 5×10^{-7} std cc He/sec

4. Units passing He test are then bubble tested.

5. Immerse device 1 in. below surface of ethylene glycol maintained at 150 C ± 10 C. Hold 10 sec.

6. Watch for bubbles. Any sign of escaping bubbles or growing bubbles shall constitute a leaky device.

NOTE: FC-43 may be substituted for glycol per Spec AA0607-010. Bath temperature is 125 ± 5 C.

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APPENDIX A. ANALYSIS OF DIELECTRIC DEFECTS IN SiO2

A.1 INVESTIGATION OF METHODS FOR THE DETECTION OF STRUCTURAL DEFECTS IN SILICON OXIDE LAYERS

BY
P. J. BESSER AND J.E. MEINHARD

INTRODUCTION

Present information indicates that passivation oxide is subject to two general process-dependent structural anomalies; ionic impurities in sound oxide (device failure modes: high or unstable MOS gate threshold voltages, inversion in bipolar devices), and unsound oxide penetrated by local dielectric defects (failure mode: metallization to substrate shorts). Although the latter problem has been cited frequently in the past, it has received comparatively little intensive study, partly because of the lack of adequate detection methods and partly because of the urgency to resolve the ionic impurity problem. The incidence of oxide dielectric defects, often called pinholes, is now recognized as a serious reliability problem, particularly with respect to MOS gate structures, metal intraconnections over thinned oxide regions, and abrupt thickness transitions in the oxide. The structural discontinuities comprising such defects offer far less resistance to electrical discharge than sound oxide which is capable of supporting fields up to 10^{-1} V/Å as compared with breakdown fields of about 10^{-4} V/Å for air. MOS gate voltage parameters seldom involve fields in excess of 10^{-2} V/Å which is well within the dielectric capability of sound oxide but considerably higher than that of gaseous insulation at ordinary pressures. Thus, shorting may occur regardless of whether the overlying metallization has penetrated a crack or pinhole in the oxide.

A major purpose of this investigation was to develop and evaluate test methods for the detection of dielectric defects in passivation layers. Selection of methods was based on the following performance criteria: nondestructiveness, reproducibility, recordability, and convenience of use as a process screening technique. Previously described techniques, such as the high temperature HCl etch[1] or chlorine etching at around 900C[2][3], fall short of this goal in terms of convenience and nondestructiveness. Metallization techniques likewise are impractical and lack the resolution necessary for the accurate location of defects. Both methods were useful, however, in corroborating results obtained with the new techniques under study.

Additional objectives were to gain an understanding of the physical nature of the defects and to determine, if possible, their process origins. For example, the presence of fast-etching loci in grown silicon dioxide, as reported by Lopez[4], would appear to contraindicate etch-thinning procedures for adjustment of oxide thickness. Defects therefore may be classified as inherent or latent, and may consist of physical openings in the oxide (pores, microcracks), thin spots, foreign inclusions (e.g., glass-forming metal oxides), or abrupt variations in SiO_2 density. The latter three categories would be more vulnerable to HF attack (fast etching) than adjacent sound oxide, and more subject to electrical breakdown as well. Likewise factors contributing to the formation of dielectric defects would include the inherent mismatch in thermal expansion between the oxide and the substrate, as well as initial and subsequent

*Proceedings, Symposium on Manufacturing In-Process Control and Measuring Techniques for Semiconductors, Phoenix, Arizona, March 1966, Vol II, p 16-1.

processing irregularities. Some of these process origins are: etch undercutting of oxide due to mechanical strains originally present or to poor adhesion of photoresist, localized etch spots due to mask flaws or variations in photoresist quality and application, local excesses of dopants or contaminant particles capable of forming silicate glasses at oxidizing temperatures, high temperature attack of active metals on oxide layers, and mechanical flexing of wafers by repeated growth and unbalanced removal of oxide layers. Conceivably, therefore, the elimination of dielectric defects might involve scrutiny of a large part of the major processing operations - a very difficult task without the availability of simple, recordable defect test methods.

TEST METHODS

Direct observation of oxide dielectric defects is hampered by their small physical size (approximately 2 to 20 μ diameter), the high reflectivity of the silicon and oxide surfaces, the lack of inherent color contrasts, and the apparent absence of a characteristic morphology for differentiating dielectric defects from other defects which are dielectrically sound. It became evident therefore that a suitable test method would require a combination of visual enhancement and transmission of charge at defect sites. Two of the more promising techniques, electrophoretic decoration and electrochemical autograph, are described below, followed by other techniques of more limited application. Succeeding sections deal with intertest correlations and process applications.

Electrophoretic Decoration

This technique provides a functional test (transmission of charge) and a visible record of the oxide anomalies sought. A passivated wafer, whose reverse side is etched and connected to a dc circuit, as shown in Figure A-1, is immersed in a dissociable dielectric fluid and the circuit completed by a copper probe situated in the fluid above the oxide surface. A mechanical stage is employed to adjust the relative position of the wafer under the probe. With a negative polarity (10-100 v) on the wafer, electrolysis at oxide anomalies is observed, under low power magnification, as trains of fine bubbles (identified as hydrogen by gas chromatography) associated with the electrochemical decomposition of the fluid or of minute traces of dissolved water. Concurrently, anodic attack of the copper probe releases colloidal particles of insoluble oxysalts of copper which are propelled by the potential gradient toward the oxide defects. This was confirmed by chemical and electron beam microprobe analysis of deposited material. Instead of plugging the defects, the insoluble matter accumulates on the surface of the surrounding oxide, covering areas ~100 diameters larger than those of the original holes. Figure A-2 shows the decorations on a portion of a wafer after removal from the cell and drying. The deposits were readily removed by acid treatment. A photograph of a decorated defect, and a microprobe photo of Cu radiation corresponding to the decoration, are shown in Figure A-3.

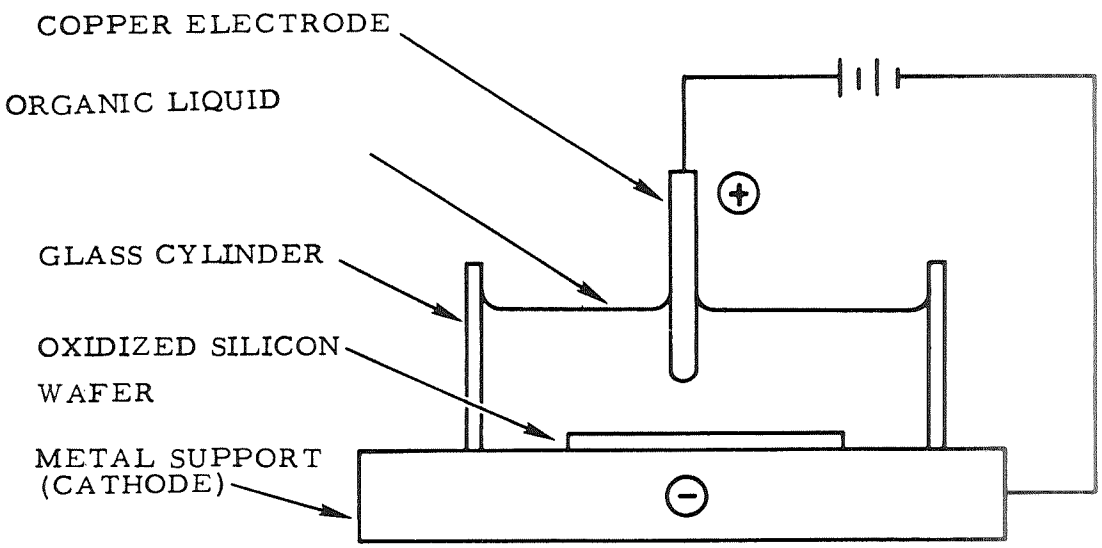


Figure A-1. -Electrophoretic Decoration Test Assembly

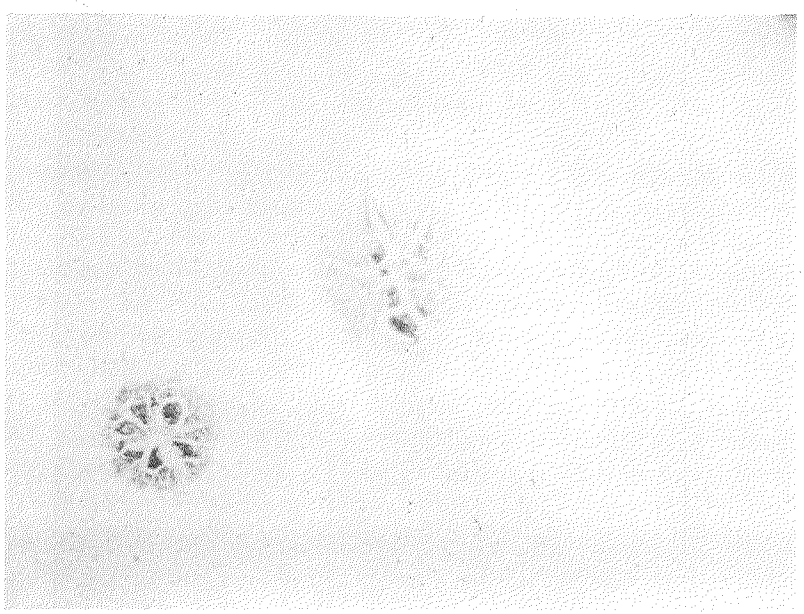
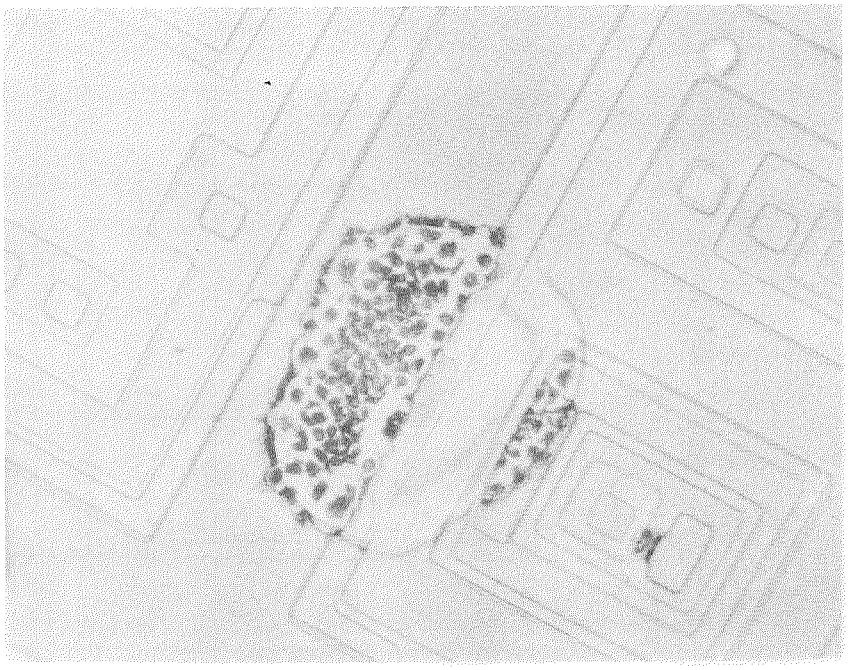


Figure A-2. -Oxide Defect Decoration After Fluid Evaporation. 100X



a. Photograph of decoration, 190X

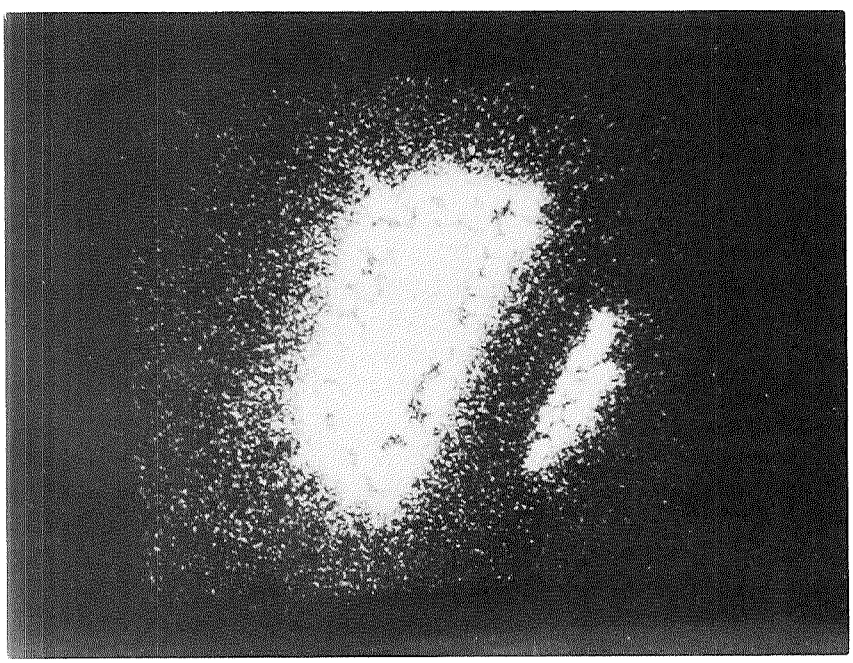


Figure A-3. - Photograph of Decoration and Cu Radiation From Electron Beam Microprobe of the Decoration

Verification of the method was obtained by correlation with other test methods. Reproducibility was checked by rinsing off the deposited material with dilute sulfuric acid and resubmitting the wafer to test. A typical sequence of this type on initial oxide is shown in Figure A-4. In its present form, this method employs a 20-point probe which decorates the complete wafer in 5-10 minutes. It is applicable as a pilot test and potentially useful as a screening test. The complete removal of copper by an acid wash has not yet been experimentally verified, and the potential gradient across the oxide and substrate has not been determined. The method is not yet completely qualified therefore as a nondestructive test. Further work is underway to characterize the nature of the decorated defects. Preliminary observations indicate that the decorated sites are actual pores in the oxide rather than regions of high conductivity.

In an earlier version of the test, attempts were made to achieve a visible record of the defects utilizing the electrolytic rather than the electrophoretic aspect of the reaction. A thin film of gelatin was applied to the wafer prior to immersion in the fluid. The electrolytically generated gas was trapped under the film causing delamination of the film from the oxide in the regions of gas evolution which revealed the characteristic oxide thickness color. The wafer could be removed from the cell with the film and trapped gases still intact. A photograph of a typical trapped gas pattern thus obtained is shown in Figure A-5. Subsequent tests, however, revealed a lack of reproducibility probably due to a nonuniform lifting of the gelatin film by the evolved gas. Various weakly acidic organic fluids such as acetone, isopropanol, and methanol are suitable for this process. Deionized and tap water were not found to be suitable.

Electrochemical Autograph

A simple electrochemical screening test for oxide defects is in the final stages of development. It can be applied to a wafer prior to final metallization or at any preceding process step, and shows promise of becoming a generally applicable technique for the location of oxide defects. It does not introduce metallic impurities and does not require large potential gradients. The method consists of making the silicon substrate an anode of an electrochemical cell and of revealing openings in the oxide by anodic oxidation of the electrolyte wherever it is in electrical contact with the underlying silicon.

The electrolyte employed consists of an aqueous solution of a benzidine salt (e.g., acetate or chloride) containing an organic nonsulfonated surfactant and a protective colloid. The function of the surfactant is to assist penetration of the electrolyte into small oxide pores. The protective colloid inhibits deposition of crystalline benzidine salts which tend to blur boundary definition. The colloid also promotes image sharpness by inhibiting lateral diffusion of dye. In principle other redox reagents will serve the same purpose as benzidine in this technique.

The electrolyte, soaked in a Millipore filter paper, is applied to the oxide surface and the assembly outgassed under vacuum. This treatment removes residual gas that might otherwise prevent pore penetration by the electrolyte. The assembly is then placed face down on a porous flexible support also soaked in electrolyte and situated on a stainless steel plate, as shown diagrammatically in Figure A-6. The purpose of the flexible support is to achieve conformal contact with the wafer surface,

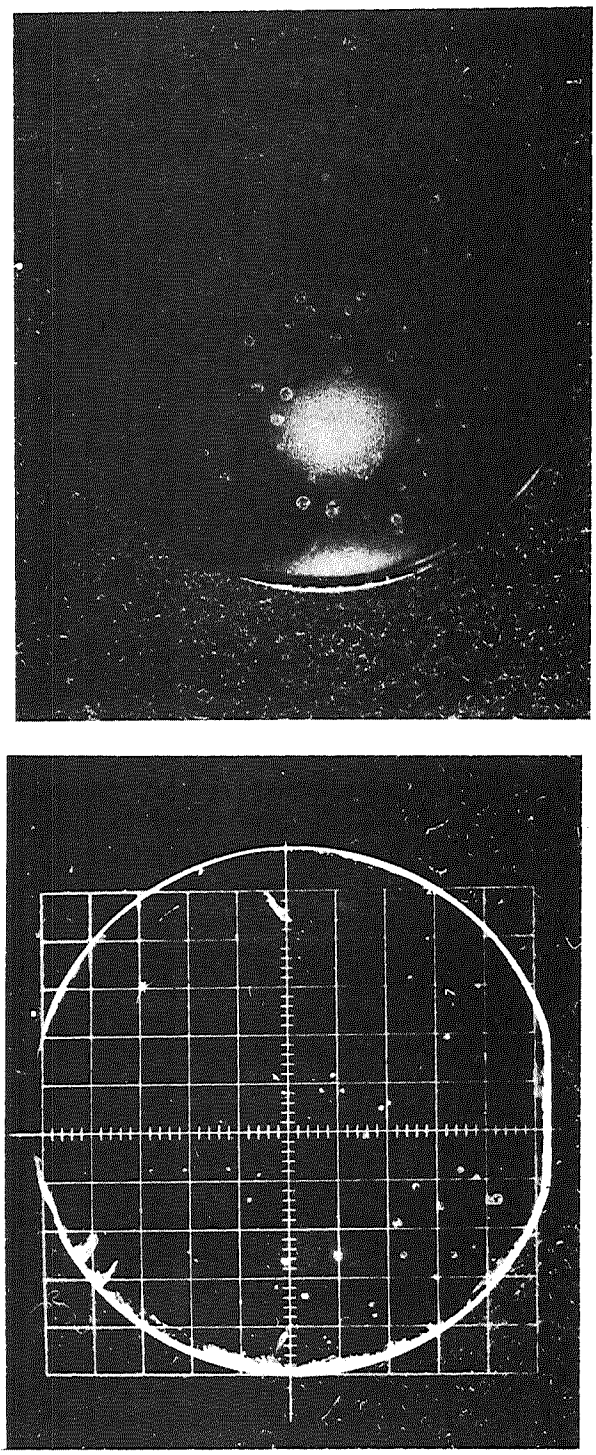


Figure A-4. - Sequential Electrophoretic Decoration of the Same Wafer

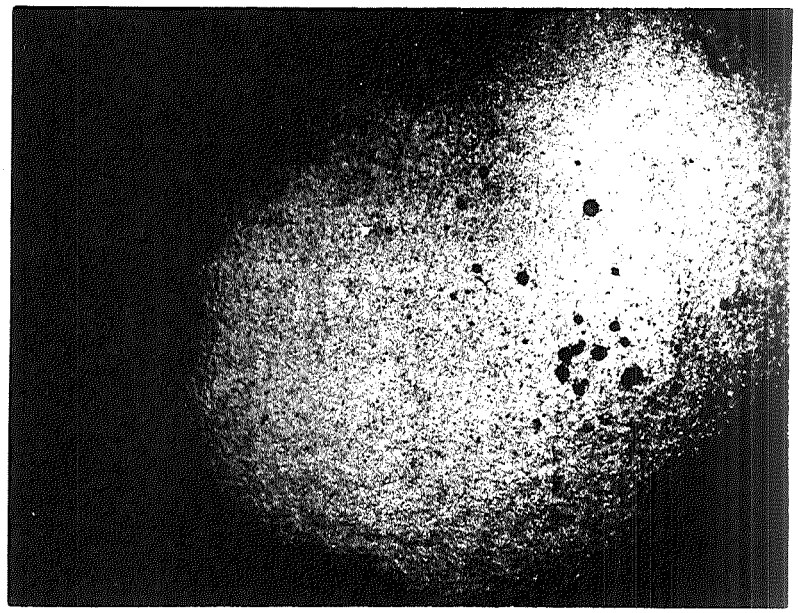


Figure A-5. - Trapped Gas Pattern Under Gelatin Film

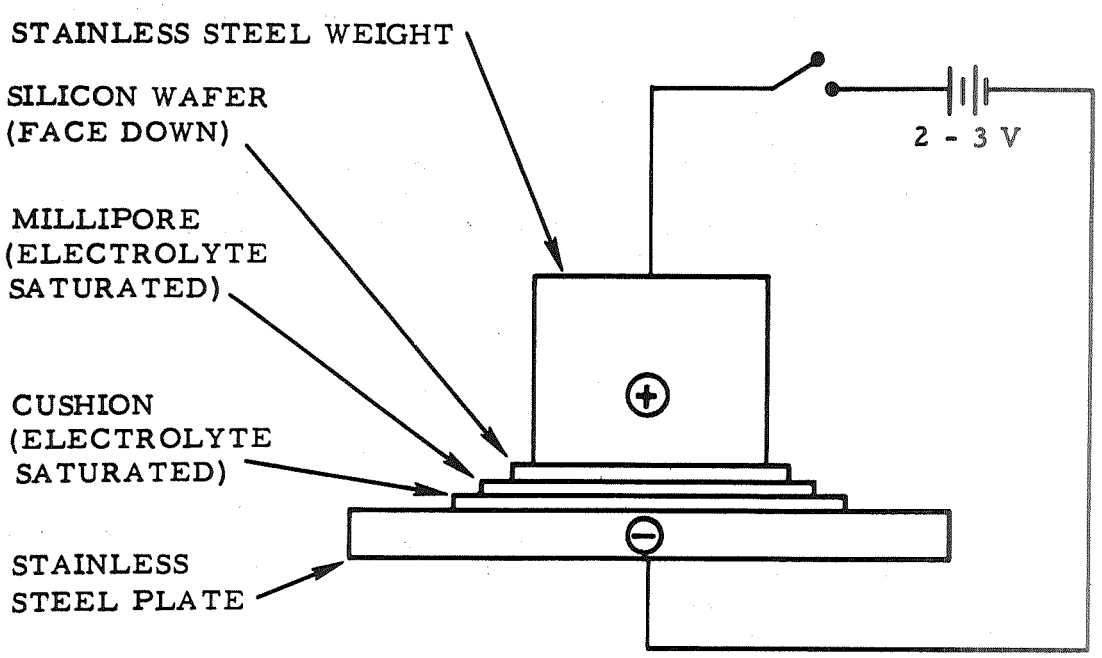


Figure A-6. - Electrochemical Autograph Assembly

which is not quite planar, and to minimize the possible transmission of a bending moment to the wafer through electrode pressure. The top stainless steel electrode, which is of sufficient mass to ensure intimate electrical contact between the assembled layers, is then placed on the oxide-free back (upper surface) of the wafer and external electrical connections made as illustrated.

Electrolysis is conducted at a potential of 2 to 5 volts for a 5-minute period. Anodic oxidation of the benzidine to a blue-black product stains the filter paper at points corresponding to openings in the oxide such as pinholes, contact and diffusion windows, and scribe lines. Following electrolysis, the apparatus is disassembled, and the Millipore filter paper is removed for microscopic examination and photography.

A photomicrograph of a typical wafer pattern after oxide removal prior to a diffusion step is shown in Figure A-7a and an enlarged view of the same pattern with an arrow indicating an oxide defect in Figure A-7b.

Substantial correlation has been obtained between this test and the electrophoretic decoration technique. Consecutive repeatability also has been confirmed many times. The detection limit is approximately 2 microns in hole diameter. This limit may be extended by more prolonged electrolysis. The wafer is easily cleaned from the electrolyte components with deionized water.

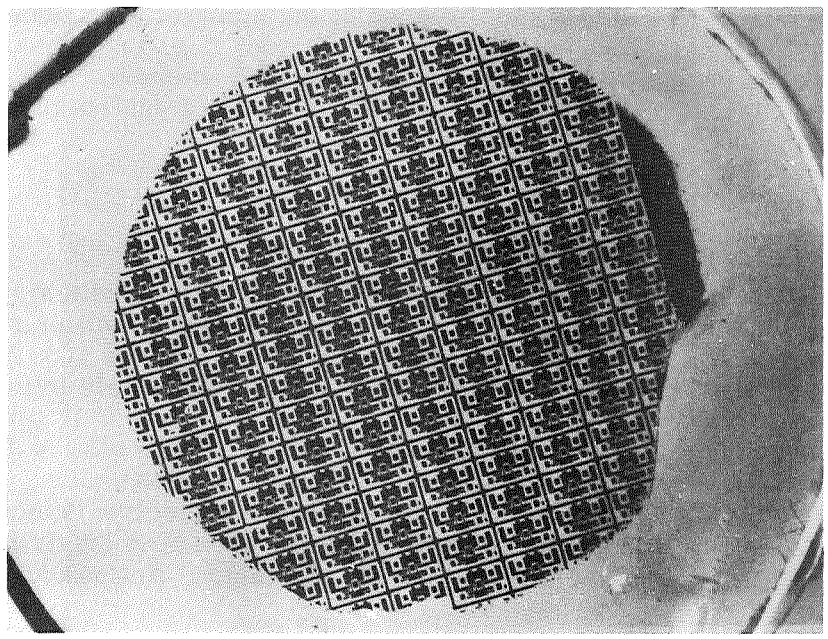
Electric Field Excitation Photography

Direct photographic recording of oxide defect sites was attempted using an alternating electric field to stimulate electron or photon emission from defect loci in or under the oxide placed in direct contact with a photographic film. Preferential exposure of the film was obtained, giving a light emission pattern that is developed only on oxidized wafers.

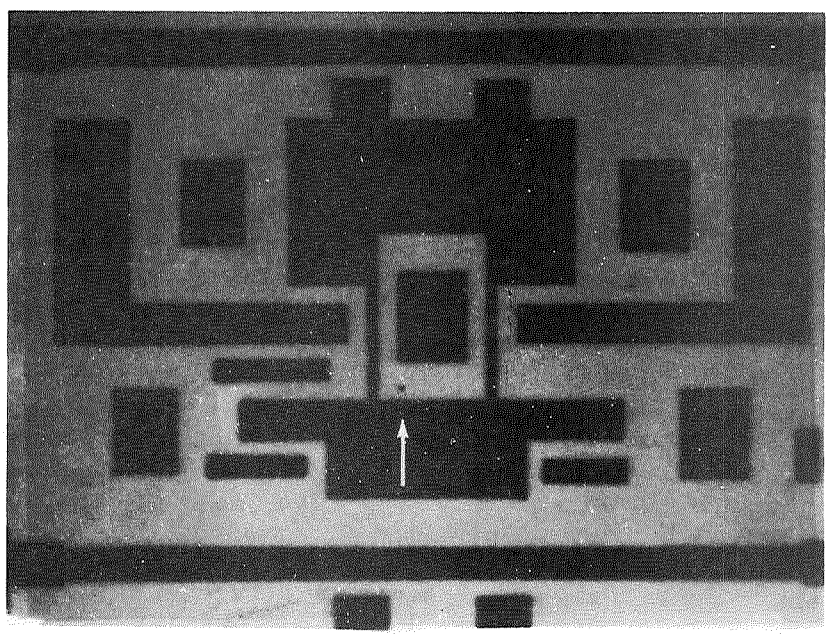
The field across the oxide and the silicon layers are unknown but may be high enough to damage device junctions in the silicon. Such damage would not necessarily occur only at oxide defect sites. Until direct evidence of non-destructiveness is obtained and the required exposure periods (1/2-2 hours) are substantially shortened, the method cannot be recommended as a screening test. It is a potentially useful tool in the investigation of oxide defect origins. Its correlation with the electric probe method is described in the following section.

Replicate Electron Microscopy

Although electron microscopy is impractical as a screening technique, it is capable of minute definition of surface morphology which may give clues to the process origins of oxide defects. The replica technique employed in this investigation involved the attainment of a large area replica. Such a replica can be used to study the original specimen after laboratory testing destructive to the original surface character. Thus, replicas made before and after a particular detection test can be examined to determine the effect of the test on the oxide.



(a)



(b)

Figure A-7. - Oxide Openings Displayed by Electrochemical Autograph Technique

The richness of detail produced by this technique poses a problem of interpretation. Only a very small percent of the observed structure is likely to delineate oxide defects capable of dielectric failure. Therefore, correlations of this technique with known sites of dielectric breakdown are especially important. Achieving such correlations, however, is a serious problem because of the minute field area covered at high magnification. Although many photographs were made, it was not possible to correlate unequivocally an observed structure with a dielectric anomaly. One correlation was made, however, by ordinary light microscopy of a replica prepared for for electron microscopy and is reported in the following section.

Microscopy

Observations by dark field, normal lighting (metallurgical illumination), and Nomarsky phase contrast were made in an attempt to develop a direct nondestructive procedure. Small defects in the oxide were readily observable at 500 to 1000 X. Covering an entire 1.25-inch diameter wafer by this method, however, is impractical because of the small field diameters (0.35 mm or 0.014 inch at 500 X; 0.17 mm or 0.007 inch at 1000 X) involved. Interpretation of observed structures also is difficult and requires correlation with other visual enhancement detection techniques. It is not yet possible to make any structural generalizations describing dielectric defects in the oxide. The method ultimately should be applicable to the inspection of single integrated circuit dice where topographical detail is available as landmarks. Automatic computerized scanning of whole wafers is foreseeable.

Preferential Etching

Chemical attack of silicon provides a direct visual enhancement of oxide holes where silicon is exposed. The etchant employed (25:3 HNO_3:HF) also corrodes the oxide to a significant degree, and probably causes a widening and deepening of the defects present as well as exposing silicon at fast etching sites as previously observed[4]. The test is therefore destructive. Defects are readily visible under dark field illumination at 500 X. The method suffers from the same limitations indicated above and is not applicable as a screening test. It holds promise, however, as a failure analysis test on defective integrated circuits. It also should be useful in stress-corrosion investigations of the origins of oxide defects.

Dye Autograph

This method was expected to locate oxide anomalies through dye or pigment color reactions similar to histological and biological staining techniques. The reasons for employing dyes are analogous in the two cases: to make morphological detail visible to ordinary light microscopy by the development of color contrasts. Although many experimental approaches were undertaken, no methods deserving continued investigation were found. The high reflectivity of the surfaces, and the chemical and physical inertness of the silica (in contrast to biological specimens) rendered ordinary staining methods ineffective.

Staining was attempted by applying soluble dyes, dye suspensions, pigment suspensions, in situ chemical reactions, commercial dye penetrants, and x-ray absorbers. Vacuum outgassing and pressurization were utilized as inoculation adjuncts, and visual enhancement was sought by applying monochromatic illumination and by ultraviolet excitation of fluorescent dyes.

Thermal Plotter

The infrared thermal plotter was considered a potential means of discovering "incipient" dielectric breakdown through an oxide defect covered with metallization. The heating effects associated with this phenomenon were found to be too small and too rapidly dissipated to be observed experimentally. Previously broken down loci dissipating approximately one watt (rms) were unambiguously detected and, almost without exception, could be related to readily discernible anomalies on the surface. Based on these negative results, the effort to detect incipient breakdown was discontinued.

Other techniques such as visual or photographic observation of defects in a low pressure gas discharge and luminescence of electrophoretically deposited phosphors were investigated but did not prove fruitful.

VERIFICATION OF METHOD

Inter-and Intra-Test Correlations

Verification of test methods under development required an independent proof relating analytical observations to anamolously low dielectric breakdown regions. Two techniques were used to induce dielectric breakdown: a bare metal probe in point contact with the oxide and vacuum-deposited metallizations on the oxide.

A potential was applied to the metal probe to break down sound oxide at known locations on the wafer. These were used as functional checks on other methods. Metallizations were deposited in the pattern shown in Figure A-8. The Al dots are 13 mils in diameter with an on-center spacing of 40 mils. Metal coverage is ~ 15 percent within the pattern boundaries.

The central test employed in this investigation was the electrophoretic decoration test. It was therefore essential to check its validity against dielectric breakdown distribution. Results employing the aluminized dot pattern are shown in Table A-1.

The results clearly indicate a correlation between defect density and dielectric breakdown. With only about 15-percent coverage by the dot pattern, a low coincidence with defects at low density is expected, as indicated for the first two samples. The high defect density in the third sample is reflected in the dielectric breakdown distribution.

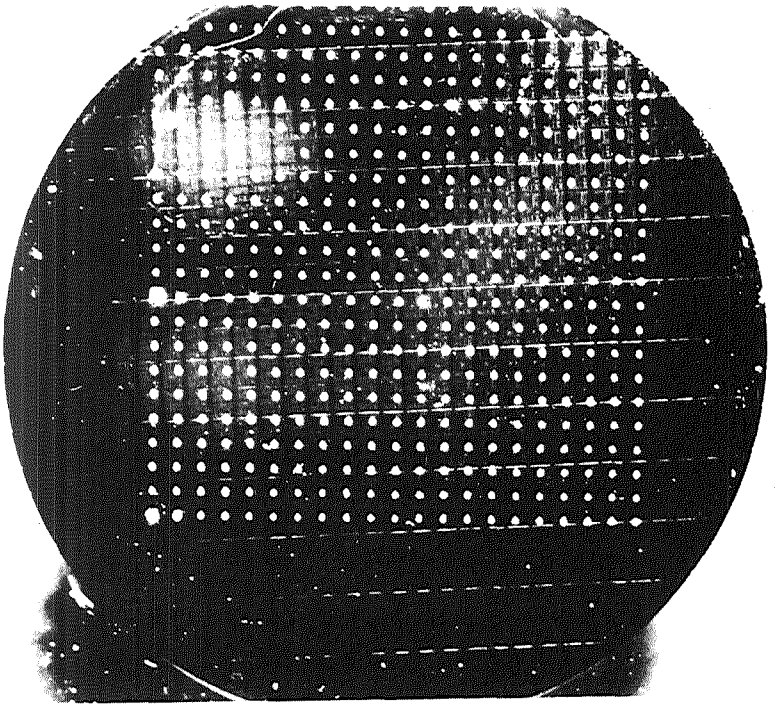


Figure A-8. -Metallization Pattern for Dielectric Breakdown Test

TABLE A-1
DIELECTRIC BREAKDOWN VS DECORATED DEFECT DENSITY

Wafer Description	Defect Density (cm^{-2})	Dielectric Breakdown Distribution
8000 Å Initial Oxide	< 5	% > 600V % > 500V % > 400V
		72 89 100
4000 Å Initial Oxide	< 5	% > 350V % > 300V
		0 100
Processed through contact oxide removal step, then 2000 Å of additional steam oxide regrown	400-600	% > 300V % > 200V % > 100V % > 40V
		11 44 89 100

Further verification of the electrophoretic decoration technique was obtained on known breakdown sites deliberately introduced by the bare metal probe. Positive identification of the breakdown sites by decoration was obtained in every case.

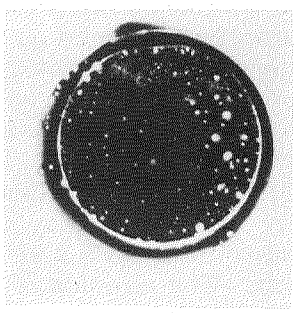
Correlation of the electrophoretic decoration technique with electric field excitation photography also was obtained, as represented in Figure A-9. Not all of the defects decorated with copper salts are successfully reproduced in the decoration photograph. However, the number density of spots on the field excitation photograph was still higher than that detected by decoration and may be due to the presence of thin oxide spots not detected by the probe method. Further investigation is required to establish correlation limits.

Cross-correlation between the electrophoretic decoration technique and the electrochemical autograph technique was performed on two wafers with initial steam grown oxide. One wafer was first decorated and photographed, and then subjected to the electrochemical autograph test while the reverse sequence was followed for the second wafer. Comparison of apparent defects determined by the two methods resulted in a significant, but not complete, correlation between the two methods. Extraneous sites were observed by both techniques. The autograph sites which did not correspond to decorations were, in general, very minute and may have been experimental artifacts unrelated to oxide defects, or to oxide defects of a size beyond the limit of detection by the electrophoretic decoration method. The absence of autograph sites at some decorations may be due to incomplete wetting of the wafer by the autograph electrolyte, a problem that has persisted in this technique, or an indication of induced breakdown at thin oxide regions by the higher fields employed in the decoration test. At the time of this writing, significant improvement in electrochemical autograph pattern coverage has been achieved, and it is expected that the correlation between the autograph and decoration techniques will improve. Since the decorated defects have not been definitely characterized solely as physical openings in the oxide, some of the decorations may correspond to regions of normal oxide thickness but of high conductivity, which might not be detected by the autograph.

Evidence of the Nature of Dielectric Anomalies

Some characterization of the microscopic structure of a defect was obtained using a surface replica prepared for electron microscopy. A photo-micrograph of this replica under normal illumination (at ~ 1000X) is shown in the upper photograph of Figure A-10. The centrally located oxide blemish (about 10 microns in diameter) in this photograph was indicated as a dielectric defect by the electrophoretic decoration method. The lower photograph shows the same defect after the decoration test. The oxide structure is seen to be relatively undisturbed by this treatment, but the underlying silicon has acquired a triangular etch-pit. Such etch-pits frequently have been observed after decoration testing. Since the silicon is at a negative potential during the test, the etch-pit formation cannot be associated with anodic oxidation. More detailed investigation may reveal that the etch-pits result from impurities or precipitates originally embedded in the silicon which act as precursors of the oxide defects and are expelled during the test. This result, plus the observation that deliberately induced breakdown loci are always detected by the decoration technique, apparently indicates that the test is not likely to introduce oxide defects where none previously existed, with the possible exception of unusually thin oxide regions noted above.

A preferential etch (25:3 HNO_3:HF) was applied to one of the two wafers used in the cross-correlation between the autograph and decoration methods. Considerable correlation between decoration sites and etch-pits in the silicon was found. However,



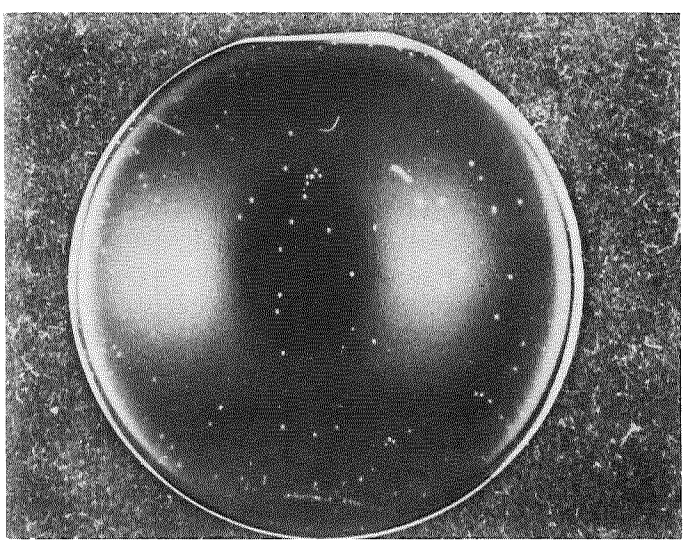


Figure A-9. – Top: Wafer Photographed by Electric Field Excitation; Bottom: Same Wafer Treated by Electrophoretic Decoration Method

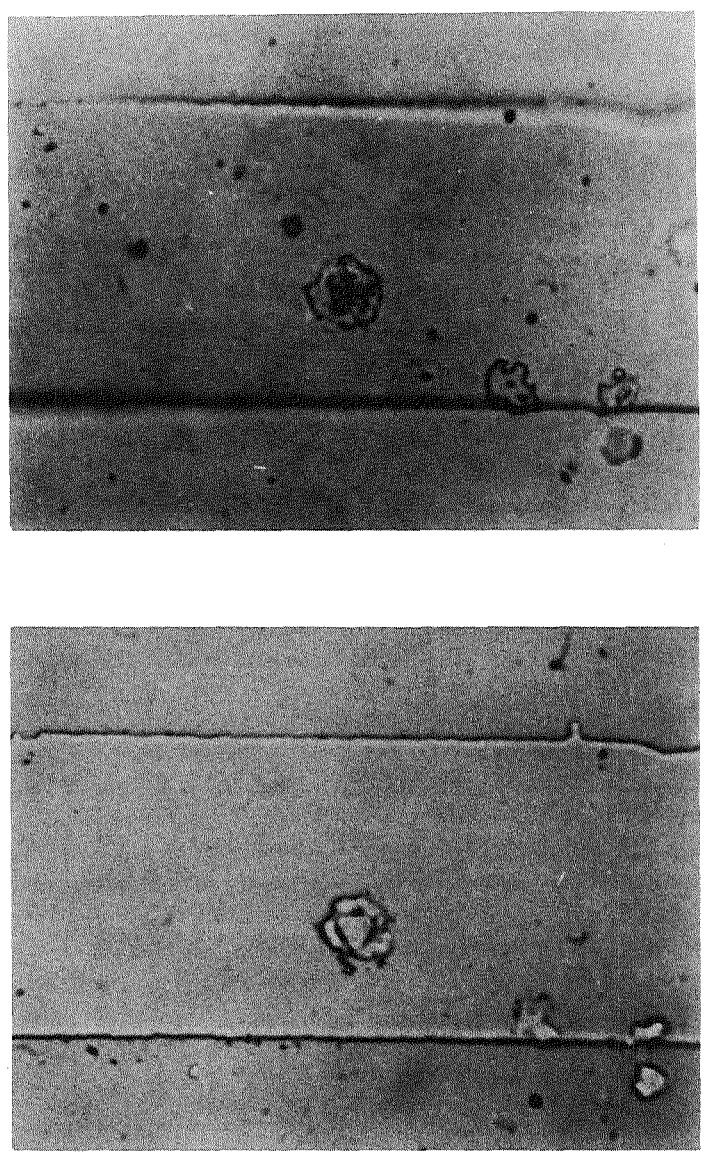


Figure A-10. - Oxide Defect Before (Top) and After Electrophoretic Decoration Test (Bottom). Top Photograph from Replica.
Parallel Boundary Interval: 42 Microns

since this etchant does attack the oxide to some degree, it does not resolve unambiguously the question of whether the decorated points correspond to actual oxide pores or to other anomalies such as fast-etching imperfections or thin spots.

The other wafer from the cross-correlation was subjected to a high temperature (1150 C, 10 minutes) HCl vapor etch which should not attack the oxide but preferentially etches any Si exposed by holes in the oxide. The etch pattern actually observed had a high degree of coincidence with the decoration pattern, but there were extraneous points in each case leaving the complete characterization of the defect nature unresolved.

Study by replicate electron microscopy is being continued in order to learn more about the physical nature of oxide defects and whether the electrophoretic decoration test induces defects at increasing probe voltages.

PROCESS CORRELATIONS

An additional objective of this program although somewhat ambitious for the allotted time and manpower, was at least partially fulfilled. The test data consisted principally of decorated defect counts and mechanical stress measurements on wafers selected at various stages of processing. The results are presented in Table G-2. Stress measurements were obtained from strain gage data, and Proficorder traces, before and after removal of one oxide layer from the wafer.

A number of inferences can be drawn from this tabulation. Most significant, perhaps, is the apparent gradual increase of both stress and defect density with processing (cf. wafer groups 1, 2, 5) and the defect healing effect of deposited oxide (wafer group 6). The deposition of uniform oxide, however, may be a continuing process problem, as indicated by wafer 6-B. The presence of an additional thermally grown oxide layer prior to final contact oxide removal was not very beneficial in reducing the defect count (cf. group 5).

The possible contribution of mechanical stress as a process origin of dielectric defects is somewhat subtle. A correlation of increasing stress with decreasing thickness (wafer groups 1, 3) is not accompanied by a corresponding increase in defect density in single-step oxides. Multiple-step oxides, however (wafer groups 2, 5), show a positive correlation between defect density and stress. To explain these observations, it can be postulated that mechanical stress induces dielectric defects through localized spalling of the oxide which serves to relieve a portion of the stress. Thus, highly stressed oxides, such as those in wafer group 5, would be under still higher stress at lower defect densities. The occurrence of such spalling would be expected to require a threshold stress for initiation which would decrease with increasing thickness of oxide. Thus, thinner oxides should tolerate higher stresses. Multiple heating and cooling, however, would be expected to increase spalling significantly through mechanical flexing (due to thermal expansion mismatch). Consequently, multiple-step oxides would be expected to display higher defect densities, as appears to be true from Table A-2.

TABLE A-2
OCCURRENCE OF DIELECTRIC DEFECTS AND MECHANICAL STRESS IN OXIDE AS A FUNCTION OF PROCESSING

Wafer Group	Description	Defect Density (cm^{-2})	Distribution	Average Stress (psi)
1A	8500 Å initial steam grown oxide	< 5	Random	29, 000
1B		< 5	Random	
1C		5-10	Random	
2A	8000 Å steam grown in	15	Random	39, 000
2B	2000 Å increments	45	Random	
2C		25	Random	
3A	4000 Å initial steam grown oxide	< 5	Random	38, 000
3B		< 5	Random	
4A	8500 Å - 2000 Å steam grown after first diffusion	< 5	Random	40, 000
4B		< 5	Random	
5A	Wafers after contact oxide removal step + additional steam grown oxide	90-100	Almost all along grid lines and at diffusion windows	62, 000
5B		400-600		
6A	Wafers after contact oxide removal step + additional deposited oxide	1-2	Random	
6B		2-4*	Random except where deposited oxide very thin; one area > 2000 cm^{-2}	

*Excluding high density region of thin deposited oxide.

Probably most of the inferred spalling does not produce dielectric defects directly, but small surface pits. Such pits would be especially vulnerable to etchant attack at later processing steps because of localized high surface energies. It would be possible therefore for such pits to grow into dielectric defects under succeeding chemical treatments. This conclusion is suggested by comparison of wafer groups 2 and 5. The former group experienced no intermediate chemical treatments, and the average defect density is only slightly higher than single-step oxide of the same thickness.

All of the data in Table A-2 were obtained on nonepitaxial wafers. Measurements on oxidized epitaxial layers have shown that the defect density and stress in thermally grown initial oxides ~ 8000 Å thick are not significantly different from those of oxides grown on nonepitaxial surfaces.

CONCLUSIONS

The electrophoretic decoration test provides a recordable, reproducible test for sites of anomalously low oxide dielectric strength. The test was checked by independent dielectric breakdown measurements and was used extensively in seeking process correlations with the incidence of dielectric defects. The test provides enormous visual magnification of the defects which are estimated from optical microscopy to be pores a few microns in diameter. Optical observation of a defect site before and after the probe test indicated that the test is not destructive to adjacent oxide although regions of thin oxide may be vulnerable to this treatment as suggested by other test correlations.

The electrochemical autograph test has overcome early problems of technique and is now capable of providing completely reproducible replicas of openings in oxide layers. It does not provide any appreciable magnification but appears to be nondestructive and noncontaminating. Complete correlation with the decoration technique has not been achieved but is expected to improve with present refinements and the continued characterization of oxide defects.

The contact photography test shows promise, but additional development and correlation will be needed before it can qualify as a useful screening or detection technique. The other methods and approaches that were investigated in some cases assisted in the verification of techniques and the interpretation of results, but have not appeared promising enough as screening tests to warrant continued development.

The decoration and autograph techniques are most applicable to testing at the wafer level. Although either is potentially available for use at any process stage, they are more efficiently applied in a complementary manner. The decoration technique is generally superior when applied to an oxide with no intentional openings (i.e., initial oxide or after a diffusion-oxide growth step), whereas the electrochemical autograph technique is more convenient when applied to a wafer with diffusion windows, grid lines, or contact windows opened in the oxide to provide a reference pattern for the location of defects on the autograph. The resolution of the methods is unknown but is at least of the order of a few microns.

Analysis of the test observations indicates an increasing incidence of dielectric defects with processing. The results also showed that deposited oxide is effective in reducing such defects but may be a difficult process to control. Evidence that residual mechanical stress in the oxide plays a significant role in the incidence of defects was obtained. Interpretation of this evidence led to an oxide spalling hypothesis as a possibly significant source of defect sites. It was also concluded that high stresses associated with thinner oxides do not necessarily portend increases in defect density. No particular processing step was indicated as a predominating source of dielectric defects.

Continued investigations are expected to reveal more clearly the physical structure of the observed defects and their process origins. Further examination of the nondestructive and noncontaminating aspects of these tests, and additional intercorrelation of test results, also are needed to define completely the limits of applicability and resolution of these methods.

Acknowledgements

Valuable suggestions and experimental contributions were made by the following: J. L. Kersey, J. P. McCloskey, C. G. Jennings, C. W. Scott, and S. Merrill.

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A-2. SUMMARY
FACTORS INFLUENCING DIELECTRIC DEFECTS IN SILICON OXIDE LAYERS*

BY
P. J. BESSER, J. E. MEINHARD, AND P. H. EISENBERG

Abstract

The incidence of dielectric defects in thermally grown silicon oxide films has been investigated utilizing previously developed defect detection techniques. The oxide layers exhibited a strong dependence of dielectric defect density on film thickness, on moisture content of the oxidizing ambient and on type and concentration of the substrate dopant. Characterization of the defects indicates that they are primarily pores in the oxide layer. Mechanical stress resulting from the mismatch in thermal expansion characteristics of the silicon and the oxide is postulated as an important defect-producing mechanism and the experimental results are interpreted on this basis.

Procedures. -- Silicon wafers with various dopant concentrations and procedures were procured and thermally oxidized at temperatures from 1050 C to 1180 C in various ambients. Films were grown in the thickness range from 850 Å to 12,000 Å. Two techniques were utilized for defect detection - electrophorite decoration and electrochemical autograph.

Results. -- Application of previously developed methods for the detection of dielectric defects to silicon oxides formed on silicon wafers has made possible a determination of the dependence of dielectric integrity on various factors involved in device fabrication. Most of the results can be consistently explained by a model which postulates the mechanical stress developed as a result of the thermal expansion mismatch between Si and SiO_2 as a principal source of dielectric failures by the mechanism of film rupture. Other possible defect origins are being investigated but have not been verified.

Below is a detailed discussion of the results obtained in terms of various parameters.

Film thickness. -- The experimental data demonstrated that the dielectric integrity of virgin thermal oxides is strongly thickness dependent. This variation with thickness is shown in Figure A-11 for the average of a typical group of samples oxidized under the same conditions. All of the oxides studied show this same functional dependence of defect density and thickness; but the position and shape of the curve are influenced by a number of factors, some of which are considered in this paper. The number of defects is relatively independent of thickness in the range greater than 4000 Å but generally begins to increase gradually in the 2000-4000 Å range with a very rapid increase below 2000 Å.

*Appendix A-2 is a summary of a paper delivered at the 1966 Fall meeting of the Electrochemical Society, Philadelphia, Pa.

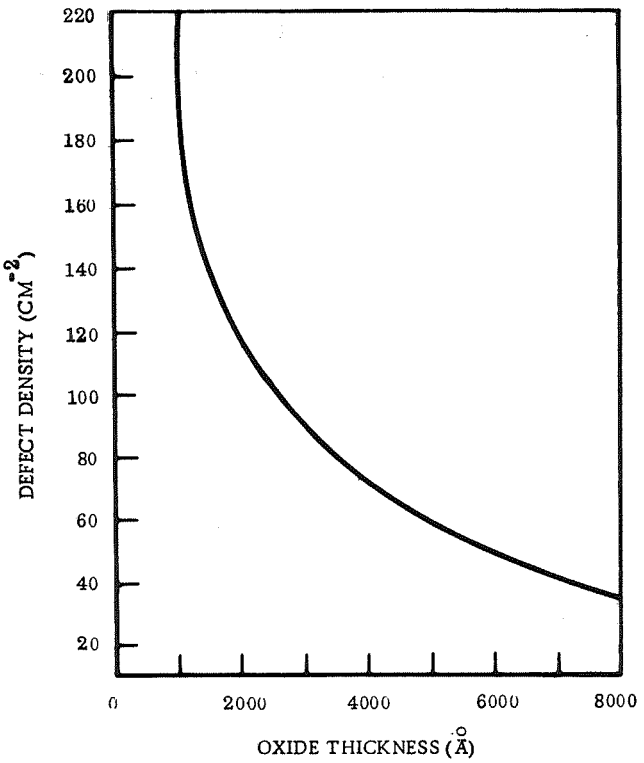

Figure A-11. Defect Density Variation in Virgin Thermal Oxide

Moisture content of oxidizing ambient. -- For oxides of a given thickness, the number of defects/cm^2 was found to be dependent on the amount of water vapor in the oxidizing ambient.

Etched oxide layers. -- The same functional dependence of defect density on thickness that was determined on virgin oxides was also observed in oxide layers as they were thinned by etching. However, the defect density at a particular thickness was greater for the thinned oxide than for the unaltered oxide. When the etched layer is regrown to successively greater thicknesses, the defect density decreases in a manner closely approximating the etch-back curve rather than the curve for the as-grown oxides.

Silicon surface preparation. -- The effect of preoxidation surface treatment of a silicon substrate on defect density was also investigated. The wafers were oxidized under identical conditions and the defects measured on each group. The oxide thickness was 1200 Å and the results indicate that the effect on surface preparation on oxide dielectric integrity is relatively small in this thickness range. The general trend, however, was that oxides grown over surfaces in which the chemical polish was the final step contained fewer defects than those grown on wafers with a final mechanical or mechanical-HCℓ vapor polish.

Oxidation temperature and growth rate. -- A dependence of dielectric integrity upon growth temperature (or growth rate) was observed for oxide layers less than 2000 Å thick grown in dry O_2 over heavily boron-diffused regions. The layers grown at lower

temperatures contained more defects than those of the same thickness grown at higher temperatures. The variation with growth temperature became less as the film thickness increased. The results of the stem and wet N_2 oxidations also indicate an absence of growth rate effects in thicker layers although it may be that the presence of moisture is the dominant influence in wet oxides.

Substrate impurity type and concentration. -- Preliminary work in other phases of this investigation indicated that oxides grown over heavily boron-doped regions in dry O_2 were more defect-free than those grown over regions of low boron concentration or over phorphorous-doped regions. This suggested a possible influence of substrate impurity type and concentration on the integrity of the grown oxide. Since the amount of impurity incorporated in the oxide and the degree of partition of impurity between the oxide and silicon are partially dependent on the growth conditions, it was decided to vary impurity type, impurity concentration, and oxidation conditions on a group of samples to determine the combined influences of impurity and oxidation procedure, densities found and the poorer quality of the etched layers. Also, from previous discussion, terminating with a wet (rapid) oxidation step may produce in the lower portion of the film a higher incidence of substrate-related oxide defects.

Discussion

Consideration of the experimental data from this investigation in conjunction with the present knowledge and conception of the silicon oxide structure and the results of other studies on the properties of SiO_2 and silicate glasses leads to a consistent picture of the nature, structural roots, and process origins of regions of anomalously low dielectric breakdown.

Most of the experimental data can be explained by considering oxide dielectric defects to result from microscopic cracks or fissures in the layer produced by the mechanical stress resulting from the differential thermal expansion characteristics of the Si-SiO_2 system. It should be pointed out that glass always fails from a tensile component of stress even when the loading is compressive. Since the stress originates at the interface between the silicon and the oxide, it is expected that ruptures in the oxide will occur at this boundary and propagate toward the outer surface of the oxide. In thicker films the propagating stress, which should be partially relieved by the rupture of the oxide, may not be sufficient to allow all the defects to penetrate the entire thickness of the layer. This could account for the observed decrease in defect density with increasing oxide thickness. In an oxide grown to any thickness on a silicon wafer, there is presumably a distribution in the local stress levels. Those regions which are just below the rupture level or see only compressive components of stress would be attacked more rapidly by chemical etching. This is thought to be the basis of the higher density of defects in an etched film as compared to a virgin layer of the same thickness. The ineffectiveness of thermal regrowth of oxide as a defect elimination technique is apparently a result of the appearance of additional defects in previously sound oxide as a result of the thermal (and stress) cycling. This was demonstrated by measuring the defects on an initial oxide, taking the wafer through five temperature cycles from room temperature to 1150 C in an inert atmosphere, and remeasuring the defect density. It was found that the temperature cycling produced an order to magnitude increase in the number of dielectric flaws.

The beneficial effect of moisture in the oxidizing ambient is attributed to the incorporation of hydroxyl groups in the oxide and the resulting improvement in the oxide thermal expansion characteristics relative to the silicon. The contribution of this factor to improved oxide dielectric quality can be partly offset by the ion trapping characteristic associated with the exchange of protons for other positive ions at these sites. The variation of the defect density versus thickness characteristic with growth temperature can be explained on the basis of incorporation of more boron in the oxide grown at the higher temperature. This is a result of the increased ratio of oxidation rate constant to diffusion coefficient of the impurity in the silicon as the temperature is increased. Since the setting point of the oxide is ~ 1000 C, the temperature range over which the mechanical stress develops is the same for each oxidation temperature and may even be less for the more heavily boron-doped oxide. The 1100 C oxide should also have a higher expansion coefficient resulting in a lower stress level and fewer ruptures in the film as experimentally observed. Also, as shown in Figures A-12 and A-13, the impurity profile in the oxide is such that the best match in expansion characteristics occurs at the oxide-silicon interface where the stress originates.

The data indicate that the surface preparation techniques investigated had relatively little influence on the oxide integrity. Preliminary work on wafers deliberately contaminated with particles at levels differing by an order of magnitude has shown little variation of oxide integrity with particulate contamination.

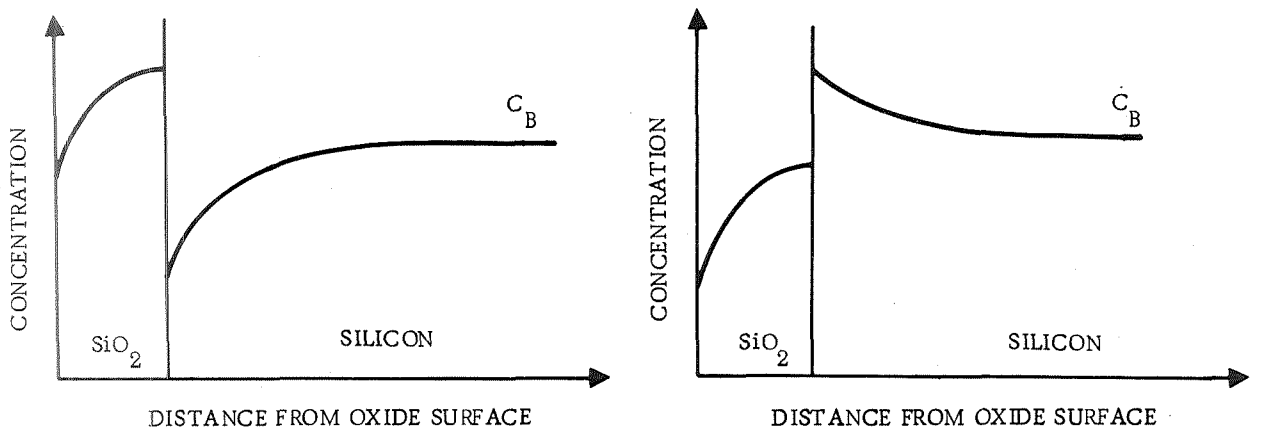

Figure A-12. Impurity Profiles in Oxidized Silicon Wafers. C_B Denoted Bulk Impurity Concentration (From Grove, et al, Ref 20)

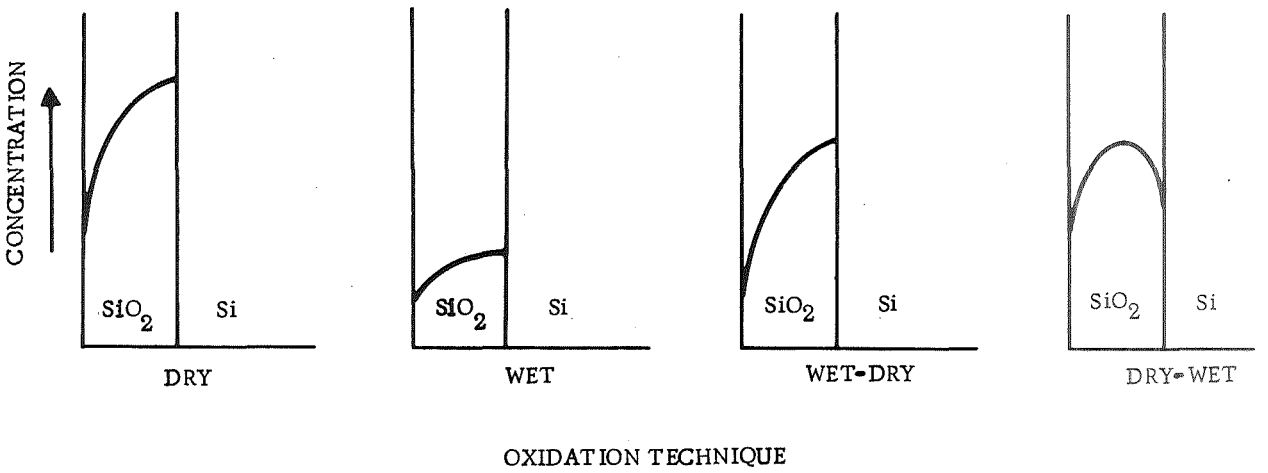

Figure A-13. Postulated Boron Distributions in Thermally Grown Oxides

A-3. OXIDE DEFECT TEST PROCEDURE

Scope

The purpose of this test procedure is to detect the locations of dielectric defects in layers of silicon dioxide grown on silicon wafers and to provide a semiquantitative estimate of such defects per unit area. The test is applicable to an oxide thickness range of 1000 to 15,000 Å. It also is applicable to pyrolytic oxide layers provided they have been adequately densified. Poorly densified layers are disrupted by the test.

Specimen

The specimen shall consist of a silicon wafer derived from any planar processing step, prior to metallization, in which new oxide has been grown or where bare silicon has not been intentionally exposed, as in window etching.

Apparatus

The apparatus consists of a microscope, test cell, anode clamp, and power supply. Auxiliary equipment includes a hand counter and a diamond scribe.

The microscope to which this procedure applies is a Leitz Ortholux, fitted with a mechanical stage. If another microscope is substituted, the wafer area subtended by the 50X optics must be recomputed to give accurate defect densities. Alternatively, a defect count of the entire wafer may be taken which is then divided by the wafer area to give defect density. This alternative is impractically slow for high defect counts, such as those encountered with thin oxide layers.

The test cell consists of a heavily gold-plated brass cup affixed to an insulating substrate which can be conveniently clamped by the mechanical stage. The cup is circular with an inner diameter at least 3/16 in. greater than the largest diameter wafer to be counted. The present cup, with an i.d. of 1-3/4 in., is adequate for all wafers normally encountered. A small radius filet is machined into the wall-bottom intersection to reduce electrochemical erosion. The cell depth is 1/4 in. A binding post of electrical connection to the power supply is mounted on the external wall of the cup.

The anode for the cell consists of an independently mounted wire loop with provision for lowering it in a precisely parallel orientation over the wafer contained in the cell. The wire loop at its end, is formed in such a manner that it clears both the microscope objective and the upper edge of the cell wall, yet permits a limited vertical traverse for precise adjustment of displacement over the wafer. The wire is affixed to a metal arm pivoted at its other end for movement in a vertical arc and mounted in a block fashioned from insulating material, such as lucite. Also mounted in the block is a rotatable shaft, parallel to but displaced from the pivot axis. The rotatable shaft

carries an insulating cam in contact with the metal arm which, by means of an external insulating knob, can be manually rotated to adjust the height of the metal arm supporting the wire loop. Means for locking the rotatable shaft in place is provided by a set screw in the insulating block. Electrical connection to the power supply is made directly to the metal arm or to the pivot shaft on which it is mounted. The insulating block on which the adjustable anode is mounted is supported independently of the microscope stage or test cell.

The power supply shall consist of a 50v dc source with 10 to 15K impedance. Provision for the selection of other voltages is desirable if deviations in electrode spacing from that specified herein are anticipated (Note 1).

The hand counter shall consist of a mechanical key type register, or equivalent.

Reagents

Methanol (anhydrous, Reagent Grade)

Hydrofluoric acid (48 percent, Reagent Grade)

Hydrochloric acid (Reagent Grade)

Water (distilled or deionized)

Apiezon wax (or equivalent, for masking)

Trichlorethylene (or other solvent for Apiezon wax)

Procedure

Preparation of sample. -- Keep wafers protected in suitable containers at all times. Handle only at extreme edges, preferably with plastic-tipped tweezers and preferably only in the zone making contact with the quartz boat during oxidation. Avoid as much as possible all mechanical contacts to the surface to be tested (Note 2). Open the back oxide for electrical connection by scribing with a diamond stylus. Alternatively, remove a small area of oxide using Apiezon wax as a mask and hydrofluoric acid (diluted 1:1) as an etchant (Note 3). Carefully rinse off acid, dry, dissolve off Apiezon wax with solvent, follow with isopropanol or acetone rinse, blot dry.

Performance of test (bubble mode). --

1. Set microscope for 50X magnification. Connect the wire loop to the positive terminal of the power supply. Insert wire loop anode into the field and adjust level, by means of the cam control knob, until the top of the loop is exactly in focus. Secure it in this position using the set screw provided.

2. Clamp gold plated brass dish on microscope stage below anode. Connect to the negative terminal of the power supply. Fill dish approximately 3/4 full of methanol from a polyethylene dispensing bottle.

3. Insert wafer into center of dish with scribed (or etched) surface down. Add methanol to top of dish.

4. Slowly raise stage carrying the dish until the previously positioned wire loop anode is immersed and just touches the oxide surface to be tested.

5. Note the fine-adjust drum reading on the vertical traverse mechanism, then lower stage 300μ from this position. This should place the surface of the wafer in focus, rather than the loop anode, because of the refractive effect of the added methanol. For this reason, replace any methanol lost by evaporation over extended periods in order to maintain proper focus (Note 4). Do not readjust stage level, as gap between anode loop and wafer should remain relatively constant (Note 5).

6. Turn on voltage supply. Defects in the oxide are observed as emissions of fine trains of hydrogen bubbles (Note 6) from the wafer surface. Count each emission site as a single oxide defect. Occasionally emission will occur only a short time from a particular site and then stop. This probably is due to gas polarization which prevents fresh methanol from penetrating to the exposed silicon. Count as a defect even if only a momentary emission is observed.

Low counts. -- If less than five counts per field at 50X are observed this is arbitrarily classed as a low count wafer. In this case scan the entire wafer using the x-y adjustment of the mechanical stage to reveal successive fields. Record bubble emission sites on the hand counter. Where extreme variations in defect densities are observed on a single wafer, as sometimes occurs, report only the defect density characteristic of the wafer as a whole, omitting anomalous regions. This may be done using the high count method described below. The reason for this is that anomalously high regions usually are indicative of local irregularities, such as scratches or deformations in the silicon, and are not generally characteristic of the oxidation procedure itself. The presence of anomalous regions, however, should be recorded and the sources sought if recurrent. For analogous reasons the outer edges of the wafer and the portion previously in contact with the quartz boat also should be omitted. A correction for these areas is therefore estimated and deducted from the total area of the wafer. Divide the total count tallied on the counter by the corrected wafer area and report as defects/cm^2.

High counts. -- When five or more counts per field at 50X are observed proceed as follows: count fifteen (15) separate fields located by successive x-y adjustments of the mechanical stage, taking care to avoid anomalous regions. Report the entire tally as defects/cm^2, as there are 15.1 fields (at 50X on the Leitz Ortholux Microscope) per cm^2. Alternatively, count any number or fields not less than ten, maintaining an accurate count of the number of fields. Divide the total defect tally by the number of fields counted, then multiply by 15.1 to obtain defects/cm^2. To obtain standard deviation, record the count of each field independently, sum, take the average and compute average percent deviation therefrom.

7. Turn off voltage supply and lower stage to a point where the cell can be conveniently removed. Grasp wafer carefully with tweezers and lay face up on blotting paper to dry. If three successive tests have been performed,

discard the methanol, which has picked up moisture from the atmosphere and electrolysis products from the test (Note 4). At the same time, clean the test cell and the wire loop electrode as follows: Rinse with hydrochloric acid (diluted with water 1:1) to remove accumulated metal salts; rinse with water; rinse with methanol and allow to dry, or reassembly for next test (Note 7). If wafer is to be reclaimed for further investigation, allow to stand 10 minutes in hydrochloric acid (diluted with water 1:1) to remove deposited salts; rinse thoroughly with water, then with methanol. Allow to dry in dust free environment.

Performance of test (decoration mode). -- In the decoration mode a wire loop electrode of copper, nickle or nichrome is used because the decoration depends on the anodic attack of this electrode. This attack may be accompanied, or preceded, by anodic oxidation of the methanol to formic acid. Thus, the metal salts formed may be hydrates or hydrated formates. Regardless of their exact composition these salts are insoluble in the methanol and, being positively charged, are propelled as colloidal particles away from the wire loop anode. They are attracted to, and collected by, cathodic sites on the wafer surface, namely, oxide defect sites where silicon is exposed as a negative electrode. The process is analogous to electrophoresis and, for this reason, is often referred to as "electrophoretic decoration." The colloidal salts collect in the form of rosettes around each functional defect, thereby providing an enormously magnified marker at the defect site. The defect sites are conveniently observed under low magnification (10X to 20X) and may be counted or photographed. Metal residues corresponding to the anode used remain at the defect sites even after an acid wash, as confirmed by electron microprobe examination. The microprobe therefore can be used as an alternative defect detection method after decoration. The metal residues render the decoration mode unfit for screening purposes but convenient for control and documentation purposes.

Follow steps (1) through (5) as defined for the bubble mode test.

6a. Turn on voltage supply. Slowly traverse the entire wafer by means of the x-y adjustment control knobs of the mechanical stage. Continue until visible build-ups of metal salts have collected around defect sites (approximately ten minutes) using the 50X magnification to monitor the process.

7a. Turn off voltage supply and lower stage to a point where the cell can be conveniently removed. Carefully drain off the methanol, taking care not to disturb the decorations. Using tweezers, gently remove the wafer from the cell and place face up on blotting paper to dry. Clean the cell and electrode as described in previous Step (7). Count the defects according to the most appropriate of the methods described in previous Step (6).

For low defect densities where the entire wafer is counted use wide angle low magnification. Alternatively, photograph the wafer at 3X to 5X magnification and perform the counting analysis on the photograph. Convert all counting data to defects/cm^2. If recovery of the wafer for other investigations is anticipated, clean as described in previous Step (7).

Safety precautions. -- Voltage: The exposed metal surfaces of the test cell and of the wire loop anode and supporting arm, particularly in close proximity to metal parts of the microscope, may constitute a hazard at a potential of 50 v dc. Apply voltage

only during performance of the test, taking care not to touch any charged metal surface. Avoid touching the microscope, or any other metallic object, with the exposed metal surfaces either of the test cell or the wire loop anode. Always check for clearances before turning on voltage. Avoid touching the test cell directly with the wire loop anode while potential is applied. Sparks are produced which damage the plating of the test cell.

Hydrofluoric Acid: Concentrated hydrofluoric acid is a highly caustic liquid, penetrating the skin rapidly and causing deep and painful wounds. It also acts as a systemic poison. Use only in a hood provided with adequate rinsing facilities. Use of rubber gloves is not recommended unless a rigid glove inspection procedure prior to use is adopted.

Solvents: Avoid extended or copious inhalation of methanol vapors which are poisonous. Similarly avoid inhalation of trichlorethylene which may induce temporary "black-out" and has been known to cause liver damage.

Precision

Repeatability generally is within five percent with one operator and one apparatus except for very thin oxides. With different operators using the same apparatus reproducibility may vary as much as 20 percent but can be brought down to around five percent with careful coordination and duplication of test conditions. Reproducibility on different apparatus is not known.

Accuracy

No assessment of accuracy can be made without an exact definition of what constitutes an oxide flaw. Such flaws can be defined functionally on the basis of dielectric breakdown during systems use. Such breakdowns, however, are determined by the path length and the applied voltage, factors which cannot be standardized. The test method likewise makes use of dielectric breakdown at the site of the oxide flaw, standardized empirically at a potential well below the dielectric strength of the oxide but high enough to constitute a significant indicator of oxide quality. In general this potential will exceed by some variable amount the gradients to be encountered in future systems use. Accuracy, therefore, will tend to err on the positive side in inverse proportion to the rigors of use conditions.

Dimensional Limits

Defect size resolution is estimated at 0.5 μ on the basis of electron microscopic evidence. Gas polarization at very small defects often interferes with their detection.

Notes

1. Adjustments in voltage may be required for other variations in test conditions (see Note 4) or for samples where the oxide layers are extremely thin.

2. Gentle wiping of an oxide surface with a cotton swab has been found to increase the defect count, probably by mechanically dislodging some silica fracture chips that would otherwise except detection.

3. Do not remove entire back oxide, as this introduces warp in the wafer and increases the density of observable defects in the remaining oxide layer.

4. Anhydrous methanol absorbs moisture from the air and should be replaced periodically, as detailed in Step (7), rather than made up to volume with incremental additions. Moisture, and accumulated electrolysis products, tend to increase the conductivity which results in increased fields across the oxide under test. Voltage adjustments which could be used to offset these effects cannot be accurately selected on the basis of percent information.

5. The spacing of 300μ was selected to bring the wafer surface into focus at 50X when covered by methanol to the total cup depth. The spacing is somewhat arbitrary with respect to actual current flow and total defect count, effects which are governed mainly by defect diameter and fluid transport to the cathodic silicon surface. Recent evidence indicates the spacing may vary by as much as -30 and +300 percent without seriously affecting the analysis.

6. Identified by gas chromatography.

7. Exercise extreme care in preventing contact of acids or acid fumes with the microscope. Conduct all acid treatments a safe distance from the microscope, preferably in a hood.

APPENDIX B. STRESS IN SiO_2 LAYERS

B-1. EVIDENCE OF MECHANICAL STRESS AS A CAUSE OF DIELECTRIC DEFECTS IN SILICON DIOXIDE LAYERS

The presence of compressive stress in room temperature specimens of silicon dioxide grown on silicon at elevated temperatures has been previously recognized (Ref B-1). The effect of this stress has been considered insufficient to affect the band gap and, therefore, the performance of planar silicon devices passivated by such oxide layers (Ref B-2), and correlations with other effects, such as the presence of interface surface states, have been regarded as purely conjectural (Ref B-3). More recently the existence of residual mechanical stress in oxide layers grown on silicon has been confirmed (Ref B-4), and evidence has been advanced implicating this stress in the formation of structural defects in the oxide that are susceptible to dielectric breakdown under the influence of a potential gradient (Ref B-4, 5). Such defects have the practical effect of severely limiting the fabrication of large area planar arrays on a single silicon chip. Until now no single definitive experiment associating oxide dielectric defects with mechanical stress has been performed.

Compressive stress in grown silicon dioxide layers originates in the fact that the coefficient of linear thermal expansion of silicon is a factor of $\sim$10 higher than that of vitreous silica, and in the fact that oxide layers are grown at temperatures $\geq$1000 C followed by cooling to room temperature. Therefore, an etching test for defects on freshly grown oxide prior to cooling, followed by a decoration test (Ref B-4) of defects present after cooling, should yield a direct indication whether a correlation exists between dielectric defect incidence and thermal contraction-induced mechanical stress.

Eight mechanically polished silicon wafers with (111) surfaces were oxidized in a conventional processing furnace in a 1:1 O_2/N_2 atmosphere. Water vapor was carried by the O_2 stream from a reservoir maintained at 100 C. The treatment was continued for 1.5 hours at a temperature of 1150°C producing 8000Å vitreous oxide layers as determined subsequently be conventional optical interference technique. Water injection then was discontinued and HCl gas introduced into the N_2 line at a flow rate sufficient to provide a 0.1 mole ratio in the process gas. However, residual water in the system was present during this treatment. Vapor phase etching in this ambient was continued for ten minutes followed by a forty-minute flush with N_2 alone. Wafer temperature was held constant within $\pm$0.5 C during the entire sequence, after which the oxide-coated wafers were cooled to room temperature in an inert ambient. Dielectric defects in the oxide layers of each wafer were revealed by a previously developed (Ref B-4) electrophoretic decoration procedure. The defect locations appear as roughly circular deposits as shown in Figure B-1. After photographing and counting the defects on each wafer, the decorations were removed with an acid rinse and the vitreous silica layers with hydrofluoric acid. The thoroughly cleansed wafers were then examined microscopically for etch-pits that may have formed in the silicon during the HCl treatment.

The results of electrophoretic oxide defect decorations are given in Table B-1. However, in all of the wafers only one etch-pit in the silicon was found by microscopy after removal of the oxide layers. A photomicrograph (Nomarsky phase contrast) of the etch-pit is shown in the center area of Figure B-2. This etch-pit corresponds to

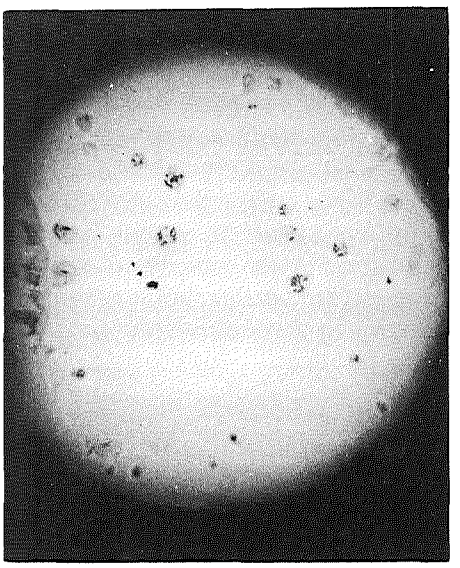

Figure B-1. Oxide Defect Decorations on Silicon Wafer Specimen No. 4 of Table H-1 (outer diameter 2.3 cm)

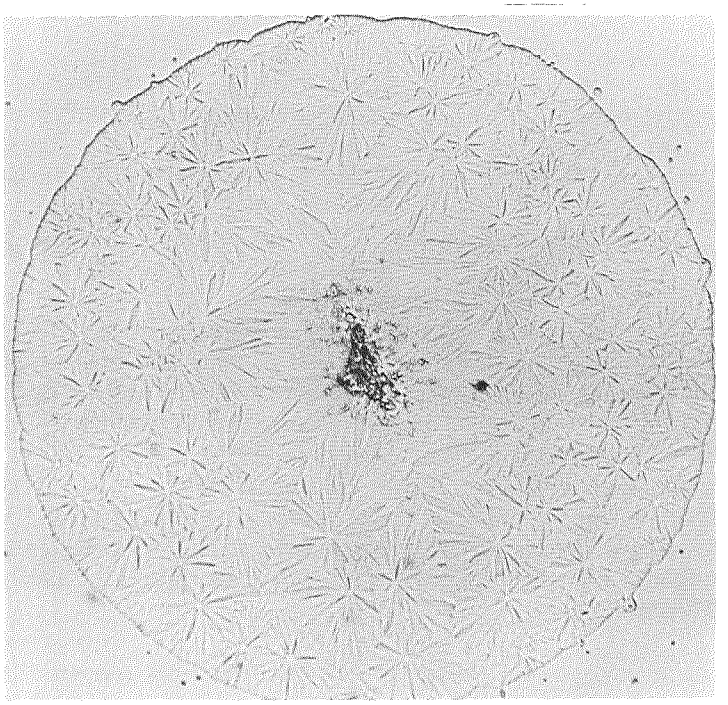

Figure B-2. Etch Pit in Silicon (center) and Surrounding Structure (outer diameter 600 microns)

TABLE B-1
OXIDE DIELECTRIC DEFECTS LOCATED BY ELECTROPHORETIC DECORATION*

Wafer Specimen	Total Defects
1	33
2	27
3	15
4	24
5	28
6	18
7	13
8	27
Total	195

*Procedure given in Reference B-4.

one of the total of 195 decorated spots and may have originated from one or more lapping grits originally embedded in the wafer. At present, the crow-foot structure surrounding this pit is an unexplained experimental artifact. However, this pattern has been observed previously (Ref B-6) in studies of HCl etching at 1150 C through oxide "pinholes" deliberately introduced by photolithographic procedure. In these previous studies a five-minute rather than a ten-minute treatment with HCl was used. The structure appears to adopt a three-fold symmetry pattern induced by the (111) surface orientation and may be a region of redeposited (epitaxial) silicon. No evidence of the more characteristic triangular etch-pits was found.

It is clear from the foregoing results that there is a better than 99 percent correlation between the formation of silicon dioxide structural defects and the process of wafer cooling from >1000 C to room temperature. The only obvious origin of this effect is the thermal contraction mismatch between the respective layers. A substantial amount of less direct evidence exists (Ref B-4, B-5) in support of this conclusion.

Thanks are due Dr. P.J. Besser and T.E. Hagey for experimental support, and to NASA-ERC for funded support under Contract NAS 12-4.

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B-4. P.J. Besser, J.E. Meinhard and P.H. Eisenberg, Electrochemical Society Meeting, Philadelphia, Pennsylvania, October 10-14, 1966. (To be published).

B-5. Manufacturing In-Process Control and Measuring Techniques for Integral Electronics, No. 4, IR-8-140 (IV), Motorola, Inc., January, 1965, p. 97.

B-2. MEASUREMENT OF COMPRESSIVE STRESS IN OXIDE LAYERS

The compressive stresses associated with oxide layers of various thicknesses and defect densities are listed in Table B-2. Determinations were made by Proficorder tracing arranged to give both the step thickness of an etch mark and the delta curvature, or deflection, over a given trace distance produced by removal of an oxide layer. From the deflection data the compressive stress is computed using the following relation:

$$\theta_o = 4E_s \, Z_s^2 \, d_s / 3Z_o \, 1^2 \qquad \text{(B-1)}$$

where E_s is the modulus of elasticity of silicon (27.3×10^6 psi), Z_s and Z_o are the thicknesses (inches) of the silicon and oxide layers respectively, d_s is the deflection

TABLE B-2
CORRELATION OF DEFECT DENSITIES WITH OXIDATION AND STRESS

Run	Oxidation		Defects vs Stress (No./Wafer)			Measured Stress[d] (Psi x 10^{-3})
	Time, $t^{1/2}$ (Min)	Thickness (Angstroms)	No Stress[a]	Full Stress[b]	Partial Stress[c]	
A	2.24	1720	131	545	987	40.3
B	3.16	1995	35	511	644	49.5
C	3.87	2590	10	343	479	36.8
D	4.47	3125	5	111	146	40.0
E	5.00	2945	8	170	353	42.1
J	5.00	3760	0.5	205	333	37.3
F	6.32	4010	1	31	140	41.4
G	7.81	5325	0	24	90	42.6
					Av:	41.3 ±6.4%

a. Silicon etch pit count produced before cooling.
b. Decoration count after cooling.
c. Decoration count after removal of back oxide layer.
d. By Proficorder trace method described in text.

produced by oxide removal and 1 is the length of Proficorder traverse, yielding the compressive stress, θ_o, in psi. Mutually perpendicular Proficorder traces were made on each wafer.

Error in these measurements arose from two sources: step thickness determinations (±250 Å) and curvature irregularities in about 50 percent of the Proficorder traces. The thickness error is apparent from Table F-1 where the calculated stresses deviate from the average most for the thinner oxides (i.e., where the measurement error is proportionately greater). There is, however, no apparent change in stress with oxide thickness, as was deduced earlier from more limited evidence. Curvature irregularities were dealt with by area summation technique applied to the regions enclosed by the pre- and post-oxide removal curve traces. This resulted in an improvement of about 50 percent (to 6.4 percent) over earlier computations.

The magnitude of the compressive stress in the oxide (4×10^4 psi) is considered substantial enough to rupture a large proportion of existing thin spots in the oxide in cooling from the oxidation temperature. Other thin spots, although fractured, may be held together by the residual compressive stress and escape detection by electrophoretic decoration. These spots appear in turn to be opened up (i.e., they become detectable by decoration) by the convex curvature and relief of stress introduced by back oxide removal. The convex curvature is, of course, readily apparent from the Proficorder traces.

APPENDIX C. EFFECT OF HYDROGEN ON INTEGRATED CIRCUIT PERFORMANCE

Present process control of packaging techniques is inadequate in several respects and fosters a variety of modes of failure. These include variations in gas ambient compositions, nonhermeticity, corrosion of leads, inferior heat sinks and cracked dice. These problems often are interdependent and augment each other or additional failure modes. Nonhermeticity may contribute to variations in package ambients and corrosion of leads; inferior heat sinks may contribute to cracked dice, degradation of h_{FE} and metallization mass transport, all of which are current reliability problems. Associated with the problem of nonhermetic package is the lack of an adequate gross leak test. The objective of this investigation is to locate the sources of these problems in process control techniques and to seek remedies therefor.

Previous program activities in this area have been limited mainly to the analysis of package ambients and the investigation of the effects of certain of these gases on transistor function. Using mass spectrometric and gas chromatographic techniques a large variety of gaseous species were detected in the packages of transistors and integrated circuits. It was shown that the presence of moisture seriously affected the low temperature performance of mesa transistors but not of planar transistors. It also was shown that baking for limited periods in a hydrogen ambient produced irreversible increases in the betas of some groups of transistors but not in others. General conclusions could not be reached because of the limited sampling and the insufficiency of available process histories.

Improved facilities were established for similar investigations on integrated circuits providing considerable flexibility in the selection of test ambient compositions, temperatures and pressures. Investigations also were extended to the major problems indicated above. The general approach to these problems consisted of examining current practice for clues to the process origins of component defects followed by chemical and instrumental failure analysis by established procedures.

Environmental testing on a first group of integrated circuits was inconclusive as a result of poor versatility of the external circuitry. A second group of 15 type 947 GPA integrated circuits were selected and prepared for environmental testing using an improved electrical connection network which permitted both beta and voltage breakdown measurements on the output section without the need to rebond any components inside the package. However, four separate connections were needed for each device which limited the number inside the vacuum chamber to seven plus two control devices.

The devices were placed on a special pyrex platen grooved to accept each device lead in a separate 0.010 inch deep by 0.025 inch wide slot (Figure C-1). Gold-plated Kovar 0.003 by 0.010 inch ribbon lead wires connecting the devices to the bakeable high vacuum feed-through connector inside the chamber were attached to the devices by thermal compression welding. Exact positioning of each device and lead wire on the platen was maintained by pyrex cover plates mechanically clamped to the base platen. Location and clamping is such that stress loads are not applied to

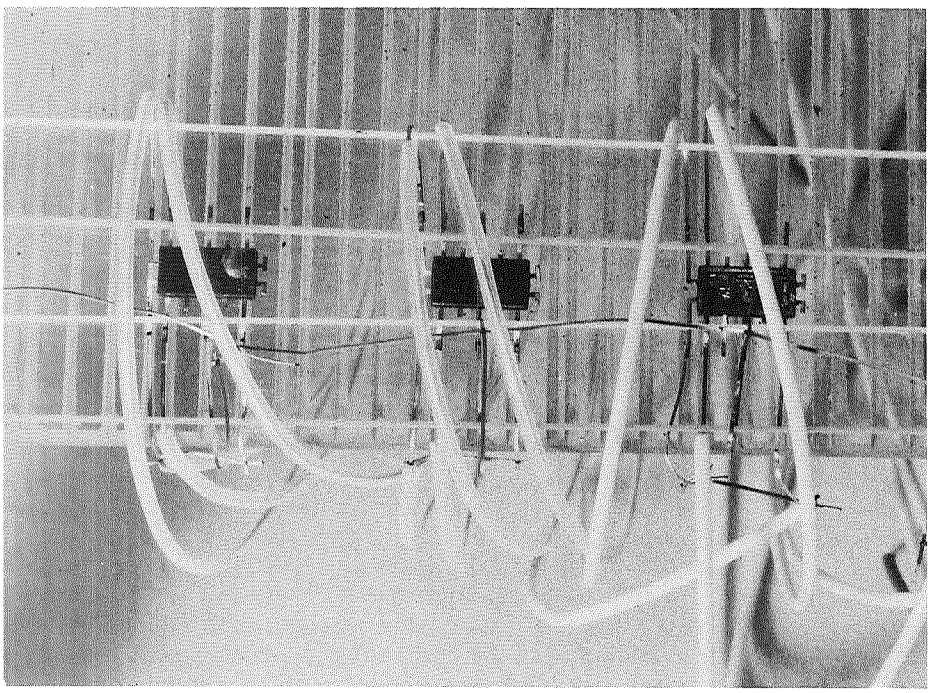


Figure C-1. – Integrated Circuitry Mounted on Paper Platen

either the device or lead. Insulation of leads between the vacuum feed-through connector and platen was teflon sleeving which had been punctured along each length to reduce virtual gas loads. This new mounting configuration eliminated the use of any bonding adhesives to attach either the devices or connecting leads.

It was found necessary to develop special methods of delidding and lead bonding to eliminate mechanical failures due to handling. These problems were solved by constructing a special furnace for freeing the lids from the packages and by adapting a split tip welder of Autonetics design to the bonding process. Electrical tests on a group of five IC's performed before and after the applications of both techniques revealed no change in BV_{ceo}, BV_{cer} and beta, thereby establishing nondestructiveness of the procedures.

The initial test sequence adopted for nine Norden IC's was designed to approach ambient survival limits cautiously. It was found that moderate heating in vacuum (100 C and 150 C) produced no significant change in the room temperature characteristics although large changes were noted at the elevated temperatures. The reversible nature of the high temperature effects indicate generally good device stability.

In a second test sequence, the nine IC's (two of which remained lidded) were thermally cycled from room temperature to 150 C in vacuum and in "forming gas" (15 percent H_2 and 85 percent N_2). Only two of the devices (both delidded) survived this treatment, both of which returned to their original room temperature characteristics. The performance (average beta) of the two devices is plotted in Figure C-2 as a function of ambient treatment and indicates that an ambient of 15 percent hydrogen at 150 C produces no irreversible change, even under a constant electrical load of potentially destructive magnitude. This result once again suggests that the effects of hydrogen on the characteristics of most planar devices is largely insignificant. Figure C-2 also indicates that high temperature performance in the presence of hydrogen is scarcely different from that in vacuum.

Optical examination of the seven failed devices revealed that failure invariably occurred at the transistor emitter-to-pad metallization (Figure C-3). The failure mode was an open circuit produced by fusion and parting of the metallization, followed by contraction of the molten metal by surface tension into a module adjacent to the pad bond. The evidence indicates excessive heat generation in the vicinity of the emitter-base region combined with inadequate dissipation. It also appears possible that the failures may have been initiated by prior mass transport of metallization because the devices had endured previous periods of treatment at 150 C under the same current load without evidence of change. The two lidded devices not exposed to hydrogen suffered the same failures.

The two unlidded devices that survived the above thermal treatments were remounted on the Pyrex platen as shown in Figure C-4 and reinserted in the environmental test chamber shown in Figures C-5 and C-6. In this figure the right-hand

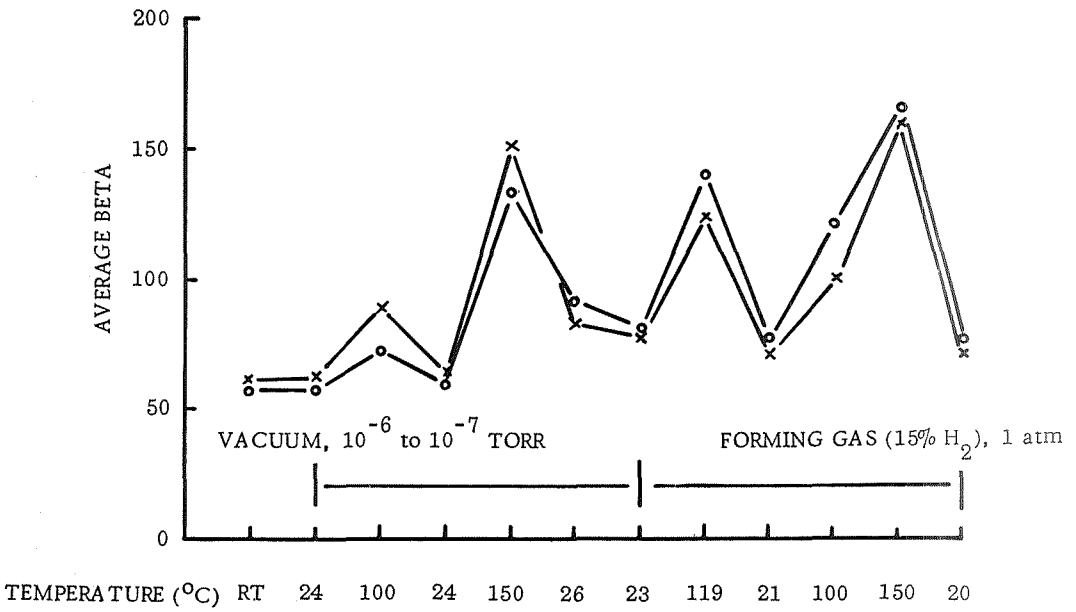


Figure C-2. – Behavior of Two Surviving Units in 15-Percent Hydrogen Ambient

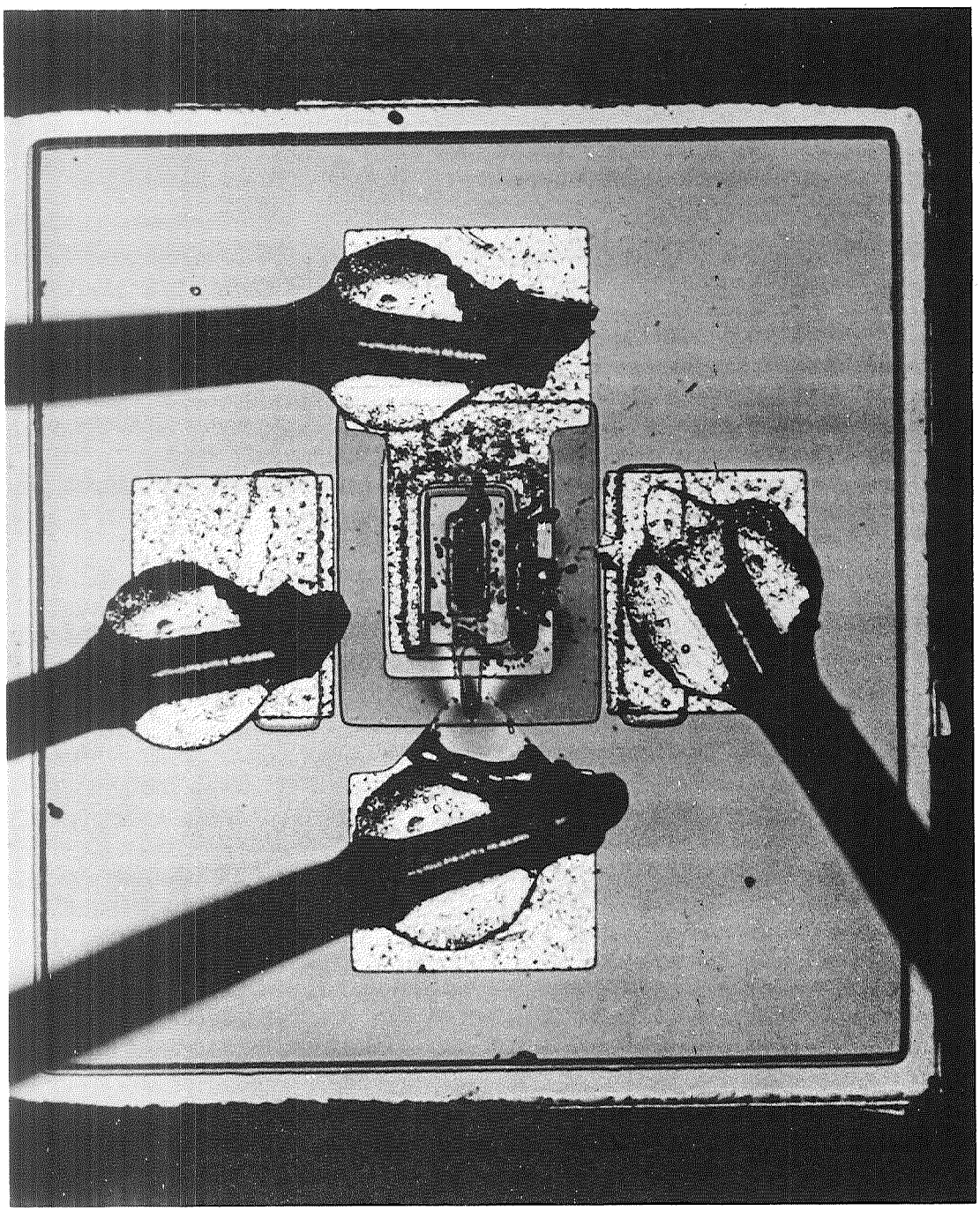


Figure C-3. – High Temperature Failure of Emitter-to-Pad Metallization

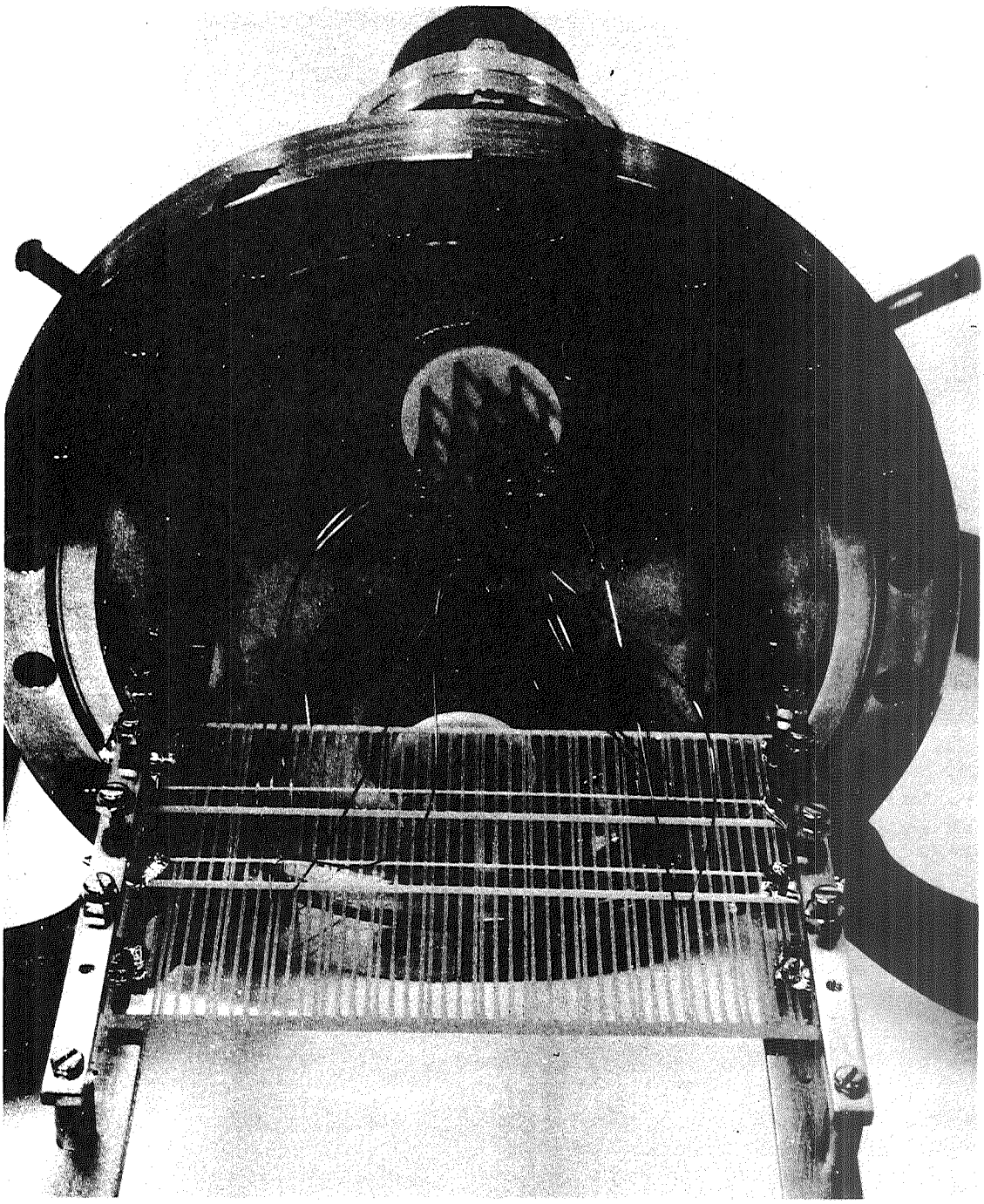


Figure C-4. – IC's Mounted on Platen

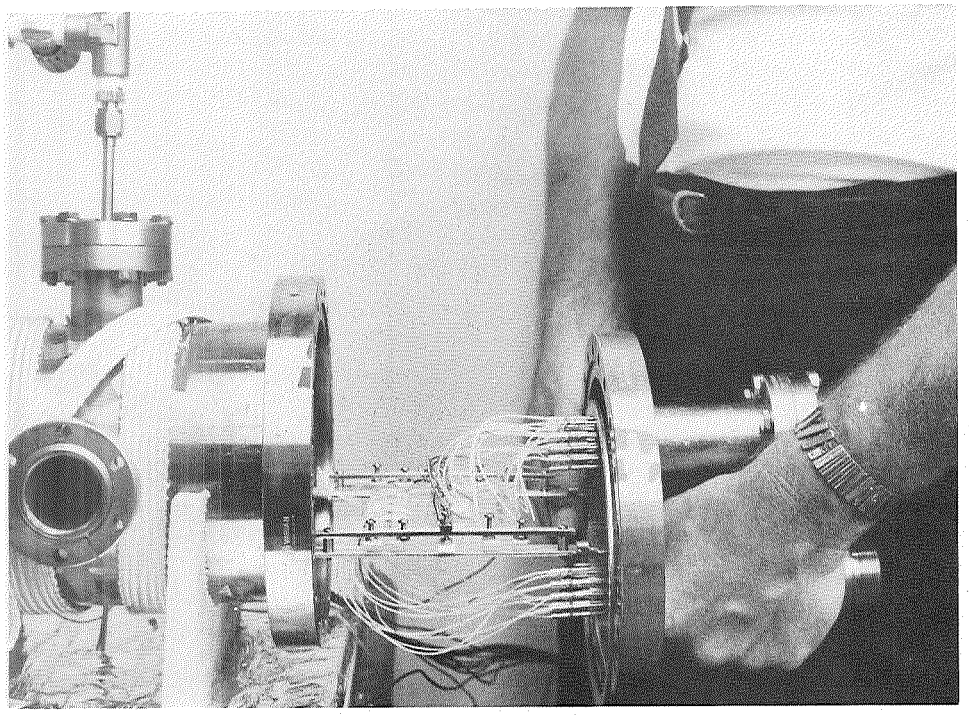


Figure C-5. – Insertion of Test Specimens Into Environmental Chamber

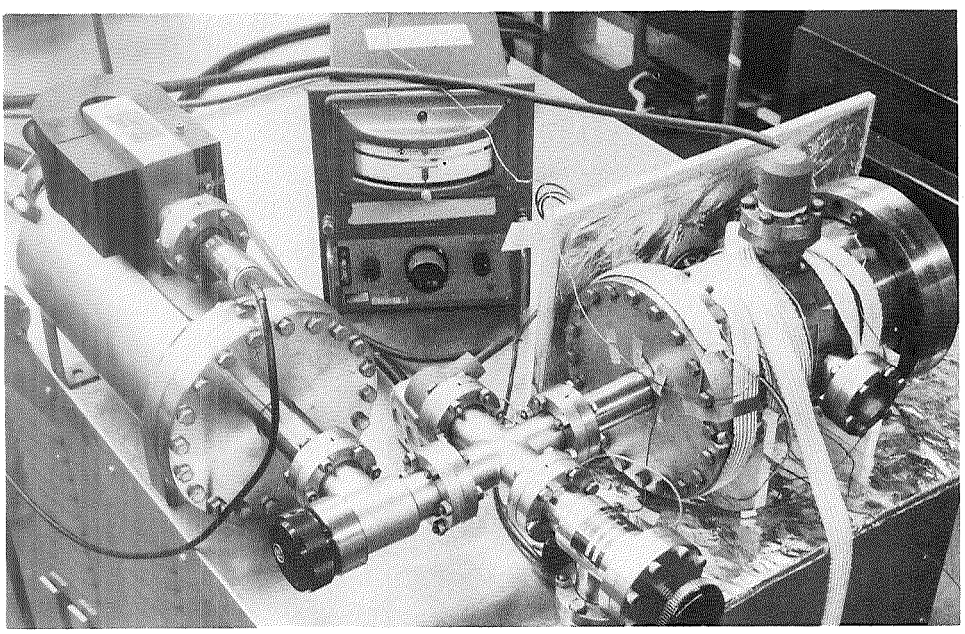


Figure C-6. – Environmental Test Assembly

cylindrical structure, mounted with thermocouples and heating tapes, is the assembled test chamber containing the devices and the left-hand cylindrical structure is the ion pump. Roughing pump, trap and gas metering devices are not shown. Thermal treatments to 350 C under vacuum and zero bias were conducted on the two IC's with the results shown in Figure C-7. All electrical measurements were made after cooling the chamber to room temperature but under continuous vacuum. The 350 C bake in vacuum was followed by a six hour treatment with forming gas at 250 C.

The upper curves (β-8 and β-13) in Figure C-7 represent the individual betas of the respective outboard transistors while the lower curves represent the combined betas simultaneously measured. It is seen that the individual betas are much more sensitive indicators of the effects of these treatments than the combined betas. Specifically, the individual betas drop significantly above 300 C. Heating in forming gas, however, tends to revive them, suggesting that the reason for the degradation in betas is a gas desorption process under vacuum at elevated temperatures. Rebaking the devices under vacuum again produced a drop in beta showing the process to be reversible. It was found in subsequent experiments that the transistor betas could be completely revived by baking either in a pure nitrogen atmosphere or a pure hydrogen atmosphere, thus eliminating hydrogen as a unique agent in the recovery of transistor betas. It is worth pointing out that this effect of hydrogen was observed on an earlier group of transistors as indicated in the second paragraph of this section. It is possible that this former group of transistors may have been vacuum baked prior to sealing, and that baking in nitrogen might have accomplished the same effect as hydrogen.

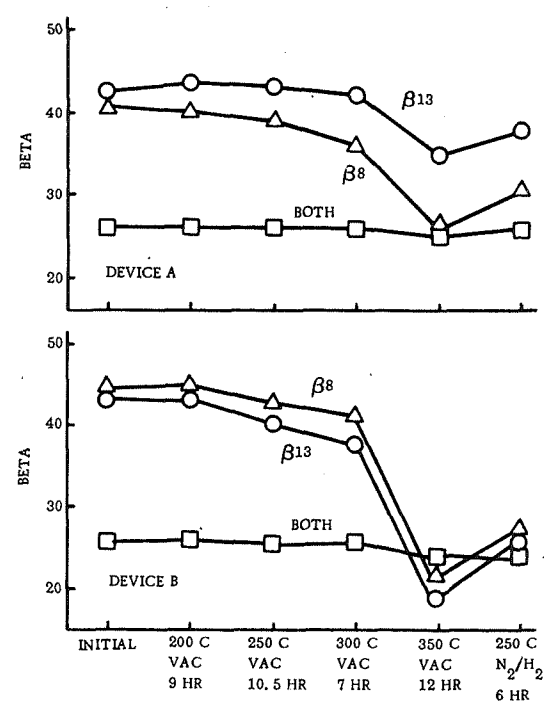
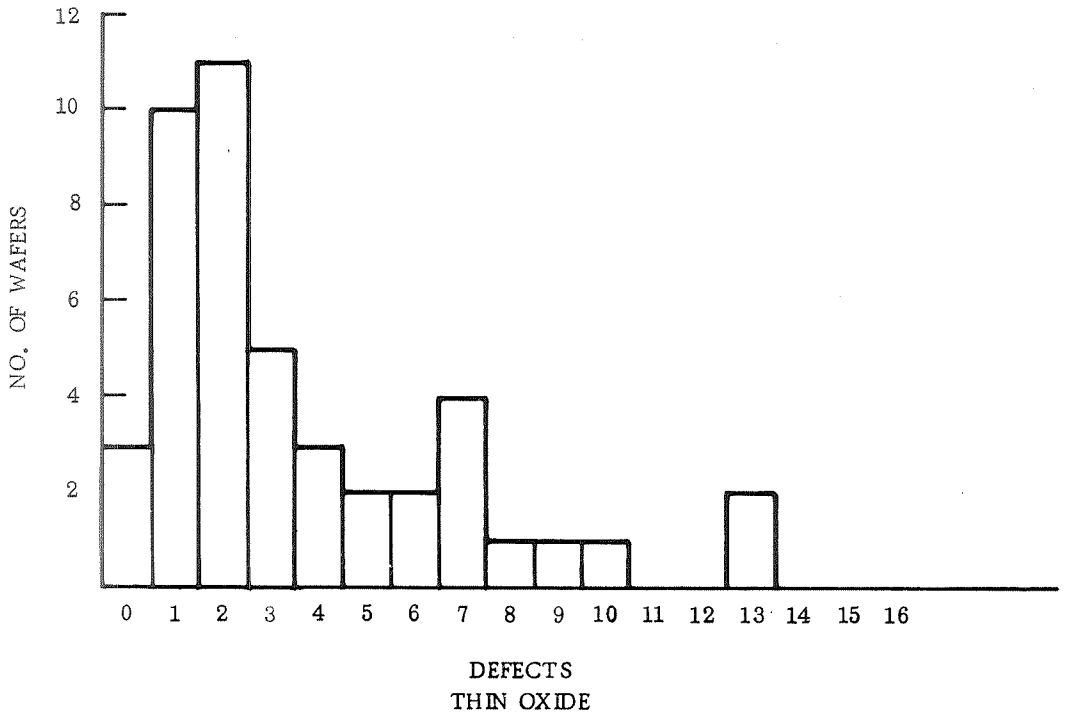


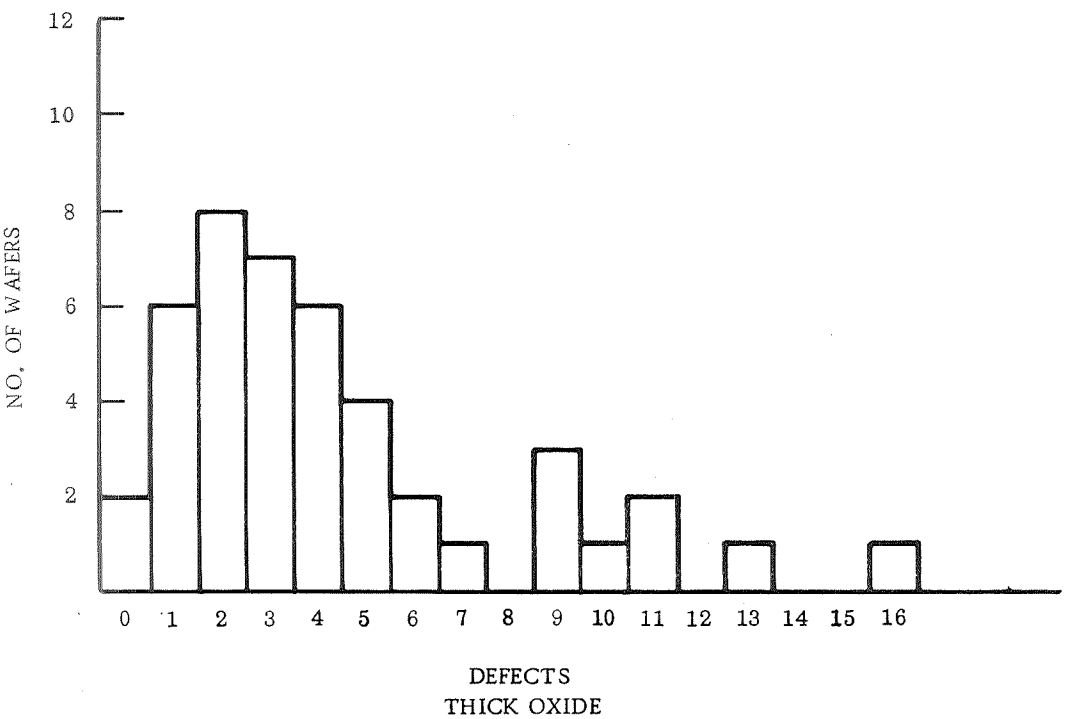
Figure C-7. – Effects of Vacuum and Forming Gas on Beta at Elevated Temperatures

A second group of five identical IC's was baked in nitrogen ambient without prior vacuum treatment. The baking was conducted at successively increasing temperature intervals with room temperature electrical testing after each bake. The final bake was at 525 C for nineteen hours. Except for one IC, which succumbed at a 375 C treatment (emitter/base short), these devices endured the entire sequence without significant degradation of room temperature electrical characteristics. Thus it was established that the thermal exposures used in earlier experiments were not excessive with respect to ambient temperature alone.

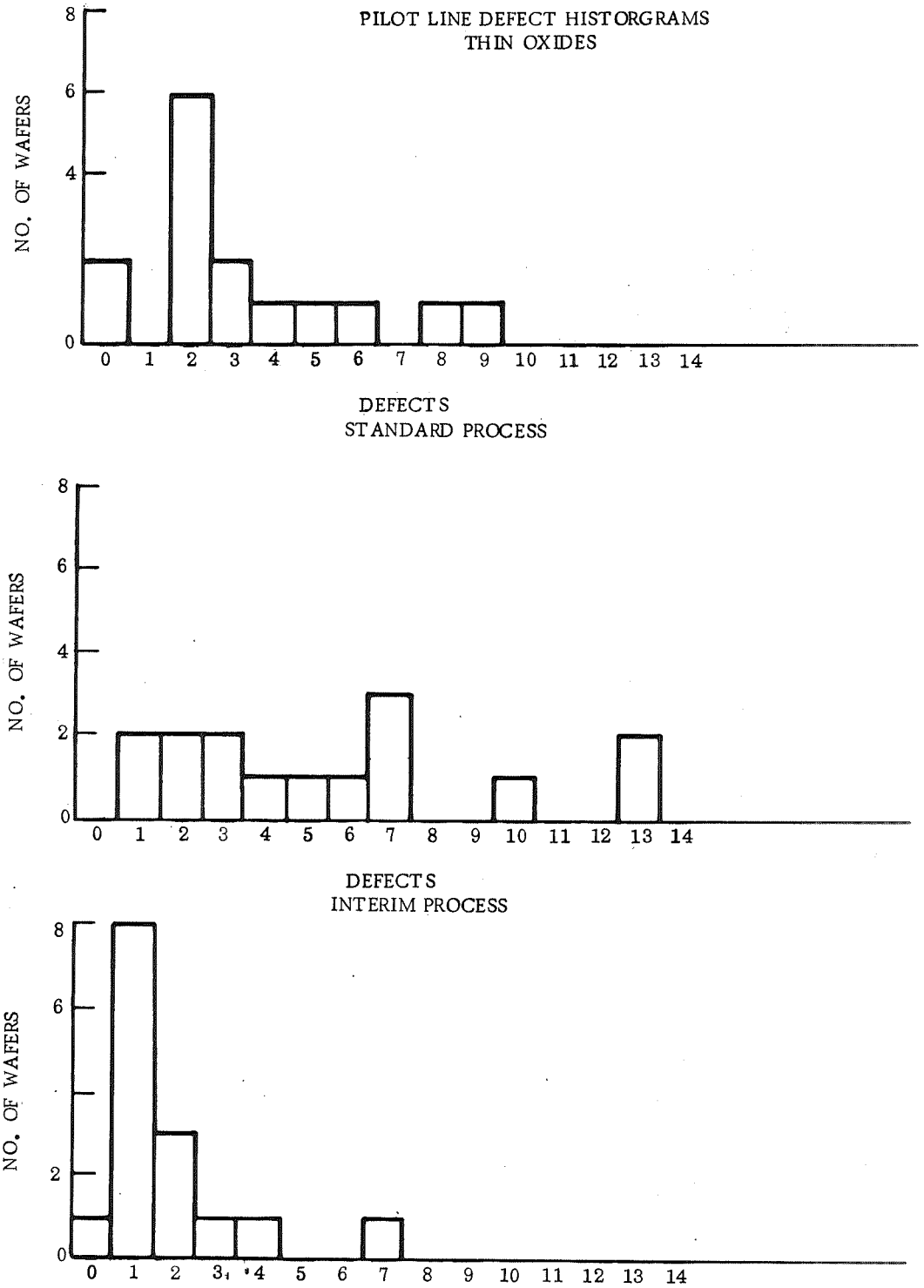
On the basis of present and earlier results it appears that the effects, if any, of hydrogen ambients on planar devices are curative rather than degradative and are not likely to occur at significant rates except at well above use temperatures. It also appears that hydrogen is not unique in this respect and that improvement in betas after vacuum baking may be effected by other "inert" gases, such as nitrogen. The precise reason for the effects of vacuum baking are not known at this time but should be further investigated in view of the deep space nature of NASA missions.

APPENDIX D
WAFER OXIDE DEFECT DATA
AUTONETICS MOS DEVICE PILOT LINE





Pilot Line Defect Historograms



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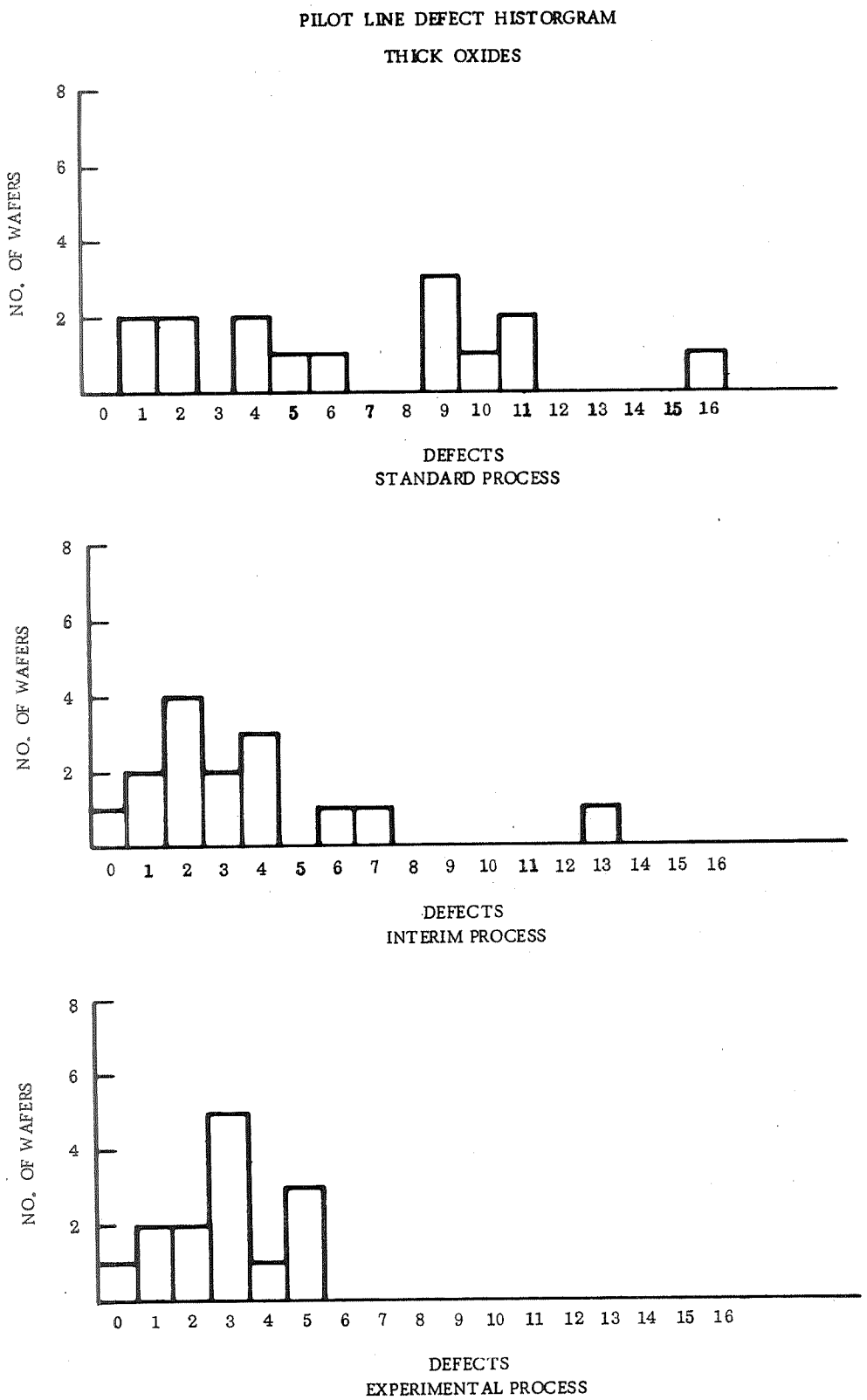

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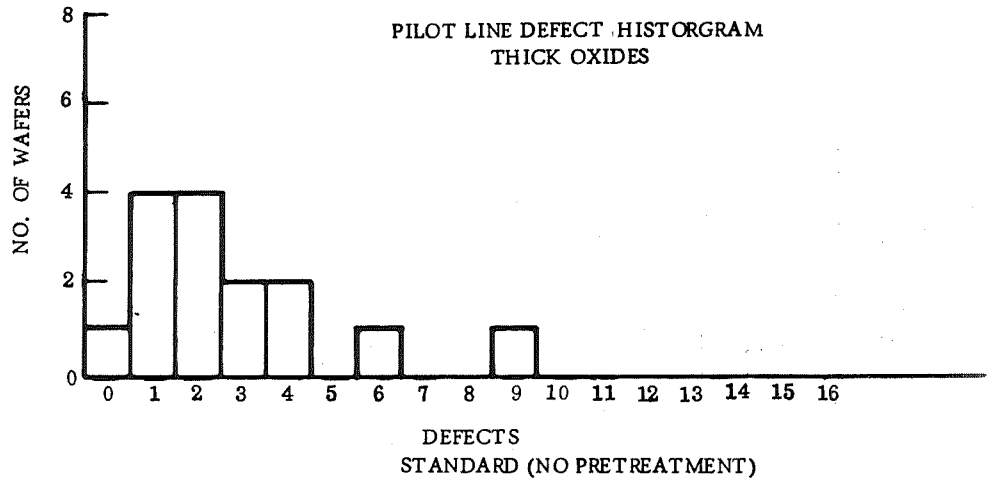

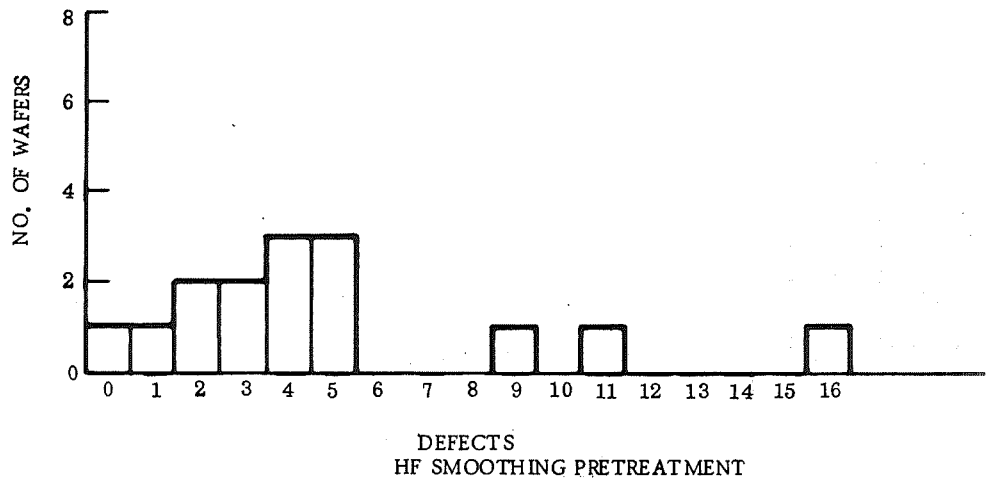

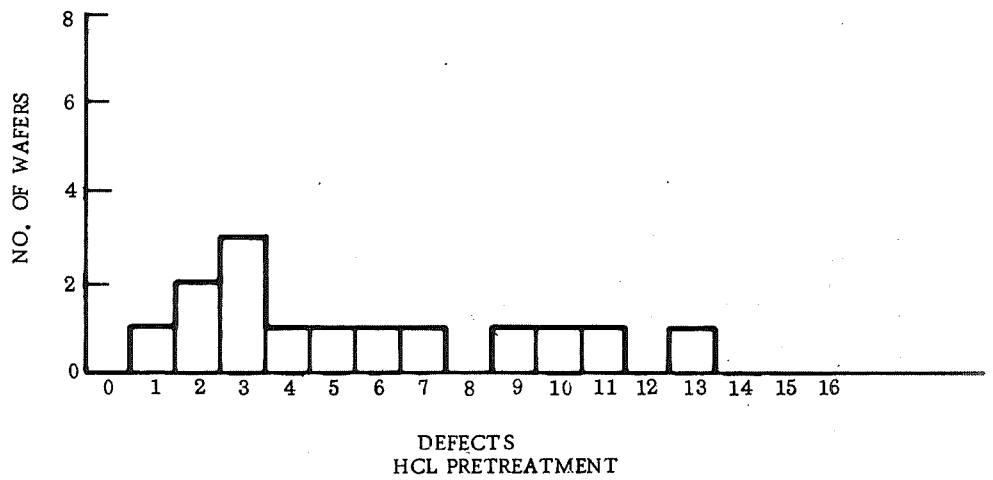

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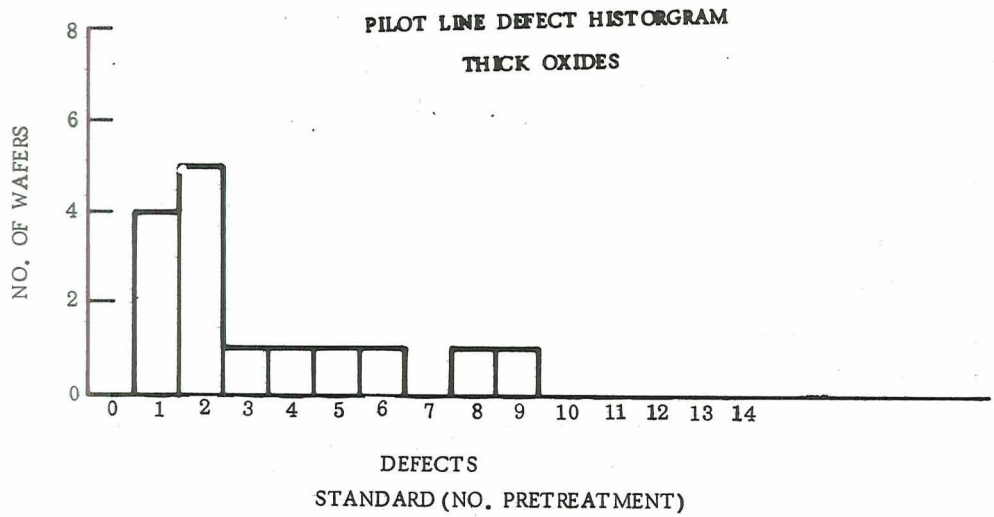

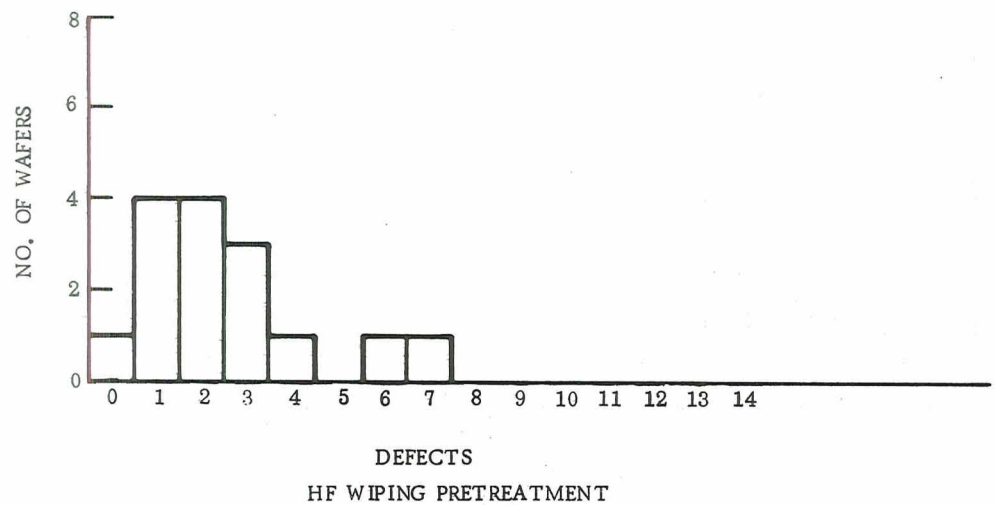

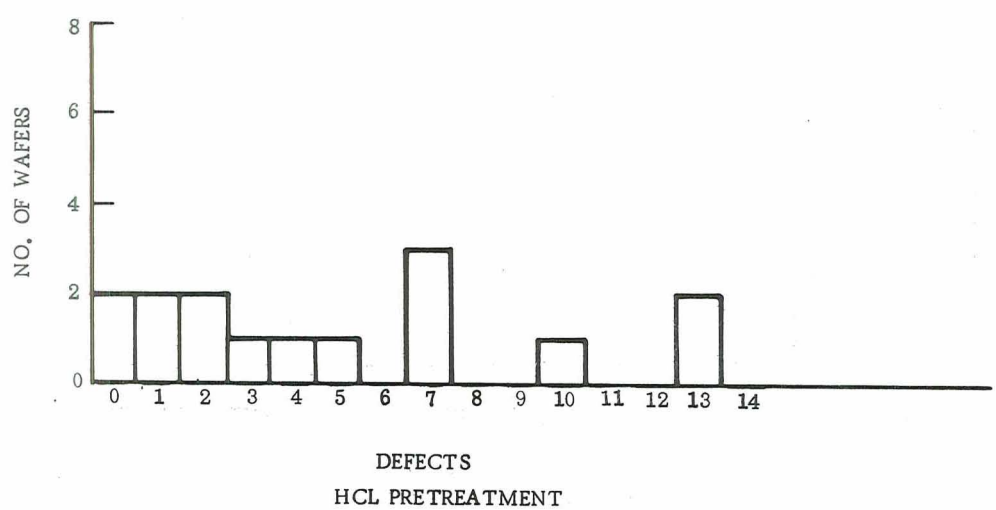

Pilot Line Defect Historograms

APPENDIX E. HYDROGEN ISOTOPE INVESTIGATION OF PASSIVATION SILICON OXIDES*

BY
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The silicon dioxide passivation layers utilized for dielectric isolation in planar silicon devices are subject to two general types of failure: dielectric anomalies which give rise to shorts between metallizations and the silicon substrate, and field induced accumulations of positive charge which produce inversion in bipolar transistors and gate threshold voltage instability in MOS-FET's. The present study attempts to shed light on the latter problem by identifying positive charge accumulation with the electromigration of specific positive ions.

Conventional thermal oxidation procedures employ a small proportion of steam in the process gas to promote favorable mechanical and dielectric properties in the resulting oxide[1]. Although these procedures are conducted at elevated temperatures (1000-1200 C), opportunity nevertheless exists for the oxide entrapment of hydrogen derived from the steam. This can be understood from the schematic representation of the process postulated in Figure E-1. Most of the initially produced --- Si-O-H groupings should interact with equivalent nearest neighbors with the elimination of water and the formation of Si-O-Si bridges. A small proportion of such groupings, however, will be isolated from reactive neighbors in the process and will remain randomly distributed in the oxide. The residual --- Si-O-H groupings may be regarded as acidic sites capable of releasing protons under the influence of an applied electric field, or of exchanging protons for other monovalent cations, such as sodium ions, analogous to the function of ion exchange zeolites. The density of residual acidic sites will then be a function of the base concentration (HOH, NaOH) present during oxidation, and they will act as reservoirs of positive ions which may contribute to the inversion phenomenon.

In order to demonstrate whether residual hydrogen was present in the oxide a tritiated oxidation run was performed on boron-doped high resistivity silicon wafers using one gram of water containing 100 ± 5 millicuries of tritium. Oxidation was conducted at 1150 C in the apparatus shown schematically in Figure E-2. Gases were metered and purified by conventional means using an N_2:O_2 flow ratio of 3:2. Tritium labeled water was picked up by the O_2 stream from a reservoir maintained at 95 C This reservoir was a single, bypass fitted U-tube of sufficient internal diameter to permit evaporation of the water without mechanical carry-over by the gas stream. The process was timed to produce approximately 2000 Å of oxide on the wafers which utilized the entire charge of water in the reservoir. The entire procedure was designed to duplicate as closely as possible conventional methods of silicon oxidation for planar devices.

[1]Delivered at the Electrochemical Society Meeting, Cleveland, Ohio, 3 May 1966.

Several techniques were used to measure the level of tritium present in the treated samples. A 2π counter was employed without any indication of H^3 activity. Similar results were obtained with a liquid scintillation counter. A 4π counter was then utilized with the results given in Table E-1. The plus-or-minus value represents one standard deviation determined from counting statistics only. In this case, this represents an 82-percent probability that H^3 was detected. An approximate hydrogen level of 10^{10} atoms/cm^2 in 2000 Å of oxide was tentatively inferred from this result.

TABLE E-1
TRITIUM ACTIVITY IN OXIDE DERIVED FROM 100 MC/GRAM WATER

	Counting Time, Minutes	Total Counts	Net Counts per Minute
Background	450	52667	
Treated Disc	913	108054	1.32 ± 0.93

In view of the somewhat inconclusive nature of these results, it was decided to examine the oxide for other impurities that might displace hydrogen from the oxide matrix and to repeat the experiment using a higher tritium activity. Sodium ions were sought, therefore, by neutron activation analysis of a five-wafer sample. An additional five-wafer sample from which the oxide had been stripped also was activated. The composite samples and a sodium standard were irradiated 1/2 hour at 250 kw in a Mark I TRIGA reactor with a thermal neutron flux of 1.8×10^{12} cm^{-2} sec^{-1}. The activated oxide was stripped off the first sample, concentrated by evaporation, and counted overnight in a NaI well detector coupled to a multichannel pulse-height analyzer. The irradiated sodium standard was counted in identical geometry. The 2.75 Mev photopeak of Na^{24} was used for analysis because of the comparative freedom from interference by other residual activities (e.g., Si^{31}) present in the samples. Other peaks attributable to Au^{198}, Cu^{64}, and Mn^{56} also were found. The etch solution concentrate (0.9799g) was found to contain 0.0196-0.004 ug Na which indicates an average concentration of approximately 8×10^{17} atoms/cm^3 in the original oxide. Sodium in the stripped wafers was found to be indistinguishable from a slight Cu^{64} background indicating a level ≤ 0.73 ppb, or 4×10^{13} atoms/cm^3, Na in the original silicon. It was presumed from these results that the sodium in the oxide originally had boiled out of the quartz tube during the oxidation or had been introduced by the gas stream.

The tritium labeled oxidation was repeated with the following modifications:

1. On the day prior to the run, the quartz reaction chamber was purged 8 hours at 1200 C with an O_2/N_2 mixture containing HCl in an attempt to extract out available sodium (as NaCl) from the quartz surfaces. The quartz wafer holder also was included in this treatment.

2. Specific activity of tritiated water was increased to 1 curie/gram. Total quantity remained 1 gram.

3. After initial purging prior to the oxidation, the O_2/N_2 carrier gas flow was reduced to a negligible value (about 5 ml/min), while the tritiated water was distilled into the reaction chamber. When transfer of the water was complete (about 40 min), gas flow was shut off producing an open-ended static system. The intention here was to extend the catalytic effect of the water for a longer period while maintaining the selected ratio of oxygen to nitrogen. The volume of the system was such that the uptake of oxygen by the silicon would have a negligible effect on this ratio.

4. Treatment was prolonged (to 2.5 hours) in order to produce thicker oxide (9000-10,000Å) and a more significant sample activity.

Oxide thickness on the treated wafers was estimated visually to be uniformly about 9000 Å and confirmed interferometrically at 9140 Å. Net area of wafer surfaces was 3.38 cm^2 per side, giving an oxide volume (2 sides) of 6.19×10^{-4} cm^3/slice.

Four wafers (of a total of 24 treated) were counted using 4-π geometry with an estimated counting efficiency of 50 percent. The loss of 50-percent efficiency was due to the combined absorption of the 9000 Å oxide layer on both sides and the 10,000 Å sample support film on one side of the sample. Calibration for tritium was derived from a polymethylmethacrylate H^3 standard from New England Nuclear Corporation. The net H^3 count rates of the four samples had a standard deviation of about 1 percent of the value in each case. The atomic ratio of H^1:H^3 in the tritiated water employed was 3390:1. Total hydrogen content in the silicon oxide of each wafer, computed from the observed count rates and the data given above is presented in Table E-2.

TABLE E-2.
TRITIUM ACTIVITY IN OXIDE DERIVED FROM 1 CURIE/GRAM WATER

Sample	Net CPM, Total	DPM H^3 per cm^2	H^3 Atoms per cm^2	Total H Atoms per cm^2	Total H Atoms per cm^3
1	360.5	103	9.8×10^8	3.4×10^{12}	3.7×10^{16}
2	345.4	101	9.5×10^8	3.3×10^{12}	3.6×10^{16}
3	225.2	67	6.2×10^8	2.1×10^{12}	2.3×10^{16}
4	199.1	59	5.5×10^8	1.9×10^{12}	2.1×10^{16}
Average				$2.7 \pm 0.7 \times 10^{12}$	$2.9 \pm 0.7 \times 10^{16}$

The spread in these results is somewhat higher than expected and difficult to explain inasmuch as differences in oxide geometry (i.e., wafer area and oxide thickness) were relatively insignificant. However, this variation could not be attributed to differences in surface absorption of tritium labeled water because the oxidation run was terminated by a tracer-free nitrogen purge in excess of 1 hour at the oxidation temperature. Entrapment of hydrogen during formation of the oxide at 1150 C was thereby established.

The last three specimens given in Table E-2 were re-assayed for beta activity in the 4- π counter after 550 hours exposure to a laboratory environment ranging from 20- to 40-percent relative humidity.

The average hydrogen concentration in the oxide layers was found to be relatively unchanged, as shown in Table E-3, indicating negligible exchange of the tritium with ambient moisture.

TABLE E-3.
TRITIUM EXCHANGE WITH HUMID ENVIRONMENT

Period	Sample	Net CPM, Total	Total H Atoms per cm^3	Average
Initial	2	345.4	3.6×10^{16}	2.7×10^{16}
	3	225.2	2.3×10^{16}	
	4	199.1	2.1×10^{16}	
After 550 hours humid exposure	2	354.6	3.7×10^{16}	2.7×10^{16}
	3	270.1	2.8×10^{16}	
	4	142.7	1.5×10^{16}	

Assay for sodium in the oxide layers of these wafers was then carried out by the neutron activation method previously described. The average sodium population was found to be 1.1×10^{18} atoms/cm^3. This result is not substantially different from that observed in the first tritiated oxidation sample, and the HC1 pretreatment was deemed ineffective.

Beta assay on the remaining 20 wafers was performed 5 months after their initial treatment. Results are compared with earlier assays in Table E-4.

TABLE E-4.
STABILITY OF TRITIUM LABELED PASSIVATION OXIDE

Elapsed Time (Days)	Number of Samples	Average Net Beta Count/Wafer C/M	Calculated H Content (x 10^{16} Atoms/cc)
0	3	257 ± 59	2.7 ± 0.6
23	3	253 ± 74	2.7 ± 0.8
150	20	186.7 ± 58.8	1.96 ± 0.60*

* Corrected for radioactive H^3 decay

Loss of activity due to H^3 exchange with the environment cannot be inferred from the last entry because of the spread in results (about 33 percent). Nevertheless, a wrapper (paper) from one of the specimens was analyzed in the 4- π counter. No evidence of H^3 exchange was detected.

Tritium activity distribution likewise was examined for internal consistency by inverting the first three wafers (of the group of 20) on the aluminized mylar support film and recounting. Deviation of beta activity between opposite sides was found to be relatively insignificant compared to deviation between wafers, as shown in Table E-5.

TABLE E-5.
BETA ACTIVITY VERSUS COUNTING ORIENTATION

Sample Number	Side Supported	Activity (C/M)	Average	Deviation, Percent
1	A	88	94	6
	B	100		
2	A	279	284	1.4
	B	288		
3	A	120	118	3.3
	B	114		

It was concluded from these results that significant amounts of hydrogen are retained in the oxide matrix if steam is present in the oxidation process gas, and that it does not exchange readily at room temperature with covalently bonded ambient hydrogen.

In order to investigate whether hydrogen trapped in passivation oxide was capable of contributing to inversion, fabrication of thirty small geometry pnp planar silicon transistors was requested from an established manufacturer* prepared under identical conditions except that the initial oxide on half the specimens was grown in the presence of 99-percent D_2O. These devices were subjected to inversion stress (temperature and collector-base reverse bias) and the kinetics of inversion recovery (baking at timed intervals under zero bias) determined. Thermal activation energies of recovery were calculated from the kinetic data according to a previously described method[2], and the results for hydrated and deuterated specimens compared. A greater activation energy was expected to be associated with the diffusion of the isotope of higher mass.

All 30 of the transistors were electrically good as-received. Their response to inversion stress, however, was variable. Consequently, they were subjected to initial inversion stress of 200 C at 40 V_{CB} for various lengths of time in order to classify them in terms of usefulness for recovery experiments. In order to be useful, the inverted device was required to show a leakage about 1×10^{-9} amps (with available instrumentation) and have a region where I_{CBO} was independent of voltage. This would indicate surface leakage as distinguished from bulk leakage. Of the 30 specimens, only eight were found to undergo inversions suitable for study, five of which were deuterated.

*Fairchild Semiconductors

The group of eight transistors was subjected to two complete evaluations, each of which involved from four to eight inversions and recoveries. The thermal activation energies associated with the recoveries are presented in Table E-6. Results from the first treatment indicate that the deuterated values may be higher than the hydrated values, as expected, but the spread in results does not permit definite conclusions to be drawn. The activation energy of the last listed result may, in fact, be a result of a trace of sodium for contamination rather than deuterium. Omitting this value, the remaining four deuterated samples yield an average recovery activation energy of 0.67 ± 0.06 cv.

TABLE E-6

INVERSION RECOVERY KINETICS OF HYDRATED AND DEUTERATED TRANSISTORS

Process Steam, Initial Oxidation	Thermal Activation Energy of Recovery (e.v.)		
	First Treatment	Second Treatment	Third Treatment
H_2O	0.46	0.86	
	0.54	0.50	
	0.74	0.56	
Average	0.58 ± 0.08	0.64 ± 0.15	
D_2O	0.56	0.72	
	0.68	0.40	
	0.70	0.74	
	0.74	0.45	
	1.29	0.82	0.55
Average	0.79 ± 0.19	0.60 ± 0.16	

Results from the second treatment appear to be generally more uniform between the two groups but are more erratic. Assuming that inversion is produced by an electrochemical transport of positive ions, one might also expect a contribution from electrode processes. Discharge of such ions in the form of neutral species at the cathodic surface would tend to remove them from participation in the charge transport process. If more than one type of ion is present in the rigid SiO_2 electrolyte, their ratios should change in succeeding inversion treatments, thus introducing variations in the kinetics of inversion recovery. Moreover, the deuterium, undoubtedly present as a minor component since it was employed only in the first oxidation, should discharge and escape by normal diffusion ultimately into the can atmosphere leaving residual normal hydrogen as the major participant. This type of proton transport in SiO_2 has been considered in detail previously by Collins[3]. Thus, the increasing spread in results and the apparent decrease in difference between the two isotopic groups with succeeding inversions can be explained. Additional evidence of these effects is indicated by the third inversion recovery treatment on the last deuterated specimen given in Table E-6.

It can be concluded from these experiments that hydrogen is definitely trapped in conventional steam grown silicon dioxide, that the phenomenon of inversion probably is electrochemical in nature, and that hydrogen ion migration probably is a contributing factor in inversion.

Acknowledgements

The work reported herein was performed under contract with the National Aeronautics and Space Administration, Electronic Research Center, Cambridge, Massachusetts. Thanks also are due H. Sello, C. Bittman, and B. Deal, of Fairchild Semiconductors, who kindly provided the set of deuterated and nondeuterated transistor specimens for study.

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2. J. E. Forrester, R. E. Harris, J. E. Meinhard, and R. L. Nolder, "Imperfections and Impurities in Silicon Associated with Device Surface Failure Mechanisms," presented at the Physics of Failure in Electronics 4th Annual Symposium, Chicago, Illinois, sponsored by the Illinois Institute of Technology and Wright Air Force Development Center, November 16-18, 1965.

3. F. C. Collins, J. Electrochem. Soc., 112, 786 (1965).

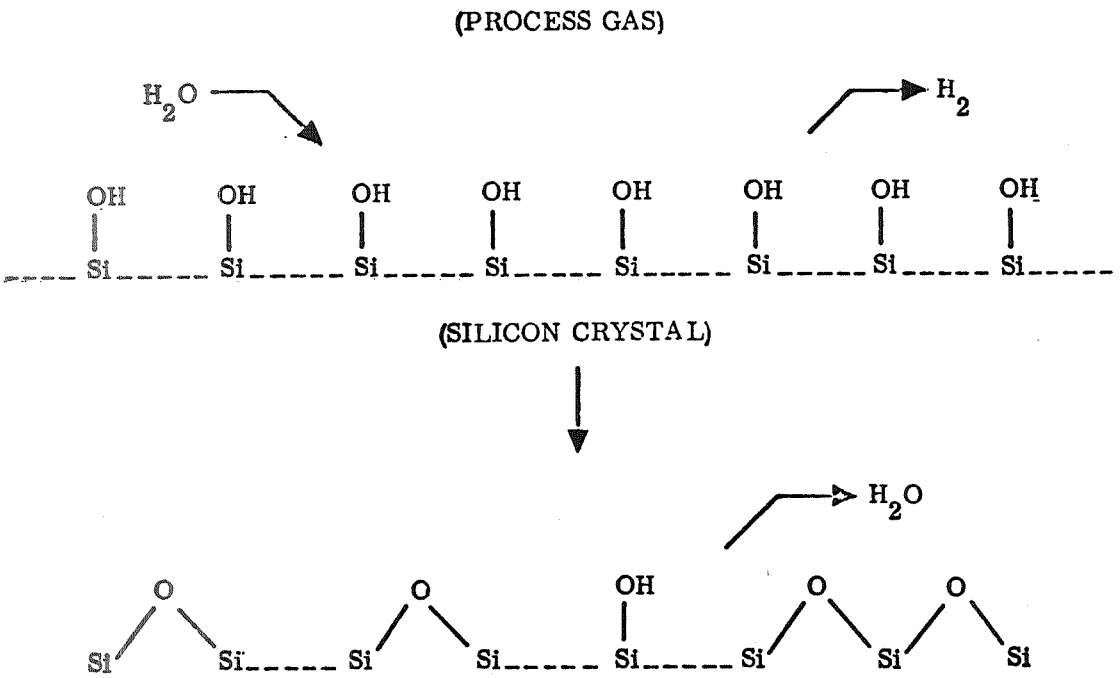

Figure E-1. - Interaction of Water With Silicon (Schematic)

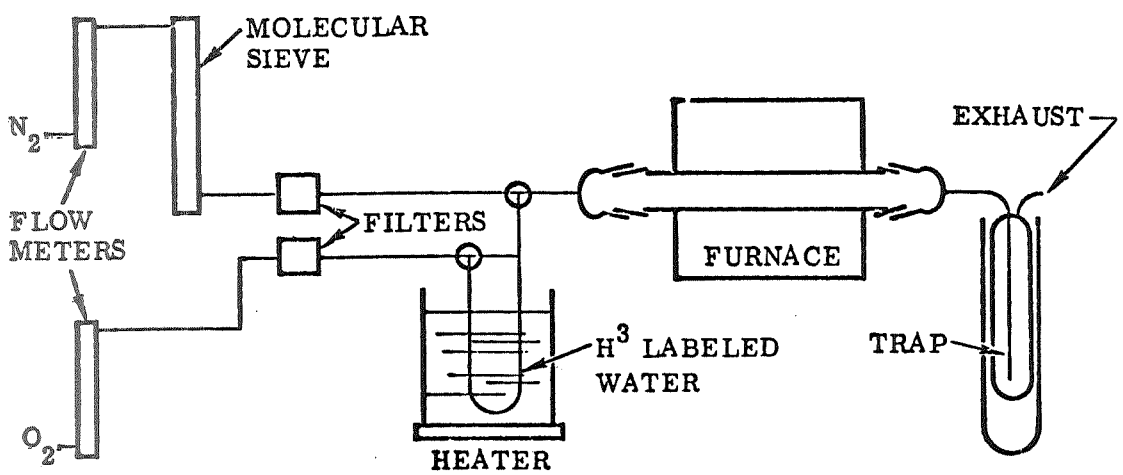

Figure E-2. -Silicon Wafer Oxidation Equipment (Schematic)

APPENDIX F. INVERSION HARDENING: NASA TECH BRIEF 67-10176

Evidence is presented in Table F-I to show that repeated inversions are capable of producing "inversion hardening" in planar transistors. This effect is potentially desirable because it reduces the possibility of long-term drift in transistor performance. Thus inversion hardening may be of some utility in deep space missions where reliable transistor function is needed over extended periods of time.

It should be recognized that these data are preliminary in nature and do not necessarily represent the maximum inversion resistence that may be possible with this technique. It also is evident from the data that considerable variability in response to the treatment exists between transistors. This variability could be used for screening purposes in selecting components for missions of long duration. Some transistors, of course, show no initial tendency to invert, which indicates good process control in their manufacture. Further investigation of inversion phenomena is required before this effect can be assigned a mechanistic model.

TABLE F-1
INVERSION HARDENING OF 2N2412 SMALL SIGNAL PNP TRANSISTORS

Unit	Initial Inversion Leakage (na)*	Number of Inversions	Total Time Under Inversion (hours)**	Final Inversion Leakage (na)*	Inversion Hardening (%)
1	108	8	96	17.4	84
2	900	8	96	375	58
3	19	6	6	50	None
4	80	2	2	34	58
5	96	2	2	27	72
6	50	8	96	25	50
7	3.5	4	4	1.65	53

*At 40 V_{cB}, 25 C
**At 40 V_{cB}, 200 C

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APPENDIX G. EPR INVESTIGATION OF THERMALLY GROWN SiO_2

Introduction

The employment of integrated circuits in electronic systems has shown that a major failure mode is excessive current across reverse biased p-n junctions. The two main conditions that cause this excessive current are silicon surface inversion and contamination of the passivation oxide surface. Silicon dioxide is almost universally used for surface passivation. The basic problem is one of oxide purity and its control during the processing of the integrated circuits. The thermal oxidation of the silicon surface has been found to induce a negative charge near the silicon surface causing it to become more n type. This is thought to occur by charge trapping in fast states related to chemical impurities or structural defects in the interface region and in slow states related to oxide impurities. Several oxide models have been postulated in the literature to explain the integrated circuit surface inversion problem. These include oxygen vacancy migration, impurity redistribution during oxidation, metallic ion migration, hydrogen or hydroxyl ion migration, oxide surface charge separation, precipitation near bulk oxygen, interface states, and a heterojunction formation. Several recent review articles describe these in detail (Ref G-1, G-2). A comprehensive bibliography was recently published (Ref G-3). The defect structure of silicon dioxide showing its complexity is shown in Figure G-1 (Ref G-4).

In this study, electron paramagnetic resonance has been used on thermally grown silicon dioxide to investigate the oxygen vacancy model. Four resonance signals have been detected from silicon dioxide samples prepared under various conditions of temperature, ambient, and chemical contamination. These data were taken at the X-band frequency of 9.3 GHz and 3400 gauss using a dual cavity operating between -180 C and +300 C. In addition to the known silicon line at $g = 2.006$, several others have been found after oxidation of both intrinsic and extrinsic silicon powder. These have been associated with sodium or fluorine retention in the oxide and hydrogen entrapment. Signals also were obtained from single crystal samples with high purity aluminum vacuum deposited over the oxide. This resonance may be due to oxygen vacancies generated by an electrode reaction between the aluminum and the oxide.

Silicon Dioxide Sample Preparation

The silicon crystals used for oxide growths in this study were obtained in wafer form from major suppliers. They were either chemically or mechanically polished prior to oxidation. A wide range of resistivity was used, which included acceptor type (boron), donor type (phosphorus), and intrinsic material. These parameters are listed in Table G-1. Single crystal samples, with various oxides grown up to 20,000 Å thickness showed no resonance absorption, so powdered samples were then used. The powdered samples provide a much larger ratio of silicon dioxide to silicon for the sample tubes used in the resonance cavity. A few oxide samples were made on float zone silicon while most were on the more common Czochralski type. From the resonance data, it was shown that the signal characteristics found depended only on the oxidation method and not on the silicon resistivity or type dopant. No signals,

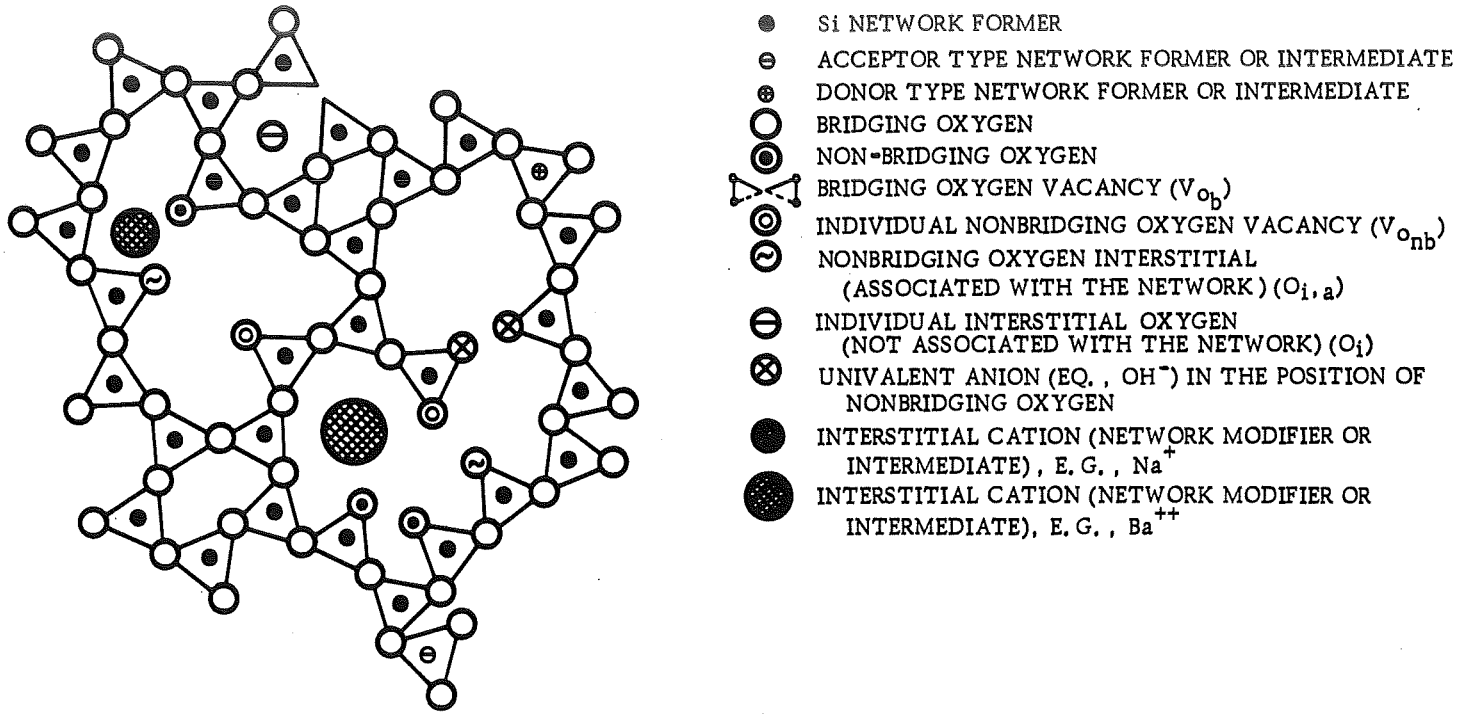


Figure G-1.- Schematic Model of Some Defects in a Two-Dimensional Model of the Silicon Dioxide Network. The Si-O Tetrahedra Are Shown as Triangles.

TABLE G-1
SILICON MATERIAL PARAMETERS OF SAMPLES USED FOR OXIDE GROWTH

Source	Original Form	Dopant	Resistivity ohm-cm
Texas Instruments	Wafer	Phosphorus	8 - 12
Monosilicon	Wafer	Boron	31 - 34
	Wafer	Boron	0.004 - 0.005
	Polycrystalline	Intrinsic	> 500
Dow Corning	Wafer	Boron	75 - 125
	Wafer	Boron	5 - 10

however, were found using the heavily doped 0.004 ohm-cm silicon material which is most likely due to the large microwave energy losses expected in a conductive material.

The oxides studied here were thermally grown by the conventional methods being used for integrated circuit manufacturing. The silicon was usually oxidized at temperatures between 1100 C to 1150 C in dry oxygen or wet oxygen. The water bath temperature was at 99 C for the steam or wet oxide growth. The silicon powder was usually etched in HF, rinsed with deionized water, and dried in a nitrogen stream. The powder was carried in a small quartz boat inside the furnace. For the wet oxide growth the silicon was usually exposed to dry oxygen and dry nitrogen for 5 minutes at 1150 C before introduction of wet oxygen for various growth periods. The oxidation time was used to control the oxide thickness. For wet oxides the period was usually extended to 6 hours because resonance signals recorded on thinner oxides had less intensity. For dry oxides the oxidation period was extended to 90 hours to achieve an equivalent thickness. These two methods gave oxides of thickness between 14,000 and 18,000 Å. For comparative data a single crystal of silicon was sometimes placed near the powder samples during oxidation. Capacitance - voltage measurements were made on these single crystal oxide samples after oxidation. Weight measurements were also made before and after oxidation on a few of the initial samples.

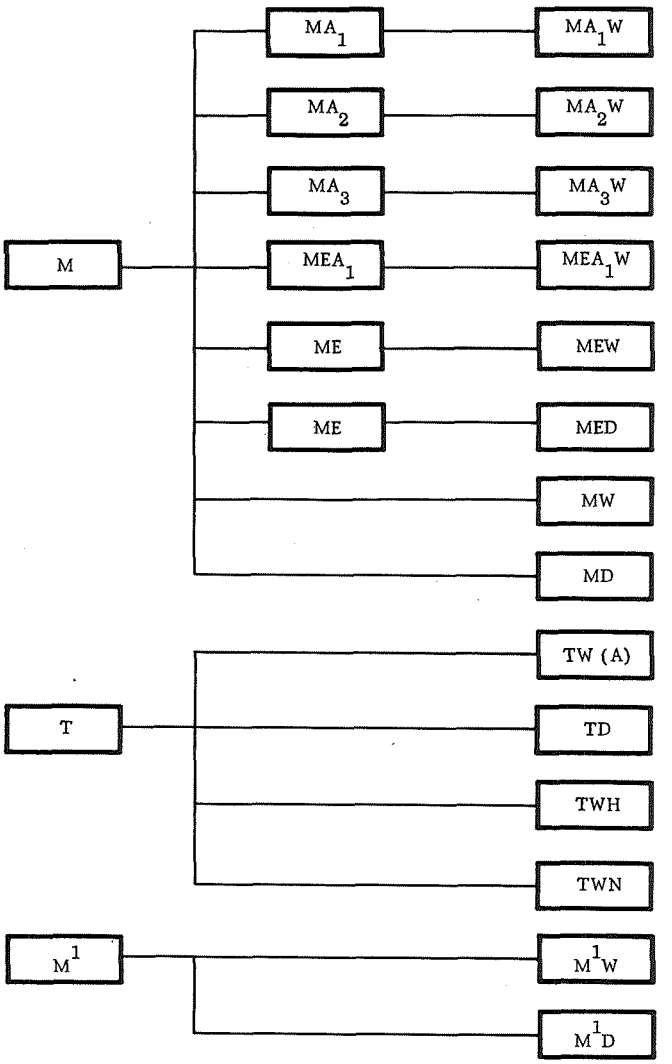
After resonance data had been taken on the silicon and silicon dioxide samples prepared in the conventional way, a number of special treatments were made on the samples to generate comparative data. These thermal and chemical treatments are listed in Table G-2. The controlled chemical contamination of the samples before and after oxidation had the greatest effect on the resonance spectra. Two other types of samples were briefly studied. One was silicon dioxide baked in hydrogen at 1150 C. The other samples had high purity aluminum vacuum deposited on single crystal oxides. The breakdown of sample treatments for the first set of samples is shown in Figure G-2. Each letter shown denotes the material type or process step taken.

TABLE G-2
SPECIAL SAMPLE TREATMENTS

	Thermal	Chemical	Etch
Preoxidation Treatment	Anneal in nitrogen between 800 C and 1200 C for periods up to 96 hours	NaOH NaCl HCl P_2O_5	HF + HNO_3
Postoxidation Treatment	Anneal in nitrogen at 1150 C for various periods	NaCl HCl H_2 HF	HF

Resonance Spectra

Electron spin resonance technique.- The theory of electron paramagnetic resonance is well developed and the technique widely used to study chemical structure and bonding of paramagnetic materials. The interactions that the unpaired electrons have in real materials are generally complicated. It is through these interactions which perturb the magnetic states of the system, that the materials can be studied by electron spin resonance. A system of free electrons has its electron spins and associated magnetic moments distributed randomly in all directions each with the same energy. If a steady magnetic field is applied to the system the electrons will align themselves either with or opposite to the applied field. These two system states will have different energy levels in the applied field. By superimposing a microwave radiation on the sample field electron transitions can be made to the higher energy state and this loss in microwave energy detected as a resonance condition. Those electrons in the higher energy state will emit photons and return to the lower energy state. Other mechanisms allow these electrons to give up their energy also and these lead to a study of relaxation processes between the electrons and the lattice or other spins. The simplest condition for microwave absorption of energy is that the microwave frequency f satisfy $hf = g \mu H_o$ where H_o is the applied constant magnetic field, g is the spectroscopic splitting factor (a tensor in general), with h and μ constants. The factor of interest is usually the g-factor. It is analogous to the Lande g-factor which describes the addition of spin angular momentum to orbital angular momentum to give the total angular momentum. The free electron g-factor has a value of 2.0023. Measured g-factors which differ from this valve are a measure of interactions involving the orbital angular momentum of the unpaired electron. Since this momentum depends on the chemical environment the g factor also depends on this environment. In a solid the energy levels of the unpaired electrons cannot be taken as the Zeeman splitting mentioned above since the electron is coupled with many other fields from its surrounding environment in addition to the applied magnetic field.



LEGEND:
- M - MONOSILICON INTRINSIC SILICON
- M^1 - MONOSILICON SILICON (31-34 OHM CM) BORON
- T - TEXAS INSTRUMENTS (8-12 OHM CM) PHOSPHORUS
- A_1 - ANNEALED 6 HOURS AT 800C IN N_2
- A_2 - ANNEALED 96 HOURS AT 800C IN N_2
- A_3 - ANNEALED 4 HOURS AT 1150C IN N_2
- E - ETCHED IN HF + HNO_3 TO REMOVE 750 MICRONS
- W - WET OXIDE 6 HOURS AT 1150C
- D - DRY OXIDE 72-87 HOURS AT 1150C
- N - NaOH ADDED DURING OXIDE GROWTH
- H - HC1 ADDED DURING OXIDE GROWTH

Figure G-2.- EPR Sample Preparations

The equipment used in this study was an X-band Varian Model 4500-10A EPR spectrometer with 100 Kc modulation. The powdered samples about 1.5 cm in length were put in a 3 mm diameter quartz tube, and initial experiments were performed at room temperature. The maximum sample width that will fit into the microwave cavity is one cm; however, it was found necessary to use the thinner samples because of large energy losses when the silicon dioxide sample extended into the electric field in the cavity.

To induce electron spin flipping the silicon dioxide sample is simultaneously subjected to a dc magnetic field H_0 and a weak microwave field whose frequency is near the precessional frequency of the electron. A block diagram of the Varian EPR spectrometer used in this investigation is shown in Figure G-3. A Klystron oscillator provides the microwave field at 9.5 Kmc while a large electromagnet provides an H_0 of about 3400 gauss for this type sample. The EPR cavity is tuned to resonance with the microwave field with the sample in place inside the cavity. The cavity is connected to one arm of a microwave bridge, another arm of which contains a crystal detector, and the bridge is adjusted for balance in the absence of electron resonance. During spin flipping energy is absorbed from the microwave field which unbalances the bridge and is sensed by the crystal detector.

The resonance data taken in this study was recorded on either a single or a dual channel recorder with the sample temperature between -180 C and + 300 C. Use was made of a dual cavity with the second one providing a reference standard. The resonance spectra to be shown below were recorded by sweeping the field H_0 about one hundred gauss on each side of 3300 gauss keeping the microwave frequency fixed at about 9.3 GHz. The data recorded as the intensity of the resonance signal is the radio frequency magnetization $X''H$ rather than the susceptibility X'' or the power absorbed $1/2\ (\omega H^2 X'')$ due to the crystal detectors employed in the type equipment used here. These resonance absorption signals do however represent the first derivation of the energy absorbed as a function of applied dc field strength. Precise g values can be determined by measuring the microwave frequency and magnetic field strength at resonance or by comparison of the unknown signal with that of a known sample. This latter method was used in this investigation by employing a dual sample cavity.

Signal types detected. - Three basically different electron spin resonance absorption signals were recorded from the powder samples investigated on this part of the program. A fourth type was recorded from single crystal samples with aluminum deposited over the oxide and might be caused by oxygen vacancies.

The first or main type of signal was detected from all silicon and silicon dioxide powder samples. This signal has been reported by others investigating the properties of silicon alone (Ref G-5 and G-6). The silicon signal is attributed to an oxygen-vacancy pair on the surface formed by the capture of an oxygen atom (or ion). This oxygen is adsorbed in a vacancy created by the mechanical damage when the silicon is crushed into a powder.

The second signal is the one of main interest in this investigation. Both it and the first signal are shown in Figure G-4 for Sample A (TW) on which it was first detected. These signals were recorded at room temperature from silicon dioxide

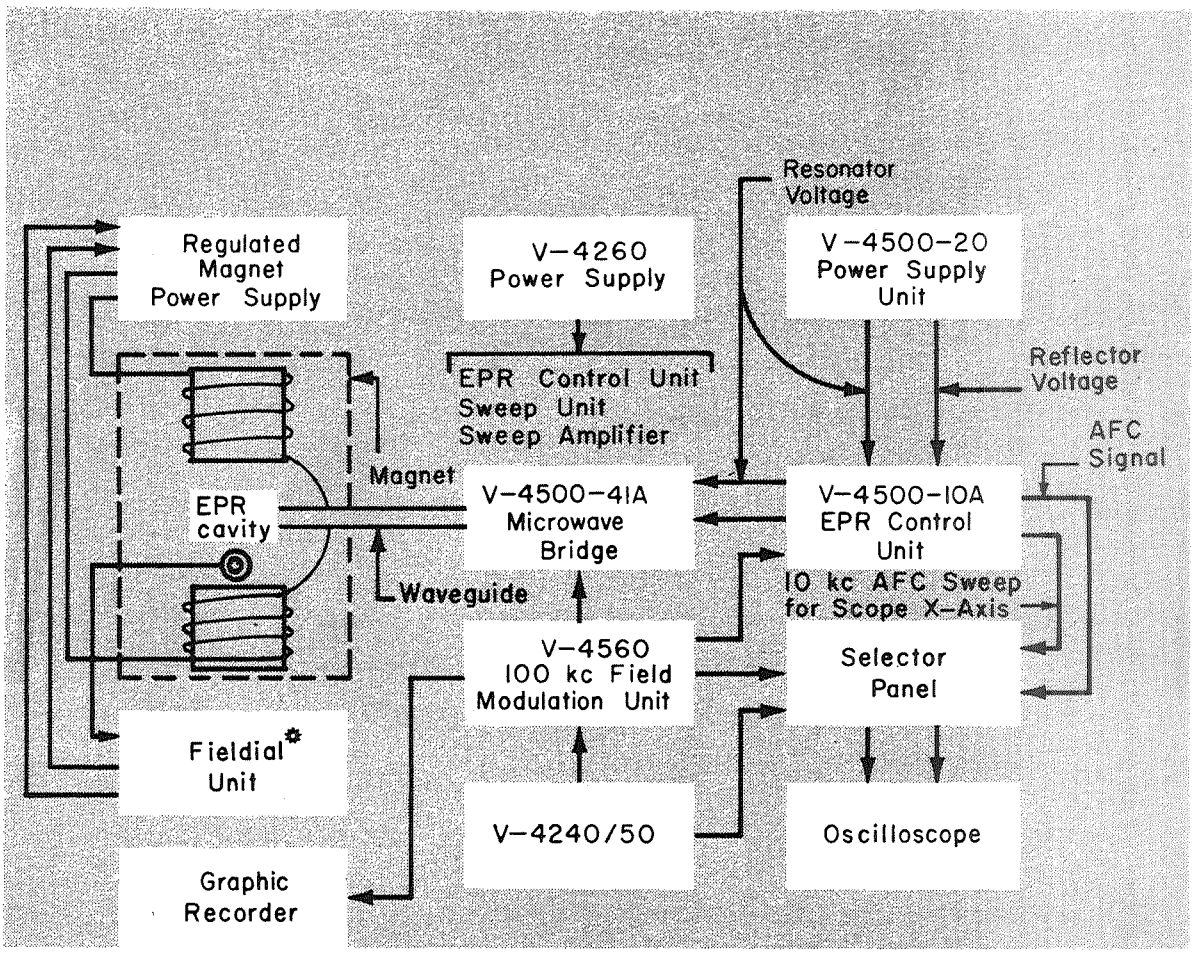


Figure G-3.- Block Diagram of the Varian V-4502 EPR Spectrometer Systems

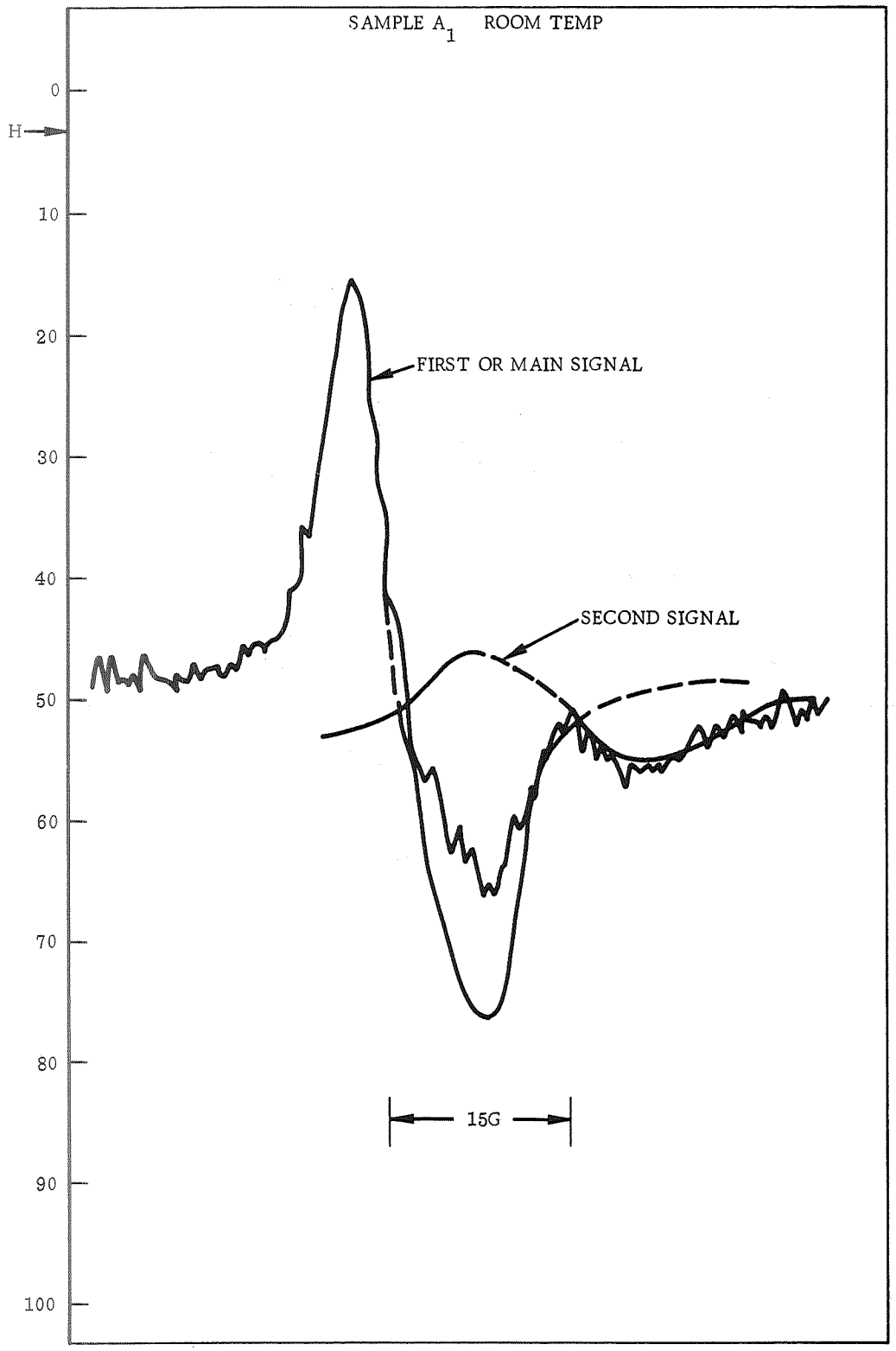


Figure G-4. - Discovery of Second Signal or Silicon Dioxide Grown Wet by Convection Method

grown wet at 1150 C to a thickness of 12,000 Å. The second signal will be discussed below in more detail. It is normally only recorded from oxide samples grown wet.

The third signal was found with silicon dioxide baked in hydrogen for one hour at 1150 C. It had been reported earlier by another investigator (Ref G-7) performing the same type study as being done on this program. He did not detect any signal from silicon dioxide so he baked his sample in hydrogen and then found an additional resonance. This signal is not related to the second one being investigated here and will be only briefly discussed later.

Signal characteristics. - There are many factors which can affect the character of EPR signals made on the silicon dioxide samples. The impurity atoms in the unoxidized silicon for the cases of both donors and acceptors do not alter the absorption curves. After oxidation the sample has oxygen interstitials, thought to be the predominant diffusing agent during oxidation and leading to acceptor states, as well as trivalent silicon and oxygen vacancies which are considered to produce donor states. These should contribute to the character of the absorption curves, along with the electron spin interactions with neighboring nuclei and the resulting local magnetic fields that alter the symmetry and lead to hyperfine splitting. Silicon is mostly (92 percent) Si^{28}, but the Si^{29} (4.7 percent) atoms, for example, have a nuclear spin of 1/2 while Si^{28} has zero nuclear spin. Thus, even the Si^{29} unpaired electron spins can interact with their nuclei and alter the absorption curve. The unoxidized silicon samples produced a strong symmetric absorption curve of about 25 gauss full width, while the oxidized sample showed an asymmetric complex curve indicative of multiple absorptions. The large signal to noise ratio with the unoxidized sample permitted a scan of 50 gauss in 10 minutes, and showed the absorption derivative curve was symmetric and without hyperfine splitting. The detected resonance absorption with the first oxidized sample was at the lower limits of detection of the equipment. Figure G-5 is the resonance absorption curve for a wet oxide sample, which more clearly shows both the first and second signals at room temperature.

The thermally grown silicon dioxide on powdered silicon produced a multiple absorption curve in contrast to the single symmetric absorption curve obtained from bare silicon. To factor out any effect of the dopant (mainly phosphorus) in initial silicon samples, intrinsic silicon was then used. The absorption curves with intrinsic silicon were found to be nearly identical with the earlier 8-12 ohm-cm n-type samples. Thus the main absorption mechanism observed in both cases appears to be associated with surface damage in the silicon caused by the pulverizing of the single crystal wafers. This was also verified on the oxide samples by using HF to remove the oxide from one sample and comparing its absorption intensity with a bare sample. The use of powder samples was found to be necessary to provide enough surface area for detectable energy absorption.

As noted above, it is thought that the main absorption curve is caused by oxygen-vacancy pairs produced at vacancy defects by pulverizing the silicon. A 100 cm^2 surface area of silicon contains about 10^{17} atom sites with the surface mostly (111), the main cleavage plane for silicon. This main absorption curve is reported to disappear if at least 10^{-4} cm of the silicon surface is removed by HF plus HNO_3 but is

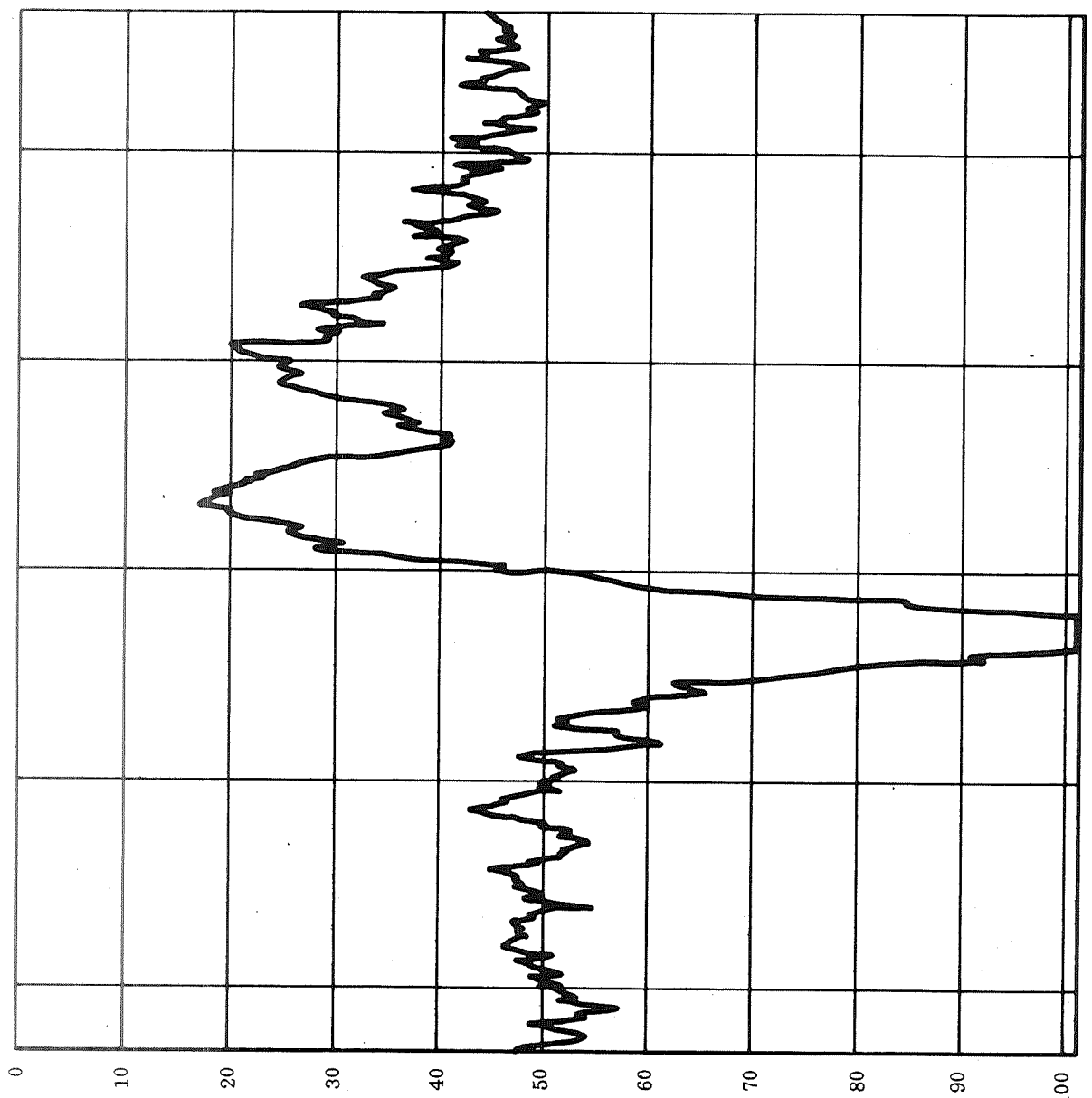


Figure G-5. - Sample A Showing Second Signal at 20 C

not removed by treatment with concentrated HF, HNO_3, or HCl acting alone (Ref G-8). Thus the main absorption appears to be associated with the silicon and the silicon surface which has an estimated ratio of ruptured bonds to surface atoms of 1:5 in these samples. The reduction in intensity of this main signal after oxidation may be caused by annealing effects during the high temperature oxidation process.

A large number of samples with various surface preparations were made in this study to investigate several phenomena reported in the literature. Two of these are the removal of surface damage by etching and the atomic surface reconstruction produced by annealing (Ref G-9. As mentioned above, a removal of more than one micron of silicon surface causes the EPR signal due to silicon surface damage in the powder samples to disappear. Samples ME and MEA had 750 microns of silicon removed from the surface, and yet a relatively strong symmetrical absorption was still present. This signal is still observed, along with the second signal, after growth of an oxide on these samples. It should be noted that the EPR spectrometer used here is one of the best available and has close to the theoretical detection limit of about 3×10^{11} ΔH spins per gauss where ΔH is the signal width. The second phenomenon on the effects of annealing was difficult to determine because of some very broad (1-2 Kg) drift lines recorded from the annealed samples which obscured any detailed line structure.

Figure G-6 shows the second signal (shifted to the left of the main signal) of sample MA_1W (Monosilicon intrinsic, Annealed 6 hours in N_2 at 800 C, and a Wet oxide grown) taken at -160 C that still has a relatively large second signal intensity after annealing. Figure G-7 shows the second signal being brought out on sample MA_1EW at -150 C, which indicates how it could be overlooked at low gains while taking this type of data. Figure G-8 shows the second signal on two other samples that were etched prior to oxidation in a and annealed after etch in b.

Two samples, TW and M, were subjected to heat treatment in dry nitrogen during EPR scanning to seek any changes in the absorption curves. Data were recorded from 0 C to 300 C in 50 C steps. No qualitative change in the shape or character of the curves was noted. The effect of heat treatment on silicon has been shown by low energy electron diffraction experiments to cause a surface rearrangement of silicon atoms (Ref. G-10). Several surface models have been postulated on the basis of these experiments. It is of interest to note that upon admitting oxygen during the low energy electron diffraction study at elevated temperatures the pattern shifted to show that the silicon atoms arranged themselves back to the diamond configuration of the bulk crystal. After a few hundred Angstroms of oxide form on the silicon the diffraction patterns disappear.

To more fully study the second signal of the oxides grown wet a temperature controller and a dual cavity were employed. The temperature of the oxide sample could be varied from -180 C to +300 C while continuously scanning. A reference sample of either pitch in KCl or DPPH was used in the reference cavity which remained at room temperature.

Samples A (TW) and MEA_1W were cooled to -180 C to improve the absorption signal intensity and help in resolving the second peak. A rather unusual and interesting phenomenon was observed as the samples cooled, namely, the second peak appeared to shift position with respect to the main peak. This shift of about 30 gauss is shown for sample A in Figures G-9 and G-10. The physical origin of this second

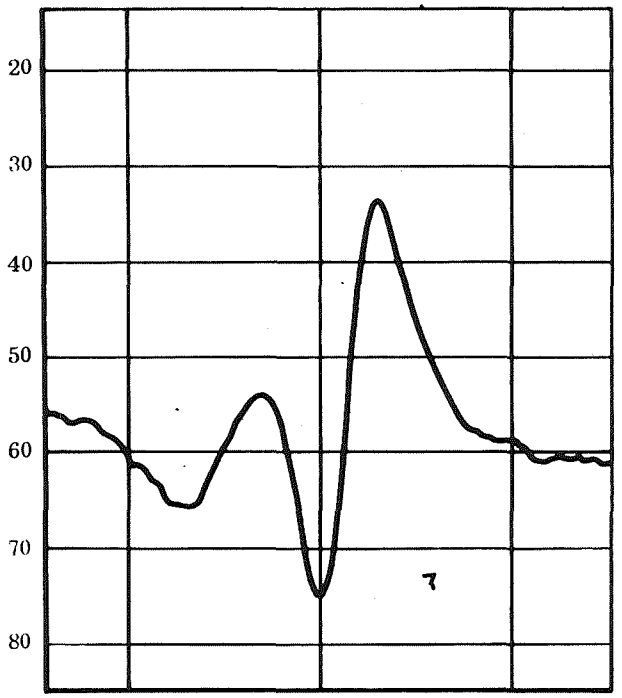


Figure G-6. - Sample MA_1W at -160 C

peak and the temperature dependent shift mechanism were considered with known interactions which affect the g values. There are two types of magnetic dipole interactions that might be considered here since silicon is about 5 percent Si^{29}, which has a nuclear spin I = 1/2. One is called the anisotropic dipolar hyperfine interaction caused by the ordinary coupling of the electron magnetic moment with the nuclear magnetic moment. The other is the Fermi contact, or isotropic hyperfine interaction, arising from the relativistic treatment necessary when the electron motion is near the nucleus, causing a very large kinetic energy increase. This again couples the dipoles and shifts the energy levels. The second signal does not appear to be due to the dipolar hyperfine interaction since this usually produces two separate peaks about the main one, nor is it characteristic of the signals reported in the literature for silicon surface damage or surface reconstruction due to heat treatment of the silicon. Since it has been observed only with the SiO_2 samples and for both the phosphorus doped and intrinsic silicon, it definitely appeared to be a signal originating from the oxide. It is possible that one of the signals is broadened with the temperature variation and only appears to shift.

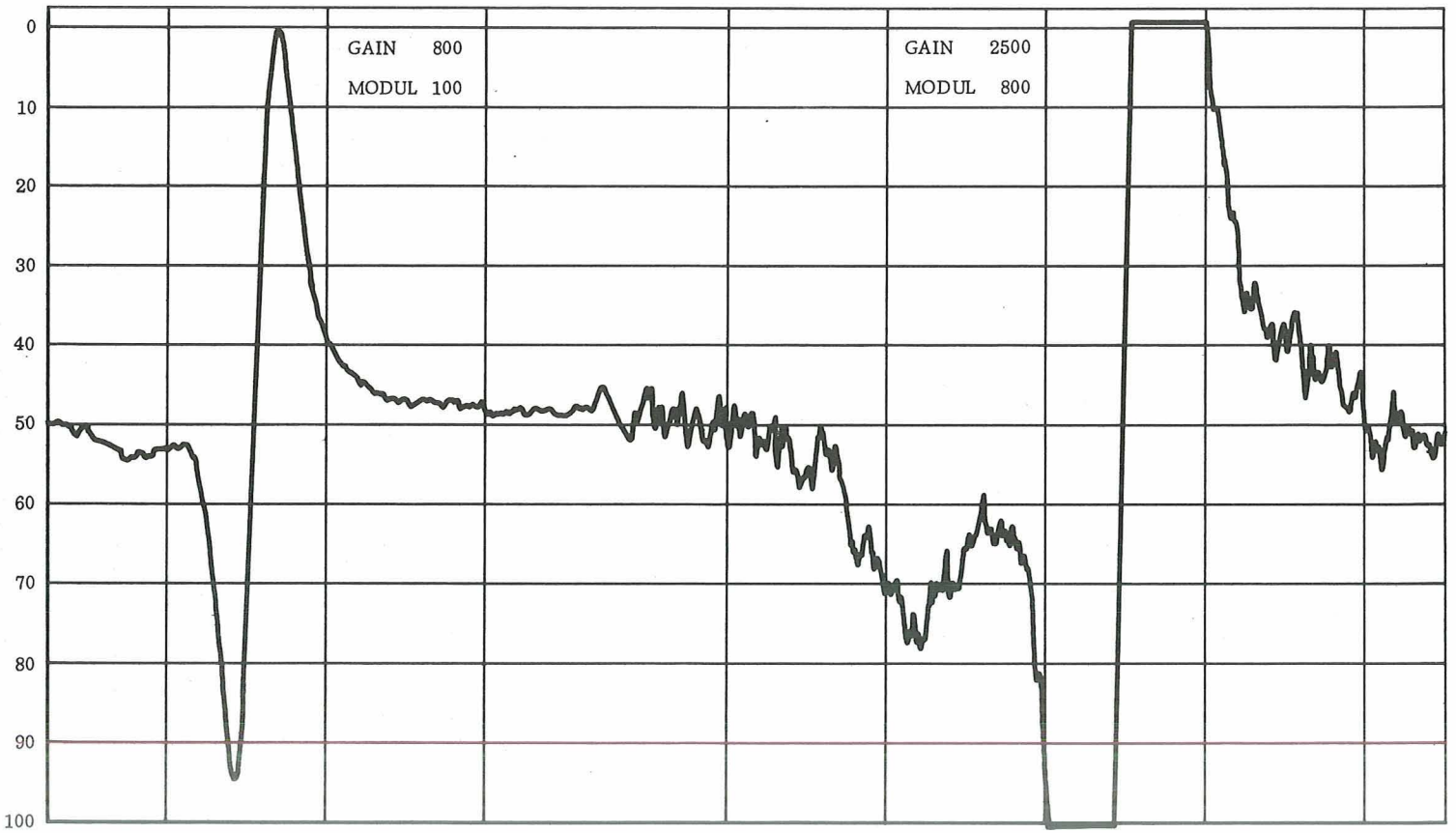
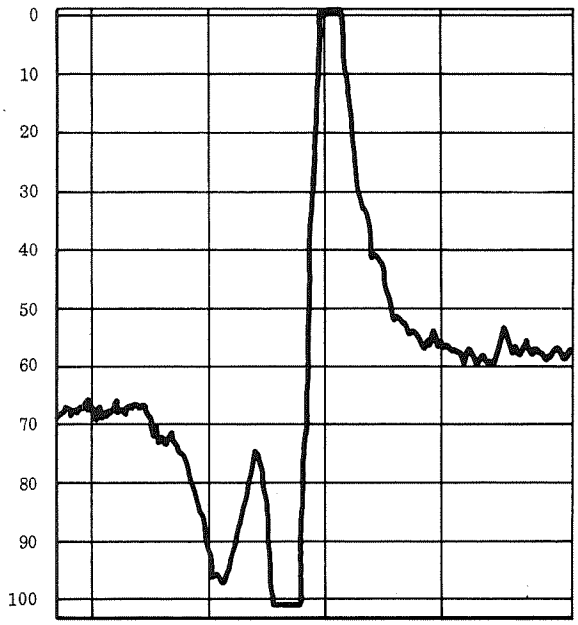


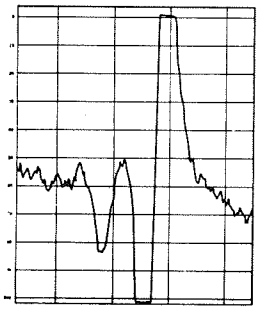
Figure G-7. - Sample MA_1EW at -150 C Showing How Second Signal Is Brought Out by Increased Gain



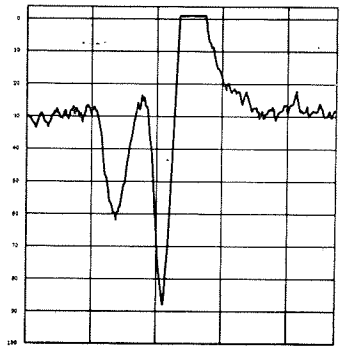
a. Sample MEW

b. Sample MEA_1W

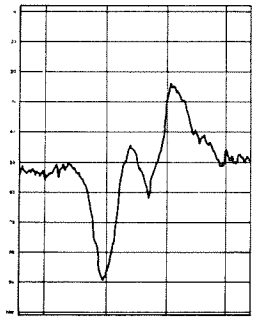
Figure G-8. - Second Signal at -160 C



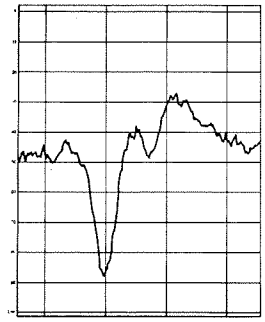
-164 C



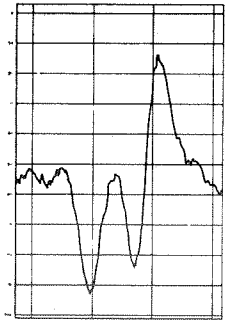
-125 C



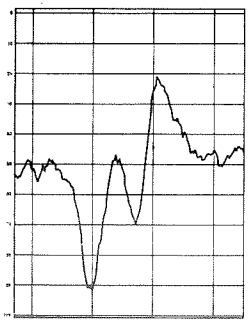
-50 C



-30 C

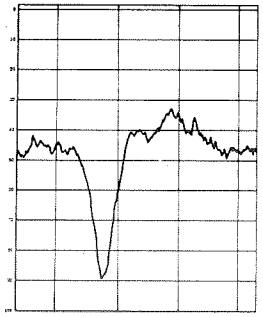


-90 C

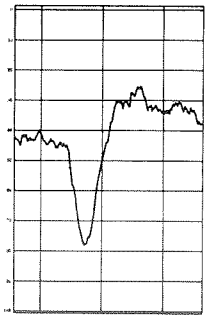


-70 C

Figure G-9. - Sample A Going From -164 C to -70 C



-10 C



+40 C

Figure G-10. - Sample A Going From -50 C to + 40 C

Line shape and spin concentrations. - Another factor in analyzing resonance spectra is the line shape. The shape of the absorption curve is influenced by many internal interactions that the unpaired electrons undergo and lead to two classes of lines. One class is called homogeneously broadened which arises when all the electron spins have the same local environment. The second class is called inhomogeneously broadened and refers to electron spins interfacing through a variety of different environments, such as local impurities and defect centers. In EPR of solids most powdered materials exhibit inhomogeneous broadening depending on the anisotropies of the spin interactions. Two approximate line shape equations are the Lorentzian and Gaussian:

$$I = \frac{I_o}{T^2 (H - H_o)^2 + 1} \qquad \text{(Lorentzian)}$$

$$I = I_o e^{-b (H - H_o)^2 T^2} \qquad \text{(Gaussian)}$$

where I_o is the intensity of the absorption line at its center, H_o is the magnetic field intensity at the center of resonance, and b and T are constants related to half-widths of the two type curves. By differentiating these equations the maxima are found and the experimental data normalized for comparison. Figure G-11 shows the plots of theoretical position (TP) on the curve versus the experiment position (EP) for a sample of intrinsic powdered silicon. If a straight line results for a given absorption spectrum, then the absorption is either Lorentzian or Gaussian. As can be seen, the line shape in this case is Lorentzian, and lines having this shape are usually homogeneously broadened. Similar calculations on data for oxidized samples did not produce a straight line for either plot. Physically, the Lorentz shape arises in a manner similar to a harmonically bound electron which, during the emission of radiation, is randomly and rapidly perturbed in its motion, producing a Lorentzian distribution of frequencies. In EPR measurements this perturbation can occur through the exchange of equivalent electrons between different paramagnetic silicon atoms when the electron wave functions overlap. For the sample here this would obviously lead to the case of homogeneous broadening. The Gaussian line shape will arise when each paramagnetic electron sees a slightly different internal magnetic field from neighboring nuclei or electrons. An example of this would be a substitutional impurity producing a variation of the total field the electron sees during the spin flip process. There is no reason to expect that the SiO_2 samples should produce a Gaussian line shape since in general the data from complex systems such as this rarely fit either line shape.

It is possible to measure the number of unpaired electron spins for a given absorption signal by comparing it to the signal of a known standard. This has been done only on a silicon sample using its signal. A standard sample of 0.1 percent pitch in KCl was used in the reference side of the dual cavity and the dual data recorded. The standard has 3×10^{15} electron spins per centimeter of length. The

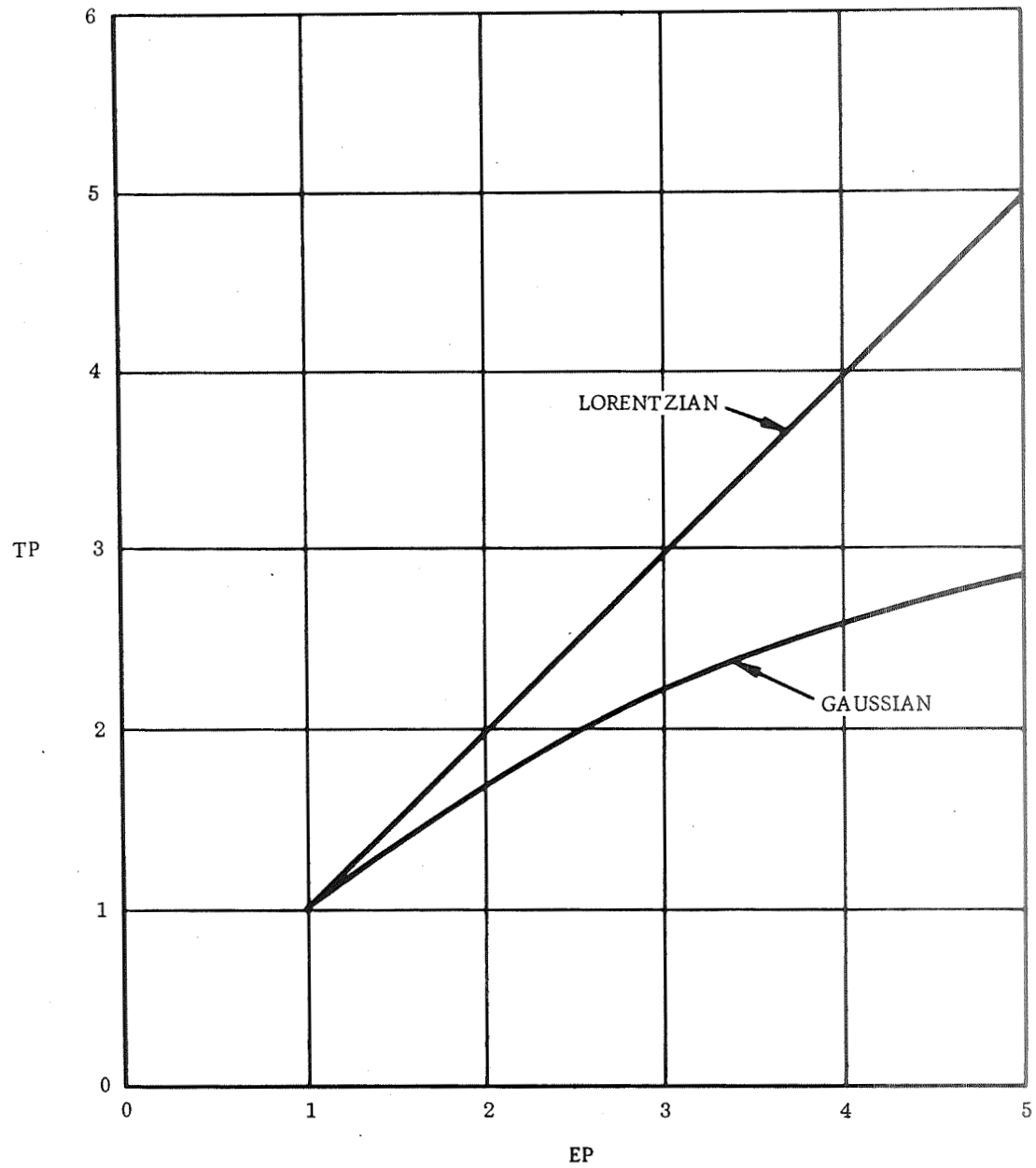


Figure G-11.- Line Shape Calculations

two samples were scanned then interchanged and scanned again. Using the observed gain settings and the measured first moments of the absorption derivative curves the spin concentration of the silicon was calculated to be 3.3×10^{14} spins per cm or a total of 8.4×10^{14} spins with an estimated accuracy ±25 percent. This information provides a qualitative comparison os spin concentration for the silicon dioxide samples where it is not possible to measure their moments because signal one and signal two overlap each other.

Treated oxides. - As the large number of articles in the literature indicate, there are many effects such as ambient (Ref G-11), thermal (Ref G-12), chemical and oxide growth parameters which can cause changes in the electrical characteristics of silicon devices passivated with silicon dioxide. Most of these are associated with either oxide states, interface states or oxide defects acting as trapping sites. To gain more experimental data on the oxide samples and the second signal studied here, a number of them were treated with chemical contamination. The first samples to be treated were those in which the silicon powder was contaminated with HF, NaOH and NaCl prior to oxidation. The second signal was found to have increased in size with these contaminated samples.

It appears from the data that both HF and NaCl contamination produce a larger second signal which exhibits the same thermally activated g value shift or line broadening. Bare silicon contaminated with NaCl or HF gave resonance signals with quite a bit of drift and it was not possible to ascertain the presence of a second signal from them. Information relevant to these samples and the resulting EPR data is given in Table G-3 where the notation (MW+HF) means the oxide was grown wet on type M silicon and then HF was added directly to the sample for temperature and time shown. The symbol (M^1+NaCl) W means silicon type M^1 was soaked in NaCl and the oxide then grown wet on the contaminated oxide.

From the data it was found that silicon contaminated with NaCl and silicon dioxide contaminated with HF gave an increased second signal. This increased second signal is shown in Figure G-12 for sample (M^1 + NaCl) W.*

This sample was prepared by soaking 32 ohm cm powdered silicon in a 10 percent solution of NaCl. After the solution had dried the sample was placed inside the oxidation furnace at 1150 C and a wet oxide grown for 8 hours. EPR data recorded at various temperatures between -184 C to 300 C showed a marked decrease in the signal quality above 0 C.

The scan for -120 C was run in the single cavity while the others were taken with the dual cavity during the same run using pitch in KCl for a reference. The noise is large from the reference cavity because of the low frequency modulation of 200 cps used on it.

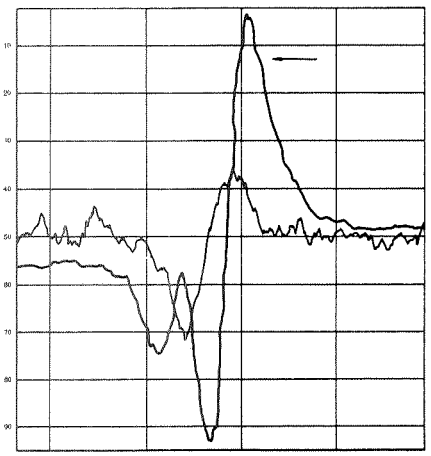
*(Note that dual cavity data was taken in red and blue ink. The oxide sample is identified in the figures here by the arrow.)

TABLE G-3
EPR SAMPLE DATA AND RESULTS

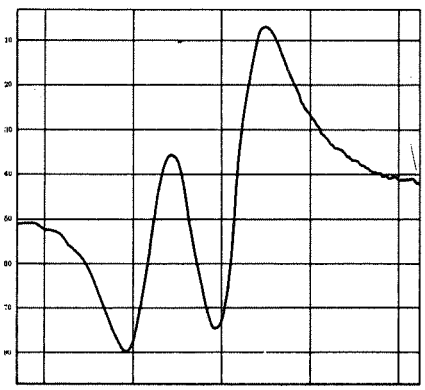
Sample Preparation	Oxidation Period	Oxidation Temperature	Contam-ination Period	Contam-ination Temperature	Type of Silicon ohm-cm	Signal Data (See Key)
(M+HF) W	8 hr	1150 C	-	-	Intrinsic	2M
(MW+H_2)	8 hr	1150 C	1 hr	1150 C	Intrinsic	2M, 3M
(MW)	8 hr	1150 C	-	-	Intrinsic	2M
(MW+HF)	6 hr	1150 C	6 hr	40 C	Intrinsic	WS
(MW+NaCl)	6 hr	1150 C	6 hr	40 C	Intrinsic	WS
(M+HF+ NaCl)	-	-	6 hr	40 C	Intrinsic	WS
(MW+HF) W	6 hr	1150 C	-	-	Intrinsic	N2
(MEW)	6 hr	1150 C	-	-	Intrinsic	2S
(MEA_1W)	6 hr	1150 C	-	-	Intrinsic	2S
(MA_1W)	6 hr	1150 C	-	-	Intrinsic	2S
(MD)	87 hr	1150 C	-	-	Intrinsic	N2
(MED)	87 hr	1150 C	-	-	Intrinsic	N2
(M^{1}W+D*)	6 hr	1150 C	-	-	p 32	ND
(M^{1}W+HF)	6 hr	1150 C	1 hr	1200 C	p 32	2L
(M^1+NaCl) W	8 hr	1200 C	-	-	p 32	2L
(M^1+NaCl) D	90 hr	1200 C	-	-	p 32	2S
(M^{1}W+NaCl)	6 hr	1150 C	10 min	1200 C	p 32	ND
(TW)	6 hr	1150 C	-	-	n 10	2S
(TD)	87 hr	1150 C	-	-	n 10	N2
T (HC1+W)	7 hr	1150 C	-	-	n 10	WS
(T+NaOH) W	6 hr	1150 C	-	-	n 10	2M
(TW+A*)	6 hr	1150 C			n 10	N2

Key

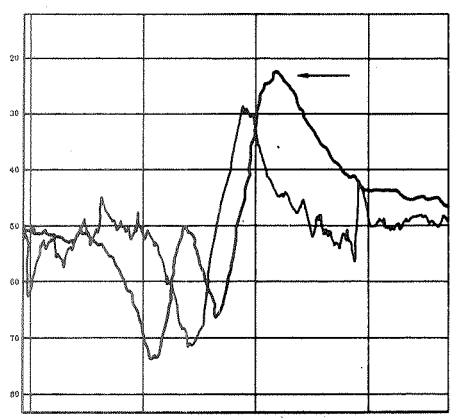
2S - 2nd Signal small
2M - 2nd Signal medium
2L - 2nd Signal large
3M - 3rd Signal medium
WS - Wavy data, inconclusive
N2 - No, 2nd Signal.
ND - 2nd Signal not detected
D* - Dry growth 2 hr, 1150 C
A* - Anneal (N_2), 2 hr, 1150 C
E - Etched silicon
A_1 - Annealed (N_2) 6 hr, 800 C



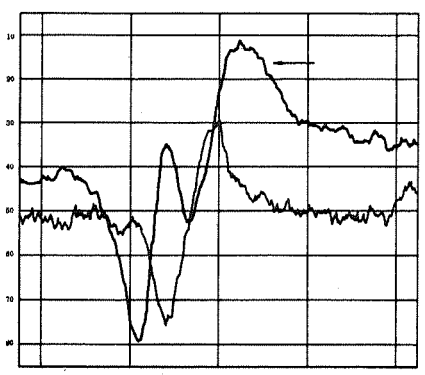
-120 C



-150 C



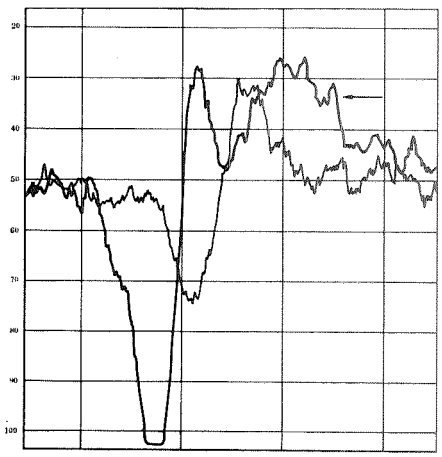
-20 C



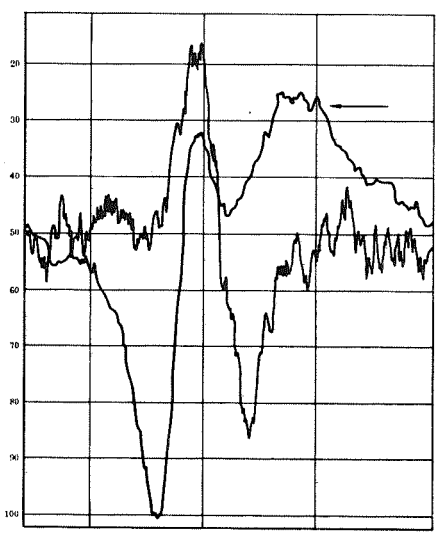
+10 C

Figure G-12. - Resonance Spectra of Silicon Dioxide Sample (M^1 + NaCl) W at Temperatures Between - 180 C and +100 C

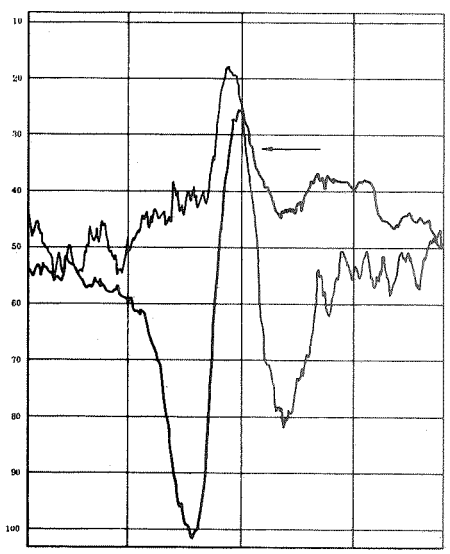
+30 C



+50 C



+60 C



+100 C

Figure G-12.- (Concluded)

From the data taken on sample (M^1 + NaCl) W, it is seen that going from -150 C to -80 C produces little change in the position of the two signals. At temperatures above 0 C it is more difficult to interpret the data because of decreased sensitivity. Sample (T+NaOH) W produced the same type second signal at -180 C as (M^1+NaCl) W as shown in Figure G-13, indicating that sodium deserves serious consideration in determining the chemical structure of these oxides. An oxide structure with sodium ions bonded to trivalent silicon atoms near the silicon-silicon dioxide interface has been recently proposed from data on MOS capacitance experiments and is among those being studied for correlation with these EPR results (Ref G-13). It appears that the second signal doesn't shift much until the temperature is near 0 C and then it shifts rapidly above 0 C and perhaps broadens out above 40 C.

To compare effects of contamination after oxide growth several samples shown in Table G-3 were contaminated with NaCl at both 1150 C and 40 C after oxidation and EPR runs made with them. The recorded signals were all very poor in that much drift and wavy patterns were found. It is not yet possible to conclude that the second signal is present on these samples even though a peak was usually found where it would be expected, along with many other nearby peaks. This is in contrast to contamination with HF. Samples contaminated with HF were made by either soaking the silicon prior to oxidation in a 0.5 percent solution of HF, followed by drying at 180 C, or by soaking a silicon dioxide sample in a 0.5 percent HF solution before insertion into the furnace at 1150 C or 40 C. The data were different from those with NaCl contamination above in that the strongest second signals were found with silicon dioxide soaked in HF. Figure G-14 shows the large second signal recorded on (M^1W+HF) at -180 C.

Figure G-15 shows a small second signal present for sample (M^1+NaCl) which is unique in that no second signal had ever been found with an oxide grown dry. This signal appears in the same location as the second signal on wet oxide samples and also changes shape with temperature.

With the experimental data recorded here it is still very difficult to postulate the identity or origin of the second signal because many substances have g values near this one and the physical system under consideration is quite complex. Even silicon-silicon surfaces without any heat treatment are not well understood. However, it appears that the second signal is related to the presence of sodium in the oxide for those samples contaminated with NaCl or NaOH prior to oxidation. The effect of baking in hydrogen, annealing in an inert ambient such as nitrogen and growing a dry oxide is to reduce the intensity of this second signal. For those oxides contaminated with HF it is possible that the HF reacts with bare silicon, either by etching through the oxide, or by acting on bare silicon caused by incomplete oxidation at points where the silicon particles were in contact with each other during oxide growth.

Additional EPR data were taken on samples (M^1W + HF), (M^1 + NaCl) and (TW). Of particular interest are the results on sample (M^1W + HF) under atmospheric and reduced pressures shown in Figure G-16. It is evident from the figure that outgassing of the HF treated sample (at 4 x 10^{-2} Torr) produces a significant reduction in the second signal. The second signals of the other two samples, however, were unresponsive to outgassing. The evidence appears to implicate the HF + Si system as a source

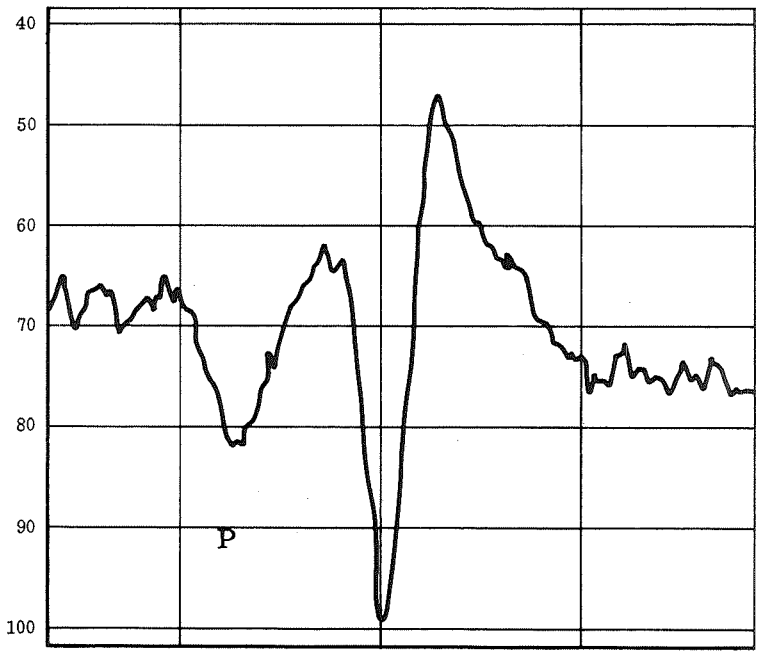


Figure G-13.- Sample (T + NaOH) W at -180 C

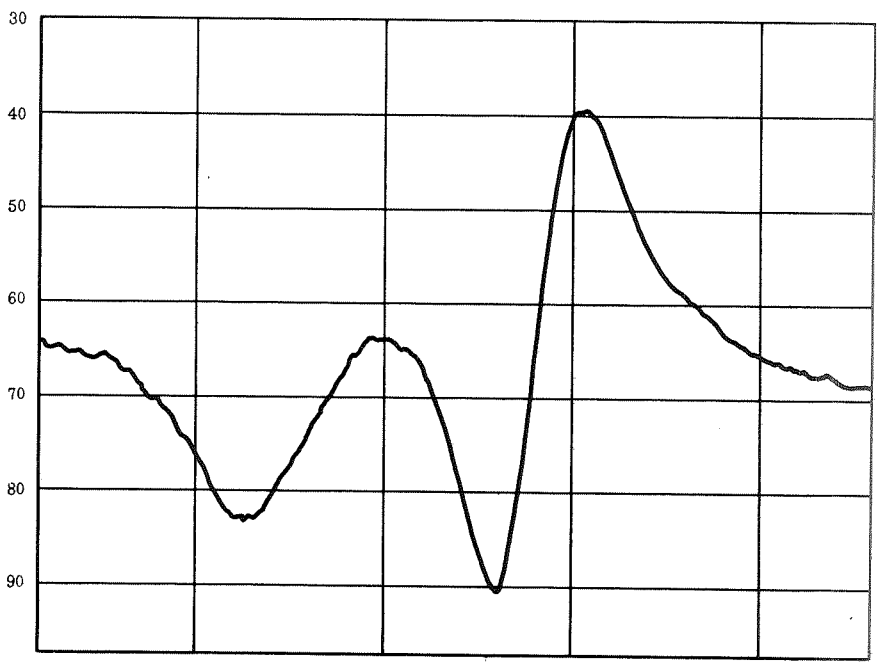


Figure G-14.- Sample (M^1W + HF) at T = -180 C

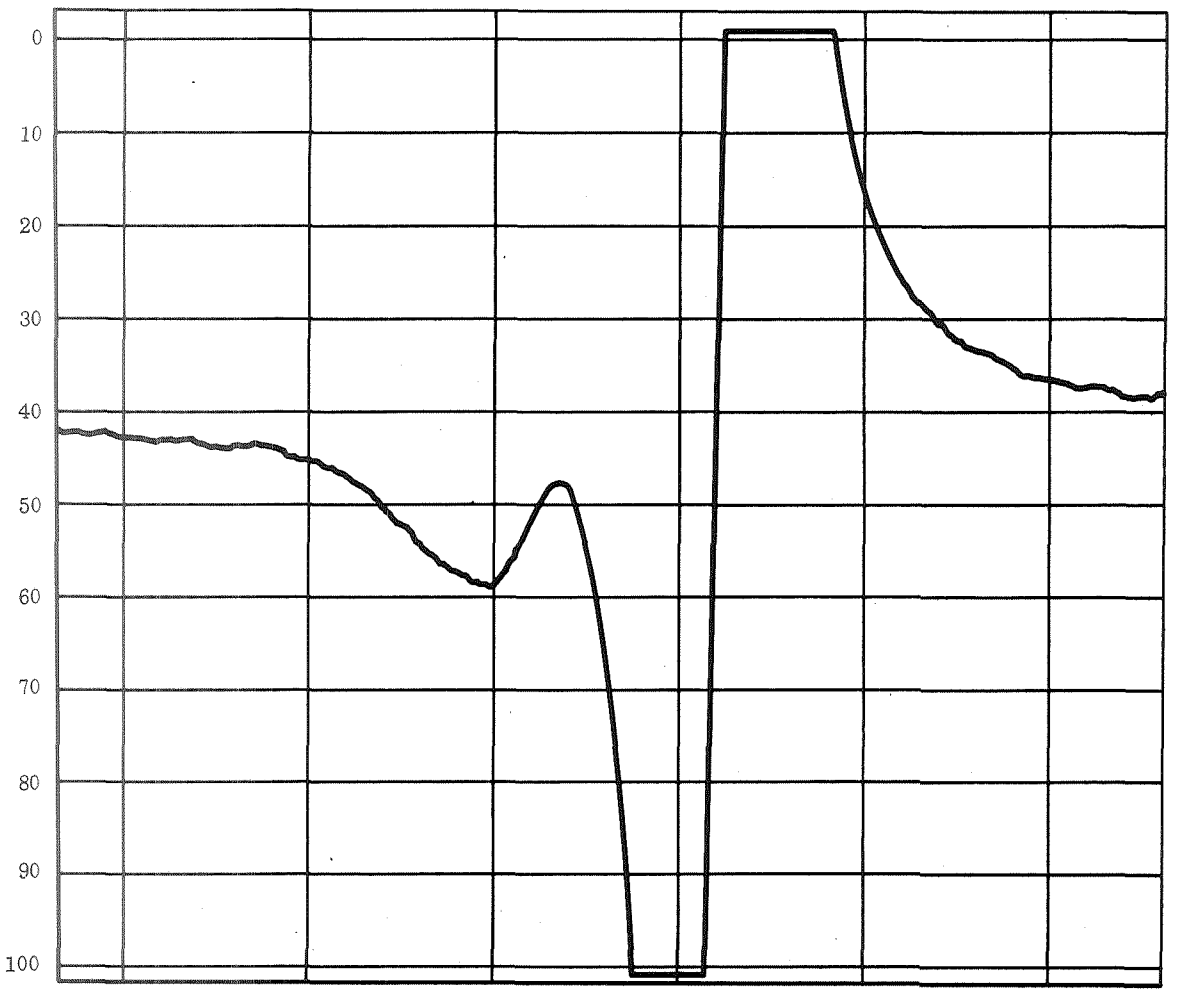
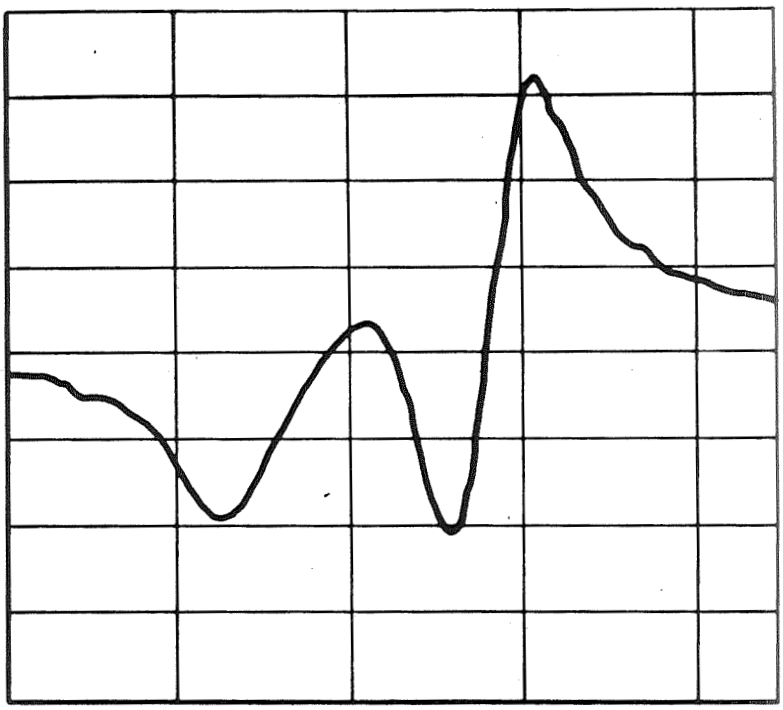
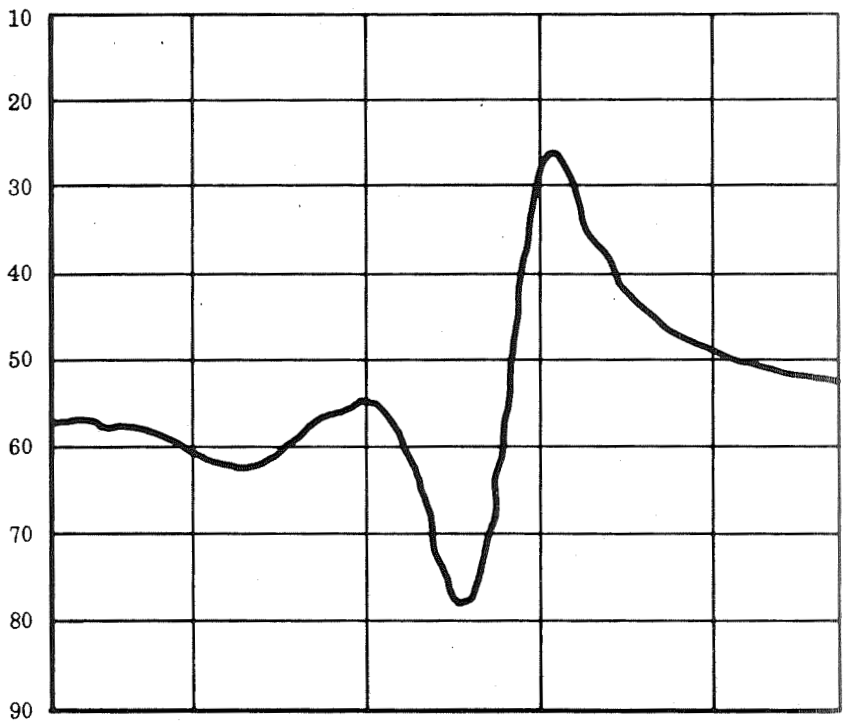


Figure G-15. - Small Second Signal at -180 C Detected From Oxide Grown Dry on Silicon That Had Been Contaminated With NaCl



a. Room Pressure



b. On Vacuum of 10^{-2} Torr

Figure G-16.- Second Signal of Oxide Treated by HF Shown at -180 C Under Room Ambient and Then Under Small Vacuum

of the second signal. It is known, for example, that SiF_4 (formed in the present experiment by HF + SiO_2) interacts with silicon at elevated temperatures to produce the biradical Si_2F_4 containing unfilled silicon orbitals. However, the reverse of this reaction at still higher temperatures should result in release of SiF_4 and deposition of "atomic" or finely divided silicon. This possibility fits well with the experimental conditions employed because the specimen (M^1W + HF) was baked for ten minutes at 1150 C in an inert atmosphere after treatment with 0.5 percent HF solution. The residual finely divided silicon then could act as adsorption sites for condensable gases during EPR Spectrometry. This also is a real possibility because the EPR Spectra were taken at -185 C, and the second signal reappeared on admission of room air to the outgassed sample. Although the possibility of residual contamination by fluorinated species cannot be ruled out, the reversibility of outgassing effects on the EPR signal appears to be associated with the sorption of atmospheric components on surfaces rendered sensitive by the HF treatment.

The implications of this finding with respect to integrated circuit processing may be significant because of the extensive utilization of pattern etching with HF followed by diffusions or other high temperature treatments. If the EPR second signal can be associated with positively charged atomic vacancies the present evidence indicates that HF may play a role in causing inversion and that steps should be introduced to remove it after it has served its function.

The independent main signal on silicon powder has been shown (Ref G-14) to be somewhat sensitive to various ambients and pressures, possibly as a result of residual surface damage. The lack of main signal change may be due to intact oxide passivation or to prior removal of surface damage by etching. According to earlier evidence it is highly unlikely that this main signal is associated with defects in the oxide structure.

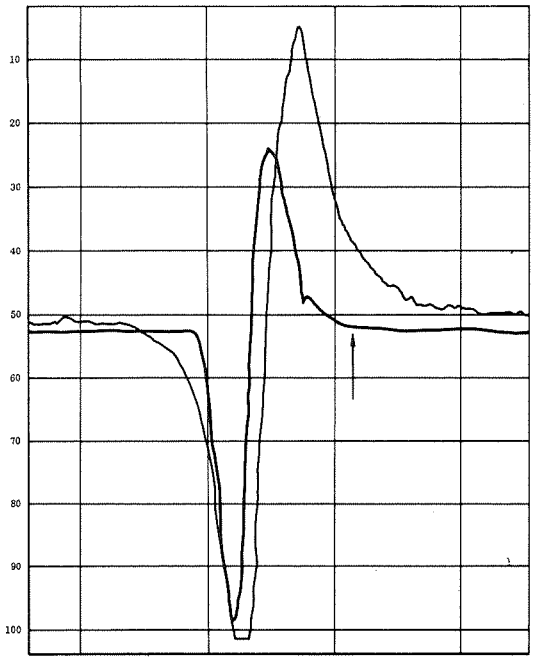
Oxides baked in hydrogen. - Only one other investigator has reported a study of silicon dioxide by EPR (Ref M-7). Silicon powder was made from p-type float zone silicon with a specific resistivity of more than 500 ohm cm. No signals other than the main one were found on these samples after they had been oxidized for two hours at 1200 C in dry oxygen. The samples were then baked in hydrogen at 1000 C for 10 minutes and a new signal found at liquid nitrogen temperature. This second signal disappears if the sample is annealed at 1200 C in dry oxygen after the hydrogen bake. It was postulated from a defect model by Revesz (Ref G-4) that the hydrogen at high temperature causes the formation of broken oxygen bridges and trivalent silicon with resulting unpaired electrons. This new signal found by Nishi is not one of those found during our investigation except that we were able to reproduce his signal by baking sample MW in hydrogen for one hour at 1150 C. Nishi's failure to find signals relatable to the silicon dioxide is due to several reasons. His oxide was only 2000 Å thick, it was grown dry on float zone silicon and the oxide area was small because of the large silicon particles used. The signal found with sample (MW + H) here, referred to as the third signal, did not show any temperature dependence. Since it has a lower g value than the main signal, while the second signal studied here has a higher g value, this third signal has not been pursured further. Many factors associated with heat treatments are possible in silicon-silicon dioxide samples that receive heat treatments (Ref G-15).

It is also of interest to note that Balk at IBM (Ref G-16) is reported to have performed EPR experiments on thermally-grown silicon dioxide with the results that a signal was found only when the final preparatory step did not include a hydrogen-containing species. This is opposite to the results of this study since only the wet oxides show additional spectra.

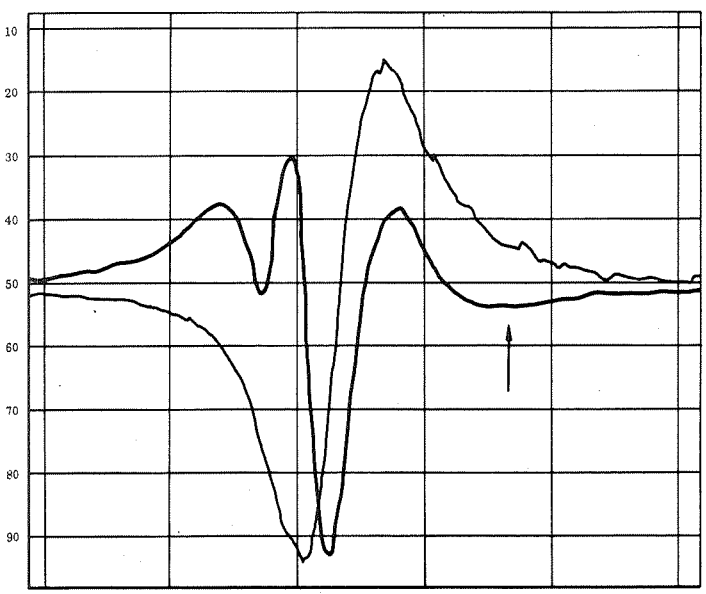
Metallized oxides. - Several silicon dioxide samples have been grown on single crystal silicon and then metallized with aluminum dots to measure possible oxygen vacancy generation as proposed by Burkhardt (Ref G-17) . EPR data taken on these samples has produced a very strong single signal. This signal is not thought to be from the aluminum itself since it will be paramagnetic only if ferromagnetic impurities are present in the aluminum. It does appear likely that this absorption peak may be a result of unfilled atomic orbitals arising from competition between aluminum and silicon for oxygen atoms originally linked only to silicon atoms.

Burkhardt's experiments on the dielectric relaxation of silicon dioxide led him to rule out sodium ions as a source of oxide instability and to postulate an oxygen vacancy generation mechanism based on a reaction of deposited metal with the silicon dioxide. To explore this possibility by EPR several samples of 800 Å oxide grown on single crystal silicon (10 ohm-cm, n type) with aluminum dots deposited on them by E-beam evaporation were prepared. The wafers were scribed into strips one in. long and 3 mm wide. Although the sample area was small (2.5 cm x 0.15 cm) the absorption signal was much larger than any recorded previously, including those of bare silicon powder with its much larger surface area. Silicon dioxide samples grown on single crystal silicon without aluminum have previously produced no signal even at high gains. This sample, (TW + Al), was only run at room temperature and produced only the single signal.

It has been reported (Ref G-18) that no resonance signals are obtained from aluminum between 4K and 300K unless ferromagnetic impurities are present. The aluminum used here was 99.999 percent and had been analyzed by emission spectrography, showing copper, iron and magnesium present in levels between 0.001 - 0.0001 percent. For the iron this represents about 10^{16} spins per cm^3. On a total volume basis the aluminum present in this sample was calculated to have about 3×10^{11} spins which is too small to produce a detectable absorportion signal with the available equipment. It appears, therefore, that the present signal is derived solely from an interaction between the aluminum deposit and the oxide surface, in substantial agreement with Burkhardt's model. The g value of this single signal has been calculated using the dual cavity and found to be 2.0023 ± 0.0004 at -180 C. It does not appear to be temperature dependent. To check for possible trace impurities these samples where analyzed with the electron microprobe. No elements above atomic number four other than aluminum were found on the oxide. Two of these samples were etched in HCl and then tested. These gave a multiple signal at zero C while only showing a single one at -180 C as shown in Figure G-17. This effect was reversible. Electron microprobe analysis of these two samples revealed carbon and chlorine around the residual aluminum dots. The origin of this carbon contamination of more than 2 percent by weight is unknown and has not been pursued further.



a. T = -180 C



b. T = -50 C

Figure G-17. - Spectra of Single Crystal Silicon With the Aluminum on Oxide Partially Dissolved by HC1.

Summary

From the data taken on many oxide samples in this study it appears that sodium and fluorine can be retained in the thermally grown oxides in relatively large amounts. Figure G-18 shows the possible defect structures that can exist in the silicon dioxide samples studied here. Table G-4 presents a summary of the signal types detected.

Attempts have been made to determine g values for these signals by comparison with either pitch in KCl or DPPH. The main obstacle to this has been the partial overlap of the second signal with the main one due to the silicon. It appears from the data taken with the dual cavity and plots of ΔH vs g that the second signal has a g value of 2.011 ± 0.001 at -180C with $\Delta H_{p-p} = 9$ gauss which overlaps the reported main signal at $g = 2.006$. The second signal is either temperature - dependent and shifts 17 gauss past the main signal when going from -180 C to +50 C or one signal has much line broadening with temperature. Introduction of trace contaminants during oxidation increases this signal intensity markedly and leads to the postulated retention of sodium and fluorine impurities as the origin of the second signal.

The unexpected resonance signal for the samples with aluminum over the oxide is considered important because aluminum is widely used as interconnections over the oxide on integrated circuit surfaces. This type oxide sample is actually simplier to investigate than the powder samples since it is on a single crystal of silicon. It could be electrically biased during EPR scanning to provide further data on the capacitance voltage behavior of the oxide. It is recommended that this type sample be further studied rather than the silicon powder samples which are very difficult to analyze because of the overlapping temperature dependent behavior of the resonance signals and the more difficult nature of powdered silicon material. The relevance of this type sample to modern planar technology further supports this recommendation.

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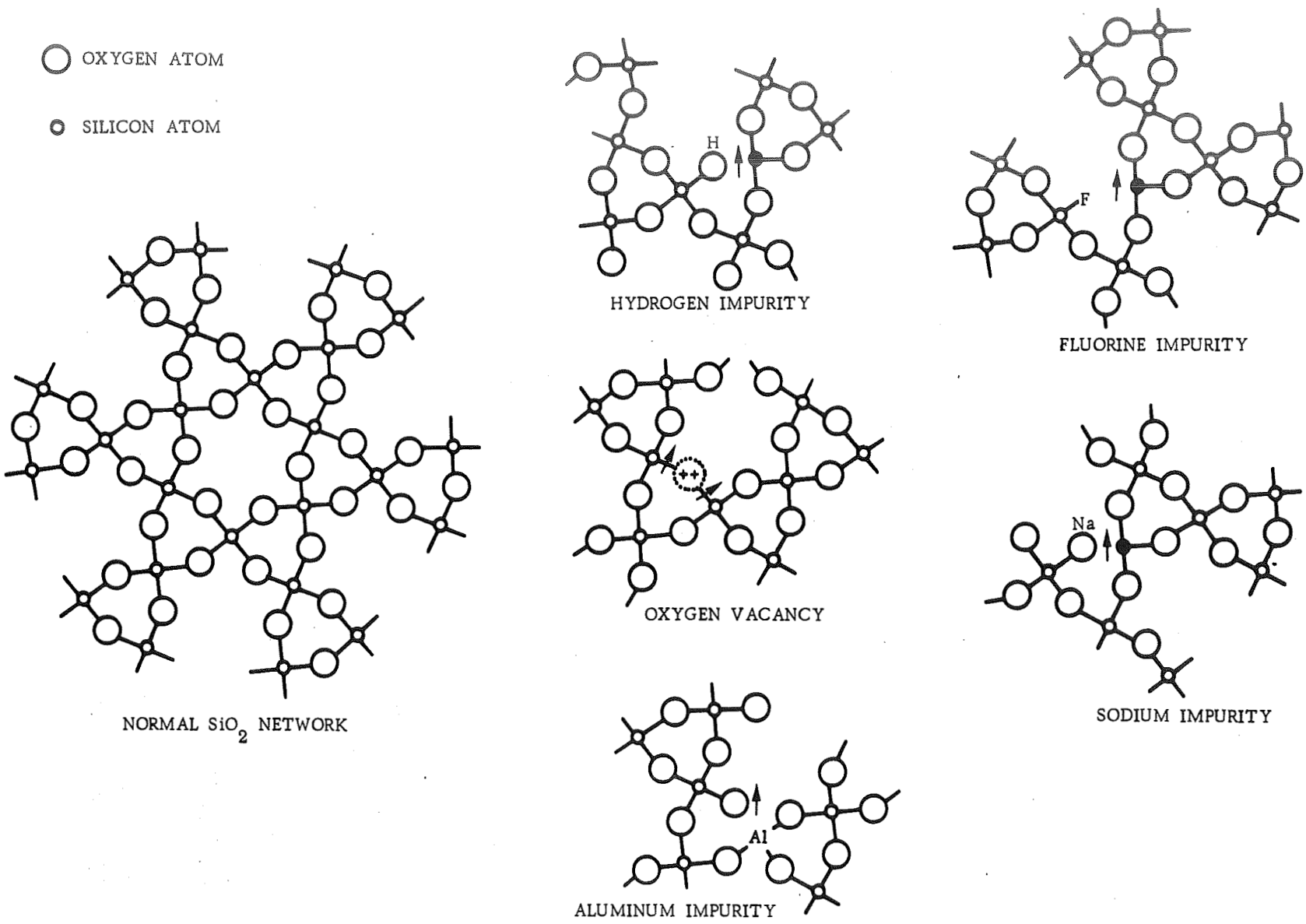
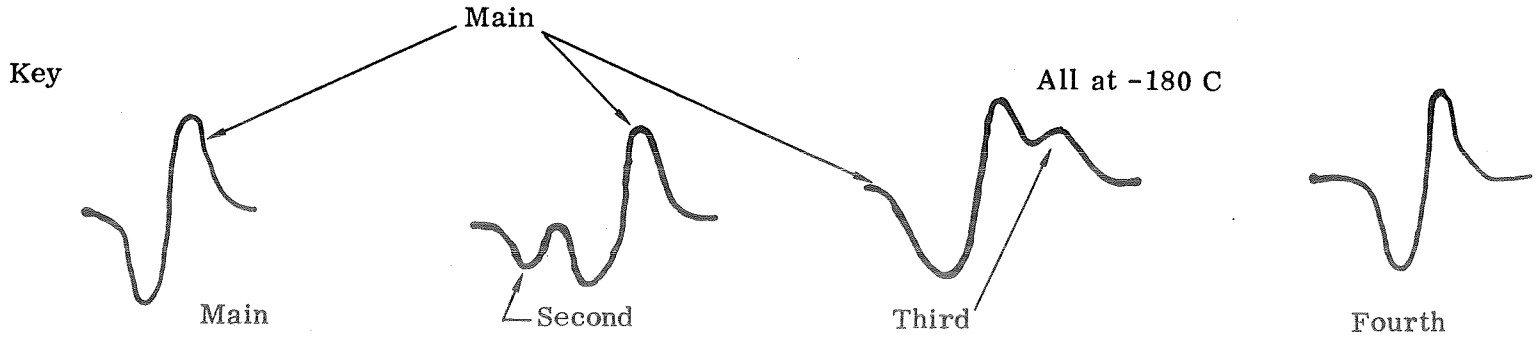


Figure G-18.- Possible Impurity Structures and Oxidation States in S_iO_2

TABLE G-4
SIGNAL SUMMARY FOR $Si-SiO_2$ SYSTEM

	Silicon Dioxide on Powered Silicon (Boron, Phosphorus and Intrinsic)						Single Crystal Al on $Si O_2$	
	Wet	Dry	Na OH (Wet)	Na CI (Wet)	HF (Wet)	H_2 Bake (Wet)	Wet	Dry
Main	Yes	Yes	Yes	Yes	Yes	Yes	No	No
Second	Yes	No (except Na CI)	Yes	Yes	Yes	No	No	No
Third	No	No	No	No	No	Yes	No	No
Fourth	No	No	No	No	No	No	Yes	Yes



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APPENDIX H. THERMODYNAMIC ANALYSIS OF AMBIENT GAS EFFECTS

Introduction

Silicon device and integrated circuit technology, which represents one of the major areas of progress in electronics, depends heavily on the sophisticated use of highly specialized materials. The juxtaposition of such materials needed to produce the desired electronic function also often contains the seeds of long-term drift or deterioration of that very function. The mechanistic reasons for this frequenctly are unobvious because of the specialized nature of the materials and the intricate manner in which they are assembled. As a first step in anticipating such long-term interactions it should at least be determined which of them are thermodynamically permissible and which can be eliminated from further consideration. The present analysis attempts to do this for gaseous components that have been encountered by instrumental techniques, such as gas chromatography and mass spectrometry, in the packages of integrated circuits.

Gases considered were: nitrogen, hydrogen, argon, helium, methane, oxygen, water vapor, carbon dioxide, carbon monoxide, benzene, toluene, methylcyclohexane, and freon. Additional gases will be included as they are revealed by instrumental analysis.

Solid surfaces under examination were: silicon, silicon dioxide, aluminum, and aluminum oxide. Other surface compositions will be added in order of frequency and general reactivity.

Chemical reactions for the foregoing gases and solids were considered in terms of the simple thermodynamic free energy of reaction.

A literature survey concerned with integrated circuits and ambient gases is appended.

Free Energy Values

An important thermodynamic property is the free energy of reaction, for it is the magnitude and algebraic sign of this quantity which describes the chemical species which will exist under equilibrium conditions at a given temperature. Thus, the free energy of reaction or the change in free energy for a chemical reaction and its sign offers a means for the prediction that ambient gases will or will not chemically react with the solid surface materials present in packaged integrated circuits. With this connotation in mind Tables H-1 and H-2 summarize pertinent standard free energy values for temperatures, 298, 500 and 1000 K. The standard state is 298^{0} K at atmospheric pressure. For gases a correction must be made for fact that a real gas is not a perfect gas (Ref H-1). Furthermore, it is important to note that the standard free energy of formation of an element is, by definition, zero for the standard state. It is through application of an equation that the standard change in free energy is calculated for possible chemical reaction between ambient gases and solids in packaged integrated circuits.

TABLE H-1
THERMODYNAMIC VALUES FOR AMBIENT GASES [2] [3]

Gaseous Species	Standard Free Energy of Formation Kcal/Mole and ev					
	298°K	500°K	1000°K	298°K	500°K	1000°K
	Kcal/Mole			ev		
N_2, H_2, A, He, O_2	0	0	0	0	0	0
CH_4	-12.1	-7.8	+4.6	-0.53	-0.34	+0.20
HCl	-23.0	-24.0	-25.0	-1.00	-1.04	-1.09
H_2O	-54.6	-52.0	-46.0	-2.38	-2.26	-2.00
CO	-32.8	-37.1	-47.9	-1.43	-1.61	-2.08
CO_2	-94.3	-94.4	-94.6	-4.10	-4.11	-4.12
Benzene, C_6H_6	+31.0	+39.2	+62.3	+1.35	+1.71	+2.72
Toluene, C_7H_8	+29.3	+41.8	+76.3	+1.27	+1.82	+3.54
Methylcyclohexane, C_7H_{14}	+6.5	+37.5	+119.0	+0.28	+1.63	+5.18
CCl_2F_2	-102.7	-96.4	-81.2	-4.46	-4.19	-3.53
$Si\theta_2$(g)	-76.5	-76.8	-76.9	-3.33	-3.34	-3.35
SiO(g)	-27.9	-30.1	-42.2	-1.21	-1.31	-1.83
SiH_4	+13.2	+17.3	+28.8	+0.58	+0.75	+1.25
AlC	+196.2	+186.9	+164.5	+8.54	+8.14	+7.17
AlH	+55.0	+50.6	+40.6	+2.39	+2.20	+1.77
$SiCl_4$	-132.0	-128.0	-108.0	-5.75	-5.56	-4.70
SiF_4	-360.0	-356.0	-340.0	-15.70	-15.50	-14.80

TABLE H-2
THERMODYNAMIC VALUES FOR AMBIENT SOLIDS [2][3][4]

Solid Species	Standard Free Energy of Formation Kcal/Mole and ev					
	298°K	500°K	1000°K	298°K	500°K	1000°K
	Kcal/Mole			ev		
SiO_2	-204.6	-186.0	-164.0	-8.99	-7.80	-7.12
Al_2O_3	-378.1	-362.9	-325.3	-16.49	-15.80	-14.16
Si_3N_4	-36.0	-56.0	-100.0	-1.57	-2.44	-4.35
AlN	-68.6	-63.5	-50.5	-2.99	-2.77	-2.20
SiC	-20.1	-19.7	-18.8	-0.88	-0.86	-0.82
$AlCl_3$	-150.7	-138.8	-110.3	-6.55	-6.04	-4.80
AlF_3	-337.4	-324.6	-293.9	-14.69	-14.11	-12.75

Conclusions

The results of free energy calculations are summarized in Table H-3. The data predict for the indicated ambient gas-solid surfaces in contact, at the indicated temperatures, chemical reactions in all cases where the standard free energies are negative. These are the reactions between solid silicon and oxygen gas, solid silicon and carbon monoxide or carbon dioxide, gaseous benzene and solid silicon to form silicon carbide and hydride, toluene vapors and solid silicon to form the carbide or hydride, and CF_2Cl_2 and silicon to form silicon fluoride, silicon chloride and carbon.

Silicon dioxide solid is very stable and much less reactive than silicon. Free energy calculations for solid silicon dioxide with ambient gases were negative in only one instance, i.e., the chemical reaction with difluoro-dichloro-methane.

Aluminum metal is a common component in integrated circuit technology. Accordingly, simple standard free energies of reaction were calculated for solid aluminum-ambient gas systems. These thermodynamic data disclosed that the formation of aluminum nitride solid, aluminum oxide solid, (from both water vapor and oxygen, as well as carbon monoxide and dioxide), are probable reactions which occur between ambient gases and solids in packaged integrated circuits. As in the case of silicon metal and silica, the freon, dichloro-difluoro-methane, reacts with aluminum to form halide salts and carbon.

Aluminum oxide, solid, showed no chemical reactivity with any of the ambient gases commonly found in circuit packages.

A few general statements can be made concerning the calculated data in Table H-3.

1. Only chemical reactions between ambient gases and solids most commonly used in packaged integrated circuits were considered. Other materials can be included.

2. Free energy calculations for methylcyclohexane reactions are not shown as the results show that these reactions are less favorable than those of benzene and toluene.

3. No limits of error were associated with thermodynamic values used as they were not available in many cases.

4. The predictions made concerning ambient gas-solid chemical reactions are for the equilibrium condition. The kinetic picture can be quite different. For example, the kinetic removal of one chemical product from the reaction at equilibrium can cause a complete shift in the equilibrium to form more of the reaction products. During this shifting condition the processes may be steady state and are kinetic in nature until the new equilibrium is achieved.

5. Only over-all chemical reactions were considered. The participation of potential chemical intermediates and/or activated states was omitted from consideration.

6. Reaction of hydrogen with Si, SiO_2, Al and Al_2O_3 is thermodynamically disallowed.

TABLE H-3

CHEMICAL REACTIONS FOR PROCESS INTRODUCED AMBIENT GASES AT GAS-SOLID INTERFACES IN PACKAGED INTEGRATED CIRCUITS

Reaction, Solid Silicon Ambient Gas	Free Energy of Reaction 298°K	500 °K	1000°K	Favored
	Kcal/Mole			
(1) $Si_{(s)} + 2H_{2(g)} \rightleftarrows SiH_{4(g)}$	+13.2	+17.3	+28.8	No
(2) $Si_{(s)} + O_{2(g)} \rightleftarrows SiO_{2(s)}$	-204.6	-186.5	-164.0	Strongly
(3) $2Si_{(s)} + O_{2(g)} \rightleftarrows 2SiO_{(g)}$	-27.9	-30.1	-42.2	Yes
(4) $Si_{(s)} + CH_{4(g)} \rightleftarrows SiH_{4(g)} + C_{(s)}$	+25.3	+25.1	+8.6	No
(5) $Si_{(s)} + H_2O_{(g)} \rightleftarrows SiO_{(g)} + H_{2(g)}$	+26.7	+21.6	+3.8	No
(6) $Si_{(s)} + SiO_{2(s)} \rightleftarrows 2SiO_{(g)}$	+148.8	+115.8	+79.6	No
(7) $Si_{(s)} + 2CO_{(g)} \rightleftarrows SiO_{2(s)} + 2C_{(g)}$	-139.0	-111.8	-63.2	Yes
(8) $Si_{(s)} + 2CO_{(g)} \rightleftarrows 2SiC_{(s)} + O_{2(g)}$	+25.4	+34.8	+58.2	No
(9) $Si_{(s)} + CO_{2(g)} \rightleftarrows SiO_{2(g)} + C_{(s)}$	-110.3	-91.6	-69.5	Yes
(10) $2Si_{(s)} + 2CO_{2(g)} \rightleftarrows 2SiC_{(s)} + 2O_{2(g)}$	+148.4	+149.4	+151.6	No
(11) $6Si_{(s)} + C_6H_{6(g)} \rightleftarrows 6SiC_{(s)} + 3H_{2(g)}$	-151.6	-157.4	-177.1	Yes
(12) $Si_{(s)} + C_6H_{6(g)} \rightleftarrows SiH_{4(g)} + 6C_{(s)} + H_{2(g)}$	-17.8	-21.9	-33.5	Yes
(13) $7Si_{(s)} + C_7H_{8(g)} \rightleftarrows 7SiC_{(s)} + 4H_{2(g)}$	-170.0	-179.7	-207.9	Strongly
(14) $Si_{(s)} + C_7H_{8(g)} \rightleftarrows SiH_{4(g)} + 7C_{(s)} + 2H_{2(g)}$	-16.1	-24.5	-47.5	Yes
(15) $2Si_{(s)} + 2CCl_2F_{2(g)} \rightleftarrows SiCl_{4(s)} + SiF_{4(s)} + 2C_{(s)}$	-286.6	-291.2	-285.6	Strongly

TABLE H-3 (Continued)

Reaction, Solid Silicon Ambient Gas	Free Energy of Reaction 298°K	500°K	1000°K (Kcal/Mole)	Favored
(16) $3Si_{(s)}+2N_{2(g)} \rightleftarrows Si_3N_{4(s)}$	-82.0	-104.0	-150.0	Yes
(17) $SiO_{2(s)}+2H_{2(g)} \rightleftarrows SiH_{4(g)}+O_{2(g)}$	+217.8	+203.3	+192.8	No
(18) $SiO_{2(s)}+CH_{4(g)} \rightleftarrows SiH_{4(g)}+CO_{2(g)}$	+229.9	+211.1	+188.2	No
(19) $SiO_{2(s)}+2H_2O_{(g)} \rightleftarrows SiH_{4(g)}+2O_{2(g)}$	+327.0	+301.3	+285.0	No
(20) $2SiO_{2(s)}+2CO_{(g)} \rightleftarrows 2SiC_{(g)}+3O_{2(g)}$	+434.6	+406.8	+386.6	No
(21) $SiO_{2(s)}+CO_{2(g)} \rightleftarrows SiC_{(s)}+2O_{2(g)}$	+278.8	+260.7	+240.0	No
(22) $6SiO_{2(s)}+C_6H_{6(g)} \rightleftarrows 6SiC_{(s)}+3H_2O_{(g)}+9O_{2(g)}$	+880.9	+802.6	+670.9	No
(23) $7SiO_{2(s)}+C_7H_{8(g)} \rightleftarrows 7SiC_{(s)}+4H_2O_{(g)}+5O_{2(g)}$	+1044.4	+914.3	+760.2	No
(24) $2SiO_{2(s)}+2CCl_2F_{2(g)} \rightleftarrows SiCl_{4(s)}+SiF_{4(g)}+2CO_{2(g)}$	-66.0	-104.0	-131.8	Yes
(25) $3SiO_{2(s)}+2N_{2(g)} \rightleftarrows Si_3N_{4(s)}+3O_{2(g)}$	+577.8	+502.0	+392.0	No
Solid Aluminum-Ambient Gas				
(26) $Al_{(s)}+1/2N_{2(g)} \rightleftarrows AlN_{(s)}$	-68.6	-63.5	-50.6	Yes
(27) $Al_{(s)}+1/2H_{2(g)} \rightleftarrows AlH_{(g)}$	+55.0	+50.6	+40.6	No
(28) $2Al_{(s)}+3/2O_{2(g)} \rightleftarrows Al_2O_{3(s)}$	-378.1	-362.9	-325.3	Strongly
(29) $Al_{(s)}+CH_{4(g)} \rightleftarrows AlC_{(g)}+2H_{2(g)}$	+208.3	+194.7	+159.9	No

TABLE H-3 (Concluded)

Solid Aluminum-Ambient Gas	Free Energy of Reaction 298°K	500°K	1000°K	Favored
	Kcal / Mole			
(30) $4Al_{(s)}+CH_{4(g)} \rightleftarrows 4AlH_{(g)}+C_{(s)}$	+232.1	+210.2	+157.8	No
(31) $2Al_{(s)}+3H_2O_{(g)} \rightleftarrows Al_2O_{3(s)}+3H_{2(g)}$	-214.3	-206.9	-187.3	Yes
(32) $2Al_{(s)}+3CO_{(g)} \rightleftarrows Al_2O_{3(g)}+3C_{(s)}$	-279.7	-251.6	-181.6	Yes
(33) $6Al_{(s)}+C_6H_6 \rightleftarrows 6AlC_{(g)}+3H_{2(g)}$	+1146.2	+1082.3	+924.7	No
(34) $4Al_{(s)}+3CO_{2(g)} \rightleftarrows 2Al_2O_{3(g)}+3C_{(s)}$	-473.3	-442.6	-366.8	Strongly
(35) $8Al_{(s)}+C_7H_{8(g)} \rightleftarrows 8AlH_{(g)}+7C_{(s)}$	+410.7	+363.0	+248.5	No
(36) $4Al_{(s)}+3CCl_2F_{2(g)} \rightleftarrows 3C_{(s)}+2AlCl_{3(s)}+2AlF_{3(s)}$	-668.1	-637.6	-564.8	Strongly
(37) $Al_2O_3+N_{2(g)} \rightleftarrows 2AlN_{(s)}+3/2O_{2(g)}$	+240.9	+235.9	+224.1	No
(38) $Al_2O_{3(s)}+H_{2(g)} \rightleftarrows 2AlH_{(g)}+3/2O_{2(g)}$	+488.1	+464.1	+406.5	No
(39) $Al_2O_{3(s)}+2CH_{4(g)} \rightleftarrows 2AlC_{(g)}+3H_2O_{(g)}+H_{2(g)}$	+625.9	+596.3	+501.1	No
(40) $Al_2O_{3(s)}+H_2O_{(g)} \rightleftarrows 2AlH_{(g)}+2O_{2(g)}$	+542.7	+528.1	+452.5	No
(41) $1/2Al_2O_{3(s)}+CO_{(g)} \rightleftarrows AlC_{(g)}+5/2O_{2(g)}$	+418.0	+407.9	+375.1	No
(42) $3Al_2O_{3(s)}+C_6H_{6(g)} \rightleftarrows 6AlC_{(g)}+3H_2O_{(g)}+3O_{2(g)}$	+2116.7	+2013.9	+1766.6	No
(43) $2Al_2O_{3(s)}+C_7H_{8(g)} \rightleftarrows 4AlC_{(g)}+3CO_{(g)}+3H_2O_{(g)}+H_{2(g)}$	+1237.5	+1174.5	+628.0	No
(44) $7Al_2O_{3(s)}+6CO_2F_{2(g)} \rightleftarrows 6AlC_{(g)}+4AlCl_{3(g)}+4AlF_{3(g)}+21O_{2(g)}$	+1253.9	+1164.4	+1067.3	No
(45) $2Al_2O_{3(s)}+3Si_{(s)} \rightleftarrows 4Al_{(s)}+3SiO_{2(s)}$	+142.4	+168.8	+156.6	No

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H-2. Stull, D. R., Proj. Director, Janaf Thermochemical Tables, Advanced Research Projects Agency Program. US Air Force Contract No. AF04(611)7554 Dow Chemical Co., Midland, Michigan.

H-3. Glasser, A., "A Survey of the Free Energies of Formation of the Fluorides, Chlorides and Oxides of the Elements to 2500°K", ANL-5107, August 1953.

H-4. Chu, T. L., Lee, C. H., and Gruber, G. A., J. Electrochem. Soc., Solid State. 114, No. 7, 717-722 (1967).

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H-2. Leiby, C. C. and Chen, C. L., "Diffusion Coefficients, Solubilities and Permeabilities for He, Ne, H_2 and N_2 in Vycor Glass". J. Appl. Phys., 31, 268 (1960).

In 96% silicon dioxide glass (vycor) helium diffusion rate is higher than in pure silicon dioxide glass, but is lower in most other glasses. The higher diffusion rate in vycor is probably due to the method of fabrication leading to greater porosity.

H-3. Mouison, A. J., Roberts, J. P., "Water in Silica Glass", Trans. Brit. Ceram. Soc., 59, 388-399 (1960), Trans. Faraday Soc., 59, 1208-1216 (1961).

Diffusion measured by IR absorption at 2.7 microns. Some question as to whether water or hydroxyl is diffusing species.

H-4. Zaininger, K. H., Warfield, G., "Hydrogen Induced Surface States at a Si-SiO_2 Interface", Proc. IEEE, 52, 972-973, August (1964).

Hydrogen increases the inversion layer capacitance upon contact with an MOS structure at high temperature.

H-5. Haas, C. "The Diffusion of Oxygen Into Silicon," J. Phys. Chem. Solids 15, 108-111, August (1960).

Assumption is made that internal friction and diffusion, or both, due to the same relaxation phenomenon. The diffusion coefficient for oxygen in silicon is calculated from experimental data on internal friction. Diffusion constant: 0.21 cm^2/sec, energy of activation: 2.44 electron volts.

H-6. Logan, R. A. and Peter, A. J., "Diffusion of Oxygen in Silicon". J. Appl. Phys. 28, 819-820, July 19 (1957).

Experimental results on oxygen diffusion coefficient in silicon support Haas.

H-7. Frosch, C. J. and Derick, L. "Diffusion Control in Silicon by Carrier Gas Composition". J. Electro-Chem. Soc. 105, 695-699, December (1958).

Antimony tetroxide at 950°C, one hour diffusion at 1200°C produces a junction 1.5 microns deep in a 5 ohm-cm p-type silicon. The surface concentration depends upon the quantity of water vapor in the nitrogen flow gas, from 3.3×10^{19} atoms/cm^{-3} for dry nitrogen to 8×10^{17} atoms/cm^3 for nitrogen bubbled through water at 70°C.

H-8. Thompson, C. "The Effects of Ambients on Performance of CdS Thin Film Transistors". Science Abstracts B. Electrical Engineering 68, 11389 (1965); Japan J. Appl. Phys. 4, No. 3, 207-211 March (1965).

Describes the operating mechanisms of the thin film CdS transistor at several pertinent temperatures and ambients. The effects of the ambients are correlated to device parameters with further implications.

H-9. Lehman, H. S., "Chemical and Ambient Effects on Surface Conduction in Passivated Silicon Semiconductors". Science Abstracts B. Electrical Engineering 68, 9843 (1965); IBM J. Res. and Development (USA) 8, No. 4, 422-426 September (1964).

The effect of processing variables on the surface conduction properties of passivated silicon junction devices has been studied. Insulated gate field effect transistors fabricated in p-type silicon were used as an experimental tool. Varying the metal used as the gate electrode is shown to strongly influence the surface conductivity of the field effect device. The effects of heat treatment in various ambients and variation in the insulators used are also discussed. Surface conduction is shown to be a complex function of materials thermal history and processing.

H-10. Brattain, V. H. and Garrett, C. G. "Protection of Silicon Conductive Devices by Gaseous Ambients". (Bell Telephone Lab.) US Pat. No. 2,777,974, January 15, 1957.

The use of ambient atmosphere of oxygen to control the surface characteristics of junction devices by preventing or inhibiting the formation of undesirable conducting paths (channels) at or near the surfaces of these devices is discussed. The effects of the oxygen is to form a layer of p-type material on the surface of the crystal which prevents the formation of n-type channels on the p-type region.

H-11. Many, A. and Gerlick, D. "The Effect of Gaseous Ambients on the Interface Structure of Germanium. (Hebrew Univ.) Recent news abstracts of the Electrochem. Soc., Semiconductor Symposium, May (1957).

Simultaneous measurements of surface recombination velocity and trapped charge density in the fast state as a function of surface potential were reported. The surface potential was varied over a wide range by the application of large AC fields normal to the surface. It was found that the distribution and characteristics of the fast state were markedly affected by the surrounding ambients. Initially with the sample in vacuum, rapid changes in interface structure took place. After a few days stabilization was essentially reached. Following repeated exposures to the different ambients reproducible changes resulted which presisted for many weeks.

H-12. Jauffe, K. "Gas Reaction on Semiconducting Surfaces and Space Charge Boundary Layers". Semiconductor Surface Physics, Univ. of Pennsylvania Press, 259-282 (1957).

The Fermi potential of a catalyst is related to the electronic exhange level of the reacting molecules. Applying a three dimensional term scheme the relations are generalized. On the basis of results one can determine whether an n- or p-type catalyst must be used for a reaction. Furthermore, the important rule of the space charge in the catalyst is discussed with its effect upon the reaction kinetics.

H-13. Stattz, H., DeMars, G. A., Davis, L. Jr., Adams, A. Jr., (Raytheon Manufacturing Co.) Semiconductor Surface Physics (University of Pennsylvania Press) 139-168 (1957).

Steady state and nonsteady state inversion layer conductance on silicon and germanium are discussed in terms of two types of surface states. The second type state is located at the surface of the oxide with perhaps some states in the oxide film. The states result mainly from adsorbed gas molecules. Depending upon the surrounding gas they are either predominantly acceptor or donor type and it is principally the states which determine the directions in which the bands at the surface are bent. It is possible to determine the number and energy of the interface states from nonsteady state inversion layer conductance measurement. It is found that high fields across the oxide film can influence the density of these states in silicon lying above the middle of the gap. Anomalous inversion layer conductances are found when vapors of certain liquids are adsorbed.

H-14. Kozlouskaya, V. M. "Mass Spectrometric Determination of the Amount and Composition of Gases Adsorbed on the Surface of Germanium and Silicon Monocrystals". Solid State Abstract 1, 6046 (1960-1961); Soviet Phys., Solid State 1, 940-946 January (1960).

H-15. Gleason, F. R., Greiner, J. H. and Yetter, L. R. "Gas Absorption by Vacuum Evaporated Magnetic Films". Solid State Abstract 1, 6149 (1960-1961); (IBM) Vacuum 9, 301 November (1959).

Mass spectrometric determination of the types and amounts of gases absorbed during the deposition of vacuum evaporated thin films were reported. Most of the gases came from the oil pump. The absorbed gas molecules per metal atom degassed was independent of film thickness, indicating that the gas is trapped in the film structure as well as on the surface.

H-16. Kammere, H. C., "Thermal Evaluation of High Density Electronic Packages". Solid State Abstract 3, 16912 (1962) Electron Design 9, 121-122 December (1961).

A monograph to determine the design limitation of microminiature packages exposed to thermal stress. Five basic parameters investigated were: total temperature between ambient environment and the center of the package, thermal conductivity of package material, cooling technique and size and configuration of maximum.

H-17. Kislev, A. U. and Lygin, V. I. "University of Moscow". Solid State Abstract 5, 28828 (1964); Surface Science 2, 236-244 (1964).

The shift of the absorption band of silica surface hydroxyl groups on adsorption of molecules of different electronic structures is in accordance with their heats of adsorption and ionization potentials. On the basis of vibrational theory the spectra of water and ammonia molecules adsorbed on silica and zeolites have been analyzed.

H-18. Boutin, H. and Prask, H. "Study of Water Vapor Absorption on Gamma Alumina and Silica by Slow Neutron Inelastic Scattering". Solid State Abstract 5, 28830 (1964); Surface Science 2, 261-266 (1964).

The energy spectrum of neutrons, inelastically scattered by hydrogenous groups adsorbed on the solid surface is able to provide information concerning the degree of mobility of those groups, the nature and strength of the binding with the adsorbent and the frequencies of rotational or vibrational motions ranging from 20 to 1,000 cm^{-1}. The principle of the technique is given and is applied to water adsorbed on silica and gamma alumina after the samples have been heated to a 150° under vacuum. Two types of water molecules exist on the surface: distorted molecules with hydroxyl groups hydrogen-bonded to oxygen atoms, and tetrahedral molecules similar to the liquid. Additional water layers on the surface become more water-like.

H-19. Vokenstein, F. F. and Karpenke, I. V. "Theory of Photoadsorptive Effect in Semiconductors". Solid State Abstract 5, 30709 (1964); STAR 2, 3457A December (1964) AD605733.

The sign of the photo-adsorptive effect in semiconductors depends on selection of the system, on the mode of experiment and the preparation of the sample for experiment. Report offers formulas for establishing basic criteria for determination of the photo-adsorption effect.

H-20. Farnsworth, H. E. and Campbell, B. D. (Brown University) "Study of the Surface Properties of Atomically Clean Metal and Semiconductors". Solid State Abstract 6, 37205 (1966); Contract DA28304 ANC 0029E US Government Research and Development Reports 40, 146A May 20, (1965) AD 31-699.

Oxygen adsorption on the (0001) matte surface was enhanced when an intense light was incident on the crystal. A 3-5 Torr-min oxygen exposure in intense light extinguished the diffraction pattern whereas a 759 Torr-min exposure in the dark had little effect upon the pattern, but did cause a slight decrease in conductivity of the surface. Ion bombardment increased the dark conductivity and greatly decreased the effect of intense light. Photo-adsorption of oxygen is indicated. Unlike matte surface (0001) specular surface was not effected by exposure to light.

H-21. Hobson, J. P. "A New Method for Finding Heterogeneous Energy Distributions from Physical Adsorption Isotherms". Solid State Abstracts 6, 41617 (1966); Canadian J. Phys. 4, 1934 November (1965).

A model is described which assumes that a hetergeneous surface has a distribution of adsorption energies for physical adsorption. A new solution is presented giving a number of step types: local isotherms, which are chosen to represent varying degrees of adsorbate-adsorbate interaction. The solution permits energy distributions to be obtained quite simply from isotherm data at one temperature. This solution may be used to calculate isotherms at other temperatures.

H-22. Howling, D. H. "Photoelectric Response of Metal Surfaces in Ambient Atmospheres". Solid State Abstract 7, 48029 (1967); J. Appl. Phys. 37, 1844 (1966).

Experiments are described which examine variations in the photoelectric response of metal surfaces immersed in gas atmospheres. Work function changes have been produced by gas bombardment, electrode heating, deposition of small amounts of K on the surface. By operating the electrode under study as the cathode of geiger muller photon counter, photocurrents as low as 10^{-21} A could be measured. Factors which influence irreversible changes in work functions have been explored. A less well known increase in work function which is thermally activated has been demonstrated. Systems included were: tungsten/hydrogen, nickel/hydrogen, iron/hydrogen, platinum/hydrogen, paladium/hydrogen, rhenium/hydrogen; also nitrogen, neon, argon and ammonia.

H-23. Logan, R. M. and Stickney, R. E., "Simple Classical Model for the Scattering of Gas Atoms from a Solid Surface". Solid State Abstract 7, 46668 (1967); J. Chem. Phys. 44, 195 (1966).

A simple classical model for the scattering of gas atoms from a solid surface is proposed and its characteristics discussed. Results are obtained for the angular distribution of scattered particles. The model correctly predicts the general appearance of the scattering pattern, and its dependence upon the angle of incidence of the beam and on the temperature and masses of the gas and surface atoms.

H-24. Lu, Wei-Kao, "The General Rate Equation for Gas Solid Reaction in Metallurgical Processes with the Restrictions of Reversibility of Chemical Reaction and Gaseous Equimolar Counter-Diffusion". Solid State Abstract 7, 46669 (1967); AIME. Trans. 236, 531 (1965).

An improved general rate equation for a one dimensional gas-solid system has been derived. The concentrations of gaseous reactant and product have been calculated with relations furnished by the following constraints on the system: quasi-steady state and equimolar counter diffusion of gases. The interfacial chemical reaction is taken as 1st order with respect to the concentration of the gases involved. The equation has proper dependence on gas composition and on solid structure through the relative values of Knudsen and normal diffusivities.

H-25. Micheletti, F. B., and Mark, P., "Effects of Chemi-sorbed Oxygen on the Electrical Properties of Chemically Sprayed CdS Thin Films". Electronics and Communications Abstracts 6, 4467 (1967); Appl. Phys. Letters 10, No. 4, 136-138 (1967).

Measurements with spray deposited semiconducting CdS films are reported that demonstrate the primary effect of oxygen chemi-sorption is the reduction of hall mobility.

H-26. Blum, J., Warwick, R. and Genser, M. "Surface Studies with Silicon Planar Junction Structures". Presented at the Spring Meeting of the Electrochemical Society, Toronto, Canada, May 3-7 (1964) (Gen. Prec. Aerospace., Kearfott Div.)

Changes in: emitter current gain, beta, with collector current. Surface recombination velocity limits beta and is in turn determined by the density of fast interface states and the surface potential. Changes in characteristics of silicon npn planar transistors were observed after heating for various times at temperatures between 300-350°C in forming gas (15% H_2, 85% N_2), oxygen, vacuum and nitrogen.

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APPENDIX I. FAILURE ANALYSIS REPORTS

X-Radiography. - Components were examined for foreign particles, percent void area in the die to header bond and other anomalies. The void area data are given in Table I-1 and indicate an excess of 40 percent voids in 50 percent of the sample. Foreign particles were noted in seven devices using the Search-Ray. Typical findings are shown in Figures I-1 to I-3. Shake testing was performed simultaneously to determine particle mobility but no particle displacement was noted. Particles remained in position after cautious delidding.

Hermeticity. - The fine leak test (Veeco) revealed no failures per Autonetics procurement specification which requires a leak rate not to exceed 5.0×10^{-7}. All helium leak rates fell between 1×10^{-8} and 3×10^{-9}. However, 25 percent of the devices failed the gross leak test per specification using ethylene glycol at 150 C. These failures are identified in Table I-2.

Electrical parameters. - Electrical failures are listed in Table I-3. The parameters not meeting specifications are identified with an asterisk (*). The remaining devices performed according to specification.

Electrical dynamics. - Components were subjected to vibrational stress while observing electrical characteristics on a Tektronix 575 Curve Tracer. Eight components displayed an excessive forward voltage drop at high forward conductance (2 volts at 200 ma); one of these was intermittent. The components and failure modes are identified in Table I-4.

Optical examination. - Eight components were delidded for optical examination of surface anomalies. Evidences of tool damage, or other mishandling, prior to lidding resulting in damage to metallization on two devices are shown in Figures I-4 and I-5. The remaining devices were free of obvious anomalies except for No. 35 (Part No. 00995, Log No. 433) which had a detached post bond weld.

Metallurgical examination. - The eight components delidded for optical examination also were subjected to metallurgical sectioning and microscopy, revealing several previously unobvious anomalies. Partial post bonds are shown in Figures I-6 and I-7 with electrical contact constricted through intermetallic fragments. Figure I-8 shows approximately 60 percent of aluminum wire destroyed in welding and the presence of intermetallic formation at a base post bond. Cracks probably due to excessive deformation on an emitter pad bond are shown in Figure I-9. An interface between aluminum wire and aluminum pad is shown in Figure I-10; Figure I-11 indicates excessive wire deformation during welding and cracking from intermetallic formation. A partial base post bond with intermetallic formation is shown in Figure I-12. Each numbered figure represents a separate device identified by the caption.

Tensile strengths, Au/Al post bonds. - The metallographic anomalies enumerated above suggested the presence of a general bond reliability problem in this group of transistors. Accordingly, tensile strengths were measured on the post bonds of 25 delidded specimens using the test equipment shown in Figure I-13 at a pull angle of 45 degrees. Criteria of acceptance are defined in an Autonetics procurement specification which requires a minimum allowable breaking strength of 2.0 grams at

TABLE I-1
VOIDS OBSERVED BY X-RADIOGRAPHY IN SAMPLE CQF-101

Greater Than 40%	Part No.	Lot No.	% Voids in Bonding of Chip	Less Than 40%	Part No.	Lot No.	% Voids in Bonding of Chip
1	03750	437	27	2	03767	437	80
4	03749	435	30	3	03729	437	55
5	03748	435	25	6	03756	437	40
9	03742	435	20	7	03743	437	65
10	03711	437	15	8	03740	437	65
11	03703	435	15	13	03714	435	60
12	03747	435	30	14	03773	437	70
18	03681	435	20	15	03719	435	80
20	03698	435	20(FP)	16	03734	435	50(FP)
21	00125	433	25	17	03728	435	60
24	00153	433	15	19	03691	435	60
25	00156	439	20(FP)	22	00135	433	60
27	00285	439	30	23	00143	433	40
28	00399	433	20	26	00256	433	75
30	00542	436	20	29	00463	439	40
31	00556	436	30	33	00879	433	50(FP)
32	00821	433	25	39	00626	439	60
34	00943	433	30	41	00638	436	60
35	00995	433	30	42	00639	438	55
36	00032	433	25	43	00650	436	50
37	00617	436	25	44	00653	438	70
38	006260	436	30	46	00673	436	45
40	00630	438	35	49	00704	433	70
45	00666	438	20	50	00708	439	40
47	00675	438	30(FP)	54	00736	438	40
48	00686	433	30	56	00788	433	60
51	00727	436	20	59	01176	433	70
52	00731	438	30	60	01122	433	80
53	00732	438	20	61	01221	432	60
55	00738	439	25	63	01261	432	60
57	01002	439	20	67	01300	432	50(FP)
58	01065	439	30	71	02426	434	40
62	01222	432	20	74	02567	434	45
64	01262	432	30	75	02592	434	60
65	01282	432	15	77	05028	435	50
66	01291	432	30	78	05055	435	60
68	01310	432	20	79	05072	435	60
69	02259	434	30	81	05144	435	50
70	02322	434	20	82	05274	435	60(FP)
72	02458	434	20	83	05314	435	60
73	02475	434	20	84	05318	435	70
76	02620	434	35	85	03740	435	60
80	05079	435	20	86	03744	435	80
88	03739	435	20	87	03741	435	60
89	03750	435	30				

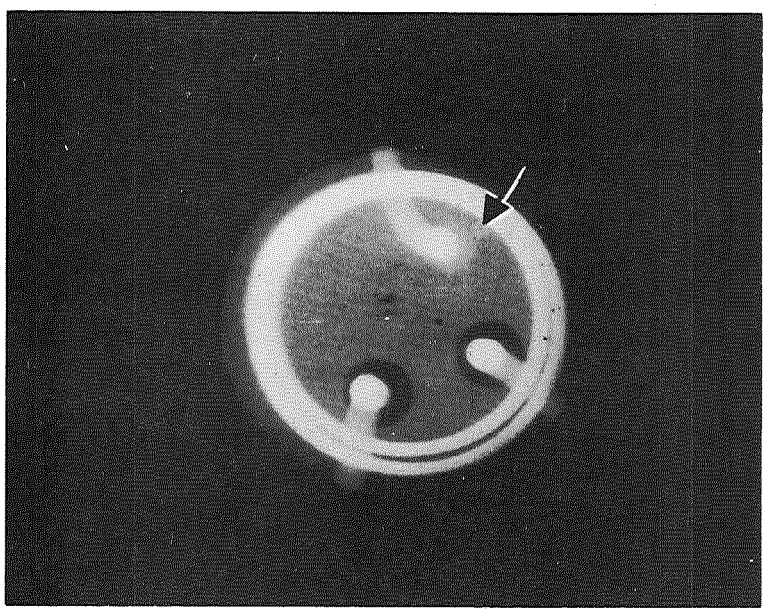

Figure I-1. Lot No. 435, Part No. 03698

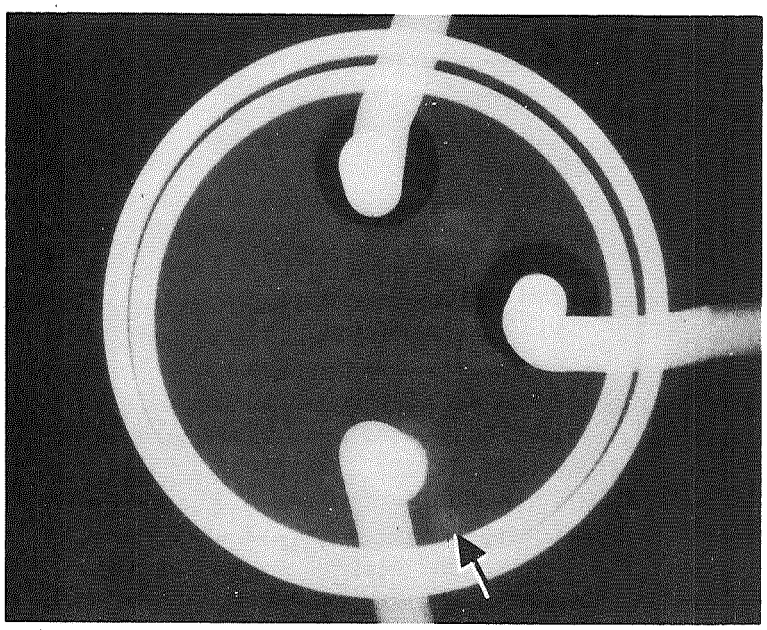

Figure I-2. - Part No. 03698, Lot No. 435

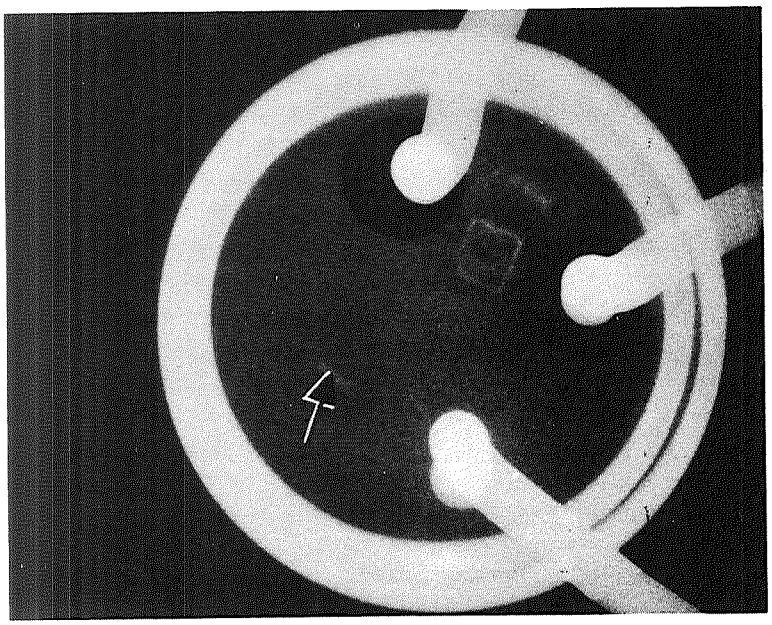

Figure I-3. - Part No. 00156, Lot No. 439

TABLE I-2
GROSS LEAK FAILURES

No.	Part No.	Lot No.
6	03756	437
8	03740	437
13	03714	435
14	03773	437
15	03719	435
18	03681	435
19	03691	435
20	03698	435
23	00143	433
26	00256	433
32	00821	433
34	00943	433
38	006260	436
43	00650	436
66	01291	432
67	01300	432
70	02322	434
74	02567	434
76	02620	434
82	05274	435

TABLE I-3
ELECTRICAL FAILURES

No.	Part No.	Lot No.	Parameter I_{CBO}	Parameter h_{FE}
1	03750	437		*
10	03711	437		*
13	03714	435		*
14	03773	437		*
19	03691	435		*
25	00156	439		*
29	00463	439		*
34	00943	433	*	*
41	00638	436		*
47	00675	438		*
61	001221	432		*
62	001222	432		*
75	02567	434		*
78	05055	435		*
81	05144	435		*
85	03740	435		* *

TABLE I-4
DYNAMIC ELECTRICAL FAILURES

No.	Part No.	Lot No.	High Forward Voltage Drop	Intermittents
5	03748	435	*	
8	03740	437	*	
13	03714	435	*	
35	00995	433	*	*
40	00630	438	*	
44	00653	438	*	
58	01065	439	*	
61	01221	432	*	

the bond edge (BE) and 3.0 grams for a complete bond (CB) failure. Obviously a BE rupture below 3.0 grams could mask a potential CB failure. The parent strength of the aluminum lead wire was 12-15 grams.

The results of these tests are given in Table I-5 with the mode of rupture identified in each case as BE or CB except where detached leads or zero pull strengths were encountered. The BE failures are ascribed to a possible excessive pinching during bonding resulting in reduction of wire cross section at the bond edges. The CB failures may have resulted from insufficient weld interface, granule formations or oxide contaminations at interfaces.

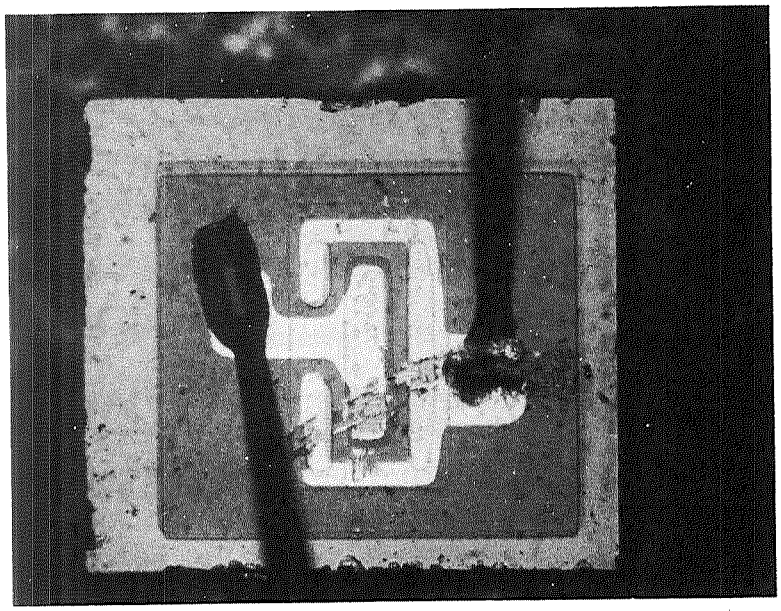

Figure I-4. Part No. 03748, Lot No. 435

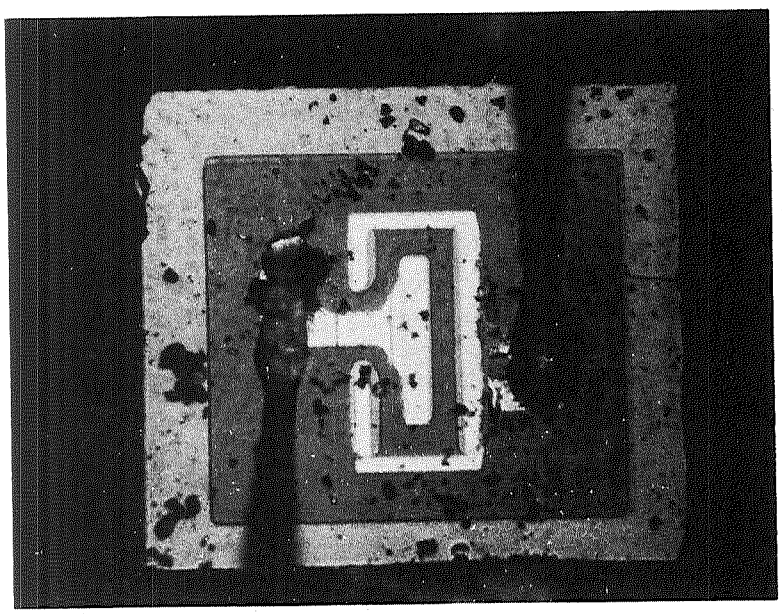

Figure I-5. Part No. 00653, Lot No. 438

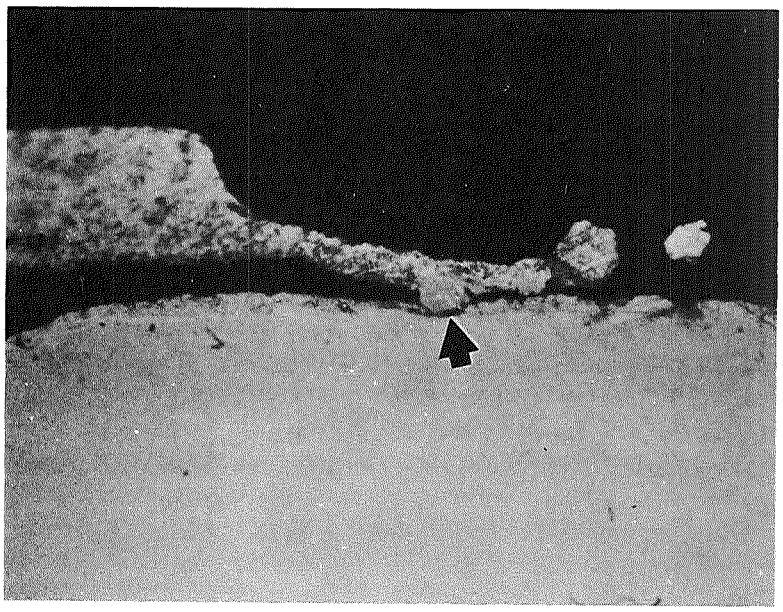

Figure I-6. - Part No. 03740, Lot No. 437

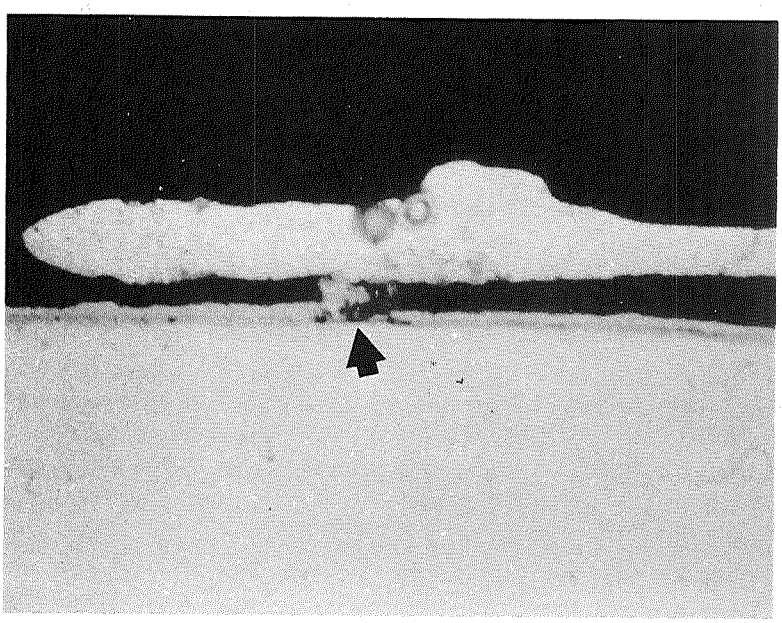

Figure I-7. - Part No. 03714, Lot No. 435

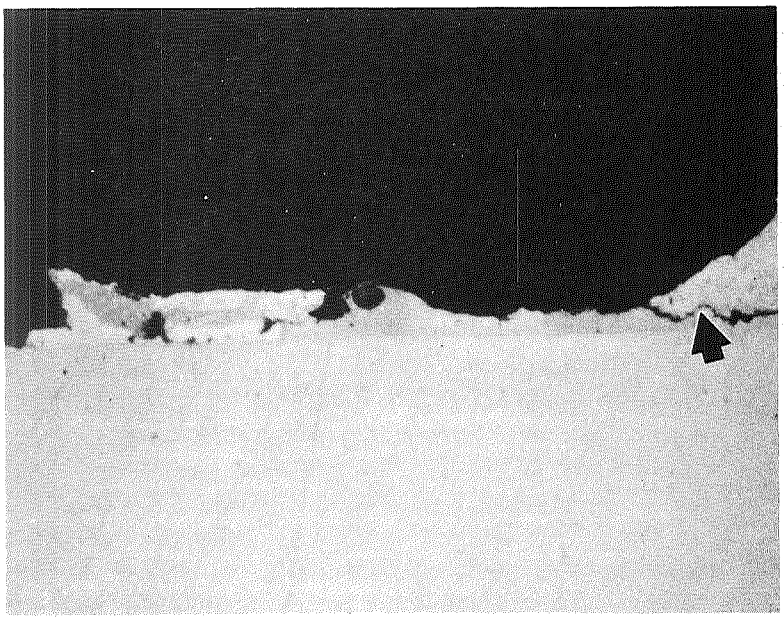

Figure I-8. - Part No. 00630, Lot No. 438

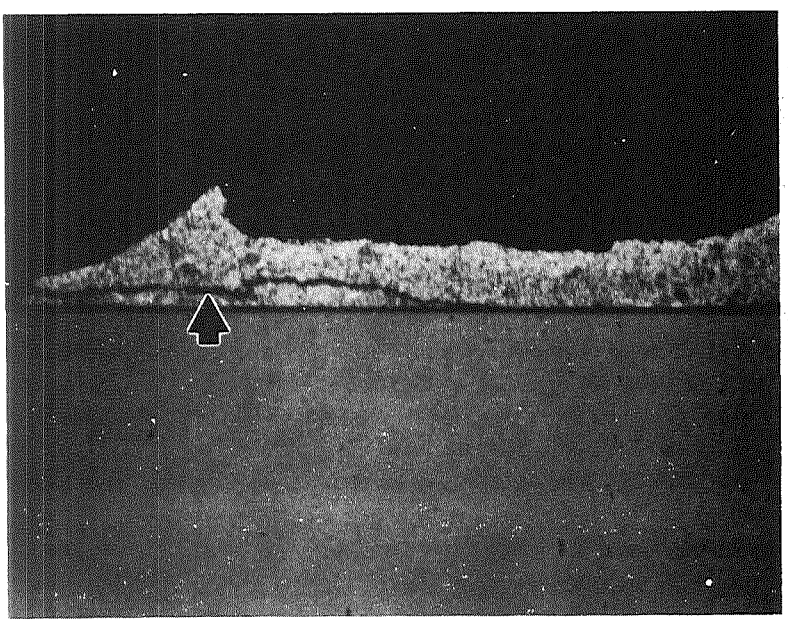

Figure I-9. - Part No. 00653, Lot No. 438

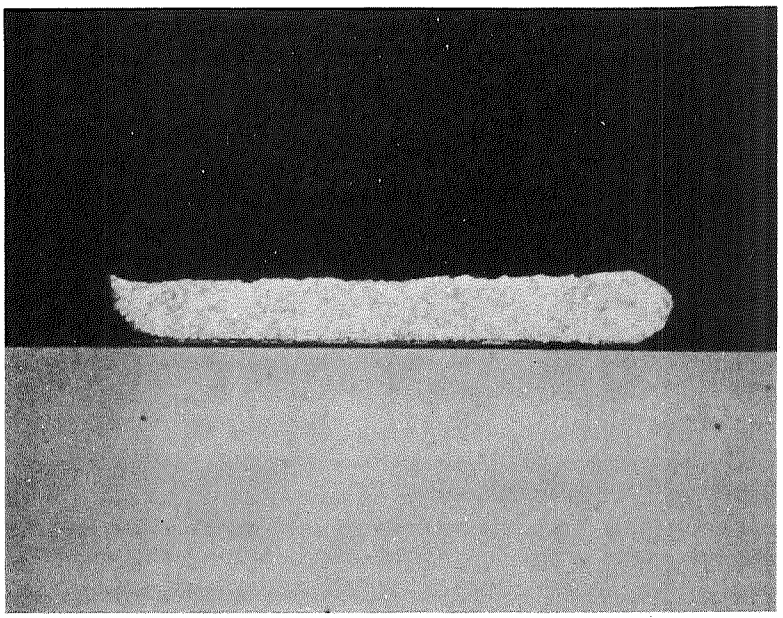

Figure I-10. - Part No. 01065, Lot No. 439

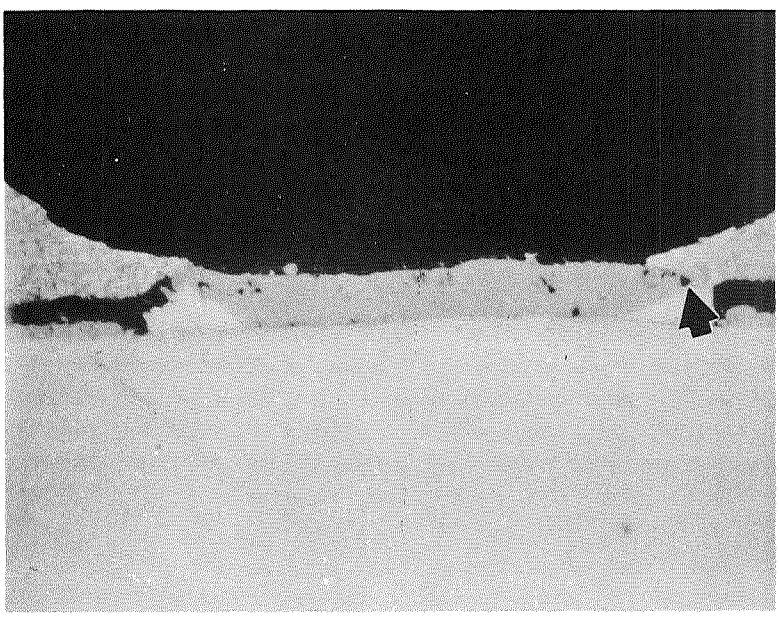

Figure I-11. - Part No. 01065, Lot No. 439

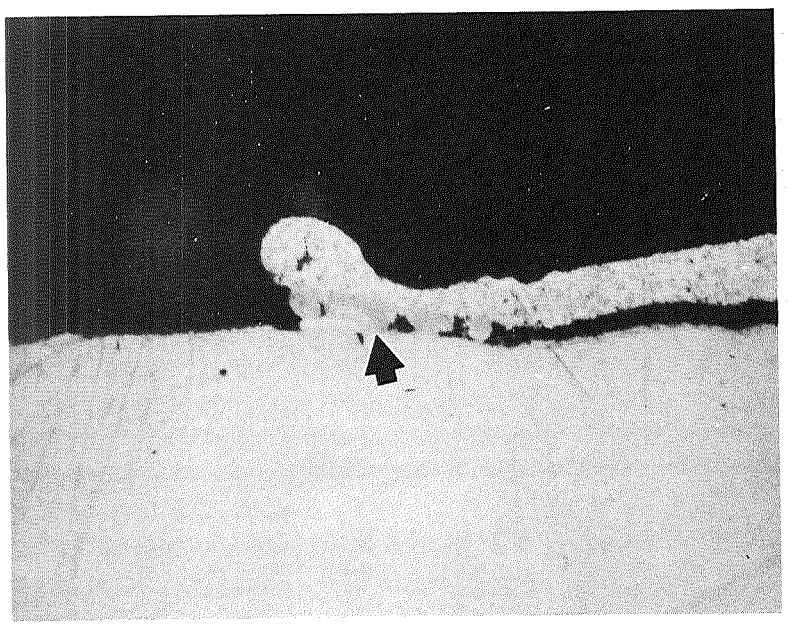

Figure I-12. - Part No. 01221, Lot No. 432

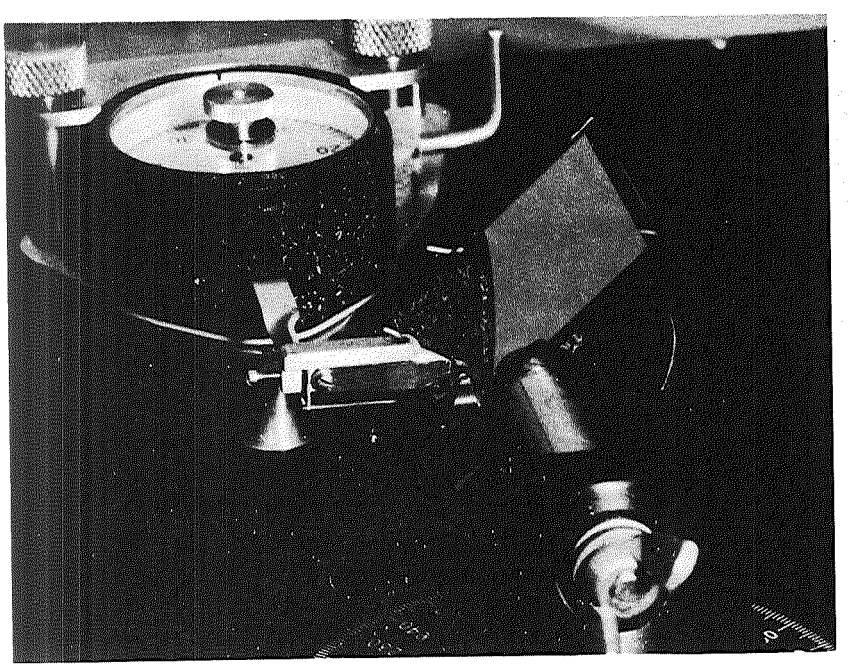

Figure I-13. - Lead Bond Tensile Tester

TABLE I-5
POST DATA YIELD STRENGTH DATA

No.	Part No.	Lot No.	Emitter Pull Strength (grams)	Mode of Failure	Base Pull Strength (grams)	Mode of Failure
63	01261	432	0	--	0	--
67	01300	432	1.7	BE*	2.0	BE
66	01291	432	3.3	CB*	2.0	CB*
70	02322	434	3.5	BE	1.7	CB*
89	03750	435	2.0	CB*	0	--
80	05079	435	3.5	CB	1.5	CB*
87	03741	435	2.6	BE	2.5	BE
62	01222	432	5.0	BE	3.7	BE
69	02259	434	3.2	CB	0	--
64	01262	432	3.7	BE	1.5	BE*
75	02592	434	3.5	CB	4.2	BE
79	05072	435	3.5	BE	5.3	CB
76	02620	434	1.0	CB*	1.3	CB*
74	02567	434	2.0	CB*	(detached)	--
68	01310	432	2.6	BE	3.3	BE
81	05144	435	4.0	BE	5.2	BE
86	03744	435	2.0	BE	2.0	CB*
83	05314	435	0	(detached)	0	--
78	05055	435	3.9	CB	0.5	CB*
65	01282	432	2.0	CB*	3.2	CB
85	03740	435	2.1	CB*	(detached)	--
77	05028	435	0	(detached)	3.5	CB
82	05274	435	2.0	BE	0	--
84	05318	435	3.0	BE	3.3	CB
88	03739	435	2.9	BE	4.1	BE

*Below specifications.

Tensile strengths, Al/Al pad bonds. - Ten devices were picked at random and delidded for investigation of the Al wire to Al pad ultrasonic bonds. Both the emitter and base pad bonds were tensile tested. These bonds were tested with the same equipment and at the same 45 deg angle as the post bonds. The results of these tests are listed in Table I-6. The average pull strength of these bonds is 2.2 grams which just exceeds the minimum per specification. Four of the ten devices are considered acceptable.

Moisture analysis of package ambient. - Moisture analyses were carried out on five devices mounted individually in a test holder designed specifically for the TO-18 package which was plumbed into the carrier gas system of a gas chromatograph. Sampling was accomplished by driving hollow pins through the case of the package and sweeping the ambient gas out of the package through one of the pins and into the instrument for analysis. Results obtained are presented in Table I-7.

TABLE I-6
PAD BOND YIELD STRENGTH DATA

No.	Part No.	Lot No.	Emitter Pull Strength (grams)	Mode of Failure	Base Pull Strength (grams)	Mode of Failure
15	03719	435	0	--	0	--
19	03691	435	2.6	BE	2.7	BE
18	03681	435	1.9	BE*	2.5	BE
14	03773	437	2.7	BE	0	--
23	00143	433	3.4	BE	2.8	BE
26	00256	433	3.1	BE	2.4*	CB
32	00821	433	0	--	3.0	BE
34	00943	433	2.1	BE	2.4	BE
38	00626	436	3.4	BE	4.2	BE
43	00650	436	5.1	BE	0	--

*Below specification.

TABLE I-7
MOISTURE CONTENT OF SELECTED DEVICES

Sample No.	Part No.	Lot No.	% Water by Weight	Absolute H_2O Content
11	03703	435	Lost	--
10	03711	437	85	1.51×10^{-4} grams
41	00638	436	77	1.29×10^{-5} grams
51	00727	436	53	2.0×10^{-5} grams
52	00731	438	88	1.47×10^{-5} grams

These moisture levels are considered to be intolerably high.

Package ambient analysis. - Analysis of package gas composition was performed on five TO-18 packages by gas chromatography using helium as a carrier gas. In view of the excessive moisture levels found in the five previous analyses, the water peak in this group also was estimated. All five devices had survived fine and gross leak tests and static and dynamic electrical tests. Chromatography was performed on a dual column system consisting of a 12 ft x 1/8 in. Poropak Q column and an 8 ft x 1/8 in. Molecular Sieve 5 A column. Conditions employed are as follows:

Columns	- Dual, Molecular Sieve 5 A, Poropak Q
Temperature	- 70°C
Carrier Gas	- Helium
Carrier Pressure	- 20 psi
Bridge Current	- 300 ma

The analytical results are given in Table I-8. These results indicate that the intended ambient was pure nitrogen. However, considerable contamination with oxygen is present, and the moisture levels are again excessive, in all cases exceeding the dew point of the contained gas. In view of this latter fact the moisture levels given in Table I-8 are split into gas phase content at 100 percent relative humidity (25 C) and liquid phase.

The gas ambient compositions in these devices appear to warrant investigation of their manufacture. The presence of oxygen suggests ineffective process control of lidding atmospheres. The presence of moisture is more difficult to explain (because the samples were hermetic) but may be due to incomplete curing of the Pyroceram prior to lidding.

Electron microprobe analysis of Al/Al bonds. After ambient analysis these devices were delidded and examined microscopically (optical) for corrosion. In spite of the excessive moisture no evidence of metal corrosion was found. Electron microprobe analysis of one of these specimens yielded no evidence of the presence of corrosive contaminants. Taken together these observations indicate that the manufacturer employs a clean process except for the anomalies noted in the previous paragraph.

In summary, this group of devices is characterized by several defective conditions which could impair long term electrical performance. These defects are: excessive voids in die-header bonds, gross leak failures, h_{FE} degradation, inferior post bonds and pad bonds and extreme moisture levels in packages. Other anomalous conditions are present to an extent of less than ten percent of the sample and do not necessarily portend serious reliability problems or indicate substandard control of process techniques. The manufacturer could avoid most of these problems by applying strict quality control measures.

TABLE I-8
GAS CONTENTS OF SELECTED DEVICES

Sample No.	Part No.	Lot No.	O_2% by Volume	N_2% by Volume	H_2O in Gas Phase	Gas Phase ppm H_2O (weight)	Excess H_2O Liquid
73	02475	434	42.7	54.4	1×10^{-6} gms	18000	3.2
71	02426	434	11.3	85.8	5×10^{-7} gms	18000	3.14
72	02458	434	5.1	92.0	4×10^{-7} gms	18000	2.84
45	00666	438	3.7	93.4	4×10^{-7} gms	18000	2.7
46	00673	436	11.5	85.6	2×10^{-7} gms	18000	2.8

Accuracy ± 5 Percent

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I-2. FAILURE ANALYSIS OF INTEGRATED CIRCUITS

Introduction

Sixty-five ITT integrated circuits were received by Autonetics for failure analysis as a portion of NASA Contract NAS 12-4.* These devices were rejected during breadboard fabrication of a system being built for NASA-ERC.

Conclusions

1. Thirty of the 58 devices had external package markings which incorrectly identified the pin numbers. This resulted in a 180° misorientation causing power to be applied incorrectly resulting in electrical overstress of several of the devices.

2. Inadequate vendor process control techniques were evident due to the high incidence of manufacturing defects noted during visual examination.

3. Package mechanical damage was induced during device system removal. This was indicated since 34 devices were gross leakers and several had broken external leads.

Procedure

The devices were analyzed using the procedure described below and summarized in Figure I-14.

1. All 58 devices were microscopically examined for external damage or anomalies.

2. All devices were subjected to a Z-axis orientation radiographic examination prior to electrical testing and delidding using a Norelco Be window 150 KV X-ray tube.

3. The devices were then subjected to a functional test involving a computerized sequential evaluation of approximately 30 electrical parameters using a Fairchild, type 4000 M, Integrated Circuit Tester.

4. Hermeticity tests were made on all devices utilizing a Veeco Model MX9AB Helium Leak Detector. All devices were pressurized in helium at 40 psi for 20 hours prior to testing. A standard gross leak "bubble test" was performed utilizing FC-43 Fluorocarbon Solvent heated to about 150°C.

5. The devices were then subjected to pin-to-pin electrical measurements using a Tektronics 575 Curve Tracer.

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*Letter to P. H. Eisenberg from Mike Emelianoff (NASA-ERC) dated December 2, 1968 regarding Failure Analysis of Integrated Circuits.

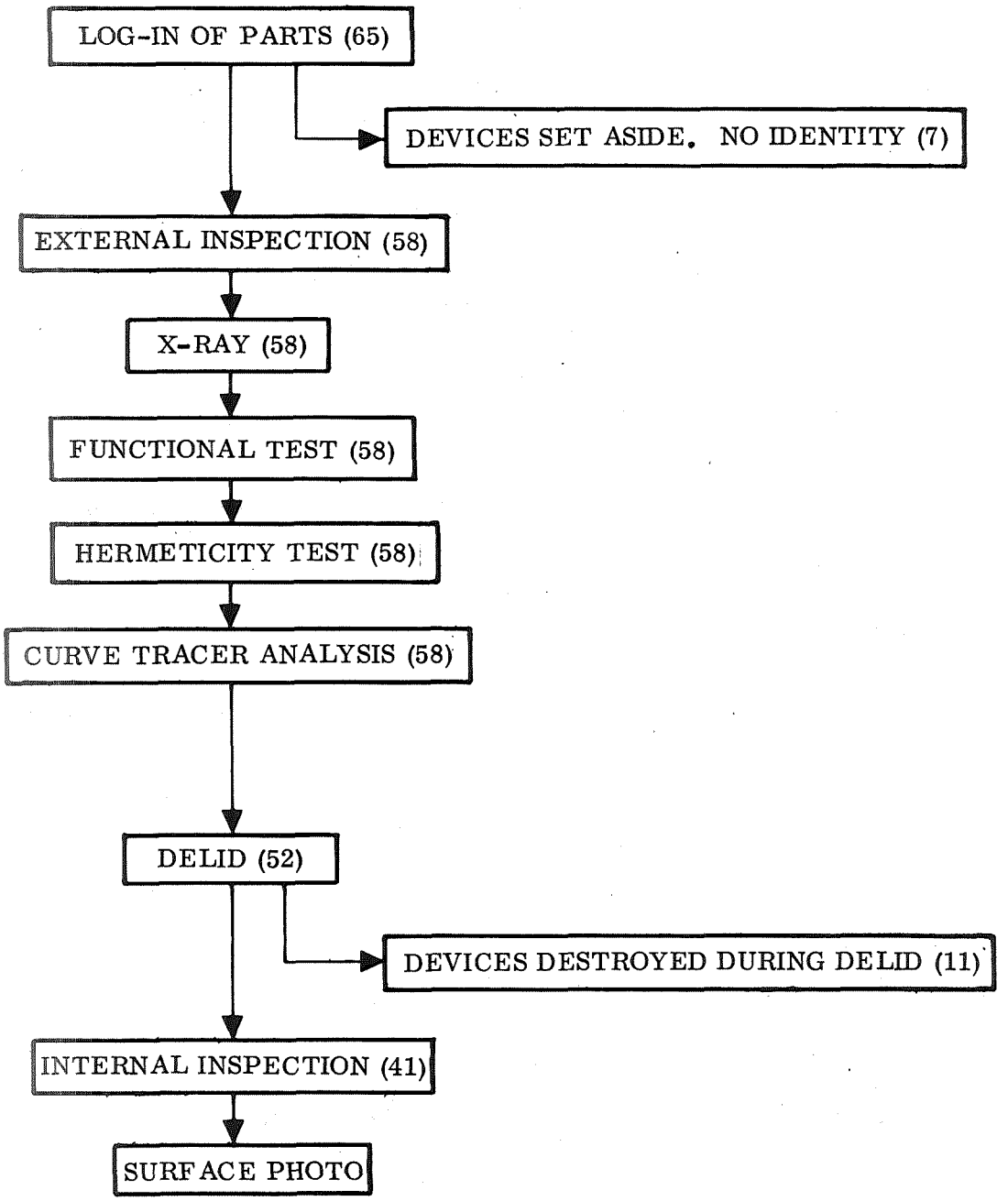

Figure I-14. Failure Analysis Flow Chart

6. The devices were delidded utilizing a special technique to minimize die surface contamination. The die surfaces were microscopically examined and abnormalities photographed on several devices.

Results

The test results obtained on each of the 58 devices analyzed are given in Table I-9. and summarized below:

1. External examination indicated that several of the devices contained broken or very short leads and other evidence of mishandling which probably occurred during removal from a system.

2. Radiographic examination revealed that an excess of Pyroceram was used for die mounting and package lid sealing in several devices (Figure I-15). Voids in the Pyroceram beneath the die were observed in some devices but were considered insignificant.

3. The functional and curve tracer electrical tests revealed that 30 devices were 180° reversed in the packages as indicated by the lid markings. Schematic diagrams of the devices were simultaneously studied while observing the oscilloscope presentation to aid in the interpretation. Specific circuit elements were identified and assigned as the failure cause where possible. An additional five devices were found to have degraded p-n junctions as indicated by "soft knees" and low breakdown voltages. The remainder of the devices (23) were electrically acceptable during retest.

4. Hermeticity tests indicated that 34 devices were gross leakers and one additional device had a leak rate greater than 5×10^{-8} atm-cc/sec. This confirmed that the devices were severely mishandled during removal from circuit boards.

5. Visual inspection of the devices following delidding revealed several abnormalities. (11 devices were destroyed during the delidding process.) Those devices previously determined to have mislabeled pin numbers by curve tracer analysis were verified by visual comparison of the metallization pattern and surface topology to the schematics. Other anomalies were observed in 14 devices including poor bond positioning (Figure I-16), poor trimming and alloyed metallization from electrical overstress (Figure I-17). Dual bonds were observed on the same pad in one device (Figure I-16). Metallization smearing and tool damage were present in other devices (Figure I-18).

TABLE I-9.
NASA IC FAILURE ANALYSIS

Manufacturer Part No.	Device	*Electrical Testing	Leak Rate atm-cc/sec He	Internal Inspection	Devices Returned to NASA	Remarks
9930 (1534)	126	RTOK	2.0×10^{-8}	No Defects Noted		Good Device
	384	180° Reversed	1×10^{-9}	No Defects Noted	X	Good Device Except for Marking
	415	180° Reversed	1×10^{-9}	No Defects Noted	X	Good Device Except for Marking
	630	180° Reversed	2.5×10^{-9}	No Defects Noted		Good Device Except for Marking
9932 (1539)	1343	Output Transistors Degraded	3.0×10^{-8}	--		Held for Gas Analysis
	1365	180° Reversed	Gross Leaker	Metallization Melted Open Near Pin 7		Device Overstressed Due to Misorientation
	1565	180° Reversed	3.5×10^{-8}	Metallization Melted Open Near Pin 7		Device Overstressed Due to Misorientation
9936 (1536)	64	RTOK	Gross Leaker	Double Bond at Pin 11		Good Device
	209	RTOK	Gross Leaker	Die Surface Contamination, Double Al Bond on Both Post and Die at Pin 14, Bond Misbonded		Good Device
	313	RTOK	Gross Leaker	Destroyed During Delidding		--
	377	Pin 5 Open	Gross Leaker	Al Wire Bond Separated at Pin 5 Post		Mechanical Bond Failure
	519	RTOK	5.0×10^{-9}	--		Held for Gas Analysis
	606	180° Reversed	Gross Leaker	No Defects Noted	X	Good Device Except for Marking
	664	180° Reversed	Gross Leaker	Destroyed During Delidding		--
	749	180° Reversed	7.5×10^{-9}	No Defects Noted		Good Device Except for Marking
	787	180° Reversed	5.0×10^{-9}	No Defects Noted		Good Device Except for Marking
	827	180° Reversed	Gross Leaker	No Defects Noted		Good Device Except for Marking
	922	180° Reversed	Gross Leaker	--		Destroyed During Delidding
	1164	180° Reversed	Gross Leaker	No Defects Noted		Good Device Except for Marking
9944 (1537)	98	Input Diode	1×10^{-9}	Destroyed During Delidding		--
	107	180° Reversed	5.0×10^{-9}	--		Held for Gas Analysis
8846 (1538)	109	180° Reversed	Gross Leaker	No Defects Noted		Good Device Except for Marking
	196	180° Reversed	Gross Leaker	No Defects Noted	X	Good Device Except for Marking
	244	No Defects Noted	3.0×10^{-7}	No Defects Noted		Good Device
	854	180° Reversed	2.8×10^{-8}	No Defects Noted		Good Device Except for Marking
	1072	No Defects Noted	2.8×10^{-8}	No Defects Noted		Good Device
	1122	180° Reversed	Gross Leaker	No Defects Noted		Good Device Except for Marking
	1175	Retest Good	1.0×10^{-8}	No Defects Noted		Good Device
	1176	180° Reversed	3.0×10^{-8}	No Defects Noted		Good Device Except for Marking
	1298	Input Diode Degraded	3.0×10^{-8}	Cracked Die.		Possible Electrical Overstress
	1299	Input Diode Degraded	Gross Leaker	Cracked Die		Possible Electrical Overstress
	2038	180° Reversed	Gross Leaker	No Defects Noted	X	Good Device Except for Marking
	3320	180° Reversed	1.8×10^{-8}	Oxide Thickness Variations		Good Device Except for Marking
	4025	180° Reversed	1.3×10^{-8}	No Defects Noted		Good Device Except for Marking
	4375	180° Reversed	Gross Leaker	No Defects Noted		Good Device Except for Marking
	4476	180° Reversed	4.5×10^{-8}	--		Held for Gas Analysis
9948 (1535)	176	--	Gross Leaker	--		--
	186	No Defects Noted	Gross Leaker	Excessive Bond Tool Marks at Die Bond - Pin 10		Good Device
	337	RTOK	Gross Leaker	No Defects Noted		Good Device
	389	180° Reversed	Gross Leaker	Destroyed During Delidding		Good Device Except for Marking
	470	180° Reversed	Gross Leaker	No Defects Noted	X	Good Device Except for Marking
	575	Pin 3 Open	7.8×10^{-9}	Al Wire to Pin 3 Melted Open		Electrical Overstress
	651	RTOK	Gross Leaker	Destroyed During Delidding		Good Device
	627	RTOK	Gross Leaker	Destoryed During Delidding		Good Device
	662	180° Reversed	Gross Leaker	No Defects Noted	X	Good Device Except for Marking
	996	RTOK	Gross Leaker	Destroyed During Delidding		Good Device
	1021	RTOK	Gross Leaker	Destroyed During Delidding		Good Device
	1037	180° Reversed	Gross Leaker	No Defects Noted	X	Good Device Except for Marking
	1129	No Defects Noted	Gross Leaker	Tooling Marks on Al Near Pins 10 & 11		Good Device
	1236	RTOK	Gross Leaker	No Defects Noted	X	Good Device
	1395	RTOK	Gross Leaker	External Lead 11/12 Missing		Good Device Except for Mechanical Damage
	1656	180° Reversed	1.5×10^{-8}	Poor Bonding - Excess Not Trimmed		Good Device Except for Marking
	2197	RTOK	Gross Leaker	Destroyed During Delidding		Good Device
	2534	RTOK	Gross Leaker	Destroyed During Delidding		Good Device
	2535	RTOK	2.8×10^{-8}	--		Held for Gas Analysis
	2580	180° Reversed	Gross Leaker	No Defects Noted	X	Good Device Except for Marking
	2929	180° Reversed	Gross Leaker	No Defects Noted	X	Good Device Except for Marking
9984 (1535)	2874	RTOK	3.0×10^{-8}	Destroyed During Opening		Good Device

*RTOK - Retest Electrically Good

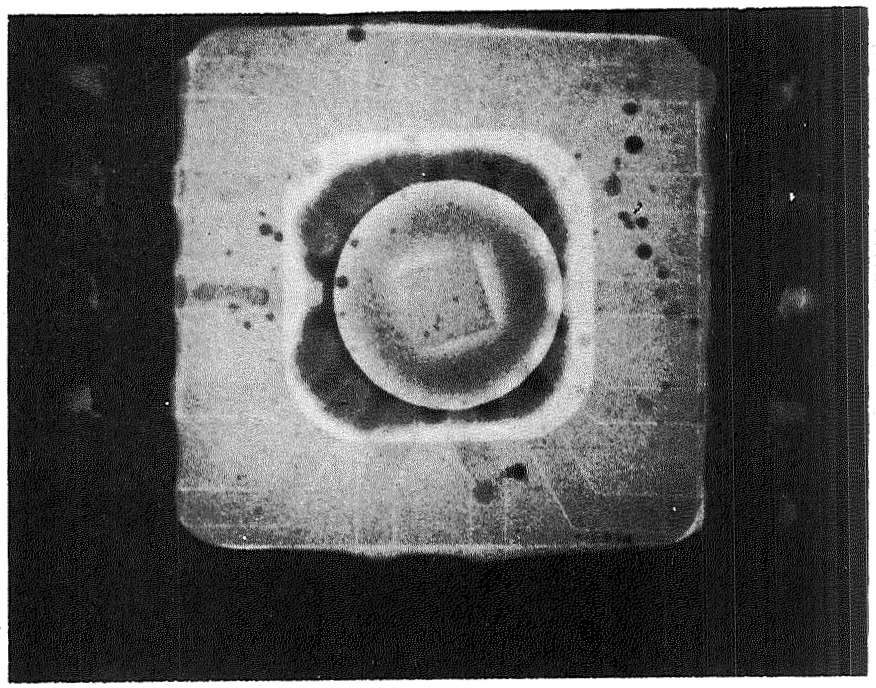

Figure I-15. Radiograph of Typical Device Showing Excess Pyroceram.

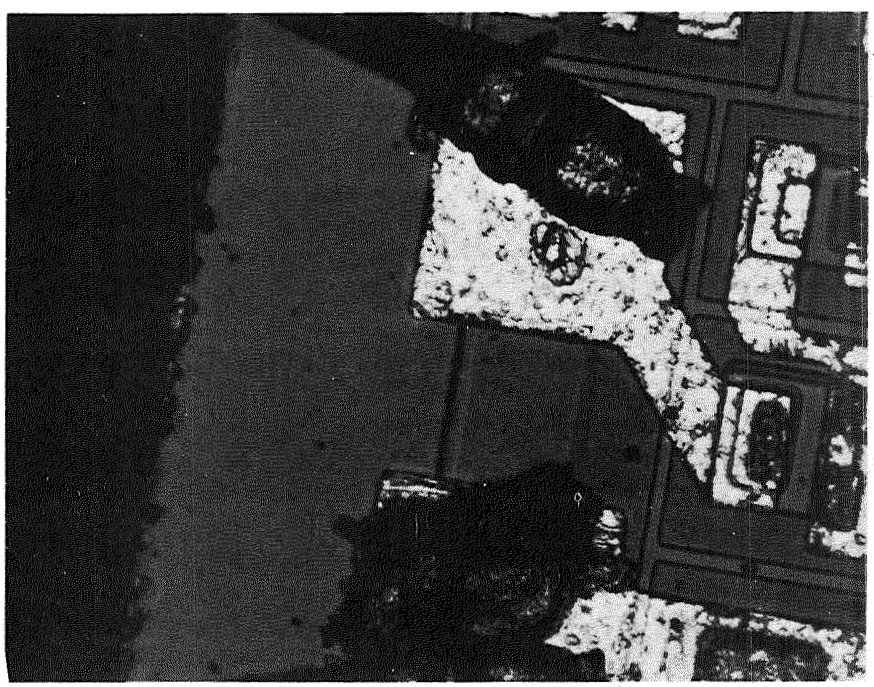

Figure I-16. Surface Photo of Type MIC 936 Failure Device Showing Dual Bond on Pad

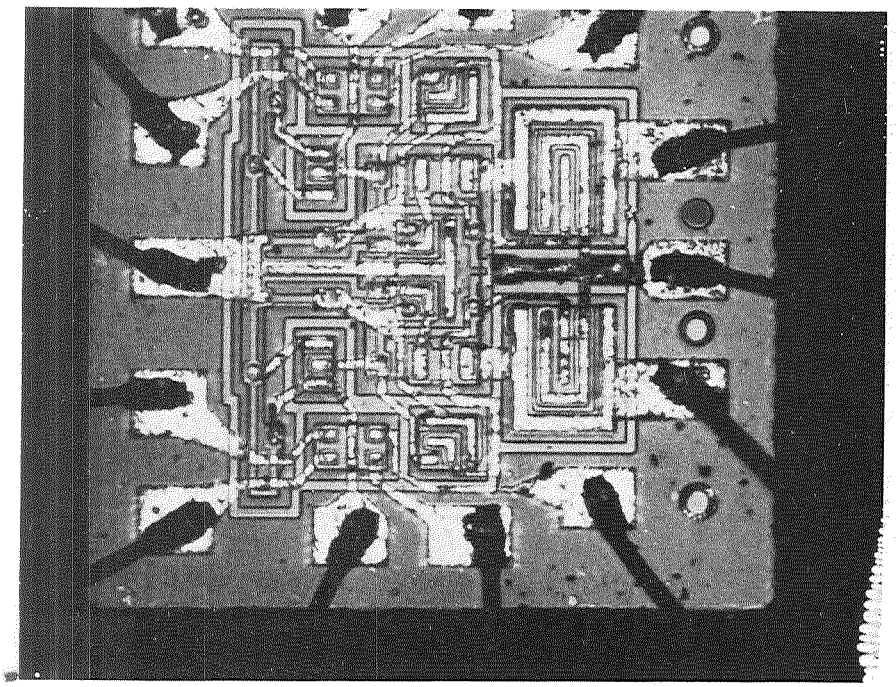

Figure I-17. Surface Photo of Type MIC 932 Failure Device Showing Discolored Metallization from Electrical Overstress

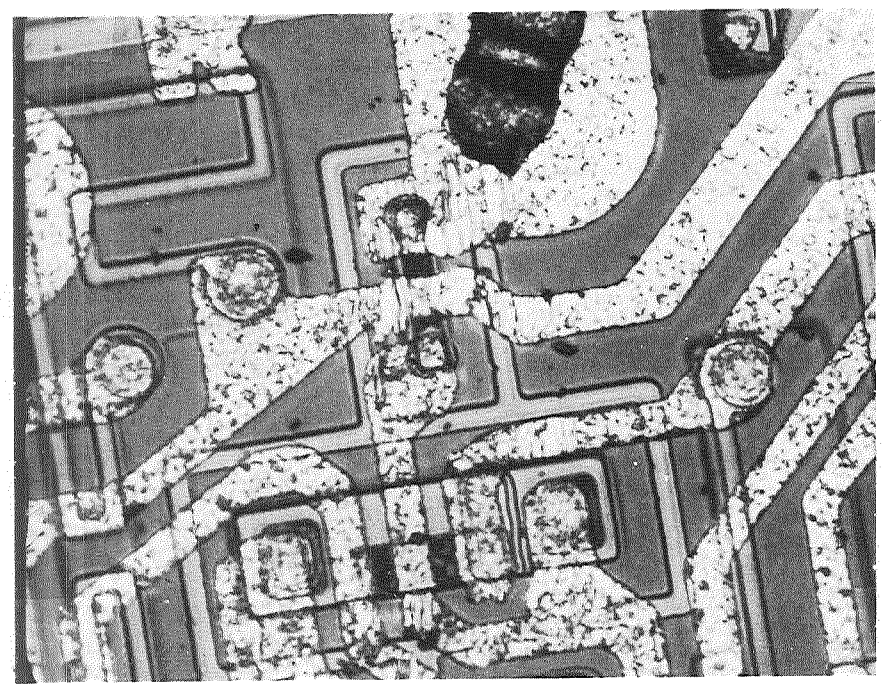

Figure I-18. Surface Photo of Type MIC 938 Failure Device Showing Tool Damage and Smeared Metallization

APPENDIX J. INSTRUMENTS FOR FAILURE ANALYSIS

INSTRUMENTS FOR FAILURE ANALYSIS

Instrument	Abnormality Observed (physical)	Related Failure Modes	Probable Failure Mechanisms
Dye penetrant	Cracks in package seals	Leaks	Inversion (change in semiconductor type)
Etching and microscopy	Dislocation distribution	Soft junction (gradual rather than sharp increase in current characteristic across junction)	Electrical parameter drifts
	Pits, cracks, and chips	Opens	Mechanical failure
	Pinholes and cracks in oxide insulating layer	Shorts	Migrating of metallization
Binocular microscope (3-120X magnification)	Inhomogeneity (Oxidation, contamination, intermetallics or rub marks.)	Weak bonds or electrical leakage	Poor surface wetting Migration of charged contaminant causes inversion. Intermetallics form by diffusion. May have resulted from overheating.
	Opened bonds	Electrical open circuit	Mishandling, overheating, or contaminated surface.
	Cracked dice	Open circuit or shift in resistance	Pressure during die or lead bonding.
	Cracks in package lead seals	Leaks	Rough handling, misalignment, thermal mismatch, or bubbles in glass.

INSTRUMENTS FOR FAILURE ANALYSIS (Cont)

Instrument	Abnormality Observed (physical)	Related Failure Modes	Probable Failure Mechanisms
Binocular microscope (3-120X magnivication) (continued)	Pits and pyramids on dice	High leakage or hot spots at thinner base areas	Poor epitaxial growth control results in thin localized base areas (after diffusion).
	Poor registry or masking	High leakage, shorts or opens	Narrow insulating path may short, or inversion may cause high leakage current.
	Scratches on dice or intraconnects	Open or high resistance	Handling and testing.
	Microplasma in operating device	Soft junction	Current concentrates at stacking faults, dislocations, or thin spots in base.
Phase contract microscope	Stacking faults	Soft junctions	Shifting electrical parameters.
	Transparent contaminants	Surface inversion	Ionic contaminants migrate and result in reverse leakage.
	Improper oxide metallization topography	Electrical leakage, shorts, or opens	Misalignment creates narrow insulating paths which short or leak as result of inversion.
Dark field microscope	Photoresist residues, dust	Inversion	Diffusion of charged contaminants.
	Bubbles in Sealant glass	Leaks	Inversion.
Interferometer	Oxide and surface topography varies from design	Electrical leakage, shorts or opens	Misalignment creates narrow insulating paths which short or leak as result of inversion.

INSTRUMENTS FOR FAILURE ANALYSIS (Cont)

Instrument	Abnormality Observed (physical)	Related Failure Modes	Probable Failure Mechanisms
Interferometer (continued)			Meager contacts melt and open.
	Oxide thickness varies from design	Stray capacitance, electrical leakage or inversion	Metal diffuses through oxide and causes leakage.
	Metal thickness varies from design	Opens	Thin metal areas burn out.
Electron microscope (magnifies to 100,000X)	Dislocation and stacking faults distribution	Soft junctions	Precipitates in bulk silicon.
	Contaminant and corrosion location	Weak bonds or electrical leakage	Electrochemical reaction.
	Etch pits, scratches dust, and deposit roughness	Opens, shorts, or parameter drift	Surface roughness cause thin spots in conductor deposits which may heat and melt.
	Pattern alignment and topology errors	Shorts or opens	Meager contacts burn open. Narrow isolation areas short across.
	Undercut etched edges	Opens or inversion	Contaminants cause corrosion and opens or migrate and cause inversion.
	Weld porosity	Contaminants	Contaminants cause corrosion and opens or migrate and cause inversion.
	Porous diffusion products	Contaminants or weak bonds	Contaminants cause corrosion and opens or migrate and cause inversion. Kirkendall effect (mismatched diffusion rates of dissimilar metals)

INSTRUMENTS FOR FAILURE ANALYSIS (Cont)

Instrument	Abnormality Observed (physical)	Related Failure Modes	Probable Failure Mechanisms
Electron Microscope (magnifies to 100,000X) (continued)			causes voids. Thin spots may heat and melt.
	Scribe cracks	Opens (if cracks propagate)	Thermal or mechanical stress causes cracks to propagate.
Radiographic equipment	Voids in welds	Leaks in package; opens if voids are associated with bonding of wires and package to IC die	Inversion corrosion, poor welding control.
	Metal migration	Shorts or opens	Kirkendall voids form weak bonds.
	Contaminant particles	Shorts	Mobile metallic contaminants shorts.
	Cracks	Opens or leaks	Cracks propagate and open connections.
	Long wires	Shorts	Wires sag, cause shorts.
	Misalignment of metal parts	Leaks, opens, or shorts	Misalignment causes weak bonds, shorts, opens, or leaky packages.
Controlled etching	Depth of inversion charge	Inversion	Inversion
X-ray diffraction	Identity of contaminant compounds or corrosion product compounds	Weak bonds or electrical leakage	Electrochemical reaction
	Identity of materials	Abnormal electrical parameters	Drift of electrical parameters.

INSTRUMENTS FOR FAILURE ANALYSIS (Cont)

Instrument	Abnormality Observed (physical)	Related Failure Modes	Probable Failure Mechanisms
Metallograph	Observes same abnormalities as binocular microscope; also:		
	Poorly adherent interconnects or bond structures	Opens	Improper deposition and/or bonding conditions.
	Abnormal junction depth (by angle lapping)	Improper electrical characteristics.	Bad junction depth.
	Voids in thermocompression bonds	Bond has high electrical and/or thermal resistance and may be mechanically weak	Hot spots, poor electrical characteristics or opens.
	Incomplete or poor welds	Leak in package	Faulty package seals.
	Thin or non-adherent plating	Poor joints	Opens bonds and/or package leaks.
Electron backscatter thickness meter	Thickness of oxide, plating or photoresist	Stray capacitance, electrical leakage, inversion or opens	Electrical parameter drift
Scanning Electron Microscope	Metallization thinning or undercutting	Opens	Thin spots Burn open
	Contaminant and corrosion location	Weak bonds or electrical leakage	Electrochemical reaction

INSTRUMENTS FOR FAILURE ANALYSIS (Cont)

Instrument	Abnormality Observed (chemical)	Related Failure Modes	Probable Failure Mechanisms
Hot stage metallograph	Contaminant melting point and reactivity (for identification)	Weak bonds or electrical leakage	Electrochemical reaction.
	Interdiffusion of metals, for example, Al-Au, Mo-Au, Ti-Au, Kovar-Au	Parameter drift	Intermetallics form from diffusion.
	Whisker growth	Shorts or opens	Metal whiskers grow and make shorts. Removal of metal leaves opens.

INSTRUMENTS FOR FAILURE ANALYSIS (Cont)

Instrument	Abnormality Observed (chemical)	Related Failure Modes	Probable Failure Mechanisms
Hot stage metallograph (continued)	Grain growth	Parameter drift	Drift in braze, bond, or interconnect resistance.
	Surface diffusion or metal films	Shorts, opens or parameter drift	Metal films cause shorts or inversion. Lack of diffusion barriers.
Electron diffraction	Contaminant crystal structure and identity of intermetallic compounds	Weak bonds or electrical leakage	Electrochemical reaction.
	Deposit crystallinity	Open, shorts, or parameter drift	
Low-energy electron diffraction	Presence of absorbed substances in surface	Inversion	Migration of charged absorbates causes inversion.
Electron microprobe (elemental chemical analysis)	Contaminant or rub mark residue identity and map	Weak bonds or electrical leakage	Migration of charged contaminants causes inversion.
	Dopant and Dopant concentration	Related to process control	
	Intermetallic analysis	Weak bonds or electrical leakage	
	Corrosion product identity	Weak bonds or electrical leakage	
	Deposit topography map by chemical element	Opens, shorts, or parameter drift	
	Deposit thickness map by chemical element	Opens	Thin areas melt and open.
	Crack, pit, and pinhole maps	Opens or shorts	Thin or narrow areas on interconnects open. Pinholes.

INSTRUMENTS FOR FAILURE ANALYSIS (Cont)

Instrument	Abnormality Observed (chemical)	Related Failure Modes	Probable Failure Mechanisms
Electron microprobe (elemental chemical analysis) (continued)	Junction misalignment or movement	Electrical leakage, shorts, opens, or inversion	Migration of metal is evidence of inversion.
	Opens, short and current and/or voltage nonuniformity map	Abnormal electrical parameters	Cause of abnormal electrical parameter may pinpoint failure mechanism.
Gas chromatograph	Abnormal package ambients	Inversion or gain drift	Absorption, then charge migration causes inversion.
	Leaks (by presence of air or test fluid)	Inversion or gain drift	Absorption, then charge migration causes inversion.
Mass spectrograph	Leaks. Also: reaction of device to ambient changes in the spectrograph	Inversion or gain drift	Absorption, then charge migration causes inversion
Infrared absorption spectrograph	Thin oxide	Shorts or electrical leakage	Abnormal electrical parameters
	Abnormal oxygen content in silicon	Drift of electrical parameters	Recombination centers
	Abnormal epitaxy thickness	Slow switching, punch-through	Drift of marginal electrical parameters
	Impure photoresist	Inversion	Migration of impurities.
	Water	Surface current leakage	Water vapor enters through leak.
Emission ultraviolet and visible spectrographs	Analysis and identity of contaminants	Parameter drift, opens, inversion	Contaminants migrate and change electrical properties or cause corrosion.

INSTRUMENTS FOR FAILURE ANALYSIS (Cont)

Instrument	Abnormality Observed (chemical)	Related Failure Modes	Probable Failure Mechanisms
Visible and ultra-violet absorption spectrographs	Analysis and identify of contaminants	Parameter drift, opens, inversion	Contaminants migrate and change electrical properties or cause corrosion.
Neutron activation analyzer	Same as emission spectrographs but at lower concentrations	Parameter drift, opens, inversion	Contaminants migrate and change electrical properties or cause corrosion.
Ion Microanalyzer	Dopant and diffusion profile	Process control problems	
	Oxide impurity concentration	Parameter drift or electrical leakage	Inversion
	Topography map of surface by chemical element	Opens, shorts, or parameter drift	
Auger spectrography	Surface impurities	Parameter drift or electrical leakage	
Flame photometer	Residual chemical identity	Electrical leakage, opens	Electrochemical reaction

Instrument	Abnormality Observed (mechanical)	Related Failure Modes	Probable Failure Mechanisms
Strain gauges	Loose headers or dice	Thermal	Nonadhesion of braze evident from thermal expansion of can. Poor thermal path causes overheating.
	Poorly brazed headers or dice	Thermal	Nonadhesion of braze evident from thermal expansion of can. Poor thermal path causes overheating.
Bubble tester	Gross leaks in packages	Channeling or inversion	Nonadhesion of braze evident from thermal expansion of can. Poor thermal path causes overheating.
		Opens or shorts	Corrosion causes opens or shorts.
Helium leak tester or Radioflo tester	Small leaks	Uncontrolled package ambient causes inversion and corrosion	Charged absorbates from ambient migrate and cause inversion. Corrosion by ambient causes opens or shorts.

INSTRUMENTS FOR FAILURE ANALYSIS (Concluded)

Instrument	Abnormality Observed (mechanical)	Related Failure Modes	Probable Failure Mechanisms
Thermal plotter	Hot spots due to voids	Excess currents	Material degradation.
	Hot spots due to thin base areas	Excess currents	Uneven diffusion and thin base areas.
	Hot spots due to dislocation or stacking faults	Excess currents	Faster diffusion along fault causes thin base area.
Curve tracer	Shorts	Shorts	Sagging wire, punch through or surface creep of metal.
	Opens or intermittent contacts	Opens or intermittent contact	Mishandling, intermetallic formation.
	Soft junctions	Soft junctions	Surface leakage.
	Abnormal resistance	Abnormal resistance	Mechanical damage or corrosion.
	Leakage currents and inversion	Inversion	Surface charge migration or surface contamination.

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APPENDIX K. BIBLIOGRAPHY ON SILICON SURFACE PASSIVATION

This program has been directed toward an understanding of the interrelationship of semiconductor device processing and the resultant reliability. Specifically, the role of surface passivation and related process variables has been studied.

In conjunction with the research carried out on this program, a continual literature review was made, with a goal of relating other findings to the results of this program. Also searched for were improved passivation techniques which might reduce or eliminate the problems defined for currently used Si-SiO_2 systems. The following is a synopsis of some of the pertinent information which is applicable to the research performed. The information is presented in several related sections.

Preparation of Oxide Layers

A comprehensive report on the process parameters for oxidized silicon was prepared by the Research Triangle Corporation (Ref 1). A more detailed analysis of the kinetics of the growth process has been presented in several articles by Deal (Ref 2) and Burkhardt and Gregor (Ref 3). The parabolic growth rate constants as a function of various process variables was explored by Ainger (Ref 4). The oxidation kinetics of silicon were studied by Law (Ref 5) at temperatures from 1000 to 1300K and pressures from 10^{-3} to 5×10^{-2} mm. This information confirmed the parabolic growth rate, with the rate constant being markedly pressure dependent.

It has been demonstrated that hydroxyl groups can be introduced into silica by high temperature exposure to water vapor (Ref 6), that oxides grown in steam or wet ambients contain measurable amounts of hydrogen (Ref 7, 8, 9), and that thermally grown oxides incorporate varying amounts of the substrate dopant into the oxide structure (Ref 10, 11). Investigators have shown that the growing oxide has an affinity for boron but rejects phosphorus and antimony (Ref 11).

Nossibian and Whiting (Ref 12) showed that particulate contaminations on the oxide surface act as loci for the formation of high concentration regions of P_2O_5 during a deposition of phosphorus. In the subsequent diffusion, the phosphorus is considered to penetrate the oxide preferentially beneath these high concentration sources, doping the silicon substrate in localized regions under the oxide.

Several low temperature techniques have been proposed for forming silicon oxide films. These methods are of special interest in that they reduce the thermal stress problem possibilities.

Thin oxide films were formed by dilute HNO_3 and studied (Ref 13). The formation of SiO_2 films by the low temperature (750 C) decomposition of tetraethoxysilane in an evacuated system was studied (Ref 14). The performance of the system was investigated and the film characteristics evaluated. Most of the properties of the deposited oxides were similar to those of thermally grown oxides after a thermal treatment. Hennisch (Ref 15) devised a closed tube method for deposition of SiO_2 via decomposition of tetraethoxysilane.

The growth of SiO_2 in a microwave discharge was investigated by Kraitchman (Ref 16). This technique provided rapidly oxidized silicon at temperatures estimated to be 500 C or lower.

Ing and Davern (Ref 17) described a process for the formation of silicon oxide thin films by the low temperature decomposition of tetraethoxysilane in an a-c glow discharge. It was shown that films produced in this manner can be used effectively as the dielectric in thin film capacitors. The resultant capacitors have low dielectric losses and are very stable under various life test conditions.

Other Passivation Techniques

Several other materials or combinations of materials have been investigated in an attempt to eliminate some of the objectionable problems detected for the $Si-SiO_2$ system.

Aboaf (Ref 18) experimented with amorphous aluminum oxide films deposited at 420 C by thermal decomposition of an aluminum alkoxide. The dielectric and moisture resistance properties were favorable when compared with conventional SiO_2.

MOS transistors with aluminum oxide gate dielectric were fabricated and tested by Waxman and Zaininger (Ref 19). Their films are formed by anodizing aluminum in an oxygen plasma. The radiation resistance of these devices appeared excellent.

The most promising substitute and the one with extensive work involves various types of silicon nitride films. Typically silicon nitride films have been deposited on silicon by reacting $SiCl_4$ and NH_3 at 550 - 1250 C (Ref 20). One important finding is that the deposited films are extremely effective diffusion masks for sodium.

Amorphous silicon nitride films have been deposited in a gas flow system by the ammonolysis of silicon tetrachloride and the nitridation of silane with ammonia (Ref 21, 22). The substrate temperature during the deposition process appeared to have the most significant influence on the film properties. It has been shown that such amorphous nitride films can be converted to anodic SiO_2 (Ref 23).

Amorphous films of silicon nitride-silicon dioxide mixtures were deposited and evaluated by Chu and coworkers at Westinghouse (Ref 24). The technique utilized was the pyrolysis of silane in ammonia-oxygen mixtures in a gas flow system. Heat treatment of silicon nitride films (Ref 25) was found to result in severe structural changes resulting in fractured layers.

Passivation Layer Mechanical Aspects

Mechanical rupturing of the oxide film has been related in this report and by others (Ref 26) to the difference in coefficient of thermal expansion between silicon and the passivation layers utilized.

The evidence as reported (Ref 27, 28) indicates that dielectric failures are a result primarily of actual physical openings in the insulating layer rather than regions of enhanced conductivity in uniformly thick oxide.

The silicon-silicon oxide stress has been experimentally measured (Ref 27, 29) and was found to be in the range from 30,000 to 60,000 psi. The expansion characteristics of silicon apparently exhibit unusual behavior (Ref 30) above ~ 1000 C.

The effect of structural defects such as hydroxl groups and network forming or other modifications is to alter the silica structure producing a less rigid network. This alteration is reflected in changed physical and electrical properties. For example, the introduction of either boron (Ref 31) or hydroxl (Ref 32) into the SiO_2 structure increases the thermal expansion coefficient and decreases the viscosity of the modified material relative to the intrinsic oxide. Strains at the Si-SiO_2 interface were measured by Joecodine and Schlegel (Ref 33) and Whelan (Ref 34). Besser and Eisenberg (Ref 35) and Lopez (Ref 36) studied the factors that affect the density of defects in SiO_2 films. Lane (Ref 37) has recently correlated stress in the Si-SiO_2 interface to surface state density.

Lopez (Ref 38) found that defect density for a particular thickness was greater for the thinned oxide than for the unaltered oxide.

It has been shown that mechanical polishing results in a certain amount of structural damage to the silicon surface and may leave particles of the polishing compound embedded in the polished surface. This was recently confirmed (Ref 39) by electron microprobe analysis performed by Cocca and Carroll at NASA-ERC. This may be the origin of the somewhat higher defect density in the oxide grown on such wafers.

Fisher and Amick (Ref 40) detected defect structures on silicon surfaces after oxidation which were partially due to stresses induced by the oxidation processes. Slip in Si crystals has also been suggested. Recently Drum and Rand reported (Ref 41) a method of reducing stress by using a silicon oxide-silicon nitride combination. Stresses of the order of 10^7 dynes/cm^2 were obtained which is 2 to 3 orders of magnitude lower than usually obtained.

Techniques utilized by other investigators were evaluated for use on this program for the detection of dielectric defects. Techniques such as a high temperature HCl etch (Ref 42) or Cl etching around 900 C (Ref 43, 44) were found to be not conveniently applicable. The results obtained earlier on this contract have been reported (Ref 27) and two techniques which were found to be suitable, electrophoretic decoration and electrochemical autograph, were utilized in this study for the observation of oxide defects.

Passivation Layer Properties and Evaluation Techniques

Techniques for the physical and chemical evaluation of silicon oxide films formed by a wide variety of techniques have been developed (Ref 45). Silicon oxide films were characterized on the basis of refractive index, etch rate, infrared spectra, stoichiometry, passivation efficiency and thermal densification. It was found that films formed by low temperature techniques generally had properties inferior to oxides formed by conventional high temperature techniques.

Worthing (Ref 46) and Klein (Ref 47) made evaluations of dielectric breakdown in thin oxide films. At positive silicon potentials, Worthing found that dielectric breakdown occurred abruptly with no detectable conduction at lower voltages. At negative silicon potentials, conduction in the nanoamp range and time dependence of dielectric breakdown was detected. Klein confirmed that breakdown starts on electric field induced thermal instability at flaws in the dielectric resulting in a hole through the oxide.

The properties of silicon nitride-silicon oxide mixtures were obtained by Chu, Szedon, and Lee (Ref 24).

The electrical properties of both silicon nitride and silicon oxide were investigated by Deal, Fleming and Castro (Ref 48). As contrasted to the thermal oxides, the silicon nitride films are characterized by polarization and room temperature trapping instabilities, relatively high conductance, and high surface state charge densities. The vapor-deposited oxides were found to resemble the nitrides in those properties which were associated with the silicon-dielectric interface, but the bulk properties were more like those of thermal oxides. The properties of a $SI_XO_YN_Z$ film on Si was investigated by Brown and others at G. E. Research, Schenectady (Ref 49). These films were formed by the pyrolysis of various mixtures of SiH_4, NH_3, and NO.

Several investigators have utilized the MOS test structure as a means for electrical evaluation of silicon oxide films. Typical reviews by Fairchild personnel describe impurity distributions of oxidized silicon and ion migration kinetics (Ref 50, 51).

A method of doping the oxide film with (DEP) diethylphosphate-nitrate-tetrahydrofuryl alcohol alcohol was studied for use in device diffusion of phosphorus (Ref 52). The fabrication of simple device structures by controlled out-diffusion of phosphorous from the oxide was evaluated.

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APPENDIX L. SUMMARY OF LITERATURE ON OXIDE IMPURITIES AND RELATED ELECTRICAL EFFECTS

Ion drift has been proposed as a significant reason for instability in MOS devices (Ref 1, 2 and 3). Sodium ions, protons, polarization of the dielectric material and oxygen vacancies have been postulated as some of the specific reasons for unstable electrical parameters of the MOS devices. The effect of sodium ions on device stability has been extensively studied by many investigators (Ref 1, 4, 5 and 6).

The results of a detailed study of the charge motion and instability in thermally grown, undoped silicon dioxide films at high electric fields and elevated temperatures were presented by S. R. Hofstein (Ref 2). The transient behavior of the charge motion in the oxide was analyzed and a model proposed to explain the observations. It was shown that the instability consists of the motion of positively charged ions and that interface trapping effects play a significant role in determining the transient behavior. Detailed consideration was given to the nature of these trapping effects. It was concluded that caution must be exercised in ascribing the activation energy measured for the instability to that for the true mobility of these ions in a "bulk" oxide. The effects of various ambient treatments on the instability were discussed, and conclusions drawn concerning the physical and chemical nature of the observed instability.

E. H. Snow et. al., Ref 1, showed that changes in the capacitance-voltage characteristics of a metal-insulator-semiconductor structure provide a powerful tool for the observation of ion motion in thin insulating films. Using this method, a detailed study of the kinetics of alkali ion migration in thermally grown silicon dioxide films has been made. Alkali ions were initially deposited at the metal oxide interface and their transport through the oxide was studied as a function of time, temperature and applied voltage. When the metal is biased positively the number of ions accumulated at the oxide-silicon interface initially proportional to the square root of time and then approaches a saturation value. The temperature dependence is exponential and leads to an activation energy for the diffusion coefficient of 32 kcal/mole for Na and 22 kcal/mole for Li.

A simple model was developed which was based on the division of the insulator into two regions: a thin boundary layer near the metal-insulator interface in which ion transport is by diffusion, and the remainder of the insulator where field transport dominates. It was shown that most features of this model were in excellent agreement with the experimental results.

The effects of alkali-metals on the vehavior of the oxide protected silicon surfaces has been investigated using a p-n structure by J. R. Mathews, W. A. Griffin and K. H. Olson (Ref 3). Examination of diode characteristics and photoresponses on controlled samples revealed the manner of alkali-metal electrolysis through the oxide and the formation of donor-type surface states at the $Si-SiO_2$ interface.

A direct comparison between Na distribution determined radiochemically and electrically in 6000 Å thermal oxide on 10 Ω-cm n-type silicon was made by E. Yon, W. H. Ko and A. B. Kuper (Ref 5). Sodium within $\lesssim$ 1000 Å of $SiSiO_2$ interface

correlates in most cases with MOS flat band voltage shift, i.e., N_{na} ($\gtrsim$ 1000 Å) $\approx$ $+\Delta Q_{MOS}$. Appreciable Na, which does not appear to affect Si surface potential, is found through the bulk of the oxide. Neutron activation of "clean" oxide (grown in wet or dry oxygen) showed ~ 1 ppm Na throughout, ~ 10 ppm at free surface. Gold was also identified at ppm concentrations but did not correlate with ΔQ_{MOS}. The V-shaped profile seen after diffusion (300 to 1000°C in dry N_2) or in drift (~ 200°C, 5×10^5 V/cm) is believed due to rate limitation at the free surface; electrostatic binding plus enhanced solubility at the 800°C, which is not expected from the fast diffusion of Na. This is also attributed to the surface rate limitation. The anion significantly affects Na diffusion kinetics and distribution in contamination experiments with radiotracer $Na^{24}OH$, $Na^{24}Cl$, and $Na^{24}Br^{82}$. Br is found to accompany Na diffusion, suggesting anion neutralization of Na within the bulk oxide. P_2O_5 SiO_2 is seen to "getter" Na from the oxide. These results support the suggestion of Snow et al. that Na is responsible for uncontrolled drift of surface potential in oxidized Si devices.

Interactions between sodium ions and protons to cause both fast and slow instabilities as well as active and inactive ion forms have been described (Ref 6, 7, and 8). Motion of chromium, gold, aluminum and nickel in oxide layers has also been studied (Ref 9 and 10). E. Kooi and M. V. Whelan (Ref 7) used MOS-capacitance measurements combined with neutron activation analysis to show that positive charge at oxidized silicon surfaces could be increased by the presence of sodium in the oxidation system. The amount of charge depends on the surface orientation and the oxide thickness. It can be decreased by low-temperature heat treatment in water vapor by hydrogen. The same treatment can cause an effective reduction of the number of interface state. In both cases an explanation can be found in the formation of Si-H bonds.

Protons were postulated as mobile ions but subsequent studies with radio-tracer methods revealed that tritium in the oxide does not move in an electrical field (Ref 2, 9, 11, and 12).

Phosphorous diffusion into the oxide layer has been found to stop or reduce ion migration if boron is not present in large amounts (Ref 13, 14 and 15). However, thick phosphosilicate layers were observed to polarize and cause additional instability (Ref 16 and 17).

The admittance-voltage characteristic of a metal-insulator-semiconductor capacitor was explained by E. H. Nicollian and A. Goetzberger (Ref 13) in the depletion-inversion range for the case in which the entire surface of the semiconductor is inverted by charges in the insulator and the frequency is too high for minority carriers to follow. Lateral AC current flow into the inverted layer beyond the field plate has to be considered. The model was verified by several experiments and a simple equivalent circuit was shown to quantitatively fit the characteristics. The lateral current model was used to explain drift in the characteristics caused by ion migration along the oxide surface under dc bias. This type of ion migration is separated from true changes of charge density within the insulator.

Michael Yamin (Ref 14) performed two experiments with phosphorous stabilized and untreated silicon dioxide films on silicon substrates. In the first, the interaction of phosphorous and boron was studied; it was found that diffusion of boron over a phosphorous stabilized film destroyed its stabilization against ion drift effects at 400°C,

but that diffusion of phosphorous over a boron diffused film resulted in a stabilized oxide. In the second experiment, a slowly varying voltage was applied at 600°C to a silicon-silicon dioxide-gold structure and the current through the oxide film was recorded. Both phosphorous stabilized and untreated silicon dioxide films show rectifying characteristics, the more highly conducting direction being that with the silicon negative. In the case of the untreated film, a large peak of current is superimposed on this characteristic at -2.5 volts. This peak is absent in phosphorous stabilized films. Discharge currents equivalent to the charging currents are not observed on removing voltage from the specimen, as they are at 400°C. Five distinguishable types of charge transfer in silicon dioxide films are tabulated, and compared with those described in the literature as occurring in crystal quartz.

E. H. Snow and B. E. Deal (Ref 16) made a study of phosphosilicate glass films prepared by predepositing P_2O_5 on thermally oxidized silicon. Many of the properties of these films including composition, density, etch rate, conductivity, dielectric constant, and dielectric strength were measured and are compared with the corresponding properties of thermally produced silicon dioxide layers. A polarization effect is discussed which gives rise to an increase of about 20 percent in the dielectric constant of the glass at high temperatures and low frequencies (~ 250°C at 50 cps). Under dc bias at lower temperatures this polarization causes a slow drift in the capacitance-voltage characteristics of metal-oxide-semiconductor (MOS) capacitors which use the glass as a dielectric. The MOS capacitance-voltage method is used to study the time, temperature, and voltage dependence of the polarization, and mechanisms are discussed which can account for the observed results.

It was shown by E. H. Snow and M. E. Dumesnil (Ref 17) that electrical polarization effects in glass films can be conveniently studied using a metal-glass-silicon dioxide-silicon double-layer capacitor. The build-up of a polarization in the glass layer under the application of a voltage at elevated temperatures can be detected from the resulting shift ΔV in the capacitance-voltage characteristic. Equations are derived on the basis of a simple model which gives ΔV as a function of time, temperature, applied voltage, and the glass and oxide thicknesses.

Experimental data for a lead borosilicate glass are presented and shown to be in excellent agreement with this model. The time constant for polarization of the glass has an activation energy of 1.05 eV and is of the order of weeks at room temperature and minutes at 100°C. The diffusion coefficient calculated from this time constant is in agreement with that for lead in glasses of similar composition and hence it is concluded that in this glass the major mobile ion is Pb^{++}.

Additional long-term polarization effects are observed when the metal is biased positively and these are related to the diffusion of sodium contaminant out of the glass layer into the underlying silicon dioxide.

Oxygen vacancies as a mobile species were advanced as a hypothesis but was later questioned on the basis of the diffusion constant and the activation energy (Ref 8 and 11).

J. E. Thomas and D. R. Young (Ref 18) found that semipermanent changes in the semiconductor surface potential occurred in insulator-covered semiconductors when external fields were applied for long times, particularly at elevated temperatures.

An attempt to explain these changes in terms of the charging and discharging of interface states led to conclusions that disagree with many of the experimental facts. Specifically, the semipermanent effects of interface-state charges can always be overcome by the application of a field smaller than that which is used to induce the effect, and of the same sign, while the experiments described in the accompanying papers generally show that a field much larger than the inducing field, and of the opposite sign, is required to return the insulator covered surface to its initial status. The accumulation of space charge in the insulating layer can give rise to very large fields at the semiconductor surface that persist after the removal of an external inducing field. The size and sign of such space-charge fields agree with the experimental observations. Measurements made after treatment at temperatures above 125°C show that the surface of silicon passivated with silicon dioxide can become strongly n-type as a result of such a positive space-charge layer formed at the interface. A model is presented based on the concept that this space charge arises from oxygen vacancies in the silicon dioxide. It is suggested that the improvement resulting from the use of phosphorous pentoxide on the outside surface is due to the elimination of vacancies by the oxidizing action of the P_2O_5.

Silicon nitride and aluminum oxide have been reported to be immune to ion drift problems (Ref 19, 20 and 21). Devices fabricated with MNS structures, however, have shown undesirable properties due to high density surface states and conditions at the nitride-silicon interface (Ref 20).

Capacitance-voltage measurements have been utilized by many investigators as a technique for evaluating charge motion in oxide layers (Ref 22, 23, 24 and 25). Correlation of C-V curves with electrical charge in insulating layers (Ref 26 and 27) of MOS capacitors was published in some detail by Grove, et al. (Ref 22).

A. S. Grove, B. E. Deal, E. H. Snow and C. T. Sah (Ref 22) presented the results of a comprehensive study of the overall characteristics of thermally oxidized silicon surfaces and interpreted the results on the basis of a simple physical model of the MOS structure. Extreme care was taken throughout the study to insure the validity, significance and reproducibility of the quantities measured. It is shown that the charge in the surface states is constant over a wide range of variation of the surface potential, and that this charge is positive for both n- and p-type oxidized silicon. The density of surface state charge is about 2×10^{11} cm^{-2}, and is essentially unaffected by a twenty-fold variation in the oxide thickness and by a 250 fold variation in the concentration of boron in the p-type samples. The effects of measurement frequency, illumination and temperature on the capacitance was shown to follow one of three simple models depending on the measurement frequency and the rate of generation of minority carriers.

The redistribution of impurities during thermal oxidation of silicon was studied both theoretically and experimentally by Grove, Leistiko and Sah (Ref 11). Experiments with specific impurities indicate that gallium, boron, and indium deplete from silicon while phosphorous, antimony, and arsenic pile up during thermal oxidation. It was shown that the redistribution process can be significantly influenced by the escape of impurities through the oxide layer as well as by the segregation of the impurity at the oxide-silicon interface.

C-V graphical data has been reported a useful tool for evaluating MOS capacitors (Ref 28). Analysis characteristics and limitations of the C-V method for measuring surface-state densities has been discussed (Ref 23, 30 and 31).

C-V curves for n- and p- MOS devices with large numbers of surface states were measured at various frequencies by M. V. Whelan (Ref 31). These measurements indicate a difference in the relaxation times of the states of n- and p-type silicon. Comparisons were made with samples in which a large number of surface states had been removed by a suitable heat treatment. Two types of hysteresis effects occurring in certain measurements were discussed. The effects of heating MOS devices with and without a phosphate glass under a dc bias were compared.

Curves which relate the silicon space-charge capacitance at high frequencies to the band bending and the total space charge at a silicon surface were plotted by M. V. Whelan (Ref 28) for various values of silicon resistivity.

A. Goetzberger (Ref 29) computer ideal curves for silicon with oxide thickness and doping as a parameter. High-frequency and low-frequency capacity curves are presented for the doping ranges between 1×10^{14} and 1×10^{17} cm^{-3} and SiO_2 thickness between 100 and 12000 Å. Additional curves give flatband capacitance, minimum capacitance and voltage of the minimum capacitance in the same ranges.

Carrier concentrations and lifetimes have been studied by C-V measurements (Ref 32 and 33). Movement of impurities during thermal oxidation and gold diffusion has been followed by use of C-V data (Ref 24, 25 and 34). The technique has also been used to examine lateral motion of mobile charge in inversion layers of MOS capacitors (Ref 8 and 13).

A method to determine the carrier concentration and the minority carrier lifetime in semiconductor epitaxial layers was described by C. Jund and R. Poirier (Ref 32). This method implies the use of a MOS capacitance realized on the epitaxial layer. The carrier concentration is reached by measurements of maximum and limit values of the capacitance with bias voltage. The minority carrier lifetime is obtained by time constant measurement of the limit capacitance response to a voltage step.

Effects of ion drift on C-V curves in the fringing field around a MOS capacitor has been observed (Ref 35). The effect of a forward biased p-n junction on the C-V curve has also been studied and automatic equipment for obtaining C-V curves for in-process control has been described (Ref 36, 37 and 38).

A. Goetzberger (Ref 35) observed that MOS capacitance of p-type silicon in the inversion range is governed by lateral current flow in the channel. The inversion layer of devices into which alkali ions have been introduced can be enhanced under the field plate by bias aging. The MOS curve after aging takes on differnet shapes dependent on whether pinch-off occurs uniformly under the field plate (case 1) or in the fringing region (case 2). A curve of type 1 is shifted to more negative voltage without change of shape. In case 2, only the depletion-accumulation part is shifted leading to a broad valley. The fringing field at the interface can be calculated and the exact location of pinch-off determined. Its distance from the edge of the metal is usually less than twice the oxide thickness. The charge concentration profile at the edge is therefore very steep.

*ECS Journal, Vol. 116, No. 7. Characteristics of Fast Surface States Associated with SiO_2 - Si and Si_3 Ni - SiO_2 - Si Structures, B. E. Deal, E. L. MacKenna, P. L. Castro. An analysis of fast surface states in MOS and MNOS structures was conducted. The presence of aluminum metallization during certain annealing conditions (500 - 550C in an inert ambient) was confirmed to reduce the fast surface state density in MOS structures. Thin silicon nitride films (MNOS structures) were then found to mask or reduce this effect during the post-aluminum annealing treatment. It was postulated that a hydrogen species was produced in MOS structures during the post-metallization anneal by the reaction of aluminum and water absorbed on the oxide. The hydrogen then migrates to the Si - SiO_2 interface to annihilate the fast states. The silicon nitrate on the other hand is believed to retard the migration.

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NEW TECHNOLOGY APPENDIX

A. ELECTROPHORETIC DECORATION TECHNIQUE FOR LOCATION OF SiO_2 DIELECTRIC DEFECT

Technique 1:

This resulted from original work performed by J. Lytle at Westinghouse. Original development work was performed at Autonetics. Significant experimental data was accomplished on this contract (NAS 12-4). A special electrode developed for this technique was disclosed as PF69ER12 and reported under Air Force Contract AF0470-68-C-0174.

This technique is described in Appendix A-3 (p 99)

B. ELECTROGRAPH METHOD FOR LOCATING PINHOLES IN THIN SiO_2 FILMS

Technique 2:

This resulted from original work performed by J. McCloskey, Dept. 244, under Air Force contract funds and disclosed as PF69ER21 under Air Force Contract AF04(694)-626. This technique was utilized and further tested under this contract (NAS 12-4).

This technique is described in Appendix A-1 under Test Methods (p 73).

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