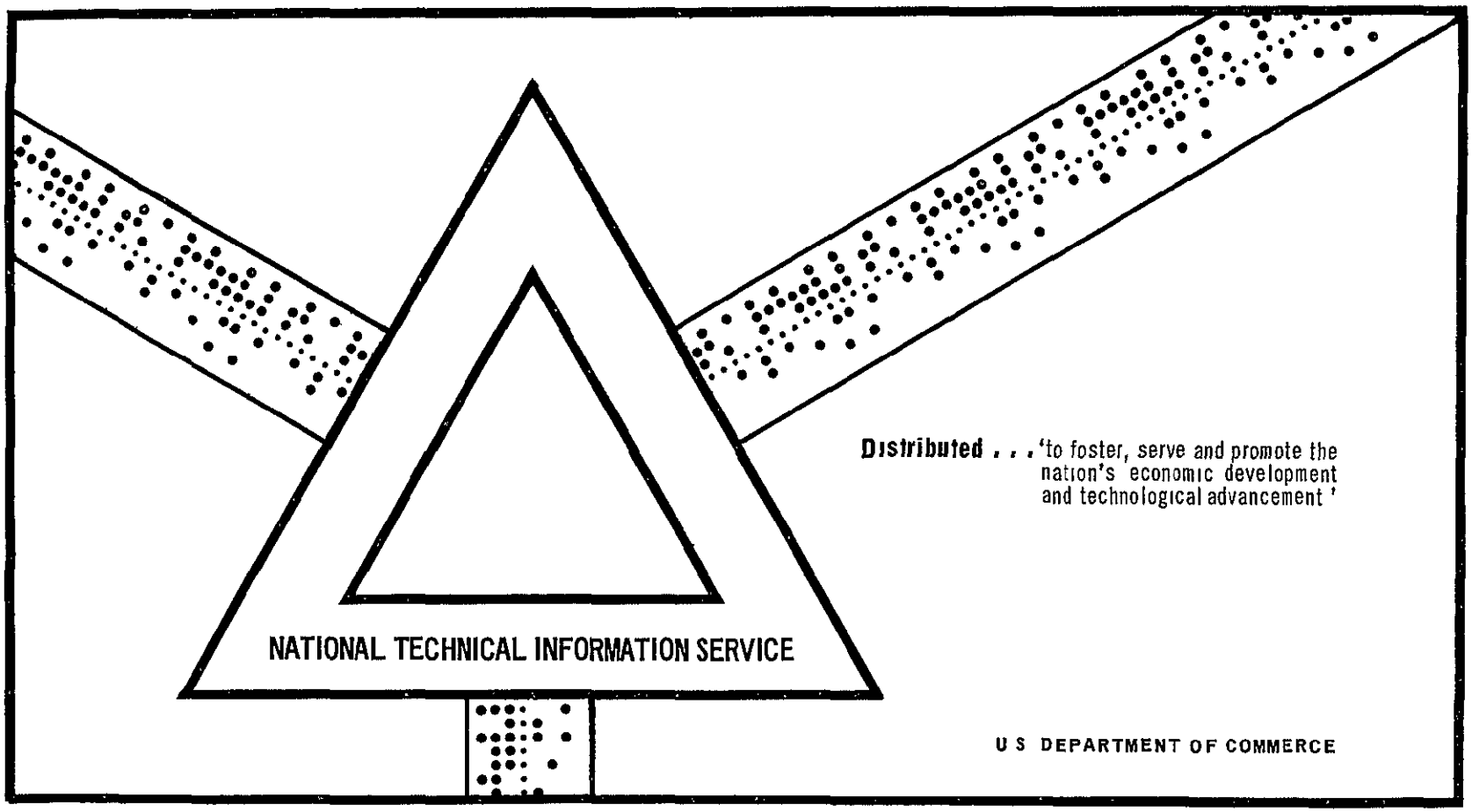
N71-25391

# STUDY TO DEVELOP PROCESS CONTROLS FOR LINE CERTIFICATION ON HYBRID MICROCIRCUITS

R. A. Rossmeisl, et al

Electronic Communications, Incorporated
St. Petersburg, Florida

1971



CR-103126

# STUDY TO DEVELOP PROCESS CONTROLS FOR LINE CERTIFICATION ON HYBRID MICROCIRCUITS

FINAL REPORT
COVERING THE PERIOD
OF
NOVEMBER 1970 TO FEBRUARY 1971


**ELECTRONIC COMMUNICATIONS, INC.**
**A SUBSIDIARY OF NCR**


SYSTEM DEVELOPMENT
COMMUNICATIONS
DATA LINK
DATA PROCESSING
ANTENNAS
MULTIPLEXERS


ST. PETERSBURG, FLORIDA

# STUDY TO DEVELOP PROCESS CONTROLS FOR LINE CERTIFICATION ON HYBRID MICROCIRCUITS

CONTRACT NO. NAS 8-26381

FINAL REPORT
COVERING THE PERIOD
OF
NOVEMBER 1970 TO FEBRUARY 1971

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# SECTION I

# INTRODUCTION

1.1 Scope. This report will set forth the basic process steps utilized by the contractor in the fabrication of thick or thin film hybrid microcircuits and the measurements, tests and inspections required to maintain consistent control of these process steps. The testing methods, tolerances and inspection criteria are based on proven experience in pilot and low volume production of high reliability hybrid microcircuits. Remedial action procedures will be indicated in the event tolerances are exceeded.

Because the intent of this contract is to determine a means of obtaining reasonable assurance by NASA that a vendor's line can consistently produce reliable hybrid microcircuits as may be required in long term space applications, the all welded device-in-carrier fabrication scheme will form the basis of this report.

1.2 Purpose. The purpose of this report is to help develop documentation for a program of line certification based on process controls for producing thin and thick film hybrid microcircuits for NASA use.

1.3 Referenced Documents

ECI Process Specification Documents

| | |
|---|---|
| 49-00170 | Cleaning |
| 49-00171 | Thin Film Thermal Evaporation |
| 49-00173 | Thin Film Photo Fabrication |
| 49-00174 | Thick Film Screening |
| 49-00175 | Sizing, Drilling & Trimming |
| 49-00176 | Discrete Component Bonding |

ECI Process Specification Documents (Cont)

| | |
|---|---|
| 49-00177 | Bonding of Electrical Connections |
| 49-00178 | Sealing |
| 49-00179 | Pincher Bonding |
| 49-00191 | Thick Film Circuit Soldering |
| 49-00198 | Hermetic Seal Testing |

ECI Materials Specification Documents

| | |
|---|---|
| 22-00322 | Thick Film Paste |
| 48-00108 | Substrate Material, Ceramic |
| 48-00109 | Deposition Material |
| 31-00273 | Electrical Interconnect Wire |
| 22-00347 | Adhesives, Epoxy |

ECI Inspection Instructions

| | |
|---|---|
| 171.300 | Controlled Environment Work Areas |
| 171.000 Section 9.02 | Q.C. Instructions |
| 171.000 Section 10.0 | Calibration Instructions |

## 1.4 General Requirements for Line Certification for Hybrid Microcircuits

1.4.1 State-of-the-Art. The vendor should give evidence that the requirements invoked in a line certification program are being regularly met and that further research or development is not necessary.

1.4.2 Engineering Change Notice. The vendor should supply a copy of the Engineering Change Notice procedure in current use, the form of the Notice and advise NASA of any notice in effect.

1.4.3 Route Ticket. The vendor should prepare and use a route ticket for each microcircuit module. This ticket should show as a minimum the following information.

a. Operation
b. Date
c. Reading
d. Scrap
e. Operator's Name
f. Substrate Identification.

This route ticket, in use by ECI, is shown in Figure 1-1. It has also been found useful to use a route ticket for each circuit substrate (see Figure 1-2) which is attached to the appropriate module ticket.

1.4.4 Handling of Substrate and Parts. The vendor should show evidence of careful handling of substrates and parts throughout the production cycle. Substrates may be handled by tweezers or other handling devices provided care is used to avoid touching the substrate area used for circuitry. No excessive cracking, breaking or other defects should occur at the substrate periphery. Tweezers or other handling devices may be used to handle parts provided that nicks or other excessive damage to transformer wires, insulation on wires, plating on leads, chipping of ceramic capacitors or other material, damage to lead wires and active devices such as transistors or diodes does not occur. Damage should be recorded on a route ticket so that an operation or an operator with a significant loss rate can be identified. The vendor should show evidence that persons responsible for significant damage or loss receive remedial instruction. Any action necessary to improve handling procedures should be taken expeditiously.

1.4.5 High Purity Water. High purity water should be used in any operation which requires a critically clean surface. In most instances in hybrid microcircuit processing, its use is desirable but not necessary. ECI uses

a high purity water rinse just prior to thin film deposition and the specifications it must meet are detailed in Data Sheet 2.3-2.

Where rinsing operations are not critical, deionized water obtained by filtering public drinking water supplies with a suitable ion exchange column has been found satisfactory.

1.4.6 Processing Environments. The ECI microcircuit assembly, vacuum deposition and photoetching facilities are controlled environment work areas (clean rooms) and the specifications are documented under ECI Quality Assurance Policy No.171.300.

In general these areas must have.

a. A maximum humidity no greater than 50 percent at room temperature

b. An airborne particle count of less than 300 particles per cubic foot of a size 5 micron or greater.

c. A temperature in the range of 72 ±10 degrees Fahrenheit.

Clean room pressure is maintained above that of surrounding areas and environmental conditions such as temperature, humidity, pressure differential and airborne particle count are inspected and recorded periodically. Documentation for environmental control and instructions for corrective action have been established.

The entire thick film process work area is not in a controlled environment as such but periodic measurements indicate the quality of the environment is nearly equal to the microcircuit assembly areas. All

critical operations in this area and in the entire microelectronics facility are carried out in laminar flow hoods.

1.4.7 Location. The vendor should provide necessary information to locate each process step that is certified. Moving a process step to another location should require approval or recertification.

1.4.8 Documentation. The vendor should prepare and maintain documentation which sets forth the materials, procedures, calibration, techniques, measurements, tests, inspection, safety rules, equipment and apparatus with necessary tolerances used in current fabrication and quality assurance functions for each of the basic process steps. The applicable ECI documents are listed in Section 1.3.

1.4.9 Failure Analysis. The vendor should maintain an effective failure analysis program and perform analyses as required to maintain control of the various processes utilized.

## 1.5 ECI Hybrid Microcircuit Process Flow Chart

### 1.5.1 Basic Process Steps Requiring Certification

a. Inspection of Incoming Materials (#1)
b. Mask Preparation (#2)
c. Thin Film Deposition (#3)
d. Photoetching (#4)
e. Thin Film Deposition (#5)
f. Discrete Component Assembly (#6)
g. Electrical Lead Bonding (#7)
h. Preseal Visual Inspection (#7.4)
i. Sealing (#8)
j. Electrical Testing (#9)

# ELECTRONIC COMMUNICATIONS INC.

## PRODUCTION AND INSPECTION TEST

SP 215 REV 10 65

LABOR CHARGE
W/O &
LOT NO._____

SERIAL NO. _____

PART NO. _____ NAME _____

E.C N. CONFIG. _____

M O. NO _____ PROJECT _____

| INSP. TEST DEFECT | DATE | OPR NO | OPER STAGE OR DEFECT | INSP | TEST |
|---|---|---|---|---|---|
| | | | | | |
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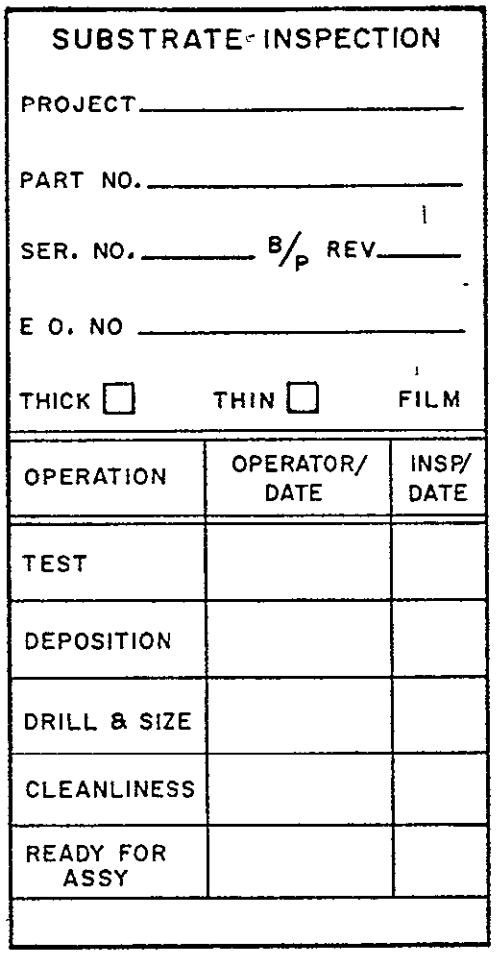
UNIT —

FIGURE 1-1

S/N —

ASSEMBLY



SUBSTRATE INSPECTION

PROJECT _____

PART NO. _____

SER. NO. _____ B/P REV _____

E O. NO _____

THICK ☐ THIN ☐ FILM

| OPERATION | OPERATOR/ DATE | INSP/ DATE |
|---|---|---|
| TEST | | |
| DEPOSITION | | |
| DRILL & SIZE | | |
| CLEANLINESS | | |
| READY FOR ASSY | | |

FIGURE 1-2.

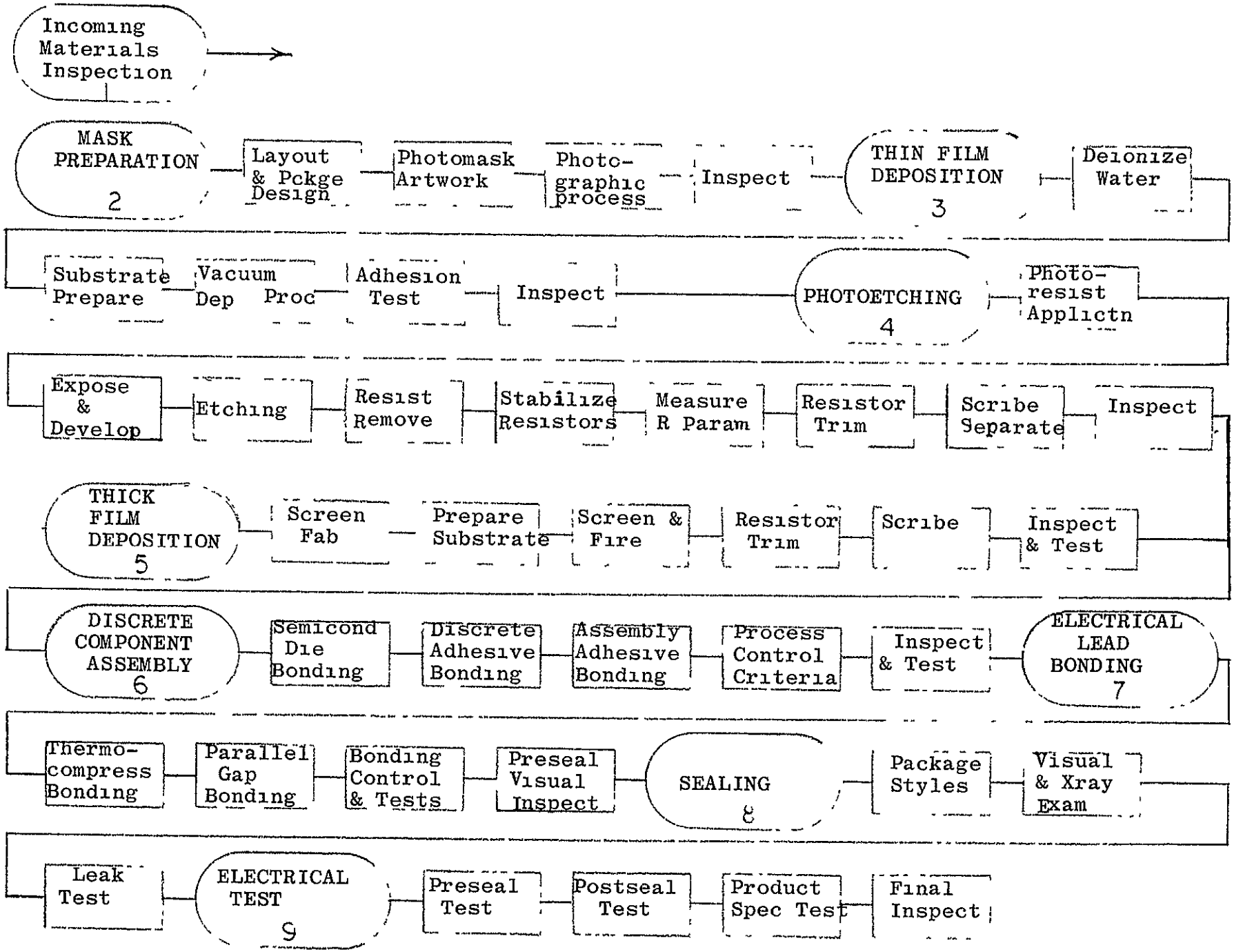



FIGURE 1-3. ECI HYBRID MICROCIRCUIT PROCESS - FLOW CHART

# SECTION II

# PROCESS CONTROLS IMPOSED BY ECI ON BASIC PROCESS STEPS

## 2.1 Inspection of Incoming Materials

2.1.1 Ceramic Substrates. ECI evaluates incoming ceramic substrate material for adequate packaging, identification and for required documents such as Certification of Conformance and physical/chemical analysis. See ECI Specification 48-00108.

Visual inspection is performed on a sampling basis (4.0% AQL) by viewing under a 3X maximum magnification viewer and normal room light illumination at all angles for material imperfections. Examples of imperfections evaluated are as follows pits .007 inch diameter or greater on unglazed surfaces, .005 inch diameter or greater on glazed surfaces, scratches .007 inch or greater in depth on unglazed surfaces and .005 inch or greater in depth on glazed surfaces.

Dimensional inspection is performed on a sampling basis (4.0% AQL) on size and thickness requirements as specified by the print. Electromechanical and mechanical comparators such as micrometers having accuracy ratios of 4.1 and 10.1 are used to obtain actual measurements.

Camber/warpage-to-print requirements of .004 inches per inch maximum except for substrates 1/2" x 1/2" or less which have .002 inches maximum tolerance are checked 100% between two parallel planes that are controlled by precision gage blocks and/or wires having known sizes and tolerances.

Glazed substrates for thin film deposition are inspected further for surface defects by means of a phase contrast interferometer as described in Data Sheet 2.1-1.

2.1.2 Deposition Material. ECI evaluates all deposition materials for adequate packaging, identification and required documentation such as Certification of Conformance and physical/chemical analysis. See ECI Specification 48-00109.

All questionable materials are forwarded to a qualified laboratory for evaluation on ECI form SP 113.

Dimensional inspection is performed on one piece from each lot of material received in order to verify size and thickness requirements in accordance with print specifications. Micrometers and vernier calipers having an accuracy ratio of 4:1 are utilized for measurements.

Before use, the nichrome deposition charges are weighed on a laboratory double pan balance to within 5 percent of a specified mass.

2.1.3 Thick Film Paste. ECI evaluates all paste containers for adequate packaging, identification and required documentation such as Certification of Conformance, physical/chemical analysis, lot control and age control data in accordance with print requirements. See ECI Specifications 22-00322, 00323, and 00324.

All questionable material and/or containers are forwarded to a qualified laboratory for evaluation on ECI form SP 113.

2.1.4 Electrical Interconnect Wire. ECI evaluates each lot of wire for individual spool packaging in a plastic enclosed container that provides protection against shock, vibration, and temperature extremes. Bar/melt numbers, wire size, values of elongation, tensile strength, lot number, purchase order number and part number are also verified.

Material analysis and inspection reports are reviewed to determine conformance of wire characteristics such as elongation (1 to 4 percent

for 31-00273-001 wire), tensile strength (2.7 min grams for 31-00273-001 wire), composition (gold 99.99 percent and stress relieved 2 ±1 percent for 31-00273-001 wire) in accordance with applicable print specifications.

Wire size and thickness are checked on all samples provided with each lot received. Inspection normally utilizes a Unitron Universal Measuring Microscope - Model TMD 3455 magnification to 400X to obtain measurements.

All wire is sent to the Microelectronics Laboratory on ECI form SP 113 for contamination tests.

2.1.5 Adhesives (Microelectronics). ECI evaluates all adhesive containers for adequate packaging, identification and required documentation such as Certification of Conformance, physical/chemical analysis, lot control and age control data in accordance with print requirements. See ECI Specification 22-00347 as an example.

2.1.6 Ceramic Capacitors (Unencapsulated). Vendor Material Inspection performs visual inspection in accordance with established sampling procedures to ensure device compliance with applicable specifications. Visual inspection is normally performed with the aid of up to 10X magnification and consists of examination for such criteria as scratches, chips, voids, metallization defects or edge chips, as well as physical compliance with the product specification. Electrical inspection is performed in accordance with established sampling procedures to ensure device compliance with the applicable specifications. Electrical inspection normally consists of measurement of the following parameters.

a. Capacitance and Dissipation Factor.

1. Devices with a capacitance value of 100 pF or less shall be measured at a test frequency of 1 MHz ±1 kHz on a Micro Instruments Model 1212 Capacitance Tester or equivalent.

D. C. bias shall be applied as required from an external source such as a Harrison Model 6116A.

2. Devices with a capacitance value of greater than 100 pF shall be measured at a test frequency of 1 kHz ±100 Hz on a General Radio Type 1680 Automatic Capacitance Bridge or equivalent. D. C. bias shall be applied as required from an external source such as a General Radio Model 2995-9149 Bias Supply.

b. Dielectric Withstanding Voltage. Devices shall be measured to ensure compliance with applicable specifications. A test voltage normally of 2.5 times the rated voltage shall be applied and leakage current measured.

c. Insulation Resistance. Devices shall have a voltage applied to them in accordance with the product specification and the insulation resistance shall be measured by means of equipment such as General Radio Megohmmeter Model 1862-B or equivalent.

d. Burn-In. Devices shall be burned-in for a period of time in accordance with applicable specifications. This burn-in shall be conducted at the maximum operating temperature ±5°C and at 200 percent of the rated working voltage specified in the product specification. The devices shall be electrically tested after burn-in to ensure parameter changes are within the range of the applicable specification.

2.1.7 Resistors (Microelectronic). Resistors shall be visually inspected in accordance with established sampling procedures to ensure device compliance with applicable specifications.

a. Visual inspection shall normally be performed with the aid of magnification and shall consist of examination for defects such as:

1. Scratches or voids
2. Corrosion defects

3. Metallization defects
4. Foreign material
5. Chips
6. Physical noncompliance with product specification.

b. Electrical inspection shall be performed in accordance with established sampling procedures to ensure device compliance with the applicable specifications. Electrical inspection shall normally consist of the measurement of resistance using equipment of sufficient accuracy such as General Radio Model 1652A Resistance Limit Bridge, Industrial Instrument RN-1 Wheatstone Bridge, or ESI Model 242B Precision Resistance Measuring System.

c. Burn-In. Devices shall normally be burned-in for a period of time in accordance with applicable specifications. This burn-in shall be conducted at an operating temperature and under load conditions as specified in the applicable specification.

The devices shall be electrically tested after burn-in to ensure parameter changes are within the range of the applicable specification.

2.1.8 Inductors. Inductors shall be visually inspected in accordance with established sampling procedures to ensure device compliance with applicable specifications.

a. Visual inspection shall normally be performed with the aid of magnification and shall consist of examination for defects such as:

1. Scratches or voids
2. Corrosion defects
3. Bridged metallization defects
4. Metallization defects
5. Foreign material

6. Chips
7. Physical noncompliance with product specification.

b. Electrical inspection shall be performed in accordance with established sampling procedures to ensure device compliance with the applicable specifications. Electrical inspection shall normally consist of the measurement of such parameters as inductance and "Q" using equipment of sufficient accuracy such as Boonton Model 260 Q Meter, General Radio Model 1630 Inductance Measuring Assembly, or Boonton Model 190 Q Meter.

c. Burn-In. Devices shall normally be burned-in for a period of time in accordance with applicable specifications. This burn-in shall be conducted at an operating temperature and under load conditions as specified in the applicable specification.

The devices shall be electrically tested after burn-in to ensure parameter changes are within the range of the applicable specification.

2.1.9 Active Device Chips. Active device chips shall be visually inspected in accordance with established sampling procedures to ensure device compliance with applicable specifications. Visual inspection will normally be performed with the aid of a minimum of 50X magnification and shall consist of examination for the following defects:

a. Scratches or voids
b. Metallization corrosion defects
c. Bridged metallization defects
d. Metallization alignment
e. Metallization defects
f. Exposed junctions
g. Contact cuts
h. Cracks

i. Edge distance on scribed chips

j. Oxide and diffusion faults

k. Gross undercutting

l. Foreign material.

2.1.10 Active Devices in Carriers. Active devices in carriers shall be visually inspected in the same manner as active device chips. Examination shall also be made for the following additional defects.

a. Carrier Defects

1. Flaking or blistering of plating
2. Cracks, chips, or scratches
3. Excessive gold eutectic material
4. Die position on carrier.

b. Bonding Defects

1. Overlapping bonds
2. Bond placement on pad
3. Missing or broken bonds or leads
4. Off center ball bonds
5. Pigtail length
6. Bonding pads showing evidence of horizontal force
7. Bond over bond or more than one bond attempt per pad
8. Twists, nicks, crimps, or scoring of leads
9. Taut leads between ball bonds
10. Ball bond size
11. Stitch bond placement.

c. Electrical tests on active devices in carriers shall be performed in accordance with established sampling procedures to ensure device compliance with the applicable specification. Electrical parameters measured shall normally be as described in the following

paragraphs. If a burn-in is performed, electrical parameters shall normally be measured both before and after burn-in to ensure parameter changes are within the range of the applicable specifications.

1. Transistors. Transistors shall normally be tested on the Fairchild 600 Semiconductor test system. Any of the following parameters may be tested in accordance with conditions given on the product specification: $I_{CBO}$, $I_{EBO}$, $I_{CEO}$, $I_{ECO}$, $I_{CER}$, $I_{CES}$, $BV_{CBO}$, $BV_{EBO}$, $BV_{ECO}$, $BV_{CEO}$, $BV_{CER}$, $BV_{CES}$, $H_{FE}$, $V_{BESAT}$, $V_{CESAT}$, $V_{BE\ ON}$.

Burn-in shall be conducted with the devices in a dry nitrogen atmosphere. Devices shall be operated at the maximum rated power and with current and voltage levels as specified in the product specification. The ambient temperature, duration time of burn-in and power pulse cycle schedule shall be as specified in the applicable specifications.

2. Signal Diodes and Rectifiers. These devices shall normally be tested on the Fairchild 600 Semiconductor test system. Any of the following parameters may be tested in accordance with conditions given in the product specifications. Forward Voltage, Forward Current, Breakdown Voltage, Reverse Current.

Burn-in shall be conducted with the devices in a dry nitrogen atmosphere. Signal diodes shall be operated at the maximum rated power for 240 hours minimum at an ambient temperature of 25°C. Rectifiers shall be burned-in for 240 hours minimum at an ambient temperature of 25°C with working peak reverse voltage and maximum forward rectifier current as specified in the product specification and applied to the device at a rate of 60 Hz AC.

3. Zener Diodes. These devices shall normally be tested on the Fairchild 600 Semiconductor test system, or on the Fairchild 5000 Integrated Circuit test system if a requirement exists for accurate control of a soak time prior to measuring device parameters. Any of the following parameters may be tested in accordance with conditions given in the product specification: Reverse Current, Forward Voltage, Forward Current, Zener Voltage.

Burn-in shall be conducted with the devices in a dry nitrogen atmosphere. Devices shall be operated at maximum power for 240 hours minimum at an ambient temperature as specified in the applicable specification.

4. Field Effect Transistors. These devices shall normally be tested on the Fairchild 600 Semiconductor test system, the Fairchild 5000 Integrated Circuit test system, or the Tequipco Model 1-12 Field Effect Transistor Tester. Any of the following device parameters may be tested in accordance with conditions given in the product specification: IDSS, IGSS, BVGDS, Vp, ID, VGS, gm.

Burn-in shall be conducted with the device in a dry nitrogen atmosphere. Devices shall be operated for 240 hours minimum at an ambient temperature as specified in the applicable specification. For MOS devices, 80% of the maximum rated drain-to-source voltage shall be applied with the gate and source terminals connected to ground. For junction FET's, 80% of the maximum rated gate to source reverse voltage shall be applied with the gate connected to ground and the drain and source connected together.

DATA SHEET 2. 1-1

PROCESS STEP. Inspection of Incoming Materials
Interferometer Examination

DESCRIPTION OF PROCEDURE. Visual examination of glazed aluminum oxide substrate surface with a phase contrast interferometer to determine if excessive pits, scratches, or glaze defects exist.

FREQUENCY OF TEST: Upon receipt of any new batch of glazed substrates.

SAMPLE SIZE· Random check of two out of every twenty-five units.

MEASURING INSTRUMENT. Reichert Research Microscope NR 324-945. with Nomarski Phase Contrast attachment.

ACCURACY IN PERCENT. Operator judgement to within 200 Å.

LIMITS OR TOLERANCES. Any pits, cracks, excess materials, scratches, discoloration, or indentations visible under magnification.

DATA RECORDING METHODS. Visual examination of new substrate on a go-no-go basis. Upon discovery of excessive defects entire batch could be rejected. Quality is mentioned on data sheet.

CALIBRATION PROCEDURE. ECI Calibration Department annual check.

ACTION TAKEN IF TOLERANCES ARE EXCEEDED. Rejection of piece under observation, careful examination of all pieces in same batch.

2.2 Mask Preparation. Mask preparation begins with a topology layout which by its nature establishes the geometrical characteristics of a microcircuit. Also important decisions about terminal metallization, bonding methods and materials, package concept, and device selection must be made, before proceeding with a layout. To prevent making decisions that result in unreliable microcircuits, design guidelines should be established and adhered to. As part of a Line Certification Program these guidelines should be published and available for review.

2.2.1 Topology Design for Channel Carrier Microcircuits. The use of ceramic carrier devices such as channel carriers offer some design advantages over other microelectronic packaging approaches for high reliability microcircuits.

a. A single conductor may be run under a carrier, saving space and number of crossovers required.

b. The artwork does not have to be critically taped as with flip chips, saving time and photographic effort.

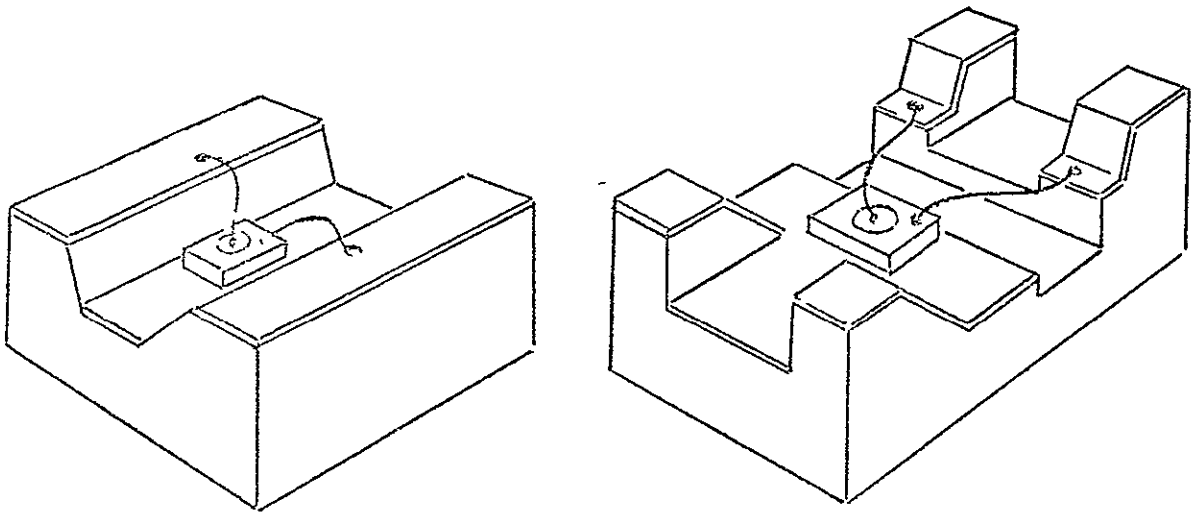
c. Circuit density is optimized.

d. All discrete parts may be screened by burn-in prior to assembly.

A number of channel carrier configurations are available, the two basic types being U-channel and leadless inverted devices (LIDS) as shown in Figure 2-1.

The selection of a carrier is based on the number of leads required, the chip size and metallization and reliability of the carrier approach.

The metallized terminal pad area of a carrier must be at least 5 mils square and 150 micro inch thick and be capable of being bonded by



U-Channel

Leadless Inverted Device
(LID)

Figure 2-1.

thermocompression, ultrasonic or parallel-gap bonding techniques using .001 inch or larger nominal diameter, gold or aluminum wire.

Lids that are used in a solder assembly must be capable of accepting solder and have protection for the device during soldering operations.

Once the decision has been made to use channel carriers, the next question which arises is whether to use thin film or thick film. Some physical comparisons between the two systems are listed in Table 2-1.

Thin Film

a. Conductors. Excellent line definition is obtained by photoetch techniques.

Crossovers are difficult to produce with thin film systems; therefore, circuit layout must be made accordingly. Where crossovers are required,

TABLE 2-1.

| Circuit Requirements | Thick Film | Thin Film |
|---|---|---|
| 1. Frequency | Resistor Application Normally up to 100Mhz | Up to and including S band |
| 2. Resistivity Range | Conductors: .001 to .1Ω/square<br>Resistors: 50 to 1 MegΩ/square | Conductors: .01 to .1Ω/square<br>Resistors: 50 to 500 Ω/square |
| 3. Resistor Material | Ruthenium Base | Nichrome |
| 4. Resistor Initial Tolerance | ±10% as fired<br>± 1% matching | ±5% as deposited<br>±.1% matching |
| 5. Resistor Close Trimming | ± .5% | ± .1% |
| 6. Resistor Line Width | .015 Min. (Power Dependent)<br>.020 Std. | .005 Min. (Power Dependent)<br>.010 Std. |
| 7. Power Dissipation | Up to 60W/in.$^2$<br>25W/in.$^2$ - Std. | Up to 60W/in.$^2$<br>15W/in.$^2$ - Std. |
| 8. Resistor TCR | < 100 PPM/°C | < 50 PPM/°C |
| 9. Conductor Material | Au, PdAu, PtAu<br>PdAg, Ag. | Au/Mo, Al, Ta, Cu |
| 10. Conductor Current Limit | Au-25MA/mil width<br>PdAu-8MA/mil width | Au, Al) -- 2.5MA/mil$_{width}$ |
| 11. Conductor Line Widths | .002" Minimum<br>.010" Standard | .0001" Minimum<br>.005" Standard |
| 12. Conductor Spacing | .002" Minimum<br>.010" Standard | .002" Minimum<br>.010" Standard |
| 13. Electrical Bonding Methods | | |
| Ultrasonic Wire | Good | Excellent |
| Parallel Gap | Good | Excellent |
| Solder | Excellent | Good |
| Thermocompression | Excellent | Excellent |
| Die Attach (U.S.) | Good | Good |
| Die Braze | Excellent | Good |
| Flip Chip | Good | Good |
| Beam Lead | Excellent | Good |
| 14. Discrete Components Availability | Excellent | Excellent |
| 15. Reliability | Excellent | Excellent |
| 16. Large Quantity Producibility | Excellent | Good |

it can be accomplished by running a conductor under a carrier or next to it and the flying lead from the carrier will crossover the same conductor. See Figure 2-2. Silastic or other silicone material may be used for insulation to prevent shorting of flying leads.

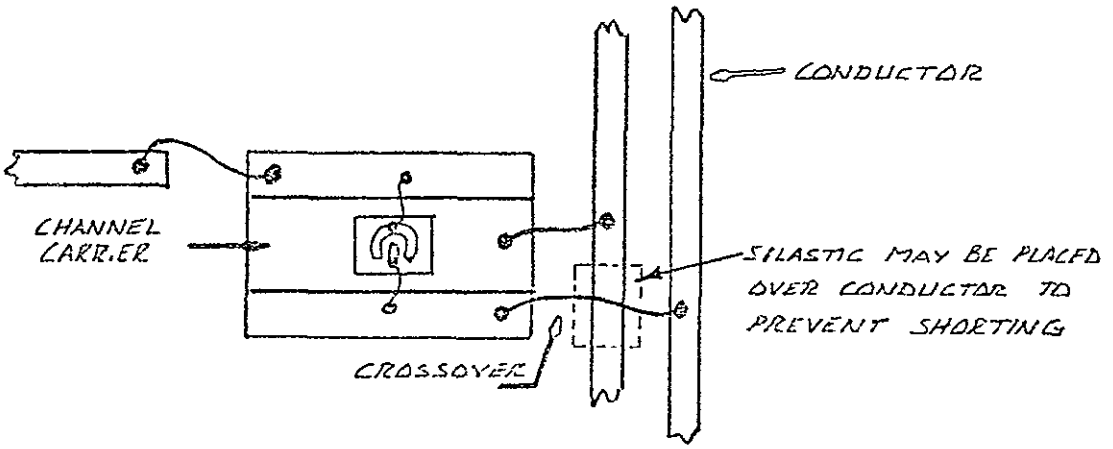



Figure 2-2.

Deposited thin film conductors have a nominal sheet resistivity of .60 Ω/ square for gold or aluminum at a thickness of 600 Å.

b. Resistors. Thin film resistors can be designed in a meandor pattern with trim bars where possible. Trim bars are added to the resistor for removal in increments of 1%, 2%, and 5%. For extremely close tolerance resistors an edge trim is used. See Figure 2-3.

The minimum width of a resistor is determined by the equation

$$W \text{ min} = \left( \frac{\rho P}{KR} \right)^{1/2}$$

where:
- $\rho$ = Sheet resistivity in Ω /square.
- P = Power to be dissipated by resistor in watts.
- K = Substrate power capability in watts/sq.in.
- R = Resistance in ohms.

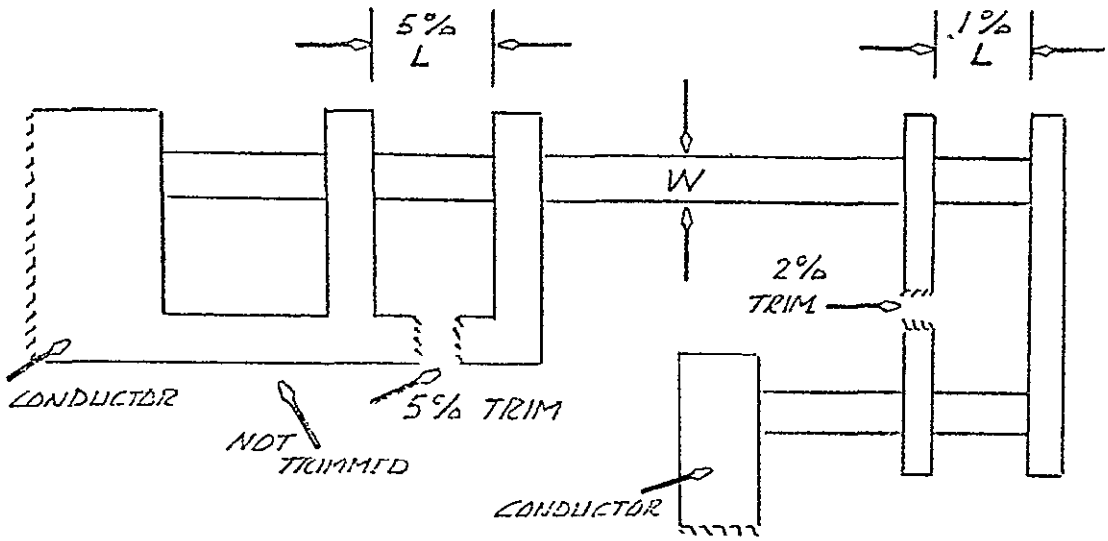



Figure 2-3.

The length of a resistor is calculated by the equation:

$$L = \frac{RW}{\rho}$$

Where W is the width of the resistor $\geq$ W min and no smaller than 5 mils

For considerations of line widths and spaces, see Table 2-1.

c. Reference Designations. Wherever space is available, components will be identified by reference designations. These reference designations will be placed on the resistor pattern if one is used.

Thick Film

a. Conductors. Since thick film processing is a screen and fire process, line definition is not as good as that of thin film. However, with care line widths and spacings of .002" may be obtained without shorts or opens.

Thick film systems offer a major advantage over thin film in the form of multilayer capabilities. Multilayer interconnect circuitry is accomplished by sequentially screening and firing conductor and dielectric material to form the required conductor and insulation path as shown in Figure 2-4.

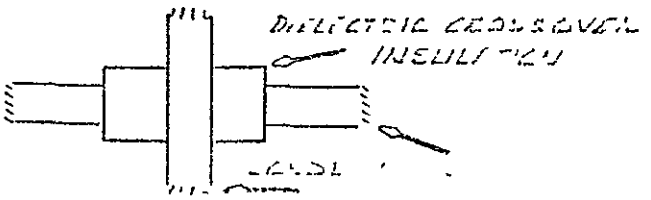


Figure 2-4.

The average "as fired" conductor sheet resistivities for thick films are .001 Ω/square for gold and .01 to .1 Ω/square for palladium and platinum gold.

b. Resistors. Thick film resistors can be designed in a straight line edge trim pattern or a "top hat" middle trim pattern as shown in Figure 2-5.

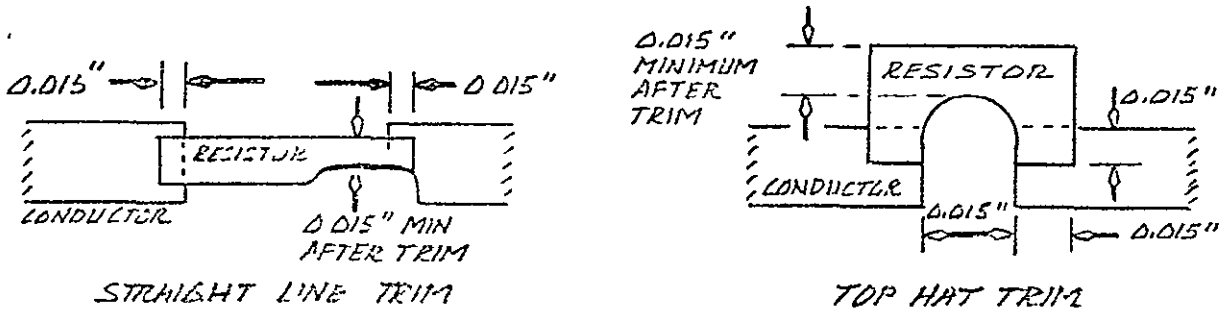



Figure 2-5.

Resistor trimming is accomplished by air abrasive removal of material to bring the resistor to value. Tolerance of ±5% or greater

can be accomplished in an "as fired" condition without necessity of physical trimming.

The minimum width of resistor after trimming is determined by the equation:

$$W \text{ min} = \left(\frac{\rho P}{KR}\right)^{1/2}$$

where:
- $\rho$ = Sheet resistivity in $\Omega$/square.
- P = Power to be dissipated by resistor in watts.
- K = Substrate power dissipation capabilities in watts/square inch.
- R = Resistance in ohms.

The length of a resistor is calculated by the equation:

$$L = \frac{RW}{\rho}$$

where W = Width of the resistor $\geqq$ W min.

A minimum overlay or termination interface of .015" is used for resistor design to maintain resistor predictability.

The after trimming resistor dimensions used for design purposes are given in Figure 2-5.

For "as fired" resistors where no physical trimming is desired, a minimum size of .020 wide by .020 long is used to ensure electrical characteristics.

For consideration of line widths and spaces, see Table 2-1.

## Selection of Discrete Components

Components that cannot be designed into the circuitry must be mounted on a channel carrier or mounted individually and electrical connections made to them. In selection of these discrete components the first considerations are electrical characteristics, then size.

Termination materials must be compatible with the fabrication and assembly processes.

Other considerations are availability by more than one vendor, reliability, size, and cost. Discrete components are tested at incoming inspection and again before and after assembly.

## Metallization Compatibility

The termination metallization of most channel carriers is gold, therefore, the conductor or pad material must be compatible. Electrical connections are normally made with .001" diameter or larger gold wire, thermocompression bonded to carrier bonding pad and to conductor or pad on the substrate.

Component interconnect circuitry can be either thick or thin film gold or aluminum for T.C. bonding and parallel gap welding. Solder or die braze assemblies require gold thin film or gold and its alloys for thick film metallization.

Package leads extending external to the package must have a metallization compatible with the discrete component bonding method used for the rest of the assembly.

The termination metallization on channel carriers is usually large enough so that more than one bond can be made to it. Sufficient pad or conductor area should be available so that if one bond attempt fails, another can be made.

Channel carriers are normally attached to the substrate with epoxy. Care must be taken to ensure that they can be removed and replaced easily without destroying the interconnect circuitry.

Where reliability is critical, redundant bonding is usually required.

No more than one conductor line may run under a carrier. Some epoxies have a tendency to support electrolytic corrosion at elevated temperatures where conductors of different potentials pass through it. Failures can result in the form of opens and shorts.

Component-to-component bonded connections when possible are preferred to component-to-substrate bonds, as the total number of bonds is reduced significantly.

Optimum Package Size

Substrates should be designed to achieve optimum package size. This can generally be done by making the layout as small as possible. Some techniques are.

a. Make the layout in accordance with the flow of the circuit schematic so conductor lengths are as short as possible.

b. Select minimum size carriers and discrete components.

c. Design resistors as small as possible.

d. Select a package that fits substrate configuration as well as the space the package must fit into.

e. Calculate the minimum substrate area required to dissipate the power required. This should include thermal conductivity of the entire package.

f. Consider electric parasitic problems and make layout accordingly. At low frequencies, conductor sizes are determined by D.C. current capabilities. At high frequencies, conductor sizes and geometries are determined by stray capacitance and inductance. For current carrying capabilities of conductors, see Table 2-1.

General Guidelines

The following general rules may be used to improve the quality and reliability of a hybrid package.

a. Crossovers of conductors should be kept at a minimum.

b. Components should be placed parallel to the edges of a substrate whenever possible.

c. Resistors should be placed so that they can be readily trimmed (resistors should be designed to exclude trimming if possible).

d. Bonding pad areas for a thermocompression bond must be at least 10 mils square and parallel gap bonding should be a minimum of 35 x 30 mils.

e. Maximum length of an unsupported wire should be .100 inch.

f. Dielectric dams should be used in areas to be soldered or die brazed so that migration of material does not occur.

g. A hybrid package using channel carriers must be hermetically sealed.

h. Holes in the substrates should be avoided. If holes are necessary, the following rules should apply·

1. The edge of a hole must be at least .030" from the edge of the bonding pad.

2. The edge of a hole should be placed on the edge of the bonding pad.

3. Hole diameters should be at least 1-1/2 times the size of the wire or ribbon.

i. Conductors shall be placed no closer than 10 mils from the edge of a substrate.

j. Reference designations and orientation marks shall be used whenever possible.

k. Avoid as many resistor and conductor right angle turns as possible.

2.2.2 Artwork Preparation. After the topological design is complete it must be translated into camera-ready artwork. Drafting techniques are used to make an outline of the positive areas of the circuit. Red transparent tape with a tolerance on the width of ±.001 is used to block out the positive pattern. Taping is done on matted mylar sheets .004 to .007 inches thick to provide a stable base. Trimming where necessary is accomplished with a surgical-type knife, using care not to make knife marks in the mylar. Whenever large amounts of opaquing are required, Rubylith or Amberlith cut and strip material may be used.

Registration marks and photographic reduction marks are placed on the artwork. In addition to a title block for artwork identification, component identification is included to expedite assembly operations.

2.2.3 Inspection of Microcircuit Photographic Film. All exposed photographic film processed or obtained from outside sources by the ECI Engineering Photographic Laboratory for use in the fabrication of thin film or thick film microcircuits, will be inspected.

These include both the subtractive process utilizing a photo-resist/etch and the additive process using masks fabricated in conformance with the photographic image.

Inspection Method. All inspection of the photographic film or registration and pin holes shall be accomplished by placing the film in an open frame mask or a glassine envelope on a light table of a back-lighted stage. Film to be inspected for scratches will be removed from the glassine envelope and inspected without placing the film against any surface. Light table shall be cleaned with a lint-free cloth prior to use.

Magnification. Ten power (10X) magnification shall be used for inspecting circuitry, spacing, reduction, and registration. Higher magnification can be used for verification of questionable areas or checking di dimensions.

Inspection Characteristics. Film received for inspection shall be enclosed in individual protective covers to prevent damage to the film during handling and storage in various departments. The cover will contain an identification label.

Stable base photographic high resolution film of 0.004 to 0.010-inch thickness will be used, or high resolution glass plates. Film shall be so handled that scratches, fingerprints, or other contaminations are avoided.

Superficial scratches across the film are acceptable providing the contrast of the scratch is not great enough to be reproduced. There shall be no embedded particles in the film which may scratch the photo resist of the substrate, or the emulsion of the silk screen.

Thin Film Mask Inspection. Films for thin film application shall have the emulsion reading through the base of the film. See Figure 2-6 for limits and tolerances.

| | REGISTRATION * | MIN. CONDUCTOR WIDTH * | MIN. CLEARANCE BETWEEN CONDUCTOR PATHS * | JAGGED CONDUCTOR EDGES ** 0.002"-.010" Thin MAX 0.005"-.010" Thick | JAGGED CONDUCTOR EDGES ON CIRCUITRY OVER .010"WIDTH ** | RESISTOR PATH NOTCHES NOT TO EXCEED | REPRODUCIBLE DEFECTS NOT TO EXCEED **** | REPRODUCIBLE DEFECTS IN RESISTOR PATTERN NOT TO EXCEED |
|---|---|---|---|---|---|---|---|---|
| THIN FILM | 0.0002" | 0.002" | 0.003" | 0.0005" | 0.001" | *** 0.0005" | Black Area 0.002" --- Clear Area 0.0005" | 0.0001" |
| THICK FILM | 0.006" | 0.005" | 0.003" | 0.001" | 0.002" | 0.001 | Clear Area 0.002" --- Black Area none | None |

FIGURE 2-6. LIMITS AND TOLERANCES OF MICROELECTRONIC PHOTOGRAPHIC FILM

* Unless otherwise dictated by design

** Jagged edges of the maximum permissible size shall not exceed four peaks per linear half inch.

*** Combinations of flaws does not reduce the area by 10% of the designed width

**** The defects shall not reduce the clearance between circuit paths to less than 0.003 inch or 20% of the design clearance

DATA SHEET 2.1-1

PROCESS STEP.
Inspection of Incoming Materials
Inspection of Microcircuit Photographic Film

DESCRIPTION OF PROCEDURE Visual Inspection.

FREQUENCY OF TEST· Applies to all exposed photographic film prior to initial usage.

SAMPLE SIZE.

MEASURING INSTRUMENT: Bausch & Lomb Stereo Microscope 7X to 120X Magnification, equipped with reticle dimensioned in 0.001 inch. Nikos Comparator 12" Diameter - 10X - 31X - 100X Magnification with a 2" x 4", X-Y Micrometer Stage -- 0.0001 inch graduations.

ACCURACY IN PERCENT Accuracy is within a division of instruments.
LIMITS OR TOLERANCES As required by Customer Specifications, Drawings, and/or Inspection Instruction 171.000 Section 9.03.

DATA RECORDING METHODS· Daily Inspection Records and labels on Photographic Film is stamped by inspector when accepted.

CALIBRATION PROCEDURE. Instruments are calibrated in accordance with the Specified Calibration Schedule ECI Procedure 171.000 Section 10.

ACTION TAKEN IF TOLERANCES ARE EXCEEDED. Film is returned to Photographic Lab or Vendor, for correction.

Acceptance. Acceptance shall be indicated by stamping label with the round in-process stamp.

Defects. All defects found shall be circled with a Venus All Purpose Red, No. 1566 pencil on the glassine envelope.

Records. Inspection of the film, discrepancies and result will be listed in the Daily Inspection Record.

2.3 Thin Film Deposition. The objective of the controls imposed on the vacuum deposition of thin films for hybrid microcircuits at ECI is to obtain mechanically and electrically stable films on a stable substrate material that will result in no unpredictable changes in film characteristics through the remaining hybrid assembly steps and throughout a specified service life. Further, it is anticipated that hostile environments will be encountered during part or all of the required lifetime.

To obtain the desired performance, processes are developed, the components are tested and modifications to the processes are made. For example, at ECI many thousands of hours of environmental testing were required to establish the specifications shown in Figure 2-7 for the aluminum/nochrome deposition process.

Resistors

| | |
|---|---|
| Material | Nichrome V |
| Resistivity | 50 -250 Ω/sq. |
| Values | 10 Ω to 0.5MΩ |
| Tolerances | ±10% to ±0.1% with trimming |
| Temperature Coefficient | 25 ±25 ppm/°C |
| Operating Range | -55%°C to 125°C |
| Stability at 1000 hours | ±0.3% no load at 150°C |

Conductors

| | |
|---|---|
| Material | Aluminum |
| Resistivity | ≤ 0.1 Ω/sq. |

FIGURE 2-7. THIN FILM PASSIVE ELEMENT SPECIFICATIONS

Therefore, one of the first requirements for certification of this process step should be a detailed listing of the specifications that the deposited film components will meet along with evidence that the appropriate environmental evaluations have been performed.

To insure that these film specifications will always be met, ECI has documented control procedures at the most critical process steps. These key fabrication equipment specifications, test equipment specifications and inspection criteria are given on separate data sheets at the end of each section and are referenced in the text. A brief summary of each process step is given so that the control points can be referred to in a logical sequence.

2.3.1 Substrate Preparation. In fabricating thin film substrates, it is essential that compatible films are chosen for good adhesion to the substrate. It is also important that the substrates are cleaned to remove all contamination that would prevent chemical bonding between the film and the substrate. ECI's cleaning specification includes an initial ultrasonic cleaning in a detergent solution to remove gross contaminates. Following the ultrasonic cleaning is an immersion in a hot solution of ammonium hydroxide and hydrogen peroxide to remove any remaining organic films and inorganic contaminates. After chemically cleaning the substrates they are thoroughly rinsed in flowing deionized water as specified in Data Sheet 2.3-1. The final cleaning prior to deposition is in high purity water as described in Data Sheet 2.3-2 which is blown off with dry filtered nitrogen. The cleanliness of the substrates is tested by the water break test when they are removed from the high purity water.

A common processing problem is to keep the substrates clean during further processing. This is achieved through properly designed fixtures and

handling tools. Even after all precautions are taken to obtain clean substrates, there may be a chance of substrate recontamination. Therefore, it is important that a means be available for measuring film adhesion. ECI has developed a technique whereby the film adhesion is tested on each substrate. This is achieved by bonding a 0.006-inch gold wire onto the film and making a 90-degree pull test on at least three wires. See Data Sheet 2.3-1.

2.3.2 Vacuum Deposition Procedures. After the substrates are loaded into the evaporator, the metallization charges are placed in their specific crucibles and the system is sealed and ready for pumpdown. The type of material used for crucibles depends on the metallization desired. ECI uses high purity carbon crucibles for aluminum evaporation which minimizes the alloying effects of the molten metal. These high purity crucibles have low gas absorption properties which permit the evaporation chamber to remain at higher vacuum levels during evaporation. The higher vacuum levels allow deposition of nonporous, highly reflective and repeatable film structures. Other conductive films, such as gold, can be readily evaporated from copper crucibles with electron-beam guns. It is very important that the metal charge holders are designed and constructed from materials that will not evaporate along with the metal charge to form unknown and inconsistent film properties.

ECI developed a thin film technology using nichrome as the resistive film because of its electrical properties, stability and ease of fabrication into resistive elements. There are certain practices which must be followed when evaporating an alloy such as nichrome. During the sublimation of

the nichrome, the rate at which each element is deposited onto the substrate depends on the amount of charge remaining and the type of alloy charge. The nichrome charge mass is controlled to within five percent in weight and is replaced after each deposition run. These controls aid in achieving resistive films with consistent characteristics and are given in Data Sheet 2.3-4.

The vacuum level at which the evaporation is being performed affects the structure of the deposited films. To achieve aluminum films with good conductivity and consistent film structure the vacuum pressure must be monitored and held to a minimum of $5 \times 10^{-5}$ Torr during a deposition run. See Data Sheet 2.3-5. The evaporation is carried out with an electron-beam system as described in Data Sheet 2.3-6.

The substrates should be heated to a minimum temperature of 125 degrees C to remove any surface gases that might affect film adhesion. The charges and crucibles are outgassed by evaporating the charge material for a specified time with the shutter closed. The preevaporation step is an important one in reducing pin holes in the film and eliminating film nodules on the substrate caused by erupting gases.

After the substrates are preheated for a specified time, typically 30 minutes, and the charges are outgassed, the resistive film is deposited to a prescribed sheet resistivity such as 250 Ω/square. The film resistivity is measured and controlled by monitoring the film on the substrate or a separate monitor substrate. For close tolerance resistivity control, it is important that the monitor substrate have the

same surface composition and the same surface finish. If these films are to be used for the fabrication of circuits which were designed for a particular sheet resistivity, the monitor resistivity must be controlled to better than 1 percent in value. See Data Sheet 2.3-7.

The conductive film is deposited over the resistive film immediately after the latter deposition to provide the best possible film adhesion. The outgassed charges are evaporated to form highly conductive films with typical sheet resistances of 0.06 Ω/square for aluminum films. The conductive film thickness is controlled by monitoring the frequency shift of a crystal oscillator caused by the change as the film deposits on a piezoelectric crystal. This frequency shift, f, is related to the thickness, t, through the density, d, of the film material by $t = \frac{2 - f}{d}$. The required thickness of a film will depend on the application and the method of bonding to be used. ECI specifies a minimum thickness of 2500 Å when thermocompression bonds will be made to the films. See Data Sheet 2.3-8.

After the substrates are allowed to cool below 100 degrees C, they are removed from the evaporator and marked for identification. The identification code allows the substrate to be traced to the particular evaporation run and system in which the film was deposited. The freshly deposited substrates are then stored in precleaned plastic boxes ready for the next process. See Figure 2-8 for the Deposition Log Control Sheet.

DATA SHEET 2 3-1

PROCESS STEP Deionized Water Rinse
Barnstead Deionized Water Rinse Stations (3)

DESCRIPTION OF PROCEDURE A Barnstead #D0809 Mixed Resin Cartridge is used as a prefilter and ion exchange column to provide deionized water for routine rinsing. Parts to be rinsed are held in a container or holder and deionized running water is continually flushed over the part.

FREQUENCY OF TEST. N/A

SAMPLE SIZE. N/A

MEASURING INSTRUMENT. The cartridge lifetime is indicated by a lamp which glows when the water resistivity drops to 50,000Ω.

ACCURACY IN PERCENT Qualitative

LIMITS OR TOLERANCES A minimum of approximately 50,000Ω water.

DATA RECORDING METHODS N/A

CALIBRATION PROCEDURE· N/A

ACTION TAKEN IF TOLERANCES ARE EXCEEDED. Cartridge is replaced.

## DATA SHEET 2.3-2

PROCESS STEP Deionized Water Rinse
Millipore High Purity Water Rinse Station and Water Film Break Test

DESCRIPTION OF PROCEDURE. Final cleaning of thin film substrates prior to thin film deposition is achieved by rinsing thoroughly in high purity water processed thru a Millipore Super Q System. The system is a closed loop circulating type with a cascade rinse tank. The step is carried out at room temperature and follows a prerinse in dionized water.

FREQUENCY OF TEST Continuous visual monitor of water break on substrate surfaces for each substrate batch processed.

SAMPLE SIZE. 100%

MEASURING INSTRUMENT: Millipore Meg-O-Meter in a Recirculating Super-Q high purity water system. Meter range is 0.5 to 18 megohm-cm.

ACCURACY IN PERCENT Meg-O-Meter is calibrated to ±5% of full scale.

LIMITS OR TOLERANCES Water shall contain no particles greater than 1 micron and have a resistivity greater than 12 megohm-cm minimum. A resistivity of 1 megohm-cm at 25°C is equivalent to less than 10 ppb of ionizable impurities.

DATA RECORDING METHODS· Visual observation of meter.

CALIBRATION PROCEDURE Annual check by calibration.

ACTION TAKEN IF TOLERANCES ARE EXCEEDED. Cartridges are changed and substrates must be recleaned.

## DATA SHEET 2.3-3

PROCESS STEP. Vacuum Deposition
Thin Film Adhesion Test with Tensile Tester

DESCRIPTION OF PROCEDURE Before any thin film substrate is cut to size it must be subjected to an adhesion test. Three pieces of .006 gold wire are parallel gap welded to random unused areas of metallization using established welding schedules which have been established by isostrength diagram and certification. A custom designed ECI pull tester is employed and each wire is pulled past the breaking point at a rate of one inch per minute.

FREQUENCY OF TEST. Three .006 gold wires for each thin film substrate produced.

SAMPLE SIZE. 100 percent.

MEASURING INSTRUMENT. Scherr Tumico Gram Gage

ACCURACY IN PERCENT ±1% for full length of scale on all scale heads. (0-15 gms, 10 to 100 gms, 15-150 gms, 25-250 gms)

LIMITS OR TOLERANCES As a minimum the .006 inch gold wire will yield at 75 grams or more when pulled normal to the substrate.

DATA RECORDING METHODS Values are recorded in Engineering Log and kept as permanent record (QC Certification Records)

CALIBRATION PROCEDURE· Calibrated quarterly by ECI Calibration Department.

ACTION TAKEN IF TOLERANCES ARE EXCEEDED: Immediate calibration or replacement. Substrate is rejected or submitted for MRB action.

## DATA SHEET 2.3-4

PROCESS STEP. Vacuum Deposition
Weighing of Nichrome Evaporant

DESCRIPTION OF PROCEDURE. Weigh evaporation charges on double pan balance.

FREQUENCY OF TEST. As required.

SAMPLE SIZE. 100 percent.

MEASURING INSTRUMENT. Fisher Scientific Co. double pan balance.

ACCURACY IN PERCENT: Sensitivity to 0.1 gram.

LIMITS OR TOLERANCES. 1.5 grams ± 0.1 grams

DATA RECORDING METHODS. Go-no-go test without recording.

CALIBRATION PROCEDURE. Balance is calibrated annually to secondary NBS standard.

ACTION TAKEN IF TOLERANCES ARE EXCEEDED: Charge is rejected for use.

DATA SHEET 2.3-5

PROCESS STEP Vacuum Deposition
Veeco Vacuum System and Gages

DESCRIPTION OF PROCEDURE A Veeco VE-776 High Volume System capable of 1 x $10^{-6}$ Torr is used in this procedure. Vacuum is monitored with an ionization tube, located between the high vacuum valve and the diffusion pump, and is capable of measuring pressure in the $10^{-10}$ Torr range. The thermocouple gage reads pressure in two areas of the vacuum system.

FREQUENCY OF TEST. Monitor with all three sensors during every evaporation cycle.

SAMPLE SIZE N/A

MEASURING INSTRUMENT: Veeco Ionization Gage RGLL-7, Veeco Thermocouple Gage TG-7.

ACCURACY IN PERCENT: Ionization Gage Controller is ±5% total on all ranges. Less than 1% drift for 50 hours on all pressure ranges greater than $10^{-10}$ Torr after warmup.

LIMITS OR TOLERANCES Evaporation may not procede above 5 x $10^{-5}$ Torr.

DATA RECORDING METHODS: Readings are recorded on Deposition Log Sheet accompanying each pump down.

CALIBRATION PROCEDURE Units are calibrated semiannually by ECI Calibration Department.

ACTION TAKEN IF TOLERANCES ARE EXCEEDED: Immediate test and repair of equipment where required. Substrates are rejected or submitted for MRB action.

DATA SHEET 2.3-6

PROCESS STEP Vacuum Deposition
Electron Beam System Veeco 776

DESCRIPTION OF PROCEDURE· The E-Beam gun provides a heat source for the evaporation of nichrome and aluminum. A preevaporation cycle is used in order to purify or outgas the material to be evaporated. This is accomplished by heating the material at a lower temperature than that required for evaporation. Monitors for thickness and conductance are used to determine amounts of metal evaporated during the evaporation cycle.

FREQUENCY OF TEST· The E-Beam gun is used twice during each evaporation cycle.

SAMPLE SIZE· N/A

MEASURING INSTRUMENT: A wattmeter which measures in KW the total power output of the VEB-6 Electron Gun.

ACCURACY IN PERCENT ±0.1% over full range

LIMITS OR TOLERANCES Nichrome limits will be specified depending on the resistance needed. Conductors shall be from 2500 A to 6000 A thick.

DATA RECORDING METHODS· The Deposition Log Sheet accompanying each pump down contains space for aluminum thickness and monitor resistance value as well as E-Beam Power.

CALIBRATION PROCEDURE Test equipment is calibrated semiannually by the ECI Calibration Department.

ACTION TAKEN IF TOLERANCES ARE EXCEEDED. Immediate check and repair of defective part. Substrates may be scrapped or submitted for MRB action.

## DATA SHEET 2.3-7

PROCESS STEP. Vacuum Deposition
Sheet Resistance Film Monitor

DESCRIPTION OF PROCEDURE The Bendix Model RM-4 thin film conductance rate monitor provides continuous measurement of conductive films being deposited in the high vacuum system.

FREQUENCY OF TEST Conductance rate monitor is utilized during every evaporation cycle.

SAMPLE SIZE. Varies with number of substrates per batch.

MEASURING INSTRUMENT. The Bendix Model RM-4 Conductance Bridge has two d'Arsonnal panel-mounted meters for measuring percentage of desired conductance and the rate of change of conductance.

ACCURACY IN PERCENT· ±1% from 100 Ω to 10 Meg Ω.

LIMITS OR TOLERANCES Depends on desired sheet resistivity.

DATA RECORDING METHODS All resistance measurements are recorded on Deposition Log Sheet.

CALIBRATION PROCEDURE· Semiannually calibrated by ECI Calibration Department.

ACTION TAKEN IF TOLERANCES ARE EXCEEDED Substrate may be processed before scrapping or MRB action to determine actual sheet resistance.

## DATA SHEET 2.3-8

PROCESS STEP: Vacuum Deposition
Conductor Film Thickness Monitor

DESCRIPTION OF PROCEDURE: To monitor thickness the Sloan DTM-3 employs a sensor head consisting of a 5 MHz quartz crystal oscillator installed in the vacuum, facing and exposed to the source. As the evaporant builds upon the surface of the crystal its frequency changes. This changing frequency is compared against a tunable reference oscillator in the control unit. The beat frequency is converted to a dc signal and displayed on a panel meter.

FREQUENCY OF TEST. Once during each evaporation cycle.

SAMPLE SIZE. Varies with number of substrates per batch.

MEASURING INSTRUMENT: Sloan DTM-3 unit.

ACCURACY IN PERCENT. Frequency to 2% of full scale. Stability for one hour is ±30 parts per million.

LIMITS OR TOLERANCES. Monitor to specified value between 2500Å and 6000Å.

DATA RECORDING METHODS. Data recorded on Deposition Log Sheet every pump down.

CALIBRATION PROCEDURE Calibrated semiannually by ECI Calibration Department.

ACTION TAKEN IF TOLERANCES ARE EXPECTED. Immediate calibration or repair where necessary. Substrates may be rejected or submitted for MRB action.

DATE _____

RUN # _____

EXPERIMENT _____

1. SUBSTRATE TYPE _____
2. MONITOR SIZE _____
3. ROTATION _____
4. R MONITOR _____
5. HEATER _____
6. HEAT SOAK TIME _____
7. PREEVAP. TIME _____
8. E. B. POWER _____
9. DEPOSITION TIME _____
10. E. B. POWER _____
11. NICHROME BEHAVIOR _____
12. MAX PRESSURE _____
13. THICKNESS MONITOR _____
14. CONDUCTOR _____
15. DEPOSITION TIME _____
16. MAX PRESSURE _____
17. E. B. POWER _____
18. PRE ANNEAL RESISTANCE % TO NOMINAL _____
19. POST BAKE RESISTANCE % TO NOMINAL _____
20. AVERAGE TCR _____

COMMENTS·

ACTUAL CONDUCTOR THICKNESS _____

FIGURE 2-8. BATCH PROCESSOR RUN PROFILE

2.4 Photoetching. Microlithographic techniques using both positive or negative photoresists can be utilized in the delineation of circuit patterns for most thin film systems. The photoresist is applied to the deposited substrate and dried prior to exposure. The resist is exposed through a mask with the proper light source and the exposed pattern is developed and stabilized prior to film etching.

2.4.1 Photoresist Application. Many controls and guidelines must be followed to achieve an acceptable pattern. The photoresist must have a consistent viscosity such that the thickness is repeatable from one application to the next. The most accepted method of applying the photoresist is to spin the substrate to obtain a uniform layer. The speed and time of the spin affect the thickness of the photoresist. ECI controls the viscosity of KTFR to 60 ±10 centipoise by diluting the concentrated photoresist with KTFR thinner. The mixture is filtered through a 1.5 micron filter and stored in a clean amber bottle for a maximum of three days. Spin speed and the quantity of photoresist are dependent upon the size of the substrate to be coated. These controls are given in Data Sheet 2.4-1.

2.4.2 Exposure and Development. The exposure time depends on resist thickness, light intensity and type of photoresist. Typical exposures using an ultraviolet source with an intensity of 70 ±15 units will be 20 seconds. These are relative values and must be determined for each thickness. ECI uses a UV monitor to control the exposure source as described in Data Sheet 2.4-2.

Stoddard solvent or KTFR Developer is used to develop the pattern by spray developing for 30 seconds minimum. The development process is followed by a spray rinse to remove any residue. The substrate is then blown off with dry nitrogen. Substrates with an image acceptable for etching are placed in an uncovered petri dish and stabilized for 20 minutes at a temperature of 160° ±10°C.

2.4.3 Etching. Etching solutions are selected depending on the required line resolution. Some etchants, while fast and adequate for wide lines, may cause severe undercutting for narrow lines. Some etchants may retard or passivate remaining films making it very difficult or impossible to complete further processing. Control of the etching process begins by requiring fresh solutions to be prepared at least once a week. The aluminum etchant is usually a sodium hydroxide solution that is prepared by diluting a saturated solution of sodium hydroxide to 15 percent by volume with demineralized water. Etching is carried out by agitating a substrate in the solution held at 50°C for approximately one minute. The nichrome etchant is prepared by mixing 12 grams of cerium sulfate, 20 ml of nitric acid and 180 ml of demineralized water. With the solution at 65°C the etch time is approximately 30 seconds. Controls on the concentration, time and temperature of the etching solutions are maintained with simple laboratory equipment such as graduated cylinders, stop watches, and mercury bulb thermometers. The final and most important control on the photoresist and etching process is the visual inspection of the completed substrate.

2.4.4 Resistor Stabilization and Measurement. The thin film resistors must be annealed and passivated to achieve highly stable resistors with acceptable TCR values. A nichrome resistor film can be stabilized by annealing at 350°C for 1 hour and achieve TCR's of 25 ±25 PPM/°C.

After stabilization the resistor values are within 10 percent of final values and typically they are within 5 percent of final values. For resistors requiring closer tolerances, there are means to adjust the value by using trim bars or mechanical scribing.

Two-point probes and multi-point probes are generally used to measure resistor values where contact resistance can be ignored. When

resistor values are low enough or have close enough tolerances where contact resistance is important, a four-point probe system is used for testing. All values of resistors are read and recorded for reference on a data sheet as shown in Figure 2-9. The resistance changes during the stabilization (passivation) bake and the TCR of the nichrone resistors are two important parameters that are used to continuously monitor the resistor film deposition process. Any marked change in either parameter is an indication that the deposition process deviated during a run. A digital ohmmeter as described in Data Sheet 2.4-3 is used to measure values and TCR measurements are made as outlined in Data Sheet 2.4-4.

The size of most microcircuits allows many such circuits to be produced on the same substrate. When resistor testing is complete the circuits are separated into individual circuits by diamond-scribe sawing or by fracturing prescribed substrates. The separated circuits are placed in a precleaned plastic box for storage.

2.4.5 Inspection Criteria.

Adhesion Test. A minimum of three 0.006-inch diameter wires are bonded to the periphery area or monitor strip on each substrate per ECI Specification 49-00177. Pull tests of the bonds shall meet the requirements of ECI Specification 49-00177 using the Chatillon Vari-Speed Motorized Stage. Data is recorded on the Bond Verification Chart shown in Figure 2-15.

Surface Quality. An acceptable thin film having a thickness less than 10,000 Angstroms deposited on a glazed substrate will appear as a polished reflective surface and not frosty or grainy. Metallization deposited on an unglazed substrate will have a smooth and uniform appearance.

Defects. Defects, as defined in this specification, include pinholes, porosity, cracks and scratches. Each processed substrate will be examined utilizing a minimum of 30X magnification.

Foreign Material. Conductive foreign material embedded in the metallization shall be rejected. Conductive foreign material is defined as any opaque substance that is alien to the process requirements. Loose surface material shall be removed. Conductive foreign material from any cause in excess of 0.003 inch in any dimension shall be cause for rejection.

Thin filmed surfaces containing evidence of splatter, watermarks and blisters, or foreign material imbedded in the film are unacceptable, unless defect area is isolated from active circuitry.

Scratches and Voids. Metallization scratches and voids are acceptable, with the following exceptions.

a. A scratch or void in any circuit metallization which reduces the conductor line to less than 50 percent of the minimum design cross-section. Areas reduced to beyond 50 percent may be acceptable by MRB action providing the remaining circuitry of the defect area shall afford maximum continuous operating current flow at a temperature rise in the conductor of 20°C (68°F) above ambient room temperature with a safety factor of 50 percent.

b. Any scratch or void in the metallization, under the dielectric isolation area of a capacitor or crossover.

c. A scratch or void in the bonding metallization if more than 1/2 of the bond area is isolated from the conductor.

Poor Adhesion. Poor adhesion may be evidenced by the presence of blisters, excessive ragged edges, discoloration or disfiguration.

Clearance. Minimum spacing between any metallization and an edge of the substrate shall be 0.010 inch unless the substrate is to be mounted in card guides, in which case clearance between metallization and the edge of the guide shall be 0.010 inch minimum.

Any crack in the substrate that exceeds 0.003 inch in length and is directed toward a circuit area, metallization, or bond shall be cause for rejection. Any crack within any active area shall also be cause for rejection.

Chips. Chips or other such breaks in substrate material shall be considered voids if they fall within the active circuit paths. Chips are considered particles if they fall outside of the active circuit paths. Reject a chip covering greater than 50 percent of the spacing between active circuit paths, an edge chip encroaching into active circuit paths, or any chip exceeding 1/16 inch in its major axis.

Minimum conductor design width shall be 0.002 inch unless otherwise dictated by design.

Physical Dimensions. The substrates shall be examined to verify that the physical dimensions are as specified on the drill and trim drawings. Hole sizes shall be measured on the metallized side of the substrate, which shall exhibit the smallest diameter of the tapered hole.

Inspection is performed at a magnification of 30X using specular illumination impinging at various angles.

Deposition Log - Verification. Quality Assurance will ensure that the process data recorded is accurate and traceable to each substrate deposition. Data validation shall be evidenced by placement of the inspectors in-process stamp on the log sheet.

Records. Daily inspection records are kept in the appropriate Microelectronics Notebook, Adhesion Bond Sample Record, or Production, Inspection and Test (PIT) tag.

## DATA SHEET 2.4-1

PROCESS STEP. Subtractive Etching
Photoresist Spin Coating

DESCRIPTION OF PROCEDURE. A variable speed automatically timed spinner is used to apply photo resist to substrate material. A spin speed of 1500 RPM is used when applying photoresist to glazed surfaces. For unglazed surfaces a speed of 1000 RPM is used. The spin time is adjustable and preset at 30 seconds. A vacuum hold-down is provided for substrate mounting.

FREQUENCY OF TEST. Unit is used for all applications of photoresist as required.

SAMPLE SIZE. N/A

MEASURING INSTRUMENT· The Headway Corp. motor control unit contains a tachometer indicator and automatic timer.

ACCURACY IN PERCENT. Barring operator error, meter should be accurate for its full range of 500 to 9500 RPM within ±5%.

LIMITS OR TOLERANCES Spin speed variable from 500 to 10,000 RPM. Timer range is 5 to 120 seconds. Either 1000 or 1500 RPM for 30 seconds is normally used.

DATA RECORDING METHODS N/A.

CALIBRATION PROCEDURE· Calibrated semiannually by ECI Calibration Department.

ACTION TAKEN IF TOLERANCES ARE EXCEEDED· Immediate repair in case of any malfunction. If resist coating appears to be abnormal, it can be stripped and recoated.

DATA SHEET 2.4-2

PROCESS STEP· Subtractive Etching
Ultraviolet Exposure Meter

DESCRIPTION OF PROCEDURE Before exposing a photoresist coated substrate to a high intensity lamp, the probe of the UV Exposure meter is placed on the substrate holder. On the X5 scale a reading of 60 should be obtained.

FREQUENCY OF TEST. Once before UV lamp is used or each half shift.

SAMPLE SIZE. N/A

MEASURING INSTRUMENT. International Light UV intensity meter.

ACCURACY IN PERCENT. After standard reading is adopted, meter should hold to within ±2% at that range.

LIMITS OR TOLERANCES Distance and size of light source is constant. UV source will vary with age, but standard reading of 60 on X5 scale is minimum.

DATA RECORDING METHODS. No record kept.

CALIBRATION PROCEDURE. None required.

ACTION TAKEN IF TOLERANCES ARE EXCEEDED. Immediate repair or replacement of mercury bulb (UV source) as necessary.

## DATA SHEET 2.4-3

PROCESS STEP Photoetching
Thin Film Resistor Measurements

DESCRIPTION OF PROCEDURE: The value of each thin film resistor is recorded both before and after annealing. Single point probes over a moving (x axis) platform ensure a minimum of scratching on circuit surface The combination digital voltmeter NLS-X2 and NLS Model 2504 Data Printer are used to obtain and record resistor values.

FREQUENCY OF TEST Every resistor produced under contract is measured with this equipment.

SAMPLE SIZE 100%.

MEASURING INSTRUMENT. Nonlinear Systems X-2 Digital Voltmeter NLS Model 2504 Data Printer.

ACCURACY IN PERCENT: Voltmeter ±0.01% of full scale ±0.02% of reading.

LIMITS OR TOLERANCES. Voltmeter. ±9.999 ±99.99 ±999.9 with 20% over range on the two lower ranges. Resistor values to tolerances specified by contract.

DATA RECORDING METHODS: Information obtained from Digital Voltmeter is printed out on the Data Printer and retained along with a data sheet for that particular substrate.

CALIBRATION PROCEDURE Calibrated semiannually by ECI Calibration Department.

ACTION TAKEN IF TOLERANCES ARE EXCEEDED. Immediate calibration or repair as required. Substrates with out of tolerance resistors are either rejected or submitted for MRB action.

| | |
|---|---|
| CKT NAME | SUB. NO. |
| CKT NO. | MONITOR VALUE |
| NO. CKTS ON SUB | NiCr DEPOSITION TIME |
| 1st ETCH | AVERAGE BAKE % |
| 2nd ETCH | AVERAGE TC IN PPM/C° |
| RESISTOR TRIM & ETCH | SIZE & DRILL |
| COMMENTS | |

| R | INITIAL VALUE | POST BAKE | Δ R | 150° | 25°C | Δ R | T.C. PPM | FINAL TEST | |
|---|---|---|---|---|---|---|---|---|---|
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FIGURE 2-9.

## DATA SHEET 2.4-4

PROCESS STEP. Photoetching
Thin Film Resistor Measurements (TCR)

DESCRIPTION OF PROCEDURE After annealing, all circuits are subjected to a TCR measurement as follows·

(a) Measure resistance at room temperature and record,
(b) Measure resistance at +150°C (use ECI hot plate and Harrel Temperature Controller), and record,
(c) Remeasure resistance at room temperature and record. Use the formula $\frac{\Delta R}{R_0 \Delta T}$ to calculate the temperature coefficient of resistance for each resistor.

FREQUENCY OF TEST. Selected resistors with a minimum of one per circuit.

SAMPLE SIZE. Approximately 20%.

MEASURING INSTRUMENT. NLS -X2 Digital Voltmeter, NLS Model 2504 Data Printer, Harrel Temperature Controller.

ACCURACY IN PERCENT Harrel .01% full scale from -100°F to 500°F Voltmeter ±0.01% of full scale ±0.02% of reading.

LIMITS OR TOLERANCES TCR Specification is 25 PPM/°C ±25 PPM/°C.

DATA RECORDING METHODS All data is printed out on the NLS 2504 Printer tape and attached to data sheets.

CALIBRATION PROCEDURE: All equipment is calibrated semiannually by ECI Calibration Department.

ACTION TAKEN IF TOLERANCES ARE EXCEEDED. Immediate repair or calibration. Any discrepant TCR readings would cause circuit units to be rejected or submitted for MRB action.

DATA SHEET 2.4-5

PROCESS STEP. Vacuum Deposition and Photoetching Inspection Equipment

DESCRIPTION OF PROCEDURE Visual and mechanical inspection of thin film substrates in accordance with the blueprint and Quality Control Instruction 171.000 Section 9.02 and appropriate ECI 49-document.

FREQUENCY OF TEST All substrates inspected.

SAMPLE SIZE 100%

MEASURING INSTRUMENT·

(1) Nikon "S" Microscope - Magnification with 10X eyepiece 30X, 50X, 100X, and 400X. Backlighting provisions. Vernier X & Y carriage with millimeter provisions. Micrometer height adjust knob - 1 div. = .002 MM.
(2) Nikon comparator 10X - 31X - 100X Magnification with 2" x 4" X-Y micrometer stage .0001 per division and 360° turntable calibrated to 2 minutes.
(3) Chatillon Vari-speed Motorized Tension and Compression Tester. Selection of scales from 0 - 25 lbs and 0 - 1000 grams.

ACCURACY IN PERCENT

(1) Accuracy is within a division of the instrument.
(2) Accuracy is within a division of the instrument.
(3) 0.5% of full scale.

LIMITS OR TOLERANCES As required by customer's specifications, drawings, and/or inspection instructions.

DATA RECORDING METHODS: Daily Microelectronics inspection records. Production Inspection Test (PIT) Tag. Adhesion Bond Sample Record.

CALIBRATION PROCEDURE Instruments calibrated in accordance with the specified calibration schedule ECI Procedure 171.000 section 10.

ACTION TAKEN IF TOLERANCES ARE EXCEEDED Rejected substrates are returned for rework, repair, or scrapped, after MRB action.

2.5 Thick Film Deposition. The same basic objective applies to thick film deposition control that was stated for the case of thin film. Emphasis is placed on testing different physical properties since each process has different characteristics. Thick film substrate fabrication is not as critically dependent upon clean room conditions as that of thin film and monolithic circuit fabrication. Clean room conditions are maintained, however, to satisfy contract requirements. The most critical functions dependent upon clean room conditions are screen fabrication and actual screen printing prior to firing operations.

Before use in circuit fabrication, conductive paste materials are evaluated for resistivity and adhesion characteristics. Evaluation is required for each new lot of paste materials received. Resistivity of the conductor material is determined by screening and firing using a monitor pattern. Fired material must show sheet resistivity as applicable per contract requirements or per vendor specification. Also, adhesion samples are required to be made on a weekly basis.

Adhesion of conductor material is determined as follows:

a. Screen and fire a solder pad adhesion monitor pattern.

b. Solder attach a minimum of ten tinned-copper No. 26 AWG bus wires.

c. Pull test at 90° to monitor pattern surface using a suitable pull-tester. See Data Sheet 2.5-1 and Figure 2-10 for Quality Control sheet.

2.5.1 Screen Fabrication. Screens are selected for the mesh and material appropriate to the required circuit line width, thickness and spacing. The screen is trimmed and installed on a stretcher frame for stretching, with

screen strands positioned parallel to the stretcher straight edges. Printing frames are oriented to present as nearly as possible a 45° difference between the screen mesh axes and the printing frame sides.

The prepared precast print frame is set up with the screen side down against the clean glossy surface of a sheet of acetate positioned on the top surface of a plexiglass plate. A small quantity of the prepared emulsion is squeezed onto the screen surface. Fifteen minutes minimum drying time is allowed at room ambient and then a second coat of emulsion is applied. Coated screens are exposed and developed within 16 hours after being coated. The acetate sheet is not removed until immediately prior to the printing exposure operation. All processes involving photosensitive materials are performed under "photographic-safe" light conditions.

The finished screen must be capable of producing screened circuits of clean delineation, and must be free of pin-holes, flakes, and other contamination or surface irregularities as observed under 30X magnification.

2.5.2 Substrate Preparation. The substrates to be processed are cleaned in liquid detergent and tap water. They are then rinsed in flowing nonrecirculated water and blown dry with a jet of nitrogen (at no more than 50 PSIG) directed across the surface of substrate. Cleaned substrates are stored in appropriate enclosed containers that are non-deleterious to subsequent processing. Containers are cleaned prior to use.

Appropriate printing frames are installed in the holder and aligned to achieve proper screen registration with the substrate. The vertical spacing between the screen and the substrate is adjusted for precise parallel alignment. The spacing between screen and substrate is adjusted to approximately 0.025 inch for a first trial run.

2.5.3 Screen and Fire Operations. All paste materials are well stirred immediately prior to use with a stainless steel spatula. Stirred jars of paste are stored on a 45° active mixer that is rotating at one to three RPH When preparing blends of pastes, to achieve intermediate resistance values for example, the following procedure is used·

a. Each jar of paste must be stirred thoroughly before the required amount of paste is removed.

b. When a small amount of one paste is to be blended with a larger amount of another paste, a comparable volume of the larger should be added to the smaller one and then stirred for a minimum of 5 minutes.

c. Subsequently, the remaining amount of material is added in small increments and stirred to uniformity after each addition until the blending has been completed.

d. When intermediate resistor values are to be obtained it is desired to blend adjacent resistance value compositions in the series rather than those which are separated over a wide range.

The paste of the highest firing temperature is selected for first screening application. The printer is cycled to produce a sample deposition of material and adjusted as required until proper screening is accomplished. An adequate supply of paste is maintained on the screen to ensure complete screening of circuits. All substrates after printing are dried under

radiant heat at 125° ±15°C (257° ±27°F) for 15 minutes minimum prior to firing, depending upon the characteristics of the paste material applied.

Substrates are placed on the conveyor belt of a continuous belt furnace for the appropriate firing cycle. Belt speed and temperature profile programs are in accordance with established optimum criteria for the various paste materials to be processed. Precise firing cycle data is recorded for each production run of deliverable substrates. Temperature profiles are maintained within ±5°C. The rates of temperature rise and temperature fall ahead of and following the firing level are within 30° to 70°C per minute. It is desirable for a given profile, that control be held to within ±5°C per minute along the rising segment of the profile. See Data Sheet 2.5-2.

2.5.4 Resistor Trim. Prior to trimming, the resistors have been established as being within the required trim range. The substrate is placed on platform in the trim station so that the resistor is centered beneath the abrasive nozzle. The resistance bridge monitor probes are lowered to make contact with the resistor terminals. The bridge is adjusted to the required resistance, and the nozzle movement speed control adjusted for the desired feed. When the programed resistance value is obtained, the bridge will cut off the abrasive flow automatically. See Data Sheet 2.5-3 describing the trimming station.

2.5.5 Final Processing. Unless otherwise specified, sizing of thick film substrates shall be performed before resistors have been trimmed. The sizing tool is a sharp tip diamond scribe which is positioned in the sizing fixture approximately 10° from the vertical, with the slope in the direction of scribe movement. With substrate held firmly in position the scribe carriage is pushed across the substrate surface. The substrate is placed with scribed side down (circuit side up) on approximately

0.125 inch foam rubber pad on the breaking fixture platform. The movable jaw is lowered onto the substrate until the substrate snaps. Following the breaking operation should any surface require rework, the function is performed using a diamond abrasive disc.

In prototype quantities, if holes are required, they are drilled using an abrasive air stream. The substrate is placed on a drilling platform in the abrasion station and aligned by use of a cross-hair cursor. With substrate held firmly in position, the abrasive stream is actuated until the hole is enlarged to its required size. See Data Sheet 2.5-4.

To ensure even tinning and minimum amalgamation of conductor material, thick film conductor pad areas to be tinned are cleaned. A stick eraser is applied by hand with a light burnishing action until the conductor pad exhibits a slight metallic luster. Residue is removed with solvent. After soldering, flux or any entrapped residue is removed from solder area with cotton swabs saturated in solvent.

2.5.6 Inspection Criteria.

Film Thickness. Conductive circuit films shall evidence relative uniformity in thickness. Noticeable thin areas which reduce the effective cross-sectional area by more than 50 percent shall be rejected. Severe surface scratches in metallization shall be cause for rejection. Conductive line resistance of a fired circuit shall not exceed the following resistivities:

| Conductive Paste Material | 49-00174 Dash No. | Maximum Sheet Resistivity |
|---|---|---|
| Gold | -001 & -010 | 0.03 ohms/square |
| Palladium/Gold | -002 | 0.3 ohms/square |
| Blend | -009 | 0.1 ohms/square |

Dielectric films shall be evaluated by electrical test.

Process Log Verification. Inspection will ensure that the process data record is accurate for each production run. Daily Inspection Record "Microelectronics," Solder Adhesion Test Record and Substrate Inspection Tag are used to document the inspection and testing of the thick film substrate.

Foreign Materials. Conductive foreign material embedded in the metallization or dielectric shall be rejected. Conductive foreign material is defined as any opaque substance that is alien to process requirements. Loose surface material shall be removed.

Conductive foreign material from any cause in excess of 0.003 inch in any dimension shall be cause for rejection. Conductive material shall not reduce the clearance between circuit paths by more than 25 percent of the design clearance.

Chips. Chips or other such breaks in substrate material shall be considered voids if they fall within the circuit paths. Chips are considered particles if they fall outside of the circuit paths.

A chip covering greater than 50 percent of the spacing between circuit paths shall be cause for rejection. Any edge chip encroaching into circuit paths shall be cause for rejection and any chip exceeding 1/16 inch in its major axis shall be cause for rejection.

Adhesion Testing of Thick Film. Adhesion samples are made weekly. These solder pad adhesion monitor patterns are submitted for pull testing.

Minimum acceptable pull strength shall be 1/4 pound for pad size of 0.050 x 0.100 inch. The pull test shall be done at 90° to monitor pattern surface using the Chatillon pull-tester. The rate of pull shall not exceed 1 linear inch per minute.

Visual Inspection. Each substrate shall be examined after firing, using a minimum of 30X magnification. This will serve to verify the integrity of the screen as well as the printing process.

a. Circuit line width shall not exceed 150 percent, nor be less than 75 percent of that registered on the photographic film from which the screen was made.

b. Conductor design width shall be 0.005 inch minimum unless otherwise dictated by design. Spacing between fired circuit paths shall not be less than 0.003 inch.

Minimum spacing between any metallization and an edge of the substrate shall be 0.010 inch unless the substrate is to be mounted in card guides in which case clearance between metallization and the edge of the guide shall be 0.010 inch.

c. Registration between successive layers of deposition shall be adequate to ensure electrical continuity or dielectric integrity, as intended.

d. Defects such as edge indentation, pin-holes, blisters, or other voids are acceptable in conductor paths as long as line width is not reduced beyond 50 percent of cross-section. Pad area must afford adequate area for bonding. Metallization shall evidence no contamination or non-uniformity when viewed under 50X magnification.

e. Areas reduced to beyond 50 percent may be acceptable by MRB action providing the remaining circuitry of the defect area shall afford maximum continuous operating current flow at a temperature rise in the conductor of 20°C (36°F) above ambient room temperature with a safety factor of 50 percent.

f. Dielectric films in all cases shall overlap metallization films by at least 0.005 inch. Any voids, bubbles, or holes in areas isolating conductor crossovers shall be cause for rejection.

g. Any crack in the substrate that exceeds 0.003 inch in length and directed toward a circuit area, metallization or bond shall be cause for rejection. Any crack within any deposited area shall be cause for rejection.

TO: Thick Film Department

FROM: Engineering Quality Control

DATE:

REF: 49-00174

In Accordance With ECI Process Specification 49-00174 Thick Film, Screening Process, Microelectronics Paragraph 3.5.1. It Is Requested You Submit One Sample On Solder Pad Adhesion Monitor Patterns To Engineering Q.C. For Testing Per Paragraph 3.1.1.2.

Engineering Q.C. (Dept 650)

---

TO BE FILLED IN BY THICK FILM DEPARTMENT

Type of Paste: _____ Paste Lot No. _____

P.O._____ Date Fired: _____

Firing Lot No._____

Firing Temp. _____ °F

| No | Pull Test Value | Failure Mode | No | Pull Test Value | Failure Mode |
|---|---|---|---|---|---|
| 1 | Lbs. | | 6 | Lbs. | |
| 2 | Lbs. | | 7 | Lbs. | |
| 3 | Lbs. | | 8 | Lbs. | |
| 4 | Lbs. | | 9 | Lbs. | |
| 5 | Lbs. | | 10 | Lbs. | |

MINIMUM PULL STRENGTH REQUIRED .25 POUNDS

Accept: _____ Reject: _____

Date Tested:_____ By Stamp:_____

NOTE: A Completed Copy To Be Forwarded To Thick Film Department

EQC: 080 2/10/69

FIGURE 2-10.

## DATA SHEET 2.5-1

PROCESS STEP. Thick Film Deposition
Conductor Adhesion Test

DESCRIPTION OF PROCEDURE. An ECI No. X324 test pattern is screened and fired with the metallization being used at the time of test. After firing, the substrate is inspected and 10 #26 gage wires are soldered to each pad. These wires are pull tested on an ECI pull tester. Readings must be 1/4 pound minimum but average greater than five pounds.

FREQUENCY OF TEST. Weekly and receipt of new shipment of paste.

SAMPLE SIZE Varies, approximately 10%.

MEASURING INSTRUMENT. ECI pull tester with Hunter Spring Gage.

ACCURACY IN PERCENT Spring gage .05% over full scale.

LIMITS OR TOLERANCES Average must be greater than 5 lbs with a minimum of 1/4 lb.

DATA RECORDING METHODS Entered in log book and kept as permanent ECI record.

CALIBRATION PROCEDURE· Pull tester is calibrated semiannually by ECI Calibration Department.

ACTION TAKEN IF TOLERANCES ARE EXCEEDED Immediate search of process, humidity, etc., for cause. First suspect is equipment, then material, then process. Calibrate or repair where necessary. Paste may be rejected.

DATA SHEET 2.5-2

PROCESS STEP: Thick Film Deposition
Belt Furnaces and Controllers

DESCRIPTION OF PROCEDURE During the thick film process, each layer must be sequentially fired at a controlled temperature profile. A standard profile is run a minimum of once every six months and belt speed is checked.

FREQUENCY OF TEST: Controllers are monitored once for each firing of a thick film layer.

SAMPLE SIZE: N/A

MEASURING INSTRUMENT Honeywell Controllers on Trent & Watkins Johnson furnaces. A Texas Instruments Chart Recorder and high temperature thermocouple for profile.

ACCURACY IN PERCENT WJ furnace will hold to ±1 degree F. Trent will hold to ±5 degrees F.

LIMITS OR TOLERANCES: Speed - WJ and Trent to 4 inches per minute. Temperature ±5°C.

DATA RECORDING METHODS. A Data Control Sheet for each substrate contains its furnace profile.

CALIBRATION PROCEDURE. Standard semiannual ECI procedure.

ACTION TAKEN IF TOLERANCES ARE EXCEEDED Immediate repair or calibration as required. Substrates may be rejected or submitted for MRB action.

## DATA SHEET 2.5-3

PROCESS STEP. Thick Film Deposition
Resistor Trim Measurements

DESCRIPTION OF PROCEDURE: Upon finishing a thick film resistor, where initial test warrants trimming, the apparatus is preset to the resistor final value. The resistor is cut with air abrasive in the proper manner until the preset value is reached (value increase only). Equipment shuts off automatically when preset value is obtained.

FREQUENCY OF TEST All resistors.

SAMPLE SIZE: 100%.

MEASURING INSTRUMENT DeHart resistor trimmer with SS White Air Abrasive Generator and Boonton Nulling Bridge.

ACCURACY IN PERCENT: Boonton Bridge is ±0.1% over entire range.

LIMITS OR TOLERANCES· All resistors usually trimmed within 0.5%.

DATA RECORDING METHODS Data Sheet for each substrate. Readings recorded in a go/no-go procedure.

CALIBRATION PROCEDURE: Calibrated semiannually or upon malfunction.

ACTION TAKEN IF TOLERANCES ARE EXCEEDED. Immediate calibration or repair. Substrates may be rejected or submitted for MRB action.

## DATA SHEET 2.5-4

PROCESS STEP Thick Film Deposition
Abrasive Jet Machining of Ceramic Substrates

DESCRIPTION OF PROCEDURE Hole is drilled from the opposite side of substrate by high pressure fine spray of abrasive material. Spray is automatically interrupted to prevent buildup of abrasive material in hole.

FREQUENCY OF TEST. N/A

SAMPLE SIZE N/A

MEASURING INSTRUMENT. Nikon Comparator.

ACCURACY IN PERCENT· True position within .002 inch.

LIMITS OR TOLERANCES Hole sizes range from .003 to .005 inches.

DATA RECORDING METHODS: N/A

CALIBRATION PROCEDURE None required.

ACTION TAKEN IF TOLERANCES ARE EXCEEDED Immediate repair or replacement of equipment. Substrate may be rejected or submitted for MRB action.

DATA SHEET 2.5-5

PROCESS STEP: Thick Film Deposition
Inspection Criteria

DESCRIPTION OF PROCEDURE. Visual and mechanical inspection of thick film substrates in accordance with blueprint and Quality Control Instruction 171.000 section 9.02 and appropriate ECI 49-document.

FREQUENCY OF TEST: All substrates inspected.

SAMPLE SIZE: 100%.

MEASURING INSTRUMENT
(1) Baush & Lomb Stereo Microscope 7X to 120X Magnification equipped with reticle, dimensions in .001 inch.
(2) Dial Verniers
(3) Nikon Comparator 10X - 31X - 100X Magnification with 2" x 4" X and Y micrometer stage - .0001 per division, and 360° turntable calibrated to 2 minutes.
(4) Chatillon Vari-Speed Motorized Stage Tension and compression Tester. Selection of scales from 0 - 25 lbs and 0 - 1000 grams.

ACCURACY IN PERCENT
(1) Accuracy is within dimensions of the instrument.
(2)
(3)
(4) 0.5% of full scale.

LIMITS OR TOLERANCES As required by customer.

DATA RECORDING METHODS: Daily inspection records, Solder Adhesion Test Record, Substrate Inspection Tag.

CALIBRATION PROCEDURE Instruments calibrated in accordance with the specified calibration schedule ECI Procedure 171.000 section 10.

ACTION TAKEN IF TOLERANCES ARE EXCEEDED Rejected substrates are returned for rework or repair, or scrapped after MRB action.

2.6 Discrete Component Assembly. Before assembly can begin, complete detailed assembly drawings must be provided which include drawings of carriers and devices to be used. ECI presently has carrier device drawings which show mechanical data as well as electrical test data. Electrical wire bonding information and chip geometry are also included. At the substrate level, other pertinent information is necessary. Location of discrete components, their orientation and wire bonding scheme must be clearly presented. ECI assembly drawings include components and are normally 10X final module size. Assembly drawings also indicate the types of interconnect material to be used, its quality specification, the type of bond to be made and its appropriate specification. Adhesive compounds and their application are also called out including both component-to-substrate and substrate-to-header mounting. Assembly drawings specify such items as parts list data, electrical schematic documentation, and next assembly information. If any necessary dimensions are required for specific item location, these are also included. Subassembly drawings are oriented to the same type of specific information.

Only the chip-in-carrier method of hybrid assembly is utilized for high reliability microcircuits. This approach also incorporates the concept of repairability to the individual component level. In some cases devices are not available in carrier form or the vendor does not meet the desired quality standards, therefore, ECI has developed assembly procedures for attaching active devices to ceramic carriers.

The metallized terminal pad area of a carrier must be at least 5 mils square and 150 micro-inch thick and be capable of being bonded by thermocompression, ultrasonic or parallel-gap bonding techniques using 0.001 inch or larger nominal diameter gold or aluminum wire. LIDS that are used in a solder assembly must be capable of accepting solder and have protection for the device during soldering operations.

Assembly drawings for direct die attachment, include such necessary information as device type, location, orientation, and wire bonding scheme. Detailed drawings of the devices, their geometry, and physical size are utilized. The bonding technique to be used is also stated on the assembly drawing.

2.6.1 Semiconductor Die Bonding. ECI has used devices which have complex back metallization systems. The preference is for chips with gold metallization on the backside since it simplifies bonding techniques and it more compatible with gold metallization systems. The use of gold/silicon preforms is quite common; however, and bonding schedules using them have been developed. Conductive epoxy has also been evaluated and is avoided whenever possible.

ECI uses a K&S Model 4221 ultrasonic bonder with a Buyfield generator and transducer. The generator has the capability of sweeping a 2 KC range superimposed on the resonant frequency during the bonding process. In addition, a die brazing bonding plate has been designed and fabricated in order to improve thermal contact between the heated stage and the substrate to be bonded. The heated stage and temperature controller have been specially designed such that precise temperature controls can be exercised. Temperature control has been found to be the most important parameter during die attachment. See Data Sheet 2.6-1 and Quality Control form for Data Collection Figure 2-11.

Rework of eutectic bonded chips is difficult. It can be accomplished at elevated temperatures, however, if the heat is carefully controlled. Special equipment is necessary and previous bonding methods must be considered. It is also necessary to remove wire bonds and their fragments for rebonding purposes.

2.6.2 Adhesive Bonding of Discrete Components. Discrete component attachment is usually accomplished by adhesive bonding. Carrier devices are generally adhesive bonded except when soldering of the LID type carrier is used. Adhesive bonding of carrier devices and ceramic capacitors has been thoroughly evaluated at ECI over the past years demonstrating that excellent shear strengths and bond reliability can be achieved. Two part epoxy systems must be carefully weighed and mixed in order to obtain repeatable results. Curing temperatures and times must also be controlled. Mixing containers should be clean and minimum quantities of adhesives to be mixed must be specified. Pot life of each adhesive compound determines how long a given quantity can be used during assembly. To minimize errors in mixing bonding with single part frozen adhesives is utilized. These adhesives are contained in small tubes and are kept frozen at specified temperatures until needed.

Qualification of an adhesive for discrete component bonding is accomplished by subjecting the adhesive to the following environmental conditions

a. Moisture Resistance in accordance with MIL-STD-202C, Test Method 106C except as follows

1. Device shall be exposed to a minimum of three 16-hour cycle tests.

2. Step 7a of Test Method 106C shall not apply.

3. No polarizing voltage shall be used.

b. Thermal Shock. The device shall be subjected to sudden temperature extremes for a total of 15 cycles. One cycle covers specified exposure to both high and low temperatures as follows

1. High temperature 125°C for 5 minutes maximum.

2. Low temperature -55°C for 5 minutes maximum.

3. Transfer time of 10 seconds maximum in all cases.

Sample bond testing is also required. A representative test specimen is provided for each individual mixture of adhesive to be used in production bonding. The test specimen consists of a minimum of 5 dummy carriers and/or chip capacitors bonded to a substrate of the same material specification. Failure for a sample bond is sufficient cause to reject the lot. Figure 2-12 is the required control form for data collection.

Extensive evaluation of adhesives has been conducted at ECI as related to film corrosion and contamination. When two adjacent conductor lines with a potential difference between them have been coated with an adhesive, corrosion of the metallization can occur. Contamination which interferes with interconnect wire bonding has also been investigated and controls have been established. To eliminate potential epoxy corrosion and contamination, ECI has generated a design specification which is summarized in Section 2.2.

Prior to discrete component adhesive bonding to substrates, it is necessary that a cleaning procedure be used. Cleaning solutions and appropriate rinse systems are specified as well as drying techniques.

Orientation of components to be adhesive bonded is accomplished by first positioning all components on the substrate to ensure proper fit and clearance. A component is removed from the substrate or mounting device and the adhesive compound is applied to the bonding area of the component with an appropriate tool. The component is carefully repositioned on the substrate in its proper location and orientation. Pressure is applied to the component using the pickup instrument to ensure the formation of a fillet as previously described. The specification also

cautions that adhesive compounds will not be allowed to contaminate circuitry or semiconductor chip or electrical bond areas. When all components have been bonded, the substrate assembly is placed in an oven for the specified cure cycle. After curing, the assembly is removed and allowed to self-cool to ambient temperature. The unit is then stored in a covered plastic or glass container that is nondeleterious. These containers are cleaned prior to use according to a written specification. If inert atmospheres are required for storage, this is also specified.

Cleaning procedures have also been developed for use after adhesive bonding and just prior to interconnect bonding. Special solutions are necessary such that epoxy degradation does not occur. Very slight contamination can interfere with thermocompression or ultrasonic interconnect bonding.

ECI specifications also include repair procedures for adhesive-mounted devices. Repair procedures involve the heating of the component to be removed with a heated tool with only that amount of heat necessary to soften the adhesive applied. The heat is not applied directly to the substrate or semiconductor device. When the epoxy adhesive has softened, a slight shearing force is applied to the carrier or chip capacitor and the component is then lifted from its mounting surface. The adhesive residue is removed from the bonding surface using specifically designed tools. Occasionally a heated stage with a flatpack or header holding fixture is used to apply heat during component removal.

After the component is removed and the substrate cleaned, a new component may be adhesive bonded as previously described. The original wire bonds that were removed before component removal will then necessarily be replaced using standard procedures. Bonding pads are designed to afford thermocompression bonding rework so that new bonds are never made over existing bonds.

2.6.3 Final Assembly. Substrate-to-package mounting at ECI is accomplished using epoxy adhesives with the adhesive most commonly used being TC-1520. This adhesive is purchased as either a two-part system or as a single part frozen material which is cured at 125°C for a minimum of 15 minutes. Both substrates and package bonding surfaces must be free of contamination before adhesives are applied. The type of epoxy adhesive used for substrate-to-package mounting is also dependent upon the type of material and/or plating to which the substrate is to be bonded.

2.6.4 Inspection Criteria. Visual inspection is performed at a magnification of 30X minimum and 60X maximum. Higher magnification can be used for verification of questionable areas.

Die Bonding by Ultrasonic or Manual Means.

a. The die shall be flat against its mounting surface and properly oriented.

b. The die shall be positioned on the carrier so that the available wire bonding area free of eutectic material is 0.010 inch minimum, or such that it will accept two double-stitch bonds without interference.

c. There shall be no voids in the eutectic flow around the die periphery exceeding 20 percent of the periphery.

d. All eutectic material shall show evidence of wetting. There shall be no slag (dross due to oxidation) or cold (frosty) gold eutectic seen around the die or on the mounting surface.

e. Eutectic flow on top of chip shall be cause for rejection. Excessive eutectic material outside of wetted area which may break away and become loose particles shall be cause for rejection, unless such particles can be removed without damage to the device.

f. Sample bond testing shall be performed. Three acceptable samples shall be prepared prior to each production shift. One additional sample shall be prepared and tested following each ten production bonds. Chips and carriers rejected for other than mechanical defects may be used for this purpose. Testing will be accomplished by shear testing. Production shall not start until a satisfactory sample has been produced. Failure of a representative sample shall be sufficient cause to reject the 10 bonds made immediately prior to the sample bond, when shear tested per item g.

g. Shear testing shall be by application of force against the side of a chip in a direction parallel with the surface of the substrate. The force shall be applied at a rate not exceeding one inch per minute. Failure of a sample bond at less than 400 psi shall be sufficient cause for rejection. Data is recorded on Chip-to-Carrier Adhesive Test Sampling Form, Figure 2-11.

h. When it has been demonstrated that the manufacturing processes have been brought under control (acceptance of five consecutive lots) the frequency of sampling may be reduced in accordance with acceptable Quality Control procedures to a minimum of one test sample for each group of 50 bonds produced. Rejection of any reduced sampling lot will automatically revert sampling back to tightened sampling in accordance with step f.

Adhesive Bonding

a. The component shall be mounted flat to the surface of the substrate or mounting device.

b. The adhesive shall exhibit sufficient flow so that adhesive is visible at the edge of the bonded component. The fillet shall not extend more than 0.020 inch beyond any edge but may extend beyond bonding area provided extension of adhesive is not detrimental to electrical bonding area or circuit performance.

c. Bubbles and/or voids in the adhesive shall not occupy more than 20 percent of the periphery.

d. A representative test specimen shall be provided for each individual mixture of adhesive used in production bonding. The test specimen shall contain a minimum of five dummy carriers and/or capacitor chips bonded to a substrate of the same material specification. The test specimen shall be cured concurrent with the production units. Each bond on the specimen shall be shear tested by application of force against the side of a carrier or capacitor, in a direction parallel with the surface of the substrate. The force shall be applied at a rate not exceeding one inch per minute. Failure of a sample bond at less than 400 psi shall be sufficient cause to reject the lot. Visual examination, for evidence of separation and presence of adhesive in eutectic or electrical bond areas will be performed at 30X magnification minimum. Any evidence of separation or presence of adhesive in eutectic of electrical bond areas shall be cause for rejection. Data is recorded on Adhesive Bond Sampling Form, Figure 2-12.

QC DATA SHEET

CHIP TO CARRIER ADHESION TEST SAMPLING

| DATE | PART NO. | QTY. | PER SHIFT THREE SAMPLES | | | PRODUCTION SAMPLING ONE PER TEN | | | | | ONE PER FIFTY | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
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NOTE: Minimum requirement 400 P.S.I. - Area x 400 = Minimum Requirement

FIGURE 2-11

DATA SHEET 2.6-1

PROCESS STEP. Discrete Component Assembly
Die Bonding Evaluation

DESCRIPTION OF PROCEDURE: Shear testing is used for verification of eutectic bond strength. Semiconductor chips are subjected to a shear test using a special ECI built test fixture. Unit under test is forcibly sheared from its mounting. The pressure required is recorded and must meet the standard pressure listed for that particular type item.

FREQUENCY OF TEST Ten dummy mountings are sheared at the start of any die bonding run. Sampling of five pieces for every 50 thereafter until job is completed.

SAMPLE SIZE: See MIL-STD-883.

MEASURING INSTRUMENT: Chatillon Gages

ACCURACY IN PERCENT. Gages ±2% full scale on all ranges.

LIMITS OR TOLERANCES 400 PSI minimum. Failure is indicated by fracture of silicon chip.

DATA RECORDING METHODS Permanent log book record for all shear tests.

CALIBRATION PROCEDURE. Calibrated standard ECI quarterly calibration procedure.

ACTION TAKEN IF TOLERANCES ARE EXCEEDED· Immediate repair or calibration as required. Carrier devices are rejected or submitted for MRB action.

## DATA SHEET 2.6-2

PROCESS STEP Discrete Component Assembly
Adhesive Bonding Evaluation

DESCRIPTION OF PROCEDURE· Adhesive used is Ablestick 450 epoxy in frozen tube. Epoxy is applied to component and component is placed in position on the substrate. Five sample bonds are made and shear tested by QC for each epoxy batch.

FREQUENCY OF TEST: Every half shift.

SAMPLE SIZE: Five pieces per epoxy batch and/or every half shift. Varies with circuits processed.

MEASURING INSTRUMENT. Chatillon gages.

ACCURACY IN PERCENT Gages are ±2% full scale on all ranges.

LIMITS OR TOLERANCES 400 PSI minimum.

DATA RECORDING METHODS Permanent logbook record for all shear tests.

CALIBRATION PROCEDURE: Calibrated quarterly, standard ECI Calibration Procedure.

ACTION TAKEN IF TOLERANCES ARE EXCEEDED: Immediate repair or calibration as required. Defective bonds may be cause for substrate rejection after MRB action.

:E_____

ADHESIVE BOND SAMPLES

| ADHESIVE P O NO / MATERIAL BATCH NO. | OVEN TIME/TEMP IN | OVEN TIME/TEMP OUT | OPERATOR No. | ASSEMBLY PART NO | SER.NO. | C/S | TEST (lbs.) 1 | 2 | 3 | 4 | 5 | RESULT Appd | Rej |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | |

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079A

FIGURE 2-12.

## DATA SHEET 2.6-2

PROCESS STEP. Discrete Component Assembly
Inspection Criteria

DESCRIPTION OF PROCEDURE: Visual inspection of the thick or thin film substrate after component bonding in accordance with the blueprint and Quality Control Instruction 171.000 Section 9.02 and appropriate ECI 49- document.

FREQUENCY OF TEST All substrates inspected.

SAMPLE SIZE: 100%.

MEASURING INSTRUMENT:
1. Bausch and Lamb Stereo Microscope 7X to 120X Magnification equipped with reticle, dimensions in .001 inch.
2. Chatillon Vari-Speed Motorized Stage, Compression and Tension Tester. Selection of scales from 0-25 lbs and 0-1000 grams.

ACCURACY IN PERCENT· Accuracy is within divisions of the instrument (2) or 0.5% full scale.

LIMITS OR TOLERANCES. As required by customer specifications, drawings, and/or inspection instructions.

DATA RECORDING METHODS. Daily inspection records. Microelectronics Adhesive Bond Sample Record, Production Inspection Test (PIT) Tag, Chip-to-Carrier Adhesion Test Sampling Form.

CALIBRATION PROCEDURE. Instruments calibrated in accordance with the specified calibration schedule ECI Procedure 171.000 Section 10.

ACTION TAKEN IF TOLERANCES ARE EXCEEDED: Rejected bonds are returned for rework or repair. Substrate may be scrapped after MRB action.

2.7 Electrical Lead Bonding. Interconnect bonding to ceramic carriers, chip capacitors, and semiconductor chips is accomplished using thermocompression nailhead and stitch bonding. Power supply, bonder head, tip holder configuration, and tip design have been characterized thoroughly in past years. ECI uses pulsed tip thermocompression bonders (see Data Sheet 2.7-1) thereby eliminating continuous tip heating problems such as encountered in bonding gold wire to aluminum device pads which may cause intermetallic bond degradation. Tip temperatures and force settings are monitored at various periods of the working day. Bond samples are also made and tested by Quality Control personnel. Prior to production bonding, an iso-strength diagram is prepared for each type of bond and the applicable process required.

2.7.1 Bonding Controls. The iso-strength diagram is a graphical representation expressing the average strength of the bond as a function of tip temperature/energy and pressure as shown in Figure 2-13. Completed diagrams exhibit the parameters that are most suitable for producing optimum bonds using specific materials with process repeatability. The iso-strength diagram includes the materials to be bonded, size, tip configuration and composition, tip cleaning method and frequency, cleaning procedures for material to be bonded, tip temperature (energy) and force settings required for obtaining optimum parameters and bonder manufacturer, model, and serial number. For each type bond, a minimum of 52 samples are produced at the optimum settings selected from the iso-strength diagram. See Figure 2-14 for Qualification Sheet. Fifty of these samples are pull-tested normal to the bonded surface at a linear velocity not exceeding one inch per minute The remaining two bond samples are subjected to metallurgical examination. During the pull-testing of nailhead or stitch bonds, should the bond fail prior to breakage of the wire,

the bond is unsatisfactory. The strength of bonds is required to be no less than 60 percent of the ultimate yield strength of the wire for wire less than 0.005 inch. When an iso-strength diagram set of conditions has been accepted, each additional bond station must then be qualified by preparing 20 bonds that meet the above criteria. Requalification of a bond station may be required when equipment has been placed on a different primary power source, major maintenance is performed on any element of the system, or if daily process control samples do not comply with the requirements of the initial iso-strength diagram.

Process control regulations require that five samples each of the minimum-maximum bonding station parameters shall be prepared that are representative of the material, type of bond and the equipment used. A Bond Verification Chart, Figure 2-15, is used for data collection. These samples must be furnished based on the following factors.

a. At the beginning of each shift

b. At half-shift intervals

c. New machine installed or replacement of capillary tip

d. Use of a new spool of wire

e. Following a misfire or no bond condition.

It is also required that bonder mechanism interconnections be examined for cleanliness and tightness at the beginning of each shift. The above requirements are mandatory so that reliable, reproducible bonds may be obtained at all times.

Normally, nailhead bonds are bonded to substrate metallization while stitch or wedge bonding is accomplished to discrete components such as

on carriers or capacitors. It is required that the capillary tip used for stitch and nailhead bonds be securely held perpendicular to the substrate surface. Capillary tips and wires are not touched with unprotected fingers since contamination may result. Nailhead and stitch bonds have been used to bond various types of films some of which are thin film aluminum and gold, thick film gold and palladium-gold, and gold plating over various submetallizations. Normally 0.001 inch gold wire is used for interconnections except when bonding semiconductor device pads which require a smaller wire.

## DATA SHEET 2.7-1

PROCESS STEP: Electrical Lead Bonding
Thermocompression Bonding of Fine Wire Leads

DESCRIPTION OF PROCEDURE: Cold stage pulse tip bonding is carried out in a manner similar to machine welding. Fine gold wire is fed through a capillary tip that is held between two electrodes and can be positioned from point-to-point. In the region where pressure and heat are applied, diffusion takes place. When the wire run is completed a flame cutoff severs the wire and leaves a pigtail which is removed by the operator.

FREQUENCY OF TEST: Every half-shift after weld schedule is established.

SAMPLE SIZE. Five samples every half-shift.

MEASURING INSTRUMENT. Weltec Model 10A Power Supply controls augmented by calibrated thermocouple and ammeter on power supply output.

ACCURACY IN PERCENT: Tip temperature reproducible within ±10°C.

LIMITS OR TOLERANCES: Shear strength must be 60% of tensile strength of wire as a minimum or value specified on iso-strength diagram.

DATA RECORDING METHODS. Sample information is recorded on QC Bond Verification Chart. Visual observation of meters during normal bonding.

CALIBRATION PROCEDURE: Calibrated quarterly by ECI Calibration Department.

ACTION TAKEN IF TOLERANCES ARE EXCEEDED. Immediate calibration or repair as required. Substrate or carrier devices may be rejected or submitted for MRB action.

Company Electronic Communications, Inc.
Department _____

Technician _____
Inspector _____
Welding Supv. _____

WELD POWER SUPPLY
Manufacturer _____
Model No. _____
Serial No. _____
Type of Bond _____

WELD HEAD
Manufacturer _____
Model No. _____
Serial No. _____
Bond Station No. _____

PREDOMINANT FAILURE

| | |
|---|---|
| CW | (Center Wire) |
| FA | (Film Adhesion) |
| CB | (Complete Bond) |
| BE | (Bond Edge) |
| BF | (Bulk Film) |
| S | (Substrate) |
| BW | (Bulk Wire) |

ELECTRODES OR CAPILLARY (UPPER)
Material _____
Tip Size _____ Radius _____
Tip No. _____ Polarity _____
P.O. _____ Included Angle _____
Vendor _____

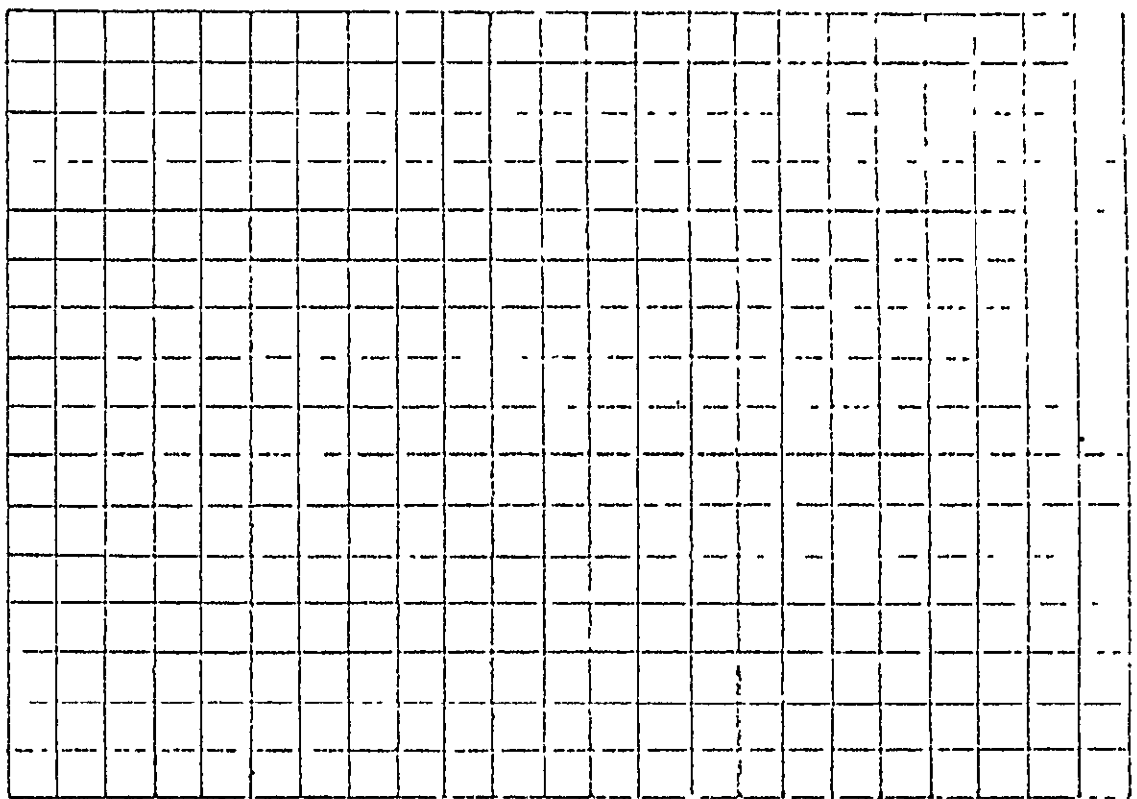
SUBSTRATE
Material _____
No. _____ P.O. _____
Vendor _____

WIRE (UPPER)
Material _____ Size _____
Tens.Str. _____ Melt# _____
P.O. _____ Vendor _____

WIRE (LOWER)
Material _____ Size _____
Tens. Str. _____ Melt# _____
P.O. _____ Vendor _____

ELECTRODES (LOWER)
Material _____ Tip Size _____
Polarity _____ Included Angle _____
Tip No. _____ P.O. _____
Vendor _____

CLEANING PROCEDURE




"ISO-STRENGTH" DIAGRAM NO. _____ DATE: _____

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FIGURE 2-13.

# WELD SYSTEM QUALIFICATION FORM

POWER SUPPLY
Mfr. _____
Model _____
Ser.No. _____

HEAD
Mfr. _____
Model _____
Ser No _____

ISO-STRENGTH DIAGRAM
No. _____
BOND STATION #_____

MATERIALS
Upper _____
Tensil Str. _____
Lower _____
Tensil Str. _____

ELECTRODES
Upper _____ Tip Size _____ Polarity _____
Lower _____ Tip Size _____ Polarity _____
Other _____

| i | Fracture Strength / Area $Y_i$ | $\bar{X}$ | $(X_i-\bar{X})$ | $(X_i-\bar{X})^2$ | i | Fracture Strength / Area $X_i$ | $\bar{X}$ | $(X_i-\bar{X})$ | $(X_i-\bar{X})^2$ |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | |

$$\sigma = \sqrt{\frac{1}{50} \sum_{i=1}^{50} (X_i - \bar{X})^2}$$

Average Weld Strength (X) _____
Standard Deviation (S) _____
0.10 $\bar{x}$ = _____

Technician _____
Inspector _____
Welding Supvr. _____
Date _____

FIGURE 2-14



NOTE: The Strength of the bonds shall be 60% of the ultimate yield strength of the weakest wire, or 75 grams minimum on .002"x.010" Flat Gold Ribbon

Date_____

Bond Station #_____

Power Supply #_____

Bonding Head #_____

Wire Type_____

Size_____

P.O. #_____

Tnsl Str._____Min._____

Tip #_____

Holder #_____

COMMENTS:

Time_____Counter Reading_____

Settings - 70V, TAP 3, 80 grams

| | TEMP. | CURRENT |
|---|---|---|
| 1. | | 1. |
| 2. | | 2. |
| 3. | | 3. |
| 4. | | 4. |
| 5. | | 5. |

Bond Sch#_____Bond Type_____

Material_____

1.
2. Average_____
3. Accept_____
4. Reject_____
5.

Bond Sch#_____Bond Type_____

Material_____

1.
2. Average_____
3. Accept_____
4. Reject_____
5.

Circuits Bonded S/N Operator No.

1.
2.
3.
4.
5.
6.
7.
8.
9.
10.

Time_____Counter Reading_____

Settings - 70V, TAP 3, 80 grams

| | TEMP. | CURRENT |
|---|---|---|
| 1. | | 1. |
| 2. | | 2. |
| 3. | | 3. |
| 4. | | 4. |
| 5. | | 5. |

Bond Sch#_____Bond Type_____

Material_____

1.
2. Average_____
3. Accept_____
4. Reject_____
5.

Bond Sch#_____Bond Type_____

Material_____

1.
2. Average_____
3. Accept_____
4. Reject_____
5.

Circuits Bonded S/N Operator No.

1.
2.
3.
4.
5.
6.
7.
8.
9.
10.

FIGURE 2-15. BOND VERIFICATION CHART

2.8 Preseal Visual Inspection

2.8.1 Thick Film Solder Joints. Each solder joint shall be thoroughly inspected utilizing a minimum of 3X magnification. Questionable solder joints shall be reexamined using higher magnification.

Lead Damage

The following are cause for rejection

a. Leads which have stress risers (sharp corners or notches) due to cutting, nicking or scraping, such as to expose the base metal

b. Indentations (smooth depression) which reduce lead diameter by more than 10 percent

c. Leads which terminate on a pad and extend through the board for a length less than the pad radius or more than the pad diameter

d. Clinched leads which do not follow the direction of the circuit or which do not partially contact the circuit

e. Clinched leads resulting in a reduction of the spacing between conductors to less than 25 percent of the designed clearance, but not less than 0.003 inch clearance

f. Solder joints which are rough and lusterless

g. Solder joints which appear disturbed or stressed

h. Connections which show embedment of lint, rosin, flux or other foreign material

i. Cracked solder joints

j. Voids, such as pits and holes if located against a lead or if solder or good wetting is not visible at the bottom of the void

k. Voids, such as pits and holes if the major axis of hole perimeter exceeds 0.010 inch, or if there are more than three voids per joint

l. Indentations (smooth depressions) which exhibit a granular appearance or any evidence of separation

m. Joints which exhibit evidence of solder layering or stacking

n. Dewetting of leads

o. Dewetting of the pad/solder interface

p. Solder fillet which does not cover at least 90 percent of the total pad periphery

q. Solder splatter which overhangs the circuitry

r. Solder splatter on circuit lines when there is no evidence of good wetting action

s. Solder splatter on areas other than circuitry

t. Clinched lead when contour of the heel (bend) of the lead is visible

u. When a concave fillet exists between the lead and circuit path

v. When the convex fillet of solder extends beyond the edge(s) of the circuit path

w. Lifted pads or lines.

The following may be accepted:

a. Exposure of base material under indentations

b. Leads which are flush to or as close as practical to the circuit provided that contact with at least one point of the circuit path is made

c. Indentations or contour changes due to cooling.

d. Smooth depressions caused by conformal coating removal or eraser tooling.

e. Layering between two or more adjacent joints.

f. Clinched lead.

g. Lead and circuit path.

h. If no extension of solder beyond the edge(s) of the circuit path.

Records are kept in Daily Inspection Records "Microelectronics", Thick Film Solder Adhesion Record, Bond Verification Chart, and Production Inspection and Test (PIT) Tag.

2.8.2 Component Adhesive Bonds. See Section 2.6.4, Adhesive Bonding.

2.8.3 Thermocompression Bonds.

Mechanical Criteria.

Thermocompression wire and ribbon bond samples will be tested by vertical pull (90 degrees to the bonded surface). Linear velocity shall be constant and not exceed one inch per minute.

During the pull testing, should the bond of a 0.001 inch wire fail prior to breakage of the wire, the bond is unsatisfactory. The strength of bonds shall be no less than 60 percent of the minimum tensile strength of the wire as specified on the drawing for wire less than 0.005 inch, and 0.001 by 0.005 inch flat ribbon wire. The strength of a bond using 0.002 by 0.010 inch flat gold ribbon interconnect lead wire 0.005 inch and greater

shall be a minimum of 75 grams. Pull strength shall be recorded on the Bond System Qualification Form.

Variations in strength shall be calculated in accordance with the following procedure. The standard deviation must be equal to or less than 10 percent of the average ultimate strength of the qualification bond sample.

Visual Criteria for Fine Wire

All bonds shall be inspected at a magnification of 30X minimum and 60X maximum. Higher magnification can be used for verification of questionable areas.

The following are cause for rejection

a. Bonds placed so that separation between the bonds, or two different pad areas, or the bond and adjacent metallization is less than 0.0005.

b. A bond which has less than 50 percent placement on the bonding pad.

c. Bonding wires with different electrical potentials which come within two wire diameters or 2X ribbon thickness of the die or header without proper insulation.

d. Broken wires.

e. Excessive wire slack which could result in shorts or wires which are higher than the package.

f. Missing bonds.

g. Pigtails which are longer than three wire diameters or 3X ribbon thickness.

h. Visible intermetallic formations such as purple plague around the periphery of the bond.

i. Any lead which exhibits a deformation, for example a nick, cut, crimp, etc., reducing the wire more than 25 percent of its original diameter or thickness.

j. Any lifted bonds.

k. Any bond that exhibits a crack in the bondment or adjacent to it.

l. Any bond that exhibits pits in either of the materials being joined.

m. Any bond in which holes or voids are evident.

n. Any bond in which portions of the materials that were in contact with electrodes exhibit fusion.

o. An open bond. An open bond is one on which a bond has been attempted but no bonding has occurred or in which a bond has been specified by a drawing but has been overlooked by the bonding machine operator.

p. Any bond which has any portion of its wire periphery (projection thereof) outside the boundaries of the bonding pad.

q. Bonds in which the termination at the ball shows nicking down to a diameter less than 75 percent of the original diameter.

r. Any bond in which its wire terminates outside the center 2/3 area of its ball (ball bonds) when viewed from the top. The 2/3 area is defined by a concentric circle.

s. Bonding pads which show evidence of horizontal force when the bond was made.

t. Ball bond diameters that are less than two wire diameters or greater than five wire diameters.

u. Bonds which have less clearance than one wire diameter or 0.003 inch whichever is smaller.

v. Any unit which has bonds missing or which is not double or triple stitch bonded at the termination area.

w. Any bond having a wire loop between stitch bonds greater than 4X wire diameter in height.

x. Any stitch having the first bond over the edge of the termination area. Spacing between stitches measured from setdown-to-setdown shall be between 1X and 4X or wire diameter.

y. Separation between adjacent wire stitch bonds shall be one wire diameter or 0.003 inch, whichever is smaller.

z. Typical wedge bonds shall be two diameters by five diameters. Any wedge bonds that show gross differences to the typical wedge shall be rejected. Separation between bonds shall be specified.

Visual Criteria for Parallel Gap Bonds

a. Acceptable bonds shall exhibit a minimum of 10 percent for ribbon wire and 25 percent for round wire setdown in the preformed area (bond zone) on the upper workpiece. There shall be no evidence of pitting, cracking, or reduction more than 50 percent in the lead cross-section, and no evidence of heating or sticking in the electrode contact area.

b. Reject bonds on the same pad area which overlap.

c. The leads shall be fully supported by the bond pad allowing a visible projection of the pad on both sides of the lead. These projections shall be nominally equal as determined by visual inspection.

d. Leads shall be aligned so that the electrodes maintain contact across the full width of the leads. Bonds indicating improper alignment shall be rejected.

Records are kept in Daily Inspection Records "Microelectronics," Bond Verification Chart, and Production Inspection and Test (PIT) Tag.

2.6.4 Preseal Cleaning. Immediately prior to sealing, covers and flatpacks shall be cleaned as follows.

a. Clean flatpack by swabbing seal area with special solvent cleaner, ECI 22-00314-001.

b. Blow dry with nitrogen, ECI 22-00262-001 at not more than 40 psig. Nozzle shall not be held closer than four (4) inches from circuitry.

c. Examine at 30X minimum magnification for distortions of interconnects or contamination of circuitry and seal area.

Records are kept in Daily Inspection Records "Microelectronics," and Production Inspection and Test (PIT) Tag.

DATA SHEET 2.8-1

PROCESS STEP: Pre-Seal Visual Inspection

DESCRIPTION OF PROCEDURE· Visual inspection of the thick or thin film substrate in the carrier or header immediately prior to sealing in accordance with Quality Control Instruction 171.000 Section 9.02 and appropriate ECI 49- document.

FREQUENCY OF TEST: All assemblies inspected.

SAMPLE SIZE: 100% inspection of all bonding and inspection of substrate and carrier for cleanliness.

MEASURING INSTRUMENT. Bausch & Lomb Stereo Microscope 7X to 120X Magnification, equipped with reticle, dimensions in .001 inch.

ACCURACY IN PERCENT· Accuracy is within division of the instrument.

LIMITS OR TOLERANCES As required by customer specifications, drawings, and/or inspection instructions.

DATA RECORDING METHODS. Daily inspection records "Microelectronics" Production Inspection and Test (PIT) Tag.

CALIBRATION PROCEDURE Instruments calibrated in accordance with the specified calibration schedule, ECI Procedure 171.000 Section 10.

ACTION TAKEN IF TOLERANCES ARE EXCEEDED. Rejected assemblies are returned for rework, repair, or scrap after MRB action.

2.9 Sealing. Package sealing at ECI involves several different methods which are dependent upon circuit application and requirements. The basic types of sealing high reliability microcircuits at ECI are

a. Hermetic sealing using eutectic preforms

b. Hermetic reflow solder sealing

Package types include:

a. All metal with glass around leads

b. All ceramic

c. Combination ceramic-metal.

2.9.1 Process Description. The most prevalent sealing method involves either eutectic preform or reflow solder sealing of various size flatpacks. Both manual and automatic sealing processes have been developed.

Prior to sealing, a complete cleaning and preseal visual inspection is required of each package. Before flatpack tinning, an ultrasonic cleaning operation is required after which tinning is accomplished using a mildly activated flux (Kester 1544) and a solid core 63-37 solder (melting point 180°C). For eutectic sealing, an 80-20 gold tin preform with a melting point of 280°C is used. Removal of flux prior to sealing is important. Cleaning is accomplished with special solvents and thorough rinsing techniques followed by drying with dry nitrogen.

A two-hour vacuum bake at 125°C at greater than 25 inches mercury is required prior to sealing. Before the circuit is removed from the oven, the oven must be allowed to cool to less than 40°C before the vacuum is released.

A nitrogen/helium dry box atmosphere must exist 30 minutes before sealing is accomplished. The helium must be approximately 25 percent of the nitrogen/helium atmosphere. The dry box exit water vapor is monitored and is not allowed to exceed 60 ppm during sealing operations. See Data Sheet 2.9-1.

Other sealing requirements include hot plate temperatures, fixture alignment dimensions, time of direct contact heating, and forces to be used. Requirements for blow hole sealing without flux are also specified. Inspection criteria includes quantity of solder at the seal, position of cover on header and leaks that may be visually detected. Most flat pack style packages are sealed in a commercially available sealer. This equipment is described in Data Sheet 2.9-2.

Rework of sealed packages is accomplished on reflow solder sealed units only. This type of package can be opened, the assembly reworked, and the package resealed. Rework of the seal area is done in a dry box atmosphere using a heated tool.

2.9.2 Leak Testing. One ECI gross leak test consists of placing the module or flat pack in a beaker of demineralized water at 90° ±5°C; the appearance of gas bubbles from the package indicates a gross leak. If no bubbles appear from the package after a minimum of three minutes immersion, it is removed from the beaker and blown dry with a jet of dry nitrogen at not more than 40 psig. An alternative test using a fluorocarbon solvent is described in Data Sheet 2.9-3.

Fine leak tests are performed in accordance with MIL-STD-202C, Method IV except upon completion of test procedure specimen shall not be checked for gross leaks. See Data Sheet 2.9-4.

2.9.3 Inspection Criteria. The sealed assembly shall be examined to verify that the cover installation and the physical dimensions are as specified on the drawing. The surfaces of the assembly shall not be distorted (oil can bulge) during the sealing operation.

a. 7X minimum magnification is used to visually inspect the solder flow for an indication of proper sealing.

b. No holes shall be allowed. Any depression of the solder between mating surfaces shall not exceed half the thickness of the container wall.

c. There shall be no evidence of flux in the area.

d. Radiographic inspection shall be used to verify seal integrity and absence of solder balls and other extraneous solder.

e. Use 4X minimum magnification to examine the plating on the case. The plating shall exhibit a smooth and fine-grained surface consistent with the surface characteristics of the base metal or underplate as well as cracks, blisters, peeling, foreign material and other defects which due to their degree, nature or extent detrimentally affect the suitability of the plating for its intended use.

f. Exposure of lead base material through the plating finish in the area of 1/32-inch to 3/4-inch from the header or glass seal is not acceptable.

g. Reject leads which have stress risers (sharp corners or notches) due to cutting, nicking or scraping such as to expose the base metal.

h. Reject indentation (smooth depression which reduce lead diameter by more than 10 percent). However, exposure of base material under indentation shall be acceptable.

i. Cracks observed in the glass seal area shall be rejected except as noted below.

Meniscus Cracks. Meniscus cracks are those cracks which lie in the raised portion of the glass bond about the lead, above the mounting plane of the header. This type of crack is acceptable as long as the bottom of the crack is visible under 20X magnification.

Thumbnail Cracks. This type is found around the outer edge of the glass seal. If the glass is removed, the cracked device will be accepted if the depth of the chip is estimated to be equal to 1/4 of the header thickness or less.

j. A circumferential chip is a chip about the circumference of the glass region around the lead from which the glass portion of the seal has been broken. If the area of the void is estimated to be less than 1/4 the area of the glass region, or if the estimated depth is not more than 1/4 thickness of the header, the device will be accepted.

k. Air bubbles in the glass region are acceptable, if the bubble does not exceed 1/4 the area of the glass region, and if the depth of the hole is visible under 20X magnification.

Fine Leak Test

a. Fine leak seal test shall be performed in accordance with MIL-STD-202C, Method 112A, Test Condition "C," Procedure IV except upon completion of test procedure specimen shall not be checked for gross leaks per test condition "A" or "B." Gross leak shall be per Section 2.9.2.

b. A leak rate of helium as indicated on mass spectrometer leak detector (MSLD) machine that is no greater than fine leak rate specified for the part will be considered acceptable for hermetic seal.

c. The specimen under test shall be subjected to a pressure level of $1 \times 10^{-5}$ Torr maximum. The pressure level shall be maintained until the leak indicator meter has stabilized.

d. Perforation of the test specimen after mass spectrometer test shall not be required.

e. In process or additional leak tests may be performed when necessary.

f. Where bomb pressures specified in MIL-STD-883, Method 1014 exceed the package capability, alternate pressure and time (bomb and dwell) conditions may be used provided they satisfy the leak rate, pressure, time relationships which apply, and provided no less than 15 psig bomb pressure is applied in any case. The maximum allowable leak rate shall be as specified for the part (Reference ECI 88-00003 or MIL-STD-202 as applicable). In all cases, the product of the bombing pressure as expressed in atmosphere and the bombing time as expressed in hours shall be no less than 12.

Gross Leak. Fluorcarbon/reduced pressure method. Applicable to any hermetically sealed electronic device whose test specification reflects this method, or, in those occurrences where the specific test method is not delineated. The procedure is as follows.

a. Assemble equipment.

b. Adjust light source so as to shine through glass beaker to a dull nonreflective background.

c. Prior to the start of each working day, degas the fluorocarbon indicating solution, ECI 22-00350-001. Degas at a pressure level of 0.1 inch Hg maximum until no more bubbles appear or 20 minutes, whichever is greater. Use a test piece immersed in solution for this operation.

d. Adjust nitrogen supply, ECI 22-00262-001 to 4 to 6 psig.

e. Switch solenoid valve to ON position.

f. Connect device(s) to be tested to the suspension mechanism and adjust to hang vertically.

g. Move piston shaft upward to immerse device(s) in indicating solution. Device(s) to be tested shall not make contact with glass beaker.

h. Place bell jar over mechanism and evacuate to maximum pressure level of 22 inches as read on the gage.

i. Appearance of bubbles denotes a leaker. Note location of bubbles and the pressure level at which leakage was first evidenced. If no bubbles appear at 22 inches of Hg, the device is acceptable. (Leak rate of $1 \times 10^{-5}$ cc/sec.)

j. Turn off vacuum pump, and solenoid valve. Open nitrogen supply valve to piston slowly until device(s) is (are) in line with spray nozzle.

k. Open vent valve to dry device with nitrogen while venting bell jar.

l. Remove tested device from suspension mechanism and mark any defective areas of device.

Records are kept in the Daily Inspection Records "Microelectronics," Production Inspection and Test (PIT) Log, and Quality Assurance Laboratory Report. The QA Lab reports document the results of the fine and gross leak test.

Visual Inspection of Marking.

a. Markings shall be free from ragged edges, wrinkles, scratches, unbalance of characters, and excess marking material.

b. Illegible or incomplete markings shall be cause for rejection.

c. Misalignment of marking is acceptable providing legibility is not affected.

d. Foil plates shall show good adhesion, and there shall be no bubbles, raised portions or curling at the edges. Location shall be in accordance with applicable documents.

Permanency of Marking.

a. Markings shall be capable of withstanding, without becoming illegible, all the environments for which the assembly has been designed.

b. Thoroughly cured markings shall not be removable by application and stripping of masking tape conforming to MIL-T-21595.

c. Markings which are flaking or otherwise showing evidence of permanency shall be cause for rejection.

Test for Permanency - Standard Method. The following test shall be conducted at least once every three months of continuous production on five units selected at random from a production run.

The samples shall be immersed for 15 minutes in Trichloroethylene ECI 22-00094-001. After immersion, the samples shall be rubbed briskly with a dry cloth five strokes in one direction followed by five strokes at right angles to the initial stroke. Marking must remain legible after this test.

| DASH NO. | MARKING METHOD | COLOR | MATERIALS |
|---|---|---|---|
| -001 | Stencil | Black | Lacquer Per TT-L-58, Type II (Ref. 22-00014) |
| -002 | Stencil | White | or |
| -003 | Stencil | Contrasting | Enamel per TT-E-529 (Ref. ECI 22-00124) |
| | | | or |
| | | | Ink per TT-I-558 (Ref. ECI 22-00023) covered with clear lacquer per TT-L-58 Type I (ECI 22-00014-001) See 3.3.9 |
| -010 | Rubber Stamping | Black | Ink, Marking, Component-Epoxy Fungus Resistant |
| -011 | or | White | (Ref ECI 22-00346) |
| -012 | Printing Machine | Contrasting | Recommended cure: 2½ hours at 125°C |
| -101 | Silk Screen | Black | |
| -102 | Silk Screen | White | Ink, Silk Screen Process 22-00168 |
| -103 | Silk Screen | Contrasting | |
| -201 | Foil Plate | Contrasting | Foil Plate per ECI 48-00113, Pressure Sensitive Adhesive per ECI 48-00112 |
| -202 | Foil Plate | Contrasting | Foil plate per ECI 48-00113 Adhesive per 22-00071-007. |

TABLE 2-2. DASH NUMBERS

DATA SHEET 2.9-1

PROCESS STEP Sealing
Glove Box Sealer

DESCRIPTION OF PROCEDURE A glove box provides an inert moisture controlled work area. This work area is reached through ports to hermetically seal flat packages and header packages. All equipment necessary for sealing and repairing is contained in the closed box. Air locks are at both ends to provide access to the interior. A moisture analyzer is used to monitor water vapor in the gas exiting the glove box.

FREQUENCY OF TEST N/A

SAMPLE SIZE N/A

MEASURING INSTRUMENT· Flow meters for helium and nitrogen, vacuum gages, a Harrel TE-16 Temperature Controller, a Digital Thermocouple for measuring heater block temperatures, and a Beckman moisture analyzer.

ACCURACY IN PERCENT Beckman Model 97 Moisture Analyzer is ±5% full scale on any range.

LIMITS OR TOLERANCES Temperature ±5°C.

DATA RECORDING METHODS All work follows a process control sheet for each different type package.

CALIBRATION PROCEDURE· Calibrated quarterly by ECI Calibration Department.

ACTION TAKEN IF TOLERANCES ARE EXCEEDED Immediate calibration or repair.

DATA SHEET 2.9-2

PROCESS STEP Sealing
Flat Pack Sealer

DESCRIPTION OF PROCEDURE· The Dix Flat Pack Sealer is a semi-automatic sealer modified to accommodate packages 1/4 inch square to 2 inch square by one inch deep. Heat is applied to make a seal around the periphery of a package only. The substrate area temperature does not exceed 104°C. When the seal area reaches the eutectic point reflow occurs. During the seal process a unit is evacuated and/or filled with inert gas. It then is vacuum pumped again and filled with helium/nitrogen mixture for a leak rate test.

FREQUENCY OF TEST· N/A

SAMPLE SIZE· N/A

MEASURING INSTRUMENT: Dix Sealer contains meters for helium, vacuum, nitrogen, temperature, gain control, annealing control, and pressure. The steps may be programmed so that the cycle is automatic.

ACCURACY IN PERCENT. N/A

LIMITS OR TOLERANCES Temperature controlled to ±1.0 degree C.

DATA RECORDING METHODS All work recorded on process control sheet for each package.

CALIBRATION PROCEDURE. Every 90 days by ECI Calibration Department.

ACTION TAKEN IF TOLERANCES ARE EXCEEDED Immediate repair or calibration.

## DATA SHEET 2.9-3

PROCESS STEP: Sealing
Gross Leak Test

DESCRIPTION OF PROCEDURE· Essentially this method involves evacuating the test chamber rather than pressurizing it. The device under test is immersed in a container with fluorocarbon solvent and placed in a chamber by standard vacuum techniques. Leaks are detected by bubbles in the fluorocarbon. The device is removed from the liquid prior to releasing the vacuum and is spin dried in nitrogen as the test chamber is vented

FREQUENCY OF TEST. This test is performed on every sealed package produced within 4 hours after seal.

SAMPLE SIZE 100%.

MEASURING INSTRUMENT. Vacuum gage and calibration chart established by using controlled (standard) leak.

ACCURACY IN PERCENT. A sensitivity of $5 \times 10^{-6}$ cc/sec can be achieved.

LIMITS OR TOLERANCES No visible bubbles.

DATA RECORDING METHODS. Data sheet accompanies every flatpack and gross leak test results are recorded.

CALIBRATION PROCEDURE. Equipment is calibrated quarterly by ECI Calibration Department.

ACTION TAKEN IF TOLERANCES ARE EXCEEDED: Immediate rework of package and re-test. If rework on seal is not possible, circuit must be removed and placed in a new package.

DATA SHEET 2 9-4

PROCESS STEP Sealing
Fine Leak Test

DESCRIPTION OF PROCEDURE: Fine leak test is performed using a Veeco Model MS12ABP mass spectrometer type instrument Packages are sealed in a helium atmosphere. When placed in the MS12ABP and pumped down to $1 \times 10^{-5}$ Torr any fine leaks will immediately be indicated by the MS12ABP

FREQUENCY OF TEST Test is performed once on every package.

SAMPLE SIZE: 100%.

MEASURING INSTRUMENT Model MS12ABP Veeco Mass Spectrometer Leak Detector.

ACCURACY IN PERCENT: $5 \times 10^{-12}$ cc per sec.

LIMITS OR TOLERANCES $5 \times 10^{-7}$ cc/sec or as specified.

DATA RECORDING METHODS On PIT tag.

CALIBRATION PROCEDURE: MS12 is calibrated (tuned and peaked) before each run and the instrument is checked against a standard leak every three months minimum.

ACTION TAKEN IF TOLERANCES ARE EXCEEDED. Package is returned for repair or rework. It may also be submitted for MRB action.

2.10 Electrical Test. In order to ensure proper electrical performance and to detect any abnormalities at the earliest stage in the assembly of the hybrid microcircuit a minimum of three testing steps should be included; namely, (1) Pre-seal Testing, (2) Post-seal Testing, and (3) Final Product Acceptance Testing. The specific parameters to be verified during electrical testing should be available from the product specification, but in the cases where specific parameters are not available, ECI determines the critical parameters and notifies the contracting agency of the proposed test criteria. The test criteria includes functional testing which can be implemented readily with a minimum of monitoring equipment and yields sufficient evidence that an assembly and/or subassembly is operating properly. The final acceptance testing includes static, dynamic, and temperature testing (as required for product compliance) which is adequate to determine satisfactory circuit performance within all specified parameter limits. All electrical tests are performed on 100 percent of the production lot.

2.10.1 Seal Testing. At any point in the assembly where a discernible electrical function can be verified, a functional test is performed. Where more than one subassembly is used to produce a functional circuit, each subassembly is functionally tested (when practical) to expedite troubleshooting and to preclude further effort being expended on a defective assembly.

Test Area. Whenever possible, the pre-seal test area is located adjacent to the assembly area for efficient repairs and minimum handling of the unsealed assembly. If a clean room environment is not available, the tests must be performed in a laminar flow bench.

Test Equipment. For pre-seal testing a probe station is used where the electrical connections to the assembly can be made with pressure probe tips positioned by "joystick" operation in the x and y plane

and with simultaneous setdown of aligned probe tips in the vertical (z) plane. The probe station is equipped with stereo optics having sufficient magnification to properly position probe tips on metallization areas.

As a minimum the test station has an oscilloscope, function generator, regulated power source, and metering for voltage/current/resistance. ECI recommends that no temperature testing is performed on a pre-sealed assembly to preclude environmental contamination such as corrosion from occurring. If temperature testing is necessary, the assembly is processed through a cleaning procedure immediately following the test and prior to any subsequent assembly processing.

When operational trimming requires a selected value component decade unit(s) with appropriate tolerance or a calibration chart is connected through the probe station for determination of the required value.

Calibration of Test Equipment. Each piece of test equipment has a calibration tag which indicates the data of the previous calibration and the date of the next required calibration. Whenever possible, the test operator verifies proper operation of the test equipment prior to performance of any electrical testing of the microcircuit.

Data Records. ECI requires that any electrical testing on customer products shall be recorded in engineering notebooks for permanent record in those cases where functional (any testing other than the customer acceptance test) testing is accomplished. The information which is recorded includes the test circuit, parameters tested, and any unique procedures. Any test performed on the assembly is also indicated on the PIT tag.

Frequency of Testing (Pre-Seal). As a minimum ECI requires that a functional test is performed following assembly inspection and immediately prior to the final pre-seal visual inspection. When a test

indicates a performance deficiency troubleshooting is performed on the assembly. After the defective component is located and appropriate repair procedures have been instituted the test is repeated.

2.10.2 Post-Seal Testing. Following the seal verification of a hybrid microcircuit an electrical test similar to the pre-seal test is performed on the assembly. Although the environmental conditions of the test area are not restricted, ECI (when practical) uses the same area and equipment as that used for pre-seal testing to ensure correlation of data.

At this point temperature testing is often performed to verify proper circuit operation within specified limits. As a general practice the temperature extremes are chosen 5 degrees centigrade greater than those required for specification compliance (i.e., circuits requiring -55°C and +125°C operation are tested at -60°C and +130°C) The 5°C guard limits ensure required performance within the specified limits and will indicate any marginal conditions of the design.

2.10.3 Final Product Acceptance Testing. For any production microcircuit (other than nonflight prototypes or engineering models) an acceptance test specification is prepared and used for product acceptance testing. The specification defines the type of test equipment, test circuit(s), test sequence and description, and test parameters with required tolerances. The test data sheet for final product acceptance is included with the assembly when it is shipped to the contracting agency.

Product acceptance testing at ECI requires the presence of an ECI Quality representative, an authorized test operator, and a customer technical representative (when required by contract).

The acceptance testing verifies that the microcircuit complies in all respect with the requirements of the customer procurement specification.

# SECTION III

# RECOMMENDATIONS

3.1 Discussion. A reasonable probability exists that a hybrid circuit selected at random from a qualified vendor would perform satisfactorily during a long term space mission. To ensure to a high degree of probability that the circuit would so perform is a much more significant undertaking. In Chapter II of this report, the methods used by ECI to obtain reliable circuits were discussed. While many of the controls which have been implemented would be applicable for extended life performance requirements, insufficient information exists to safely predict the life of such circuits much beyond 1000 hours. Since the ability to predict long-term behavior in a partially known environment is the overall objective and failure rates several orders of magnitude less than the Apollo Program are required,it would appear that the entire system of module fabrication must be subject to control. This fabrication system may be generalized into four separate categories.

a. Circuit Design
b. Materials and Processes
c. Control Methods
d. Verification Methods.

Most of the topics associated with each category are beyond the scope of this report except for some general comments.

Circuit Design. Adequate design margin must exist in a circuit design so that long term degradation due to radiation damage, thermal aging, or other causes can be compensated. Assuming that multiple sources of microcircuits will be utilized, electrical design guidelines with standard derating factors should be established. Circuit designers

should be permitted to use only parts from a preferred list such as those from a NASA Certified manufacturer of monolithic microcircuits. Line Certification should be extended to all discrete parts fabrication including the package that will be used to house the module.

Materials and Processes. Dissimilar materials such as metals in mutual contact still pose reliability problems. A monometallic interconnect system would help alleviate the situation although different problem areas may arise. These latter problem areas should receive some in-depth research so that a choice may be made whether to use either gold or aluminum exclusively. It is not clear if some of the more complex metallurgical schemes that have been proposed have subtle failure modes that are as yet undetected. Most of these schemes rely upon a barrier layer to prevent interlayer diffusion of metals but these barriers are usually disrupted at a bonding interface.

The use of adhesive materials to bond substrates into packages and discrete devices to substrates must be carefully controlled. Many different compounds are used somewhat indescriminately and their long-term behavior is not well known.

Unnecessary materials such as glaze on alumina substrates could be eliminated. The smoothness of unglazed ceramic substrates has improved markedly in the past few years and high quality resistor-conductor networks may be fabricated on such surfaces.

Control Methods. The two basic approaches used to control the quality and reliability of a microcircuit module are·

a. Inspection and test of the module, and

b. Control of the processes used to manufacture the module.

The predominant philosophy of MIL-STD-883 is expressed by (a) and (b) relates to Line Certification. Each approach usually contains elements of the other with a trend toward imposing both approaches where reliability objectives warrant. An overall approach is certainly indicated for deep space probes.

3.2 Recommendations. Some comments regarding the objectives of a Line Certification Document are as follows

a. Line Certification is process oriented and therefore should consider the end item use more specifically. For example, if the module environment will exceed a specified level of radiation, certain materials and therefore processes are more desirable. It would be worthwhile to consider classes of Line Certification such as Radiation Environment, Thermal Environment, and High Acceleration Environment similar to the levels or classes of reliability testing imposed by MIL-STD-883.

b. Line Certification should be imposed on all suppliers of parts to the prime hybrid microcircuit manufacturer particularly when extreme levels of reliability are desired.

c. Burn-in at the component level should be imposed at the hybrid microcircuit manufacturer's facility as the prime component screening test. This should not supplant burn-in at the module level which would serve to verify integrity of the entire assembly.

d. To eliminate unproven materials and techniques and reduce somewhat the technological variations from vendor to vendor, some form of standardization should be employed. A stringent set of quidelines for microcircuit design is recommended as the most expedient method of achieving standardization. For example, if active device burn-in is imposed, no proven alternative to the carrier concept exists.

e. Adhesive bonding with organic compounds is one of the undesirable features, from a reliability point of view, of the carrier hybridization approach. Bond strength is adequate and stress problems are minimal for small components, but unknown potentially harmful side effects are felt to exist. Considerable emphasis should be placed on this operation in the Line Certification Program. Other areas that fall in this same category are the module package, final substrate-package assembly, and sealing.