FINAL REPORT

ELECTRONIC SOLAR ARRAY SIMULATOR

November 1970

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA 90278

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ELECTRONIC SOLAR ARRAY SIMULATOR

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FOREWORD

This Final Report on the Electronic Solar Array Simulator was prepared for the National Aeronautics and Space Administration, Goddard Space Flight Center, Greenbelt, Maryland, in fulfillment of Contract NAS 5-21034. The report covers work performed from 30 June 1969 through 2 November 1970, and documents and summarizes the results of this contract effort. The work was conducted under the technical direction of the Space Power Technology Branch of NASA/GSFC.

Distribution of this document is established by the Contracting Officer, A. L. Essex, or his authorized representative. Communications relative to this contract should be directed to the above contract specialist, Attention Code 245, Goddard Space Flight Center, Greenbelt, Maryland 20771.

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1. INTRODUCTION

This report presents the results of tradeoff studies on multi-kilowatt solar array simulators, performed by TRW Systems for NASA's Goddard Space Flight Center on Contract NAS 5-21034. The aim of the program was to provide the technological basis for the design of high power, high frequency response simulators, and to serve as a review and amplification of the basic problems that can be encountered in such designs.

The primary source of electrical energy for the majority of space satellite power systems is derived from the conversion of the sun's radiant energy by an array of solar cells. Spacecraft power systems must be tested and evaluated and, therefore, a problem is confronted about what to use as a substitute for the array. This problem is further compounded as array power requirements get larger and users want to have built-in programmer capability for varying the static I-V curve.

Section 5 presents the various tradeoff studies which were conducted during the course of the program. Section 6 presents three simulator concepts which were selected based on the results of the tradeoff studies.

2. SUMMARY OF TRADEOFF STUDIES AND CONCEPTS

2.1 TRADEOFF STUDIES

The tradeoff studies were conducted to establish the groundwork for the future design of a 20 kilowatt solar array simulator (SAS). In general, the problems, techniques, and conclusions revealed in these studies are applicable to all multi-kilowatt simulator designs.

The studies were limited to six areas. In Section 5.1, available standard components and power supplies were reviewed so that optimum module size for the 20 kW SAS could be determined. As a result of contacts with leading manufacturers of power supplies, it was found that none produced a single standard unit capable of powering a simulator having to meet the 20 kW SAS requirements (90 to 200 V, 90 to 200 A). Thus, multi-supply configurations had to be considered. Furthermore, the use of transistor-series regulated supplies to obtain nearly ripple-free voltage was found to be impractical because of the large number of units needed. This type of supply is designed for low power applications. There is one SCR regulated supply, of which only two units would be required for this application. This model is adjustable from 0 to 135 volts and 0 to 300 amps. The best-manufacturer recommended models for use as power sources to a 20 kW simulator are discussed and their specifications are compared. The number of supplies needed of each model, total cost, and overall rack space required are listed in Table 5.1-1.

Pitfalls and techniques associated with series and/or parallel connecting of supplies are discussed in Section 5.2. It points out that the isolation voltage rating (voltage that can be connected between either output terminal and chassis ground) of each supply limits the total output voltage of a series configuration. The models evaluated in the preceding section all had sufficiently high rating for use in the 20 kW SAS system. These supplies also have protection against damage from the application of reverse potential that can occur momentarily when the configuration load is short-circuited.

For parallel operation, power supplies must feature constant voltage/constant current or constant voltage/current limit automatic

crossover operation, otherwise large circulating currents can be caused between supplies by the small voltage differences that invariably exist between voltage sources. In order to assure reasonable sharing among supplies, whether in series and/or parallel, various master-slave schemes are covered.

Section 5.3 reviews the tradeoff decisions between analog and digital generation of an array's I-V characteristic and techniques for programming it as a function of time. Schemes considered were digital generation and programming, analog generation and programming, and analog generation with digital programming. It was found that the digital generating scheme, which employed a digital computer in the control loop to provide a reference voltage or current to a series regulator in response to sampled output current or voltage, has two serious disadvantages. One is the inability to simulate the variable impedance of an array as a function of operating point. The other is that if a voltage regulator is used in conjunction with the computer, the system can only handle load changes that stay within the so-called "constant voltage" region of the I-V array curve. In other words, a voltage regulator cannot simulate the constant current characteristics that an array has below the knee of the I-V curve. Conversely, a computer-current regulator combination will only be adequate in the "constant current" region of the curve. As a result of these inadequacies, analog generation with digital programming is considered a preferred method. This method uses a forward biased solar cell as the reference element in a unique feedback circuit that not only amplifies the single cell static characteristics to that of a full array, but also amplifies the dynamic characteristics.

Section 5.4 concentrates on solar cell frequency response (cell impedance). Material contained in this section correlates test data with P-N junction theory. It also shows that a cell exhibits the same impedance when it is forward biased as when it is illuminated. A technique is offered by which an array's impedance can be predicted from single cell data. This parameter is important to power conditioner designers because it affects the dynamic behavior of regulators used to control the array.

2.2 DESIGN CONCEPTS

Based on the tradeoff studies, several approaches for simulating a 20 kW array were considered. Conceptual designs of the three more promising ones are summarized below.

Section 6.1 describes the first approach which is a modular configuration of expanded FRSAS basic units. The basic FRSAS (Fast Response Solar Array Simulator) is a 750 watt simulator that can be increased to 5 kW. For efficient use of the power supplies in the basic unit, module expansion to 3 kW is preferred for this application. The basic simulator is TRW Systems' latest contribution to the state of the art in array simulation. It features a technique for amplifying the static and dynamic characteristics of a single cell to that of a full array. It was designed and developed through work sponsored by the NASA Goddard Space Flight Center under Contract NAS 5-11581. The 20 kW configuration would consist of two banks in series of five FRSAS expanded (3 kW) modules in parallel, each with its own controls, power supplies, programmer, power stages, and protection circuitry. Each module offers excellent static and dynamic simulation plus means for programming the effects of temperature, illumination, and spin variations experienced by spacecraft arrays.

A power supply approach is discussed in Section 6.2. This consists of two high voltage-high current power supplies of the constant voltage/current limit type in series. Because the slopes exhibited by these supplies are relatively sharp, slope generators (adjustable resistor banks) are used between the supplies and the load, allowing some degree of slope matching to the I-V curve being simulated. The advantages of this approach include minimum equipment cost, size and weight; ease of transportability; ease of remote programming; minimum setup and checkout time; and minimum maintenance. The disadvantages include poor static and dynamic impedance simulation; poor "knee" simulation of an array's I-V curve; poor peak to peak ripple; and poor response time. With modification to the supplies' internal controls, remote programming can be possible.

An interesting approach incorporating a bank of diodes driven by a power supply is presented in Section 6.3. If diodes with characteristics

similar to those of the solar cells being simulated can be used, the static and dynamic simulation can be extremely good. Two alternatives are offered. One is where the bank is driven directly by a constant current supply. In this case the advantage of the diode bank's impedance will depend on the output impedance of the constant current source. The other alternative considered is where the source is a constant voltage supply. This supply, in turn, drives the bank that is in series with a large power stage used as a constant current sink. The idea here is to obtain a much higher output impedance, as seen by the diode bank, than that available in standard constant current supplies. Whether this would be possible would depend on the characteristics of the transistors used in the power stage. This diode solar array simulator (DISAS) offers a compromise between the two previously discussed concepts, however, it is the most difficult to program for voltage variations.

Section 6. 4 describes the means used in each of the design concepts to simulate effects of temperature, illumination, and spin ripple. In an array, temperature affects mainly the constant voltage region of the I-V curve, while illumination affects mainly the constant current region. On spinning spacecraft, if the geometry of the solar panels and spacecraft is such as to cause periodic shadowing, the constant current region is mainly affected.

The FRSAS 3 kW modules used in the 20 kW simulator would each have a digital programmer for varying resistor dividers in its own controller. By changing the feedback resistance, the output voltage varies. By changing the reference current to a new steady state value or by modulating it, the output current varies accordingly. A total of 30 resistors would have to be programmed if equal sharing is desired among the modules since ten 3 kW modules are required and each has three programmable dividers.

The power supply SAS is the easiest to program. The front panel controls can be replaced with resistor dividers which can be controlled by the type of programmers developed under the FRSAS contract. Since each supply has only two controls, a total of four programmers at the most is all that would be needed.

The diode SAS can be programmed for illumination and spin effects simply by varying the constant current source or the constant current sink if that is used. Variation of V_{OC}, however, is more difficult because diodes have to be bypassed to change the total bank voltage. Depending on the resolution desired, this would take a considerable number of high current relays connected across taps on the diode bank. The smallest change possible would be about 0.6 volts, unless of course, special heater elements were used to vary the temperature of the bank modules.

In Section 6.5 the estimated output impedance capabilities of the three workable concepts are described and compared. The diode SAS is shown to have the least error in simulating array impedance. However, the graphical comparison assumes the diode characteristics match the cell characteristics of the array being simulated. No attempt was made to determine what diode types were best suited for array simulation. Use of general purpose diodes, which typically exhibit high impedance bandwidth, will result in the diode SAS having a much greater error in array impedance simulation than the FRSAS. The power supply SAS exhibits the poorest response because on either side of the maximum power point of the I-V curve, the impedance is fixed and independent of operating point. On the other hand, the impedance of the FRSAS and DISAS varies continuously with operating point as does a real array. All three types of simulators will be affected by the output impedance of the power supplies used.

Section 6.6 is a brief discussion of the fault and overload protection that is or can be designed into the circuitry of the concepts described above.

3. CONCLUSIONS AND RECOMMENDATIONS

3.1 CONCLUSIONS

The overall conclusions of this study are the following:

- Development of a high power, high frequency response solar array simulator which meets all of design goals of this program is not economically feasible. From a design standpoint, the problems encountered in stabilizing the feedback scheme of concept number one, which is the most promising of the three, would undoubtedly become more severe when building up to a 20 kW configuration. Consequently, additional compensation to alter the already limited frequency response of this concept might become necessary to obtain a stable high power system. As a result, this system would exhibit a rather large error in trying to simulate the output impedance of a large array. From a standpoint of space required, ten FRSAS expanded units would occupy approximately 1260 cubic feet. Cost of parts alone would be about $200K.

- Concept number two, the power supply approach, could economically achieve the power requirements but would provide only marginal EI curve simulation and extremely poor frequency response.

- The frequency response of an ideal array (i.e., its impedance as a function of frequency) is determined by the type of cell being used. The impedance of an array at a given operating point will exhibit the cell time constant but not necessarily the cell impedance magnitude. Both parameters vary with operating point. Forward-biased cell ac measurements can be used to determine illuminated array impedances. From the standpoint of main bus regulator design, knowledge of array impedance and proper simulation thereof is important because it can affect stability.

- Implementation of multi-kilowatt solar array simulators requires the use of SCR-type power supplies to provide raw power. In general, fully transistorized standard supplies do not exceed an output capability of 200 watts so that too many units would be required for a 20 kW power system.

- There are single supplies available that can provide up to 40 kW but their current/voltage combinations do not meet the ESAS requirements given in Section 4. Therefore, at least two high current/high voltage supplies are necessary. To allow series/parallel combinations of supplies, each must include constant voltage/constant current or current limit capability.

3.2 RECOMMENDATIONS

As a result of these studies also, recommendations can be made for the type of simulator to use in testing. The PCE (power conditioning equipment) should be tested in a scaled-down configuration with a fast response simulator (for example, two 1.5 kW FRSAS's in series) and a partial load. The array time constants, which can affect the transfer function of the PCE's regulator, would be simulated. Though the 20 kW array impedance magnitude would not be simulated, its effect on the transfer function might still be realized by adjusting the partial load. If the ratio of the partial load impedance to the impedance of the scaled-down array being simulated is the same as that for the array and load in the 20 kW system there will be very little difference in the PCE's dynamic performance.

If it is not possible to establish the impedance ratio described above, then the partial load impedance should be adjusted high so that the test condition represents a high loop gain case. Higher loop gain would tend to make the regulator less stable. If the regulator is found to be stable in this scaled-down test, the gain and phase margins should improve when the PCE is incorporated in the 20 kW system. That is, as the array parallel size and/or load current increase, regulator stability improves because loop gain decreases. Thus, a scaled-down test can be performed on the PCE to detect a marginal regulator design.

It is recommended also that one of the following two methods be used for total system testing. If the full array is available, provisions should be made so that it can be used as a diode array in conjunction with a constant current source. In this configuration, the system will behave very much like when it is illuminated. If the array is not available or cannot be used because of thermal considerations, then the power supply solar array simulator discussed in the report should be used.

4. STATEMENT OF WORK

4.1 INTRODUCTION

The majority of space satellite power systems used for spacecraft design are of the solar conversion-energy storage type of power system. The primary source of energy for these systems is derived by conversion of the sun's radiant energy into electrical power. The basic conversion device is the solar cell, but because of its small size many solar cells are connected in various series and parallel combinations to form a larger electrical power source called the solar array.

In the testing of spacecraft power systems it is often necessary to simulate the solar array. At present, standard laboratory type power supplies are used for this function. However, as the technology advances more accurate simulation of the array is required. Frequency responses of standard laboratory power supplies are in the order of 1 to 10 Hz, while the frequency response of the solar array is in the order of 300 to 30,000 Hz. Thus for advanced power system testing and design evaluation, the present laboratory equipment is inadequate. This study provides the technology basis for the design of large power, high frequency response solar array simulators.

4.2 GENERAL

The contractor shall furnish the necessary qualified personnel, material, facilities, and equipment necessary to develop the basic technology concepts and a design specification for a multi-kilowatt, fast frequency response solar array simulator (SAS). In general the contractor's effort shall include but not be limited to:

a) A review of the available components and standard power supplies in order to determine the optimum size module for the SAS, in the specified power ranges. The contractor shall also determine the various series and parallel combinations of the modules required to produce the maximum specified power output.

b) Review and revise when necessary the tradeoff decisions between analog and digital control of the module output I-V characteristics. Particular attention should be paid to the problems of operating the modular units in the series and parallel connections.

c) Review the various techniques of programming and control necessary to simulate the variations in solar array temperature, intensity, and spin ripple.

d) Evaluate the output frequency response characteristics to be compatible with the present and anticipated future characteristics of state of the art solar arrays.

e) Evaluate the necessary fault and overload protection schemes to protect the SAS from external load faults, internal malfunctions, and to protect the external load from SAS malfunctions.

f) Provide a final technical report describing the work accomplished in technical detail.

4.3 TECHNICAL CHARACTERISTICS

- Power Output — The modular units of the SAS shall be capable of being connected in series or parallel combinations to form a power output capability of between 5 and 20 kilowatts. The nominal output shall be adjustable within this range and specific variations shall be programmed about the nominal setting.

- Voltage — The open circuit voltage shall be capable of supplying the output power between the voltage range 90 to 200 volts.

- Current — The short circuit current capability of the device shall be adjustable in the range 90 to 200 amperes.

- Temperature Simulation — Both current and voltage of the simulated output shall vary over an array temperature range of -100°C to +100°C. The temperature time profile shall be variable and the limits adjustable in accordance with the settings of the program control unit.

- Frequency Response — The SAS shall have an output impedance that is flat for all operating points out to 5 kHz and then falls off at a rate similar to the normal solar cell.

- Stability — The SAS shall maintain long term stability and repeatibility of any particular setting within ±0.5 percent.

- Ripple — The steady state ripple shall be less than 0.5 percent of V_{oc} or 100 mV peak to peak, whichever is less.

- Curve Shape — The SAS shall exhibit an output I-V characteristic that produces a smooth rounded knee.

- Control Unit — The SAS shall be driven from a control unit to simulate temperature, intensity, and spin variations of the solar array in a time variant domain. The unit shall be capable of external digital control as well as internal control and every effort should be made to use the same controller as that developed in the referenced document.

- Calibration — The SAS shall have a built-in load which can sweep the entire range of the I-V characteristic at any intermediate time for calibration and checking purposes. It shall be controlled manually and the output shall be available to external recording devices such as an X-Y plotter.

5. TRADEOFF STUDIES

In general, conceptual design work is seldom complete without considering tradeoffs. These allow a prospective user of a particular system to make a wise choice in selecting one that is consistent with his needs. Tradeoff studies were directed toward determining what standard power supplies are available for this large power application; what problems are associated with composite configurations when one supply is not sufficient to meet the power requirements; what are the advantages and/or limitations of the use of digital or analog control; what means can be used for programming the output characteristics; and how the frequency response of a given array can be predicted. The results of these investigations are contained in this section.

5.1 COMPONENTS AND POWER SUPPLIES

A survey was conducted for a power source with the following specifications:

1) 90-200 V, 90-200 A, 5-20 kW
2) 100 MV pk-pk ripple
3) Regulation 0.5%
4) Stability 0.5%

The power supply manufacturers who were contacted were: Trygon, Hewlett-Packard, Kepco, Lambda, Christie, Sorenson and Electronic Measurements. None of the manufacturers could provide a single power source to meet the required specifications. Series/parallel techniques using existing standard power supplies were discussed with each vendor.

The ripple characteristics of individual manufacturers' power supplies will be discussed in this section. Most of the large supplies employ SCR regulated outputs. This SCR regulation technique induces a high spike noise onto the output and input lines of the supply. The spike amplitudes are typically specified at 1 volt to 2 volts pk-pk, which is much larger than the allowable 100 mV pk-pk ripple. One manufacturer, Electronic Measurements, uses a special filter technique to reduce the

ripple to 100 mV pk-pk. Electronic Measurements manufactures two models with power outputs which are practical for the ESAS application: SCR 50-200, 50 volts - 200 amps; SCR 100-100, 100 volts - 100 amps. Four supplies of either type would be required to provide sufficient power. The total ripple from four supplies could exceed the required 100 mV specification. However, if the ESAS was in essence a voltage regulator, the ripple to the output would be reduced by some factor. The regulation factor has not been calculated at this time.

Christie Electric offers a SCR regulated supply, model 2C0135-300E4S, with a range of 2 to 135 volts and 0 to 300 amps. With certain options added, this standard model can be made to exhibit constant voltage-constant current with automatic crossover. The ripple quoted for this unit is 100 mV rms, which is approximately 300 mV peak to peak according to the manufacturer. Two of these supplies would suffice for this application. To include the options the model number must be specified as 2C0135-300EBPX-S.

There are two series transistor regulated power supplies which are practical for the ESAS application. These transistorized supplies have ripple specifications well within tolerance. The first Christie Electric's Model MH36-200KKGG24L, provides 15-36 volts and 0-200 amps. The pk-pk ripple of this supply is 2.8 millivolts. The second, Hewlett-Packard's Model 6269B, provides 0-40 volts and 0-50 amps. This supply is the smaller of the two, and 16 would be required to provide the necessary power. The output ripple is 5 mV pk-pk.

The four power supplies previously discussed were considered for the ESAS application. The supply specifications are listed in Table 5.1-1. The transistorized Christie supply has the best specifications. However, it is the most expensive and a stacked configuration requires considerable rack space for this application. The Electronic Measurements supply has the worst specifications, however, the cost and packaging are considerably better. The Hewlett-Packard supply is a compromise between these two but quite a large number are required. The last model listed in Table 5.1-1 is a better choice for the ESAS application. Even though it will require greater space, the price is reasonable and setup and programming will be the easiest.

Table 5.1-1. Standard Power Supplies Considered for ESAS Application

Mfg.	Model	V-A	Isolation Voltage (V)	Reg.	Ripple	Stability	No. Req. (*)	Total Cost	Total Rack Space
HP	6269B	40-50	300	0.2% ±100 mV	5 mV p-p	0.25% +10 mV	16	$14,000	37,088 in^3
Elect. Meas.	50-200 100-100	50-200 100-100	300	0.1%	100 mV p-p	0.2% +40 mV	4	$10,000	19,000 in^3
Christie	MH36-200	36-200	1500	0.01% or 25 mV	2.8 mV p-p	10 mV ±0.005%/°C	6	$22,400	65,382 in^3
Christie	(2C0135-300EBPX-S)	135-300	1000	0.1% or 100 mV	100 mV rms	10 mV ±0.005%/°C	2	$17,800	90,142 in^3

(*) Number of supplies required for a 20 kW system.

The discussion of series/parallel techniques indicates that parallel operation of voltage regulators should be avoided if possible. The four power supplies under consideration allow for several different power module configurations which would utilize a controller and power stages similar to the ones developed under the FRSAS program. The modules could be paralleled up to the current limitations of each supply. Therefore, each supply would be isolated from the others. The isolation voltage rating is sufficient as indicated in Table 5.1-1. Smaller power supply voltage will reduce transistor secondary-breakdown problems.

5.2 SERIES/PARALLEL TECHNIQUES FOR POWER SUPPLIES

Some of the problems involved with power supplies connected in series and parallel will now be discussed. Two or more dc regulated power supplies used as voltage regulators can be series connected to increase the total output voltage to the sum of their individual voltage settings up to the maximum voltage limit allowed by the isolation voltage specification for each power supply. The maximum isolation voltage

specifies the amount of additional voltage that can be connected between either terminal of the power supply and its grounded chassis, not including the power supply's own output voltage. The isolation specification derives from the voltage breakdown rating of the printed circuit boards, capacitors, sockets, connectors, etc.

Series connected power supplies should also be protected against the possibility of a reverse potential. (Reverse potential would occur when the load is short circuited). Reverse potential is undesirable because of the polarized components (filter capacitors) in the output circuit of a typical regulated power supply. The standard precaution is to connect the diode in the normally nonconducting direction across the output terminals of each power supply in a series string. Each diode must have a PRV rating at least equal to the maximum supply voltage of the individual supply to which it is connected, and should be able to conduct the maximum short circuit current indefinitely.

When voltage regulators are paralleled, their terminal voltages are all, of necessity, identical. Since it is unlikely that independently adjusted supplies will have the same identical terminal voltage before being paralelled, the minute differences that are bound to exist will inevitably cause large circulating currents through the near zero source resistance of the good voltage regulator. This characteristic prohibits paralleling without recourse to one of the following techniques. A voltage/current regulated power supply featuring automatic crossover between current and voltage regulation or one containing a good current limiter can be paralleled using the self-limiting feature. The maximum voltage will be the highest setting of any power supply in the parallel string. The maximum current is the sum of the individual current limit settings. One precaution that should be observed is to always have at least 10 percent of the voltage control setting as the minimum voltage setting. The reason for this is that the voltage control "sees" the entire output terminal voltage since the parallel terminal voltage is controlled by the larger of the two voltage settings. If the control setting potentiometer approaches zero resistance, the maximum current rating of the potentiometer may be exceeded.

Another technique employed to assure the equal sharing of load current is to use one regulated dc supply, designated as master, to provide control for the remaining supplies, designated slaves. One of two master-slave techniques may be used. The first method is to make the comparison amplifier of one regulated supply drive two or more sets of pass elements. Therefore, all will conduct equally, and, if paralleled, will generate the identical terminal voltage without a circulating current. The number of identical supplies that can be paralleled in this way depends on the amount of drive that can be obtained from the active comparison amplifier.

A second master-slave technique, known as parallel programming, employs a separate master control supply to drive all of the paralleled power supplies. The master control supply itself does not deliver any power to the load and need only be capable of generating the desired reference voltage.

5.3 DIGITAL VERSUS ANALOG CONTROL AND PROGRAMMING METHODS

Tradeoff studies were performed to determine the optimum method of generating the basic V-I characteristic and of programming this characteristic as function of time. Three basic schemes were considered: digital generation and programming, analog generation and programming, and analog generation with digital programming.

Two methods of digitally generating and programming the V-I characteristic were considered. Both utilize a digital computer to generate a reference voltage or current signal in response to samples of the output current or voltage. This reference signal in turn controls a series regulator which adjusts the output according to the desired V-I characteristic. The voltage regulating scheme is shown in Figure 5.3-1 and the current regulating scheme in Figure 5.3-2.

Consider the voltage regulating scheme. In the first case the computer is utilized to perform an on-line calculation of the required load voltage in response to an input load current by the following relationship:

$$V_L = \frac{n_s KT}{q} \ln\left[\frac{K_1 n_p I_R - I_L}{n_p I_o} + 1\right]$$

where

V_L = load (output) voltage

I_L = load (output) current

K = Boltzman's constant

q = electron charge

T = absolute temperature in ^{o}K (programmed)

n_s = the number of cells in series

n_p = the number of cells in parallel

I_R = the short circuit current of a single cell at the reference illumination and temperature

I_o = the reverse saturation current of a single cell at the reference illumination and temperature

K_1 = a variable constant to account for variations in illumination due to sun angle and spinning (programmed).

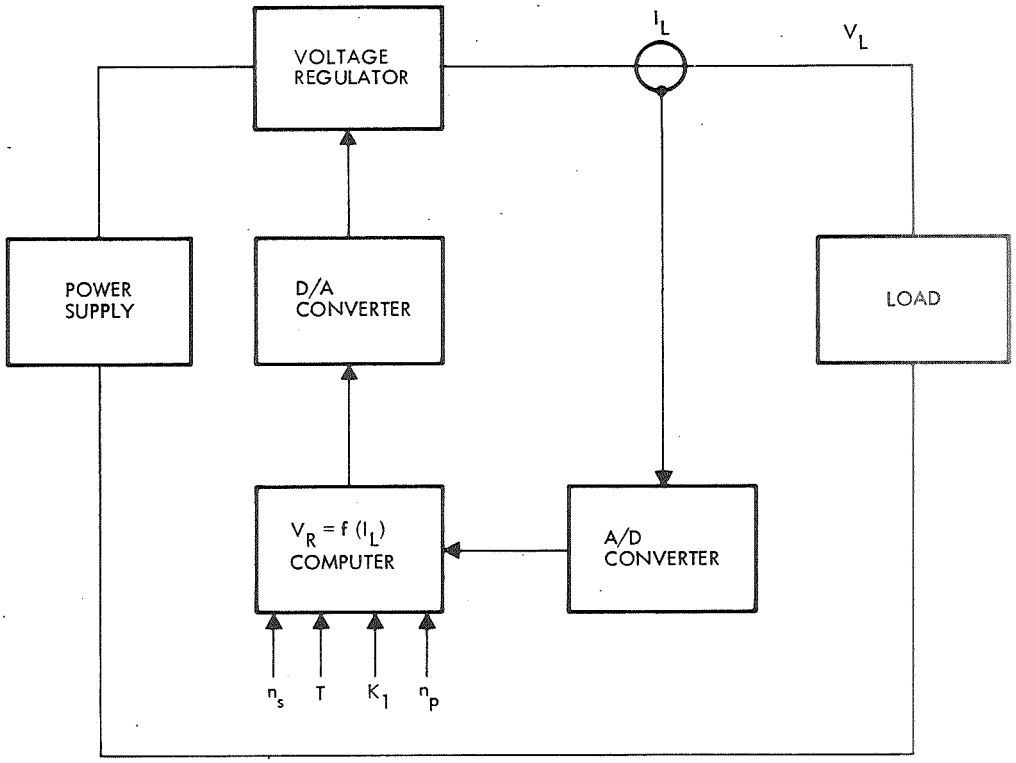

Figure 5.3-1. Digital System Using a Voltage Series Regulator

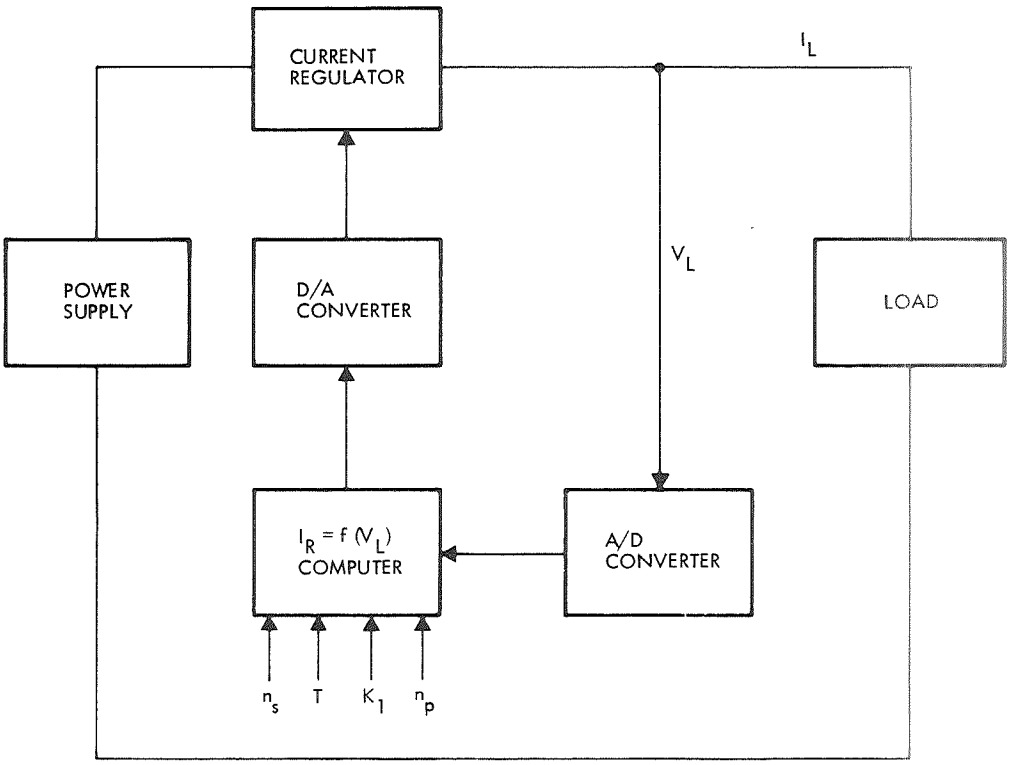

Figure 5.3-2. Digital System Using a Current Series Regulator

For a given simulation the fixed variables are entered directly into the computer and subroutines are programmed to generate K_1 and T as a function of time. For a fixed load the output voltage would vary as the variables K_1 and T vary. Even though temperature may vary rather rapidly upon exit from eclipse and K_1 could be varying at a maximum of a 2 Hz rate in a spinning satellite, these variations are slow compared to the computer calculation time. However in order to be compatible with the frequency response characteristics previously identified, the simulator must be capable of responding at least at a 14 kHz rate, that is, for a step change in load, the simulator should be at its new operating point in Υ_R seconds where

$$\Upsilon_R \approx 0.35/f_H$$

Therefore if

$$f_H = 14 \text{ kHz}$$

$$\Upsilon_R = 25 \text{ } \mu\text{sec}$$

Conversations with various computer manufacturers indicated that computation of the required function in about this length of time would be possible. Note, however, that several iterations would be required before the system could settle down at a new operating point. This, in addition to A/D and D/A conversion times, would be in excess of the desired response time.

In order to shorten this time, a second scheme was conceived that would considerably shorten the time. Under this method a series of tables of V_L vs I_L would be stored in the computer memory corresponding to the V-I characteristics as a function of time. At any discrete time a single table would be stored in the computer's core memory corresponding to the V-I characteristic for that interval of time. As I_L changed, the corresponding V_L could be outputted in one cycle time, so that now the time limitation falls only onto the A/D converter which depending on word length would be of the order of 30 microseconds.

In the current regulating scheme the computer is used to calculate

$$I_L = n_p\left[K_1 I_R - I_o\left(e^{V_L/n_s V_t} - 1\right)\right]$$

where all parameters are as before and

$$V_t = KT/q$$

the required load current in response to an input load voltage.

Both of these schemes, then, seem to be marginal from a response point of view. However, another disadvantage lies in their inability to simulate the variable impedance of the solar array. Note that while a shift in operating point will result in an effective change in the dc impedance, a capacitance would have to be added to reflect the roll-off characteristics of the array impedance. Furthermore, if the bandwidth is to remain constant for a range of operating points the capacitance must change by the same percent as the effective resistance but in the opposite direction. Adjustment of this capacitance would be difficult to do digitally in any other than a crude manner.

Their most serious disadvantage is their inherent limit cycling. This problem can best be described by looking at the response of this simulator to load changes. This is graphically displayed in Figure 5.3-3. Consider large load changes, those that would shift the operating point from the constant current region to the constant voltage region, or vice-versa. For large load changes, only decreases in load resistance (load current increases) can be accommodated when the series regulator controlled by the computer is a current regulator. Assume R1 is initially the load and the operating point is at "a." If the load resistance is suddenly decreased to R2 the sequence of events is as follows: The output voltage drops to "b"; the computer senses this voltage and calculates the current at "c"; this current and R2 cause the output voltage at "d"; for this voltage the computer calculates the current "e"; this current and R2 cause the output voltage at "f"; for this voltage the computer calculates the current "g"; this current and R2 give the voltage at "h"; the computer calculates the current "i"; this sequence continues until the operating point settles at "l." However, for load resistance increases (load current decreases) the system runs into a problem. Assume R2 is initially the load and the operating point is at "l." If the load resistance is suddenly increased to R1, the current "l" will cause the series regulator to saturate and the output voltage will increase up to the power supply voltage V_{ps}. The computer will sense this voltage at "m" and calculate that the output current should be zero. Now zero current will cause the output voltage to drop to zero and the computer next calculates, for zero volts, the output current I_{sc}. This current and R1 cause the system to saturate again. This condition of alternating between saturation and cutoff is referred to as limit cycling in this report.

For a computer controlled voltage regulator, the converse would be true. In other words, the system would limit cycle for large decreases in load resistance.

On the other hand, for small changes in load resistance, a computer-controlled current regulator would function adequately in the constant current region of the I-V curve. However, beyond the knee in the constant voltage region this system limit cycles. The converse is true for the computer controlled voltage regulator.

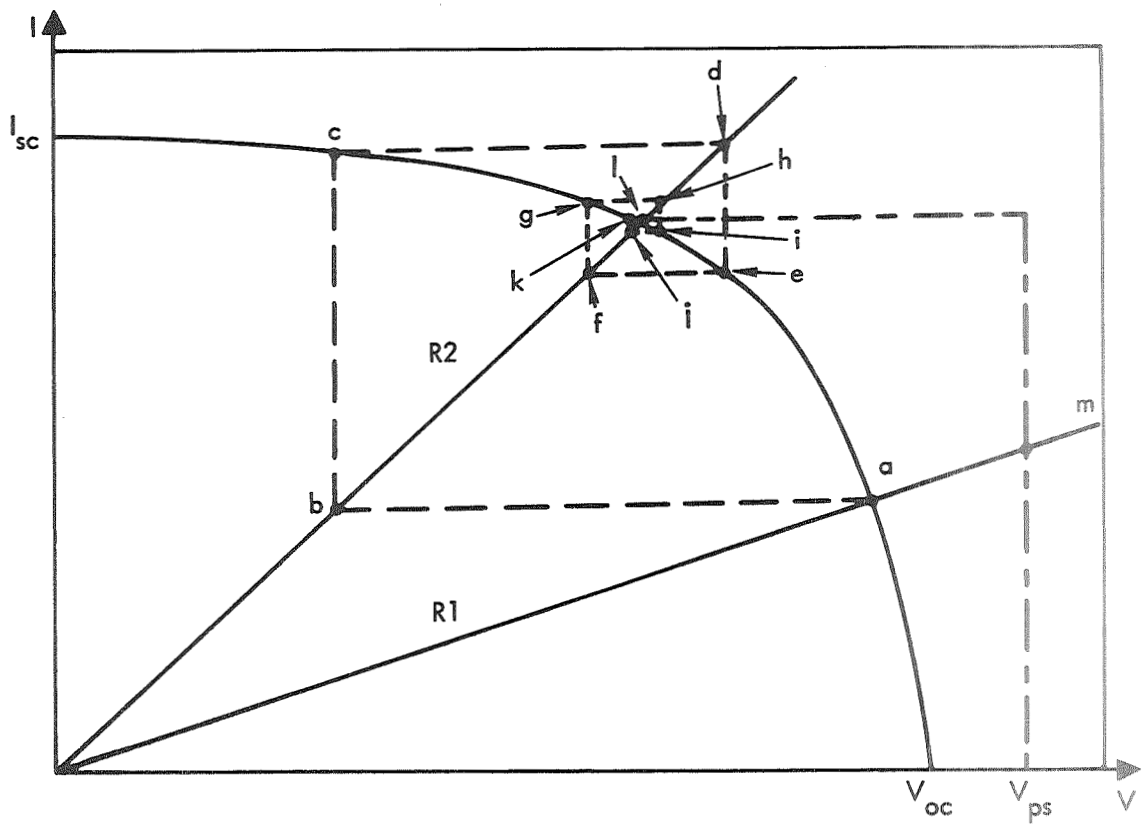

Figure 5.3-3. Graphical Representation Exposing Inherent Limit Cycling of Computer Controlled Regulator

Solution to these two major problems of the digital computer-controlled series regulator was not pursued.

The block diagram for the analog curve generation method is shown in Figure 5.3-4. This method utilizes the characteristics of the solar cell equivalent circuit to generate the basic dc curve shape as well as to provide the ac response as discussed in Section 5.1. Considering the block diagram we may write:

$$K_1 I_R - I_L/n_p = I_D$$

$$V_D - \frac{V_L}{n_s} = E$$

Then

$$I_L = n_p\left[K_1 I_R - I_D\right]$$

$$= n_p\left[K_1 I_R - I_o\left(e^{V_L/n_s V_t} - 1\right)\right]$$

where $I_R \equiv I_s$ = Short circuit current of the reference cell at the reference illumination and temperature

and all other variables have the same meaning as before. Solving for V_L:

$$V_L = n_s V_t \times \ln\left[\frac{K_1 n_p I_R - I_L}{n_p I_o} + 1\right]$$

This is identical to the basic function generated in the digital method. To simplify programming of V_{oc} and I_{sc} the I_L and V_L relationships are first reduced. When $I_L = I_{sc}$, $V_L = 0$. Therefore,

$$I_L = I_{sc} = n_p K_1 I_R$$

$K_1 I_R$ is a reference current coming from a programmable constant current supply. When $V_L = V_{oc}$, $V_L = 0$. Therefore,

$$V_{oc} = n_s V_t \ln (1 + K_1 I_R / I_o)$$

The symbol V_t stands for the volt equivalent of temperature and is defined as

$$V_t = KT/q = T/11,600 \text{ volts}$$

At room temperature ($T_R = 300^oK$), $V_t = V_R = 26$ mV.

While it is true I_o is also a function of temperature, its effect on V_{oc} is negligible compared to V_t.

Programming of V_{oc} in this system is accomplished by varying the resistor ratio of the feedback divider. It is not economically feasible to utilize the cumbersome scheme of thermo-electrically controlling the temperature of the reference cell. Nonetheless, temperature effects are incorporated by defining new parameters such that

$$n_s V_t = N_s V_R$$

where

$$N_s = n_s T/T_R$$

$$V_R = KT_R/q = \text{the volt-equivalent at the reference temperature}$$

N_s may be interpreted as the number of series cells in the array as modified by the temperature variation. Also, n_p may be interpreted as the number of parallel cells which will be modified by the illumination variation K_1.

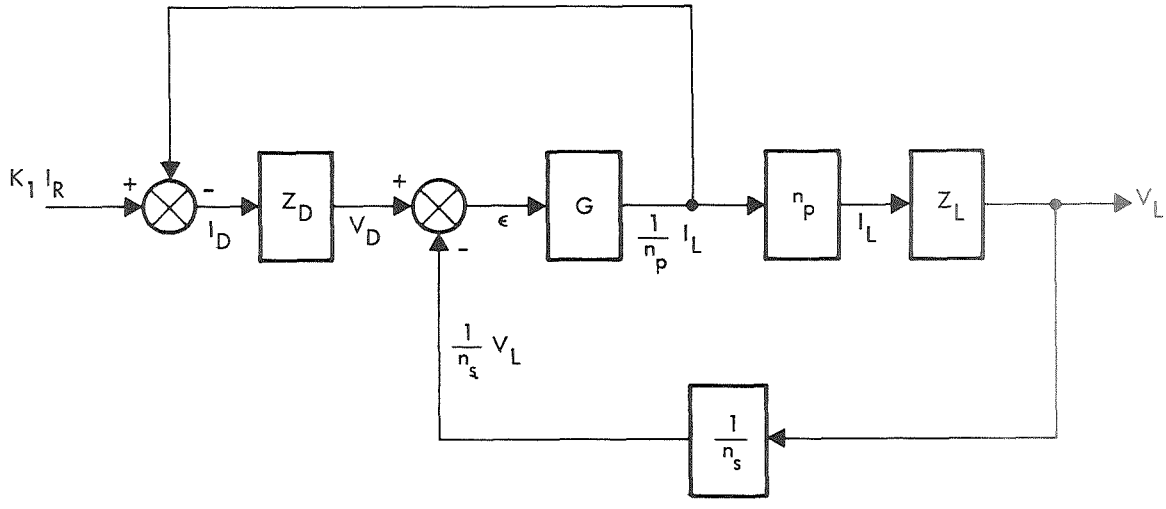

Figure 5.3-4. Analog System (Before)

The final form of the analog block diagram is shown in Figure 5.3-5.

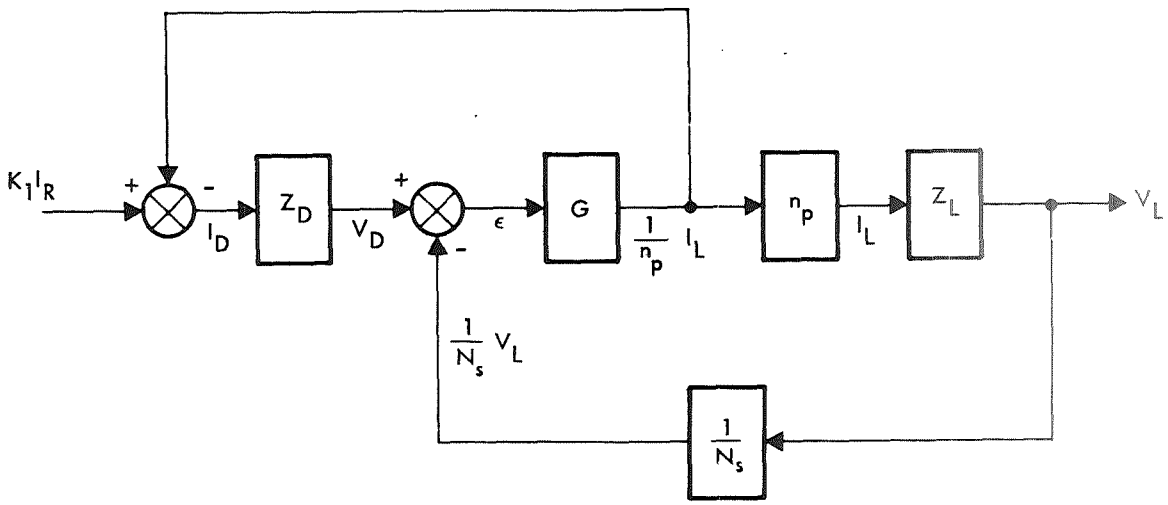

Figure 5.3-5. Analog System (After)

The governing equations incorporating the new parameters are as follows:

$$V_L = N_s V_R \ln\left[\frac{I_1 n_p I_R - I_L}{n_p I_o} + 1\right]$$

$$I_L = n_p\left[K_1 I_R - I_o\left(e^{V_L/N_s V_R} - 1\right)\right]$$

$$V_{OC} = N_s V_R \ln(1 + K_1 I_R / I_o)$$

$$I_{SC} = n_p K_1 I_R$$

Variation of N_s and n_p from array to array can be handled as an initial programmer setting of N_s and power stage setting of n_p, whereas variation from reference conditions for a given array as a function of time is handled by programming incremental variations of N_s and $K_1 I_R$ about their initial values. In order to accomplish this with a true analog or linear element would require some relatively complex electrochemical, electro-optical, or thermal electric scheme, and therefore analog programming has definite disadvantages.

Based on the above considerations, it appears that an analog generation/digital programming scheme offers the greatest advantages; i.e.

1) True analog generation of the V-I characteristic.

2) True analog simulation of the array impedance through multiplication of the ac response of the forward biased diode analog.

3) Ease of programming inherent to digital systems.

5.4 SOLAR CELL FREQUENCY RESPONSE

The purpose of this section is to discuss measurement data taken on a silicon, n on p, 10 ohm-cm, 3.8 cm^2 solar cell, to correlate the data with semiconductor p-n junction theory as discussed by Schockley and Pritchard, and to determine the impedance that will be exhibited by a 20 kW array.

In order to utilize the electrical parameters of a device in circuit design it is necessary to incorporate them into a model comprised of elements with which the designer is familiar.

A search of literature written to date revealed a small signal equivalent circuit quite appropriate for describing the impedance of a diode. This is shown in Figure 5.4-1. Since a solar cell is a large area diode the circuit shown can be used to represent its impedance where:

C_D = diffusion capacitance

C_T = transition capacitance

R_p, R_n = ohmic resistances of the P and N regime respectively

R_{SL} = resistance due to surface leakage around the junction

r_D = dynamic junction resistance

It will be assumed that

$$(R_p + R_n) \ll r_d$$

$$R_{SL} \gg r_D$$

so that the "equivalent circuit" can be simplified to that shown in Figure 5.4-2. The variations of r_D, C_D, and C_T as a function of voltage, current, and frequency are developed in the following paragraphs (Ref. 1).

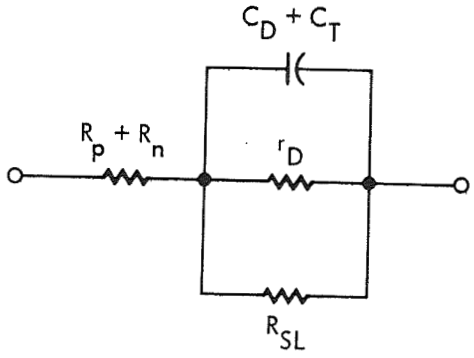

Figure 5.4-1. Small Signal "Equivalent Circuit" of a Forward Biased Nonilluminated Solar Cell

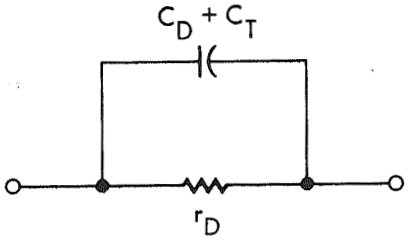

Figure 5.4-2. Simplified Equivalent Circuit For Cell

The forward biased p-n junction current-voltage relationships developed by Shockley are given as:

$$I_{dc} = I_{dc}(\text{holes}) + I_{dc}(\text{electrons}) = (I_{ps} + I_{ns})(e^{q v_o/KT} - 1) \quad (1)$$

$$I_{ps} = q p_n D_p / L_p \quad (2)$$

$$I_{ns} = q n_p D_n / L_n \quad (3)$$

$$I_{ac} = I_{ac}(\text{holes}) + I_{ac}(\text{electrons}) = \Big[(q p_n \mu_p / L_p) \left(e^{q v_o/KT}\right) \times \left(1 + j\omega\tau_p\right)^{1/2} + (q n_p \mu_n / L_n) \left(e^{q v_o/KT}\right) \times \left(1 + j\omega\tau_n\right)^{1/2} + j\omega C_T \Big] v_1 \quad (4)$$

where:

v_o = dc voltage applied to the junction

v_1 = ac voltage applied to the junction

q = electron or hole charge = 1.6×10^{-19} Coulombs

k = Boltzman constant = 1.38×10^{-23} joules/^oC

T = absolute temperature (^oK)

p_n = hole concentration in the n-region

n_p = electron concentration in the p-region

μ_p = mobility factor for holes

μ_n = mobility factor for electrons

$D_p = u_p KT/q$ = diffusion constant of holes

$D_n = u_n KT/q$ = diffusion constant of electrons

Υ_p = average lifetime of a hole in the n-region

Υ_n = average lifetime of an electron in the p-region

$L_p = \sqrt{D_p \Upsilon_p}$ = diffusion length of holes into the n-region

$L_n = \sqrt{D_n \Upsilon_n}$ = diffusion length of electrons into the p-region

The current of an n on p solar cell is primarily due to electron flow, therefore:

$$I_{dc} = I_{dc}(\text{electrons}) = I_{ns}\left(e^{q v_o/KT} - 1\right) \tag{5}$$

$$I_{ac} = \left[\left(qn_p \mu_n / L_w\right)\left(e^{qv_o/KT}\right)\left(1 + j\omega\Upsilon_n\right)^{1/2} + j\omega C_T\right] v_1$$

$$= \left[G_{n_o} e^{qv_o/KT}\left(1 + j\omega\Upsilon_n\right)^{1/2} + j\omega C_T\right] v_1$$

$$= \left(G_n + jS_n + j\omega C_T\right) v_1 = \left(A_n + j\omega C_T\right) v_1 \tag{6}$$

where:

A_n is the admittance/unit area due to electrons into the p-region.

G_n = real part of A_n

S_n = imaginary part of A_n

$$G_{no} = qn_p\mu_n/L_n \tag{7}$$

The ac admittance of a forward biased n on p solar cell can now be expressed as (Eq 6):

$$A_n = G_n + jS_n + j\omega C_T$$
$$= G_{n_o}(1 + j\omega\Upsilon_n)^{1/2} e^{qv_o/KT} + j\omega C_T \tag{8}$$

For low frequencies such that $\omega \ll 1/\Upsilon_n$, $G_n + jS_n$ can be expanded as follows:

$$Gn + jSn = G_{n_o} e^{q\,v_o/KT} + \frac{j\omega\Upsilon_n}{2} G_{n_o} e^{q\,v_o/KT} \tag{9}$$

In relation to the equivalent circuit:

$$r_D = \frac{1}{G_{n_o} e^{q\,v_o/KT}} \tag{10}$$

$$C_D = \frac{\Upsilon_n G_{n_o} e^{q\,v_o/KT}}{2} \tag{11}$$

Although $G_n + jS_n$ simulates a conductance and capacitance at low frequencies, its high frequency behavior is quite different. The behavior of $(1 + j\omega\Upsilon_n)^{1/2}$ is shown in Figures 5.4-3 and 5.4-4 for Υ_n = 1 μsec and 10 μsec (minimum and maximum values of a useful solar cell). For large ω, S_n varies as $\omega^{1/2}$ whereas S_T is ωC_T. Hence, the junction capacitance varies from its low frequency value of $(C_D + C_T)$ to an ultimate high frequency value of C_T. (Ref. 2)

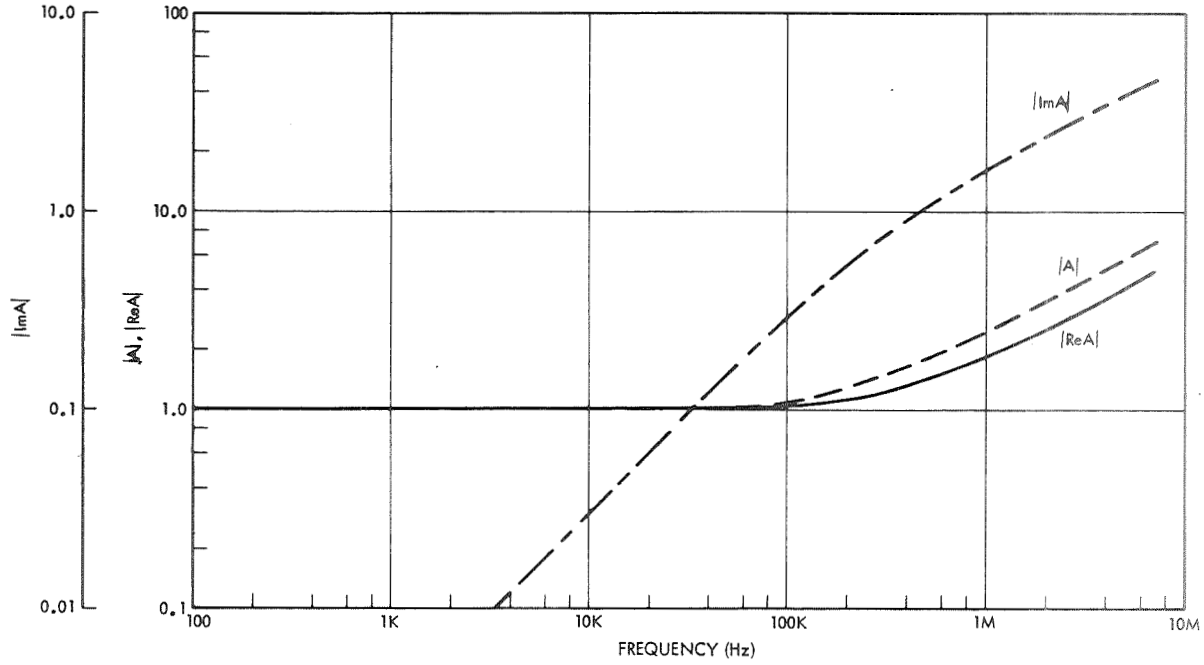

Figure 5.4-3. Plot of $A = (1 + j\omega\tau_n)^{1/2}$ Versus Frequency With $\tau_n = 1$ μsec

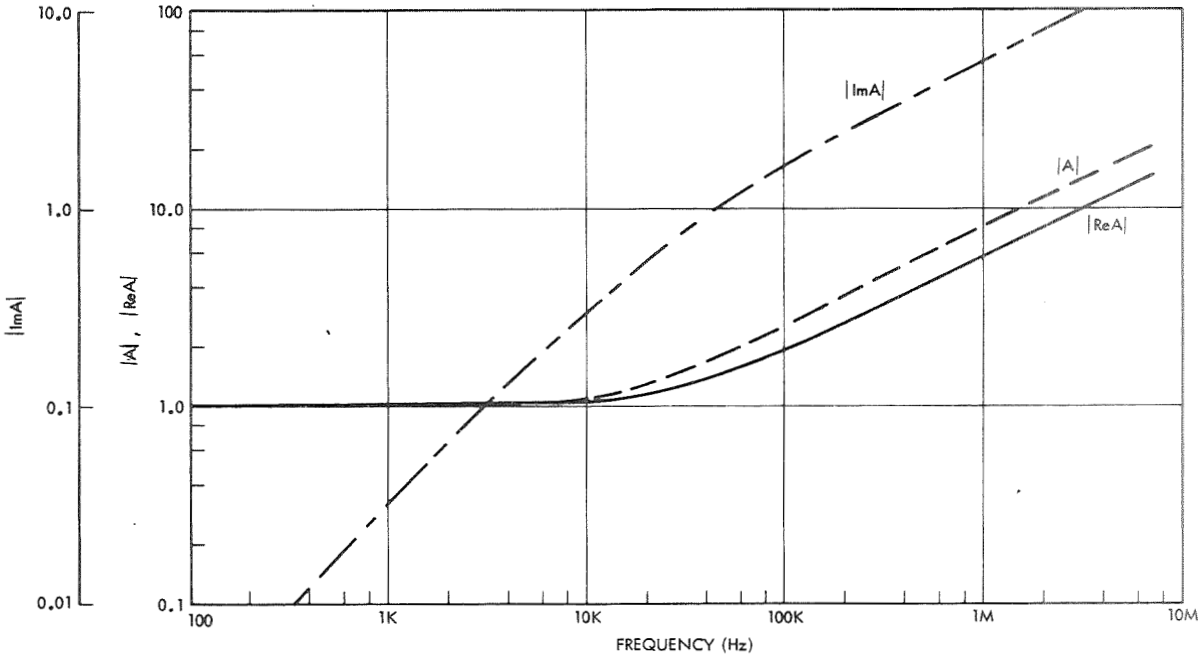

Figure 5.4-4. Plot of $A = (1 + j\omega\tau_n)^{1/2}$ with $\tau_n = 10$ μsec

The transition capacitance is proportional to the inverse square root of the dc voltage across the diode or:

$$C_T = K \Big/ \sqrt{V_R} \tag{12}$$

where: K is a constant for a given cell; V_R is the total dc voltage across the diode (including both thermal and external bias effects).

$$Z = \frac{V}{I} \tag{13}$$

$$r_D = \frac{Z}{\cos\phi} \tag{14}$$

$$C_p = \frac{\sin\phi}{2\pi f Z} \tag{15}$$

The cell was initially subjected to constant illuminations of 140 mW/cm and 70 mW/cm. The resulting V-I curves are shown in Figure 5.4-5. The forward bias dc characteristics are shown in Figure 5.4-6. Plots of Z, r_D, C_p, and ϕ vs frequency are shown in Figure 5.4-7 through 5.4-10, respectively.

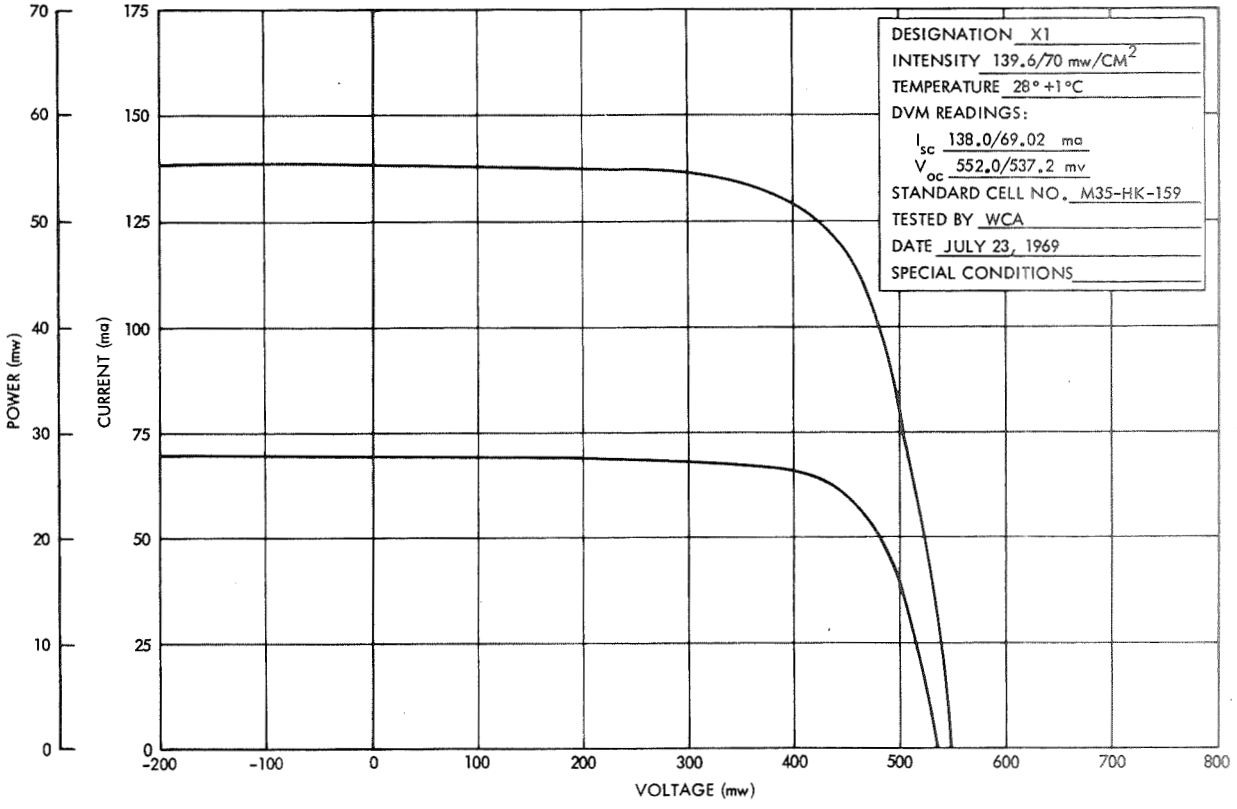

Figure 5.4-5. Photovoltaic Characteristics of 2 x 2 CM Solar Cells

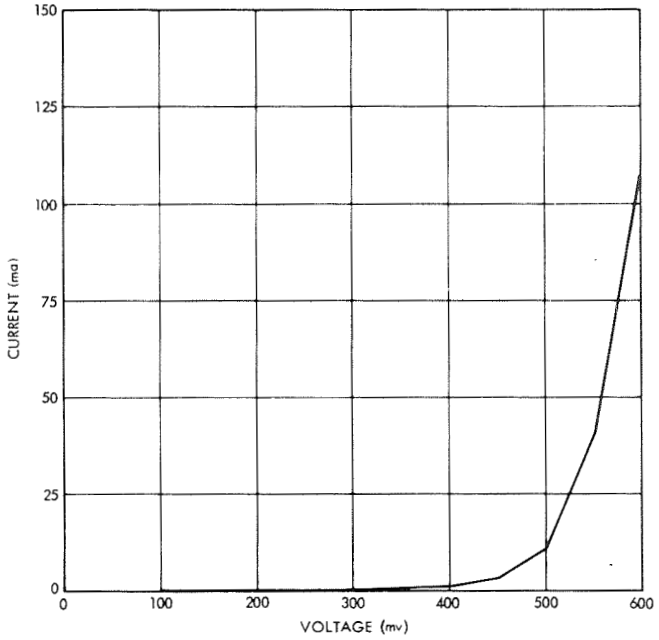

Figure 5.4-6. Solar Cell X1 dc Forward Bias Characteristics

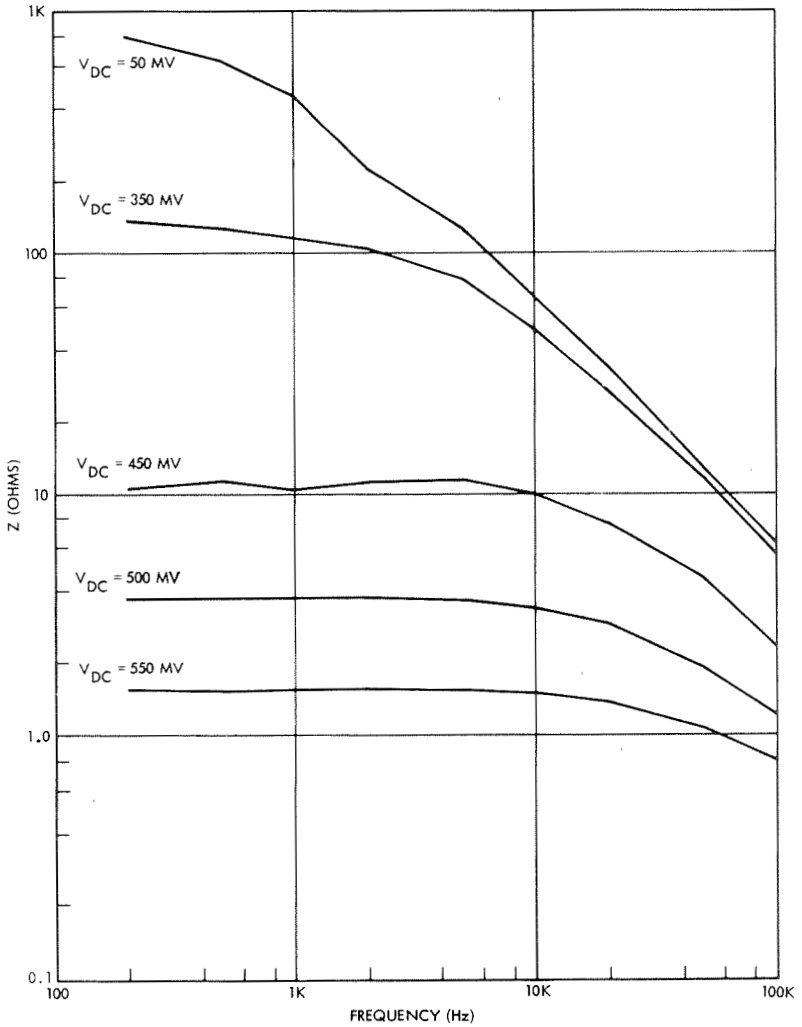

Figure 5.4-7. Forward Biased Solar Cell Ampedance Versus Frequency

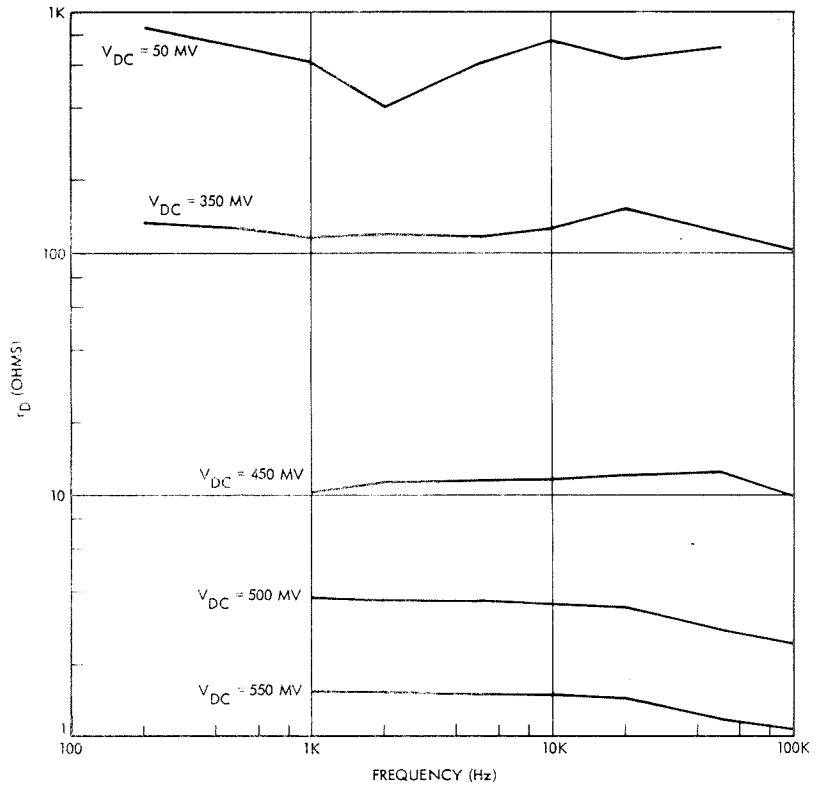

Figure 5.4-8. Forward Biased Solar Cell r_D Versus Frequency

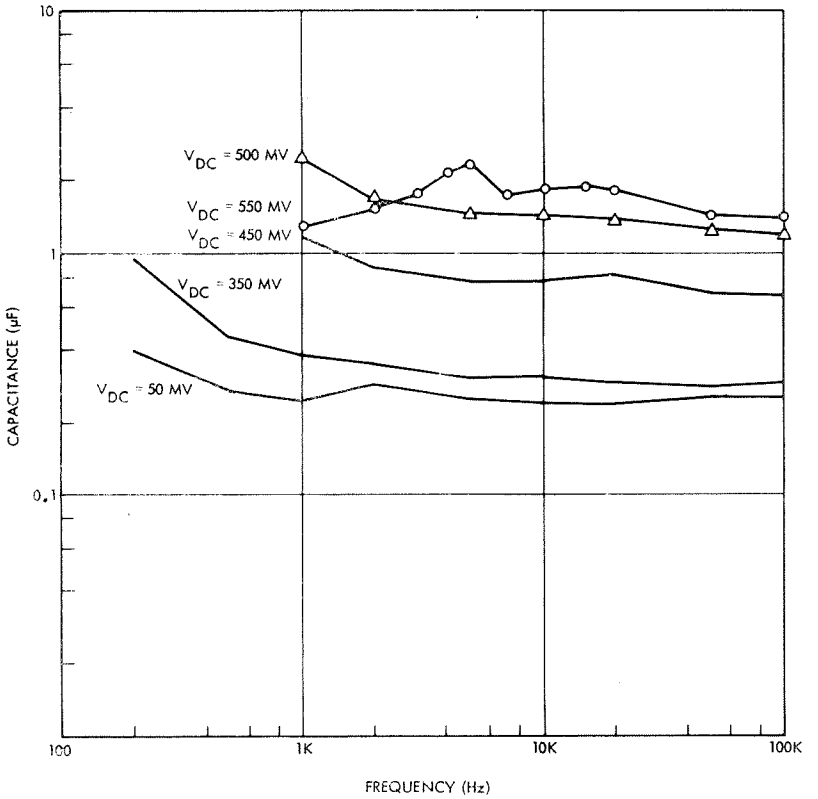

Figure 5.4-9. Forward Biased Solar Cell Capacitance Versus Frequency

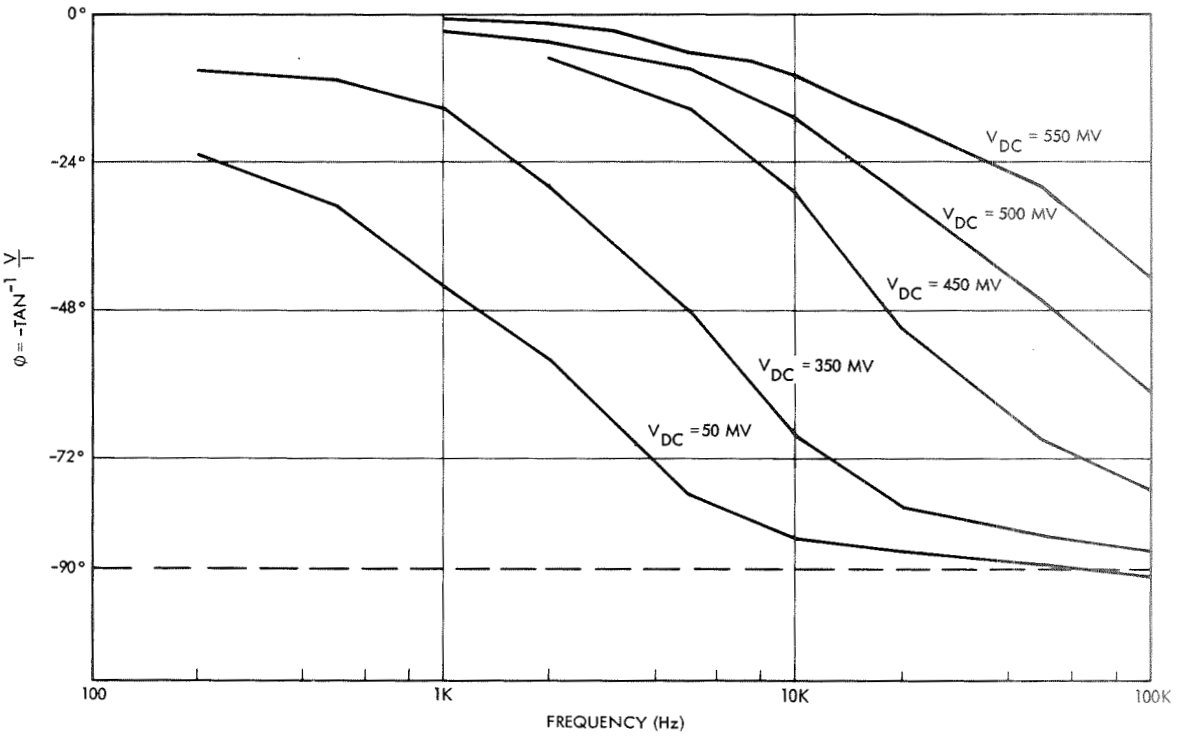

Figure 5.4-10. Forward Biased Solar Cell Phase Angle Versus Frequency

To get a comparison between theory and test we may express diffusion capacitance as:

$$C_D = \frac{\Upsilon_n G_{n_o} e^{q v_o/KT}}{2} = \Upsilon_n \frac{q n_p \mu_n}{2L_n} e^{q v_o/KT} \qquad (16)$$

since

$$I_{dc} \simeq I_{ns} e^{q v_o/KT} \text{ and } I_{ns} = KT n_p \mu_n / L_n$$

then

$$C_D = \frac{q\Upsilon_n}{2KT} I_{dc} \qquad (17)$$

where

$$\frac{KT}{q} = 0.025V \text{ at room temperature.}$$

Using this relationship to calculate diffusion capacitance:

Let

$$I_{dc} = 40 \text{ mA}(V_{dc} = 550 \text{ mV}), \quad \Upsilon_n = 1 \text{ } \mu\text{s}.$$

$$C_D = (20)(10^{-6})(40 \text{ mA}) = 0.8 \text{ } \mu\text{F}.$$

Let

$$I_{dc} = 40 \text{ mA}, \quad \Upsilon_n = 10 \text{ } \mu\text{s}$$

$$C_D = (20)(10^{-5})(40 \text{ mA}) = 8 \text{ } \mu\text{F}.$$

Let

$$I_{dc} = 0.3 \text{ mA } (V_{dc} = 350 \text{ mV}), \quad \Upsilon_n = 1 \text{ } \mu\text{s}.$$

$$C_D = (20)(10^{-6})(0.3 \text{ mA}) = 0.006 \text{ } \mu\text{F}.$$

The characteristics of C_T vs V are shown in Figure 5.4-11. Theoretically C_T becomes infinitely large as the bias approaches zero. However, in practice the value reaches a maximum as shown.

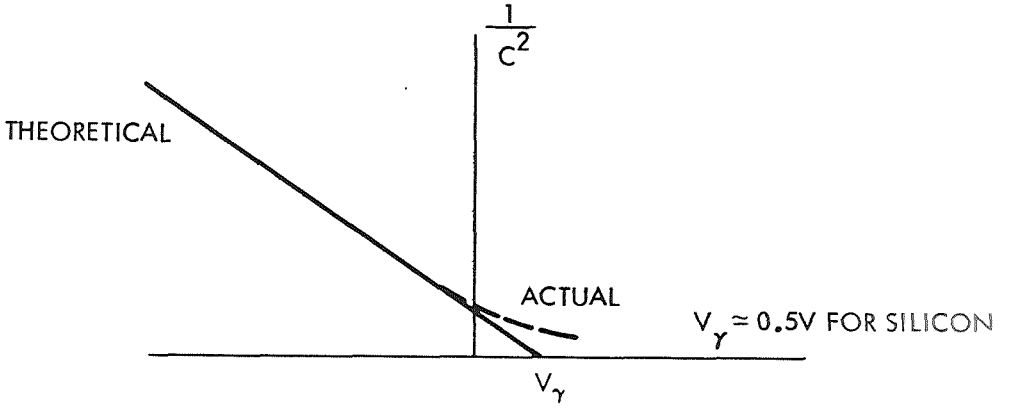

Figure 5.4-11. Variation of Transition Capacitance as a Function of Diode Voltage

Laboratory tests were performed to measure the impedance of a cell. A silicon n on p, 10 ohm-cm, 3.8 cm^2, solar cell was subjected to voltage, current, and phase measurements at selected frequencies and DC operating points. The cell was operated as a forward biased diode (nonilluminated). The test circuit is shown in Figure 5.4-12. The forward bias was applied to the cell by adjusting the power supply. An ac signal was injected with the oscillator and transformer. The cell impedance Z, dynamic resistance r_D, and parallel capacitance C_p were determined by the following relationships:

Let

$$I_{dc} = 0.3 \text{ mA}, \quad \Upsilon_n = 10 \ \mu\text{s}.$$

$$(20)(10^{-5})(0.3 \text{ mA}) = 0.06 \ \mu\text{F}.$$

The test data shows:

$$C_D \ (I_{DC} = 40 \text{ mA}) \simeq 1.7 \ \mu\text{F}.$$

$$C_D \ (I_{DC} = 0.3 \text{ mA}) \simeq 0.3 \ \mu\text{F}.$$

The transition capacitance could then be estimated as:

$$C_T \simeq 0.25 \ \mu\text{f}.$$

Vendor indicates $C_T \simeq 0.05 \ \mu$F at zero bias. Qualitatively speaking, C_D "dominates" the capacitance term at large forward dc currents, and C_T "dominates" the capacitance term at small forward dc currents.

An interesting fact pertaining to the impedance vs frequence plot is that:

$$\omega_{3dB} = \frac{1}{r_D(C_D + C_T)} \tag{18}$$

If $C_D \gg C_T$

$$\omega_{3db} = \frac{1}{r_D C_D} = \frac{G_{n_o} e^{q \ v_o/KT}}{\frac{\Upsilon_n}{2} G_{n_o} e^{q \ v_o/KT}} = \frac{2}{\Upsilon_n} \tag{19}$$

Also

$$Z = G_{n_o} e^{q v_o / KT} (1 + j\omega\tau_n)^{1/2}$$

Therefore ω_{3dB} is independent of forward bias under these conditions and a 3 dB rolloff could be expected.

If $$C_T >> C_D$$

Then $$\omega_{3dB} = \frac{1}{r_D C_T} \qquad (20)$$

and the impedance vs frequency plot would simulate an RC circuit, i.e. 6 dB rolloff.

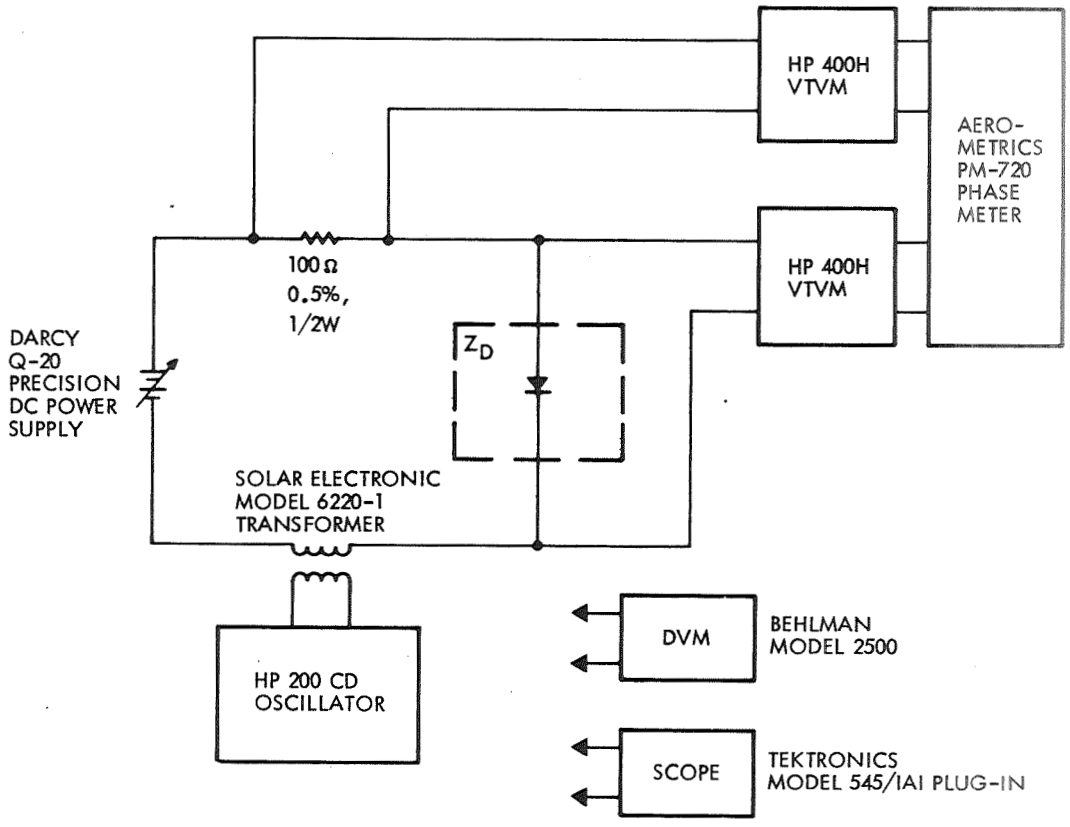

Figure 5.4-12. Solar Cell Test Circuit

The data (Figure 5.4-7) shows a varying ω_{3dB} with varying dc voltage. Also a 6 dB rolloff is indicated at small currents. This data supports the fact that C_T must be taken into account. The frequency limitations of the test circuit did not allow sufficient data points in the region where C_D dominates.

The test circuit was also limited in the region where small phase angles were measured. It is the opinion of the writer that irregularities in r_D and C_P measurements are due to this limitation.

In summary, the frequency characteristics of the solar cell have been shown to vary with current and frequency. The test data correlates with the p-n junction theory.

In spacecraft applications it is desirable to know what impedance the solar array will present to the power conditioning electronics because this impedance affects regulator stability. Since the cell studies have shown that forward-biased and illuminated cells exhibit the same impedance it is possible to measure the array impedance directly without having to illuminate it. Provisions would have to be made, though, to allow bypassing of panel isolating diodes that are normally included in large arrays. The array would need to be supplied from a constant current source having an impedance much larger than the expected array impedance throughout the frequency range and a current capability equal to I_{sc}.

However, the PCE designer wants to know the array ac response at the onset of a program, not after the array is built, when he can use this information to optimize his regulator design. Fortunately, now that cell response has been characterized, a designer can obtain a qualitative estimation for an overall array. Knowing the type of cell the array will contain a designer can measure the characteristics of this cell. He can then plot this data as shown in Figure 5.4-13, which shows the normalized impedance of a particular cell as a function of frequency. Knowing the number of series and parallel cells comprising the array, he can then generate the impedance plot for the array. Note that an array of equal number of series and parallel cells would give the same impedance as that of a single cell.

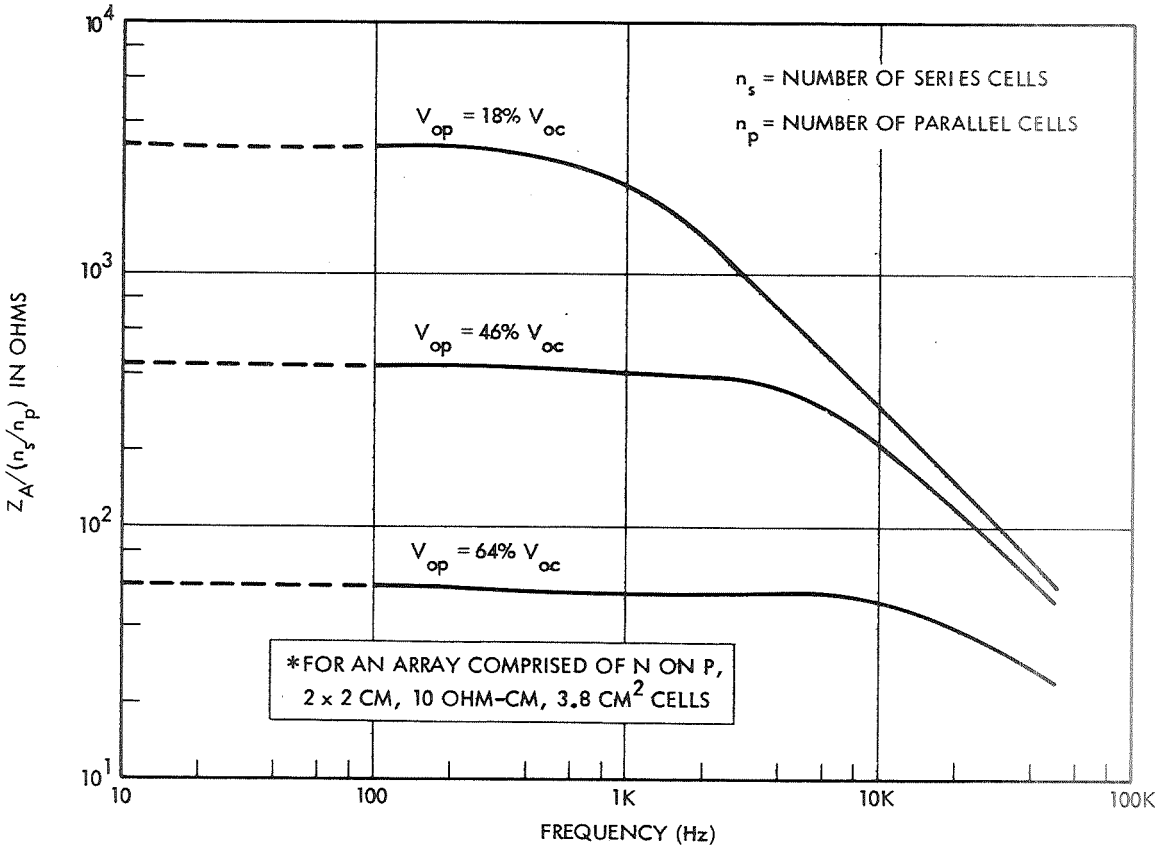

Figure 5.4-13. Normalized Solar Array Impedance* Versus Frequency T = 45°C

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5.2 R. L. Pritchard, "Frequency Variations of Junction Transistor Parameters," Proceedings of the IRE, May, 1954.

5.3 A. B. Phillips, Transistor Engineering, McGraw-Hill Book Company, New York, p. 148, 1962.

6. DESIGN CONCEPTS

Whenever an attempt is made to establish the basic technology in any field, design concepts must be introduced so that comparative discussions and qualitative evaluations can be made. The salient features of three concepts considered during the course of the program as possible candidates for a 20 kW solar array simulator are presented in this section.

6. 1 FRSAS MODULAR APPROACH

The fast response solar array (FRSAS) is a universal solar array simulator developed under NASA Contract NAS 5-11581 featuring an ac response which is identical to that of a real array over a large range of dc operating points. In addition, short circuit current (I_{sc}) and open circuit voltage (V_{oc}) are digitally programmable over a wide range for use not only in simulating a wide range of array sizes, but also to simulate I_{sc} and V_{oc} variations with illumination and temperature. A means for simulating current variations due to spinning is available. Provisions for remote control and monitoring, automatic failure sensing and warning, and a load simulator are also included.

Performance specifications of the basic FRSAS unit are as follows:

I_{sc}: Adjustable from 0. 1 to 20 amps. Programmable as a function of temperature, sun angle, and illumination.

I_{spin}: Up to ±20% programmable modulation of I from 0. 01 to 100 Hz to simulate a spinning array.

V_{oc}: Adjustable from 10 to 100 volts. Programmable as a function of temperature.

Power: Maximum power output of 750 watts. See locus of maximum power points in Figure 6. 1-1.

Input: 208 ± 10 volts 60 Hz, three phase.

Output: V_{oc} and I_{sc} accuracy—±1%

V_o and I_o stability— ±1%

I-V curve repeatability—±1%

Output can be floated.

Ripple: Less than 50 millivolts peak-to-peak.

Impedance: The output impedance is the impedance of a reference solar cell multiplied by the ratio of number of series cells to number of parallel cells of the array being simulated, within the limits given in Table 6. 1-1.

Curve Shape: The FRSAS exhibits a curve similar to that shown in Figure 6. 1-2. The axes are normalized.

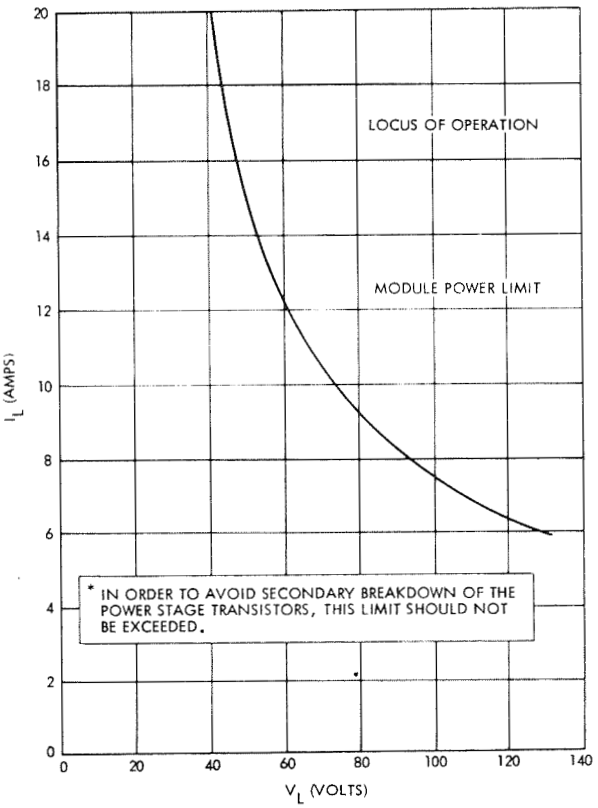


Figure 6. 1. 1. Output Power Limits of the FRSAS Basic Unit

Table 6.1-1.

V_L/V_{oc}	Frequency	Error Limits, db	$Z_{os}/(n_s/n_p)Z_c$
>0.6	dc to 200 kHz	+3	1.4
		-3	0.7
0.25 → 0.6	3 kHz to 200 kHz	0	1
		-12	0.25
	dc to 3 kHz	0	1
		-16	0.17
<0.25	3 kHz to 200 kHz	0	1
		-16	0.17
	dc to 3 kHz	-	0.17

where Z_{os} = output impedance of the simulator

Z_c = impedance of reference cell

Note: The FRSAS has a built-in load which can sweep the entire V-I characteristic at any intermediate time for purposes of checking. Design of this load includes the full specification range up to 3 kW. It is controlled manually and the output is available to external recording devices.

A recent report[1] gives a full description of the theory of operation, installation and operation, maintenance and calibration, ripple and transient performance, and expansion options, together with parts lists, assembly photographs, and drawings of the fast response solar array simulator.

The concept of combining power modules of the FRSAS type could be developed to meet the current, voltage, and power requirements of the 20 kW electronic solar array simulator (ESAS) (see Section 4.3). The basic FRSAS can deliver 750 watts and has space available for two additional power stage drawers, which can increase console capability

[1] R. Von Hatten, A. Weimer, and D. Zerbel, "Operating Manual/Final Report for the Fast Response Solar Array Simulator," Final Report on Goddard Space Flight Center Contract NAS5-11581, July 1970.

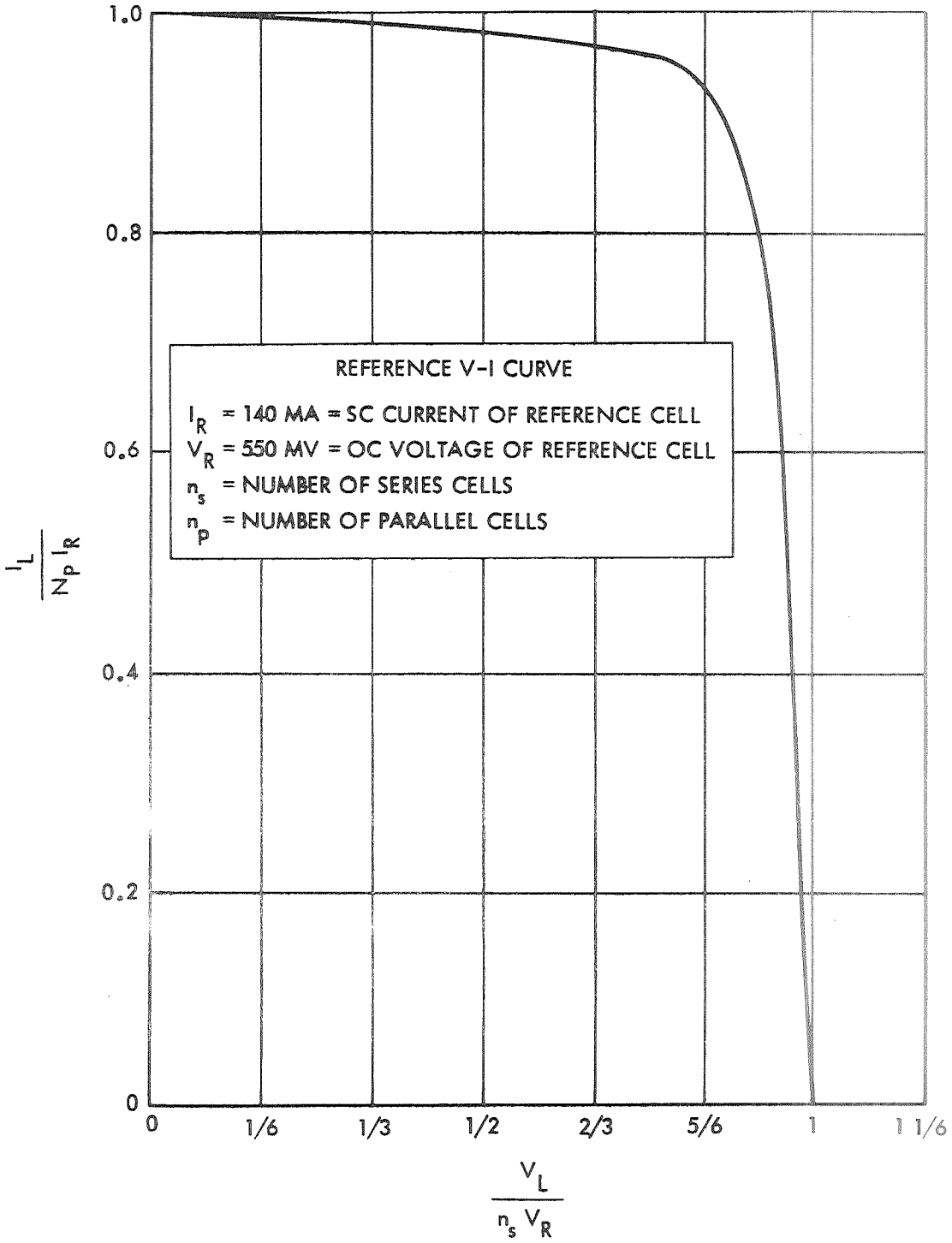


Figure 6.1-2. Normalized IV Curve for Determining the Output of the FRSAS

to 1500 watts. Furthermore, the addition of another double bay console containing power supplies, power stage drawers, a load simulator, and protection circuitry would increase single controller capability to 3000 watts. Even though the basic FRSAS can be expanded to 5 kW, the controller design was optimized at a lower power level. Expansion to 3 kW with a single controller is preferred for this application. The expanded basic unit would have a V_{oc} maximum of 100 volts and I_{sc} maximum of 40 amps (see Figure 6. 1-3).

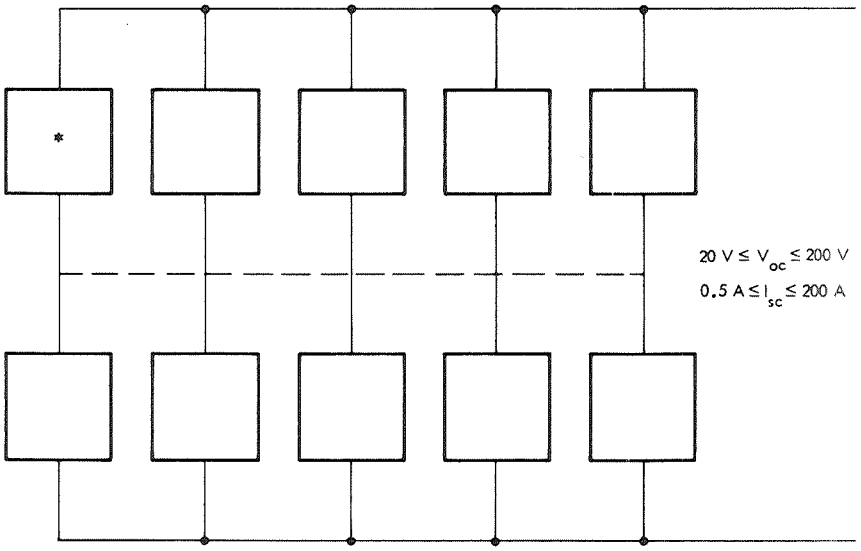


Figure 6. 1-3. 20 kW Electronic Solar Array Simulator Using FRSAS Modules

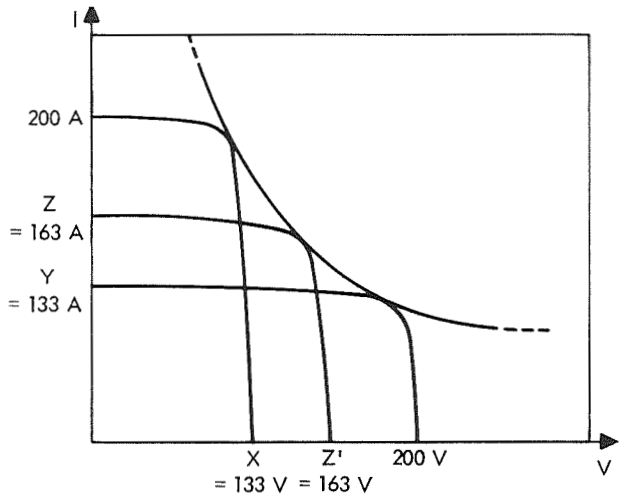
To achieve the current, voltage, and power of the ESAS requirements, two series banks of five parallel expanded (3 kW) basic units would be needed (see Table 6. 1-2, Case 4). However, a 30 kW system would result as a consequence of trying to meet all the requirements.

If the basic 750 watt unit were expanded to 2250 watts only, the series-parallel combination of 10 units could provide 22. 5 kW. This configuration can meet the power and voltage requirements, but not the current requirement, because five parallel units can provide only 150 amps (see Table 6. 1-2, Case 3).

Table 6.1-2. Single Controller Capability

Case	(P_o Watts)	V_{oc}(V)	I_{sc}(A)	No. Power Stages
1	750	100	10	2
2	1500	100	20	4
3	2250	100	30	6
4	3000	100	40	8
5	750	50	20	2
6	1500	50	40	4
7	2250	50	60	6

To obtain 20 kW of power from an array whose I_{sc} is 200A, the V_{oc} would have to be approximately 133V. See Figure 6.1-4. For an array with V_{oc} = 200V, the I_{sc} would only need to be 133A.



FOR 20 kW:

$$X \simeq \frac{P_M}{0.75\,(200)} = \frac{100}{0.75} = 133\ \text{V} = V_{OC\ MAX} \text{ WHEN } I_{SC} = 200$$

$$Y \simeq \frac{P_M}{0.75\,(200)} = 133\text{A} = I_{SC\ MAX} \text{ WHEN } V_{OC} = 200$$

$$Z \simeq \frac{P_M}{0.75\,Z'}$$

IF $Z = Z'$ $\quad Z^2 = \frac{P_M}{0.75} = 26{,}600$

THEN $Z = \sqrt{2.66 \times 10^4} = 163$ A

$Z' = 163$ V

Figure 6.1-4. Maximum Power Locus of the 20 kW Electronic Solar Array Simulator

6. 2 POWER SUPPLY APPROACH

This concept encompasses the brute force approach of series connected high current, high voltage power supplies. The use of SCR regulated supplies would allow a more compact configuration than the use of fully transistorized supplies. The configuration would look as in Figure 6. 2-1. The diodes prevent one supply from presenting a reverse bias to the other if the supplies are not on at the same time.

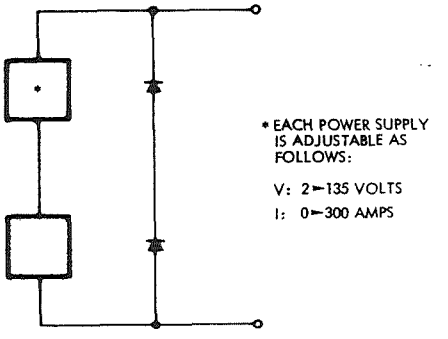


Figure 6. 2-1. 20 kW ESAS Using Constant Voltage/Current Limit Type Power Supplies

After a lengthy vendor survey on power supplies one manufacturer was found who advertises a unit that can simplify the task of parallel and series connecting of supplies to achieve 20 kW. This unit, made by the Christie Electric Corp., is model number 2C0135-300EBPX4-S. Two of these units in series would meet the ESAS power requirements. The standard features of the model are given in Section 6. 2. 1.

Most leading manufacturers advised against the use of more than three or four of their models in any stacked configuration. Some said that for these high power sources the use of SCR regulators or pre-regulators made input line interference very critical. In multi-unit configurations, having a common input line and common output load, some had experienced quite unpredictable performance. This was attributed to the switching transients of one supply affecting the firing angle of other supplies. Some even experience catastrophic failures. Others said that even though they had not attempted multi-unit configurations, this problem could be expected.

The search then centered on units with enough capability so that only two would be required. The only unit found was the Christie model 2C0135-300EBP-X45. Use of two such units will be assumed for the remainder of this discussion.

The use of the brute force power supply approach to simulate a solar array has certain advantages and disadvantages. The advantages include:

- Minimum equipment cost, size, and weight
- Ease of transportability
- Ease of remote programming because of fixed power stages
- Least number of controls allowing minimum set-up and check-out time
- Minimum maintenance.

The disadvantages include:

- Poor static and dynamic impedance simulation
- Poor "knee" simulation of an array's IV curve
- Poor peak-to-peak ripple
- Poor response time.

The static characteristics (slopes of the constant current and constant voltage regions) can be improved by the use of external resistors in series and in parallel with the output terminals of the entire system or of each supply. Choice of location would favor the former because the least number of components would be needed, and if adjustable slopes are required, the number of controls would be less.

The power supply solar array simulator "PSSAS" could look like the diagram in Figure 6.2-2. A programmer to process local or remote commands can be incorporated to control V_{oc}, I_{sc}, and the slope generators.

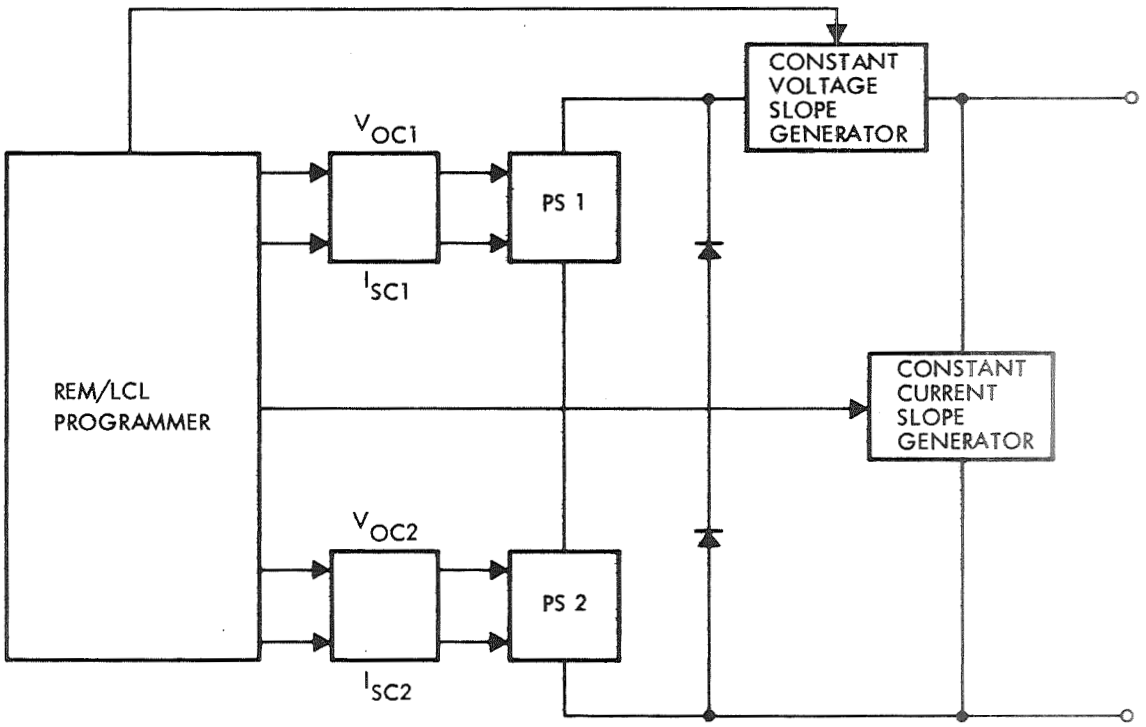


Figure 6.2-2. 20 kW Power Supply Solar Array Simulator "PSSAS" Including Slope Generators and Programmer

To determine the range of resistance required of the slope generators, consider the following:

I_{sc} max = 200 A $\qquad$ V_{oc} max = 200 V

I_{sc} min = 90 A $\qquad$ V_{oc} min = 90 V

The approximate number of series cells is:

$$N_s \text{ max} \simeq \frac{200 \text{ V}}{0.5 \text{ V}} = 400 \qquad N_s \text{ min} \simeq \frac{90 \text{ V}}{0.5 \text{V}} = 180$$

Wherease the approximate number of parallel cells is:

$$N_p \text{ max} \simeq \frac{200 \text{ A}}{0.14 \text{ A}} = 1430 \qquad N_p \text{ min} \simeq \frac{90 \text{ A}}{0.14 \text{ A}} = 642$$

The maximum series resistance required, assuming R_s (cell) $\approx 4\Omega$ at 90% V_{oc} (cell) is:

$$R_s \text{ max} = \frac{N_s \text{ max}}{N_p \text{ min}} \left[R_s(\text{cell})\right] = \frac{400}{642} (4) = 0.621 (4) = 0.621 (4) = 1.284\Omega$$

Where as the minimum is:

$$R_s \text{ min} = \frac{N_s \text{ min}}{N_p \text{ max}} (4\Omega) = \frac{180}{1430} (4\Omega) = 0.126 (4) = 0.504\Omega$$

The maximum parallel resistance required, assuming R_p (cell) $\simeq$ 2.2 K at 20% V_{oc} (cell), is:

$$R_p \text{ max} = \frac{N_s \text{ max}}{N_p \text{ min}} R_p \text{ (cell)} = \frac{400}{642} (2.2 \text{ K})$$

$$= 0.621 (2.2 \text{ K}) = 1.366 \text{ K} = 1366$$

Whereas the minimum is:

$$R_p \text{ min} = \frac{N_s \text{ min}}{N_p \text{ max}} (2.2 \text{ K}) = \frac{180}{1430} (2.2 \text{ K}) = 0.126 (2.2 \text{ K})$$

$$= 0.277 \text{ K} = 277\Omega$$

To select the proper slope, the approach used above can be followed after V_{oc} and I_{sc} are known.

If it is felt that making the maximum power point, i.e. knee, of the simulator's IV curve coincide with that of the array being simulated is more important, the generators will allow considerable range to do this. In Figure 6.2-3, the shaded area shows there are many combinations of V_{mp} and I_{mp} that can be obtained with the same V_{oc} and I_{sc}.

The parameters are related by the following expressions:

$$R_s = \frac{V_{oc} - V_{mp}}{I_{mp}}$$

$$R_p = \frac{V_{mp}}{I_{sc} - I_{mp}}$$

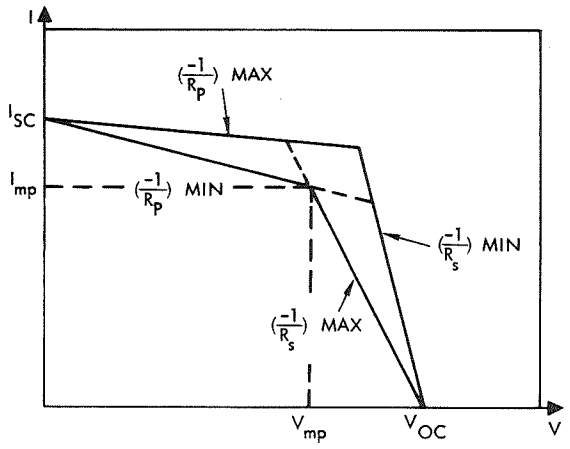


Figure 6. 2-3. Effect of Slope Generators on I-V Curve

The correct values of resistors can be calculated once V_{oc}, I_{sc}, I_{mp}, and V_{mp} are determined from the array characteristics.

6. 2. 1 Standard Features of Christie Model 2C0135-300EBPX4-S

DC voltage range	Continuous adjustment over the entire range by means of a 10-turn precision potentiometer.
Series or parallel operation	Units may be operated in series. They also may be operated in parallel, if the current limiting option under "optional extras" is included.
Remote sensing	Provision for selecting local sensing at the power supply terminals, or remote sensing at the load terminals. If remote sensing leads are opened, sensing will automatically revert to the power supply terminals.
Regulation and rectification	All solid state design including hermetically sealed SCR's. Peak voltages and currents during operation and switching held well within rated values.
Control circuit	Plug-in cards for easy servicing.
On-off controls	By ac magnetic contractor; 3 wire start-stop push-button switch on front panel. Also includes terminals for connecting remote start-stop switch.

Circuit isolation	Output circuit completely isolated from input; either positive or negative dc bus can be grounded.
Protection	Fan failure as well as thermal overload protection (automatic reset type) for sustained overloads.
Ambient temperature	Continuous operation from 0 to +50°C; storage at -62°C to +70°C.
Cooling	Fan cooling by means of induction motor with sealed ball bearings, silicone lubricated for low and high temperatures.
Stability	Negligible temperature influence; after short warmup, drift is less than 10 mv ± 0.005%/°C.
Pilot light	Indicates when unit is energized.
Meters	3-1/2 inch voltmeter and ammeter, 2% accuracy.
Multiple input	Can be set for various ac supply voltages by a simple reconnection.
Cabinet	Inside readily accessible from front or rear for inspection and servicing. Hinged front panel on stationary models.
Model No.[1]	2C0135-300EBPX4-S
DC volts output	
Nominal	120
Continuous range	2 to 135
DC amps continous	300
Output kW	40

[1] Insert suffixes for optional extras in alphabetical order just after suffix "E".

DC voltage regulation	
Static ± greater of[2]	0.1% or 100 mV
Dynamic ±[3]	10 V
Voltage ripple rms	100 mV
Response time millisec[4]	
NL-FL	50
FL-NL	125
Input ac volts ± 10% 3-phase 57 to 63 Hz	440/480
Approximate max amps/phase	
at 220 V	--
at 440 V	92
Approximate net weight, lb	775

6.3 DIODE MODULAR APPROACH

The concept is to incorporate a bank of diodes, a constant current power stage, and constant voltage power supplies. The configuation would appear as in Figure 6.3-1.

The simulator floats and point A or A' can be used as common ground for external loads. "E" can be a series-parallel combination of standard power supplies selected based on the considerations of Section 6.2.

"D" can be comprised of diode or solar cell modules of 10 V to 10 A capability (see Figure 6.3-2). The modules are plotted and would plug into matrix boards distributed in separate drawers. To meet ESAS voltage, current, and power requirements, 20 x 20 (or 400) modules of

---

[2] Deviation of the dc voltage from its average value for any combination of rated load and line variations.

[3] Maximum over or undershoot for step change from no-load to full load, or full load to no-load.

[4] For 63 percent reduction of transient in the range of 60 to 100 percent maximum rated output voltage.

NOTE: All values based on balanced supply lines.

approximately 20 x 70 (or 1400) diodes each are required. Depending on the diode or cell chosen, this scheme, being an open-loop system, affords the best technical compromise between the first and second approach and will not have the complexity of the first. In fact, if actual cells are used, the output impedance would be almost ideal except for the power stage "Q" in series with source E.

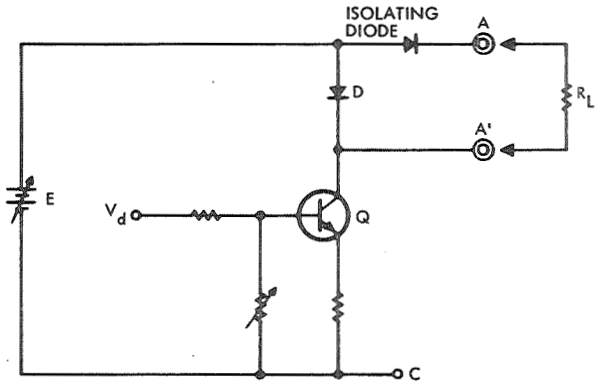


Figure 6. 3-1. Basic Circuit Configuration for a Forward Biased Diode Solar Array Simulator "DISAS"

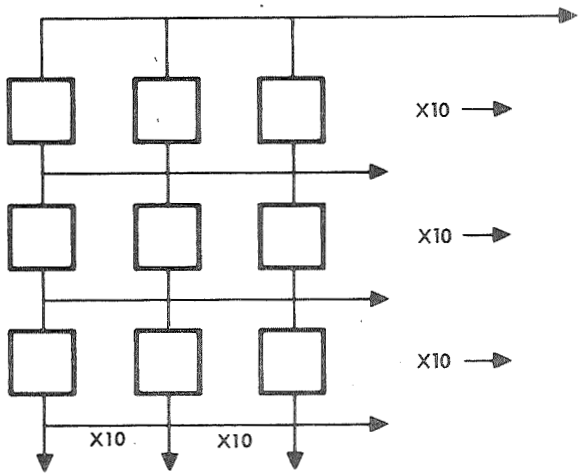


Figure 6. 3-2. Diode or Cell Modular Concept for Use in the Third Approach to a 20 kW Solar Array Simulator

The power stage can be a modified version of the FRSAS power stage, whereas two series-connected Christie Model 2C0135-300EBPX4-S E supplies can be the power supply as discussed in the second approach.

I_{sc} can be programmed about a nominal value without difficulty. This is done by varying the bias to the power stage Q. The adjustment on E is for setting the voltage drop across the power stages to be 10 volts or so above V_{oc}. If a V_{oc} of 90 volts and I_{sc} of 200 amps is to be simulated, it is unnecessary to dissipate, for example, (200 V x 200 A) 40,000 watts in the power stages when the simulator is open-circuited.

An alternative to that shown in Figure 6. 3-1 is to use the power supplies in their current limited mode. The configuration would look like Figure 6. 3-3. If the supplies exhibit relatively high output impedance, at least up to 50 kHz, this version is preferred. Note that no power stages and isolating diodes are needed. Provisions for automatic programming of the current limit would have to be worked out with the supply manufacturer.

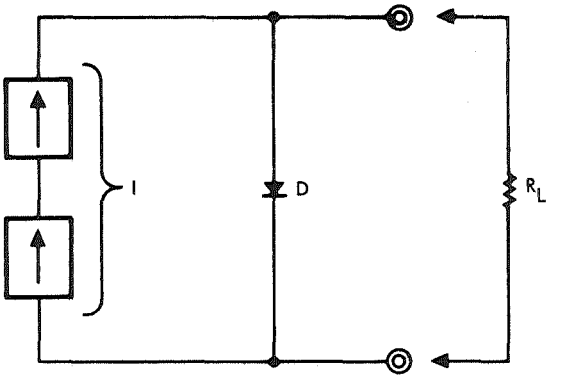


Figure 6. 3-3. Simplified DISAS Using Supplies in Current Limit Mode

To realize the advantages offered by this concept, a search must be made for the power cell or diode to use in the modules. A review of the data sheets of standard devices is not sufficient because the selection has to be based on matching semiconductor properties, junction area, and electrical characteristics. Parameters such as resistivity, minority carrier lifetime, and diffusion length are not found on data sheets. Some compromise may have to be made in the overall simulator characteristics. If not, the DISAS will exhibit impedance behavior similar to a solar array.

6.4 PROGRAMMING TECHNIQUES FOR TEMPERATURE, ILLUMINATION, AND RIPPLE

A desirable feature in a solar array simulator is provision for the operator to vary the nominal IV curve, as a function of time, to simulate effects of temperature, illumination, or spin ripple.

In the fast response solar array simulator basic unit this is accomplished as follows. The major feedback parameter N_s is varied to simulate temperature effects on V_{oc}. Similarly, a feedback parameter in the regulator of the constant current source is varied to simulate illumination effects on I_{sc}. By a variable resistance summing network, a function generator is coupled to the regulator of the same current source. In this manner the function generator modulates the reference current to simulate spin ripple. The magnitudes of the open circuit voltage V_{oc}, short circuit current I_{sc}, and spin current I_{sp} are digitally programmable. Built-in logic electronics and relays control resistor banks. At present, the basic unit is geared to process manual commands. However, adequate space has been provided for a master programmer, and, with minor wiring modifications, capability can be extended to include remote automatic programming. Thus, to interface with an external process control unit or tape reader, control logic easily can be incorporated to process decoding, error-checking, and steering programmer commands.

For the ESAS 20 kW system, attain using the FRSAS modular approach (Figure 6.1-3), choice of the number of main programmers deserves consideration. The present programmer design of the FRSAS unit requires 32 major command carrying wires coming from manual controls. If a main programmer is included to allow automatic programming, say from a process control unit, interface command wires can be reduced to about eight. Therefore, a 20 kW system using 10 expanded FRSAS units, each with its own main programmer, requires 80 interface command wires.

On the other hand, if one master main programmer is used for all units, the number of interface command wires increases to 320. The former offers an advantage from a technical point of view, since the probability of erroneous commands stemming from noise pick-up and crosstalk would be one-quarter as much.

Using the PSSAS approach (the power supply solar array simulator described in Section 6. 2), V_{oc} and I_{sc} of the IV characteristic can be varied by programming four separate resistors. Each power supply has two controllable resistors, one for setting constant voltage and one for setting constant current. The programming coefficients, in ohms per volt and ohms per amp, are obtained from the manufacturer. The power supplies to be used are of the automatic crossover type. This type of supply is unique in that it cannot be overloaded. It operates into any load from infinity to zero ohms. From infinity to crossover resistance it behaves like a constant voltage source. From crossover resistance to zero ohms it acts like a constant current source. With independent controls for the current and voltage, the crossover point can be located anywhere in the volt-ampere range of the power supply.

Because the resistors to be programmed are the feedback proportioning resistors in the voltage and current loops of the supplies regulators, special care must be taken to minimize certain factors that normally contribute to problems encountered in an application such as this. The use of precision metal film resistors with low temperature coefficients is required. Minimum lead length from resistors to comparators are necessary to avoid introducing inductance in the feedback loop. Location of the resistor banks is important since noise pick-up can be amplified. Portecting against momentary programming errors that result during interval switching will have to be worked out with the power supply manufacturer. The manufacturer can be asked to make provisions for an external ac signal to modulate the current limit, thus allowing simulation of I_{SPIN}.

To control the two power supplies two programmers of the type designed and developed for the FRSAS can be used. However, if it is desired to have the slope generators (Figure 6. 2-2) remotely programmable also, an additional programmer will be needed.

The slope generators referred to are optional and would be used only if adjustable IV slopes are desired. Load bank resistors made from special chromium alloy stainless steel are presently available. The Post-Clover Electric Company makes such units. In this particular application, heavy current relays across the load bank taps would be controlled by the programmers.

In the PSSAS, all the parameters mentioned can be programmed. However, the complexity associated with programming these parameters through any given range will be proportional to the degree of resolution desired in that range.

In the DISAS, the diode solar array simulator described in Section 6. 3, programming of I_{sc} to exhibit illumination and spin effects is fairly straightforward. A programmable constant current source similar to the one used in the FRSAS can be used as the bias for the power stages. Because of transistor voltage limitations, placing in series two independent sections of the basic configurations shown in Figure 6. 3-1 is preferred.

Programming V_{oc} to reflect temperature effects is more difficult but not impossible. For example, the 10 volt modules could be constructed with additional taps to allow bypassing of some of the diodes. Another possibility is to have heater elements built into the modules to vary the tempeature of the diodes.

Two programmers of the FRSAS design would be required to program the DISAS for illumination, ripple, and temperature variations.

6. 5 FREQUENCY RESPONSE CAPABILITIES

An ideal solar array simulator design is one that offers the capability to generate a true IV static curve, to program all parameters affected by temperature, illumination, etc., and to exhibit an ac response equivalent to the array being simulated.

A comparison of the expected output impedance for the three proposed concepts presented in Sections 6. 1, 6. 2, and 6. 3, is shown in Figure 6. 5-1. The desired simulator impedance is extracted from data plotted in Figure 5. 4-13, which is for a particular cell, at a particular operating point and temperature. The PSSAS and DISAS curves are only estimates because both systems use power supplies directly and supply manufacturers seldom provide output impedance data as a function of operating point; some do provide a typical characteristic.. For this application the supply user would need a better specification presentation of this parameter. The FRSAS curve was obtained from extrapolated

test data. The simulator at the time had been set for V_{oc} = 50 volts and I_{sc} = 20 amps, for a ratio of N_s to N_p of approximately 1.29. Reduction of the test data by a factor of 1.29 was necessary to allow comparison of the three systems simulating a symmetrical array.

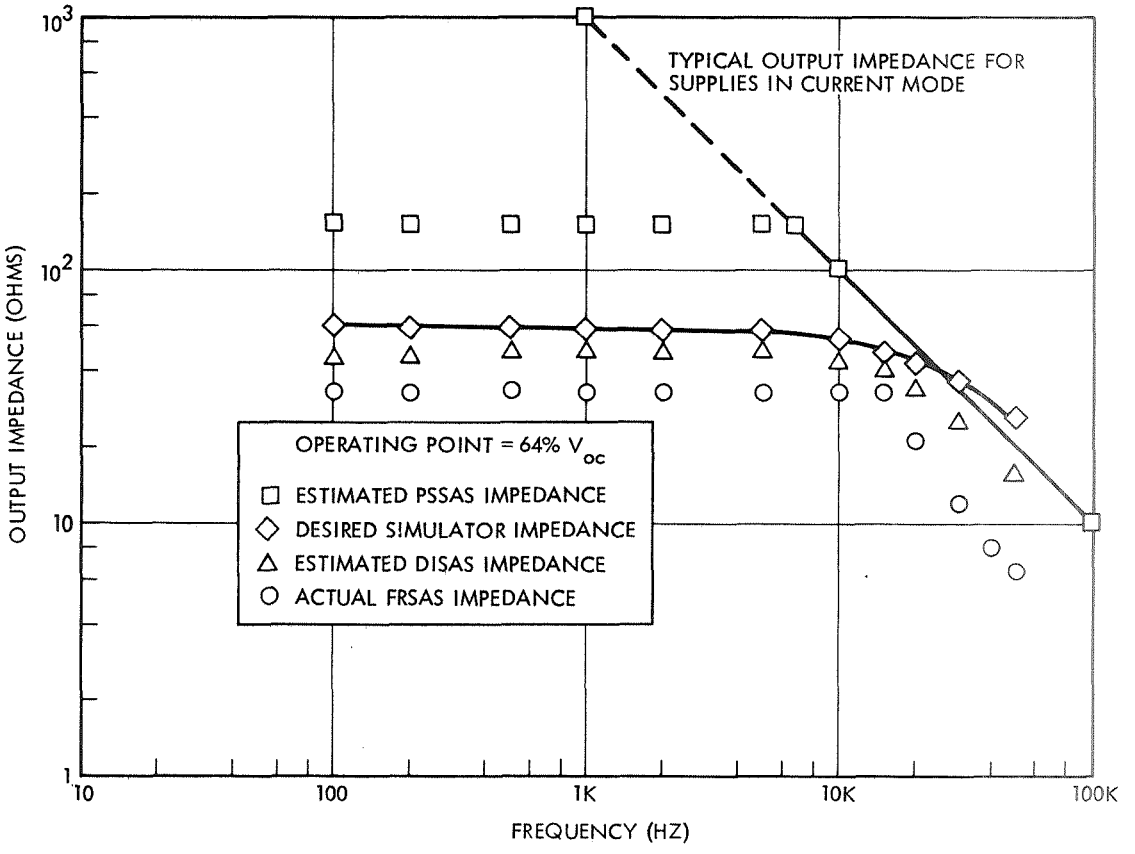


Figure 6.5-1. Comparison of the Impedance Simulation Capabilities of the FRSAS, PSSAS, and DISAS at One Operating Point for an Array of $(N_s/N_p) = 1$

The PSSAS curve shows the effect of the slope generator controlling the constant current region of the simulator's IV characteristic if it is adjusted to 152 ohms. This curve tends to remain constant with simulator operating points below 64 percent V_{oc}, introducing large impedance errors for lower operating points. Figure 5-4-13 shows that the desired impedance increases nearly two orders of magnitude when the operating point goes from 64 percent to 18 percent of V_{oc}. Test performance data has shown the FRSAS impedance increases one order of magnitude. The

DISAS tends to provide the best impedance tracking. This can be said without reservations only for the case where the DISAS uses the same cell for its diodes as the FRSAS uses for its reference.

The FRSAS uses an actual solar cell with an I_{sc} = 140 mA as a reference. The electrical design can handle cell substitutions with short circuit currents up to 140 mA. In this respect it is more versatile than the DISAS, because by cell substitution it can provide excellent static as well as dynamic simulation of a variety of solar arrays.

The DISAS concept could be difficult to implement. Use of actual large junction cells of the type comprising the array to be simulated can present quite a packaging problem. A 20 kW array using 2 x 2 cm cells has approximately half a million cells for a surface area of about 2×10^6 cm^2, or 0.31×10^6 square inches, or 2150 square feet. In addition the unit price would have to be less than 10 cents to keep the total cell cost below $50,000. To use regular diodes instead of solar cells would simplify packaging, but dynamic performance might not be as good. The diode to be used as a cell substitute would have to be selected to match the semiconductor properties of a cell, i.e., carrier lifetimes, conductivity, diffusion constants, junction area, etc. None of these parameters are noted on specification sheets. Some data sheets specify recovery or storage time, which according to Reference 5.3, is related to lifetime as follows:

$t_{dr} = 0.9\Upsilon$ for a step junction

$t_{dr} = 0.5\Upsilon$ for a graded junction

If the lifetimes of a cell and a diode can be found to match fairly closely, their impedance corners will occur at about the same frequency. The absolute value of the diode impedance will most probably be different than for a cell; however, it will vary as a function of current just like that of a cell.

7. RECOMMENDED AREAS FOR FURTHER STUDY

As an extension to the technology basis established by this study in the field of fast response solar array simulators, further study in the following areas is recommended:

- Development of a computer program to predict array impedance as it is affected by shadowing, panel decoupling diodes, and bypass diodes.
- Investigation of the effects of solar array impedance on maximum power trackers and/or switching regulators.
- Development of an experimental breadboard of a scaled-down 200 volt series-connected FRSAS configuration to prove the modular build-up concept.