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Final Report

VOLUME II

ESTABLISHING AN ELECTRICAL TEST PHILOSOPHY FOR LSI MICROCIRCUITS

February 1971

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ESTABLISHING AN ELECTRICAL TEST PHILOSOPHY FOR LSI MICROCIRCUITS

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The authors

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7. INTRODUCTION - VOLUME II

In Volume I, the authors have stated the general objectives of the task of this contract by listing the manufacturers and users of LSI microcircuits and the available test equipment. In addition, Volume I discusses test philosophies, test vehicles, and the evaluation of LSI electrical parameters. In Volume II, the authors have extracted information from Volume I and, in combination with their recommendations, have organized the material so that it may serve as a guideline for the testing of high reliability LSI devices.

8. WAFER LEVEL ELECTRICAL TESTING

The technique of employing test vehicles (test elements) on the wafer allows the verification of process control as the wafer level. The test vehicle can either be a part of the device mask or a separate mask exposed at specified locations on the wafer. The makeup of the test vehicle may range from a simple transistor to an entire circuit. Wafer-level testing can involve severe handling problems and, in fact, this is where a significant amount of infant attrition occurs. However, testing at this level is very important since one would rather discover device defects and process problems at this level rather than at final assembly after significant monetary value has been added to the device and several lots have been processed. Process monitoring of the wafer should include key parameters such as resistivity, oxide thickness (MOS) metalization, thresholds, leakage, and breakdown. Capacitance-Voltage (CV) variation plotted over temperature is also helpful in process monitoring. Desirable as it would be, tight process control and/or intensive visual inspection are not substitutes for electrical testing. (e.g., a high level of process automation.) This intensive electrical testing at the wafer level will increase infant mortality, but will allow attrition to occur at the most desirable level, at the prepackaged stage of fabrication. High speed functional testing on the wafer may present some problems and therefore the LSI testing unit must minimize lead wire capacitance problems through judicious mechanical design. High reliability applications will mandate early detection of potentially defective LSI devices.

LSI wafer level testing for MOS and bipolar devices should be implemented at ambient (25°C) temperature and 125°C. A moderate speed functional test (e.g., 50% of f max) should be made to verify functionality. This testing should be performed at worst case combinations of supply, clock, input levels, and temperature (25°C to 125°C).

Parameter testing of bipolar devices at the wafer level can be performed at ambient temperature (25°C) and should include:

- Power drain
- Breakdown voltages
- Metal continuity
- Resistivity

Parametric testing of MOS devices should include, as a minimum:

- Threshold Voltage
- Field Threshold Voltage
- ON Resistance
- Drain Breakdown Voltage
- Sheet Resistivity
- Oxide Rupture Voltage
- Metal Continuity

Utilization of test vehicles on chip that provide the above-mentioned parametric information is recommended. Readers are referred to Chapter 5 (Volume I) for a more detailed discussion of test vehicle applications.

9. PACKAGE-LEVEL TESTING—FUNCTIONAL TEST REQUIREMENTS

9.1 Functional Testing

Functional and parametric testing comprise the two general areas of LSI testing. These areas are further divided into wafer and package level testing, temperature testing, and high-and low-speed testing. LSI electrical testing is a particularly problem-ridden area due to high chip complexities, limited internal chip access, a proliferation of custom logic, mixtures of sequential and combination logic, the continual evolution of new technologies (e.g., CMOS, Field Shield, ion implantation, silicon gate, etc.) and lack of uniformity throughout the industry in testing of LSI devices.

Functional testing of LSI microcircuits comprises the generation of specific test patterns which, when applied to the input terminals, will yield information indicating the presence or absence of faults in the device. These tests routines are generally classified as either fault-diagnosis or fault-detection routines. Fault diagnosis includes the location and determination of the fault, while fault detection is, in general, the verification of the Boolean response of the device. Assumptions usually made in functional testing include the following:

- Faults can only occur one at a time
- Faults are static, not intermittent (i.e., stuck at 1, or stuck at 0)
- Logic is non-redundant

Functional testing is also categorized according to the type of logic to be tested. The logic type is either combinational or sequential. Combinational logic networks respond to each input pattern independently of the previous input. Sequential logic networks respond according to

their present state and the incoming input pattern. As a result, sequential logic testing is more complicated than combination testing. Sequential test routines, however, often include a capability for testing combinational logic.

9.2 Functional Testing Algorithms*

It is well known that the application of all possible combinations of input patterns to a device for functional testing is not at all practical, particularly with complex devices. Additionally, in as much as most LSI microcircuits are usually pin-limited, it is often impractical, if not impossible to provide sufficient external test points for monitoring the performance of internal circuit elements. The singular prohibitive factor in this exhaustive testing concept is time. As a result, algorithms have been developed outlining more efficient test approaches that will sufficiently exercise a device. Some of these algorithms are discussed in the following paragraphs.

9.2.1 Combinatorial Logic

(a) The Truth Table Method—N single faults are itemized for a particular circuit and input patterns are selected for either diagnosing or detecting these faults—N + 1 truth tables are then generated (one for the good circuit and the remainder for the circuit under each single fault condition). The test selection process becomes that of a comparison of the various truth tables.

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*Developments in L.S.I. - Motorola Semiconductors, Inc.

(b) The Method by Complements — Let G be the function for the good circuit and F be the function for the circuit with a single fault. Then the set of all tests to detect the given fault can be found from $\overline{G}F$ and $G\overline{F}$. As an algebraic example, consider that $G = AB$ and $F = A + B$. Then $\overline{G}F = \overline{B}A + \overline{A}B$ and $G\overline{F} = 0$. From $\overline{G}F$ we see that two tests are possible: $A = 1$, $B = 0$, or $A = 0$, $B = 1$. This method can be an improvement over the truth table method. However, the formation of the intersections $\overline{G}F$ and $G\overline{F}$ can be a sizable problem.

(c) The D-Algorithm — Two underlying steps are involved in this algorithm. First, having selected a fault in the net, an attempt is made to form a connected chain of the so-called D-coordinates to an output of the circuit. This determines whether the effect of the selected fault could be observed at the output. Then a consistency operation is employed in an attempt to develop an input pattern for the circuit which will account for the values set on the lines during the first step. A companion algorithm, TEST-DETECT, also uses the D-notation and serves as a kind of a converse of the D-algorithm. The TEST-DETECT algorithm finds the set of all failures detected by a given test.

(d) Tracing — A failure at a given point in the circuit is again assumed. The algorithm involves tracing forward from this point to an output and assigning logical values on the lines during the process so that the occurrence of the fault will be detected at an output. The procedure entails "backing up" if logical impossibilities are encountered. When an output that is sensitive to the fault is found, the tracing proceeds backwards from the location of the fault to the circuit inputs in an attempt to establish the required line signals which were assigned in tracing to the output. After the necessary input signals have been determined, simulation is employed to verify that the chosen test is a true test for the assumed fault.

(e) Armstrong's Equivalent Normal Form — This approach involves sensitizing a path through the circuit so that a fault along the path will be detected at the output. This method retains the path identity by means of a series of subscripts on the input variable appearing in the equivalent normal form (ENF). Each input variable may appear a number of times in the ENF possibly with different subscripts, each time corresponding to different paths through the net. Thus if X is an input variable, then X_{257} identifies the path from input X on gate 2 through gates 5 and 7 to the output. Similarly, X_{268} denotes the path from input X on gate 2 through gates 6 and 8 to the output. In this procedure, X_{257} and X_{268} are considered as two different "literals". It proves that a test devised for a literal appearance in the ENF sensitizes the path in the original net associated

with that literal apperance. Since the ENF is a sum-of-products expression, devising a test for a literal appearance is relatively straightforward. This algorithm leads to tests which detect large numbers of faults. The procedure may, however, become cumbersome when there is a large number of paths through the net.

9.2.2 Sequential Logic

(a) Straight Simulation—The N faults to be tested are selected and a test, consisting of a sequence of input combinations, is derived by manual or other means. Presumably,the test either controls (resets) or determines the state of the circuit as mentioned above. Then,the system is simulated once in its correct state and N other times to account for each fault individually. The test is applied to the N + 1 simulated circuits and faults detected by the test are identified. If there are any faults that are undetected at the end of the test, changes are made in the test to attempt to correct these omissions. Present day simulations involve sophisticated programs on a digital computer where techniques such as "parallel error simulation" achieve a marked reduction in computer time.

(b) State-Diagram Technique —— Employs a distinguishing sequence (DS) to check transitions between states in sequential machines. If a sequential machine has N states, then an input sequence is a DS if it yields N different output sequences depending on the initial states.

In these state-diagram techniques the test procedure consists of the following steps:

(1) Check the initial state by using the DS.

(2) Apply an input which causes the circuit to change state.

(3) Check the transition made in step 2 by using the DS.

(4) Repeat steps 2 and 3 until all state transitions have been checked.

An advantage of the state-diagram technique is that faults do not have to be enumerated, i.e., assumed by the diagnostician. A disadvantage is the often excessive length of the test sequence.

(c) The Scan Technique —— The SCAN concept is used in Fault Location Technology (FLT) developed for the IBM System/360. Extra inputs and outputs are added to the sequential circuit so that data can be scanned into the storage elements of the circuit with the result that all states are known. The test is then applied and the results are scanned out for analysis. The FLT approach employs both the tracing and SCAN techniques. The disadvantage of the SCAN approach is that it is not very suitable for pin-limited packages.

(d) The Seshu Approach—In the Seshu approach, each single fault is assumed to transform the given circuit into another circuit. Thus, for N faults, we have N + 1 different circuits where the 1 accounts for the good circuit. The assumption is also made that the feedback lines can be reset momentarily to a known initial state, even under failure conditions. An input pattern is applied to the N + 1 circuits (through simulation on a computer) and, on the basis of the output, the N + 1 circuits are partitioned into equivalence classes where each member of a given class has the same output for the given input pattern. Then, one of the equivalence classes is further partitioned by another input pattern. All equivalence classes are eventually partitioned as far as possible in this manner. The procedure employs local optimization at each step, that is, the effects of all possible input patterns which differ in one bit position from the previous applied input pattern are simulated, and the actual choice of which input is to be used to partition the equivalence class is based on whether detection or diagnosis is desired. Other strategies are also employed in the selection of the next input.

Testing sequences can be combinations of all 1's followed by all 0's or alternate 1's and 0's (checker board) or some other variation of binary elements. In functional testing, it is desirable to have a test system that permits a variable allocation of input and output pins and which also possesses the capability of changing all inputs at once. This allows testing flexibility from device to device and permits testing of various I/O pin configurations with maximum binary exercising.

The length and configuration of data patterns depends on the type of device to be tested. In general, the various LSI devices fall under the classifications of Random Access Memory (RAM), Read Only Memory (ROM), Shift Registers, and Logic Arrays.

ROMS require a pattern depth of 2^N, as a minimum, where N is the number of address lines. RAMS require relatively long, yet simple data patterns (e.g., write 1's, write 0's, write checkerboard) and it may be desirable to use self-generating pattern techniques to produce the large words required. The testing of Shift Registers requires propagating a logic 1 through all existing logic 0 stages and vice versa. Random logic arrays require the generation of special complex patterns. The following general recommendations are made for package level functional testing.

- Functional testing at the package level should be performed at temperature extremes ($-55^{o}C$ to $125^{o}C$)
- Functional testing should be performed at high and low speed (f_{max} and f_{min})

- Data pattern lenghts should be at least equivalent to the device length (i.e., 512 X 1 device requires a minimum test word length of 512 bits)

- Functional testing should be performed at worst case combinations of supply, clock, input levels, and temperature ($-55^{\circ}C$ to $125^{\circ}C$).

10. PACKAGE LEVEL TESTING——PARAMETRIC TEST REQUIREMENTS

10.1 General Discussion

How does one determine the quality of LSI circuits? Unfortunately, there is no simple way of answering this question without resorting to rigorous process controls and testing in the evaluation of their electrical parameters and functional performance. Due to inherent complexity of modern LSI devices, exhaustive testing of all functional parameters may require several months to complete, even if the duration of each test is reduced to as little as 10 microseconds or less. Therefore, the establishment of a meaningful and practical testing procedure which is economically feasible and which does not jeopardize the quality of high-reliability devices is of utmost importance.

The purpose of this chapter is to establish some guidelines to identify sensitive areas of functional and reliability testing in order to establish the minimum test procedures required in formulating quality standards for LSI microcircuits. Of the multitude of existing reliability indicators, only a few electrical parameters qualify to serve as significant performance indicators. These include various threshold voltage and input-output leakage parameters. It is often found that for a given failure symptom, the parameters which reflect such a situation may be dissimilar for MOS and bipolar devices. For example, a given type of device contamination may degrade the threshold voltage performance in an MOS device while the same contamination can degrade the gain characteristics in a bipolar device: such peculiarities in MOS vs bipolar device performance for a given failure mechanism necessitates the stringent monitoring of input and output levels to detect this type of behavior.

10.2 Parametric Testing——DC and AC

Electrical parameter resting of LSI devices fall into two general categories: DC or static parameter measurements, and AC or switching characteristic measurements. Parametric test relate directly to process verification and as a result are a mandatory part of LSI device testing. Test time for individual parameters is much longer than functional test time. This is due to the setup time required for each parameter along with proper sequencing of current and voltage measurements.

Measurement of device parameters at temperature extremes is a significant problem particularly for switching-time-type measurements where test fixturing difficulties can compound the problem of temperature testing. Evaluation of the temperature performance of a device should therefore be accomplished as efficiently as possible, measuring only those parameters which yield significant temperature response information. Column C of the Tables in Section 6 (Volume I) show the relative temperature sensitivity of MOS and Bipolar device parameters for several types of devices.

The extent of AC testing should be related to the intended utilization of the device. Switching characteristics of devices should be verified at as close to the designed operating speed as practicable. Characterization of circuit parameters is, at best, a compromise of proper testing procedures. For very high-reliability applications, neither bipolar nor MOS LSI processing technology is sufficiently controlled to allow ambient temperature characterization of DC parameters or low speed characterization of dynamic parameters, to preclude actual testing of the device under temperature or speed extremes.

Based on the foregoing discussion and on the thorough evaluation of the results of surveys, a number of the most critical parameters have been selected for the functional and reliability evaluation of the following four basic LSI device categories:

- Static Shift Registers
- Dynamic Shift Registers
- Random Access Memories
- Read-Only Memories

Since these minimum-required tests are for high-reliability devices (Class A, MIL-STD-883 and higher), the authors believe that 100% package testing at full temperature extremes should be mandatory. The acceptable deviations of various parameter values greatly depend both on the circuit type and technology employed. For this reason, it would not be practical to adhere to specific variations from monimal values for all parameters under test. In order to apprise the reader, however, as to the nature of this problem, we have indicated in a few cases, allowable deviations from the nominal parameter values.

Tables 10-1 through 10-7 summarize the discussion on parametric testing.

TABLE 10-1. MOS Static Shift Registers-Package Test

FUNCTIONAL PERFORMANCE PARAMETERS	RELIABILITY PERFORMANCE PARAMETERS
Input logic 0, logic 1 — under worst case input conditions: degrade the pulse width and amplitude by 50%. Use maxi-delay between clock pulses (fmin). Check logic at maximum repetition rate (fmax.)	Input Leakage Currents — all inputs (including clock) and supply leads at 20 volts or higher at elevated temperatures. A 100% change up to 1 μA is acceptable.
Output logic 0, logic 1 — under maximum load at f min and fmax.	Output Leakage Currents — Maximum degradation not more than 25%.
Clock Propagation Delay.	Input logic 0.
Repetition Rate.	Input logic 1 — maximum deviation $\pm$0.5v for standard p-channel devices.
Maximum Supply Current.	Power Drain — maximum changes -30% at +125°C.
	Output 0 and 1 Voltages — maximum degradation $\pm$20%.

NOTE: All tests done at temperature extremes.

TABLE 10-2. MOS Dynamic Shift Registers-Package Test

FUNCTIONAL PERFORMANCE PARAMETERS	RELIABILITY PERFORMANCE PARAMETERS
Inputs logic 0, logic 1 — under worst case input conditions: degrade the pulse width and amplitude by 50%. Use maximum delay between clock pulses (fmin). Check logic at maximum repetition (fmax).	Input Leakage Currents — all inputs (including clock) and supply leads at 20v or higher at elevated temperatures. A 100% change up to 1 μA is acceptable. Output Leakage Current — maximum degradation not more than 25%.
Output logic 0, logic 1 — under maximum load at f min and f max. Check the levels (for bipolar only)	Input logic 0 — maximum deviation $\pm$0.5v for standard p-channel devices. Input logic 1 — maximum deviation $\pm$0.5v for standard p-channel devices.
Clock Pulse Width.	Output 0 and 1 Voltages — maximum degradation $\pm$20%.
Clock Repetition Rate.	
Data Write (set-up) Time.	Total Power Drain — maximum changes -30% at +125°C.
Data-to-Clock Hold Time.	Clock Amplitude — at worst case loading conditions.
Maximum Supply Current.	Output Short Circuit Current (for bipolar only) — per MIL-STD-883.
Access Time — distribution of access time should be tight for a given lot: over 50% within $\pm$10% deviation from a nominal maximum value.	Minimum Repetition Rate Over Temperature Range. Power Dissipation vs. Temperature — normally double going from +25°C to -55°C, and drops 30% going from +25°C to +125°C.

TABLE 10-3. MOS Random Access Memories-Package Test

FUNCTIONAL PERFORMANCE PARAMETERS	RELIABILITY PERFORMANCE PARAMETERS
All inputs logic 0, logic 1— under worst case input conditions: degrade the pulse width and amplitude by 50%. Use maximum delay between clock pulses (f min). Check logic at maximum repetition rate (fmax).	Input Leakage Currents — all inputs (including clock) and supply leads at 20v or higher at elevated temperatures. A 100% change up to 1 μA is acceptable.
All outputs logic 0, logic 1— under maximum load at fmin and fmax.	Output Leakage Currents—maximum degradation not more than 25%.
Read-Write Cycle Time — distribution of access time should be tight for a given lot: over 50% within ±10% deviation from a nominal maximum value.	Input Logic 0.
Clock Propagation Delay.	Input Logic 1 (Threshold Voltage)— maximum deviation ±0.5v for standard p-channel devices.
	Output 0 and 1 Voltages—maximum degradation ±20%.
	Power Drain—maximum changes -30% at +125°C.

TABLE 10-4. MOS Read-Only Memories-Package Test

FUNCTIONAL PERFORMANCE PARAMETERS	RELIABILITY PERFORMANCE PARAMETERS
All Inputs logic 0, logic 1 — under worst case input conditions: degrade the pulse width and amplitude by 50%. Use maximum delay between clock pulses (fmin). Check logic at maximum repetition rate (fmax).	Input Leakage Currents — all inputs including clock and supply leads at 20 volts or higher at elevated temperatures. A 100% change up to 1 μA is acceptable.
All Outputs-logic 0, logic 1 — under maximum load at fmin and fmax.	Output Leakage Currents — Maximum degradation not more than 25%
Access Time — distribution of access time should be tight for a given lot: over 50% within ±10% deviation from a nominal maximum value.	Input logic 0.
Clock Propagation Delay.	Input logic 1 — maximum deviation ±0.5v for standard p-channel devices.
	Output 0 and 1 Voltages — maximum degradation ±20%
	Power Drain — maximum change -30% at +125°C

TABLE 10-5. Bipolar Static Shift Registers-Package Test

FUNCTIONAL PERFORMANCE PARAMETERS	RELIABILITY PERFORMANCE PARAMETERS
Input Logic 0, logic 1—under worst case input conditions degrade pulse width and amplitude by 50%. Use maximum delay between clock pulses (fmin). Check logic at maximum repetition rate (fmax). Check the levels (bipolar only)	Input Leakage Current—at inputs including clock and power leads at elevated temperatures. A 100% change up to 1 μA is acceptable.
Output logic 0, logic 1—under maximum load at fmin and fmax. Check the levels (for bipolar only)	Output Leakage Current—is relatively small. Degradation up to 10% is acceptable.
Clock Propagation Delay.	Input Logic 0.
Repetition Rate.	Input logic 1—nominally constant at specified level.
Input Load Current.	Output 0 and 1 Voltages — maximum degradation $\pm 10\%$
Maximum Supply Current.	Power Drain—maximum change +30% at +125°C.
Access Time—distribution of access time should be tight for a given lot, over 50% within $\pm 10\%$ deviation from a nominal value.	Clock Amplitude—at worst case loading condition.

TABLE 10-6. Bipolar Random Access Memories-Package Test

FUNCTIONAL PERFORMANCE PARAMETERS	RELIABILITY PERFORMANCE PARAMETERS
All Inputs logic 0, logic 1 — under worst case input conditions: degrade the pulse width and amplitude by 50%. Use maximum delay between clock pulses (fmin). Check logic at maximum repetition rate (fmax). Check the levels (for bipolar only).	Input Leakage Current — at inputs including clock and power leads at elevated temperatures. A 100% change up to $1\ \mu A$ is acceptable.
All Outputs logic 0, logic 1 — under maximum load at fmin and fmax. Check the levels (for bipolar only).	Output Leakage Current — is relatively small. Degradation up to 10% is accaptable.
Read-Write Cycle Time.	Input logic 0.
Access Time — distribution of access time should be tight for a given lot: over 50% within $\pm 10\%$ deviation from a nominal maximum value.	Input logic 1 — nominally constant at specified level
Power Per Bit.	Output 0 and 1 Voltages — maximum degradation $\pm 10\%$
Maximum Supply Current.	Clock Amplitude — at worst case loading condition.
Input Load Current.	Power Drain — maximum change +30% at $125^{\circ}C$

TABLE 10-7. Bipolar Read-Only Memories-Package Test

FUNCTIONAL PERFORMANCE PARAMETERS	RELIABILITY PERFORMANCE PARAMETERS
All Inputs logic 0, logic 1— under worst case input conditions: degrade the pulse width and amplitude by 50%. Use maximum delay between clock pulses (fmin). Check logic at maximum repetition rate (fmax). Check the levels (for bipolar only).	Input Leakage Current — at inputs including clock and power leads at elevated temperatures. A 100% change up to 1 μA is acceptable.
All Outputs logic 0, logic 1— under maximum load at fmin and fmax. Check the levels (for bipolar only).	Output Leakage Current—is relatively small. Degradation up to 10% is acceptable.
Access Time—distribution of access time should be tight for a given lot: over 50% within ±10% deviation from a nominal maximum value.	Input logic 0.
Input Load Current.	Input logic 1—nominally constant at specified level
Power Per Bit.	Output 0 and 1 Voltages—maximum degradation.
Maximum Supply Current.	Power Drain—maximum change +30% at 125°C.

11. LSI TEST SYSTEM GUIDELINES

This section describes general requirements for a high reliability LSI test system designed to accomplish all of the test objectives previously set forth in Section 7-2. A comprehensive LSI tester is inherently expensive and therefore must have long term expansion capabilities. This will allow the system to stay abreast of LSI device technology and be conservatively amortized.

The basic test objectives include the capability to automatically accomplish the following tests under computer control.

- Functional testing
- DC parametric testing
- AC parametric testing

This testing is to be performed on MOS and bipolar devices and emphasis will be on an MOS test system with bipolar adaptive capability. The MOS test capability should include p-channel, n-channel and Complementary MOS (CMOS) technologies. Testing is to be accomplished on the wafer level (64 pins) and package level (72 pins expandable) and multiplexing to allow operation of several stations is mandatory. All pin assignments (input, output, clock, power etc.) should be programmable. The tester must be capable of environmental testing over the temperature range -55°C to 125°C on the finished package and ambient to 125°C at the wafer level and these conditions (High or Low temperature) should be programmable. The system must provide operator/tester interfacing and data logging capability.

Peripheral requirements should include as a minimum:

- Teletypewriter (ASR 33)...For operator/tester communication
- High Speed Printer........For data print out
- Magnetic Tape I/O.........For test inputs and data logging output
- Additional Memory.........Allows expansion of test capability (DISC)

The functional test rate should be variable from 100 Hz to at least 2 MHz and data patterns should be expandable to 1024 bits. This word length can be accomplished by register chaining or by using random access memories. Six-phase clocking is required with a 50 nanosecond desirable resolution. DC Parametric testing capability should allow:

- ± 75v voltage force and measure
- ± 75ma current force and measure
- 1 v/ns slew rate

For AC testing the tester should be capable of switching time measurements over a 100 Hz to 2 MHz range with an accuracy of 0.5%. Finally, the system should utilize high level procedure oriented software for maximum programming flexibility.

12. FUTURE WORK

A logical extension of this work would be a hardware-oriented reliability study of LSI devices in wafer and package form. This study would be an empirical verification of the test techniques and test philosophy guidelines set forth herein and would serve as future documentation of the results obtained to date. The study would sample wafer and final package lots from major manufacturers of bipolar and MOS LSI. The devices would be subject to electrical (functional and parametric) tests at temperature extremes. Devices would be fully traceable and all test data would be data logged. Electrical tests would be performed according to recommendations developed in this report.

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