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Radiation Effects in MOS Integrated Circuits

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October, 1970

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16. Abstract

Integrated circuits containing MOSFETs were subjected to 1 MeV electron irradiation. Damage and annealing rates were measured as a function of irradiation dosage, dose rate, annealing temperature, and composition of MOSFET components.

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PREFACE

The objective of this work was to study the effects of high energy radiation on metal-oxide silicon field effect transistor (MOSFET) components in integrated circuit devices. One MEV electron irradiation at flux densities of the order of 10^{11} electrons per cm^2 per day was applied to the sample chips, and the characteristics were measured as a function of irradiation dosage and dose rate. Annealing of the radiation damage was measured as a function of temperature and sample composition.

The scope of the work included design and installation of instrumentation to measure the device characteristics, measurement of device characteristics as a function of irradiation and annealing history, and analysis of these results.

From this work, it has been concluded that MOS devices of the proper composition will operate satisfactorily for periods of a year or more in the space radiation environment, particularly if thermal annealing is provided.

The next logical step would be to test entire MOS integrated circuits in a space radiation environment in order to correlate circuit performance parameters with radiation effects on individual components.

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I. INTRODUCTION

This report covers work performed under contract No. NAS5-21106 for the period 20 October, 1969 to 20 October, 1970. The work was concerned principally with the investigation of radiation effects in MOS (Metal-Oxide-Semiconductor) integrated circuits, and involved the design, construction and installation of test equipment and the planning and carrying out of various experimental programs.

II. TEST EQUIPMENT

The design and construction of test equipment is divided into three areas:

1) MOS C-V (Capacitance-Voltage) System:

A system for displaying capacitance vs. bias characteristics for MOS transistors and capacitors was constructed and put into operation. The system was based on a design by K. Zaininger[1] as modified by Harold Hughes of the U. S. Naval Research Laboratory, the principal modification being the use of a Boonton Capacitance meter. The system provides an automatic bias sweep of either polarity while continuously monitoring the change in capacitance of the specimen. The characteristic is displayed on an X-Y recorder.

2) MOSFET(MOS Field-Effect Transistor) Test Panel:

A switching panel designed to provide various biasing configurations during irradiation and annealing to up to 40 single MOSFETs was installed and placed in operation. The panel, which was built by EMR under a previous contract, is presently being used to bias MOS complementary integrated circuits during irradiation. A patchboard built into the panel and connected to the IC holders permits biasing individual MOSFETs within the circuit.

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[1] K. H. Zaininger, Automatic Display of MOS Capacitance vs. Bias Characteristics. RCA Rev. 27, 341 (1966).

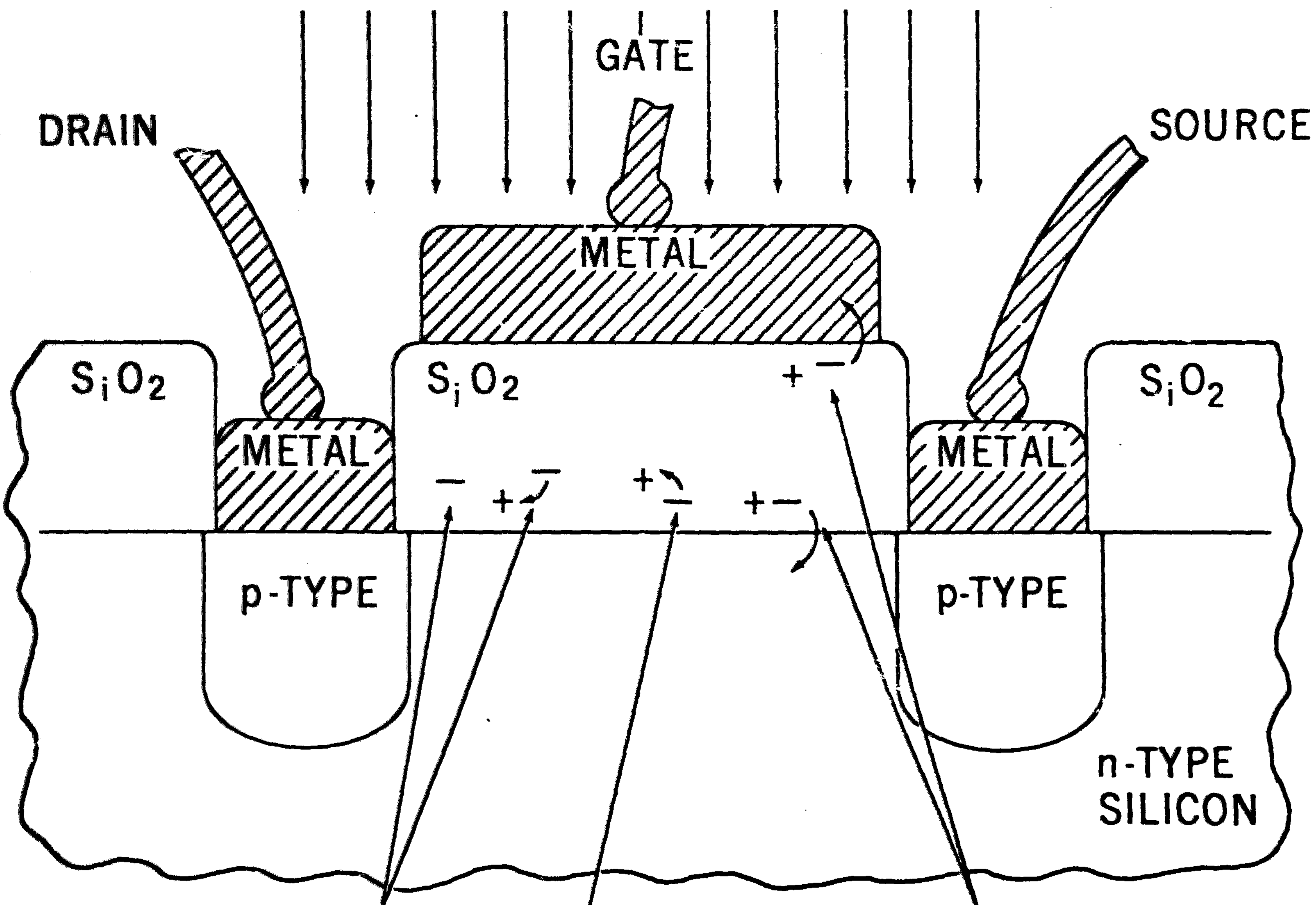
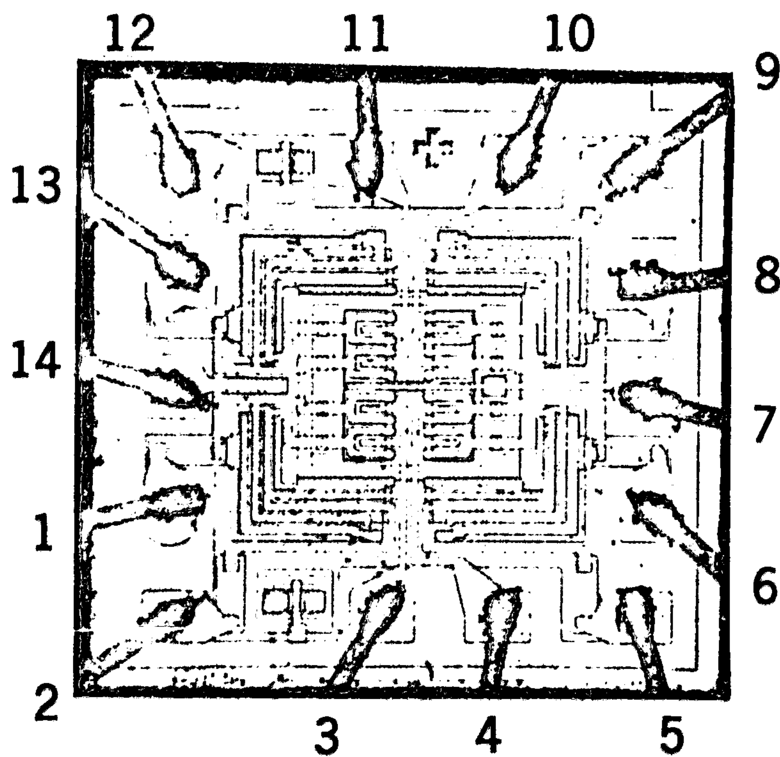
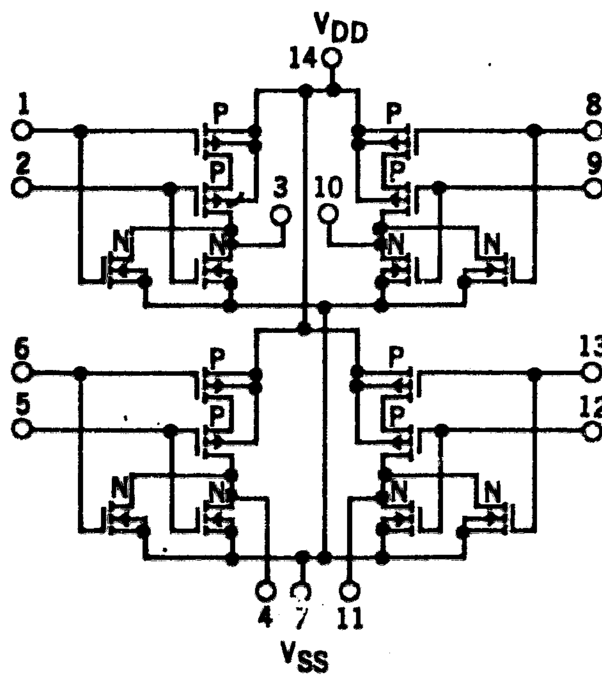


Figure 1

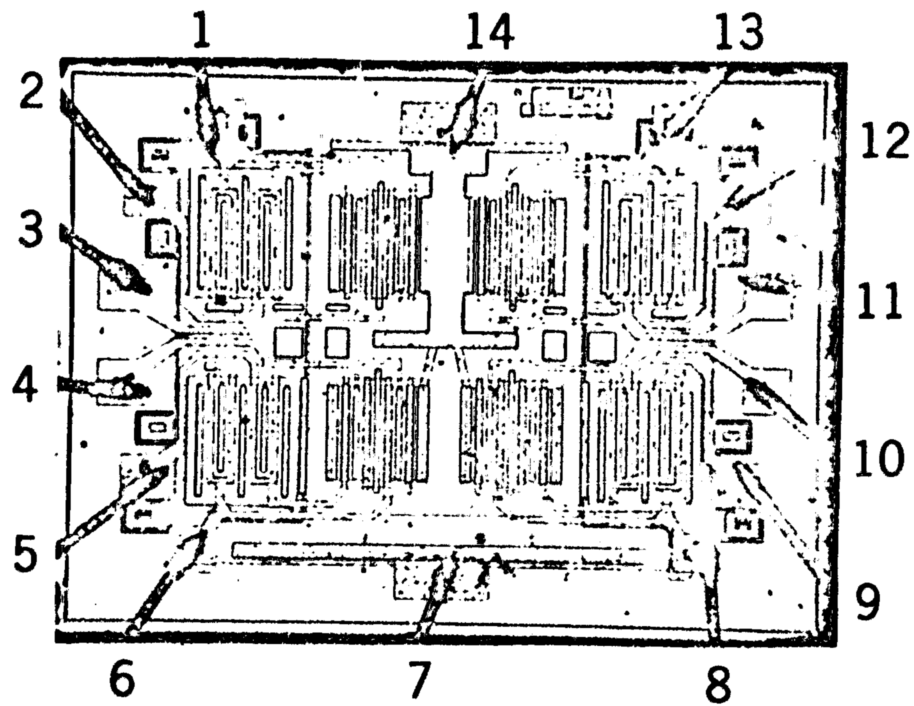
Cros -section of a typical p-channel MOSFET showing some effects of ionization in the insulating layer due to radiation.

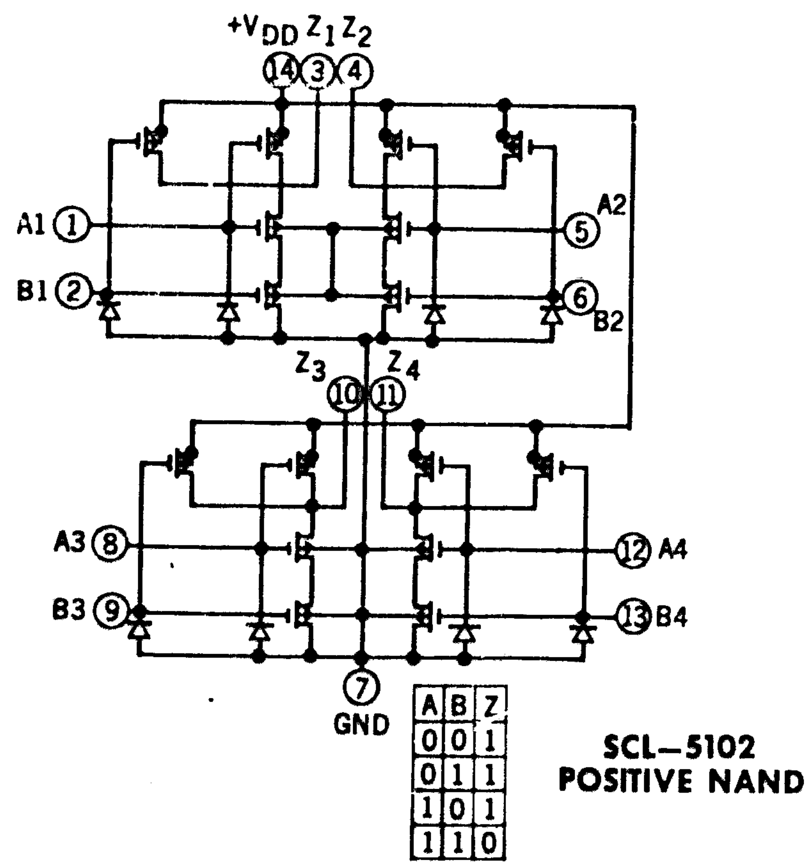




RCA CD 4001 — COMPLEMENTARY QUAD 2 — INPUT NOR

Figure 2

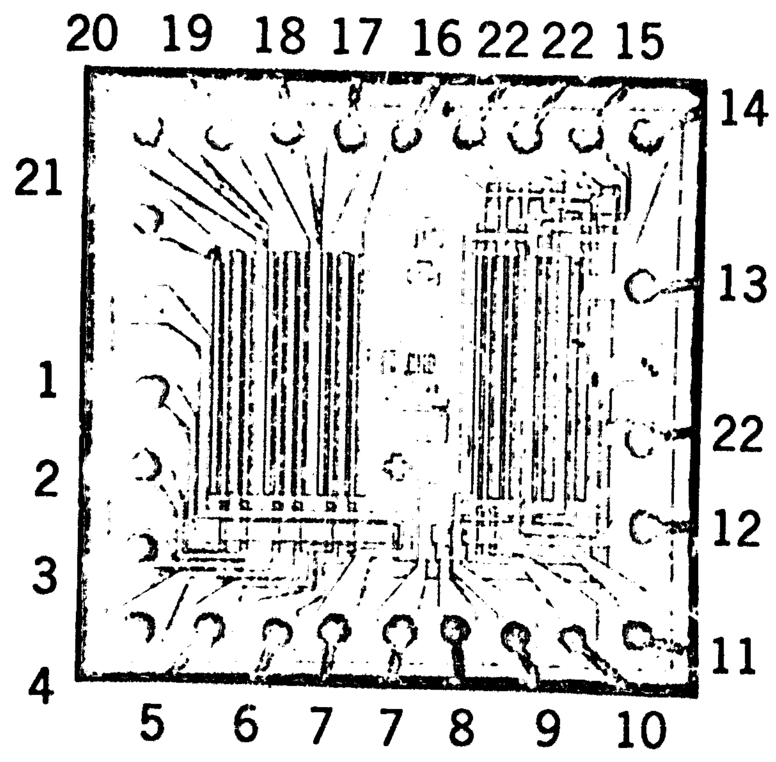


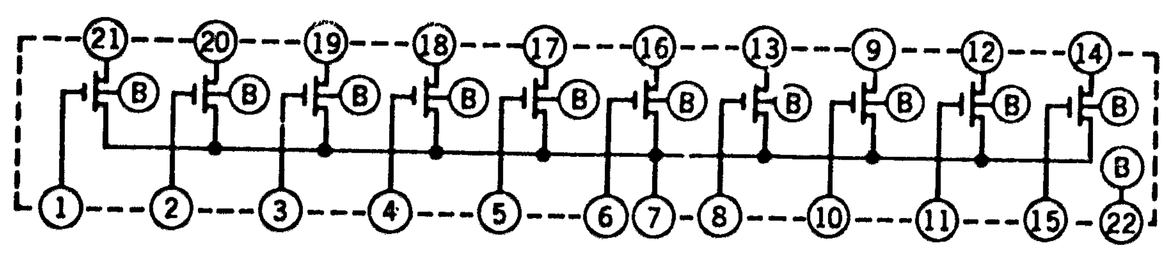


A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

SOLID STATE SCIENTIFIC SCL – 5102 – COMPLEMENTARY POSITIVE NAND

Figure 3





AMI S — 1304 OR MXO3C — p — CHANNEL
10 CHANNEL SWITCH

Figure 4

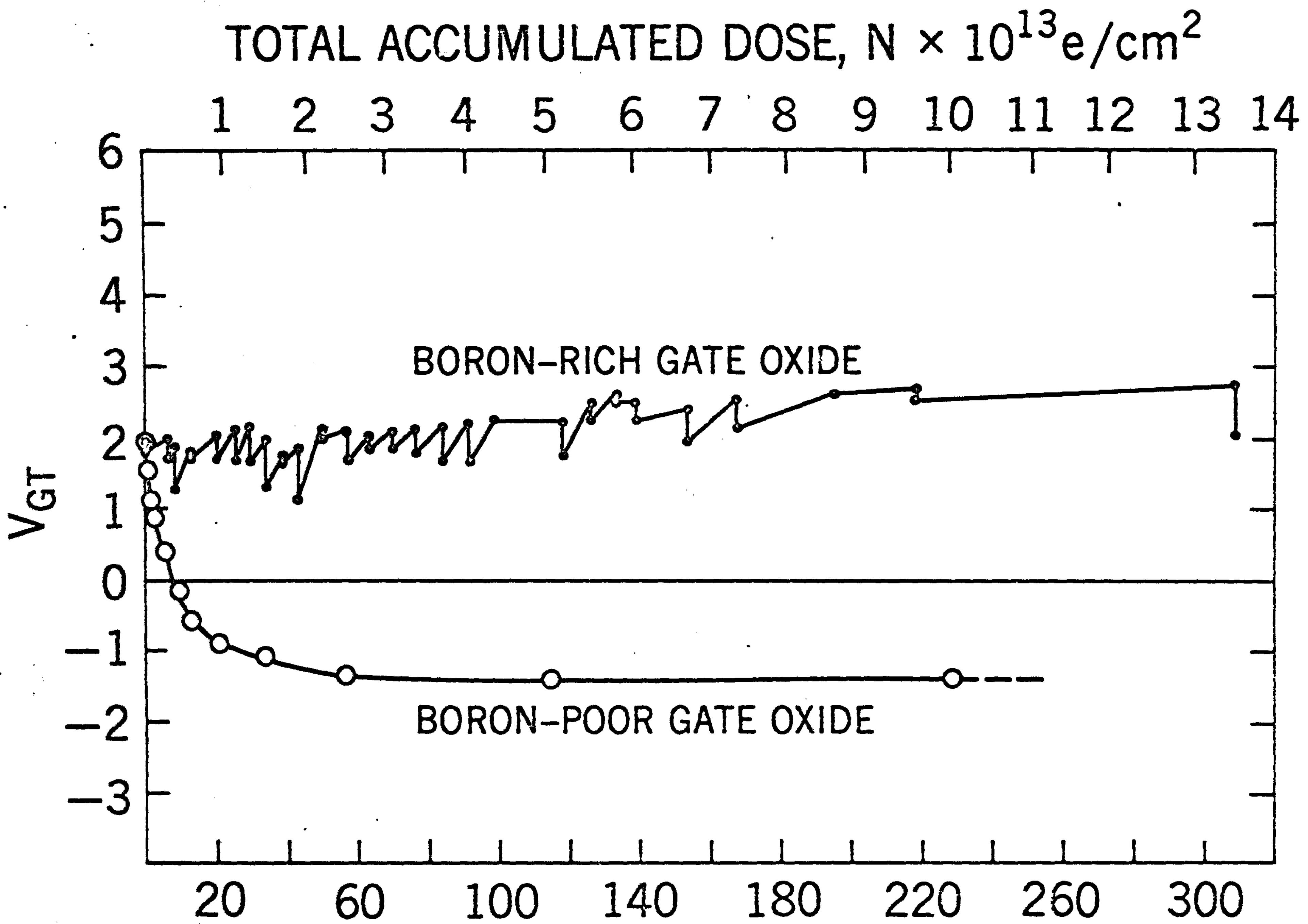


Figure 5

Comparison of simulated space radiation effects on n-channel MOSFETs in an integrated circuit, in which the MOSFETs in one of the circuits have been enriched with boron. The Y-axis shows the gate threshold voltage, V_{gt}, in volts and the X-axis, above, shows the total dose, in 1 MeV electrons, and, below, the equivalent number of days in orbit for a synchronous satellite (altitude, 22,500 mi.).

3) Irradiation and Test Jigs:

The testing of MOS complementary ICs has necessitated the construction of various special irradiation and testing circuits. In order to measure the interactions between individual MOSFETs on the same chip and to obtain individual I-V characteristics, the integrated circuit must be operated in other than the normal manner. For example, to obtain an I-V curve for the p-Channel MOSFETs in a simple inverter pair, the output is used as ground and the circuit ground is left open. To facilitate taking the large number of such curves required in a single experiment at the required speed (up to 400 per day), a separate switching system to read each manufacturer's device had to be built. Connectors were also constructed to interface the standard IC holders with the biasing panel during irradiation.

III. EXPERIMENTS

The experimental phase of the work is divided into six principal areas:

1) Westinghouse (ATS) Experiment:

This experiment was begun on March 26, 1970. Its purpose was to attempt to approximate in the laboratory the radiation environment of a synchronous satellite and to observe its effect on various MOS integrated circuits. The circuits used were as follows:

RCA	CD-4000	Dual 3-input NOR plus inverter
	CD-4001	Quad 2-input NOR (Fig. 2)
	CD-4002	Dual 4-input NOR
	CD-4013	Flip-Flop
SSS	SCL-5102	Quad 2-input NAND (Fig. 3)
	SCL-5104	Dual 3-input NAND
	SCL-5106	Dual 4-input NAND
AMI	MX03C	Multiplexer (Fig. 4)

1 MeV electrons from a Van de Graaff generator were used to provide simulated space radiation for both shielded and unshielded devices. The radiation doses were:

Shielded: 7×10^{10} electrons/cm^2/day
Unshielded: 4.4×10^{11} electrons/cm^2/day

During irradiation, the gates were continuously switched with a 10 KHz, +10V, 50% duty cycle square wave input. Readings of the p-channel, n-channel and gate threshold voltages were made using a circuit constructed by Westinghouse. In addition, current-voltage curves were taken on a few gates in each device. After nine months of simulated space radiation, most of the devices were no longer functioning, due to shorts developing between the V_{dd} and ground connections. Devices still functioning as of October 20, 1970 are:

RCA	CD-4001	#3
	CD-4002	#10
SSS	SCL-5102	#'s 6, 12
	SCL-5106	#224
AMI	MX03C	#'s 304, 309, 407

Results of eight months of low-does-rate irradiation show distinctive differences when compared with samples which received the same doses in a matter of hours. While the low-dose-rate samples exhibit a shift of threshold voltage which is approximately logarithmic with respect to dose, the high-dose-rate samples show what is apparently a radiation-induced annealing of space charge build-up in the oxide, which slows down and eventually reverses the shift. Further study of this dose-rate dependence may lead to better understanding of the mechanism of the space charge accumulation.

2) SSS Boron Diffusion Experiment:

During irradiation experiments with complementary MOS (CMOS) circuits of various technologies and with single n-channel MOSFETs, it was repeatedly observed that some n-channel devices in complementary circuits annealed far more rapidly at room temperature than did other n-channel devices (see Fig. 5), and that all of these annealed more rapidly than single n-channel MOSFETs. In contrast, p-channel devices exhibited virtually no annealing.

Since Boron is frequently used as a dopant in forming the substrates for the n-channel devices in complementary circuits (but not in single n-channel MOSFETs), and thus would be found in the oxide after it is grown, and since this is the only essential difference between the n-and p-channel devices, it was postulated that the additional boron in the n-channel oxide was somehow responsible for this rapid annealing.

To test this hypothesis, some sample CMOS circuits were prepared by Solid State Scientific, Inc. (SSS), in which both n-and p-channel devices received an additional boron diffusion after all the other steps had been carried out on the wafer.

Results from the initial test run were erratic and inconclusive, but the results from the second and third test runs showed a great increase in annealing of the p-channels, as had been hoped. The exact mechanism of boron-enhanced annealing is unknown at present, and results are very difficult to reproduce, due to difficulties with the boron diffusion process, but the results so far indicate that additional work in this field should prove quite promising.

3) Heater Experiment:

Several single MOSFET units have been fabricated with an aluminum heating element deposited directly over the gate region of the MOSFET. By applying a current through this heater, it should be possible to anneal out the space charge build-up in the oxide in flight, and thus prolong the life of the devices during a mission. A circuit was constructed to take the transfer characteristics of the devices and apply power to the heater. Temperature of the devices was measured by observing the reverse-bias current of the diodes formed by the substrate and the drain or source region of the MOSFET (see Fig. 1). Due to defects in the heater deposition, it was not possible to take any of the devices tested above 200°C without failure of the heater.

4) C-V Measurements:

A series of experiments were conducted on several MOS transistor-capacitors using the capacitance-voltage (C-V) system described above. The devices consisted of a single MOSFET and a single MOS capacitor (i.e., an MOS gate without the additional p-n junctions for the source and drain). The gate insulator of the devices consisted of a 96 Å layer of silicon dioxide (SIO_2) over which was deposited a layer of 1200 Å of silane, or silicon nitride (SI_3N_4). The devices were first tested in their unirradiated condition, after which they were irradiated and again tested. Thereafter, the devices were annealed at various temperature steps from 150° C up to 350°C. At each step, C-V readings were again taken. For each reading, two curves were taken: one at room temperature (300°K), and one with the device immersed in liquid nitrogen (77°K). Comparison of the two curves, and observation of the hysteresis seen in going from full accumulation to full depletion and back again may yield some information on the nature of the charge trapping states in the semiconductor-oxide interface. Further, the record of changes in the density of charge states as the devices were annealed may be amenable to activation energy analysis using the method of Vand[2] and Primak[3], yielding additional data on the radiation damage mechanisms.

5) Room-Temperature Annealing

During the period covered by this contract, some preliminary work on room-temperature annealing of radiation damage in MOS integrated circuits was completed. This consisted simply of irradiating the circuits in various operating configurations and then allowing them to stand, while taking curves of the operating characteristics of each MOS device in the circuit at logarithmically increasing intervals of time. This procedure served to give some idea of the rate at which the devices might be expected to anneal naturally in space.

6) Read-Only Memory:

The repeated observation in various MOS integrated circuits that the voltage applied to the gates during irradiation strongly affects the resultant shift in

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[2] V. Vand, Proc. Phys. Soc. (London) A55. 222 (1943).

[3] W. Primak, Phys. Rev. 100, 1677 (1955).

switching threshold of the respective component MOSFETs may have some value in producing an MOS read-only memory for use in on-board spacecraft computers. In such a memory, an initially "blank" MOS memory would be programmed by biasing selected MOS units while irradiating the entire memory, thus "turning off" (or "turning on") the selected components.

As a preliminary test of the feasibility of such an idea, tests have been made using the GI MEM 551, a dual p-channel MOSFET. One of the devices was biased and the other shorted while being subjected to sufficient irradiation to shift the biased device's threshold into the "0" range while the unbiased device remained in the "1" range. The devices were then allowed to stand, while being tested periodically to observe the decay of the radiation-induced shift.

The devices have so far stood for almost one year without the originally biased devices' thresholds shifting out of the "0" range of voltage values, thus implying that a similar read-only memory would remain functional for at least as long.

IV. CONCLUSION

During the period covered by this report, techniques have been developed to characterize the DC performance parameters (gate threshold voltage and transconductance) of single MOSFETs within MOS integrated circuits. Also, by use of capacitance-voltage measurements at various temperatures, an additional method of observing the charge trapped in the insulator of a MOS device has been found.

As far as the development of electronic space hardware is concerned, the next logical step would seem to be to begin observing the performance of MOS IC's in their entirety in a space radiation environment in order to correlate

circuit performance parameters, such as noise immunity and switching speed, with what has already been determined about radiation effects in their component MOSFETs.