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Technical Report 32-1540

Digital Command System Second-Order Subcarrier Tracking Performance

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Preface

The work described herein was performed by the Telecommunications Division of the Jet Propulsion Laboratory.

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Abstract

Equations are derived for the timing performance of the all-digital, second-order, phase-locked loop proposed for the *Viking* Orbiter and TOPS programs. The theory is compared with experimental results and found to agree well over the range of interest.

Digital Command System Second-Order Subcarrier Tracking Performance

I. Introduction

This report derives the relevant equations necessary to determine performance for the second-order, all-digital, phase-locked loop (ADPLL) used for subcarrier synchronization on an all-digital command system proposed for the *Viking* Orbiter and TOPS programs. The results include the steady-state phase error variance, the damping ratio, and the loop noise bandwidth for the second-order subcarrier loop. In addition, the loop noise bandwidth of the first-order subcarrier loop is obtained. The results are based on a "linear equivalent" analog PLL model which was apparently first used by Hurd (Ref. 1) for a digital loop that had an analog phase detector. From the linear equivalent model, using known results, the performance of the digital loop can be determined, excluding quantization and doppler effects. These effects are treated separately and then combined with the linear equivalent results to obtain the total phase error performance. The general approach of the linear equivalent analysis is applicable to instrumentations of the digital phase lock loop that are different from the one considered here.

The first-order, all-digital, phase-locked loop was analyzed in SPS 37-64, Vol. III (Ref. 2). At the time of that analysis, the relative doppler shift was assumed to have a maximum value of 1×10^{-5}. Recently it has been determined that the maximum relative doppler rate is, in fact, 1×10^{-4}, an order of magnitude larger. This increase caused the bias in the phase error, due to the doppler, to increase to an unacceptable level in the earlier design. It was therefore necessary to modify the existing loop to incorporate a true second-order filter, so that, in theory, all the bias would be eliminated. The resulting version of the second-order ADPLL is shown in Fig. 1.

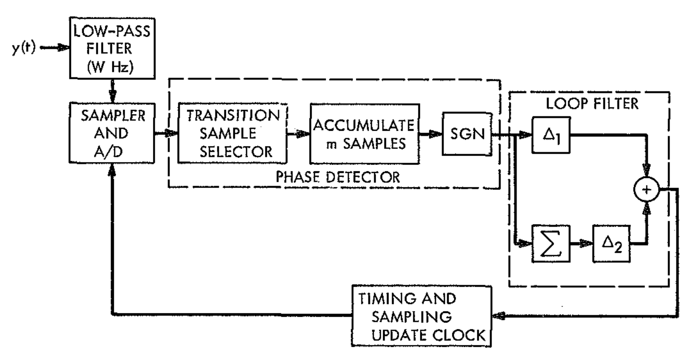

Fig. 1. Block diagram for all-digital, second-order phase-locked loop

II. Operation of the Second-Order Loop

The loop operates in the same manner as the existing first-order ADPLL (Ref. 2) except for the addition of the summer branch (discrete integrator) in the loop filter. The incoming waveform $y(t)$ is assumed to be composed of a squarewave subcarrier of amplitude A, with period T_{sc} that has passed through an additive white Gaussian noise channel. The spectral density of the channel noise is denoted by $N_0/2$ (two-sided). The low-pass filter (assumed to be ideal) passes all frequency components out to W Hz. The sampler obtains a sufficient number (16 in this case) of equally spaced samples per subcarrier (SC) cycle to adequately represent the signal. These samples are then converted by the analog-to-digital converter to digital format (4-bit words in this case). It is assumed that the digitizing introduces negligible error. The phase detector selects the sample corresponding to the point the detector thinks is the center of a subcarrier transition. If every transition sample were used there would be two transition samples per subcarrier cycle. However, due to modulation some samples are ambiguous and cannot be utilized. After the accumulation of m of these transition samples, the accumulation is hard quantized. This quantizing process is represented by the signum (SGN) block in Fig. 1. The output of the hard quantizer which occurs every M SC cycles is either $+1$ or -1 and is multiplied by a signal proportional to Δ_1, which is measured in fractions of a subcarrier cycle (FSCC). This signal then increments the clock timing by $2\pi\Delta_1$ radians. Simultaneously, the output of the hard quantizer is added to the summer of the loop filter, which produces an output proportional to Δ_2 times the value stored in the summer. This component increments the clock or transition sampler timing by $2\pi\Delta_2$ radians, where Δ_2 is specified in FSCC.

To summarize, the phase detector updates the timing every M SC cycles. The update is derived from the accumulation of m transition samples ($m \leq 2M$) and is hard quantized and fed to the loop filter. The filter controls the transition sampler timing by bumping the clock in such a manner that the timing is corrected by a discrete phase increment every M SC cycles.

III. Analysis of the Linear Equivalent Loop

An exact analysis based on Markov chain theory appears to be quite difficult to obtain for this particular second-order loop configuration since the error state of the ADPLL is no longer a simple random walk as it was in the first-order ADPLL. Consequently, to compute the steady-state error variance, the ADPLL is first modeled by an equivalent analog PLL so that the known results for analog loops can be applied. Then the effects of quantization and doppler are considered.

We shall now derive the analog equivalent loop. First, we extend the discrete phase updates to sample-and-hold, piecewise-continuous time signals (each sample is held for M subcarrier cycles) in such a way that the total phase shift in radians is the same for the discrete time DPLL as the sample-and-hold analog loop. We now describe the analog model of each element of the digital loop.

The timing update clock is modeled as an analog oscillator with the VCO parameter, $K_{vco} = 2\pi/MT_{sc}$, so that a fixed timing update of Δ out of the loop filter produces a timing (or phase) change of $2\pi\Delta$ radians. Hence the equivalent analog oscillator, in Laplace notation, can be represented as K_{vco}/s, with

$$K_{vco} = \frac{2\pi}{MT_{sc}} \tag{1}$$

Thus, instead of bumping the digital timing loop by $2\pi\Delta$ radians every MT_{sc} seconds, the analog loop is linearly phase-shifted such that in MT_{sc} seconds it has been shifted by $2\pi\Delta$ radians.

The actual output from the signum function (SGN) is a sequence of pulses spaced MT_{sc} seconds apart which vary in sign depending on the timing error and the noise. The pulses, when fed through the filter to the clock, tend to decrease the phase error after each adjustment. Under the assumption that the loop is narrow-band, the output of the hard quantizer of our "equivalent" analog loop can be modeled as a continuous signal plus the phase detector noise in the form

$$A_{eq}\,\phi + n'(t) \tag{2}$$

where ϕ is the phase error of the analog model expressed in radians, and A_{eq} is the average (equivalent) small signal gain defined, as in Ref. 1, by

$$A_{eq} = \left.\frac{\partial E\,[\hat{\phi}(\phi)]}{\partial \phi}\right|_{\phi=0} \text{rad volt} \tag{3}$$

The term $\hat{\phi}(\phi)$ is the phase detector estimate of the true phase error ϕ. Owing to the hard quantizer, $\hat{\phi}(\phi) = \pm 1$. The equivalent noise is modeled as a random sequence of pulses of amplitude 1 and duration MT_{sc} seconds. We model the occurrences of a "+1" or a "−1" as being equally likely, noting that this is only strictly true when $\phi = 0$. It is, however, a good approximation as long as ϕ is small, and since we are assuming narrow-band operation the phase error will be small with high probability. At this point we can depict our "equivalent" analog PLL model as shown in Fig. 2.

The equivalent input is the signal phase θ plus the equivalent noise normalized by the small signal gain. The oscillator produces $\hat{\theta}$, an estimate of θ. Hence the error control signal is composed of the phase error ϕ plus the normalized equivalent noise. The equivalent gain block of the equivalent loop transforms the error at the output to $A_{eq}\phi + n'(t)$.

The filter $F(s)$ is modeled as follows:

$$F(s) = \Delta_1 + \frac{\Delta_2}{MT_{sc}s} \qquad \Delta_1, \Delta_2 \text{ in FSCC} \tag{4}$$

where the first term represents the proportional update and the second term represents the analog equivalent (integrator) of the summer in the loop filter. The normalization by MT_{sc} accounts for the difference in output between a summer with a sampled input and an analog integrator with a sample-and-hold input. Using Tausworthe's notation (Ref. 3) for a perfect integrator, second-order analog loop we have

$$F(s) = \frac{1 + \tau_2 s}{\tau_1 s} = \frac{\tau_2}{\tau_1} + \frac{1}{\tau_1} s \tag{5}$$

By direct comparison of the two filters (Eqs. 4 and 5) we have

$$\tau_1 = \frac{MT_{sc}}{\Delta_2} \quad \text{and} \quad \tau_2 = MT_{sc}\frac{\Delta_1}{\Delta_2} \tag{6}$$

Now we consider the spectrum of the equivalent noise process by considering first the time autocorrelation function. Since we assume all pulses have duration MT_{sc} seconds and take on the values of $+1$ or -1 with equal probability, it can be shown that the correlation function $R(\tau)$ is given by

$$R(\tau) = 1 - \frac{|\tau|}{MT_{sc}} \tag{7}$$

for $-MT_{sc} \leqq \tau \leqq MT_{sc}$ and is zero elsewhere. The associated noise power spectrum under the assumption that $\omega MT_{sc} << 1$ is well approximated by

$$P(\omega) = MT_{sc} \tag{8}$$

so that if the loop noise bandwidth W_L is small compared to $1/MT_{sc}$ it can be assumed that $P(\omega) = P(0)$ for all ω. This assumed flatness of the noise is utilized to evaluate the phase error variance.

Now consider the heart of the ADPLL, the phase detector. The detector is formed from the combination of the transition sample detector, the hard quantizer, and the transition shape of the subcarrier waveform along with the m-sample accumulator. The model of the low-pass, filtered, squarewave subcarrier signal is illustrated in Fig. 3. The transition region is modeled as a linear function since laboratory experiments indicate that it is essentially linear.

The transition region forms an integral part of the phase detector as will be seen in the following. If, for example, the loop thinks the zero crossing is located where the negative going transition sample in Fig. 3 is positioned, a signal proportional to the error τ plus the value of the noise sample is added to the present value of the m-sample accumulator. After m of these error signals, corrected for algebraic sign, are accumulated, the sum is hard-limited by the hard quantizer. The output of the quantizer is passed through the second-order filter to the timing clock in such a manner as to tend to decrease the timing error. The larger the timing error the larger the probability of a correct timing update, up to $|\tau| = \Delta T_{sc}/2$.

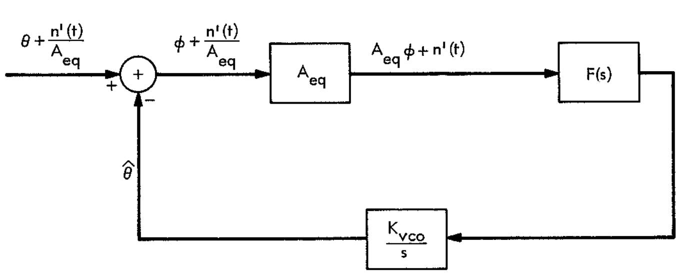

Fig. 2. Equivalent analog linear loop model

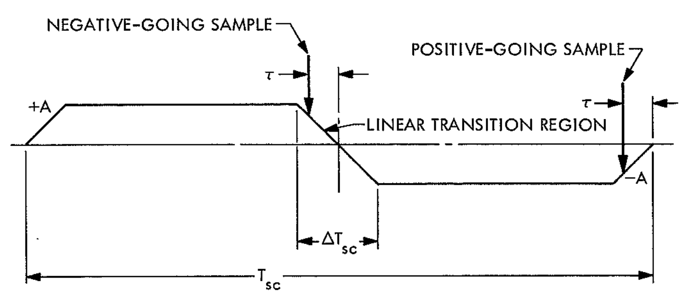

Fig. 3. Model of the filtered subcarrier waveform entering sampler with a timing error of τ

For larger values of $|\tau|$ the error control signal remains constant so that the probability of correct timing update is also constant; the control signal then decreases as the error nears 180 deg in magnitude (Fig. 3).

For a timing error of less than $\Delta T_{sc}/2$, where ΔT_{sc} is the duration of the transition, a noiseless transition sample will produce an error control signal e given by (Fig. 3)

$$e = \frac{AT_{sc}}{\pi \Delta T_{sc}} \phi \qquad \text{rad} \tag{9}$$

In the remainder of the analysis we assume that the probability of the error exceeding $\Delta T_{sc}/2$ is very small (i.e., we assume high loop SNR), so that we can assume (9) holds for all ϕ. In general, the samples are noisy with Gaussian noise n_i added to the control voltage e. Each sample has variance $\sigma^2 = N_0 W$, where N_0 is the one-sided spectral density and W is the one-sided bandwidth of the ideal low-pass filter. Thus it can be shown that the phase detector estimate $\hat{\phi}(\phi)$ is given by

$$\phi(\phi) = \text{SGN}\left(\frac{mA}{\pi\alpha}\phi + \sum_{1}^{m} n_i\right) \tag{10}$$

where for convenience we have let

$$\alpha = \frac{\Delta T_{sc}}{T_{sc}} \tag{11}$$

Evaluating A_{eq} from Eq. (3) (using Eq. 10) produces

$$A_{eq} = \left(\frac{2}{\pi}\right)^{1/2} \frac{c}{\sqrt{m}\,\sigma} \text{rad}^{-1} \tag{12}$$

where $c = mA/\pi\alpha$ volts/rad. The total open-loop equivalent gain is, therefore, from Eqs. (1) and (12) and the definition of c,

$$A_{eq}K_{vco} = \left(\frac{8}{\pi}\right)^{1/2} \frac{\rho^{1/2}}{\alpha M T_{sc}} \qquad \text{sec}^{-1} \tag{13}$$

where ρ is defined to be the signal-to-noise ratio of the m samples used for updating in the region away from the transition (where the subcarrier amplitude is A) and is given by

$$\rho = \frac{mA^2}{N_0 W} \tag{14}$$

We now have all the equivalent parameters necessary to compute the steady-state phase error variance from our analog loop equivalent. It is shown in Ref. 3 that the analog loop noise bandwidth depends on the damping parameter r given by

$$r = \frac{AK\tau_2^2}{\tau_1} \tag{15}$$

where r is unitless and A, K, τ_1, and τ_2 are parameters of the perfect integrator, analog second-order PLL. Using our equivalent parameters for A, K, τ_1, and τ_2 as given by Eqs. (1), (6), and (12), Eq. (15) becomes

$$r = \left(\frac{8}{\pi}\right)^{1/2} \frac{\rho^{1/2}\Delta_1^2}{\alpha\,\Delta_2} \tag{16}$$

The damping factor of the digital loop is then given by

$$\xi = \frac{\sqrt{r}}{2} \tag{17}$$

The loop noise bandwidth is (from Ref. 3)

$$W_L = \frac{r+1}{2\tau_2} \tag{18}$$

Combining Eqs. (6) and (16) in (18) we have, for the two-sided noise bandwidth,

$$W_L = \frac{\Delta_2}{2MT_{sc}\Delta_1} + \left(\frac{2}{\pi}\right)^{1/2} \frac{\rho^{1/2}\Delta_1}{MT_{sc}\alpha} \qquad \text{Hz} \tag{19}$$

It is important to note that this bandwidth is the bandwidth of the digital loop relative to the equivalent digital loop parameters. The equivalent analog bandwidth will be defined after we obtain the phase error variance (Eq. 23).

To compute the phase error variance for the second-order loop we use the fact that, from linear analog theory, the phase error variance σ_L^2 is given by

$$\sigma_L^2 = \frac{S_n(0)\,W_L}{A_{eq}^2} \qquad \text{rad}^2 \tag{20}$$

where now the denominator is A_{eq}^2 instead of the amplitude A^2, since A_{eq} is the relative gain between ϕ and $n'(t)$ (Fig. 2). Using Eqs. (8), (12), and (19) in (20) produces the linear equivalent phase error variance

$$\sigma_L^2 = \frac{\Delta_2\pi^3\alpha^2}{4\Delta_1\rho} + \frac{\alpha\Delta_1\pi^{5/2}}{\sqrt{2\rho}} \qquad \text{rad}^2 \tag{21}$$

where Δ_1, Δ_2, and α are expressed in FSCC.

The equivalent analog loop bandwidth can then be defined by the relationship

$$\frac{N_0}{A^2}(W_L)_{eq} = \sigma_L^2 \tag{22}$$

The equivalent analog loop bandwidth when multiplied by the normalized noise spectral density produces the phase error in radians. Solving for $(W_L)_{eq}$ we get, for the second-order loop,

$$(W_L)_{eq} = \frac{\Delta_2 \alpha^2 \pi^3 W}{4\Delta_1 m} + \frac{\Delta_1 \alpha \pi^{5/2} W \rho^{1/2}}{\sqrt{2}\, m} \text{ Hz} \tag{23}$$

Letting $\Delta_2 = 0$, the equivalent analog loop noise bandwidth for the first-order loop is

$$(W_L)_{eq} = \frac{\alpha \Delta_1 \pi^{5/2} W \rho^{1/2}}{\sqrt{2}\, m} \text{ Hz} \tag{24}$$

It can be shown that if we minimize σ_L^2, as defined by Eq. (21), for fixed Δ_2, the corresponding (optimum) value of r is unity.

IV. Total Phase Error of the Loop

Unlike the analog second-order (perfect) loop, where there is no similar effect, a doppler shift increases the steady-state phase error variance of the ADPLL. This is due to the fact that the loop control is hard-limited and occurs at discrete instants of time so that an error can build up between update times. The doppler shift is defined as the difference in frequency between half the unpurged transition sample rate of the loop and the incoming subcarrier frequency.

Assume that the loop is capable of tracking a relative doppler offset of δ Hz/Hz ($\delta \leq 10^{-4}$). The change in phase error due to doppler drift, which builds up between update times (i.e., every MT_{sc} seconds), is given by

$$\phi_d = \delta f_0 M T_{sc} \tag{25}$$

where f_0 is the subcarrier frequency and MT_{sc} is the time between updates. Since, however, the present design of the loop is to update every bit time T_b, we can write Eq. (25) as

$$\phi_d = \delta f_0 T_b \tag{26}$$

When PSK modulation is present, the loop must be modified to feed back the sign of the detected bit to remove the sign of the transition sample ambiguity. Fortunately, at the nominal command bit error rate of 10^{-5}, the effect of bit errors on the performance of the subcarrier loop can be totally neglected. At higher error rates, the loop will start to be degraded by the existence of bit errors.

Since the function of a "perfect integrator" second-order loop is to completely remove the average bias due to the doppler shift (this has been verified in the laboratory), we shall assume the phase error can be modeled at time t $(0 \leq t \leq T_b)$ in the following way

$$\phi(t) = \phi_L(t) + \phi_q(t) + \phi_d\left(\frac{t}{T_b} - \frac{1}{2}\right) \tag{27}$$

where $\phi_L(t)$ is the phase error from the linear equivalent model, $\phi_q(t)$ is the phase error due to quantization of the phase detector, and the last term is the phase error due to doppler. It is seen from the model that the average (time) phase error due to doppler is zero, although the change during a period is ϕ_d. We assume that $\phi_L(t)$ and $\phi_q(t)$ are zero mean random processes.

The time average, mean squared error is then, using (27),

$$\sigma_\phi^2 = \frac{1}{T_b}\int_0^{T_b} \overline{[\phi_L(t) + \phi_q(t)]^2}\, dt + \frac{\phi_d^2}{12} \tag{28}$$

At this point we make the additional assumption that the two errors, $\phi_L(t)$ and $\phi_q(t)$, are independent. Although this is not strictly accurate, it is certainly true in the case when the thermal noise is zero. Assuming independence, we approximate the quantization noise at arbitrary SNRs by the quantization noise when the thermal noise is zero.

The computation of the quantization noise then becomes simply a matter of computing the error state variance based on the relative occurrence of the error states of the system when no thermal noise is present. For the case $\Delta_1 = 4\Delta_2$, and assuming the initial value of the summer in the loop filter is zero, it can be shown that the loop error goes through the following four error values:

$$-\frac{1}{2}\Delta_2, \frac{9}{2}\Delta_2, \frac{1}{2}\Delta_2, -\frac{9}{2}\Delta_2, \cdots,$$

This sequence has a zero mean value. The rms quantization error is then easily computed to be $(41/4)^{1/2}\Delta_2$. For the case $\Delta_1 = 2\Delta_2$, using the same procedure, it is found that the rms phase error is $(13/4)^{1/2}\Delta_2$.

The total phase error variance for the two cases treated are given below (with Case I corresponding to the present design philosophy):

Case I, $\Delta_1 = 4\Delta_2$:

$$\sigma_\phi^2 = \frac{\alpha^2 \Delta_2 \pi^3}{4\rho\Delta_1} + \frac{\alpha\Delta_1\pi^{5/2}}{\sqrt{2\rho}} + \frac{41}{4}\Delta_2^2 + \frac{(\delta f_0 T_b)^2}{12}\,\mathrm{rad}^2 \qquad (29)$$

Case II, $\Delta_1 = 2\Delta_2$:

$$\sigma_\phi^2 = \frac{\pi^3\alpha^2 \Delta_2}{4\rho\Delta_1} + \frac{\alpha\Delta_1\pi^{5/2}}{\sqrt{2\rho}} + \frac{13}{4}\Delta_2^2 + \frac{(\delta f_0 T_b)^2}{12}\,\mathrm{rad}^2 \qquad (30)$$

Suppose we updated every βT_b seconds, for Case I, where β is a scalar factor. Then Eq. (29) would be modified to read

$$\sigma_\phi^2(\beta) = \frac{\alpha^2 \Delta_2 \pi^3}{4\beta\rho\Delta_1} + \frac{\alpha^2\Delta_2\pi^{3}}{\sqrt{2\beta\rho}} + \frac{41}{4}\Delta_2^2 + \frac{(\delta f_0 \beta T_b)^2}{12} \qquad (31)$$

The minimum value of $\sigma_\phi^2(\beta)$ (for design values of Δ_1, Δ_2, and ρ and for $\delta = 10^{-4}$) is achieved when $\beta = 1.25$. Since the minimum can be shown to be broad, the value of unity for β is essentially optimum at the present design values of $\Delta_1 = 1/80$, $\Delta_2 = 1/320$, and $\rho = 10$. In addition, updating every bit time is much simpler to instrument than updating every 1.25 bit times.

V. Comparison with Experimental Values

The loop was constructed using a commercial low-pass filter and a commercial A/D converter truncated to 4 bits; the remaining portion of the loop, which is all digital, was simulated by a computer. The simulation program was developed by Nate Burow of the JPL Telemetry and Command Development Group. The results for the timing error jitter are shown in Figs. 4 and 5, along with the theoretical curves from Eq. (29). Two values of Δ_1 and Δ_2 are presented for the case of no doppler and, in addition, the case when the relative doppler is 10^{-4}, which is the maximum expected. The ordinate is the total rms timing or phase error expressed in degrees, and the abscissa is the signal-to-noise ratio ST_b/N_0, where ST_b is the signal power times the bit time (bit energy) and N_0 is the one-sided noise spectral density.

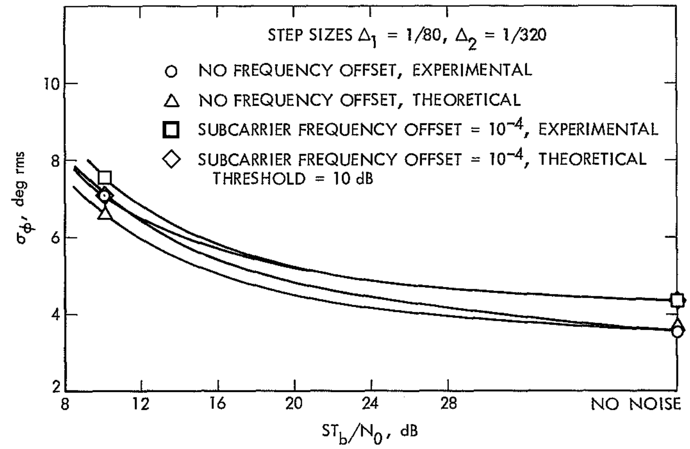

Fig. 4. Digital command system subcarrier tracking performance

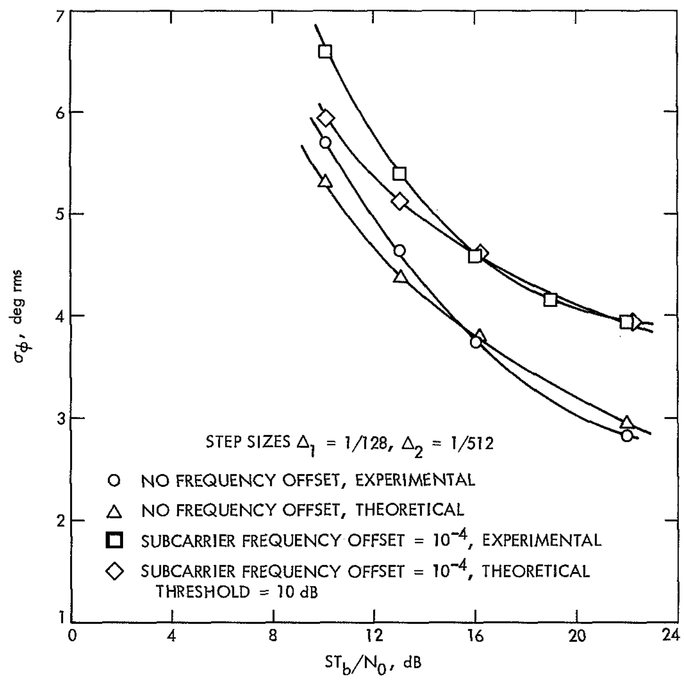

Fig. 5. Digital command system subcarrier tracking performance

It is seen in both figures that Eq. (29) is an accurate estimate of the actual loop performance. The error between the experimental and theoretical values at low SNR (10 dB) is due primarily to the phase error exceeding the linear range of the phase detector ($\Delta T_{sc}/2$). The theory was developed assuming the error never exceeded $\Delta T_{sc}/2$.

The bias was measured for the case when the doppler offset was 10^{-4} and was found to be no more than a few tenths of a degree for all SNRs of interest, so that the loop does in fact remove the bias due to doppler.

VI. Conclusions

An accurate theory for the performance of the second-order digital phase locked loop has been developed. The results have been verified by experimental measurements and shown to be accurate. In addition, the reason for going to a second-order filter, namely, the removal of the static phase error, has been justified, with only a small resulting increase in timing error variance. Furthermore, by decreasing Δ_1 and Δ_2 appropriately, the timing error variance can be reduced as small as desired.

It should be emphasized that the equations derived above will be substantially accurate as long as $\sigma_\phi > \max(\Delta_1, \Delta_2)$ and in addition σ_ϕ is less than the range of linear operation, that is, $2\sigma_\phi < \Delta T_{sc}/2$. The former condition ensures that the quantization error will not be the main source of timing error, and the latter condition ensures that the loop (with high probability) will not be outside the linear range.

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