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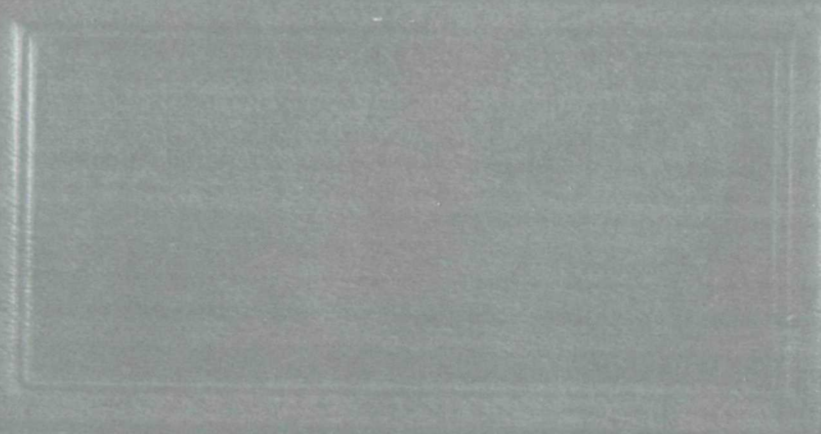


FINAL REPORT

DISCRETE INPUT EQUIPMENT DESIGN STUDY

Prepared for:

George C. Marshall Space Flight Center
Huntsville, Alabama

Contract No. NAS8-27801

Contract for Study and Design Concepts for a Discrete Input Equipment

Prepared by:

RCA
Electromagnetic and Aviation Systems Division
Van Nuys, California

January 1972

Summary

This study effort verified that a Discrete Input Equipment (DIE) could be built in accordance with all key items in the specification. No specified parameters were identified that could not be met.

The study raised some questions about the desirability of some specified parameters. The most significant of these is the scanning rate which seems to far exceed both extrapolations from Saturn experience and the capability of other equipment in the Saturn complex. Other items that should be re-examined by NASA include the specified concept of a concentrated system versus the possibility of a distributed system, the possibility of considering changes to existing data link and/or computer equipment in the existing complex, etc.

The effort on this study was performed during the period from July, 1971 through January, 1972 inclusive. With the exception of a kickoff meeting and two design reviews, all work was performed at RCA's Van Nuys facility.

Organization of Report

This report is written using the Second Design Review presentation as a vehicle. The charts used in this presentation are included in their entirety as Appendix A. In cases where the charts are not self explanatory, additional narrative is included in the body of the report.

Specification Interpretation (See A4)

The available funds and time changed dramatically from those available when the need for this study was first envisioned by MSFC. As a result of these changes, it was mutually decided to emphasize system concepts as opposed to attempting a detailed design of what would have to be limited areas of the DIE. Specifically excluded were detailed logic designs in any area and power supply design.

The specification problem referred to is that of the very high time resolution and data rates implied by the specified parameters. This problem is discussed elsewhere in this report.

Questions (See A5)

This chart elaborates on the specification problem referred to on A4. The specification requires that 3600 DI's must be scanned in a time between 0.5 and 2 milliseconds depending on the number of changes. The implications of this scan time and some of the questions it generates are discussed below.

One reason for specifying a high scan speed could be to provide good time resolution and to provide an early report on any detected activity. Since the spec does not require time tagging of activity reports, permits the scanning to stop temporarily if the data link can't keep up and since the scan period is allowed to vary by a factor of 4 as a function of activity, it seems that the goal is neither early reports nor high resolution time tagging.

Another reason for the high scan speed could be to support accurate reports during high discrete activity periods. The best data we could get on Saturn experience indicates that during peak discrete activity periods there are approximately 10 discrete changes per second. The specified DIE scan rates can handle activity as high as 1,800,000 (3600 ÷ .002) changes per second. It is improbable that this increase in activity will be realized.

Another aspect of this requirement that should be considered is the ability of the data link and computer to accept and process all of this information. A maximum discrete activity situation with the specified scan rate would generate data at the rate of 150,000 words per second. This figure becomes 300,000 words per second when special input activity is considered. This considerably exceeds the rate at which either the present or assumed data link can transmit words (5,555 and 222,222 words respectively). It also far exceeds the rate at which the computer can accept words.

We assume that the LCC computer must input the data, log it on tape, and process it for decision making, summary logging, summary printing, issuing of discrete outs, etc. At peak times, data input and logging only would bit 600,000 transfers per second (1,800,000 if information is handled as 8 bit bytes). When processing and other I/O is added to

this, it represents a challenging load for any computer.

Aircraft Integrated Data Systems (AIDS) (See A11 through A15)

This information was included as part of the design review to demonstrate a contrasting approach to a similar problem. In the particular AIDS approach shown, the signal conditioners and converters were distributed over the entire complex and interconnected with a party line. This approach as implemented traded off speed against cabling complexity, cabling weight, and a relatively large central system.

MTBF Considerations (See A17)

The MTBF of a simplex system that meets the specified probability of success of .995 for a 20 hour mission is 4,000 hours. The figures provided from the Saturn program are for reference. These figures show that the specified reliability performance is in the ballpark of that achieved for the Saturn DI's. Note that this is not a completely fair comparison for two reasons.

First, the DIE equipment includes more functions than the Saturn DI equipment. It handles more discretes at a higher rate, contains its own status memory, etc.

Second, the DIE replaces the entire 110A system except for the data link and the DCE equipments. Thus in the proposed new system only the DIE, Data Link and DCE contribute to mission failure probability whereas in the present system the entire 110A system contributes to mission failure probability.

The MTBF for a Simplex DIE was estimated at 3360 hours which is equivalent to a probability of 20 hour mission success of slightly over .994 compared to the specified value of .995. Since the MTBF calculation is based on several approximations, including the failure rate and a cursory logic count estimate, several values (ranging from 2500 to 4000 hours) are used for calculating the reliability of a TMR system in order to show a reliability range.

The MTBF of a TMR system varies as a function of time. A technique for evaluating mission success criteria of redundant systems is that of computing the probability of mission success for the redundant system and then determining what MTBF a simplex system would be required to have to achieve an equivalent success probability. These

results are listed under the TMR MTBF column.

For example, if a simplex equipment with an MTBF of 3,333 hours were built 3 times, synchronized, and the outputs voted, it would have the same probability of success for a 20 hour mission as a simplex equipment with an MTBF of 187,000 hours. The table below shows this same information using probability of failure as the dependent variable.

SIMPLEX MTBF	SIMPLEX FAILURE PROBABILITY	TMR FAILURE PROBABILITY	RATIO
4000	.005*	.0000744	67
3333	.006	.000107	56
2857	.007	.000145	48
2500	.008	.000189	42

*.005 is specified value.

Thus it is seen that the proposed system easily meets the specified probability of success.

The figures below the table on A17 were included to show the conservative nature of the numbers in the table. For example, the table assumes that the entire data link interface within the DIE can be made TMR. The data link, however, is simplex. Therefore at some point within the DIE the logic will become simplex. If we assume that the entire data link interface is simplex, the equivalent simplex DIE equipment with the same probability of success would have an MTBF of 35,000 hours. The equivalent failure probability is .000671 which far exceeds the specification.

The other two values at the bottom of A17 show that the specification is easily met even if the logic count grows by a factor of 2 and that the equipment as estimated will meet the reliability specification even if the individual integrated circuit λ increases by a factor of 7.

MTBF Qualifications (See A18)

This information is included to indicate some of the uncertainties in the reliability calculations. We believe that the results described on A17 are quite conservative and these qualifications describe some of the reasons.

The circuit MTBF figure was chosen on the basis of figures being used on some high reliability programs in process at RCA. Our experience

has shown that there is a great deal of uncertainty in available knowledge of integrated circuit failure rates. This uncertainty is very high in new technologies. General industry experience has been that the components in any given technology improve as use of that technology becomes more widespread. Experience has also been that each new technology that is reduced to practice exhibits improved reliability characteristics. The figures that we used on this study are believed to be true as of the present time. They should improve somewhat by the time a DIE is actually built. (The failure rates used assume that standard quality integrated circuits are used employing good parts control practices. We did not assume that special high reliability components would be used.)

The detailed circuit count was based on the block diagram (see A22). A cursory logic design was made for most blocks and used as a basis for a component count. Other blocks were counted by ratioing from similar blocks. All of this was done in a conservative fashion. For those blocks which have an analog in the existing Saturn equipment, the full circuit count from the existing design was translated to an integrated circuit count and used intact. This count is also very conservative since functional elements that won't be needed in the DIE were included in several cases. Also no attempt was made to optimize the existing designs for the new technology.

The reliability equation used to evaluate the TMR approach is pessimistic. It equates probability of success to the probability that either all three redundant channels are totally operational or that any two of the three channels are totally operational. In actuality the TMR equipment will continue to provide correct results in a large percentage of the multiple failure situations. Thus the calculated MTBF figure should be considered a lower bound of the actual value.

The reliability equation was applied pessimistically since the calculation assumed that voters were used only at the very output of the DIE. In reality the design uses voters at several points internally as well as at the output. In other words the expression $3R^2 - 2R^3$ was used to calculate the reliability whereas a less pessimistic expression would be of the form $\pi (3R_i^2 - 2R_i^3)$.

<u>DIE Communication with Data Link</u> (See A19 through A21)

As shown on A21, bilateral use will be made of both the data and

command channels of the data link. This makes it possible to use the existing format for DO commands. With the exception of the DO commands, all messages from the computer will be one word long. All messages to the computer will be two words long. Some details of the word format are discussed below.

A19 shows the word formats for information from the computer. The DO Address and Data will not change from the formats used now. They will not be discussed here. A description of the DI Command, Special Command, and Mask Setup formats follows.

Bit 23 is used to distinguish between Mask Setup and the other commands.

The Mask Setup command is used to control the 300 mask bits that are used in some DI modes. Bits 19 through 22 of the Mask Setup command specify 16 different sets of mask bits. Bits 0 through 18 of the Mask Setup command specify 19 actual mask bits.

Bit 22 of the DI Command and Special Command specify whether the command is for DI's or Special Inputs (SI's). Each of these command types has a different format. They are described separately below.

DI Command

Bit 21 specifies whether the mode should be Monitor or Scan.
Bit 20 specifies whether all DI's within the specified blocks should be processed or whether only those DI's with their associated mask bit set should be processed.
Bits 10 through 19 are used to specify which of the 19 blocks of 16 DI words each should be processed. (Note that the last block contains only 12 DI words.) As shown in the figure, the program would specify the first block to be used and how many consecutive blocks following should be used.
Bit 2, DL Control Word, should be marked "unused".
Bits 0 and 1 are used to control termination. As indicated one of these causes immediate termination, the other causes termination at the end of the current scan cycle. If the specified mode is Scan and the terminate bits are not set, at the end of one scan the mode will change to Monitor.

SI Command

Bits 20 and 21 specify which mode should be generated.
Bit 19 specifies whether the interrupt flag should be set in activity reports which follow. It should be noted that SI activity reports use the data link command channel and therefore each

activity report generates two computer interrupts independent of this bit. It is possible that this bit could be used to generate a special kind of interrupt. It is also possible that this bit could be used to establish priority by virtue of software interpretation.

Bit 18 is used to define whether the command applies only to the SI group defined by the group number or whether it applies to all specials.

Bits 6 through 14 specify the group. Since there are only 16 SI groups, 4 bits could be used. However, nine bits are used so that addresses for the SI's, DI's and any words used for control purposes can be made unique.

Bits 0 through 2 are the same as for DI Commands. In the case of the SI's there is little, if any, significance to the difference between Terminate Now and Terminate at End of Scan.

A20 shows the word formats for information sent to the computer. All information is sent to the computer in pairs of words. Each pair includes one ID Word and one Value Word. The Value Word contains up to 24 bits of data and in general will convey the value of one DI group or one SI group. The Value Word will also convey information such as feedback of commands, status, disagreement detector state, etc.

The ID word contains several "unused" bits. These may be used to provide message sequence numbers. Current thinking is that time information will not be included with each report. Instead a 24 bit time message will be generated at the end of each scan in which any activity occurs.

Bits 20 and 21 in the ID word define the mode in which the DIE is operating if the report is for DI or SI activity.

Bit 19 contains the Interrupt Flag if the report is for SI activity. (See the discussion under Bit 19 of the SI Command.)

Bit 18 contains the Mask Bit for the group in a DI report.

Bit 17 indicates whether a parity bit is associated with the group for an SI report.

Bit 16 indicates good or bad parity and should not be interpreted unless bit 17 indicates that a parity bit is present.

Bit 15 is used to flag a word if the data link requests a repeat transmission.

Bits 6 through 14 provide the actual identification of the nature of the report. Nine bits as shown provide 512 combinations. Three hundred are used to identify DI groups and 16 are used to identify SI groups. The remaining 196 combinations are available for other purposes. A number would be used for disagreement detector reports, some for identification of command reports that are fed back for verification, etc.

Bit 5 is used to report the state of a test bit. This will be discussed in some detail in the material under A26 and A27.

DIE Block Diagram (See A22)

As indicated above in the reliability discussion, the reliability requirement does not present a serious problem. Most probably a careful simplex design could meet it. The fault tolerant requirements imposed by the specification, however, do require a redundant system independent of the reliability performance.

Before we realized the ease with which the reliability requirement could be met, a brief literature survey was made in an attempt to locate optimal redundancy approaches. Nothing more attractive than classic TMR was located for this application.

One channel of the block diagram is shown on A22. The circles on the block diagram indicate the location of voting points. A number, n, beside a circle indicates the number of voter points symbolized by the circle. Each voter point is made up of 3 voters and 9 disagreement detectors. Each voter may be considered to be a part of 1 TMR channel in that, although it receives an input from each of the 3 channels, its output drives only one channel. Three of the nine disagreement detectors are associated with each voter so that the voter output can be compared with each input. This makes it possible to easily identify a failed channel or a failed voter.

The dashed lines on the block diagram represent the proposed implementation of timing. One of the difficult problems to resolve in any redundant design is generation of central timing in such a fashion that it is fault tolerant. Because it is necessary to vote logic signals at various points in the system it is necessary to synchronize the different channels. Thus, if multiple clocks are used, they must be synchronized. There are serious questions about

the desirability of synchronizing oscillators for this purpose. It was decided that we would resolve this problem in the proposed DIE organization by providing three switchable timing systems such that in normal operation of the system each would drive a different section of the hardware. These sections have been named SI Timing, DI Timing, and Common Timing as indicated by dashed lines and titles on A22.

The switching for the timing systems is manually controlled such that timing can be distributed to the entire DIE as long as at least one timing system is still operational. The different timing sections of the DIE were chosen in such a fashion that failure of one of the timing systems would be easily detected. For example, if one of the DI's and one of the SI's were made to cycle at a low but known rate, the failure of DI Timing or SI Timing would be detected very early and the timing systems could be switched.

The general operation of the block diagram is fairly self evident. Only certain fairly unique aspects of it will be discussed here. These aspects are DI5's, status and selection of voter points.

The term DI5's represents a block of special-design LSI circuits. Each of these circuits can interface with 25 external signals such as DI's, SI's or DIE internal status signals. In the case of SI's and DI's, 24 of these signals would be one actual group; the 25th bit is for test purposes. There will be 150 or 300 of these circuits in the DI portion of the DIE. There will be 16 of these circuits in the SI section of the equipment. The operation of this circuit is described in more detail below. (See A26 and A27)

The Status section of the equipment is identical in organization to the DI and SI section. Its purpose is to make status information available to the LCC. Complete details of what this status will include must be worked out as a portion of the final design. Examples of the type of status that will be provided are operating modes, current timing system switching arrangement, disagreement detector values, etc.

Three criteria should be used for selection of voter locations. These are maximization of probability of mission success, resolution of "race-like" conditions that might otherwise occur in normal operation, and maximizing the utility of the associated

disagreement detectors for fault isolation. (These items are not necessarily listed in order of importance.)

It is believed impractical to do a good gob of voter location for fault isolation purposes until the design is much further along. Therefore, fault isolation by use of this technique has not yet been incorporated in the block diagram.

For purposes of maximizing success probability it is desirable to divide the system into equal sections from a failure rate perspective. For the DIE, the simplex failure rate is in the range of 250 to 300 failures per million hours. The contribution of the DI5's in the DI section of the system is 150 failures per million hours which is close to optimal from a probability of success viewpoint. Symmetry would lead to the placing of voters at equivalent points in the SI and Status sections; however, there is an even better reason which is described immediately below.

Since the DI5 circuit by definition of its application interfaces with at least two sets of asynchronous signals, there will be cases where the redundant circuits will legitimately interpret the same signal differently at a given instant of time. The reasons for this are differences in wiring capacity, thresholds, etc. By voting at the the DI5 circuit output disagreements of this kind will not propogate into other sections of the DIE.

<u>Voter Quantity Considerations</u> (See A23 and A24)

At first glance the proposed DIE organization appears to use relatively few voters. It is probable that for reasons of enhanced fault isolation capabilities some voters would be added at appropriate points in the equipment. On the other hand there are reasons against adding voters. One reason is that the 9 disagreement detector status bits would have to be monitored both as status bits and as indicators. (In some cases there is a desire to have several kinds of disagreement detector report from a particular voter point.) Another reason for not adding voters is the need for complete testing of the system before each mission. The addition of each voter point adds to the complexity and execution time of this testing. Further, the point can be reached where the failure rate of the voter can actually detract from the reliability of the system.

A24 shows a comparison of the voter quantity in the existing DCE equipment and in the proposed DIE (the DCE numbers are approximate). The large voter count for the DCE is due to the parallel nature of much of the processing. One of these paths is over 2000 bits wide, several are 24 bits wide. On the other hand the DIE is predominantly serial. When this difference is taken into account the comparison is quite close.

Buffer Size Considerations (See A25)

As discussed earlier in this report, the data rates that can be generated by the DIE exceed the capacity of the balance of the system. The choice of a buffer size must be based on some assumptions about the characteristics of peak data rate periods. This chart shows some numbers as a function of 3 possible different limiting system elements and assumed peak data rate (300,000 wps) periods of 4 and 8 milliseconds. A25 assumes that no command word feedback or status word transmission takes place during peak transmission periods.

DI5 Chip Design (See A26 and A27)

These sheets show the organization of the LSI chip design upon which the proposed DIE is based. The chip would be packaged in a 40 pin package and could be built using any one of a number of technologies. A specific choice should not be made until the build date is determined in order to retain flexibility.

Sheet A26 shows some of the address gating and control. The FR GATE signal is used on A27 to sample the input signals each time that the ADDRESS IN line is true and either SCAN + UNMASKED MODE or the MASK flip flop is set.

The ADDRESS SHIFT pulse shifts the ADDRESS IN bit into a flip flop which generates ADDRESS OUT and also permits SHIFT pulses to recirculate the registers on A27. The same flip flop enables the output of the SELECTED GROUP signal which is a function of the MASK flip flop.

The MASK flip flop is controlled by the MASK IN and SAMPLE IN signals which are decoded from the Setup Mask command word.

The two registers on A27 are used to hold current and history values for the input data. The 25 "exclusive or" gates compare this information and at the appropriate time the result of this comparison is set into the CHANGE OUT flip flop. When the REG SHIFT pulses are generated, the first rank register which contains current data is shifted off the chip where it is voted with the similar outputs of two identical chips wired to the same input signals. The resultant information is transmitted to the data link and recirculated back into both the first and second rank registers on the chip under discussion.

The chip logic will be made 25 bits wide instead of the required 24 in order to facilitate various test operations. Stimulation of the 25th bit by external equipment or by special internal test circuits automatically or under program control can be used to test large portions of the DIE. The state of this bit is reported in bit 5 of the ID Word (See A20).

Test Phases (See A28)

This sheet identifies the various test phases that a development of the new DIE capability will require. Probably the most significant thing to be noted is that DIE testing is most efficiently performed at the vendor plant and will require either significant portions of the present ground computer system in close proximity or will require a significant investment in simulation equipment.

The phrase "add PB's" under "Pre Mission Validation" refers to the admissibility of adding printed circuit boards for test purposes.

Test (See A29)

Any project to build a DIE should consider use of external equipment to facilitate test. A good example of this is the signal conditioner equipment. The existing equipment has limited, manually controlled ability to control the inputs to the DIE. With the growth in quantity of DI's and availability of improved miniaturization of circuitry, serious consideration should be given toward including the signal conditioners in the programmable system test.

Control Panel Concepts (See A30 and A31)

The control panel cannot be intelligently designed until further system details are developed. However, an attempt was made to identify some functions that should be considered for the control panel. Most of the items listed on A30 are self explanatory and easily accomplished. The first few are not so obvious and are shown in somewhat more detail on A31.

The top section of A31, Dynamic DD/Word Display, may be used to monitor the overall operation of the DIE. The lights (L) are driven from points near the actual data link interface such that the display will operate only if the system is essentially operational. The switch(es) are used to control the operating mode of this section of the panel. IN/OUT determines whether the panel should display data flowing to or from the data link. DO/OTHER determines which data link channel should be monitored when data coming from the data link is being displayed. ANY/PARTICULAR determines whether every message should be displayed or whether only information with a particular group number should be displayed. In the latter case, the digiswitches (DS) are used to select the desired group number.

The matrix of 180 lights will display the disagreement detectors during normal operation. The top 3 rows display the disagreement detectors corresponding to the detectors in the DI and SI section of the equipment. Since the actual group number for which the disagreement occurred will be of interest, the 9 lights labelled GROUP NO./WORD DISP will display the appropriate group number. The 3 unlabeled indicators identify which of the top three rows of the light matrix was updated last and corresponds to the GROUP NO./ WORD DISP.

In other modes of operation, 6 lights of the GROUP NO./WORD DISP in conjunction with the 18 lights in the top row of the large matrix display a full 24 bit word. The WORD DISP in conjunction with the second row of the large matrix portrays a second 24 bit word.

The central section of the panel depicted on A31 is labelled DI5 SIMULATOR/DL COMMAND INSERTION. In the DI5 simulator mode these

switches can be used to insert manually originated data into the system as if the data originated via a DI5. The BLOCK SELECT switches make it possible to select which block the DI5 simulator should work with. In the command insertion mode, any command can be manually generated such that the DIE will treat it as if it were received from the data link.

The bottom portion of A31, labelled VOTER/DD TESTING, consists of 3 position switches that are used to control logic circuits of the form shown on A32. The concept is that circuits of this type would be packaged on special test boards. The DIE would be wired such that each channel segment would provide for insertion of this circuit at its output to a voter point. Approximately 19 of these circuits could be packaged on one plug in. (Test plug ins of this nature would be replaced by boards with printed jumpers during normal operation.)

When the test circuits are in place, the switches indicated on A31 could be used to force any combination of 1's and 0's to the voter inputs. Through the use of various combinations of these switches the operability of every channel segment, every voter, and every disagreement detector can be verified. When the test is completed the jumper boards will be reinserted. The integrity of the jumper boards can be verified by inspection of the disagreement detector lights after reinserting the jumper boards.

Packaging (See A33 and A34)

Per mutual agreement very little effort was spent in studying packaging. Sheets A33 and A34 show views of a packaging technique now being used for RCA supplied electronic equipment for use on naval destroyers. This package meets or exceeds all specified environmental parameters.

The electronics needed for DIE can be housed in one of these bays for 3600 DI's and in 1½ of these bays for 7200 DI's. There appear to be several ways in which the "guts" of this package can be mounted inside the specified NASA console and meet all requirements. A brief description of the currently favored approach follows:

Each console would contain two sliding frames. Each frame would house two racks. One of these racks can swing out when the sliding frame is in the extended position. Access to the nest wiring would be available in this fashion. (A33 shows the cabinet with the wiring

in two racks exposed.)

The favored approach would differ from that pictured in that the sliding frames and their racks would be shortened in depth such that they would occupy only the front half of the console in their normal position. This would leave the entire back half of the console for dealing with the control panel and the large quantity of interface connectors needed for this application. The control panel would be a swing out panel near the top of the console. A vertical panel with sloping surfaces would be mounted about half way back in the console. All external cable connectors would be plugged into this panel. Ribbon cables as shown on A34 would interconnect between this connector interface panel and the racks in the sliding frames.

The complete DIE would be housed in two or three consoles as described above depending on the number of DI's handled by the system. One of these two or three consoles would have a control panel in the rear. The other console(s) would have a blank panel in the rear.

In the normal secured operating position the rear of each console would be closed with swinging panels. The control panel would be mounted on one of these panels in one of the consoles.

Recommendations (See A35 and A36)

The important recommendations fall into two categories. One of these is that more effort should be exerted to take maximal advantage of "know how" that has been developed to date on the Saturn project. As many aspects as practical should be considered. Many of these are mentioned on A35 and A36.

The second recommendation involves the desire to make maximal use of advanced technology. Advances are being made so quickly that it would be desirable to reduce the DIE to practice via a multiphase project, scheduled in advance so that full advantage can be taken of then current capabilities.

APPENDIX A

SECOND DESIGN REVIEW
FOR
DISCRETE INPUT EQUIPMENT DESIGN STUDY

Prepared for:

George C. Marshall Space Flight Center
Huntsville, Alabama

Contract No. NAS8-27801

Contract for Study and Design Concepts
for a Discrete Input Equipment

Prepared by:

RCA
Electromagnetic and Aviation Systems Division
Van Nuys, California

PURPOSES OF STUDY

Propose an approach to a Discrete Input Equipment (DIE) that improves reliability of LUT system by:

- Significantly reducing the SGCS LUT equipment complement
- Using higher reliability technology that is becoming available
- Utilizing a fault tolerant organization
- Improving test and self test features

Increases discrete monitoring capability by:

- Increasing the number of discretes that can be monitored
- Reducing the time for a complete scan of all DI's
- Making the time characteristics of DI monitoring independent of computer loading

DESCRIPTION OF CONTRACT

Six month study with funds for about seven man-months

Two design reviews and a final report

SPECIFICATION INTERPRETATION

Emphasize system operation and organization - de-emphasize routine detail

Don't belabor interface details: DL, IODC, DO

Outline power supply requirements as opposed to schematic level effort

Resolve specification problem by:

- Supplying time information with each activity report
- Ignoring other facets of problem
- Assuming availability of high speed DL

QUESTIONS

Spec emphasizes fast scan time which could have goals of:

Good time resolution
But spec doesn't mention time reporting and allows DIE to slow down if DL can't keep up

Handling high activity
But data we have seen shows very low activity

Unnecessary high data acquisition rate with slow DL may lead to large buffer - desired high rel should dictate minimal hardware

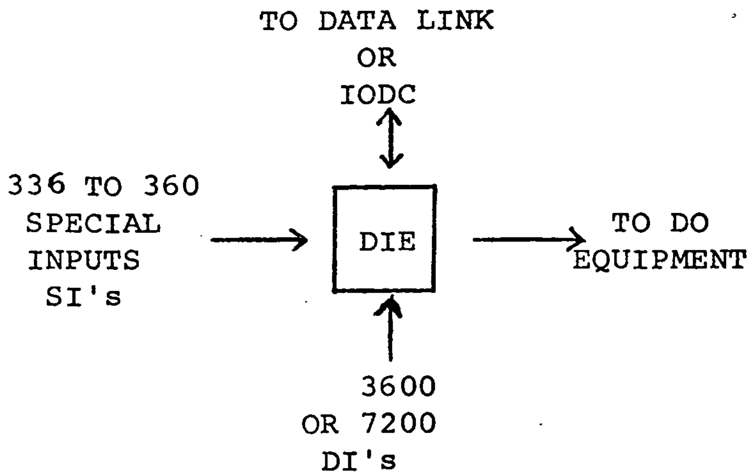
DIE can generate words at rate of 250,000 (300,000) WPS

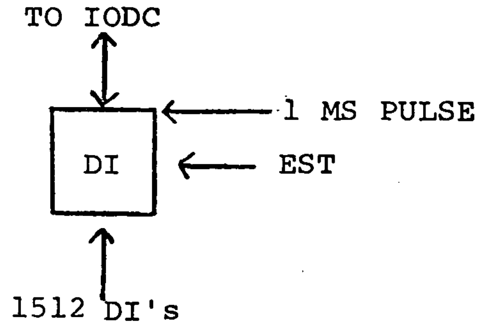
DL can accept words at rate of 5,555 WPS

DL (NASA suggested 10 MC) can accept words at rate of 222,222 WPS

IODC can accept words at
Top max. rate of 69,400 WPS
Practical rate of about 18,000 WPS

MAJOR DIE FUNCTIONS VS PRESENT DI





DIE, DL and DCE can replace SGCS equipment in LUT

Complete DI scan in .5 to 2 MS

Complete SI SCAN in .075(.08) to .3(.32) MS

Variation in scan time due to DI or SI activity

Fault tolerant

Must be close to computer

Complete DI scan in 1.2 to 3.5 to 4.8 to 14 MS

Doesn't handle specials

Variationin scan time due to DI activity, IODC activity, and computer activity

MODES

DI's

- All groups in same mode
- Scan
  - Terminates or changes to Monitor after one cycle
- Monitor
  - Masked
  - Unmasked
  - Terminates upon command

SI's

- Independent mode for each group
- Send report
  - When requested
  - When READY (once for each ready)
    - Optional interrupt submode
  - When READY and CHANGE
    - Optional interrupt submode
- Terminates upon command
- Parity - Patchable check

PACKAGING

DIE to handle 3600 DI's to be packaged in no more than 2 consoles.

Additional 3600 DI's will require a third console.

RELIABILITY

DIE reliability shall be sufficient to generate a probability of success of .995 for 20 hours.

DIE is expected to be fault tolerant.

SELF TEST

Failure Detection Lines

To communicate power failure, DL failure, and critical DIE failures.

Disagreement Detectors

Built in Self Test controllable through data link. Goal is to check all failure modes and determine replacement to the replaceable unit level. Self Test circuits must be eliminated as source of system failure during normal operation.

AIRCRAFT INTEGRATED DATA SYSTEM (AIDS)

Gathers data on aircraft systems via use of remote sensors interconnected with party line (data bus).

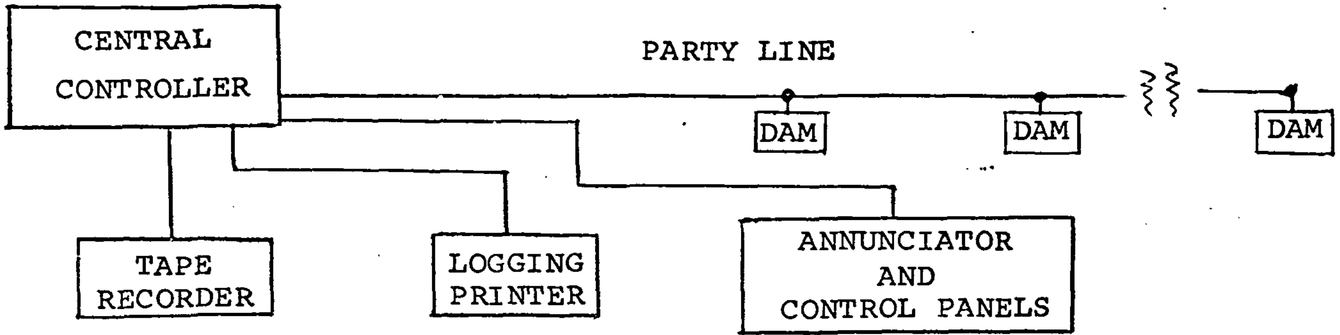
MAJOR SYSTEM ELEMENTS

- Central Controller
- Tape Unit, Printer, Annunciator, Control Panel
- Party Line
- Data Acquisition Modules (DAM's)

IMPROVES MAINTENANCE ECONOMY BY:

- Detection of failure trends
- Early detection of failures
- Fault isolation
- Permitting overhaul when needed as opposed to by schedule

AIDS BLOCK DIAGRAM



PARTY LINE OPERATION

PARTY LINE (EXPERIMENTAL) uses 7 wires

- 3 for voltages and ground
- 2 for reference voltage and return
- 2 for data and clock

COMMUNICATION SEQUENCE

<u>Addressing</u>

14 bits used for address
(every legal address contains 7 ones)

1 bit defines test or take reading

1 spare

<u>Address Verification</u>

Selected DAM returns its address to central control.

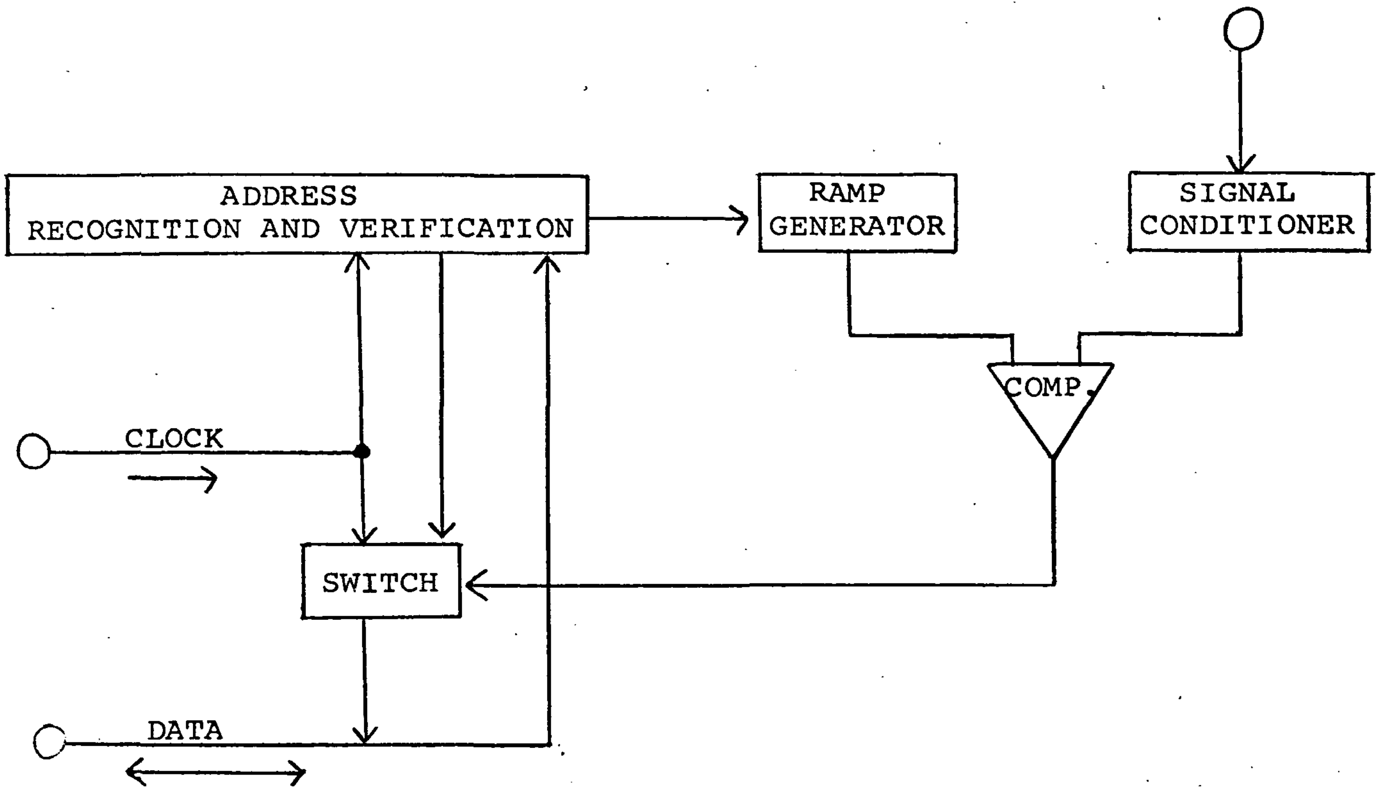
<u>Quantizing Period</u>

Central control distributes carrier on clock line.
Selected DAM returns carrier on data line for time duration proportional to data value.
Checks include reference value, minimum, and maximum normal measurements.

<u>Reset Period</u>

No signal on clock line generates DAM reset.

DAM BLOCK DIAGRAM



AIDS VARIATIONS

Sophistication of central controller logic and programs

Complement of input/output devices

Speed vs wire count tradeoffs in party line

Type of signal conditioning provided in DAMS

Availability of DAM clusters as well as stand alone DAMS

ORGANIZATION OF STUDY

Develop understanding of functional requirements.

Cursory design of nonredundant DIE approach.

Review redundancy approach.

Incorporate tentative redundancy selection into cursory design.

Compare MTBF characteristics of Saturn DI's, nonredundant DIE approach, and redundant approach.

Conduct survey of available circuit technologies.

Incorporate self test features.

Study packaging.

Prepare final report.

MTBF CONSIDERATIONS

Goal (success probability of .995 for 20 hours)			4000 hours
Saturn DI's (per May 1970 report)			
	Goal	5000	
	Prediction	2950	
	Present Status		6740
	Without screening	1910	
Simplex DIE			3360

TMR DIE

Simplex MTBF	TMR MTBF
4000	269,000
3333	187,000
2857	137,000
2500	105,000

TMR DIE (assumes entire DL interface is non-redundant)

3360	35,000

TMR DIE (assumes logic count grows by factor of 2)

2500	105,000

TMR DIE (assumes λ is low by factor of 7)

471	4,000

MTBF QUALIFICATIONS

Determination of circuit MTBF's

Detailed circuit counts

Pessimistic redundancy formula

Pessimistic application of formula

WORD FORMATS TO DIE

BIT	COMMAND DI	COMMAND SPECIAL	SETUP MASK	DO ADDRESS	DO DATA
23	← COMMAND/SETUP →				
22	← DI/SPECIAL →		MASK		
21	MONITOR/SCAN	SEND ONCE SEND WHEN READY	SEGMENT		
20	ALL/MASK	SEND IF CHANGE	(0 TO 15)		
19	STARTING	SET INTERRUPT FLAG		SAME	SAME
18	BLOCK	COMMAND APPLIES TO ALL SPECIALS			
17				FORMAT	FORMAT
16		UNUSED			
15				NOW	NOW
14	NUMBER		MASK		
13	OF	GROUP	BITS	BEING	BEING
12	BLOCKS	NUMBER			
11				USED	USED
10					
9					
8					
7					
6	UNUSED				
5					
4		UNUSED			
3					
2	← DL CONTROL WORD →				
1	← TERMINATE NOW →				
0	← TERMINATE AT END OF SCAN →				

WORD FORMATS
FROM DIE

BIT	ID WORD	VALUE
23	UNUSED	
22		
21	MODE	
20		
19	INTERRUPT FLAG	
18	SELECTED GROUP	
17	PARITY PRESENT	
16	PARITY BAD	
15	REPEAT XMISSION	
14	GROUP NO.	
13		
12		
11		
10		
9		
8		
7		
6		
5	TEST BIT	
4	UNUSED	
3		
2		
1		
0		

UTILIZATION OF DATA LINK CHANNELS

	FROM COMPUTER	TO COMPUTER
COMMAND CHANNEL	DI & SPECIAL COMMANDS MASK SETUP TEST COMMANDS	SPECIAL REPORTS TIME DO FEEDBACK COMMAND & MASK SETUP FEEDBACK
DATA CHANNEL	DO COMMANDS	DI REPORTS TIME

DIE BLOCK DIAGRAM (ONE TMR CHANNEL)

VOTER QUANTITY CONSIDERATIONS

REASONS FOR DESIRING MORE VOTERS:

1. ESTHETICS
2. INCREASED FAULT TOLERANCE
3. INCREASED FAULT ISOLATION CAPABILITIES

REASONS FOR NOT DESIRING MORE VOTERS:

1. NOT NEEDED TO MEET RELIABILITY AND FAULT TOLERANCE REQUIREMENTS
2. INCREASES TESTING COMPLEXITY
3. INCREASES STATUS REPORTING COMPLEXITY

NUMERIC CONSIDERATIONS:

VOTER IMPROVES RELIABILITY ONLY WHEN IT'S MONITORING LOGIC CONSISTING OF MORE THAN 18 BUGS.

DCE VS DIE VOTER COUNT COMPARISON

DCE		
TOTAL VOTER COUNT (APPROXIMATE)	2,276	
PARALLEL VOTERS SERIALIZED	11	
UNIQUE VOTERS	20	
EFFECTIVE EQUIVALENT		31
DIE		
TOTAL VOTER COUNT		57

BUFFER SIZE CONSIDERATIONS

DIE can generate words at rate of 300,000 WPS (exclusive of status)

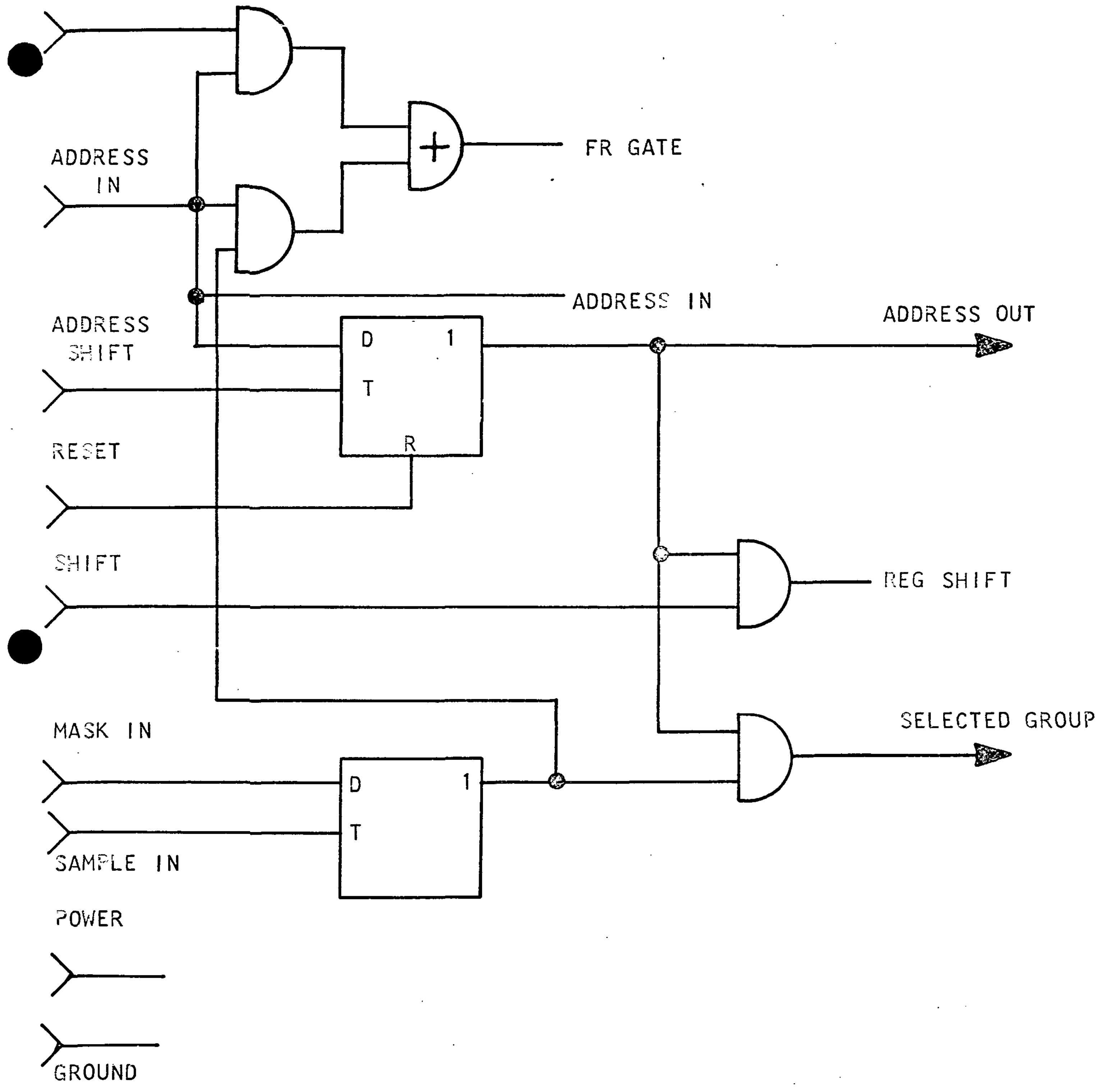
Current DL (CDL) can accept words at rate of 5,555 WPS

10 MC DL (PDL) can accept words at rate of 222,222 WPS

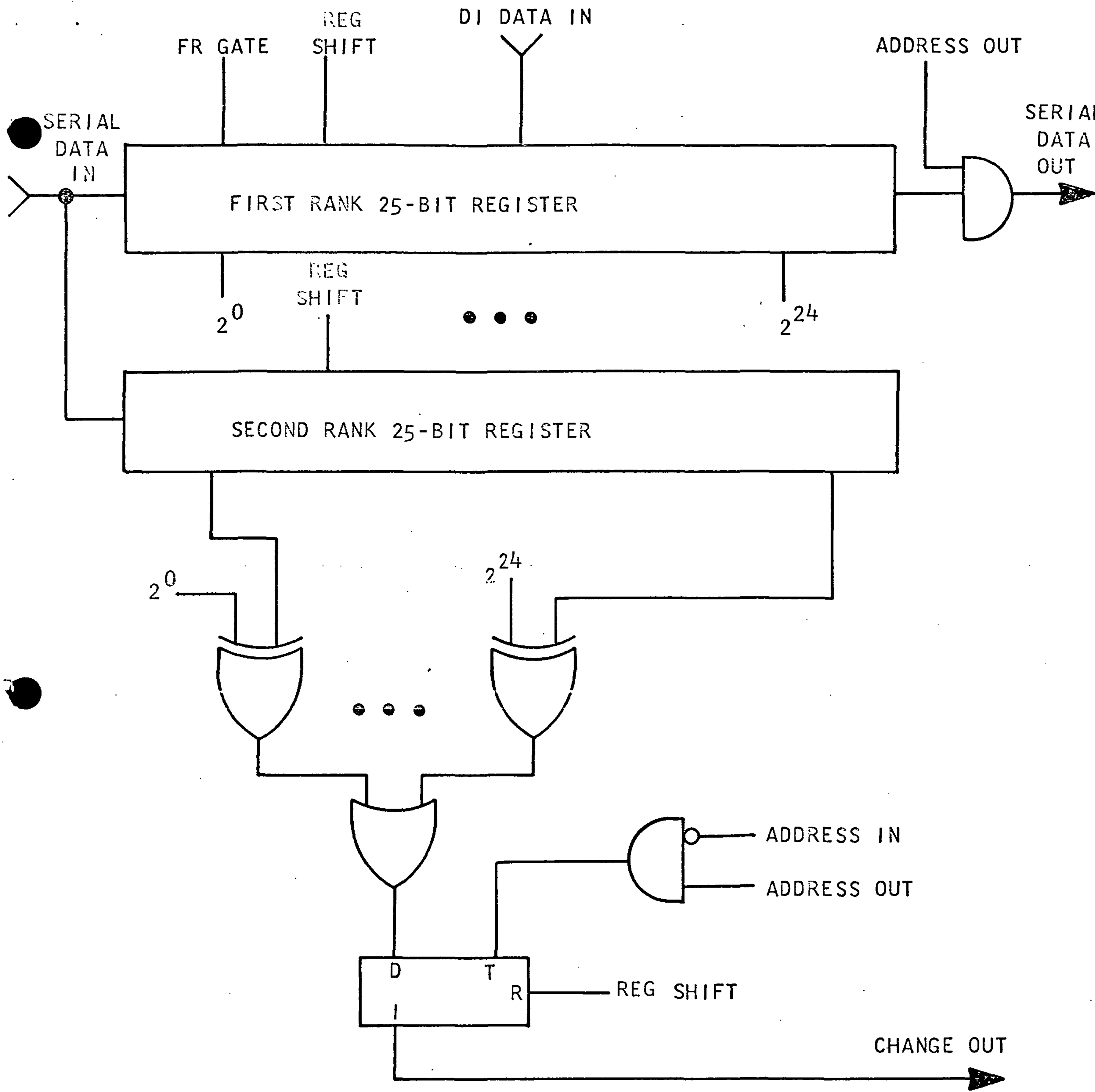
Computer can accept words at rate of about 18,000 WPS

BUFFER SIZE AS FUNCTION OF PEAK DATA RATE PERIOD AND CONFIGURATION

	1 SECOND	4 ms	8 ms
CDL	294,445	1,178	2,356
PDL	77,778	311	622
COMP	282,000	1,128	2,256



D15 CHIP


FR GATE
REG SHIFT
DI DATA IN
ADDRESS OUT
SERIAL DATA IN
SERIAL DATA OUT
FIRST RANK 25-BIT REGISTER
2^0
REG SHIFT
2^{24}
SECOND RANK 25-BIT REGISTER
2^0
2^{24}
ADDRESS IN
ADDRESS OUT
D
T
R
REG SHIFT
I
CHANGE OUT

TEST PHASES

INITIAL VALIDATION OF FIRST SYSTEMS (INCLUDING EXPANSION)

- ENVIRONMENTAL
- RELIABILITY
- DESIGN CONCEPT (REQUIRES 110A, DL, DCE, SI's, DI's)
- WIRING (REQUIRES 110A, DL, DCE, SI's, DI's)
- CIRCUITS (REQUIRES 110A, DL, DCE, SI's, DI's)

INITIAL VALIDATION OF SUBSEQUENT SYSTEMS (INCLUDING EXPANSION)

- WIRING (REQUIRES 110A, DL, DCE, SI's, DI's)
- CIRCUITS (REQUIRES 110A, DL, DCE, SI's DI's)

PRE MISSION VALIDATION

- AUTOMATIC
- PROGRAMMED
- SPECIAL TEST CONFIGURATIONS ALLOWABLE
  - ADD PB's
  - LOOP TESTS
- MANUAL OPERATIONS ALLOWABLE

VALIDATION DURING MISSION

- AUTOMATIC
- PROGRAMMED

TEST

OPERATIONAL
- AUTOMATIC
- PROGRAMMED
- MANUAL

NON-OPERATIONAL (CAN BE RECONFIGURED)
- AUTOMATIC
- PROGRAMMED
- MANUAL

USE OF EXTERNAL EQUIPMENT
- PROGRAMMABLE SIGNAL CONDITIONERS
- SIMULATOR
- MODULE TESTER

CONTROL PANEL CONCEPTS

DISAGREEMENT DETECTOR DISPLAYS

Dynamic, latching, one shot

DYNAMIC WORD DISPLAY

DI5 SIMULATOR

DATA LINK COMMAND INSERTION

VOTER, DISAGREEMENT DETECTOR, AND INDIVIDUAL CHANNEL TESTING

POWER CONTROL

POWER SUPPLY MONITORS

SINGLE STEP CONTROLS

NORMAL/TEST MODE

ON LINE/OFF LINE CONTROL

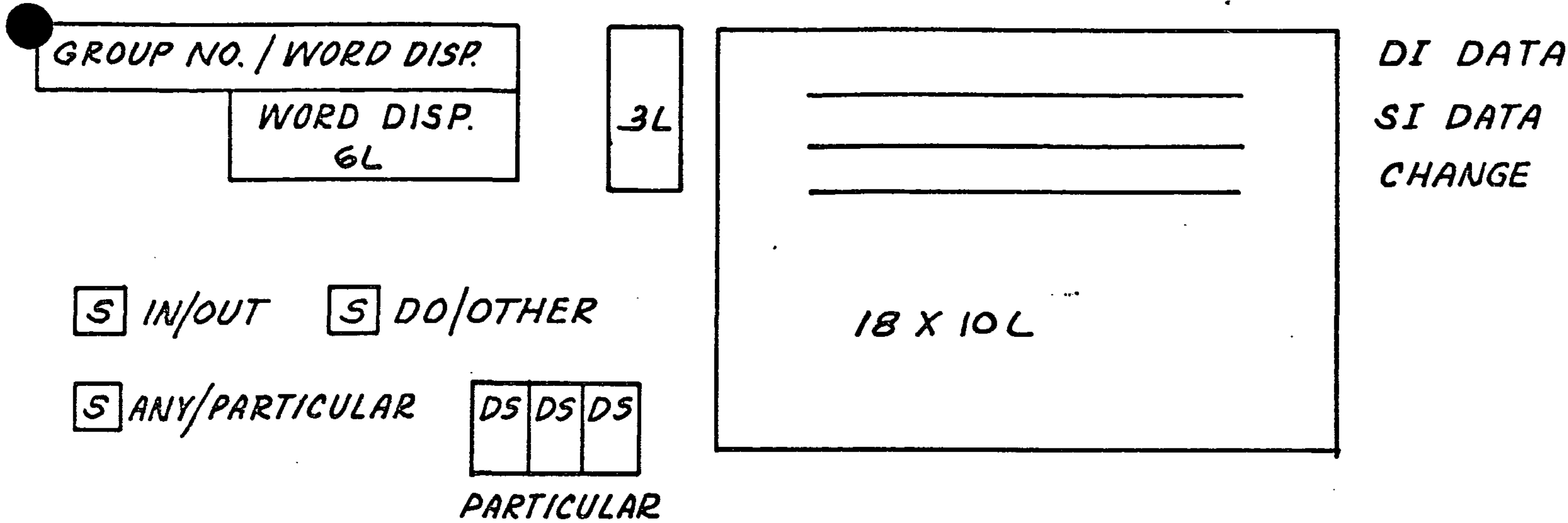
RESET

MODE INDICATORS

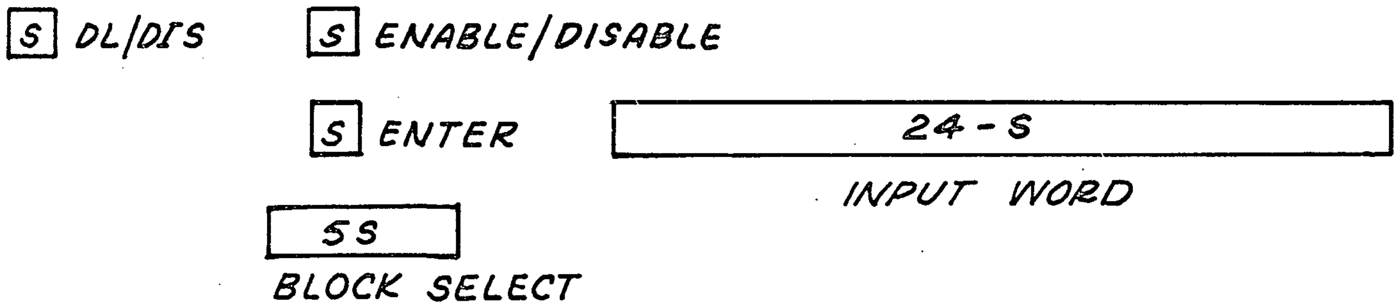
CONTROL STATE INDICATORS

ELAPSED TIME METER AND CIRCUIT BREAKERS

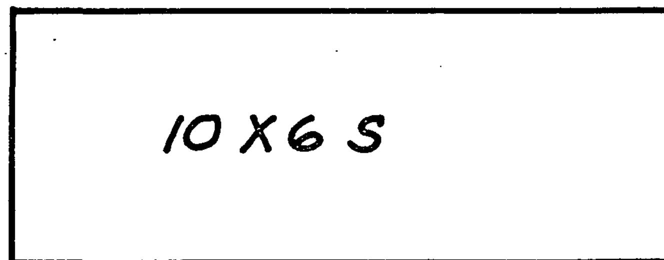
CONTROL PANEL CONCEPTS



DYNAMIC DD / WORD DISPLAY

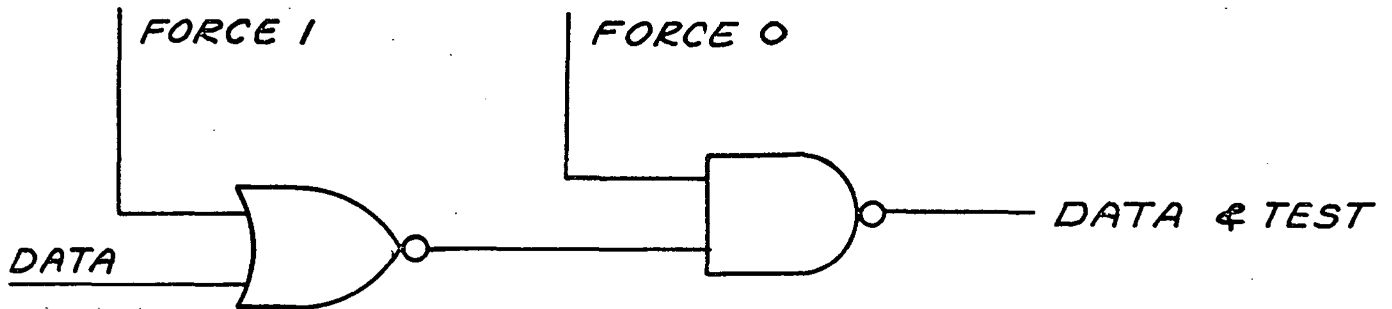


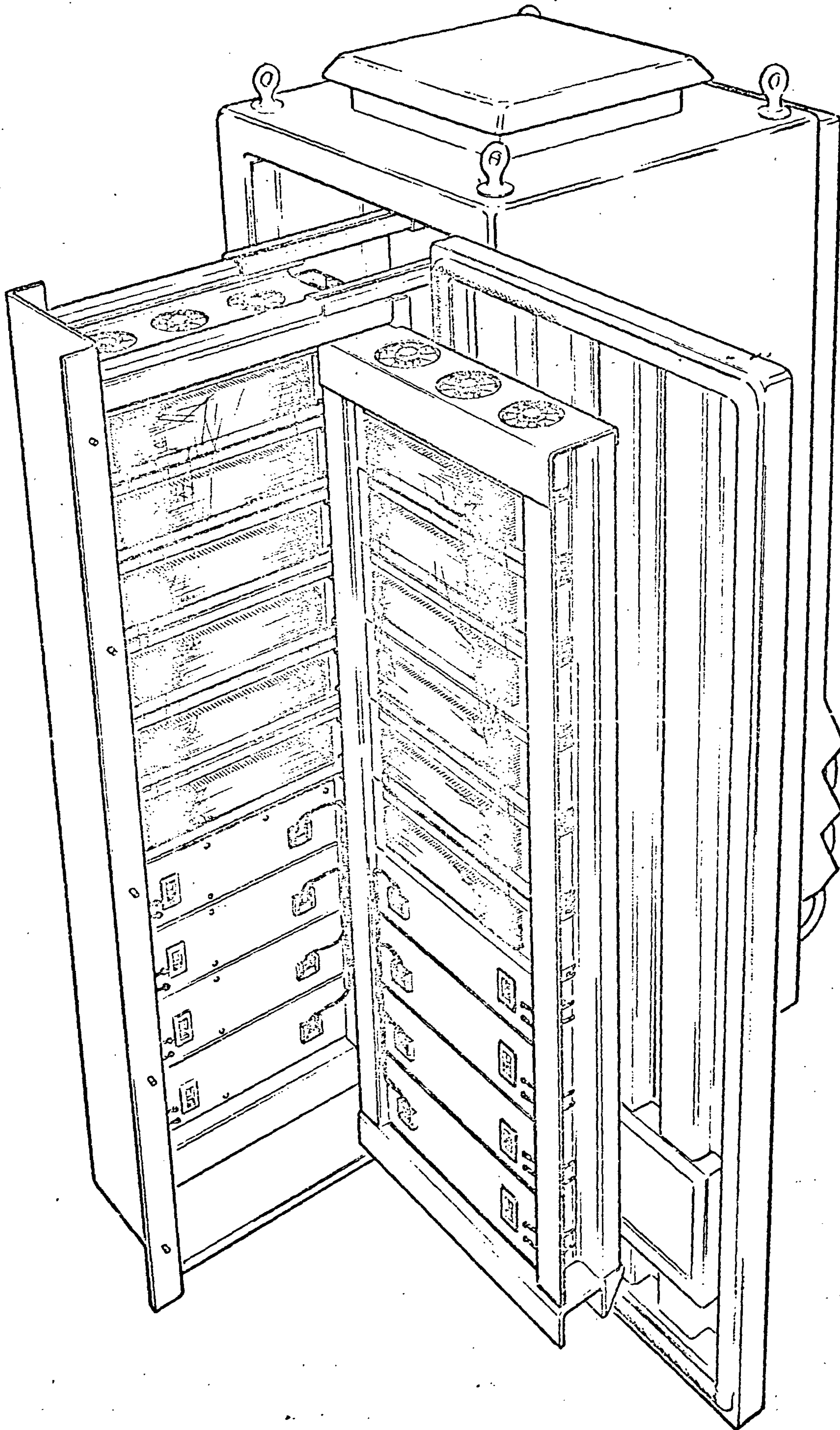
DIS SIMULATOR / DL COMMAND INSERTION

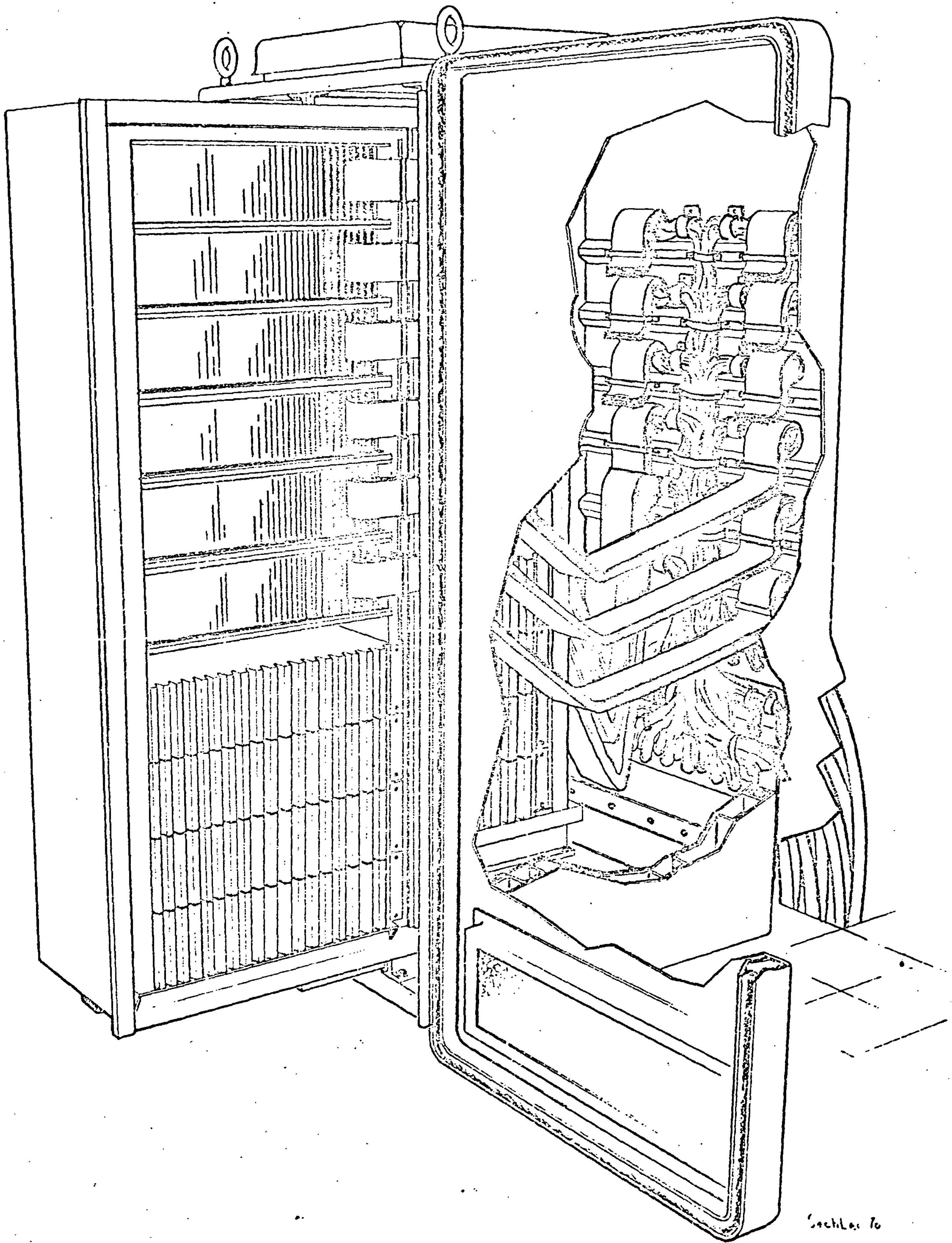


VOTER / DD TESTING

VOTER / DD EXERCISE CIRCUIT







RECOMMENDATIONS

Evaluation of Discrete System Characteristics

- As experienced in Saturn to date
- What shortcomings existed in hardware
- What shortcomings existed in software

Describe capabilities that would have been useful

Generalize from Saturn to future Saturn and other program needs

Use above results as input to specification for any new DIE

RECOMMENDATIONS FOR DIE BUILD PROJECT

Project should be multiphase with phase durations specified so that study and design effort can be in context of a specific state of technology

PHASE 1 - Prepare detailed, comprehensive spec.

- Evaluate functional performance of existing DI hardware and software.
- Evaluate functions that can't be performed because of present configuration constraints.
- Develop basis for number of discretes that must be handled.
- Develop basis for scan time and data acquisition rates.
- Consider alternate (distributed) DIE configurations.
- Select hardware technologies.
- Evaluate impact of DIE on existing hardware, software, and functional capability (technical, financial, and schedule).
- Prepare detailed program plan for PHASES 2 and 3.
- Prepare detailed cost estimate for PHASE 2.
  Prepare gross cost estimate for PHASE 3.

PHASE 2 - Prepare detailed design.

Perform circuit and logic design.
Perform mechanical design.
Prepare detailed design drawing.
Prepare detailed reliability analysis.
Prepare manuals.
Prepare test plans.
Prepare acceptance test procedures.
Prepare detailed program plan and cost estimate for PHASE 3.

PHASE 3 - Build first unit(s).